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Title:

Technical Manual
for
EPX701

RCSL Nr. 46-F 0087

A/S REGNECENTRALEN
af 1979

Keywords: RC759, Piccoline, EPX701, Technical Manual

Abstract: This paper contains all technical information about EPX701, Prom expansion module to RC759.

(26 printed pages)

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APPENDICES:

1. INTRODUCTION

The EPX701 (EXpander module) module expands the prom capacity of RC759 with 128Kbytes. This module is placed as a "baby-print" inside to the central unit in connector J13 and power supplied from this connector.

Figure 1 shows the installation of EPX701.

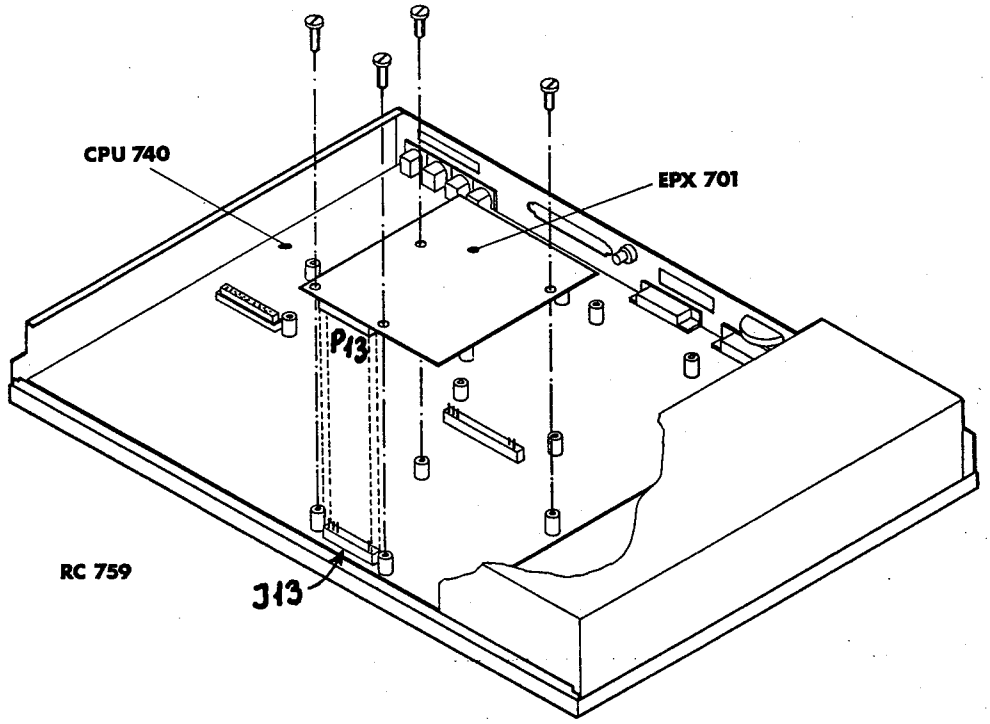


Fig. 1. Installation of EPX701

2. TECHNICAL DESCRIPTION

This module is placed in the memory address area 40000H - 60000H as shown on figure 2.

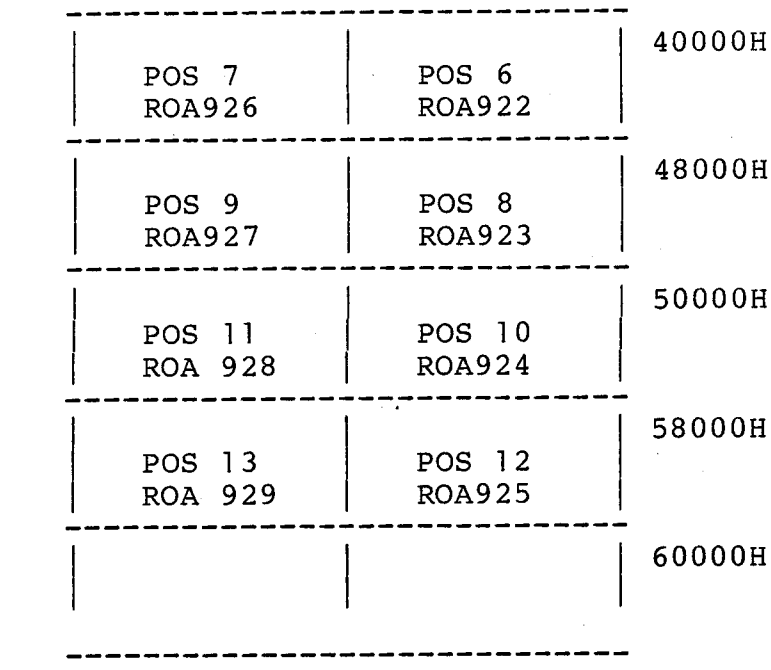


Fig. 2. Memory Address Area

The chip enable to the proms are generated by the PAL-circuit, PAT588, shown on figure 3.

```
PAL16L8                                PAL DESIGN SPECIFICATION
PAT588                                 1984.05.06,KNEH
ADDRESS DECODER TO EXP701

/RAS /CAS X2 AX15 AX14 AX16 7 8 9 GND
11 SCOL /ENBUS /POE /PCE3 /PCE2 /PCE1 /PCE0 SROW VCC

IF (VCC)    /SROW = X2+/RAS
IF (VCC)    /SCOL = X2+/CAS
IF (VCC)     PCE0 = /AX16*/AX15
IF (VCC)     PCE1 = /AX16*AX15
IF (VCC)     PCE2 = AX16*/AX15
IF (VCC)     PCE3 = AX16*AX15
IF (VCC)      POE = /X2
IF (VCC)    ENBUS = CAS*/X2

DESCRIPTION:
```

Fig. 3. PAL Design Specification

3. CHECK OUT PROCEDURE

The EPX701 is supplied with roms containg a standalone system with CCP/M + COMAL80. Use the following simple procedure to see that the module works.

a. Set default load to PROM as described in the installation manual for RC759 (PICCOLINE).

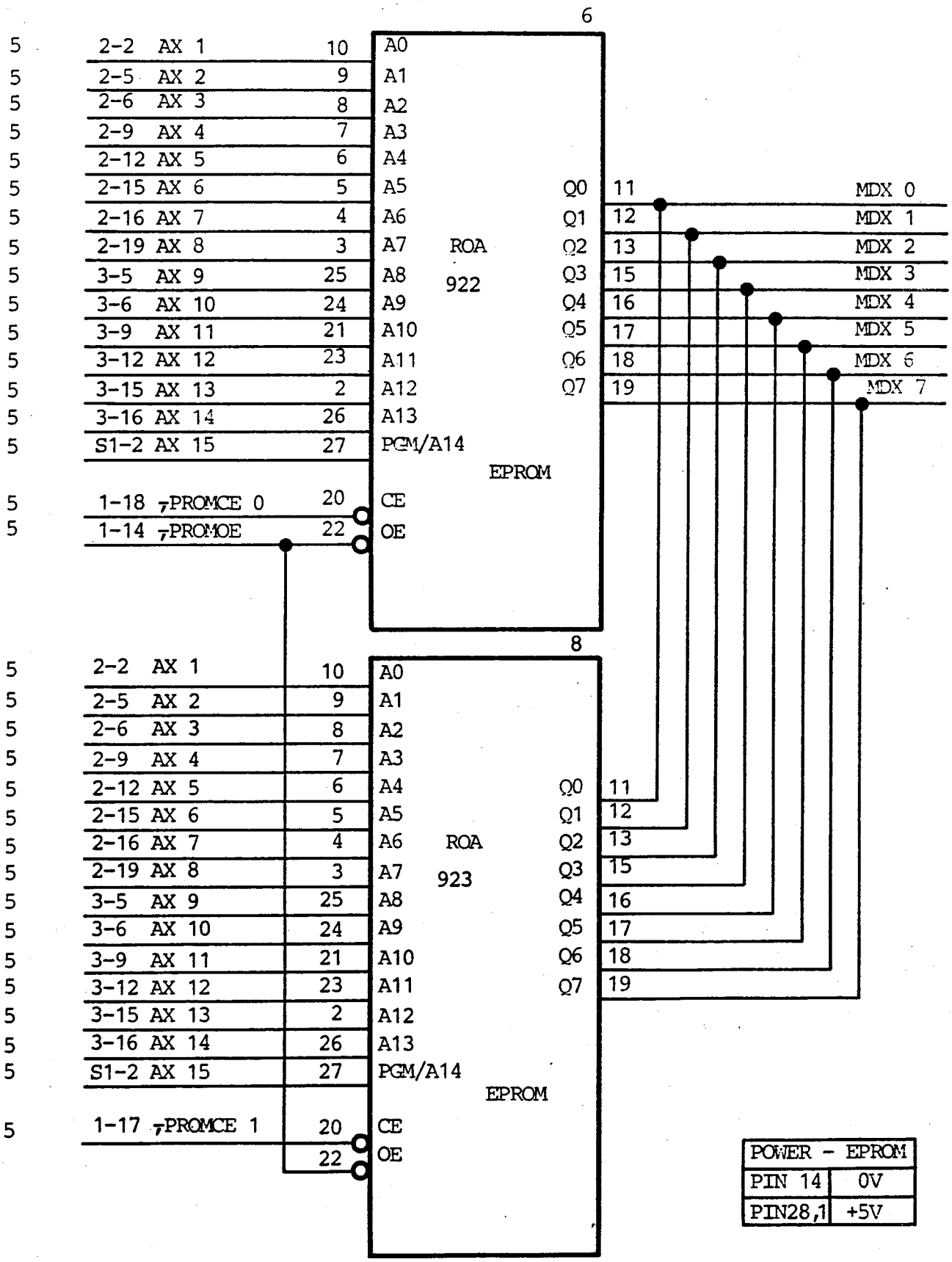
b. Push RESET on RC759. Now CCP/M is loaded from EXP701. Comal 80 is automatically started.

c. Load "sekanter".

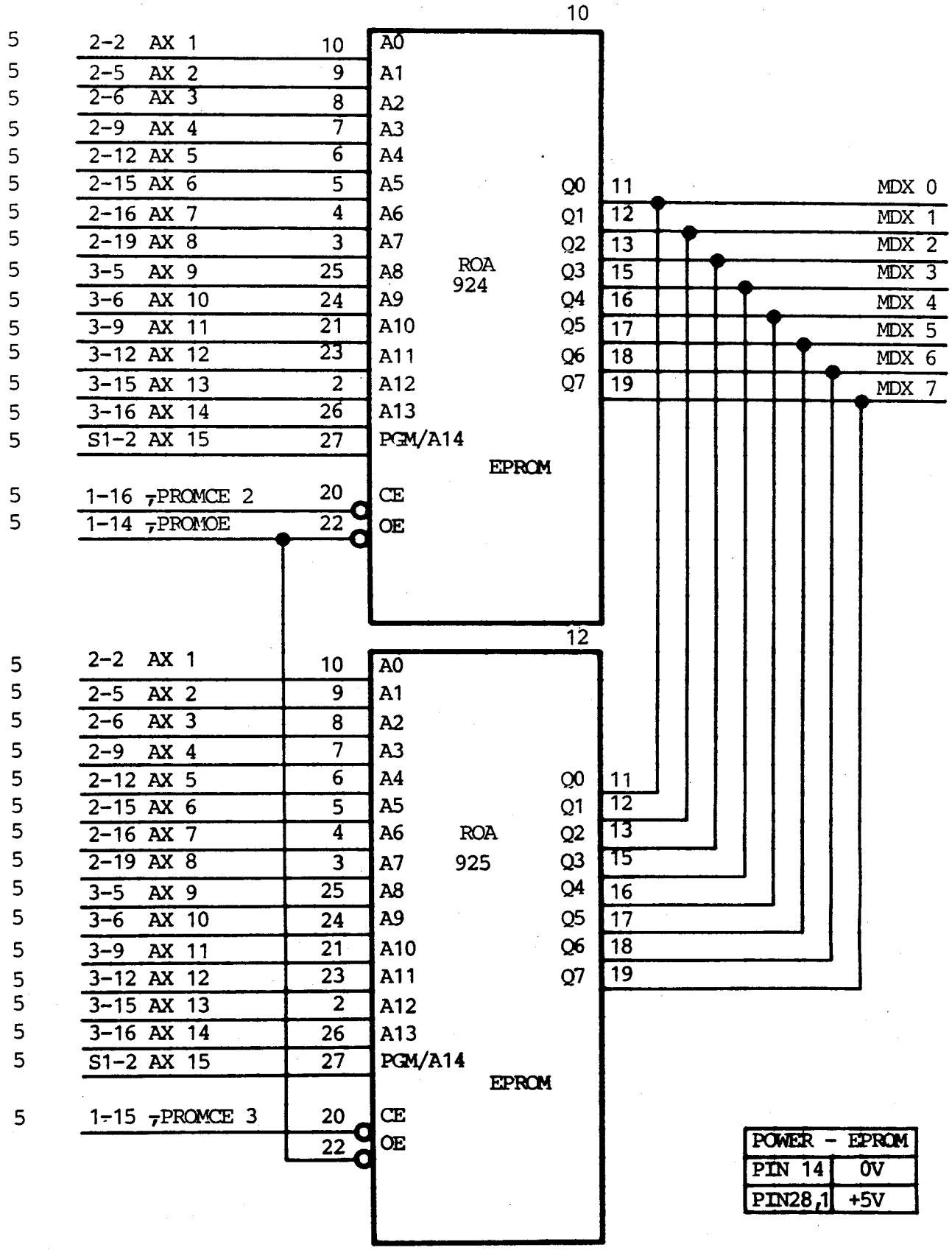
d. RUN this program.

4. Logic Diagrams

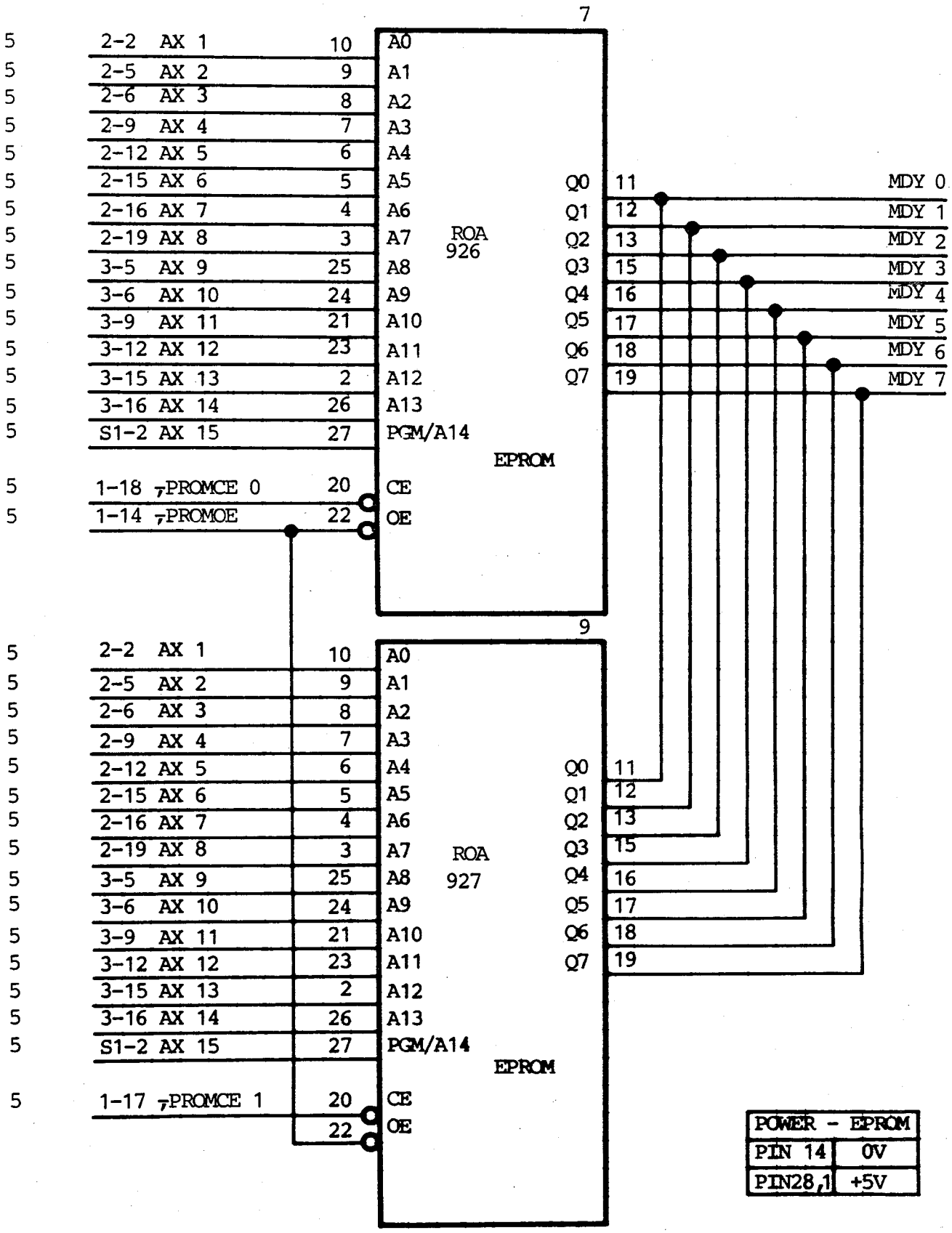
Signal Name	Destination	Description
MDX0-7	p.6	Memory Data bit X0-X7. This bits contains bit 0-7 (even byte) of the memory bus.


6
5 2-2 AX 1 10 A0
5 2-5 AX 2 9 A1
5 2-6 AX 3 8 A2
5 2-9 AX 4 7 A3
5 2-12 AX 5 6 A4
5 2-15 AX 6 5 A5
5 2-16 AX 7 4 A6
5 2-19 AX 8 3 A7
5 3-5 AX 9 25 A8
5 3-6 AX 10 24 A9
5 3-9 AX 11 21 A10
5 3-12 AX 12 23 A11
5 3-15 AX 13 2 A12
5 3-16 AX 14 26 A13
5 S1-2 AX 15 27 PGM/A14
ROA
922
EPROM
Q0 11 MDX 0
Q1 12 MDX 1
Q2 13 MDX 2
Q3 15 MDX 3
Q4 16 MDX 4
Q5 17 MDX 5
Q6 18 MDX 6
Q7 19 MDX 7
5 1-18 ₇PROMCE 0 20 CE
5 1-14 ₇PROMOE 22 OE
8
5 2-2 AX 1 10 A0
5 2-5 AX 2 9 A1
5 2-6 AX 3 8 A2
5 2-9 AX 4 7 A3
5 2-12 AX 5 6 A4
5 2-15 AX 6 5 A5
5 2-16 AX 7 4 A6
5 2-19 AX 8 3 A7
5 3-5 AX 9 25 A8
5 3-6 AX 10 24 A9
5 3-9 AX 11 21 A10
5 3-12 AX 12 23 A11
5 3-15 AX 13 2 A12
5 3-16 AX 14 26 A13
5 S1-2 AX 15 27 PGM/A14
ROA
923
EPROM
Q0 11
Q1 12
Q2 13
Q3 15
Q4 16
Q5 17
Q6 18
Q7 19
5 1-17 ₇PROMCE 1 20 CE
22 OE
84.04.09/KNEH 84.05.14/AMS
POWER - EPROM
PIN 14 0V
PIN28,1 +5V

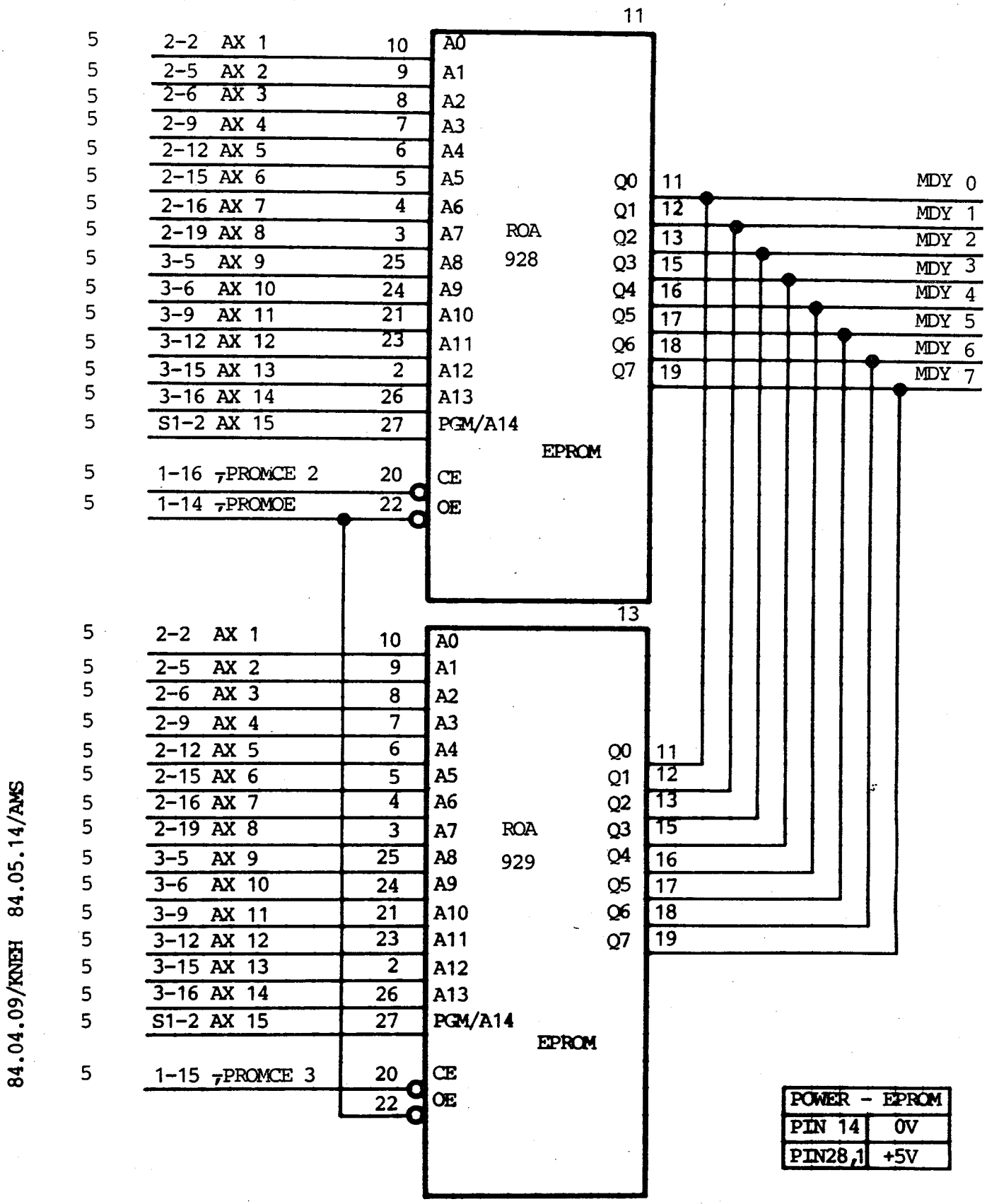
Signal Name	Destination	Description
MDX 0-7	p.6	Memory data bit X0-X7. This bits contains bit 0-7 (even byte) of the memory bus.


10
5 2-2 AX 1 10 A0
5 2-5 AX 2 9 A1
5 2-6 AX 3 8 A2
5 2-9 AX 4 7 A3
5 2-12 AX 5 6 A4
5 2-15 AX 6 5 A5
5 2-16 AX 7 4 A6
5 2-19 AX 8 3 A7
5 3-5 AX 9 25 A8
5 3-6 AX 10 24 A9
5 3-9 AX 11 21 A10
5 3-12 AX 12 23 A11
5 3-15 AX 13 2 A12
5 3-16 AX 14 26 A13
5 S1-2 AX 15 27 PGM/A14
ROA 924
EPROM
5 1-16 ₇PROMCE 2 20 CE
5 1-14 ₇PROMOE 22 OE
Q0 11 MDX 0
Q1 12 MDX 1
Q2 13 MDX 2
Q3 15 MDX 3
Q4 16 MDX 4
Q5 17 MDX 5
Q6 18 MDX 6
Q7 19 MDX 7
12
5 2-2 AX 1 10 A0
5 2-5 AX 2 9 A1
5 2-6 AX 3 8 A2
5 2-9 AX 4 7 A3
5 2-12 AX 5 6 A4
5 2-15 AX 6 5 A5
5 2-16 AX 7 4 A6
5 2-19 AX 8 3 A7
5 3-5 AX 9 25 A8
5 3-6 AX 10 24 A9
5 3-9 AX 11 21 A10
5 3-12 AX 12 23 A11
5 3-15 AX 13 2 A12
5 3-16 AX 14 26 A13
5 S1-2 AX 15 27 PGM/A14
ROA 925
EPROM
5 1-15 ₇PROMCE 3 20 CE
22 OE
Q0 11
Q1 12
Q2 13
Q3 15
Q4 16
Q5 17
Q6 18
Q7 19
POWER - EPROM
PIN 14 0V
PIN28,1 +5V
84.04.09/KNEH 84.05.14/AMS

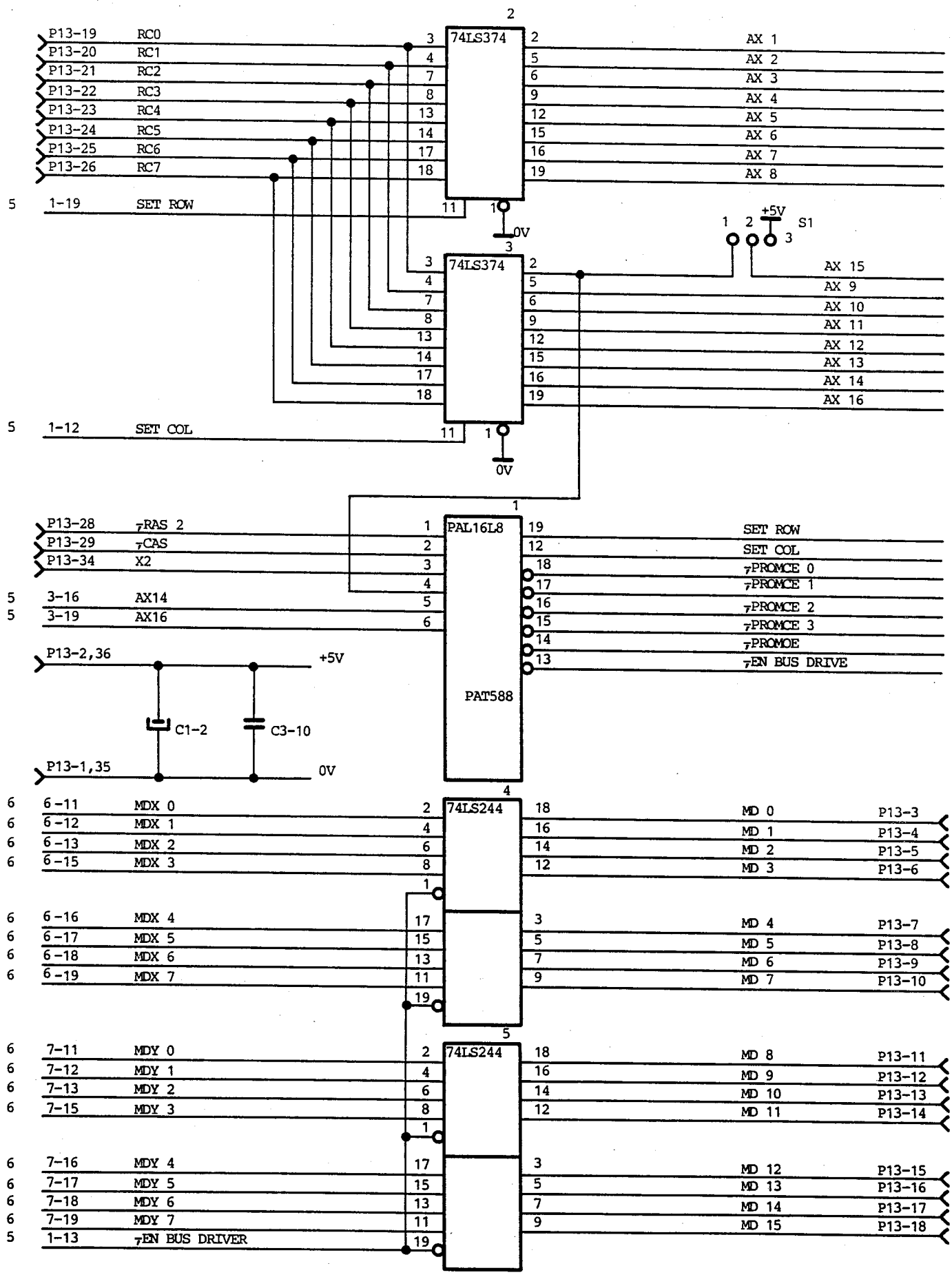
Signal Name	Destination	Description
MDY0-7	p.6	Memory data bit Y0-Y7. This bits contains bit 8-15 (ODD byte) of the memory bus.


7
5 2-2 AX 1 10 A0
5 2-5 AX 2 9 A1
5 2-6 AX 3 8 A2
5 2-9 AX 4 7 A3
5 2-12 AX 5 6 A4
5 2-15 AX 6 5 A5
5 2-16 AX 7 4 A6
5 2-19 AX 8 3 A7
5 3-5 AX 9 25 A8
5 3-6 AX 10 24 A9
5 3-9 AX 11 21 A10
5 3-12 AX 12 23 A11
5 3-15 AX 13 2 A12
5 3-16 AX 14 26 A13
5 S1-2 AX 15 27 PGM/A14
ROA 926
EPROM
5 1-18 ₇PROMCE 0 20 CE
5 1-14 ₇PROMOE 22 OE
Q0 11 MDY 0
Q1 12 MDY 1
Q2 13 MDY 2
Q3 15 MDY 3
Q4 16 MDY 4
Q5 17 MDY 5
Q6 18 MDY 6
Q7 19 MDY 7
9
5 2-2 AX 1 10 A0
5 2-5 AX 2 9 A1
5 2-6 AX 3 8 A2
5 2-9 AX 4 7 A3
5 2-12 AX 5 6 A4
5 2-15 AX 6 5 A5
5 2-16 AX 7 4 A6
5 2-19 AX 8 3 A7
5 3-5 AX 9 25 A8
5 3-6 AX 10 24 A9
5 3-9 AX 11 21 A10
5 3-12 AX 12 23 A11
5 3-15 AX 13 2 A12
5 3-16 AX 14 26 A13
5 S1-2 AX 15 27 PGM/A14
ROA 927
EPROM
5 1-17 ₇PROMCE 1 20 CE
22 OE
Q0 11
Q1 12
Q2 13
Q3 15
Q4 16
Q5 17
Q6 18
Q7 19
84.04.09/KNEH 84.05.14/AMS
POWER - EPROM
PIN 14 0V
PIN28,1 +5V

Signal Name	Destination	Description
MDY 0-7	p.6	Memory data bit Y0-Y7. This bits contains bit 8-15 (ODD byte) of the memory bus.

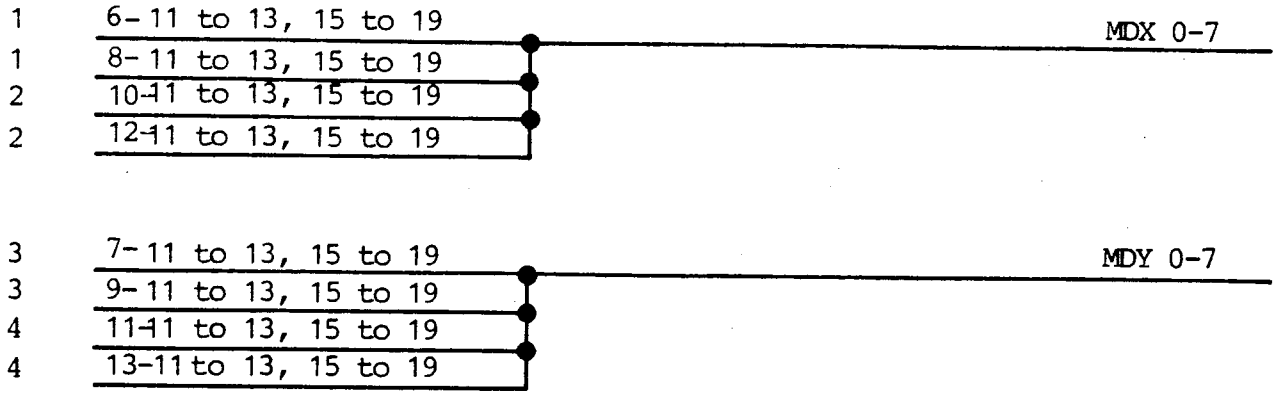

11
5 2-2 AX 1 10 A0
5 2-5 AX 2 9 A1
5 2-6 AX 3 8 A2
5 2-9 AX 4 7 A3
5 2-12 AX 5 6 A4
5 2-15 AX 6 5 A5
5 2-16 AX 7 4 A6
5 2-19 AX 8 3 A7
5 3-5 AX 9 25 A8
5 3-6 AX 10 24 A9
5 3-9 AX 11 21 A10
5 3-12 AX 12 23 A11
5 3-15 AX 13 2 A12
5 3-16 AX 14 26 A13
5 S1-2 AX 15 27 PGM/A14
ROA 928
EPROM
5 1-16 ¬PROMCE 2 20 CE
5 1-14 ¬PROMOE 22 OE
Q0 11 MDY 0
Q1 12 MDY 1
Q2 13 MDY 2
Q3 15 MDY 3
Q4 16 MDY 4
Q5 17 MDY 5
Q6 18 MDY 6
Q7 19 MDY 7
13
5 2-2 AX 1 10 A0
5 2-5 AX 2 9 A1
5 2-6 AX 3 8 A2
5 2-9 AX 4 7 A3
5 2-12 AX 5 6 A4
5 2-15 AX 6 5 A5
5 2-16 AX 7 4 A6
5 2-19 AX 8 3 A7
5 3-5 AX 9 25 A8
5 3-6 AX 10 24 A9
5 3-9 AX 11 21 A10
5 3-12 AX 12 23 A11
5 3-15 AX 13 2 A12
5 3-16 AX 14 26 A13
5 S1-2 AX 15 27 PGM/A14
ROA 929
EPROM
5 1-15 ¬PROMCE 3 20 CE
22 OE
Q0 11
Q1 12
Q2 13
Q3 15
Q4 16
Q5 17
Q6 18
Q7 19
POWER - EPROM
PIN 14 0V
PIN28,1 +5V
84.04.09/KNEH 84.05.14/AMS

Signal name	Destination	Description
AX 1-15	p.1 p.2 p.3 p.4	Address bit 1-15. Bit 1 is the least significant bit. This address is derived from the multiplexed row/COL address using RAS/CAS signals.
/EN BUS DRIVE	p.5	ENables the memory data bus drivers to the CPU740 memory bus (MD0-15). True if CAS=1 and X2=0.
MD0-15	p.13	CPU740Memory Data bus bit 0-15.
/PROM CE 0	p.1 p.3	PROM Chip Enable. Address 40000H - 47FFFH.
/PROMCE1	p.1 p.3	Prom Chip Enable Address 48000H-4FFFFH.
/PROMCE 2	p.2 p.4	Prom Chip Enable Address 50000H-57FFFH.
/PROMCE3	p.2 p.4	Prom Chip Enable Address 58000H - 5FFFFH
/PROM OE	p.1 p.2 p.3 p.4	PROM output Enable True if X2=0.
SET COL	p.5	SET COLumn part of the address The COL register is set on the leading edge of /CAS if X2=0.
SET ROW	p.5	SET ROW part of the address. The ROW register is set on the leading edge of /RAS if X2=0.



84.04.09/KNEH 84.05.16AMS

Signal Name	Destination	Description
MDX 0-7	p.5	Memory data bit X0-X7. This bits contains bit 0-7 (even byte) of the memory bus.
MDY 0-7	p.5	Memory data bit Y0-Y7. This bits contains bit 8-15 (ODD byte) of the memory bus.



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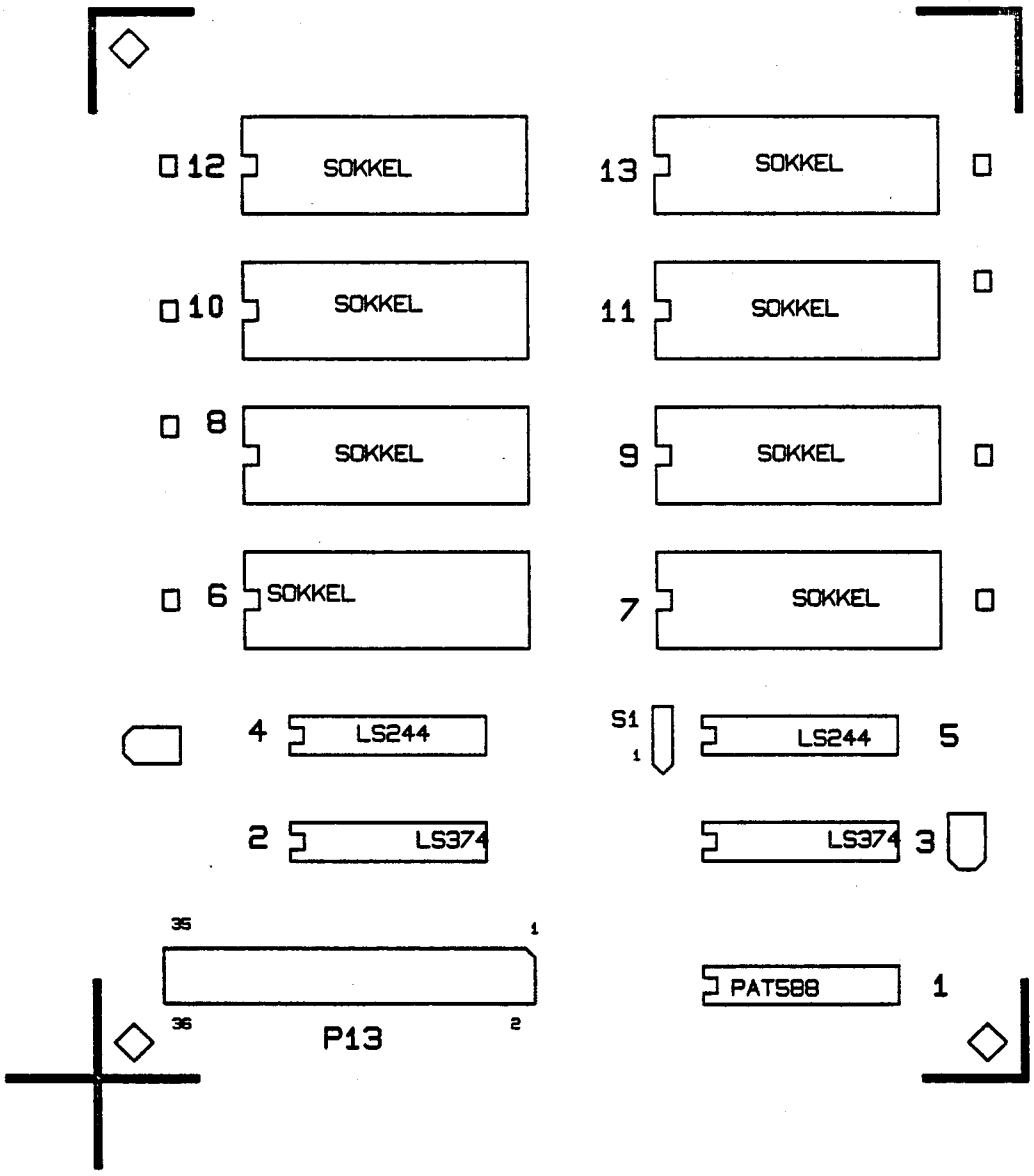

PCB126 COMPONENT NOTATION

Fig. 4. Assembly Drawing

Pin number	Signal name
1	ov
2	+5V
3	MD0
4	-1
5	-2
6	-3
7	-4
8	-5
9	-6
10	-7
11	-8
12	-9
13	-10
14	-11
15	-12
16	-13
17	-14
18	-15
19	RC0
20	-1
21	-2
22	-3
23	-4
24	-5
25	-6
26	-7
27	-8
28	/RAS2
29	/CAS
30	/WEHI
31	/WEL0
32	X0
33	X1
34	X2
35	Ov
36	+5V

Fig. 5. Plug List P13

A. INDICES

A.

A.1 Survey of Figures

A.1

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