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Author: Knud Erik Hansen

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RC759
CENTRAL PROCESSING UNIT
Technical Manual

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Abstract: This paper contains all the technical information necessary to service the RC759 Piccoline Central Processing Unit.

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1. INTRODUCTION

This paper contains all technical information about the moduls in RC759, central processing units. These modules are:

CPU740/741 Processor board

POW749	Power supply
LSU701	Speaker/battery
CBL769	Volumen control
IDP703	Power indicator
CBL770	reset button

On figure 1 and 2 are shown the internal module interconnection.

The architecture of CPU740 is described in RCSL: 52AA 1227 RC759, CPU Board, Reference Manual.

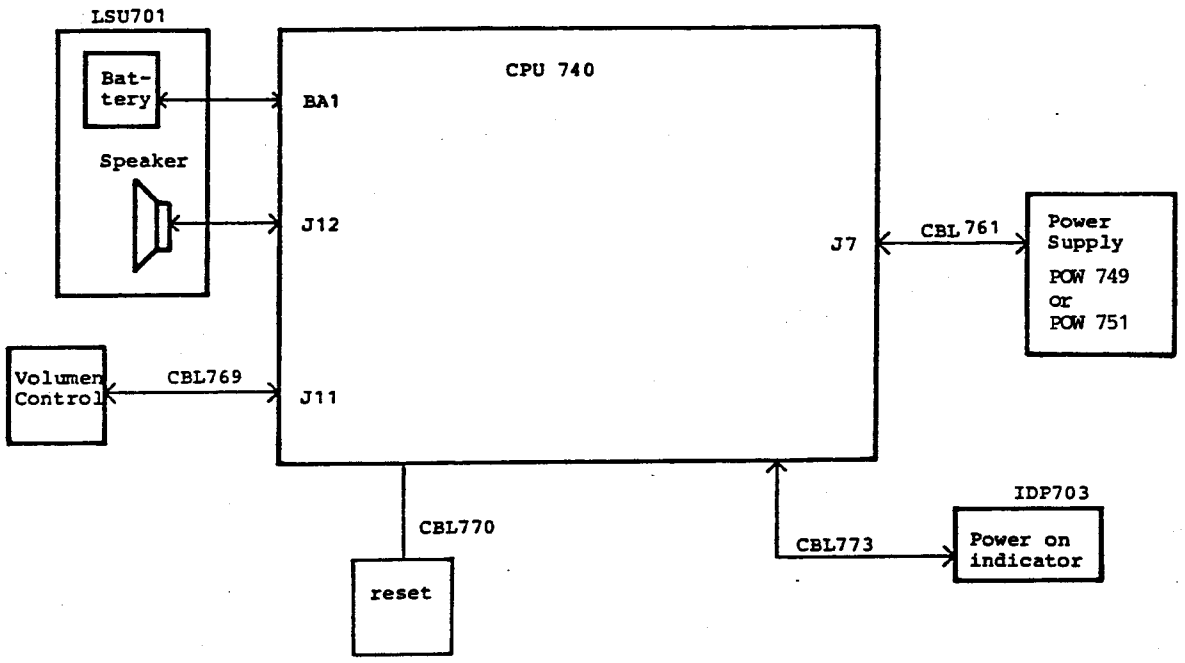


Fig. 1. RC759 Internal Cabling

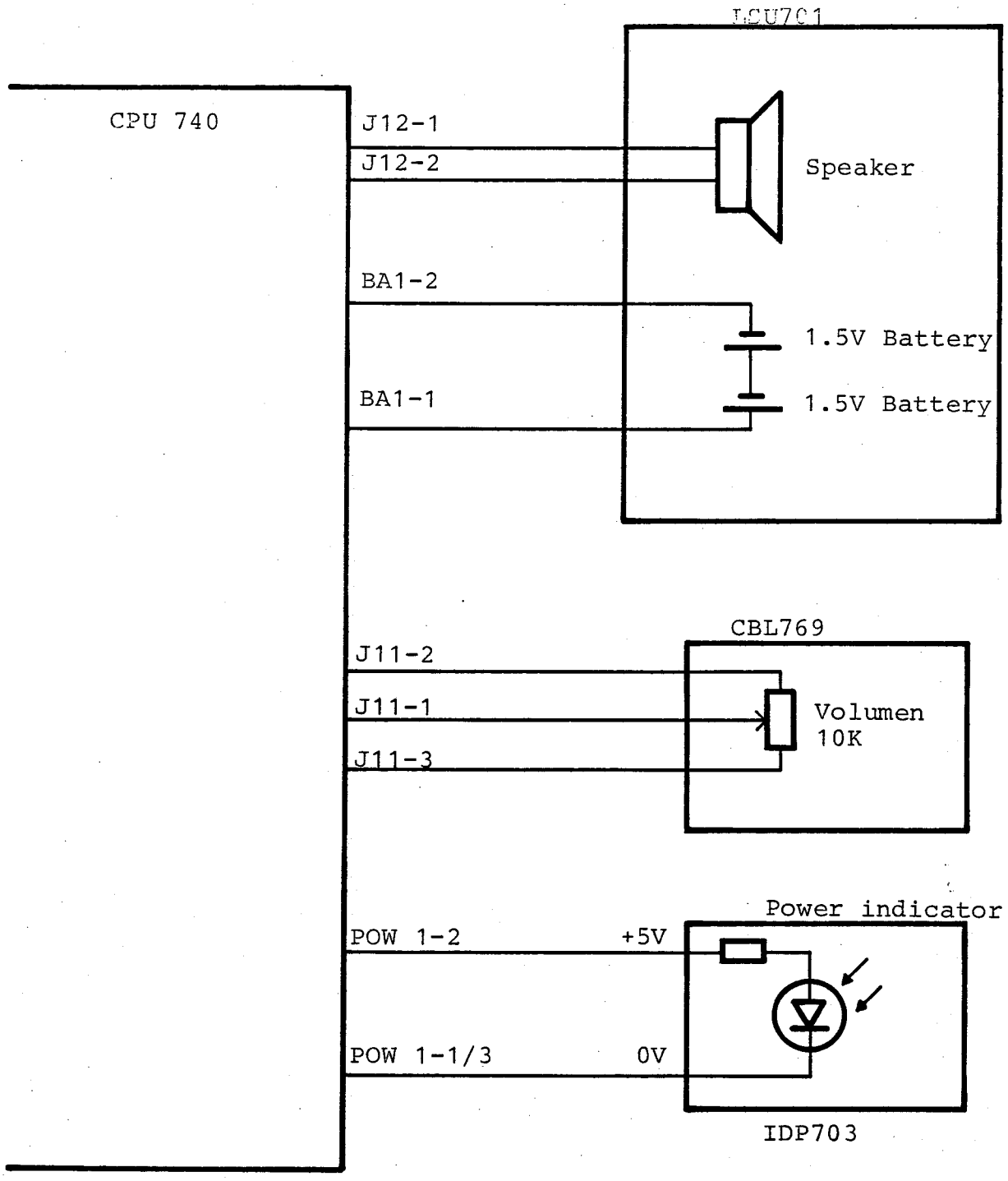


Fig. 2. Module Interconnection

2. STRAP INFORMATION (CPU740) 2.

STRAP	FUNCTION
W2 (diag. p.1)	not used
W1 (diag. p. 2)	
1-2	Select 32 K x 8 Eproms (27256)
2-3	Select 8Kx8 (2764) or 16Kx8 (27128) eproms
W3 (diag. p.15)	
IN	The built in tests writes error-messages on a TTY-terminal connected to iSBX 351 communication module.
*OUT	not use of iSBX351 by built in tests.
W5 (diag. p.19)	Selects second source clock generator.
*1-8 IN *2-7 OUT *3-6 OUT *4-5 OUT	Select MM58167 clock circuit.
1-8 OUT 2-7 IN 3-6 IN 4-5 IN	Select CDP1879 clock circuit.
W7 (diag. p.22)	Cassette data out voltage select
*1-4 IN *2-3 OUT	DATA out 0.68V
1-4 OUT 2-3 IN	DATA OUT 0.075V
W6 (diag. p.24)	not used
W4 (diag. p.29)	
*IN	iSBX without DMA channel
OUT	iSBX with DMA channel
W6 (diag.p.24)	
*1-4 IN 2-3 OUT	In the used power supply RGM703, or RGM702 with FCO 19-050.
W10(diag.p.21)	
*1-4 IN *2-3 OUT	Power supply RGM703, or RGM702 with FCO 19-050.
1-4 OUT 2-3 IN	RGM702 without FCO 19-050

*means factory set

3. PAL CIRCUITS


```
PAL16R8A                          PAL DESIGN SPECIFIKATION
PAT022                             PKA 830721
          PIXEL MEMORY CONTROLLER

CP50 CRTSEL /REFR /WELO /WEHI CNTO CNT1
CNT2 CNT3 GND /E /PIXS1 MAINCOL /MAINACC
/GPIX PIXCASEN /PIXWELO /PIXWEHI
/PIXOE VCC

PIXS1     := CNTO*/CNT1*/CNT2*/CNT3*CRTSEL +
             CNTO*/CNT1*/CNT2*CNT3 +
             PIXS1*/CNTO +
             PIXS1*/CNT2
MAINACC   := CNTO*/CNT1*/CNT2*/CNT3*CRTSEL +
             MAINACC*/CNT1 +
             MAINACC*/CNT2
GPIX      := CNTO*/CNT1*/CNT2*/CNT3*CRTSEL*/REFR +
             GPIX*/CNTO +
             GPIX*/CNT1 +
             GPIX*/CNT2
/PIXCASEN:= /GPIX*/CNT3 +
             /CNT2*/CNT1 +
             /CNT2*/CNTO +
             CNTO*CNT1*CNT2
PIXWELO   := WELO*MAINACC*/REFR
PIXWEHI   := WEHI*MAINACC*/REFR
PIXOE     := CNT3 + MAINACC*/PIXWELO*/PIXWEHI*/WELO*/WEHI
/MAINCOL:= /MAINACC + CNTO*CNT1*CNT2

DESCRIPTION:
```

Fig. 3. PAT022

```
PAL16R8A                              PAL DESIGN SPECIFICATION
PAT063 erstatter PAT023                 PKA 840809
                  CRT CLOCK CONTROL

CP50 CNT0 CNT1 CNT2 CNT3 CSYNC /GRAPH /CHOLD NC GND
/OE /A /B /C RCLK CCLK CSYND /LDCNT CNTEN VCC

A         := /B*/C*/RCLK
           +  B* C*/RCLK
           + /B* C* RCLK
           +  B*/C* RCLK

B         :=  A*/C*/RCLK
           +  A* C* RCLK
           + /A* B

C         := /A* B*/RCLK
           +  C*/RCLK
           +  C*/B
           +  C* A

/RCLK     := /A*/B*/C
           + /RCLK* A
           + /RCLK* B
           + /RCLK*/C

/CCLK     :=  CCLK +/CNT3 +/CNT2 +/CNT1 +/CNT0 + CHOLD

/CSYND    := /CSYNC
           + /CSYND* RCLK
           + /CSYND*/C
           + /CSYND* B

/CNTEN    := CSYND* CNT1* CNT2* CNT3* B
           + CSYND* CNT1* CNT2* CNT3*/C
           + CSYND* CNT1* CNT2* CNT3* RCLK
           + CHOLD* CNT1* CNT2* CNT3* B
           +/CNTEN* CNT1* CNT2* CNT3* B
           + CHOLD* CNT1* CNT2* CNT3*/C
           +/CNTEN* CNT1* CNT2* CNT3*/C
           + CHOLD* CNT1* CNT2* CNT3* RCLK

LDCNT     := /LDCNT* CNT1* CNT2* CNT3*/CSYND*/GRAPH*/CHOLD

DESCRIPTION:
```

Fig. 4. PAT063

```
PAL16R8A                    PAL DESIGN SPECIFIKATION
PAT024                        PKA 830728
          CRT DOT GENERATOR

CP50 LOAD /GRAPH CRVVD BLANK EDOT ODOT PM15 ATTR4 GND
/OE DOT NC /WRTDS /ATTB4 PHASE /PALLRD LDCOL /COLSEL4 VCC

/PHASE   := /LOAD*PHASE +
             LOAD*/GRAPH +
             LOAD*/ATTR4

/DOT     :=    BLANK*/GRAPH*/CRVVD
           + /BLANK*PHASE*GRAPH*/EDOT
           + /BLANK*PHASE*/GRAPH*/CRVVD*/EDOT
           + /BLANK*PHASE*/GRAPH*CRVVD*EDOT
           + /BLANK*/PHASE*GRAPH*/ATTB4*/ODOT
           + /BLANK*/PHASE*GRAPH*ATTB4*/DOT
           + /BLANK*/PHASE*/GRAPH*/CRVVD*/ODOT
           + /BLANK*/PHASE*/GRAPH*CRVVD*ODOT

ATTB4    := /LOAD*ATTB4 +
             LOAD*ATTR4

PALLRD   :=  GRAPH*ATTB4 +
             LOAD +
             PALLRD*/LDCOL

/LDCOL   :=  LDCOL +
            /LDCOL*/GRAPH*/PALLRD +
            /LDCOL*/ATTB4*/PALLRD +
             GRAPH*ATTB4*/PHASE

COLSEL4  :=  GRAPH*ATTR4* LOAD*PM15 +
             PALLRD*GRAPH*ATTB4*/LOAD*ODOT +
             /GRAPH*ATTR4* LOAD +
             PALLRD*/GRAPH*ATTB4*/LOAD

WRTDS    :=  LOAD + PALLRD


DESCRIPTION:
```

Fig. 5. PAT024

```
PAL16L8                              PAL DESIGN SPECIFICATION
PAT579                               1984.05.06;KNEH
MEMORY ADDRESS DECODER TO CPU740

A17 A18 A19 RASEN /REFR A16 A15 A14 A13 GND
11 X2 X1 XO /MID1 /MIDO /RAS2 /RAS1 /RASO VCC

IF (VCC)    RASO = /A17*/A18*/A19*RASEN*/REFR+RASEN*REFR
IF (VCC)    RAS1 = A17*/A18*/A19*RASEN*/REFR+RASEN*REFR
IF (VCC)    RAS2 = /A17*A18*/A19*RASEN*/REFR
                   +A17*A18*/A19*RASEN*/REFR
                   +/A17*/A18*A19*RASEN*/REFR
                   +A17*/A18*A19*RASEN*/REFR
                   +RASEN*REFR
IF (VCC)    MID1 = /X1
IF (VCC)    MIDO = /XO
IF (VCC)     /X2 =/A19*A18*/A17+/A19*A18*A17

DESCRIPTION:

 XO   X1  !   FUNCTION
-------------------------------------------
  1    1  ! NO MEMORY EXPANSION
  1    0  ! 128 KBYTES EXPANSION
  0    1  ! 256 KBYTES EXPANSION
  0    0  ! 512 KBYTES EXPANSION
-------------------------------------------
```

Fig. 6. PAT579

```
PAL16L8                          PAL DESIGN SPECIFICATION
PAT578                           1984.02.06,KNEH
ISBX BUS CONTROLLER TO CPU740.

MDR@T MINTR0 MINTR1 /MPST A4 A5 /PCS6 /DEN /IOWR GND
/IORD TC EDMA DMA0 INT1 INT0 /MDACK /MCS1 /MCS0 VCC

IF (VCC)   MCS0 = PCS6*/A4*/A5
IF (VCC)   MCS1 = PCS6*/A5*A4
IF (VCC)  MDACK = PCS6*A5*/A4*DEN
IF (VCC)  /INT0 = /MPST+/MINTR0
IF (VCC)  /INT1 = /MPST+/MINTR1
IF (VCC)  /DMA0 = /EDMA+/MPST+/MDR@T
IF (VCC)    /TC = /PCS6+/A4+/A5+/DEN

DESCRIPTION:

MODUL SELECT /MCS0=0 FOR IOBASE+30X
MODUL SELECT /MCS1=0 FOR IOBASE+31X
WHERE X=0,2,4,6,8,A,C,E.
DMA ACK IS GENERATED BY I/O INSTRUCTION TO IOBASE+320.
TC IS GENERATED BY I/O INSTRUCTION TO IOBASE+330.
```

Fig. 7. PAT578

```
PAL16R8                     PAL DESIGN SPECIFICATION
PAT587                      1984.03.29;KNEH
MAIN MEMORY CONTROLLER.

CPUCLK ALE MS0 MS1 MS2 REFREQ NC /MAINACC /RESET GND
/OE /ALED MAINM CRTSEL RASEN /REFR /CAS COLSEL MRDY VCC

ALED := ALE
/MAINM := CAS + MAINACC
          +/MAINM*MRDY*/ALE*/REFREQ + /MAINM*MRDY*ALED*/REFREQ
          +/MAINM*MS0*/REFREQ + /MAINM*/MS1*/REFREQ
          +/MAINM*RASEN
/CRTSEL:= MAINACC + RESET
          +/CRTSEL*MRDY*/ALE*/REFREQ + /CRTSEL*MRDY*ALED*/REFREQ
          +/CRTSEL*/MS0*/REFREQ + /CRTSEL*RASEN
          +/CRTSEL*REFREQ*/REFR
/RASEN := CAS + MAINACC
          +/RASEN*MRDY*/ALE*/REFREQ + /RASEN*MRDY*ALED*/REFREQ
          +/RASEN*/MS0*/MS1*/REFREQ + /RASEN*REFREQ*/REFR
REFR   := REFR*/MAINACC*/RESET
          +REFREQ*/RASEN*/MAINM*/CRTSEL*/MAINACC
/COLSEL:= CAS + /COLSEL*MRDY*/ALE + /COLSEL*MRDY*ALED
          +/COLSEL*/MS0*/MS1 + /COLSEL*MS0
          +/COLSEL*RASEN + /COLSEL*REFREQ
          +/COLSEL*REFR
CAS    := /CAS*RASEN*/REFR*/CRTSEL*MS2*MS1
          +RESET
/MRDY  := ALE*/ALED*REFR*MS1*MS2 + ALE*/ALED*REFREQ*MS1*MS2
          +ALE*/ALED*MS0
          +/MRDY*REFR + /MRDY*REFREQ + /MRDY*MS0*/MAINACC

DESCRIPTION:
```

Fig. 8. PAT587

```
PAL16R8                         PAL DESIGN SPECIFICATION
PAT594                          KNEH 840507
BUS ARBITER

CPUCK /NETH CRTH /87H HLDA LS /CLREF /MACC DRQ GND
/E NETA CRTA /DRQD HOLD /NETAD  REFRQ /MACCDD /MACCD VCC

/NETA   := /NETH+/HLDA+CRTA+DRQD+/HOLD
/CRTA   := /CRTH+/HLDA+DRQD+/HOLD+NETH*/CRTA+NETA
/HOLD   :=/NETH*/CRTH+/HOLD*DRQD+NETAD*/NETH+/HOLD*DRQ+/NETAD*DRQD*/CRTH
/REFRQ  :=/LS+CLREF
MACCD   :=MACC*/MACCD*/MACCDD
MACCDD  :=MACCD
DRQD    :=NETA*DRQ+CRTA*DRQ+DRQ*DRQD+/HOLD*HLDA+DRQD*HLDA
NETAD   :=NETA+NETAD*DRQD

DESCRIPTION:
```

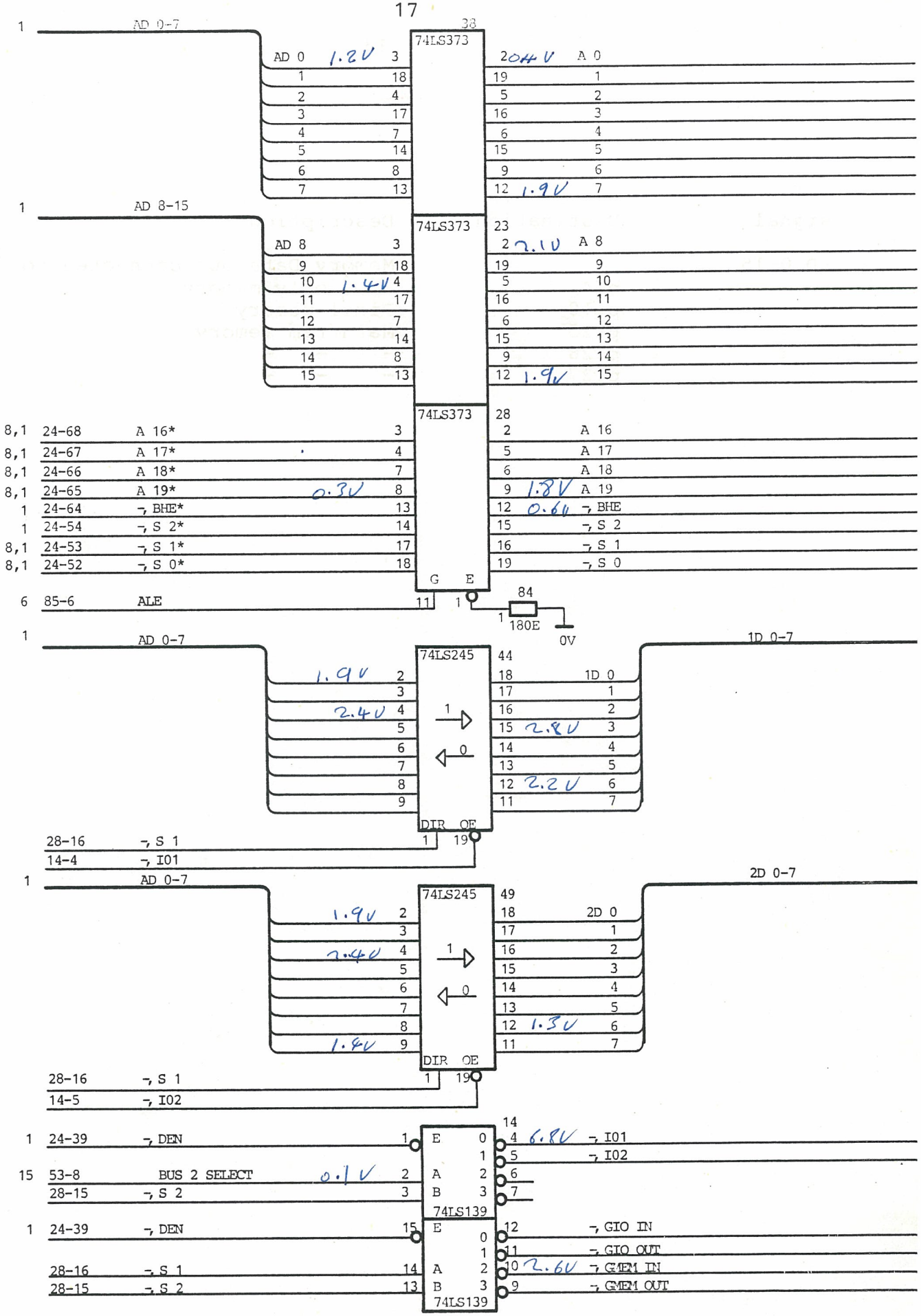
Fig. 9. PAT594

```
PAL16L8                         PAL DESIGN SPECIFICATION
PAT595                          1984.12.17,KNEH
MEMORY ADDRESS DECLDER

/S2 A14 A15 A16 A17 A18 A19 A0 /BHE GND
RASEN RC8 /S1 COLSEL /WEHI /WELO MS2 MS1 MS0 VCC

IF (VCC)  /MS0 = /A19+/A18+A17+/A16+A15+S2
IF (VCC)  /MS1 = A19*A18*A17*A16 + S2
IF (VCC)  /MS2 = A19*A18*A17*A16*A15+S2
IF (VCC)  WELO = /S2*/S1*/A0
IF (VCC)  WEHI = /S2*/S1*BHE
IF (VCC)  /RC8 = /COLSEL*/A18+COLSEL*/A17

DESCRIPTION:
```

Fig. 10. PAT595

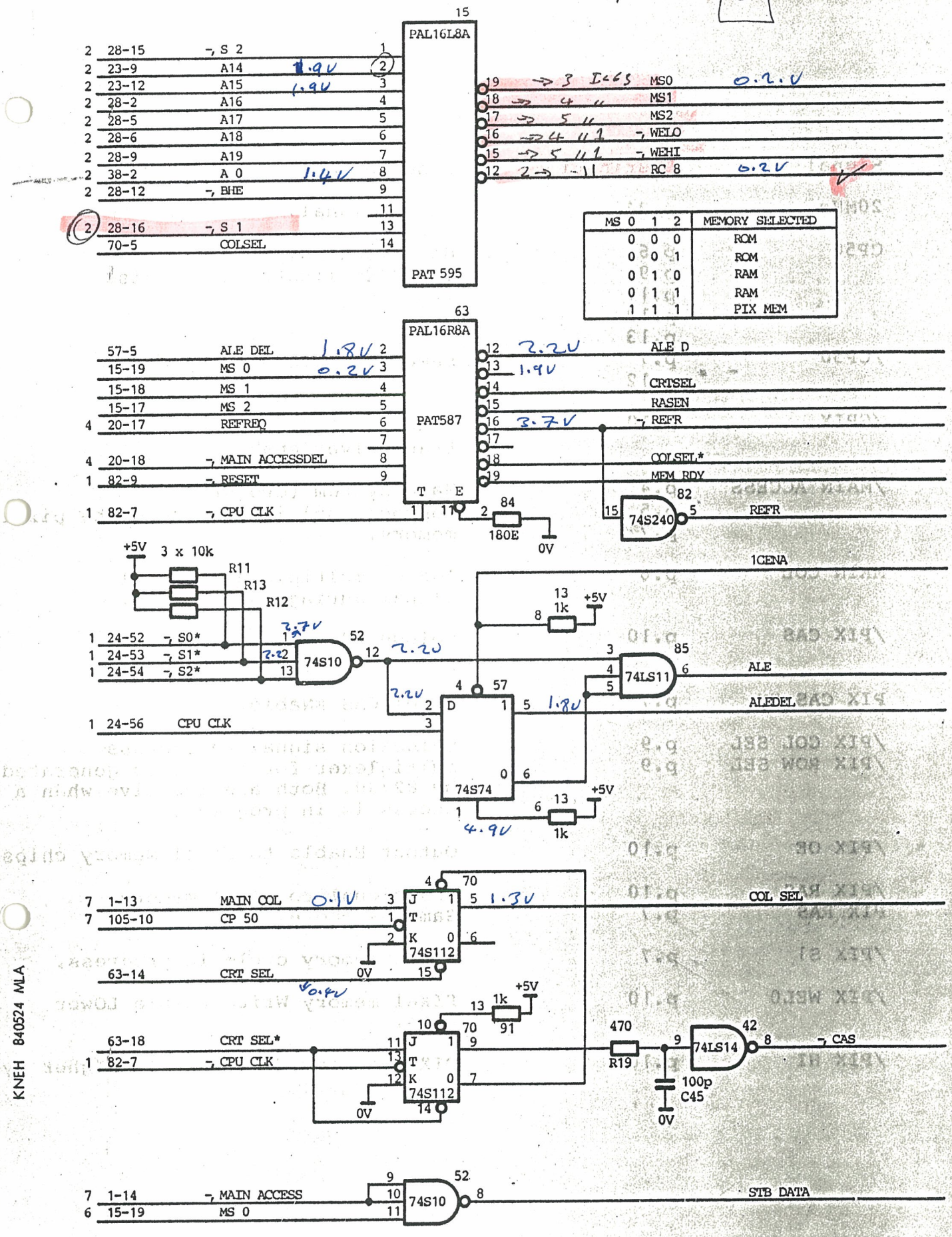
4. LOGIC DIAGRAMS

Signal	Destination	Description
AD 0-15	p.2 p.3 p.8 p.23 (wired or)	Multiplexed address/data bus common for the coprocessors. ADo is least and AD15 the most significant bit.
A16*-A19*	p.2 p.8 (wired or) p.23 (wired or)	The four most significant address bits.
/BHE*	p.2 p.23	Byte High Enable. Low when data is transferred on AD 8-15.
CAS DATA OUT	p.22	CASsette DATA OUT.
CPU CLK	p.6 p.8 p.23	CPU CLocK (6MHZ).Timing signal for logic running synchronously with the CPU.
/CPU CLK	p.6 p.21	Same as above.
/DEN	p.2 p.9 p.8 (wired or) p.23 (wired or) p.28 p.30	Data ENable. Used to enable the data buffers. DEN is active low during each memory and I/O access. /DEN is high whenever DT/R changes state.
DT//R	p.30	Data Transmit/Receive controls the direction of data flow througt the external data bus transceivers.
HLDA	p.4	HoLD Acknowledge from 80186 as response to a HOLD request.
/INTAO	p.14 p.15	Interrupt Acknowledge to the 8259 interrupt controller.
QS 0,1	p.23 (wired or)	80186 Queue status QS1 QS0 Queue Operation 0 0 No operation 0 1 First opcode byte fetched from the queue. 1 0 Subsequent byte fetched from the queue. 1 1 Empty the queue
RESET	p.8 p.15 p.23 p.30	Reset output indicates that the 80186 cpu is being reset, and can be used as system reset
/RESET	p.5 p.6 p.18 p.29	Same as above
/S0*-/S2*	p.2 p.8 (wired or) p.23	Bus status signals indicating the kind of bus cycle being performed: /S2 1 0 Bus cycle 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Halt 1 0 0 Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive
T1	p.20	output from Timer 1.
/PCS0	p.14	Peripheral Chip Select 0 Iobase + 0 H
/PCS1	p.15 p.21	Iobase + 80H. Enables the NVM
/PCS2	p.23	Iobase + 100H. Enables the local area network controller.
/PCS3	p.12	Iobase +180H. Enable the colour palet.
/PCS4	p.9	Iobase + 200H.
/PCS5	p.30 p.15	Iobase + 280H. Enable the expansion bus (DPA connection).
/PCS6	p.28	Iobase + 300H. Enable the iSBX bus.

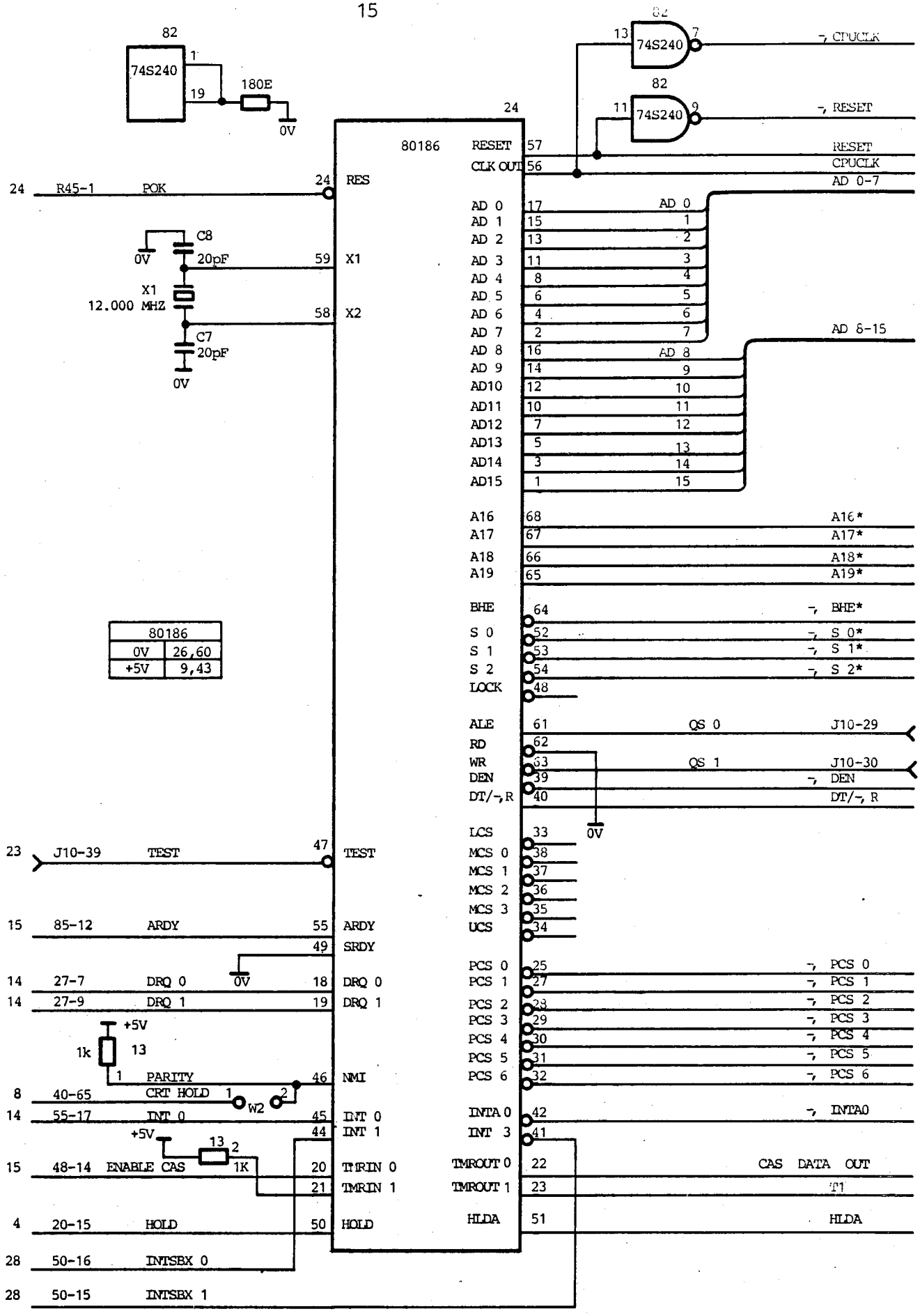


KNEH 840524 MLA

Signal	Destination	Description
MD 0-15		Memory Data bus connected to
	p.4	Read only memory
	p.10	Pixel memory
	p.25	Main ram memory
	p.26	- - -
	p.27	- - -

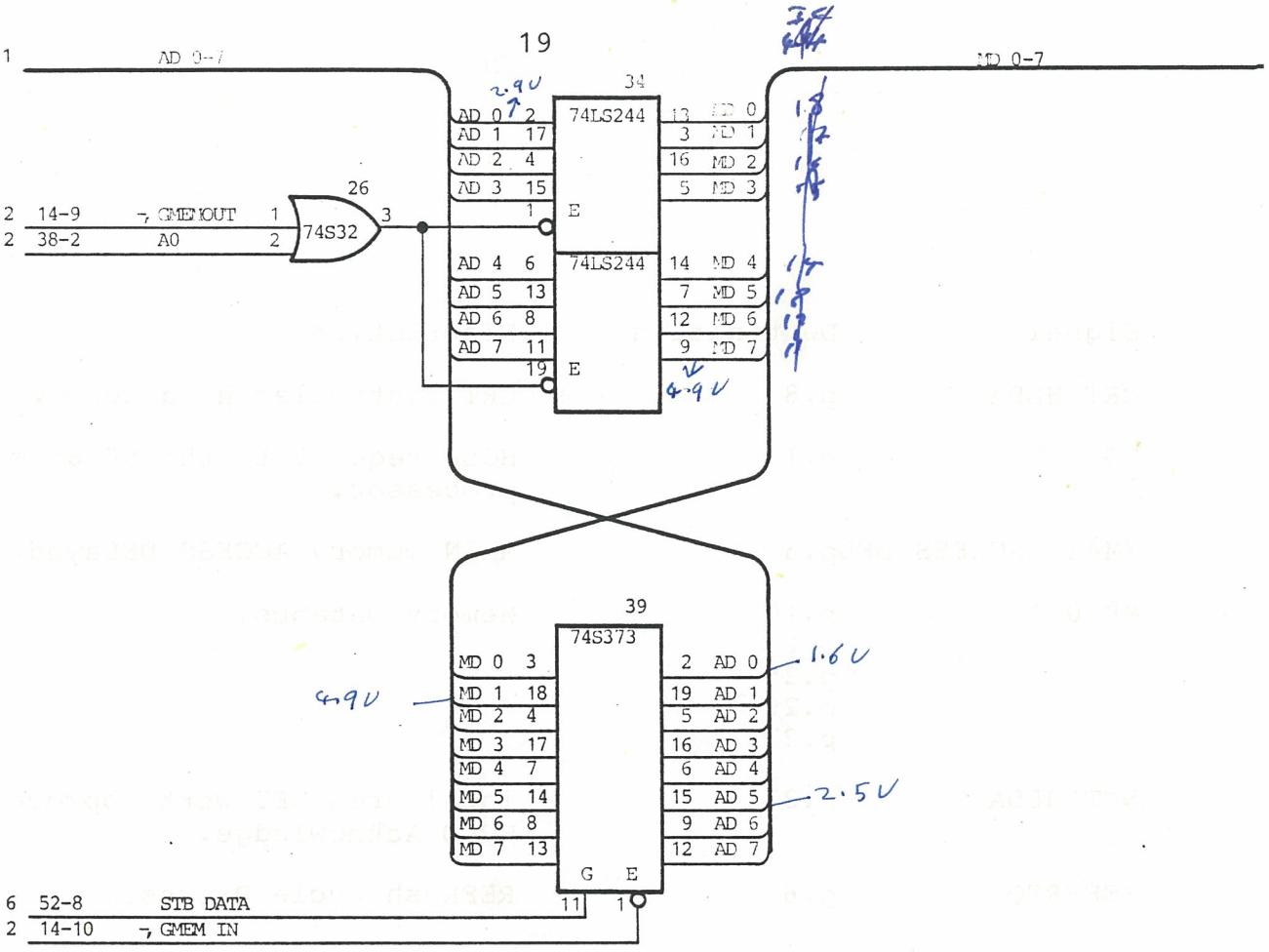


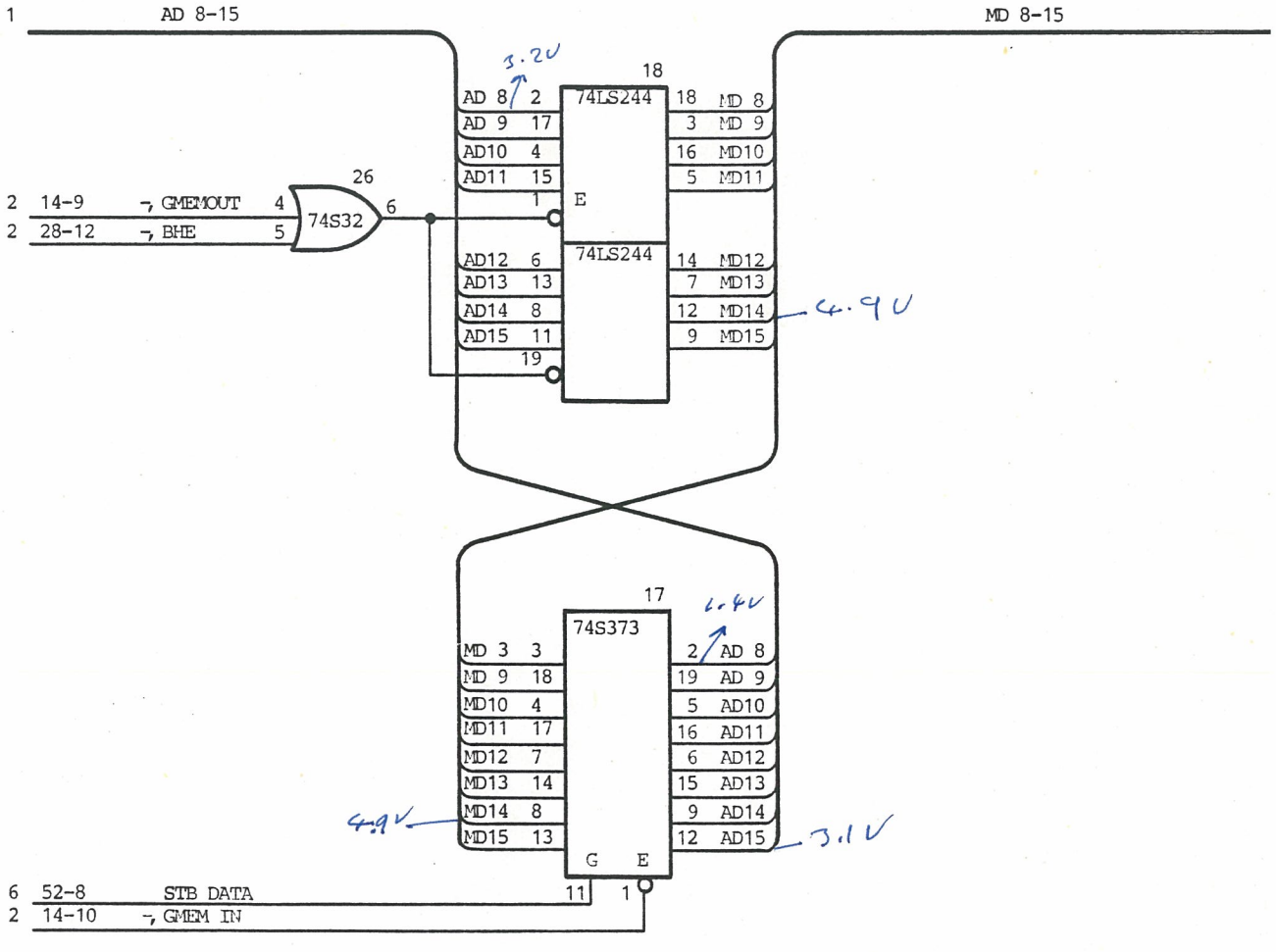
KNEH 840524 MLA



KNEH 840524 MLA

Signal	Destination	Description
A0-A19	p.3 (A0) p.4 (A1-A15) p.5 (A1-A16) p.6 (A0, A14-A19) p.9 (A4-A6) p.12 (A1-A5) p.14 (A1, A4-A6) p.15 (A1-A2) p.18 (A1-A2) p.20 (A3) p.21 (A1-A6) p.24 (A13-A19) p.28 (A1-A5) p.30 (A1-A7)	Memory or I/O address for the current bus cycle.
/BHE	p.3 p.6	Byte High Enable. Latched version of the signal from the CPU.
/GIO IN	p.15	Gate IO INput.
/GIO OUT	p.15	Gate IO OUTput.
/GMEM IN	p.3	Gate MEMory INput.
/GMEM OUT	p.3	Gate MEMory OUTput.
/IO1,/IO2	p.2	Enable either bus 1 (/IO1) or bus 2 (/IO2) transceivers.
/S0-/S2	p.6 p.10 (/S1) p.15 (/S0)	Bus signals. Latched version of the signals from the CPU.
/D0-/D7		Bus 1. This bus controls:
	p.18	Real Time Clock.
	p.17	Keyboard Interface
	p.20	Sound
	p.29	Parallel Printer Interface
	p.28	ISBX interface
	p.12	Colour Palet
2D0-2D7		BUS2. This bus controls:
	p.14	8259 Interrupt Controller
	p.15	8255 Parallel Interface (Configuration).
	p.21	Non volatile memory.
	p.30	I/O expansion.





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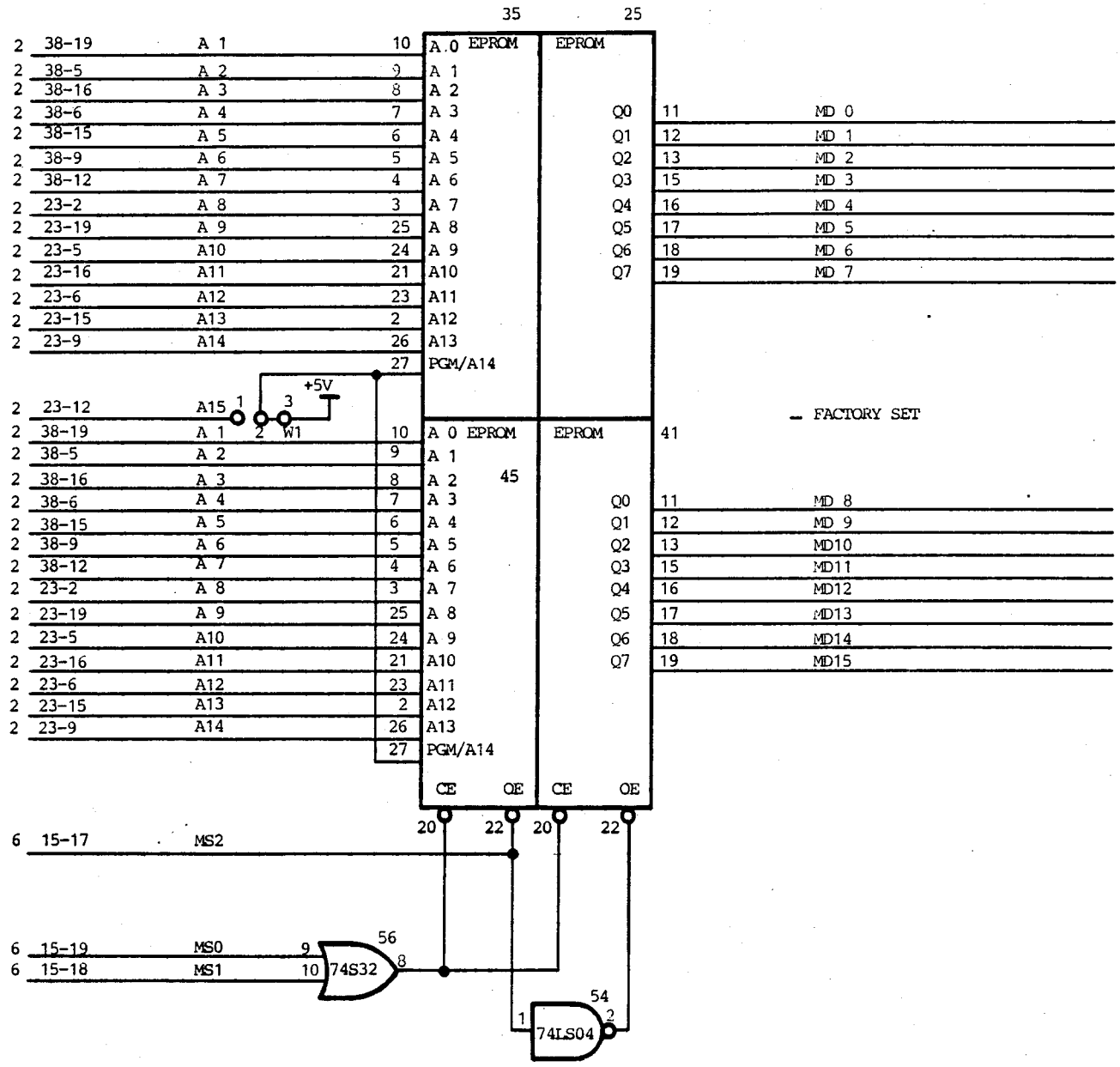
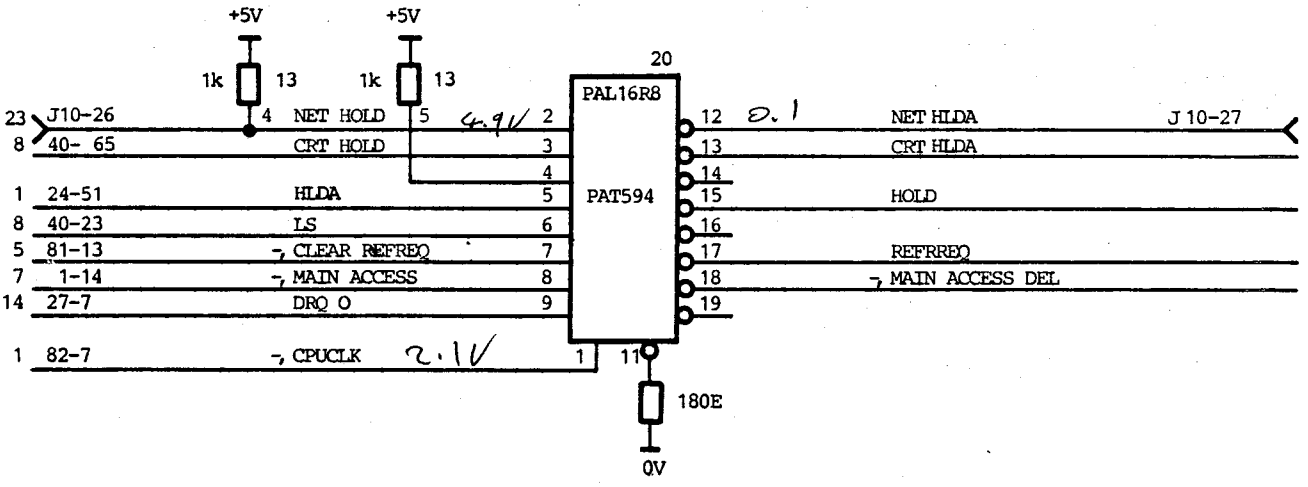
Signal	Destination	Description
CRT HLDA	p.8	CRT controller hold acknowledge.
HOLD	p.1	HOLD request to the 80186 microprocessor.
/MAIN ACCESS DEL	p.6	MAIN memory ACCESS DELayed.
MD 0-15	p.10 p.2 p.25 p.26 p.27	Memory Databus.
NET HLDA	p.23	local area NET work coprocessor HOLD Acknowledge.
REFRREQ	p.6	REFResh cycle REQuest.





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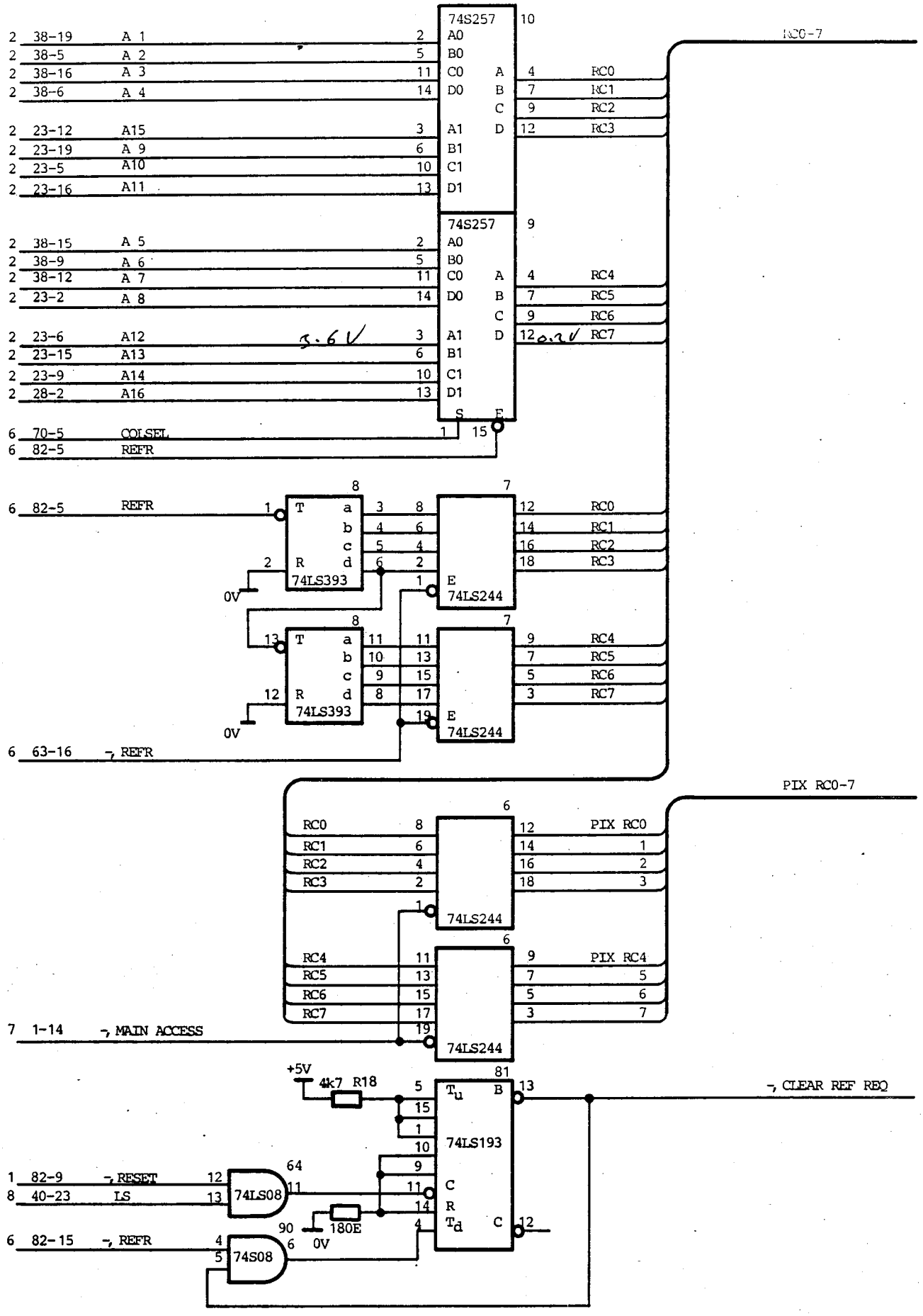
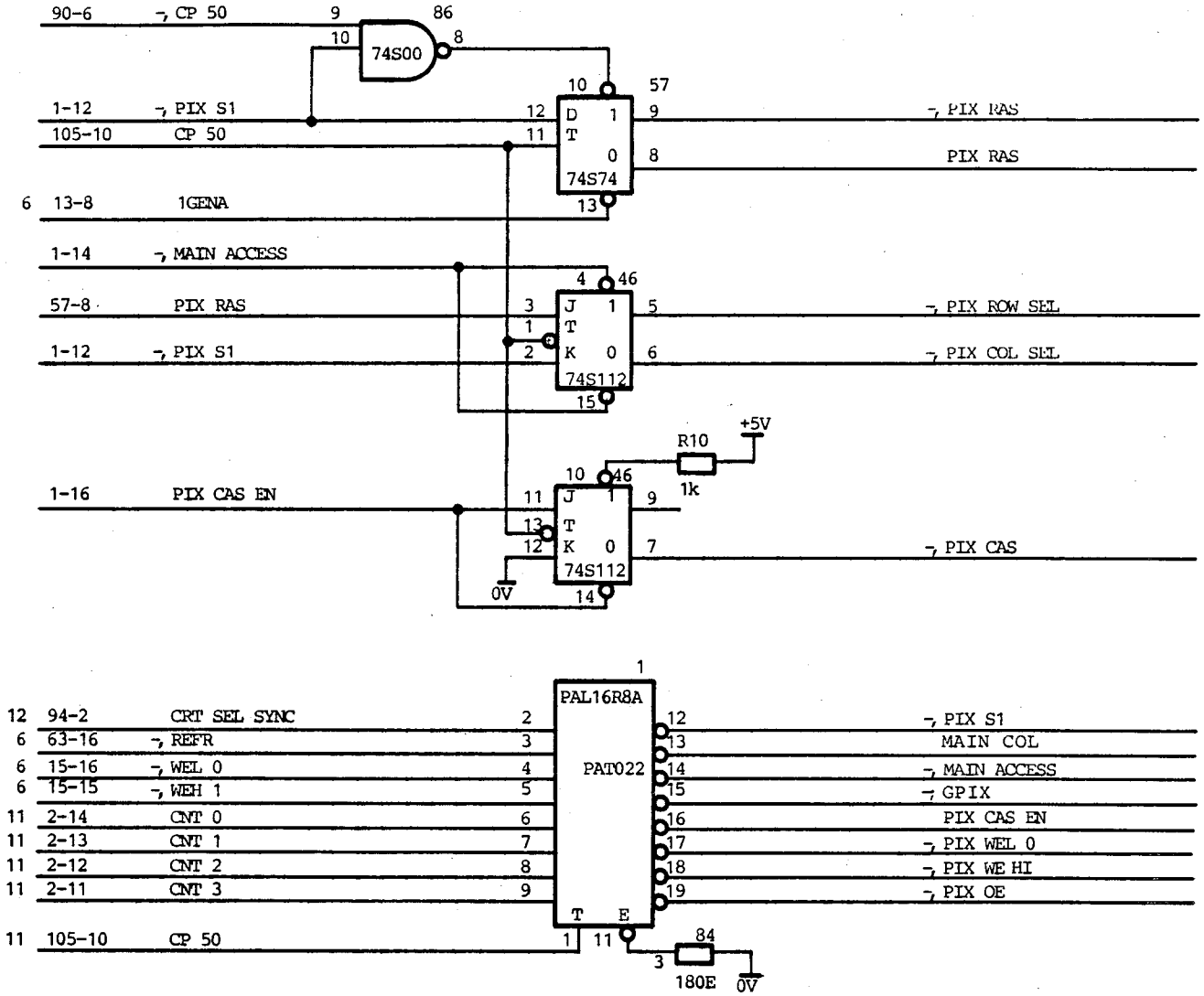
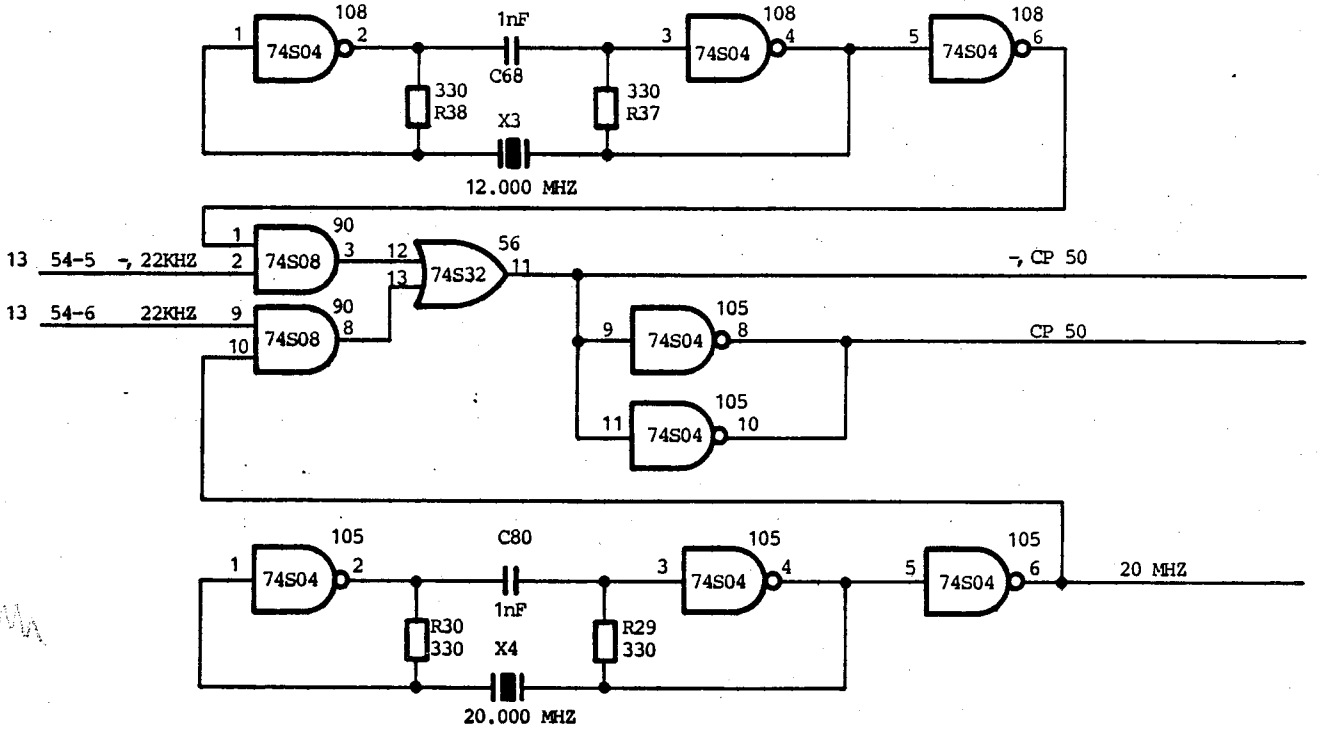
Signal	Destination	Description
/CLEAR REF REQ	p.4	CLEAR REFresh REQuest. This signal is active when the 4th (60Hz /5th (50Hz) refresh cycle in each refres burst is being executed, indicating the end of the burst.
PIX RC 0-7	p.9 (wired or) p.10	Row/Column address multiplexed for addressing of the pixel memory.
RC0-7	p.25 p.27	Row/Column address multiplexed for addressing of the main memory.



KNEH 840524 MLA

Signal	Destination	Description
ALE	p.2 p.30	Address Latches Enable.
ALEDEL	p.6	ALE DELay´ed.
ALE D	p.15	ALE further delayed (IO write state)
/CAS	p.25 p.27	Column ram Address Select.
COL SEL	p.5	COLumn addr. SELect. Control signal to the address multiplexer.
COL SEL*	p.6	
CRT SEL	p.6 p.12	Activates a mainaccess to the pixel memory.
MEM RDY	p.15	MEMory ReaDY indication to the CPU (ARDY).
MS 0-2	p.4 p.6	Memory Selection code.
RASEN	p.24	Row Address Select enable to memory.
REFR	p.5	Refresh cycle in progress.
/REFR	p.5 p.7 p.24	Same as above.
RC8	p.25 p.27	Multiplex of A18 and A19
STB DATA	p.3	Latch memory data (MB 0-15) on to the cpu bus (AD 0-15).
/WELO, /WEHI	p.24 p.27	Write Enable for LOwer and HIgh byte.





KNEH 840524 MLA

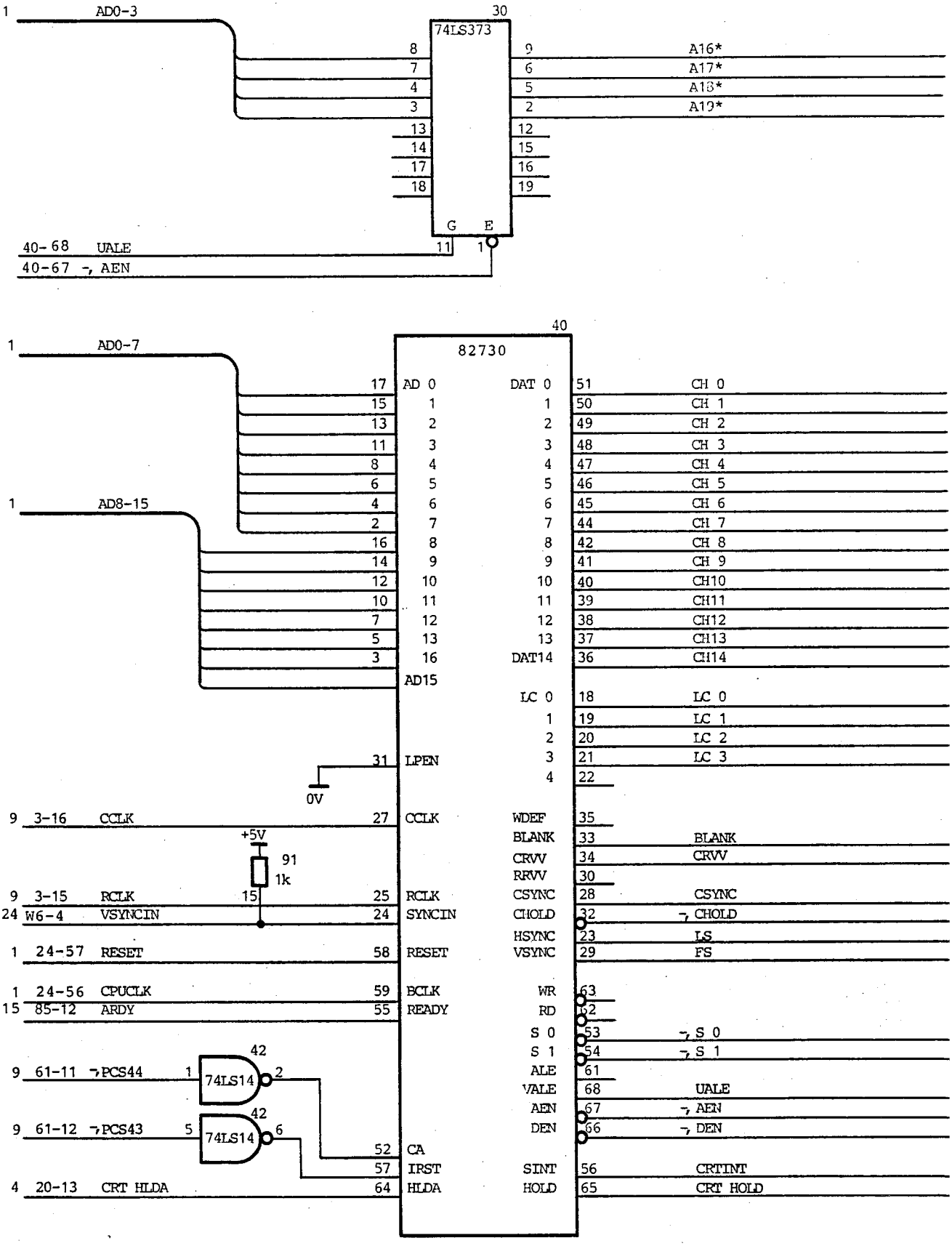
CPU 740

A14627

DOT CLOCK
PIXELMEM CONTROL & CRT REFRESH MEM CONTROL

Signal	Destination	Description
A16*-A19*	p.2 p.1 (wired or) p.23 (wired or)	Most significant address bits generated by 74LS373 which is loaded from the processor bus on UALE (Upper Address Load Enable).
CH0-14	p.9	Value of next displayed character clocked out of 82730 on CCLK.
/AEN	p.8	Address ENable is active low during the entire period when 82730 is driving the bus. It is used to unfloat the outputs of the Upper Address Latch.
BLANK	p.9	Next character is not displayed.
CRVV	p.9	Character ReVerse Video. Used to externally invert video data output.
CSYNC	p.9	CCLK synchronization output; used to synchronize external character clock generator to reference clock timing This output is active outside the display field.
/CHOLD	p.9	CCLK inhibit output. Used by external logic to inhibit CCLK generation This output is active during the tab function.
CRT INT	p.14	Status interrupt. Informs the processor that an unmasked interrupt has been generated in the 82730 status register.
CRT HOLD	p.1 p.4	Indicates that the 82730 wants bus access.
/DEN	p.2 p.9 p.1 (wired or) p.23 (wired or) p.28 p.30	Data ENable for bus transceivers.
FS	p.13	Frame sync. Active during the programmed vertical sync interval.
LS	p.4 p.13	Line Sync. Horizontal synchronization to the CRT monitor.
LC0-3		Line Count outputs. Used to address the character generator for the line positions in a row. The line number output is a function of the display mode and character attributes.
/S0*-S1*	p.2 p.1 (wired or) p.23 (wired or)	Bus status signals indicating the kind of bus cycle being performed.
UALE	p.8	Upper Address Latch Enable. It is similar to ALE except that it occurs in upper address output cycle.

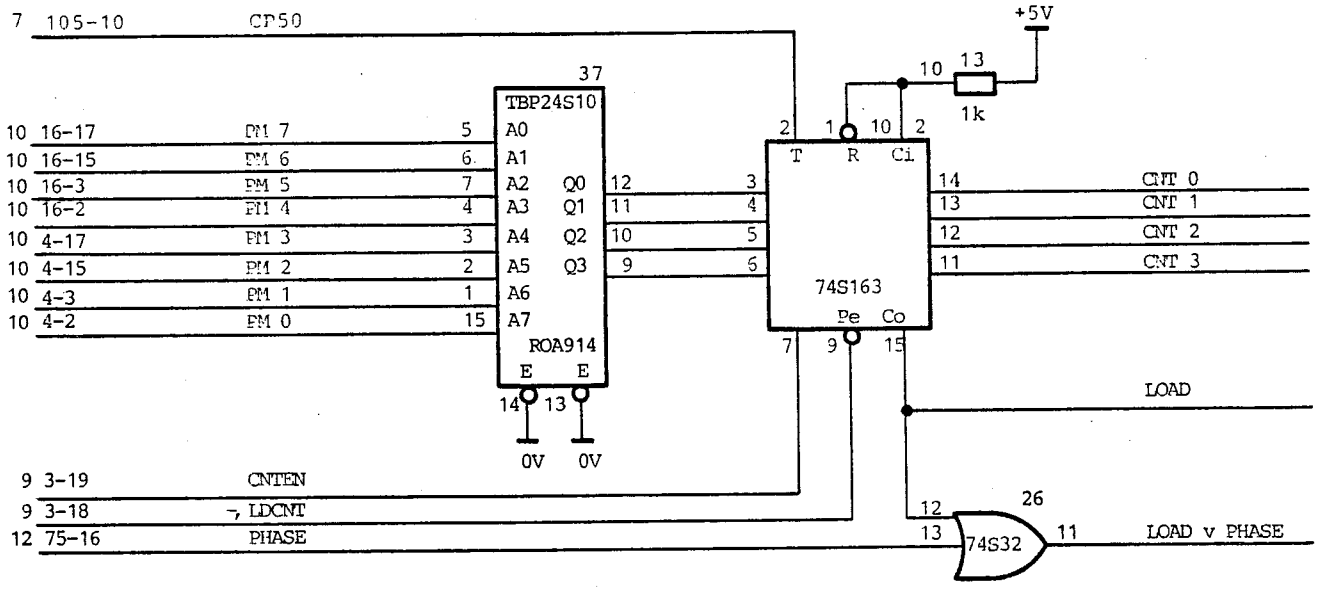
/S2	1	0	Bus cycle
0	0	0	Interrupt ACK
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	HALT
1	0	0	Code fetch
1	0	1	Read Mem
1	1	0	Write Mem
1	1	1	Passive

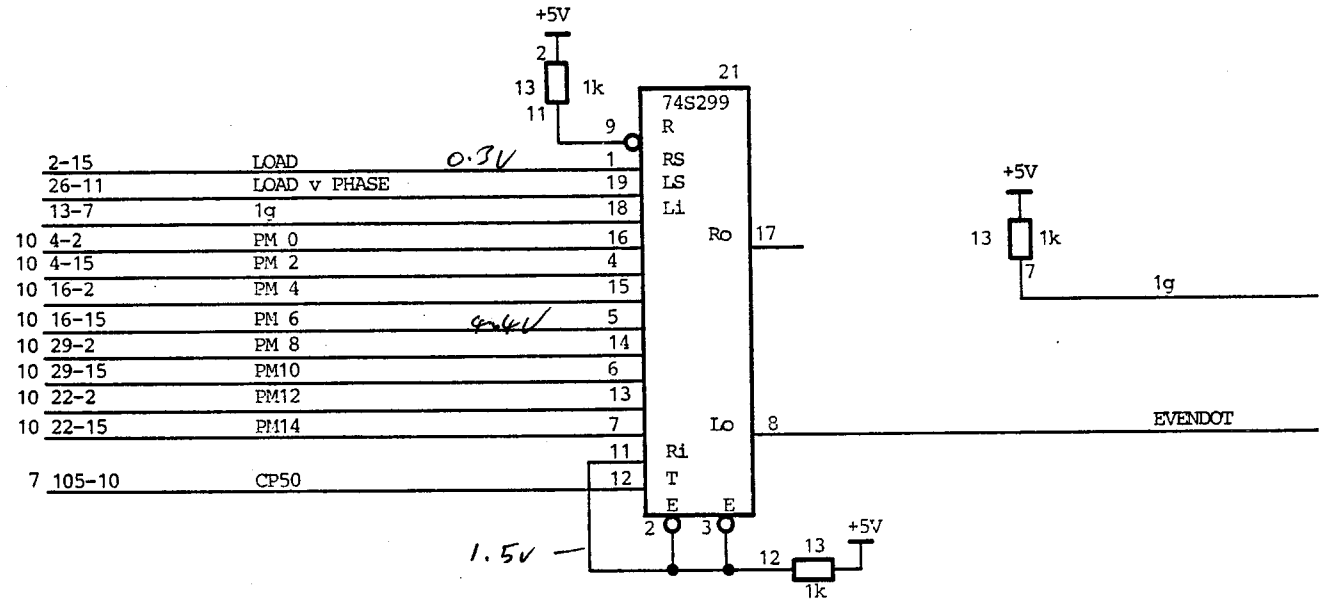


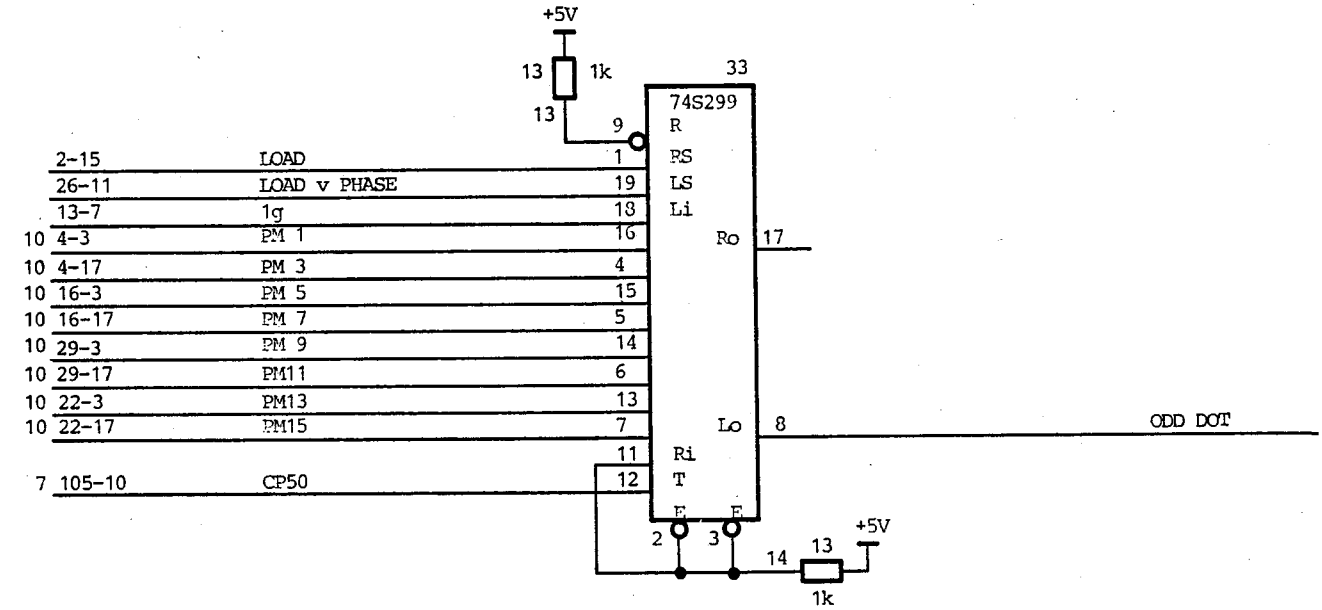
82730	
+5V	9,43
0V	26,60

KNEH 840524 MLA

Signal	Destination	Description
ATTR 0-4	p.12	ATTRibut bit 0-4. Pipelined versions of CH10-14.
BLANK D	P.12	Pipelined version of BLANK
CRWD D	p.12	Pipelined version of CRVV.
CCLK	p.8	Character CLock. Input used to clock row buffer dat, attribute, cursor, and line count out of 82730.
CSYND	p.12	Pipelined version of CSYNC.
CNTEN	p.11	CouNT ENable.
/LDCNT	p.11	LoaD CouNTer.
PIX RC 0-7	p.5 (wired or) p.10	Row/Column address Multiplexed for addressing of the pixel memory.
/PCS43	p.8	Peripheral Chip Select for I/O address IO Base + 230H.
/PCS44	p.8	Peripheral Chip Select for I/O address I/O Base + 240H.
/PCS45	p.29	Peripheral Chip Select for I/O address IO Base + 250H.
/PCS46	p.29	Peripheral Chip Select for I/O address IO Base + 260H.
RCLK	p.8	Reference CLocK. Used to generate timings for the screen layout and to define screen columns for data formatting

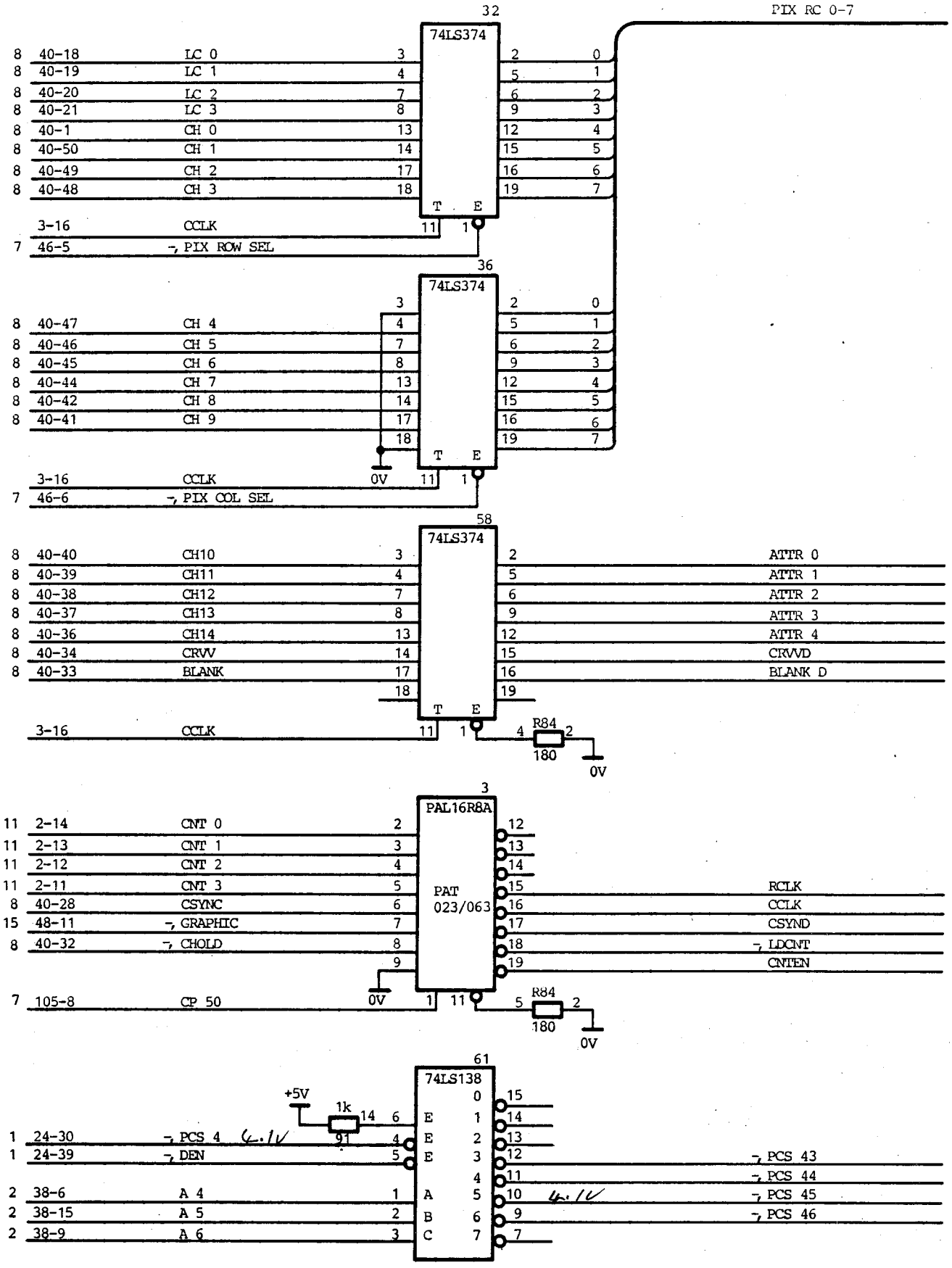






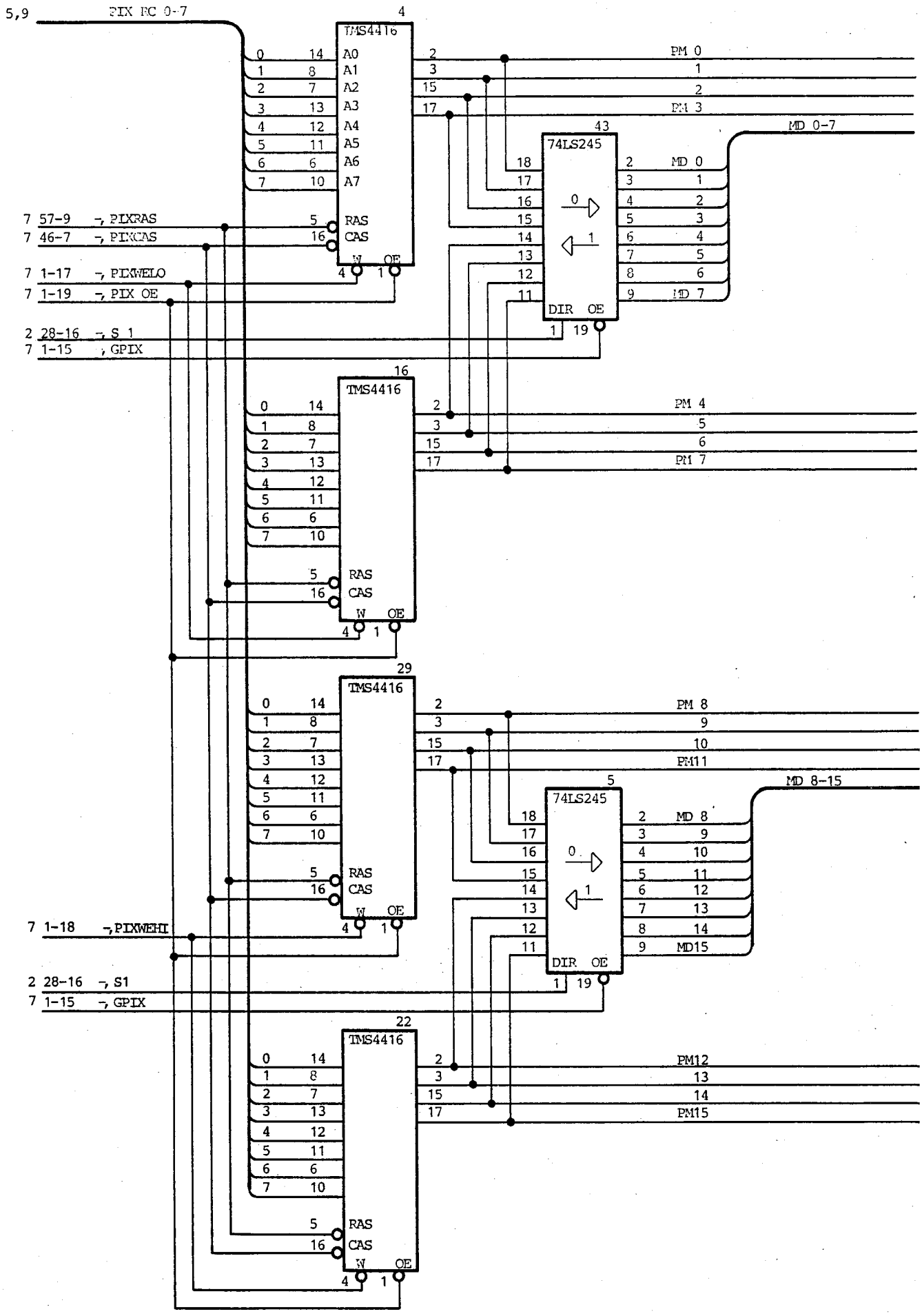
KNEH 840524 MLA

Signal	Destination	Description
B, G, R, I	p.13	Blue, Green, Red, and Intensity signals.
DOT*	p.12	In low resolution graphic equal to ODD DOT else multiplex between ODD DOT and EVEN DOT controlled by PHASE. In alpha mode DOT* is off in case of blank and inverted in case of CRVVD.
CRT SEL SYNC	p.12 p.7	CRT SEL synchronized by dot clock CP50
PCS3 SYNC	p.12	Synchronized (CP50) I/O write to Palet memory (180H-19FH).
PHASE	p.11	Control multiplexing between ODD/EVEN DOTS.
LCOLOR	p.12	Load the output COLOR´s from Palet memory.
PS0-4	p.12	Pallette Select address bit 0-3.
IC75-pin17	p.12	PALLRD (PAllette ReaD) controls the address multiplexer for the Pallette (PS0-4).
/WRTDS	p.12	WRITe DiSable. When the Palette is read and the contents are latched in the Palette output register, programmed write pulses are gated off. When low resolution are displayed, programmed writes to the Palette are dummy, in other cases the write pulses are long enough to write the Palette even if interrupted in the middle of a read.



KNEH 840524 MLA

Signal	Destination	Description
MD 0-15	p.4 (wired or) p.2 p.25 p.26 p.27	Memory Databus
PM 0-15	p.11	Pixel Memory databus.

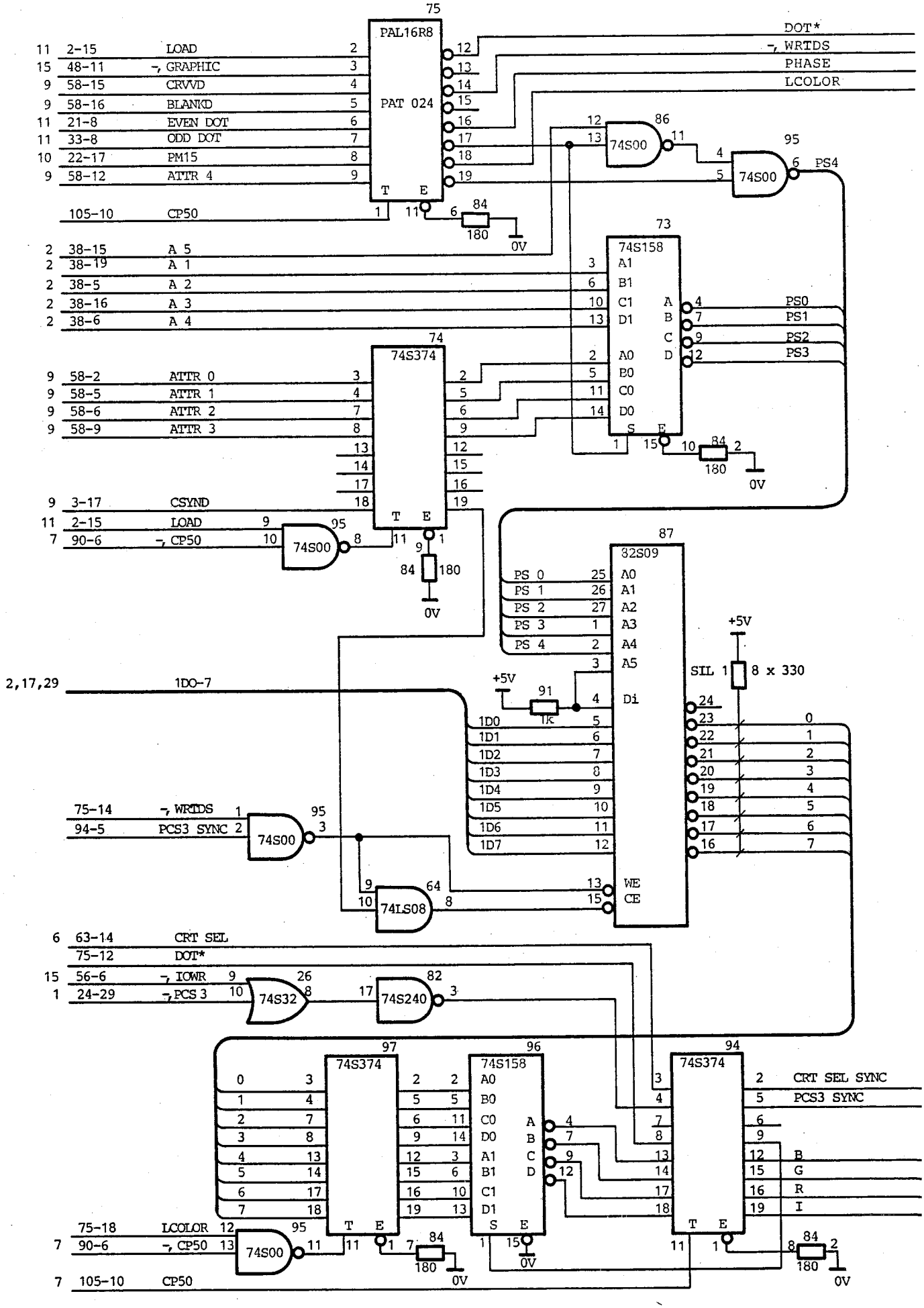


KNEH 840524 MLA

Signal	Destination	Description
CNT 0-3	p.9 p.7	Dot counter output. Used to generate CCLK and to control Pixel memory cycles. When not in graphic mode, the dot counter is loaded with 16-char. width. Char width is derived from the dot-pattern read in the pixel memory by means of ROC107:

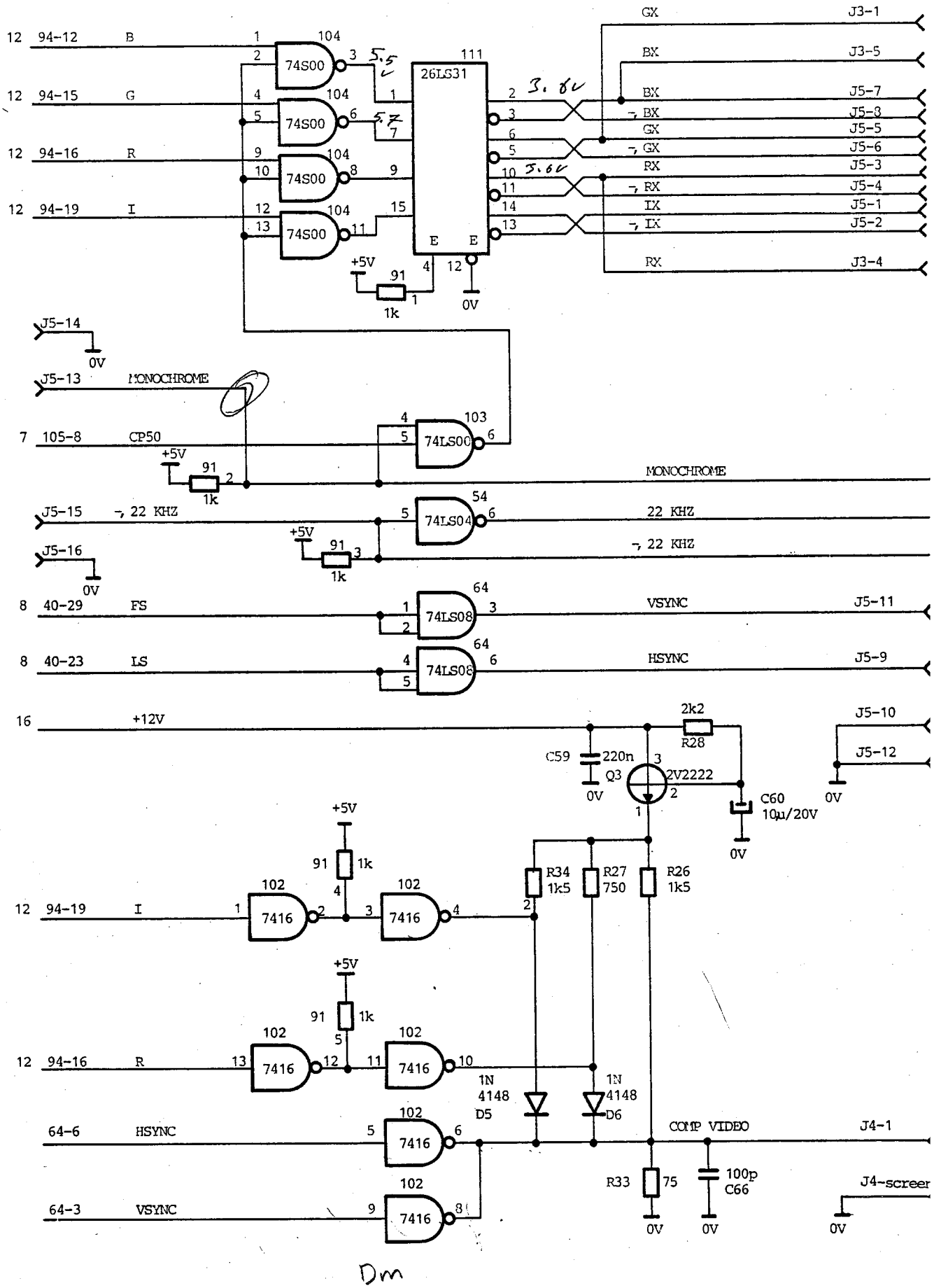
PM	7	6	5	4	3	2	1	0	16-char width	char width
	X	X	X	X	X	X	X	0	1	15
	X	X	X	X	X	X	0	1	2	14
	X	X	X	X	X	0	1	1	3	13
	X	X	X	X	0	1	1	1	4	12
	X	X	X	0	1	1	1	1	5	11
	X	X	0	1	1	1	1	1	6	10
	X	0	1	1	1	1	1	1	7	9
	0	1	1	1	1	1	1	1	8	8
	1	1	1	1	1	1	1	1	9	7

EVEN DOT	p.12	Even numbered dots from pixel memory.
LOAD	p.11 p.12	Loads next dotpattern into the shift registers.
LOAD/PHASE	p.11	True every second clock period allowing the shifters to advance only every second clock.
ODD DOT	p.12	Odd numbered dots from pixel memory. Dot bits out in parallel, this feature is used in low resolution graphic. When serial mono dot stream is used (alpha and high resolution graphic) EVENDOT and ODDDOT are multiplexed in PAT024 (page 12).



KNEH 840524 MLA

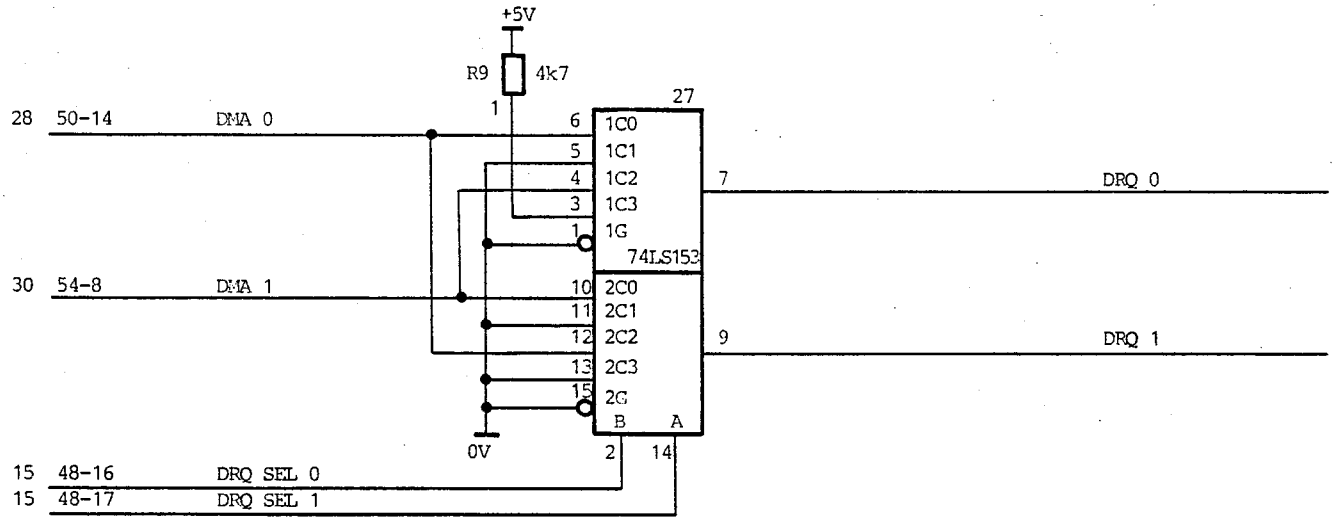
Signal	Destination	Description
Bx through Ix	J3 J5 p.13	These signals are balanced video-signals for Blue, Green, Red and Intensity. In the case a colour monitor is connected, the video signals are chopped create a uniform horizontal and vertical characteristic on the screen.
COMP VIDEO	J4	COMPosite video output to a mono-chrome monitor.
HSYNC	p.13 p.24 J5	Buffered version of LS (Horizon-tal synchronization pulses).
MONOCHROME	p.15	This signal is true if a monochrome monitor is connected, but false if a colour monitor is connected.
22KHz	p.15 p.5 p.7	If true this signal indicates that a monitor with 22KHz line frequency is connected. If false a monitor with 15.625KHz line frequency is used.
/22KHz	p.5 p.7	the same as above.
VSYNC	p.13 p.24 J5	Buffered version of FS (Frame Synchronization pulses).

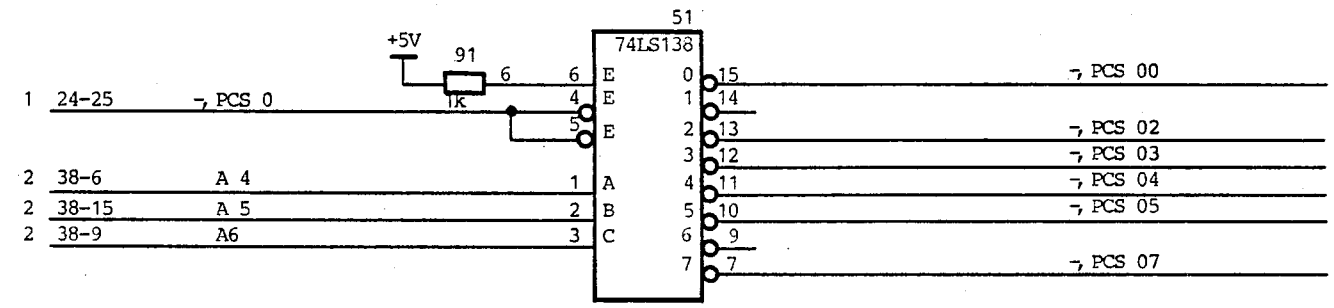


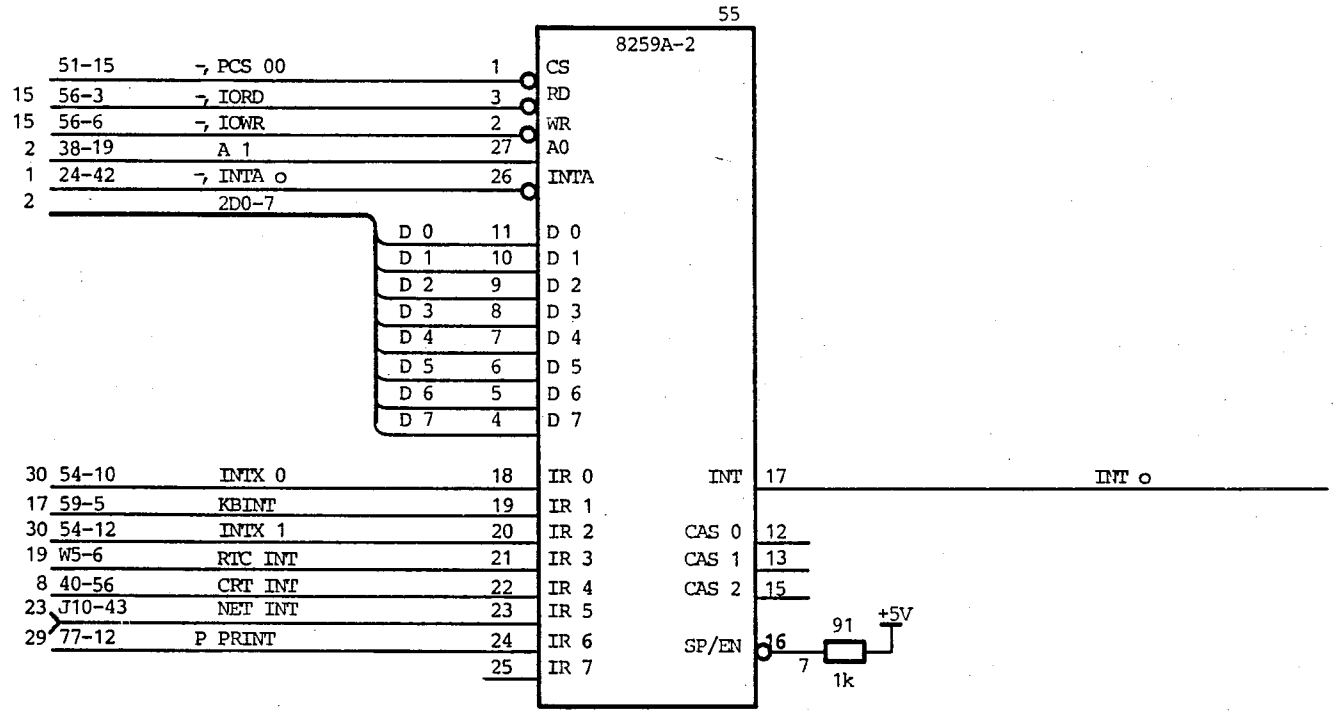
KNEH 840524 MLA

Dm

Signal	Destination	Description
ARDY	p.1 p.23	Asynchronous ReaDY. Request signal to the processor to insert wait states.
BUS 2 SELECT	p.2	When active 2D0-7 are used for I/O transfer.
CAS DATA IN	p.22 (wired or)	Cassette Data serial INput.
/DPC CONNECT	p.30 (wired or)	Configuration bit, if true, indicating that a DPA module is connected.
DR Q SEL 0-1	p.14	Dma ReQuest SELect bit 0-1. DRQ SEL 0 1 DRQ 0 DRQ 1 0 0 DMA 0 DMA 1 0 1 0 0 1 0 DMA 1 DMA 0 1 1 1 0
ENABLE CAS	p.1	Enable signal to the timer generating the cassette output data.
/GRAPHIC	p.12 p.9	CRT mode selecter.
/IORD	p.14 p.15 p.16 p.17 p.18 p.20 p.21 p.28 p.29 p.30	I/O ReaD signal.
/IOWR	p.12 p.14 p.15 p.18 p.20 p.21 p.28 p.29 p.30	I/O WRite signal.
DRQ0	p.1	Data channel ReQuest 0.
DRQ1	p.1	Data channel ReQuest 1.
/PCS00	p.14 p.15	Peripheral Chip Select for all even I/O addresses between IOBASE + OH and IOBASE + EH. Controls the 8259 interrupt controller.
/PCS02	p.17	Peripheral Chip Select for IOBASE + 20H to IOBASE + 2EH. Controls the Keyboard interface.
PCS03	p.15 p.12	Peripheral Chip Select for IOBASE +30H to IOBASE + 3EH
/PCS04	p.15	Peripheral Chip Select for IOBASE +40H to IOBASE + 4EH.
/PCS05	p.18 p.20	Peripheral Chip Select for IOBASE +50H to IOBASE + 5EH. Controls the RealTime Clock and the Sound generator.
/PCS07	p.15	Peripheral Chip Select for IOBASE + 70H to IOBASE + 7EH. Controls the 8255 parallel port interface (configuration port).
INTO	p.1	Interrupt input to the CPU.







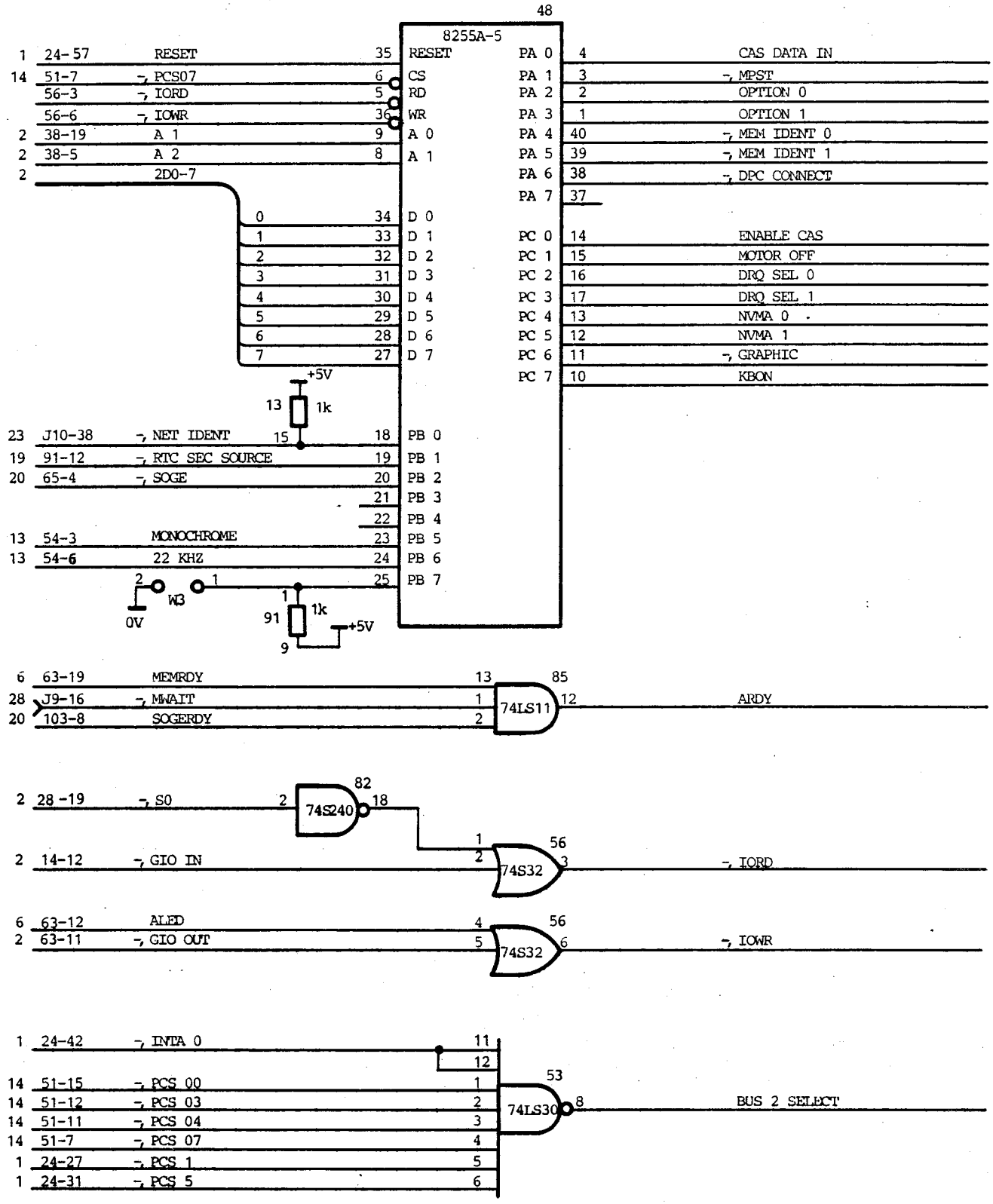
KNEH 840524 MLA

Signal	Destination	Description
KBON	p.16	Controls power to the keyboard. If true the keyboard power is switched on.
/MPST	p.28 (wired or)	Configuration bit. True if an iSBX module is installed.
/MEM IDENT 0-1	p.24 (wired or)	Indicates the memory configuration

/MEM IDENT

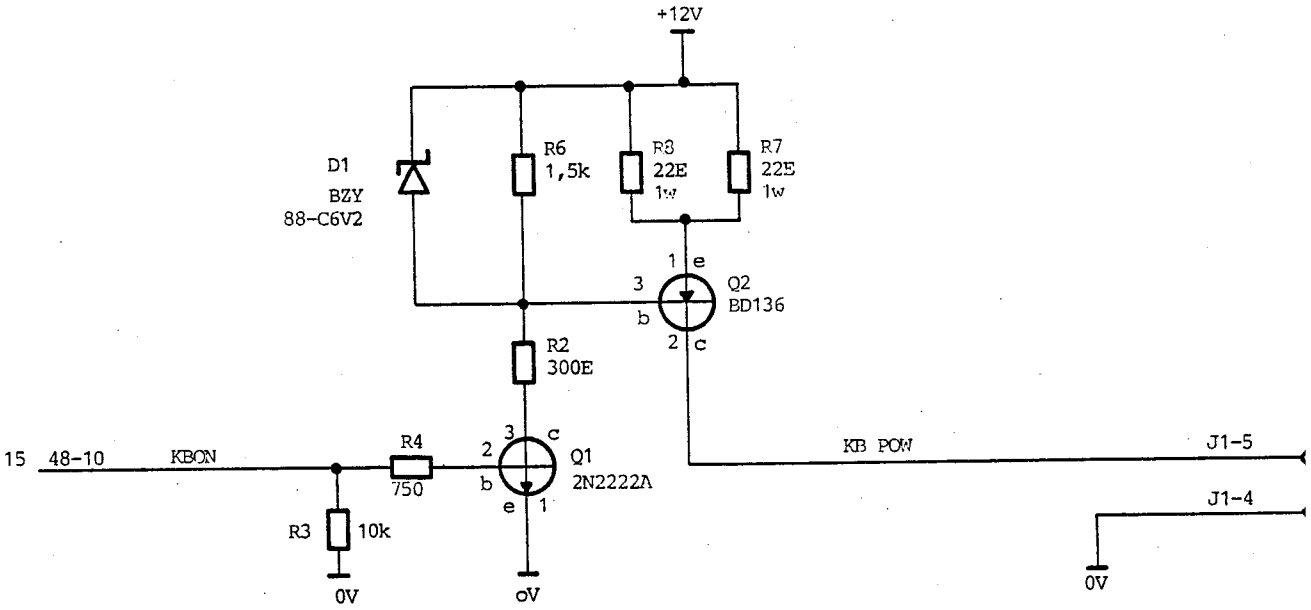
0	1	memory size
0	0	768 K
0	1	1 M
1	0	384 K
1	1	256K

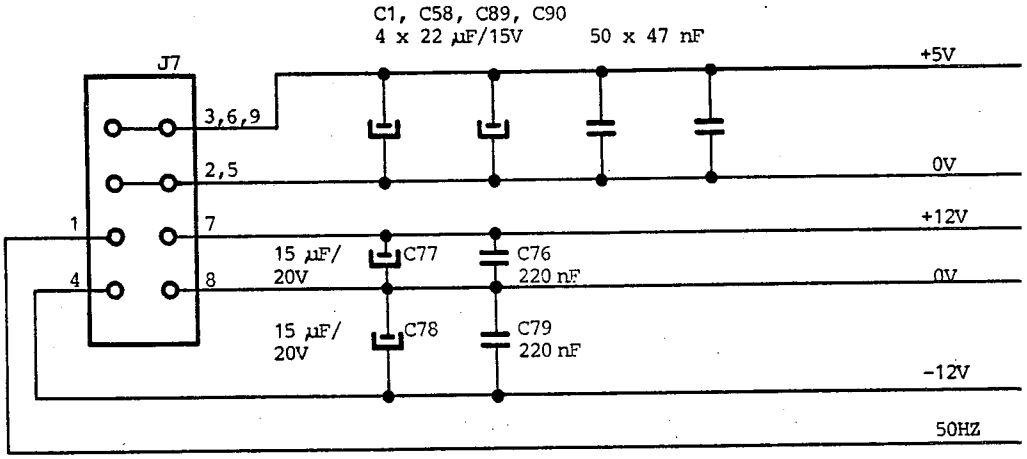
MOTOR OFF	p.22	Controls the cassette motor. If true the motor is stopped.
NVMA 0-1	p.21	Group address to the Non Volatile Memory.
OPTION 0-1	p.28 (wired or)	Optional status signals from the iSBX bus. Refer to the iSBX module manuals for the meaning of these signals.

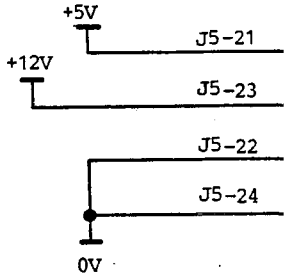


KNEH 840524 MLA

Signal	Destination	Description
KB POW	J1	Power supply to the Keyboard. When the keyboard is connected the voltage on this line is 8-10 volt.

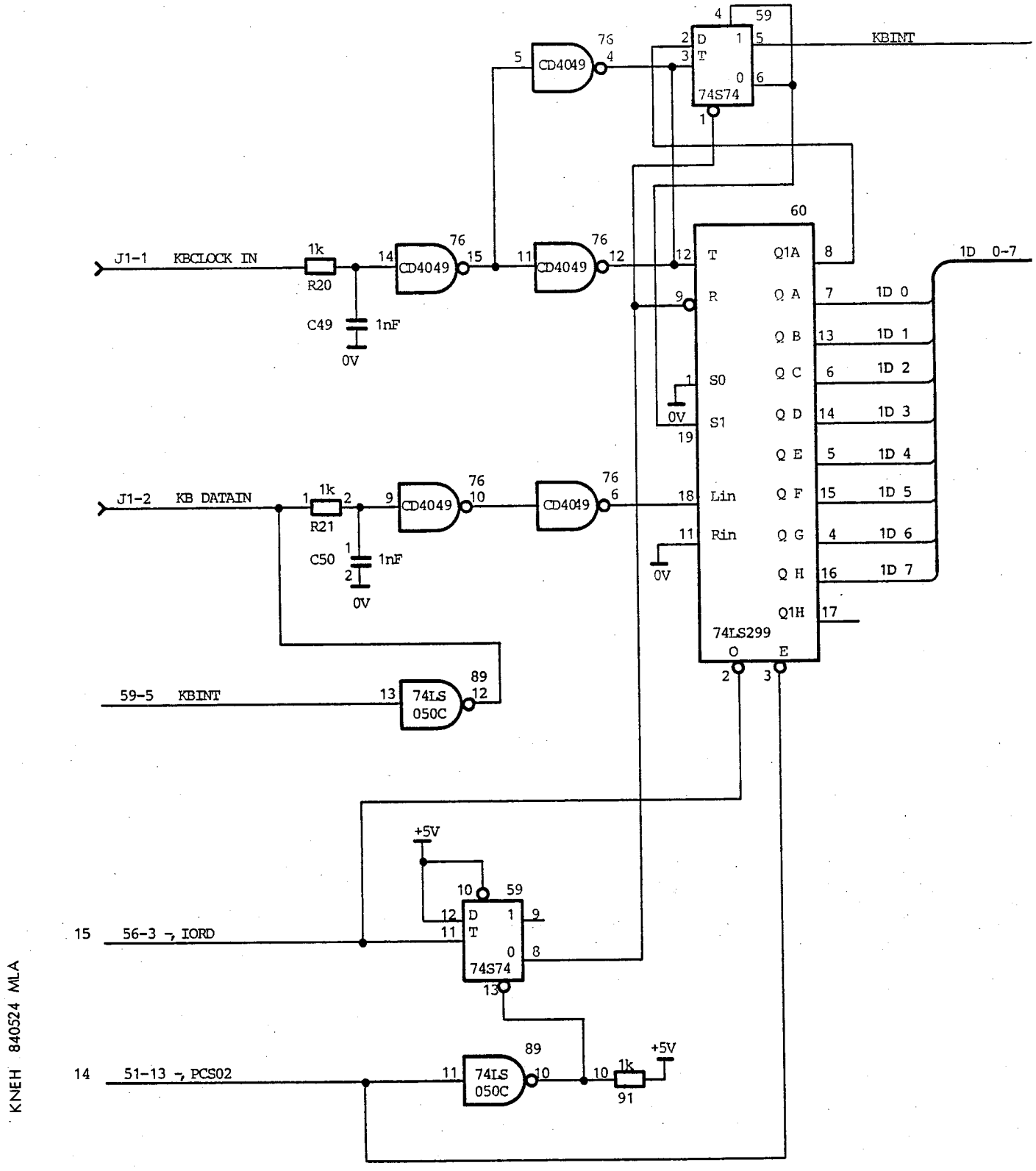






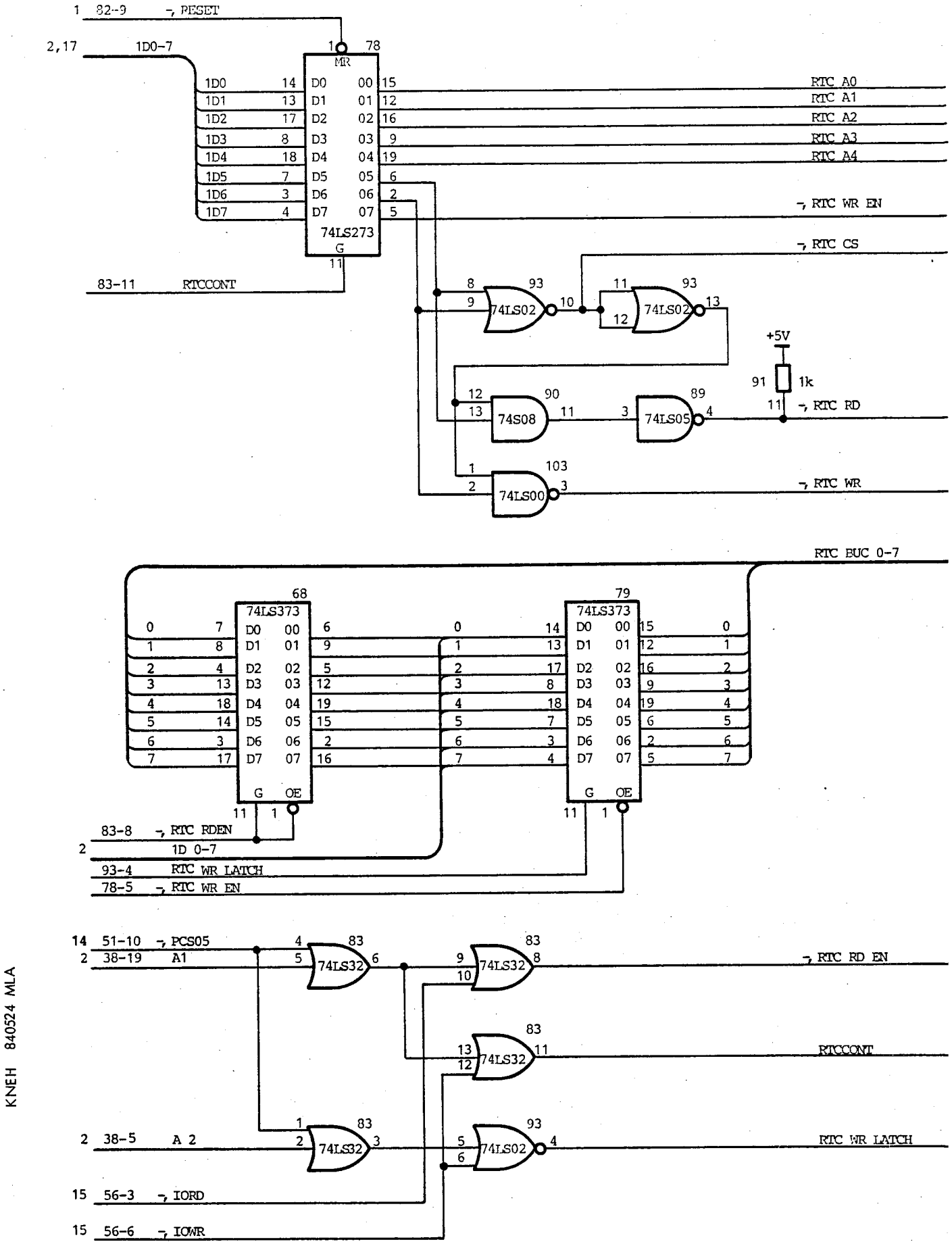
KNEH 840524 MLA

Signal	Destinaton	Description
KBINT	p.14	KeyBoard INTerrupt. Set whenever a character is received from the keyboard.
ID 0-7	p.18 p.2 p.20 p.29 p.28 p.12	I/O Bus 1.



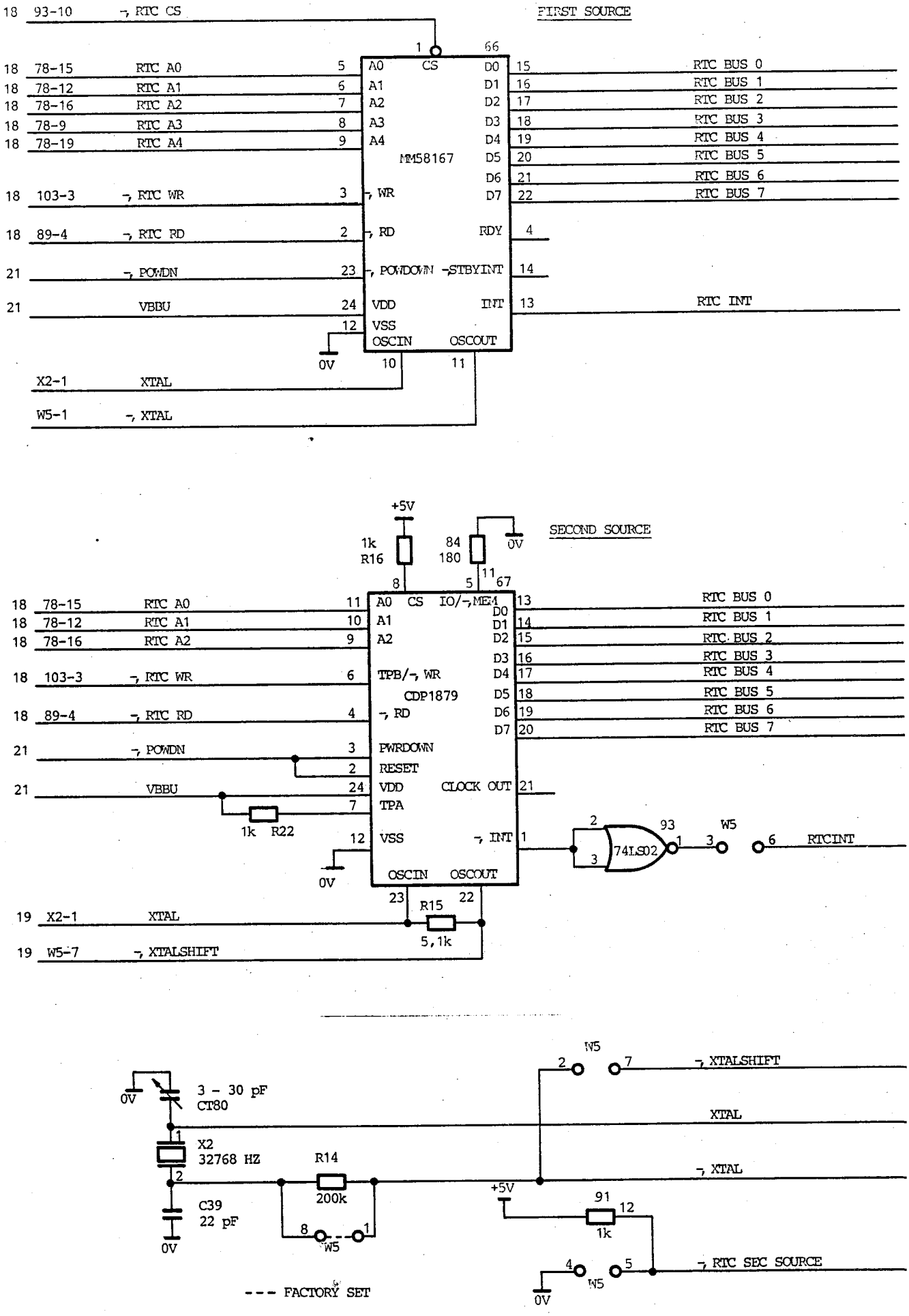
KNEH 840524 MLA

Signal	Destination	Description
RTC A0-A4	p.19	Address information to the RTC
RTC BUS 0-7	p.19 (wired or) p.20	Local data bus used by the RTC and the sound generator.
/RTC CS	p.19	Chip select signal used to control the RTC.
RTCCONT	p.18	Latch signal to the RTC address latch.
/RTC RD	p.19	Read signal to the RTC.
/RTC RC EN	p.18	RTC ReaD ENable.Enables data output from RTC.
/RTC WR EN	p.18	RTC WRite ENable. Enables data input to RTC.
RTC WR LATCH	p.18	Latches data input to RTC.
/RTC WR	p.19	Write signal to the RTC.



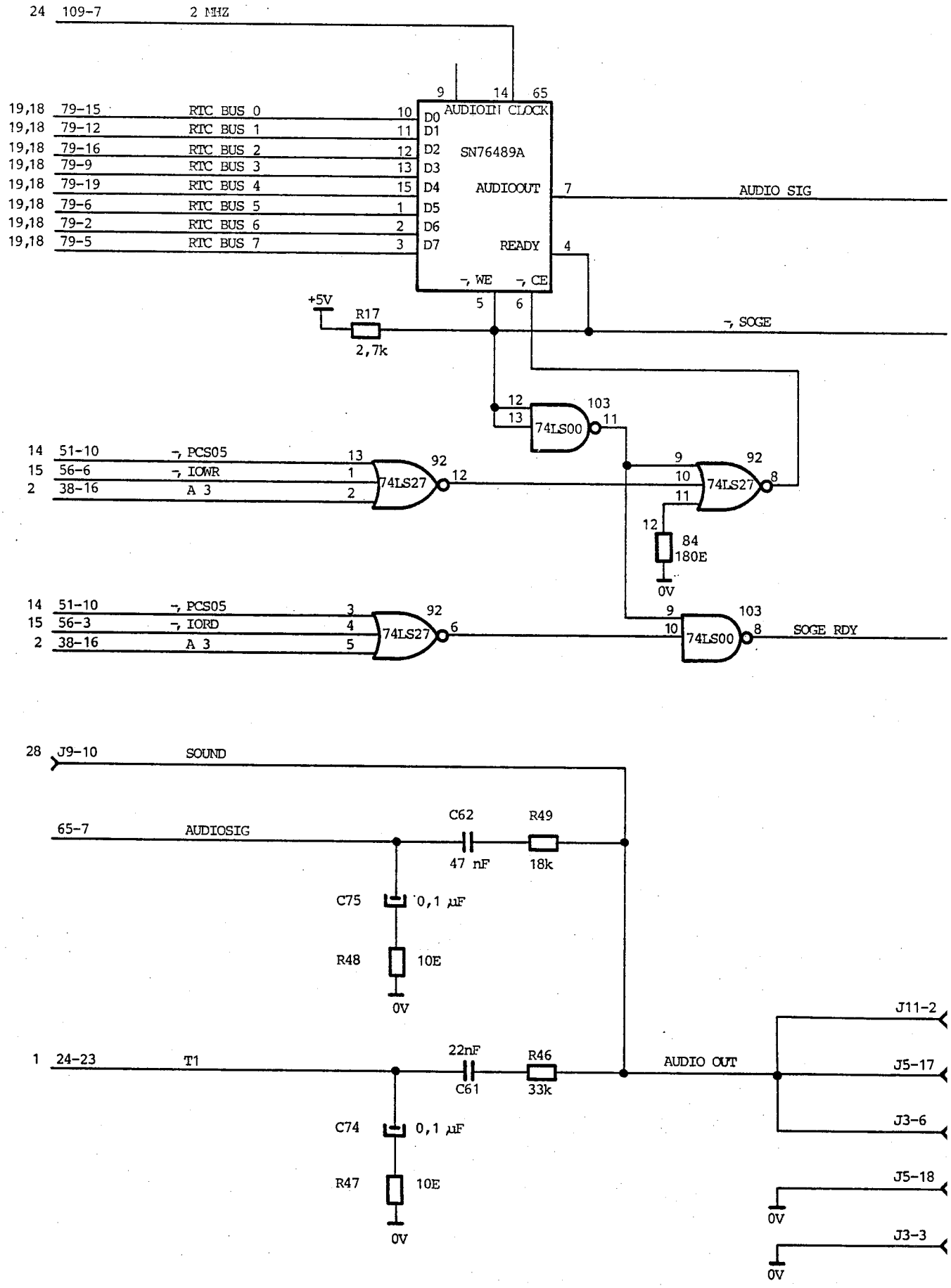
KNEH 840524 MLA

Signal	Destination	Description
RTC BUS 0-7	p.18 (wired or) p.20	Local data bus used by the RTC and the sound generator.
RTC INT	p.14	RTC INTerrupt.
/RTC SEC SOURCE	p.15	False if the MM58167 RTC chip is used. True if the CDP1879 RTC chip is used.



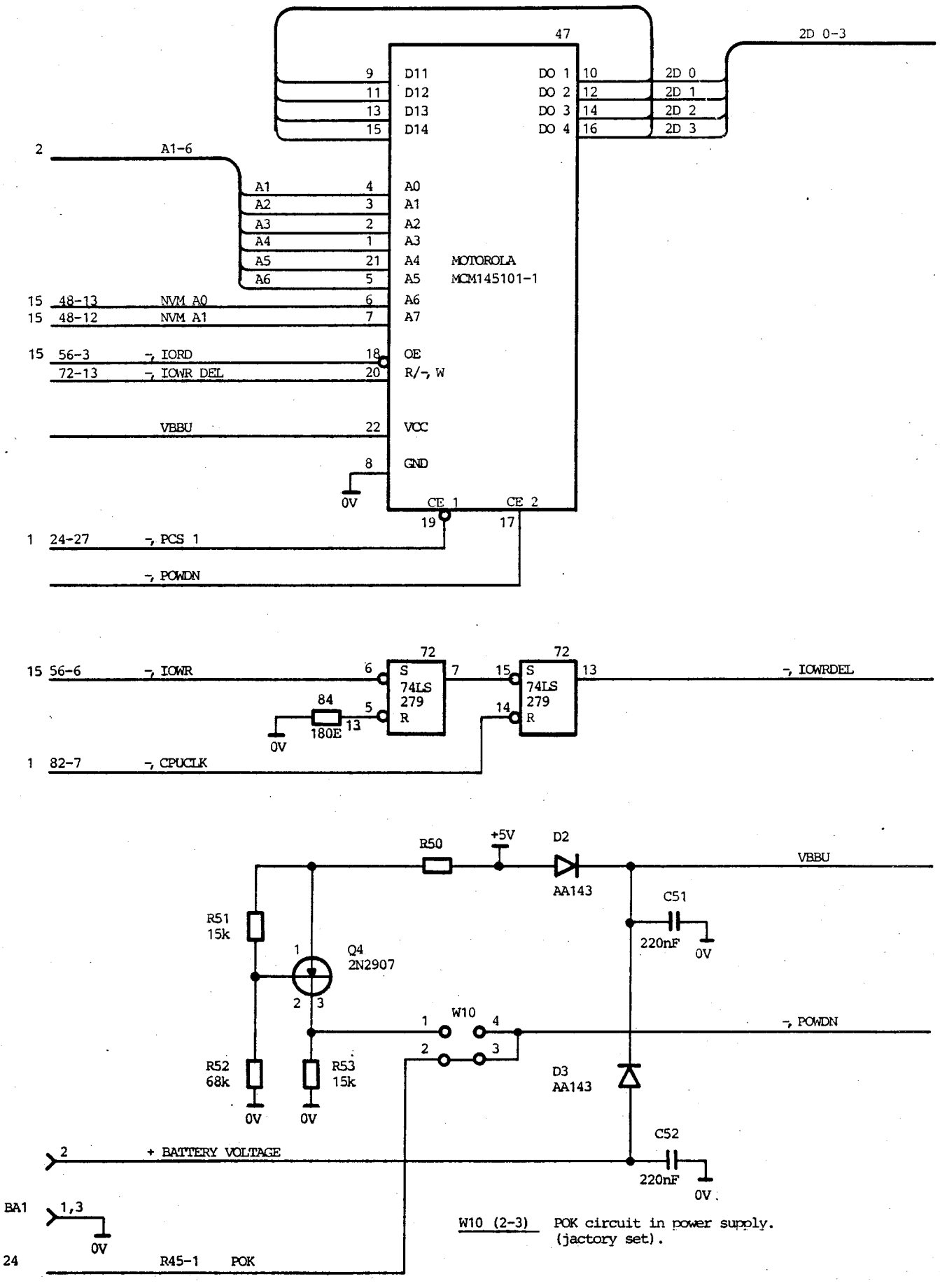
KNEH 840524 MLA

Signal	Destination	Description
AUDIO SIG AUDIO OUT	p.20 J3 J5	Analog audio output. AUDIO output signal to the audio amplifier (via the volumen control).
SOGE	p.15	Indicates the presence of the sound generator.
/SOGE RDY	p.15	Indicates the READY-condition of the sound generator.



KNEH 840524 MLA

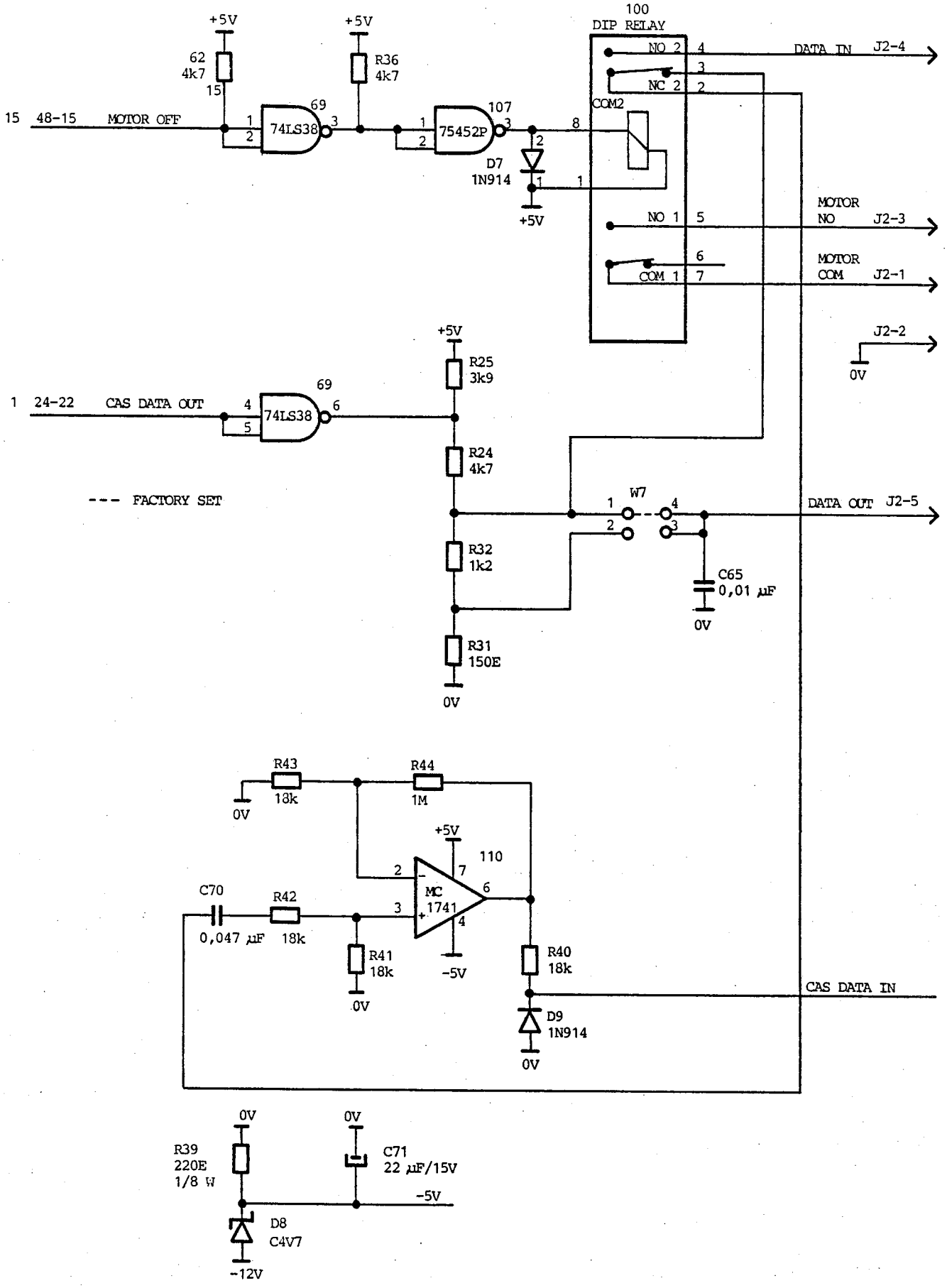
Signal	Destination	Description
2D0-3	p.14 p.15 p.30	I/O BUS 2.
/IOWR DEL	p.21	I/O WRite delayed.
VBBU	p.19 p.21	Battery supported power supply.
/POWDN	p.19 p.21	/POWer DOWN indication to disable operation of the RTC and NVM.



W10 (2-3) POK circuit in power supply. (jactory set).

KNEH 840524 MLA

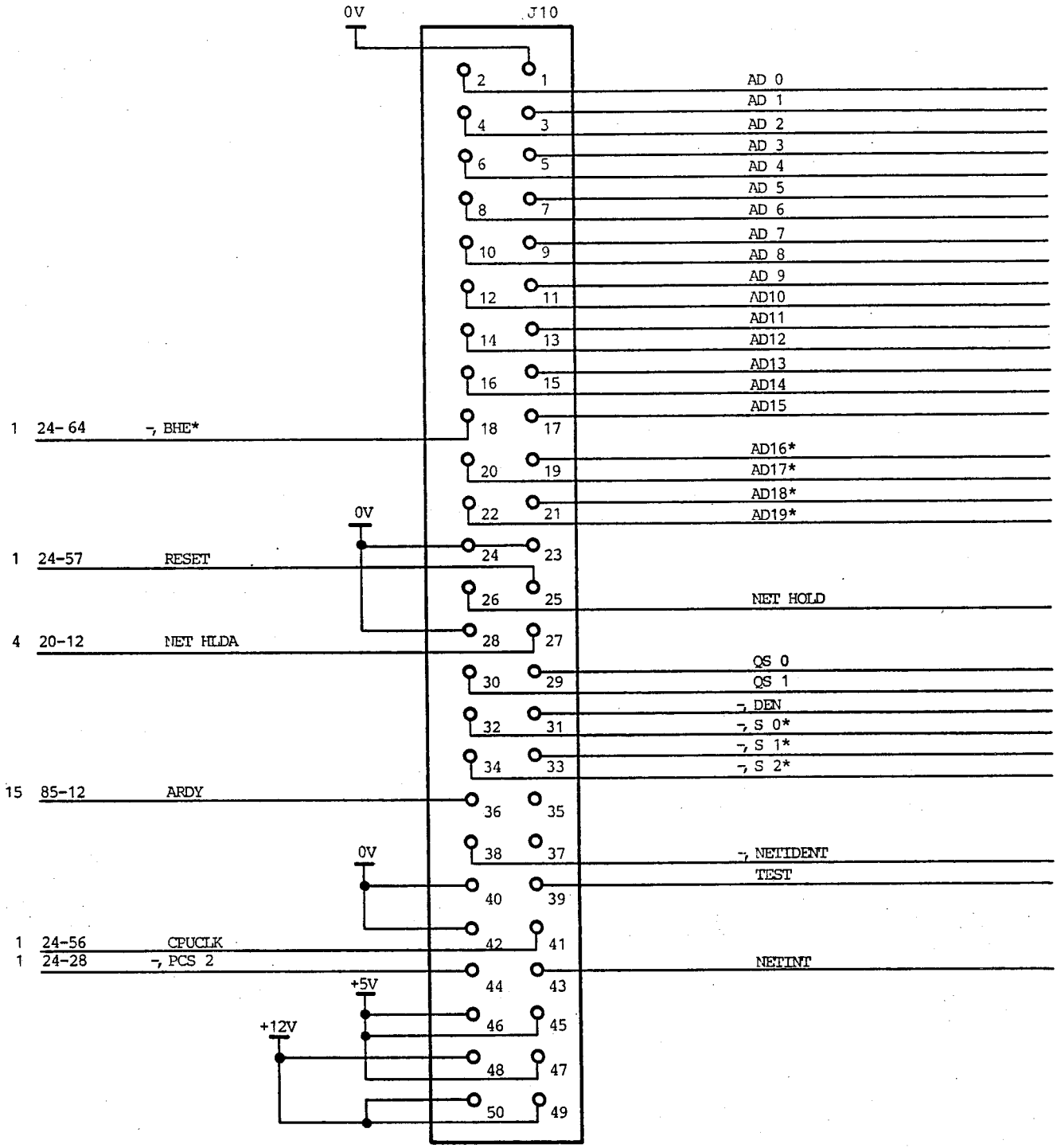
Signal	Destination	Description
CAS DATA IN	p.15 (wired or)	CASsette DATA INput to the processor.
DATA IN	J2	Serial data from the Cassette.
DATA OUT	J2	Serial data to the Cassette.
MOTOR NO, MOTOR COM	J2	Relay contacts (normal open function) to control the cassette motor.



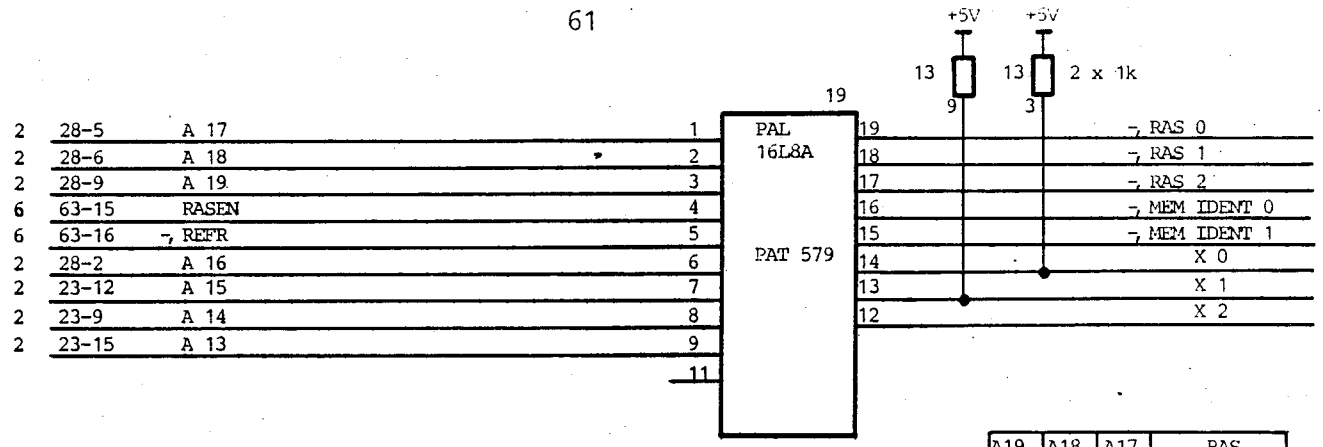
KNEH 840524 MLA

Signal	Destination	Description
AD 0-15	p.2 p.1 (wired or) p.3 p.8	Multiplexed address/data bus common for the coprocessors. ADO is the least significant bit.
AD 16%- AD 19%	p.2 p.8 p.1 (wired or).	The four most significant address bits.
/DEN	p.2 p.9 p.8 (wired or) p.1 (wired or) p.28 p.30	Data ENable. Used to enable the data buffers.
/NET IDENT	p.15	Configuration bit, indicationg that the local area network controller is present.
NET INT NET HOLD	p.14 p.4	NET controller INTerrupt to the proces sor. True when the net controller reques access to the processor bus.
QS0-QS1	p.1 (wired or)	80186 queue status.
/S0%-/S2%	p.2 p.8(wired or) p.1 (wired or)	Bus status signals, indicating the kind of bus cycle being performed:

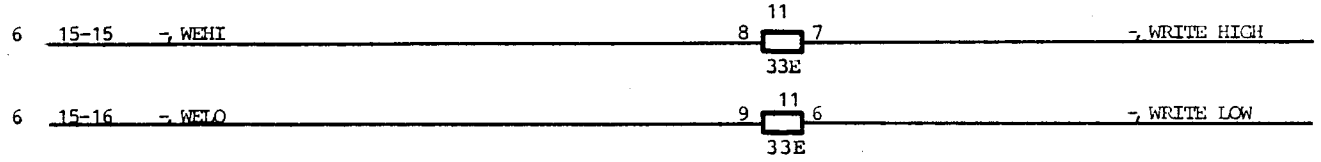
/S 2	1	0	Bus cycle
0	0	0	Interrupt ACK
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	HALT
1	0	0	Code fetch
1	0	1	Read Mem
1	1	0	Write Mem
1	1	1	Passive

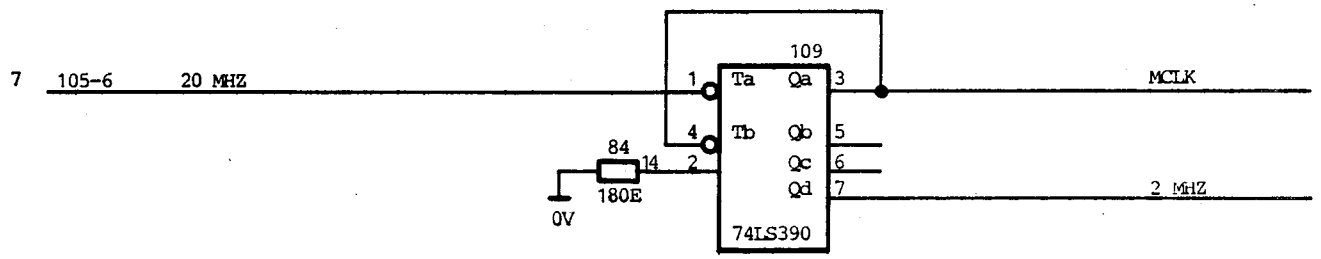

0V
J10
2
1
AD 0
AD 1
4
3
AD 2
AD 3
6
5
AD 4
AD 5
8
7
AD 6
AD 7
10
9
AD 8
AD 9
12
11
AD10
AD11
14
13
AD12
AD13
16
15
AD14
AD15
1 24-64 -, BHE*
18
17
AD16*
20
19
AD17*
AD18*
22
21
AD19*
0V
1 24-57 RESET
24
23
26
25
NET HOLD
4 20-12 NET HLDA
28
27
QS 0
30
29
QS 1
-, DEN
32
31
-, S 0*
-, S 1*
34
33
-, S 2*
15 85-12 ARDY
36
35
0V
38
37
-, NETIDENT
TEST
40
39
1 24-56 CPUCLK
42
41
1 24-28 -, PCS 2
NETINT
44
43
+5V
46
45
+12V
48
47
50
49
KNEH 840524 MLA

Signal	Destination	Description
CSYNC	J3 J5	Ored function of the horizontal synchronization and vertical synchronization pulses.
/MEM IDENT0- /MEM IDENT1	p.15 (wired or)	Indicates the memory configuration: /MEM IDENT 0 1 Memory Size 0 0 768 K bytes ram 0 1 1 M - - 1 0 384 K - - 1 1 256 K - -
MCLK	p.28	CLocK signal (10MHz) to the iSBX interface.
POK	p.1	Power OK signal generated from the power supply (+5V) and by a RESET push-button.
/RAS0 /RAS1 /RAS2	p.25 p.26 p.27	Row address Select to the dynamic memory chips. RAS0 address 0 - 20000H. RAS1 address 20000H - 40000H. RAS2 address 40000H - 60000H.
VSYNC IN	p.8	Synchronization signal to the 82730 coprocessor to synchronize the picture frame to the power frequency (50Hz).
/WRITE HIGH	p.25 p.26	Write enable to the upper bank of memory (bit 8-15).
/WRITE LOW	p.25 p.26	Write enable to the lower bank of memory (bit 0-7),
X0,X1	p.27	Indicates the type of the memory board expansion present. X0 X1 Function 1 1 no memory expansion 1 0 128 K expansion 0 1 256 K expansion 0 0 512 K expansion
X2	p.27	address decoder output. True in the area 40000H - 60000H.
2MHZ	p.20	2MHZ clock signal to the sound generator.

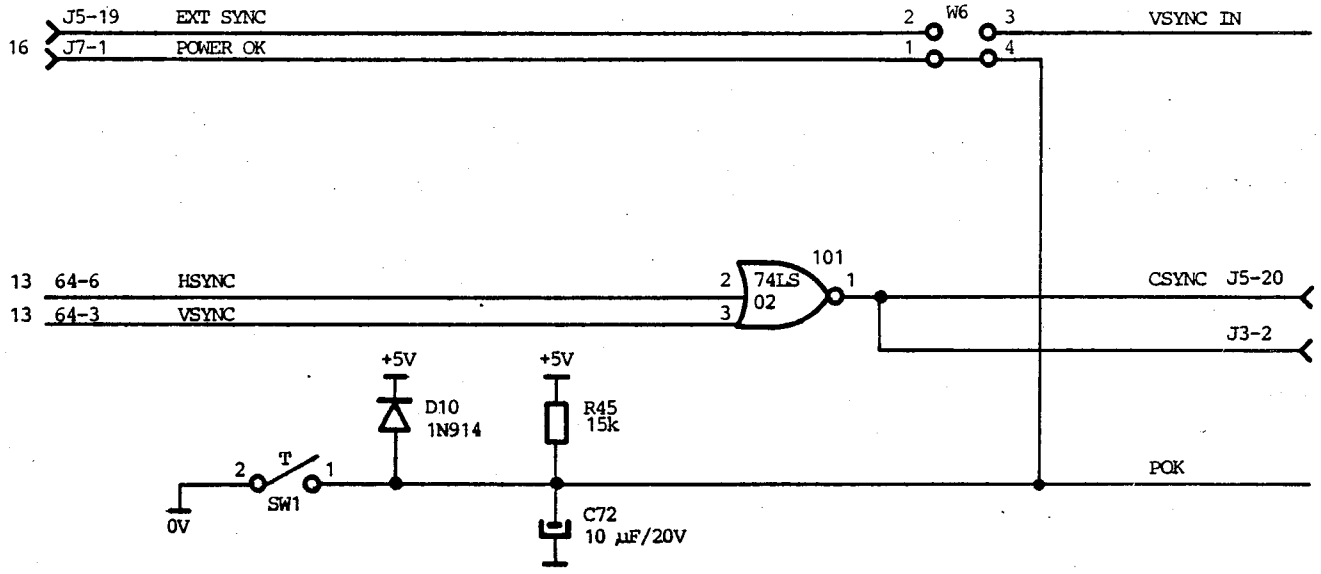


A19	A18	A17	RAS
0	0	0	-, RAS 0
0	0	1	-, RAS 1
0	1	0	-, RAS 2

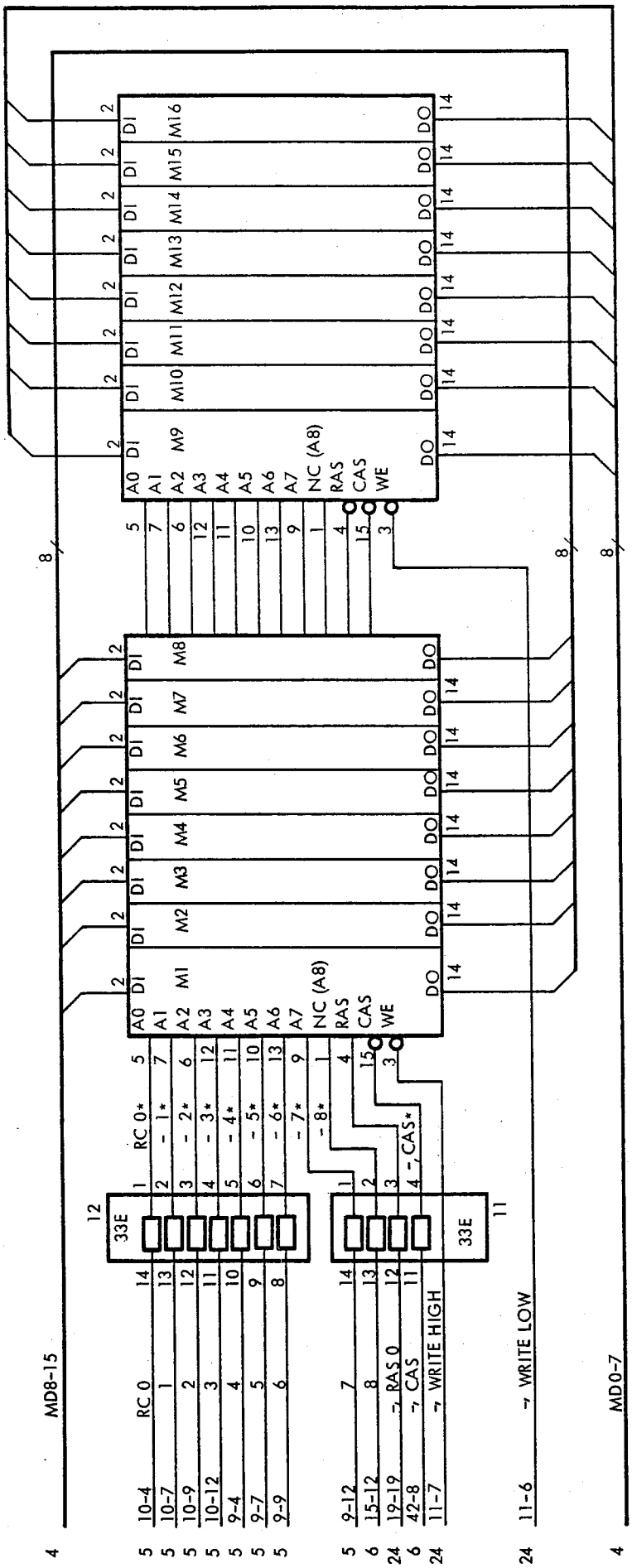




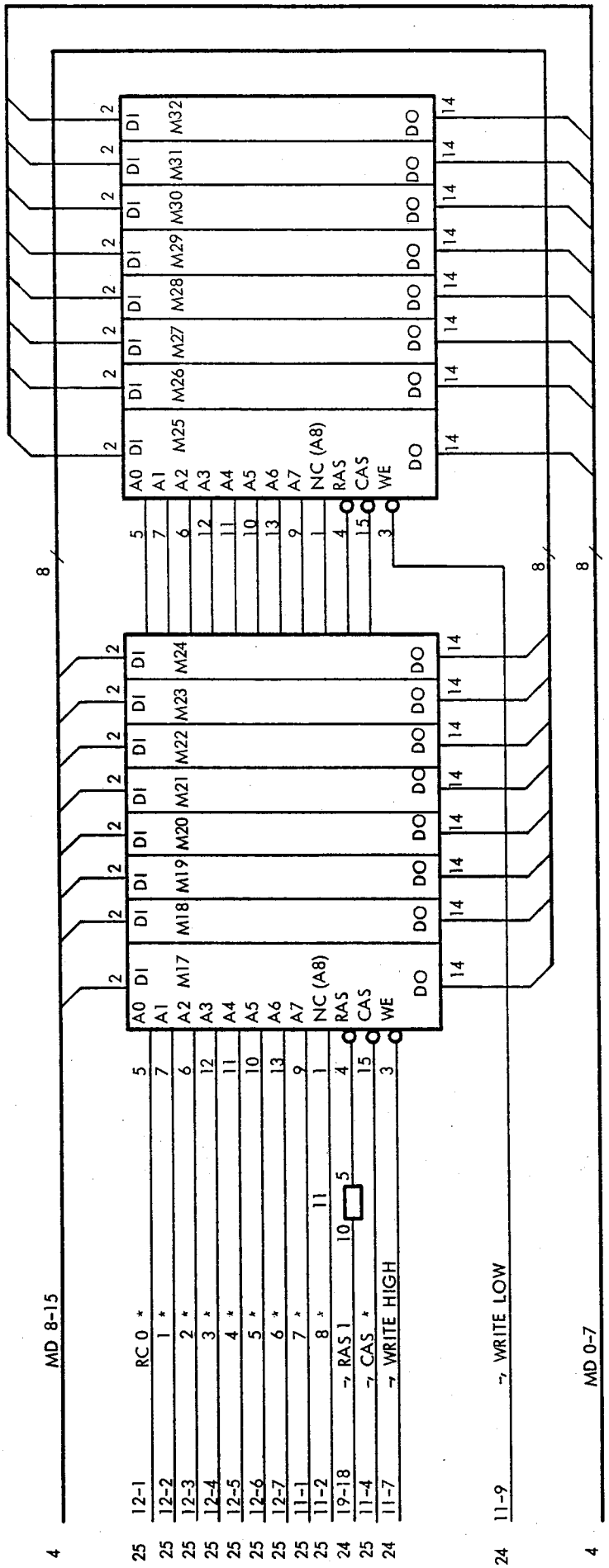
W6 (1-4) jactory set



KNEH 840524 MLA

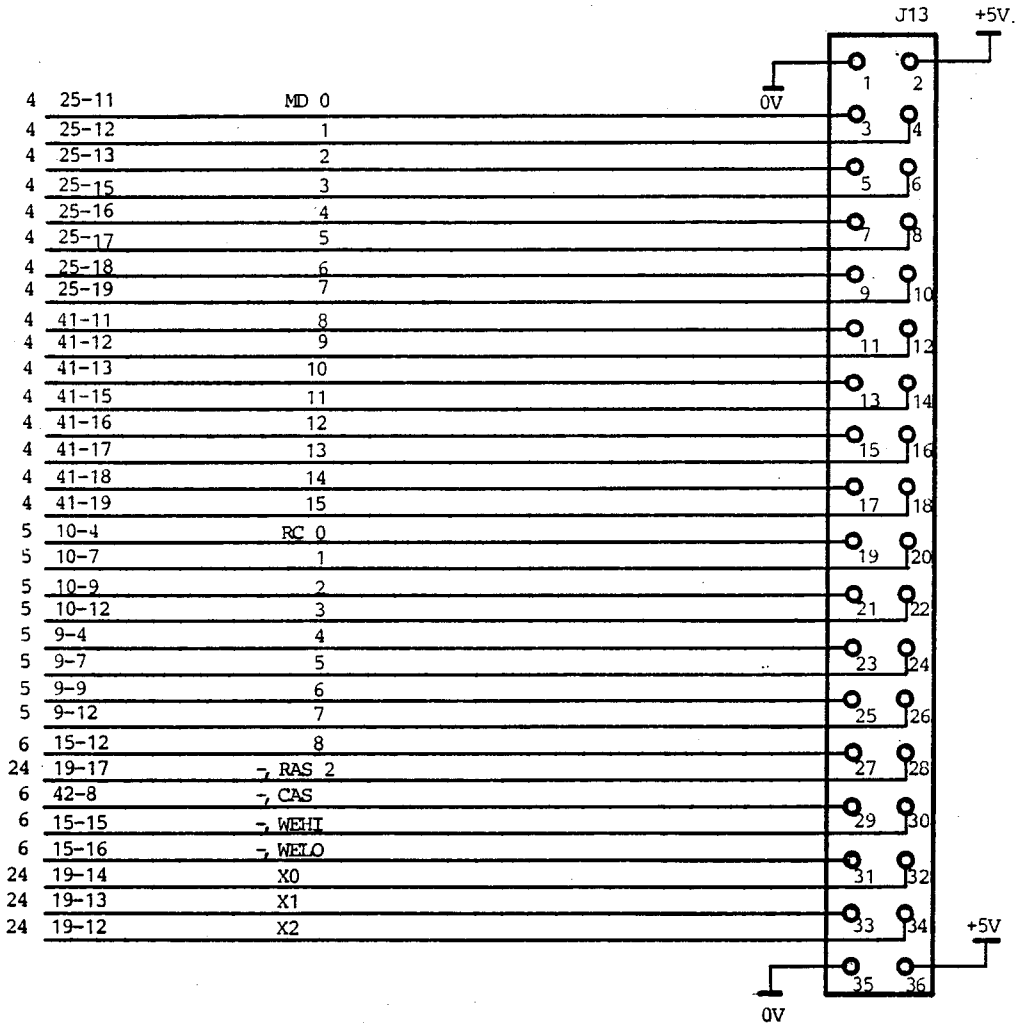


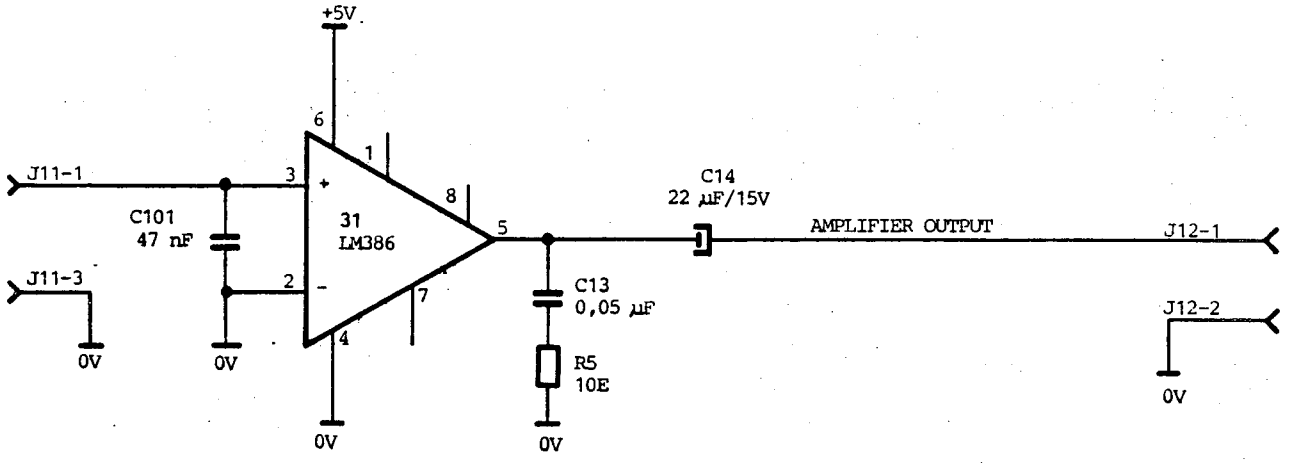
KNEH 840524 MLA



KNEH 840524 MLA

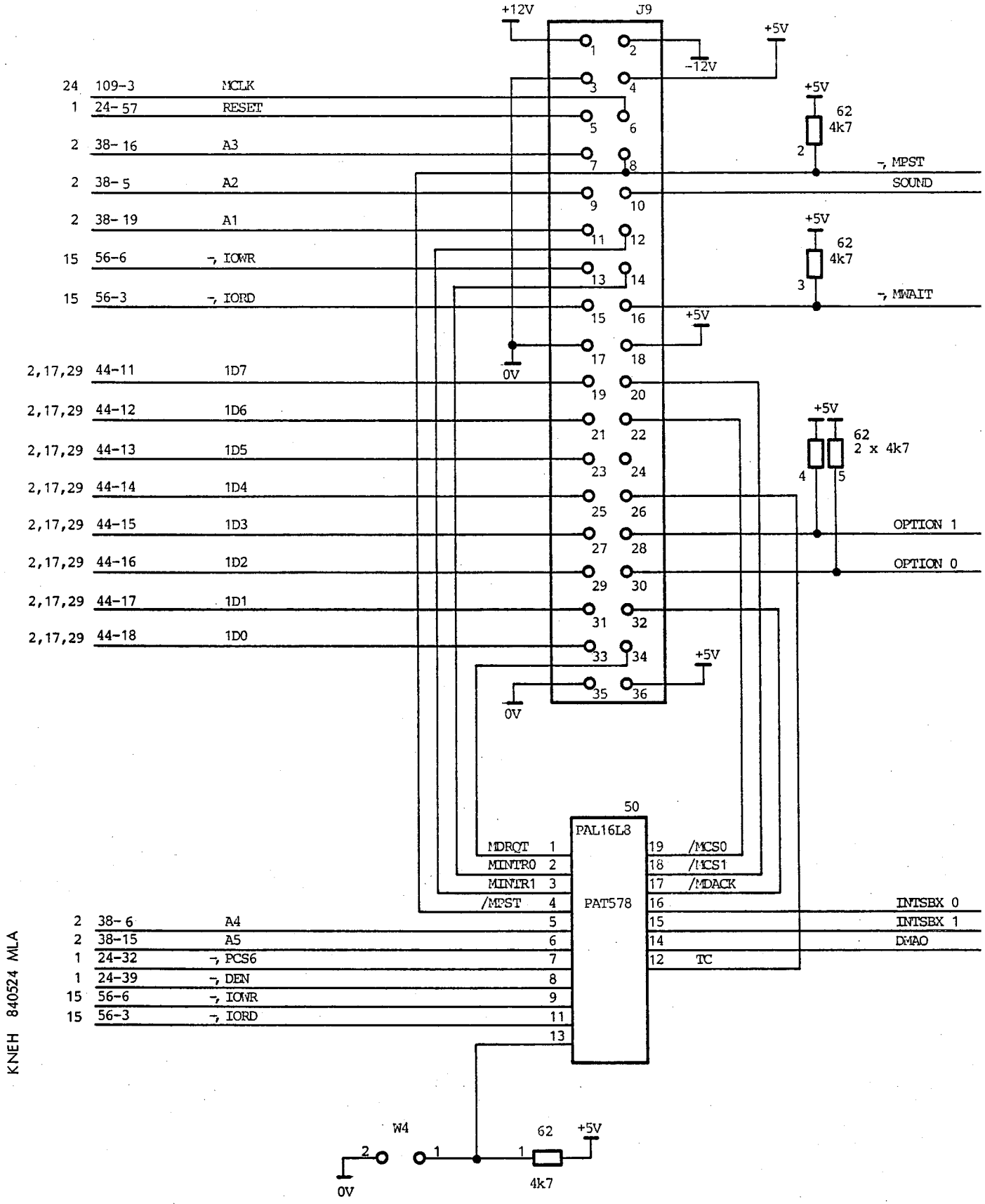
Signal	Destination	Description
AMPLIFIER OUTPUT	J12	Sound signal to an external loudspeaker. This is an amplified version of the internal audio signal p.20).



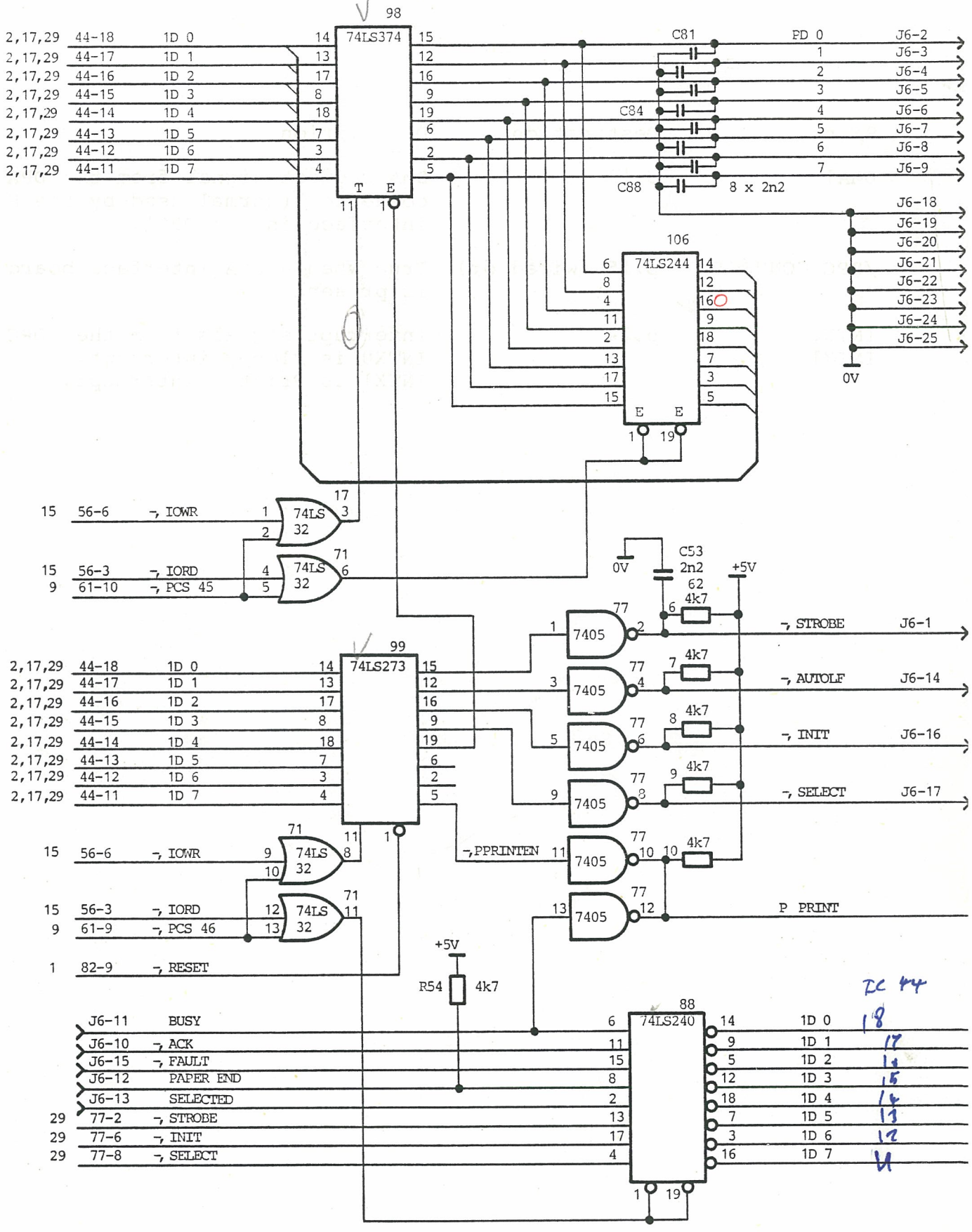


KNEH 840524 MLA

Signal	Destination	Description
DMA0	p.14	DMA request from the iSBX module.
INTSBX0- INTSBX1	p.1	INTerrupt signals from the iSBX modules. Connected to INT1 and INT3 on the 80186 microprocessor.
/MPST	p.15 (wired or)	True if an iSBX module is present.
/MWAIT	p.15	Request the processor to insert wait states.
OPTION 0- OPTION 1	p.15 (wired or)	Optional status signals from the iSBX bus. Refer to the iSBX manual for the meaning of these signals.

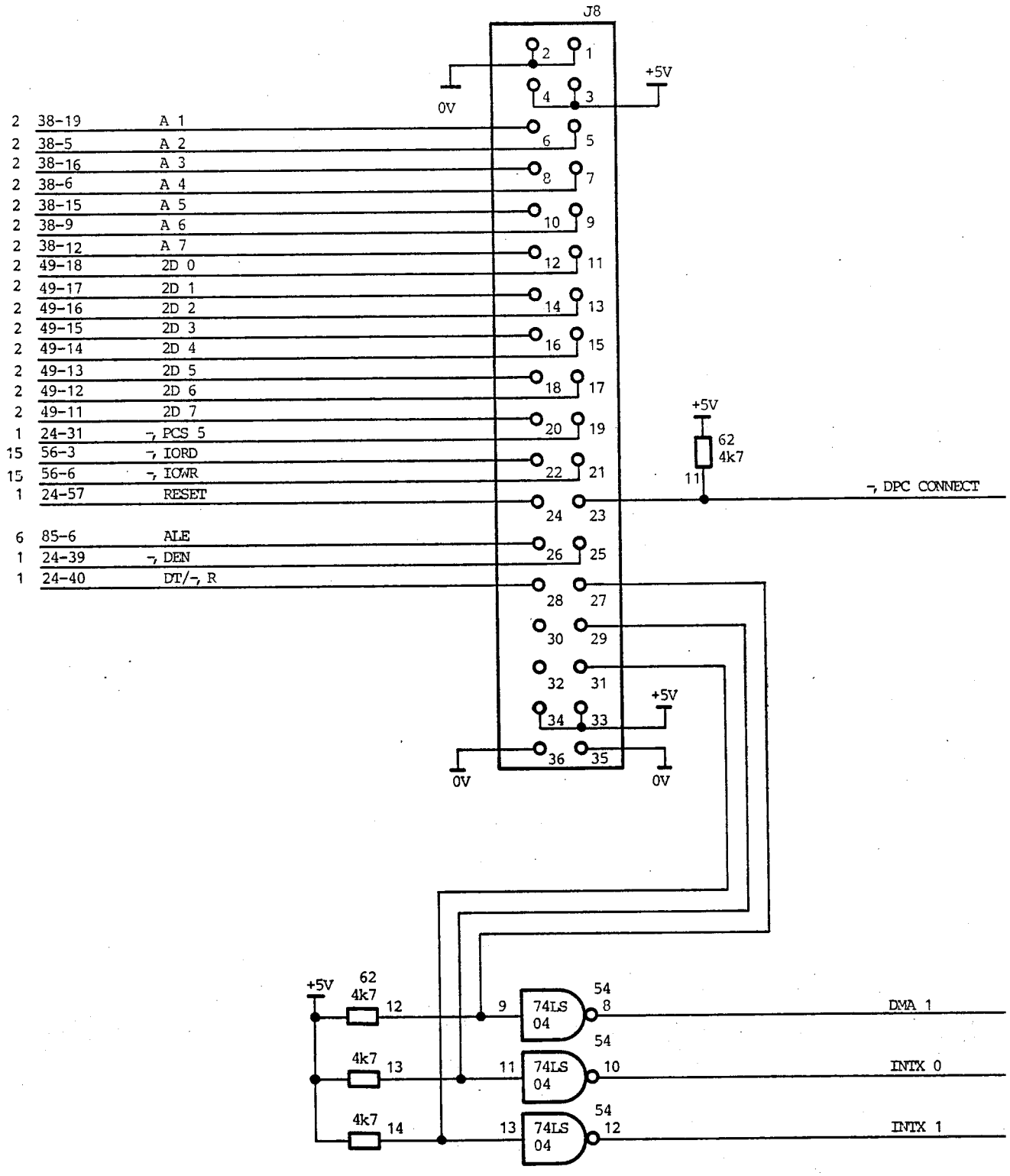

+12V
J9
+5V
-12V
24 109-3 MCLK
1 24-57 RESET
2 38-16 A3
2 38-5 A2
2 38-19 A1
15 56-6 -, IOWR
15 56-3 -, IORD
0V
+5V
62
4k7
-, MPST
SOUND
-, MWAIT
2,17,29 44-11 1D7
2,17,29 44-12 1D6
2,17,29 44-13 1D5
2,17,29 44-14 1D4
2,17,29 44-15 1D3
2,17,29 44-16 1D2
2,17,29 44-17 1D1
2,17,29 44-18 1D0
62
2 x 4k7
OPTION 1
OPTION 0
50
PAL16L8
PAT578
MDRQT
MINTR0
MINTR1
/MPST
/MCS0
/MCS1
/MDACK
INTSBX 0
INTSBX 1
DMAO
TC
2 38-6 A4
2 38-15 A5
1 24-32 -, PCS6
1 24-39 -, DEN
15 56-6 -, IOWR
15 56-3 -, IORD
W4
4k7
KNEH 840524 MLA

Signal	Destination	Description
/AUTOLF	J6	AUTO Line Feed control signal.
/INIT	p.29 J6	Reset signal to the printer.
PD0-7	J6	Printer Data bit 0-7.
pprint	p.14	Printer interrupt signal.
/SELECT	p.29 J6	Selection signal to the printer.
/STROBE	p.29 J6	Data STROBE signal to the printer.
D0-7	p.18 p.2 (wired or) p.17 p.20 p.28 p.12	I/O Bus 1.



KNEH 840524 MLA

Signal	Destination	Description
DMA1	p.14	DMA request signal from the DPA connector (normal used by the Floppy interface in the DPC).
/DPC CONNECT	p.15 (wired or)	True when a DPA interface board is present.
INTX0 INTX1	p.14	Interrupt signals from the DPC. INTX0 is Floppy interrupt. INTX1 is Printer interrupt.



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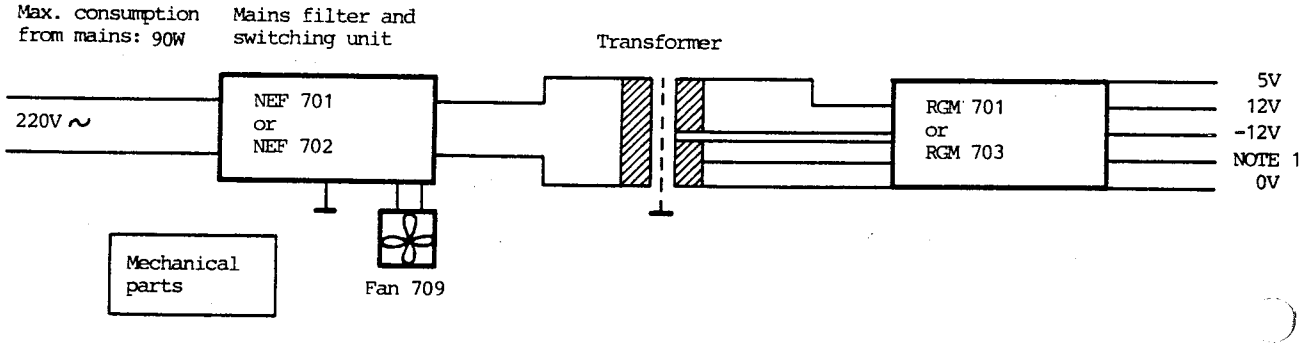
5. POWER SUPPLY 5.

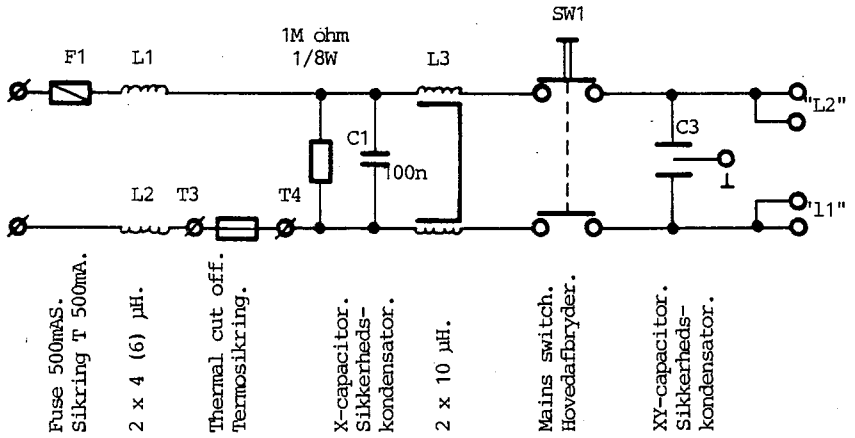


NOTE 1:

For RGM 701: AC-signal for monitor sync.
For RGM 703: Power OK (POK) signal.

Pow 749 is equipped with NEF 701 and RGM 701.
POW 751 is equipped with NEF 702 and RGM 703.
The transformer is introduced with the module name TRF 701.
This will be changed to TRF 703 when it has reached its final outlook.

Fig. 11. Module Survey of the POW749/751



PARTS LIST / STYKLISTE

RC part No	Description / Beskrivelse.
2101027	Fuse holder
2102024	500 mA fuse (slow 7 træg)
1901168	4 (6) µH coil
2118002	Thermal cut off
2003002	100n X-capacitor
1901167	2 x 10 mH choke
1510029	Mains switch
2003007	XY-capacitor
1402099	Screw terminal

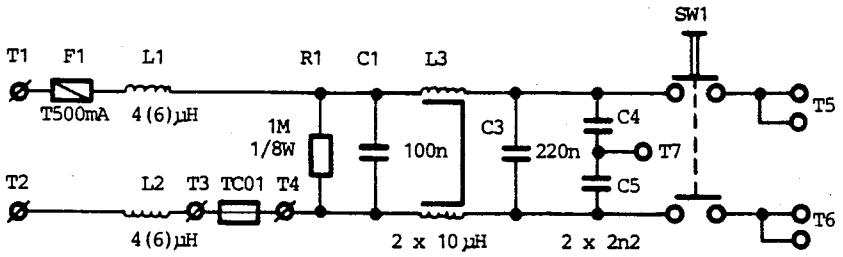
WARNING!

The NEF 701 module has vital influence on the electrical safety of the equipment in which it is mounted. Hence in case of repair it is of importance that defective are only replaced by parts of equivalent quality (see RC part No's in the parts list) and that the module is remounted as original.

ADVARSEL!

Modulet NEF 701 har vital betydning for den elektriske sikkerhed i det apparat det er monteret i. Det er derfor vigtigt, i tilfælde af reparation, at defekte dele kun erstattes med nye dele af tilsvarende kvalitet (se RC-part nr. i styklisten) og at modulet i øvrigt monteres helt som oprindeligt.

Fig. 12. NEF701, Mains Filter Unit



PARTS DESCRIPTION / KOMPONENTBESKRIVELSE

Component	Description	RC part No
F1	Fuse holder / sikringsholder	2101027
	Fuse / sikring 500 mA slow / træg	2102024
L1, L2	4 (6) µH coil / spole	1901168
TC01	Thermal cut off / termosikring 76°C	2118002
R1	1M, 1/8 W resistor / modstand	1103129
C1	X-capacitor / sikkerhedskondensator 100n	2003002
L3	Current compensated shoke / strøm-kompenseret drossel 2 x 10 mH	1901167
C3	X-capacitor / sikkerhedskondensator 220n	2003003
C4, C5	Y-capacitor / sikkerhedskondensator 2n2	2003005
SW1	Mains switch / hovedafbryder	1510029
T1, T2, T3, T4	Screw terminal / skrueterminal	1402099

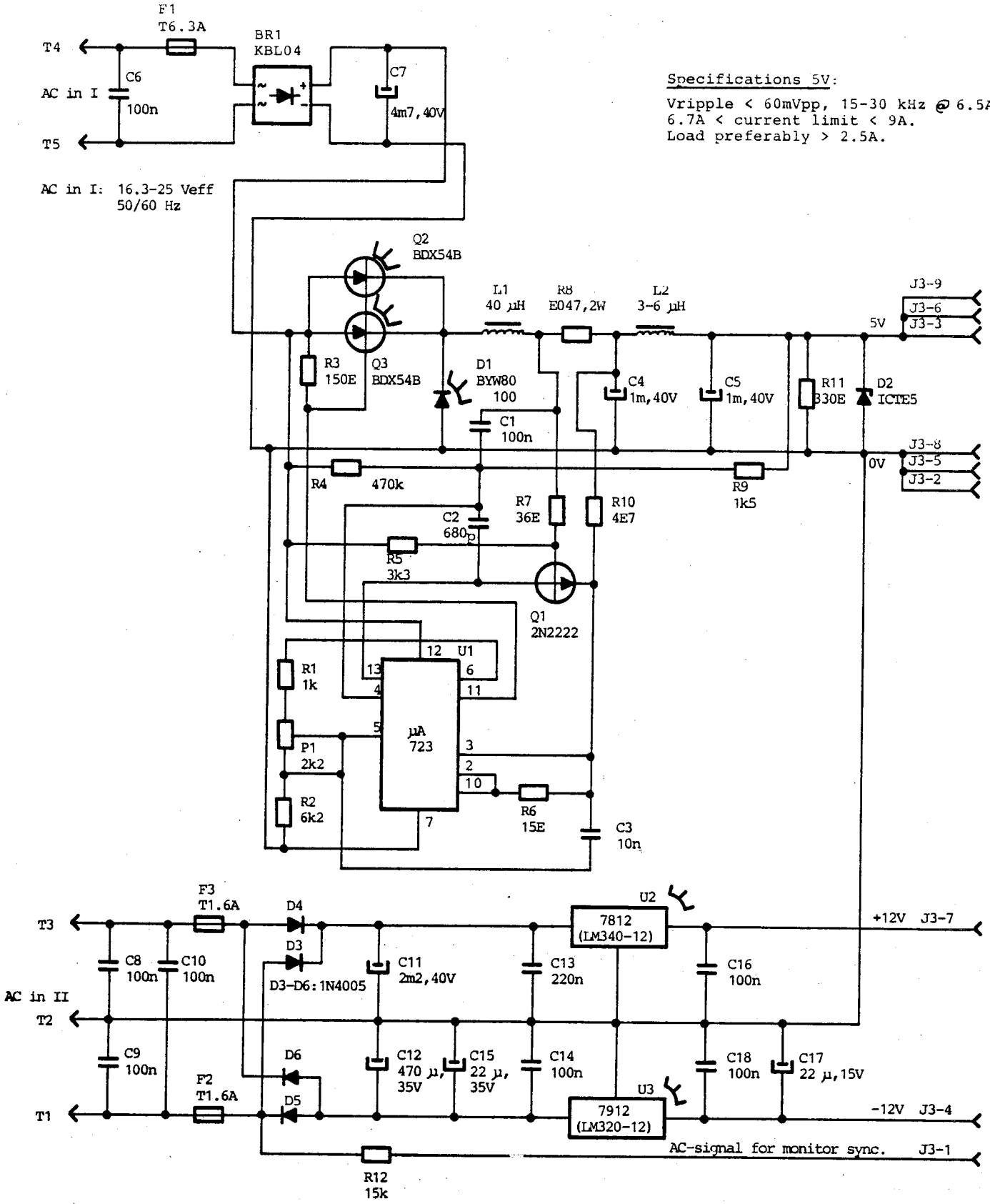
WARNING!

The NEF 702 module has vital influence on the electrical safety of the equipment in which it is installed. Hence in case of repair it is of importance that defective parts are only replaced by parts of equivalent quality (see RC parts No's in the parts description) and that the module is remounted as original.

ADVARSEL!

Modulet NEF 702 har vital betydning for den elektriske sikkerhed i det apparat, det er monteret i. Det er derfor vigtigt, i tilfælde af reparation, at defekte dele kun erstattes med nye dele af tilsvarende kvalitet (se RC-part nr. i komponentbeskrivelsen) og at modulet i øvrigt monteres helt som oprindeligt.

Fig. 13. NEF702, Mains Filter Unit



AC in II: 2 x 14-19.8 Veff, 50/60Hz.
To be supplied from transformator with two symetrical windings with one outlet in common (centertap).

T1-T5: Spade terminals.

Specifications +12V:

As specified for 7812 except that C11 will only guarantee 0.6A without mains ripple.

Specifications -12V:

As specified for 7912 except that C12 will only guarantee 0.1A without mains ripple.

Fig. 14. RGM701, Schematic Diagram

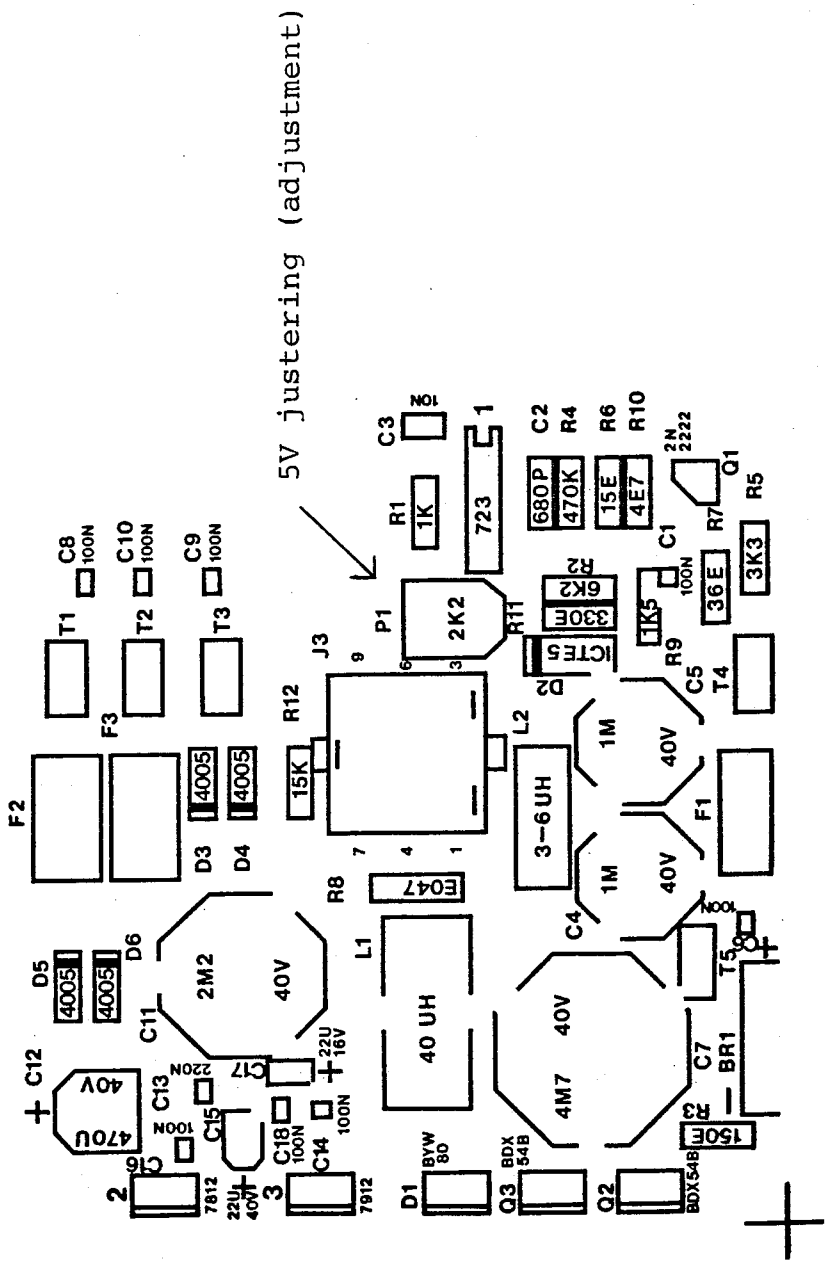
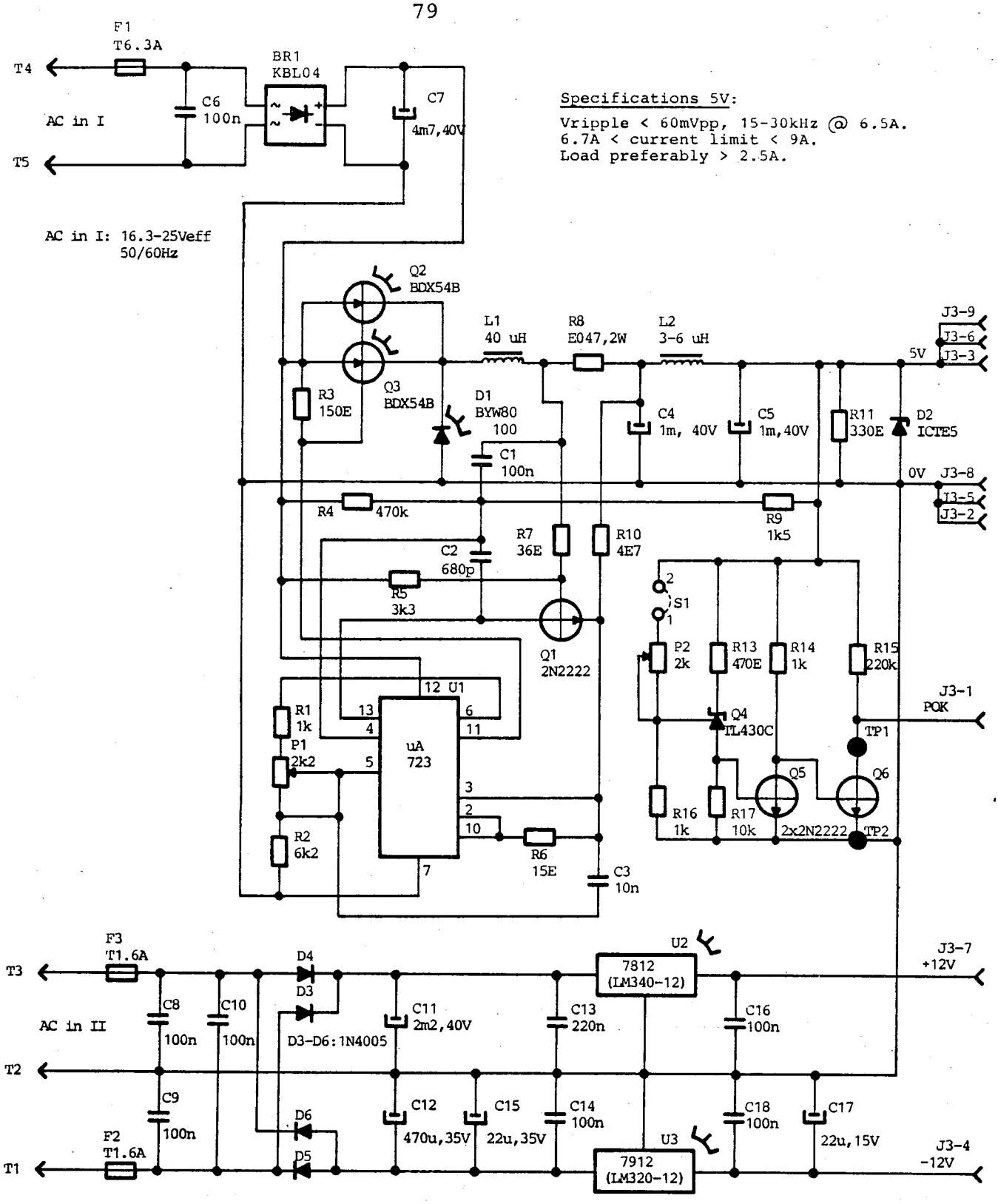


Fig. 15. RGM701 Assembly Drawing



AC in II: 2 x 14-19.8Veff, 50/60Hz.
To be supplied from transformator with two symetrical windings with one outlet in common (centertap).

T1-T5: Spade terminals.

Specifications 5V:

Vripple < 60mVpp, 15-30kHz @ 6.5A.
6.7A < current limit < 9A.
Load preferably > 2.5A.

Specifications +12V:

As specified for 7812 except that C11 will only guarantee 0.6A without mains ripple.

Specifications -12V:

As specified for 7912 except that C12 will only guarantee 0.1A without mains ripple.

840501 GBJ 840917 MLA

Fig. 16. RGM703, Schematic Diagram

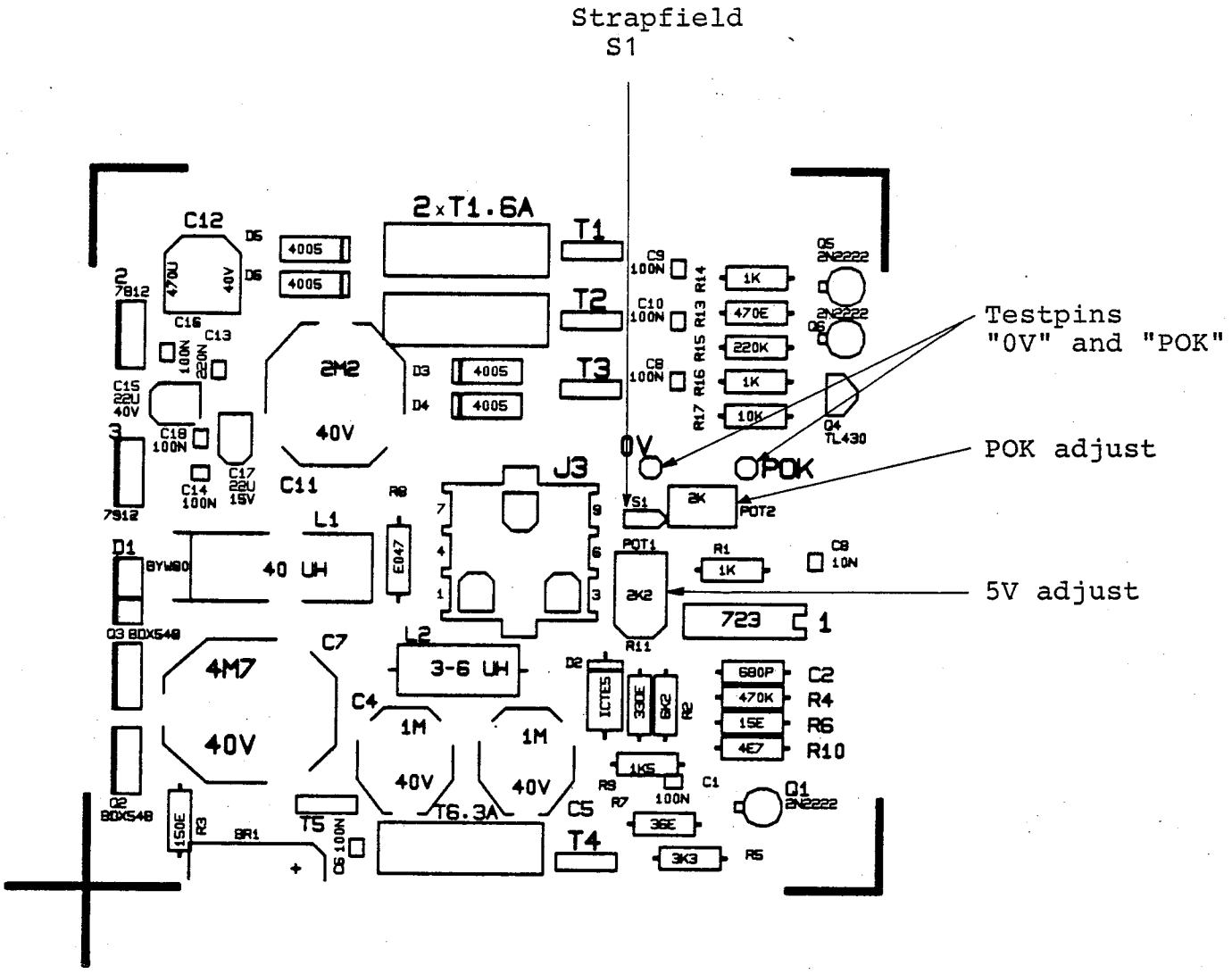


Fig. 17. RGM703 Assembly Drawing

6. ASSEMBLY DRAWINGS 6.

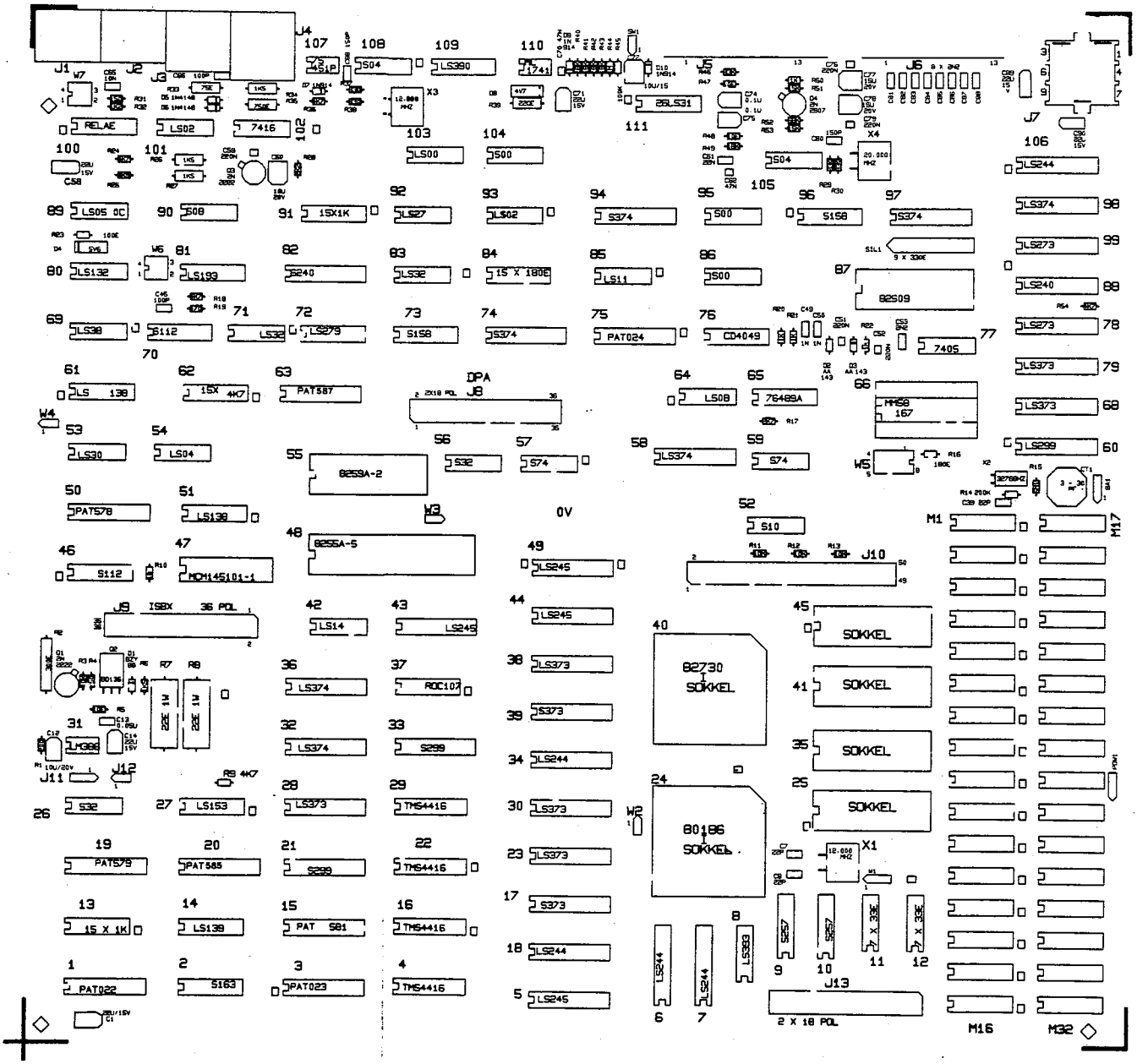
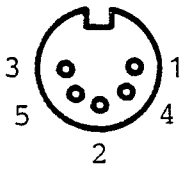


Fig. 18. CPU740 Assembly Drawing

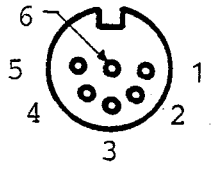
7. JACK LISTS 7.

KEYBOARD J1



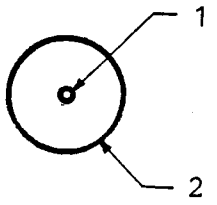
PIN-nr.	FUNCTION
1	CLOCK
2	DATA
3	-
4	OV
5	+12V/500mA

AUDIO J3



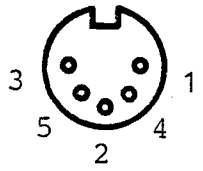
PIN-nr.	FUNCTION
1	Gx
2	CSYNC
3	OV
4	Rx
5	Bx
6	AUDIO

COMP VIDEO J4



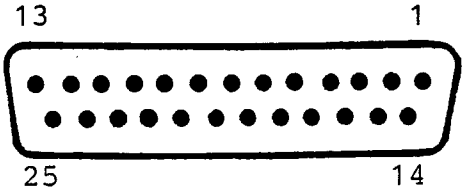
Pin-nr.	FUNCTION
1	VIDEO SIGNAL
2	0V

CASS J2



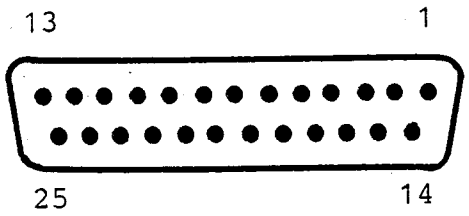
PIN-nr.	FUNCTION	DESCRIPTION
1	MOTOR CONTROL	RELAY CONTACT
2	OV	
3	MOTOR CONTROL	6VDC, MAX 1.0A, CLOSE FUNCTION
4	DATA IN	500nA at +/- 13V, 1000-2000 bps
5	DATA OUT (MIC)	250 microAmpere ved 0.68V

MONITOR J5



PIN-nr.	FUNCTION	PIN-nr.	FUNCTION
1	+Ix	14	OV
2	-Ix	15	-, 22kHz SELECT
3	+Rx	16	OV
4	-Rx	17	AUDIO OUT
5	+GX	18	OV
6	-Gx	19	VSYNC IN
7	+BX	20	CSYNC
8	-Bx	21	+5V
9	HSYNC	22	OV
10	OV	23	+12V
11	VSYNC	24	OV
12	OV	25	-12V
13	MONOCHROME		

LOCAL PRINTER J6 PRINTER



PIN-nr.	FUNCTION	PIN-nr.	FUNCTION
1	-,STROBE	14	-,AUTOLF
2	PD0	15	-,FAULT
3	PD1	16	-,INIT
4	PD2	17	-,SELECT
5	PD3	18	OV
6	PD4	19	OV
7	PD5	20	OV
8	PD6	21	OV
9	PD7	22	OV
10	-,ACK	23	OV
11	BUSY	24	OV
12	PAPER END	25	OV
13	SELECTED		

POWER CONNECTOR J7

PIN-no	Signal name
1	POK
2	OV
3	+5V
4	-12V
5	OV
6	+5V
7	+12V
8	OV

A. INDICES

A.

A.1 Survey of Figures

A.1

RETURN LETTER

Title: RC759 Central Processing Unit RCSL No.: 99 0 00768

A/S Regnecentralen af 1979/RC Computer A/S maintains a continual effort to improve the quality and usefulness of its publications. To do this effectively we need user feedback, your critical evaluation of this manual.

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Do you find errors in this manual? If so, specify by page.

How can this manual be improved?

Other comments?

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