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RC779 - 1/2
TECHNICAL MANUAL

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Abstract: This paper contains all the technical documentation for the Disk/Printer unit to the PICCOLINE microcomputer.

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APPENDICES:

1. INTRODUCTION

The RC779 Disk/Printer unit contains a Flexible disk controller incl. drives and parallel Centronic interface. These interfaces can be shared by up to 4 connected Piccoline microcomputers. The microcomputers set a Flag, when they want access to either the Flexible disk or the Printer. When the requested unit is free, control over this unit is given to the requesting microcomputer. The microcomputer remove the connection by resetting the request Flag. The Disk/Printer unit is equipped with indicators, showing which microcomputer at this moment has access to the Flexible Disk or to the Printer. The Disk/Printer unit is connected to the Piccoline as shown on figure 1. Figure 2 shows the internal modules.

2. Specifications

Flexible disk drive

Capacity (8 sectors/track)	1262KBytes
Track density	96TPI
Cylinders	77
Tracks	154
Encoding Methode	MFM
Rotation rate	500K bits/sec
Access Time	
average	91ms
track to track	3ms
setting time	15ms
Head load time	50ms
Motor Start time	1sec

Printer interface

Centronic compatible interface.

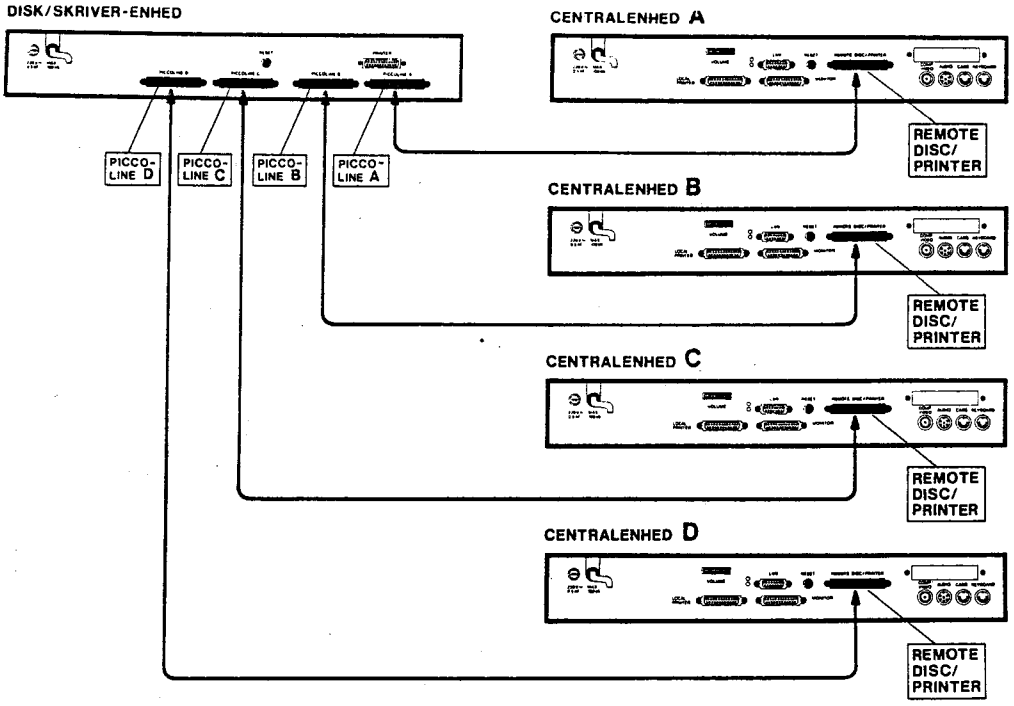


Fig. 1. Piccoline Connection

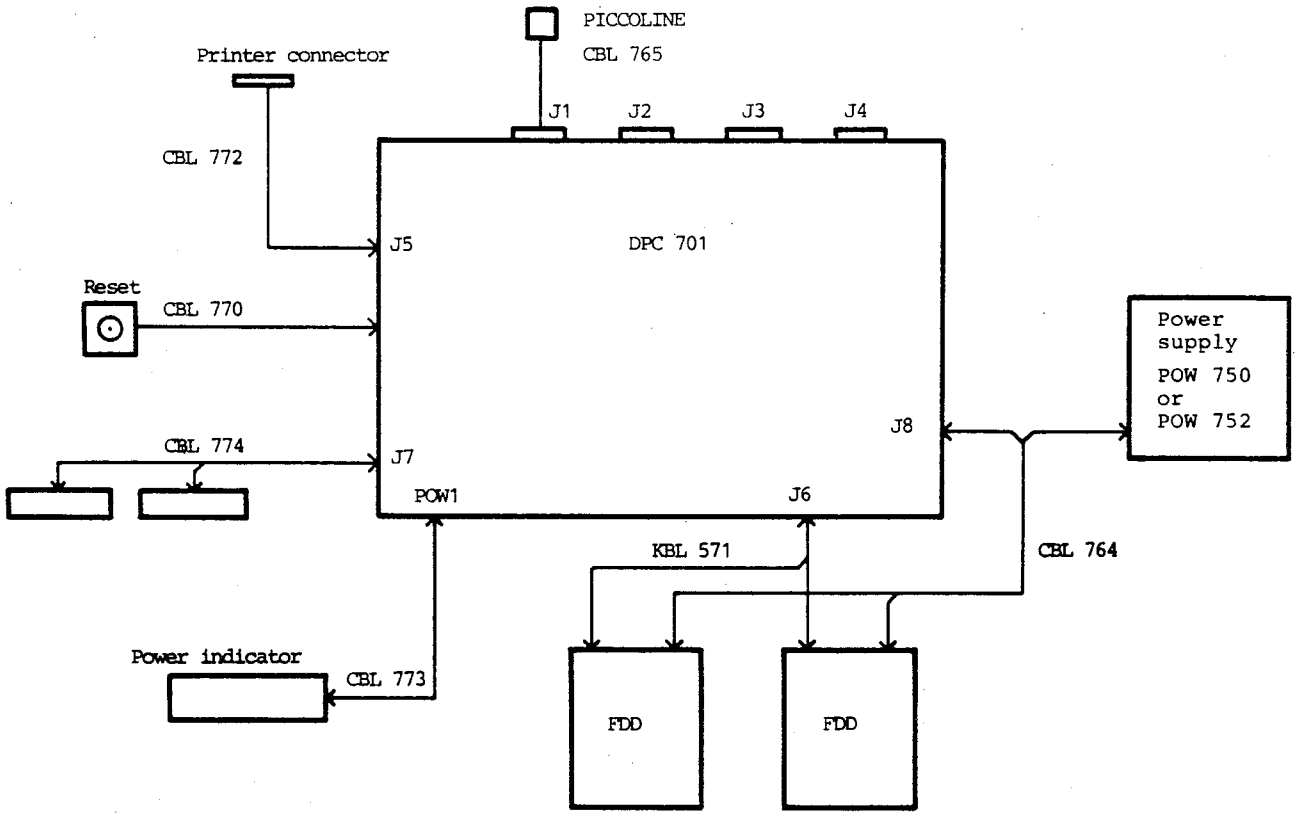


Fig. 2. Internal Cabling

3. FUNCTIONAL DESCRIPTION

Refer to the blockdiagram on figure 3.

The DPC701 module is logical split up into the following parts:

- Piccoline interface
- Arbiter circuit
- Floppy interface
- Printer interface

Each of these modules are further described in the following subsections.

3.1 Piccoline interface

This module contains balanced drivers/receivers for the Piccoline bus, I/O decoder/Flags, Floppy bus interface and Printer interface.

This module is identical for each Piccoline connection (A,B,C and D).

Piccoline interface A (channel 0) is shown on logic diagrams p.1 - p.4.

Piccoline interface B (channel 1) is shown on logic diagrams p.5 - p.8.

Piccoline interface C (channel 2) is shown on logic diagrams p.9 - p.12.

Piccoline interface D (channel 3) is shown on logic diagrams p.13 - p.16.

3.1.1 Balanced transceivers

26LS31 is used as driver circuit and 26LS32 as receiver circuit.

The 8 bit bus, EXP BUS 0-7, is a multiplexed address/data bus.

The address (/PCS 5 and A1-A7) supplied during the address phase is latched by EXPADD STROBE signal.

This address is supplied to the I/O Decoder/Flags circuit. During the data phase the EXP BUS 0-7 is controlled by EXP IORD/ IOWR.

A RESET signal is supplied to reset the interface. This RESET signal is true if the current Piccoline is powered down or the cable is removed.

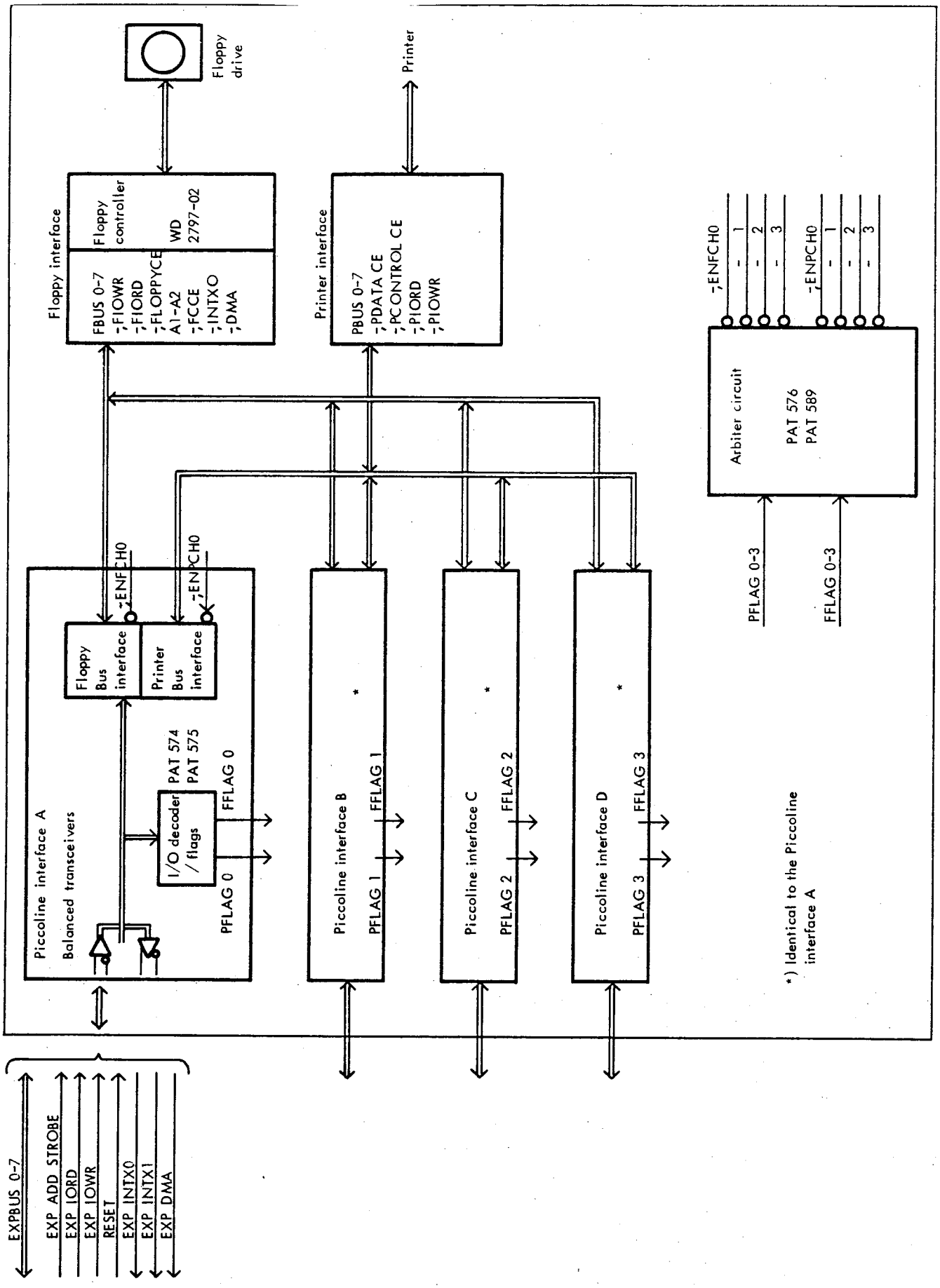
3 control signals are send back to the Piccolien, 2 interrupts and 1 DMA signal.

EXP INTX0 transfer interrupts from the Floppy interface.
EXP INTX1 transfer interrupts from the Printer interface.
EXP DMA transfer data request from the Floppy interface.

3.1.2 I/O Decoder/flags

3.1.2

This module is built with two PAL-circuits, PAT574 and PAT575. This module too supplies the two reservation request flags, PFLAG for printer reservation and FFLAG for floppy reservation, to the arbiter circuit.



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DPC 701 Blockdiagram for the DPC 701 module Fig. 3.0

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The Printer request flag (FPLAG) and the Floppy request flag (FFLAG) is set/reset by programmed output instructions (refer to figure 4 for device numbers). The flags are reset by pushing reset on the corresponding Piccoline or pushing reset on RC779.

I/O device (hex)	Direction	Description
28E	0	Set FFLAG
29O	0	reset FFLAG
28E	I	BUS 7=0 reservation of Floppy OK (the arbiter is stopped on this FFLAG).
		BUS 7=1 waiting upon Floppy
292	.0	Set PFLAG
294	0	reset PFLAG
292	I	BUS 7=0 reservation of Printer OK on this PFLAG).
		BUS 7=1 waiting upon Printer

Fig. 4. Reservation/Release Device Numbers

3.1.3 Floppy bus Interface

3.1.3

This module contains drivers and receivers for the interface to the Floppy controller. These bus circuits are enabled by the arbiter, when the Piccoline in question is given access to the Floppy.

3.1.4 Printer Bus Interface

This module contains drivers and receivers for the interface to the Printer controller. These bus circuits are enabled by the arbiter, when the Piccoline in question is given access to the Printer.

3.2 Arbiter Circuit

refer to logic diagram p. 17.

This module contains two PAL-circuits, one (PAT576) for Floppy arbitration, and one (PAT589) for Printer arbitration. These two PAL-circuits, each contains a 4-bit counter scanning the flags from the 4 Piccoline Interfaces.

PAT576 scannes the floppy request flags (FFLAG 0-3), and PAT589 scannes the printer request flags (PFLAG 0-3) When the counters meet a flag set, the counting is stopped and the corresponding enable output is set true. The counter will be stopped in this state until the flag is removed again; then the counter continues scanning for flags set.

3.3 Floppy Interface

Refer to logic diagrams p.25 and p.26.

This interface accepts the I/O devices, listed on figure 5.

I/O Device (hex)	Direction	Function
280	I	Read FDC status register
280	0	Write Control Command
282	I/O	Read/Write FDC track register
284	I/O	Read/Write FDC sector register
286	I/O	Read/Write FDC data register
288	0	Write FCR register

Fig. 5. Floppy I/O Device Table

The FCR register has the following layout:

BIT no. (0=LSB)	SIGNAL name	Description
0	Drive SeL	Selects between drives 0:Select drive 0 1:Select drive 1 A drive is only selected (ready) if its motor is on.
1 2	MOTOR 0 MOTOR 1	0: MOTOR OFF 1: MOTOR ON
3	Precomp	Enable write precompensation (150 ns).
4	-	not used
5	/DD	0: Dual density 1: Single density
6	-	not used.
7	READY CONTRO	0: ready from drive 1: ready always set

Fig. 6. FCR Register Layout

The floppy interface is built around a Western Digital floppy controller, WD2797-02.

On figure 7 is given a command/flag summary for this controller.

On figure 8 is given a status register summary.

COMMAND SUMMARY

A. Commands for Models: 2791, 2793

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

B. Commands for Models: 2795, 2797

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No. 15 MS delay E = 1, 15 MS delay (30 MS for 1 MHz)
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field: 00 / 01 / 10 / 11 L = 0: 256 / 512 / 1024 / 128 L = 1: 128 / 256 / 512 / 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset* I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

Fig. 7. Command/Flag Summary

STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a Zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

Fig. 8. Status Register Summary

3.4 Printer Interface

Refer to the logic diagram p.18.

This interface contains a data register, giving output data to the printer device. The contents of this register can be read back for test purpose. Another register gives the control signals to the printer device. This control signals together with the printer status signals can be read back.

The printer interface accepts the following I/O device numbers.

I/O divice (HEX)	Signal Direction	Description
28A	I/O	Read/write Printer Data register
28C	I/O	Read/write Printer Control register

Fig. 9. Printer I/O Device Numbers

4. FLOPPY ADJUSTMENT PROCEDURE 4.

(refer to figure 10)

Switch the power on to the Disk unit and wait 4-5 minutes before proceeding with the adjustment procedure.

a. Push reset on the Disk/Printer Unit, RC779

b. Insert the strap W4

c. Observe the pulse on T2 with an oscilloscope

d. Adjust on POT1 until the measured pulse is 225ns.

e. Observe frequency on T3

f. Adjust the variable capacitor CT1 until the frequency is 500 KHZ

g. Observe the pulse width on T1

h. Adjust POT2 for a pulse width of 150ns.

i. Remove strap W4

j. Push reset on RC779

k. Load the extended TESTs from diskette

l. Run the Floppy Head Timer adjust

m. Observe the pulse on T4

n. Adjust POT3 until the negative pulse lenght is 50ms.

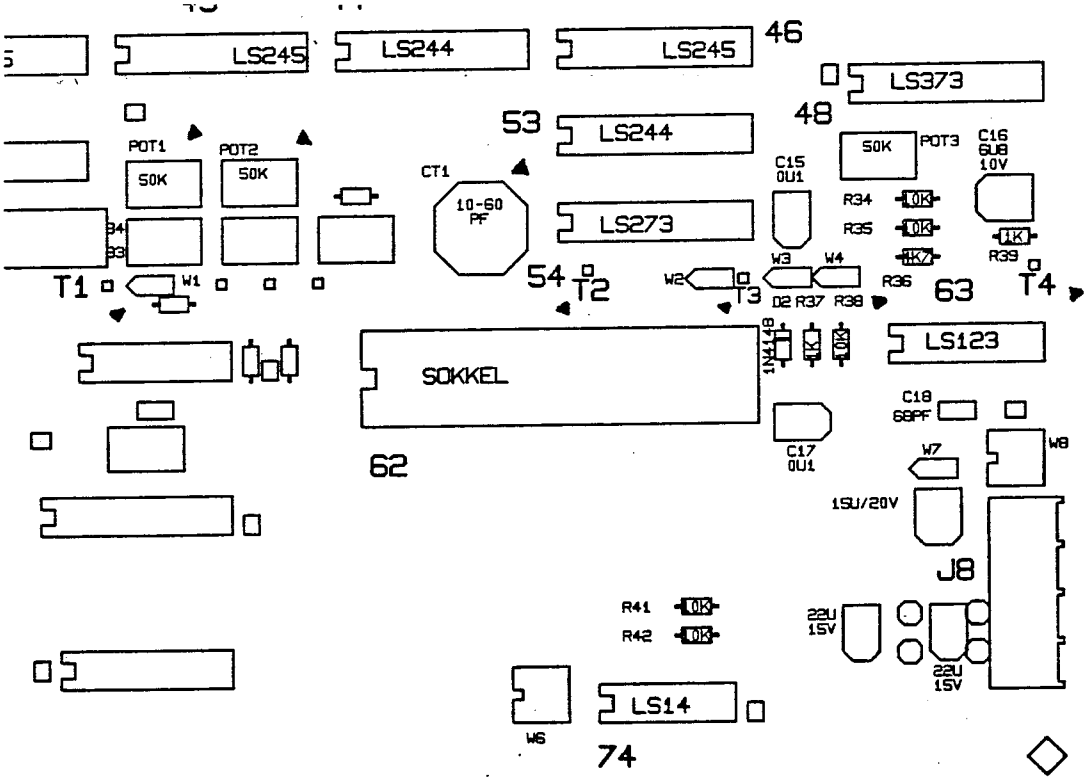
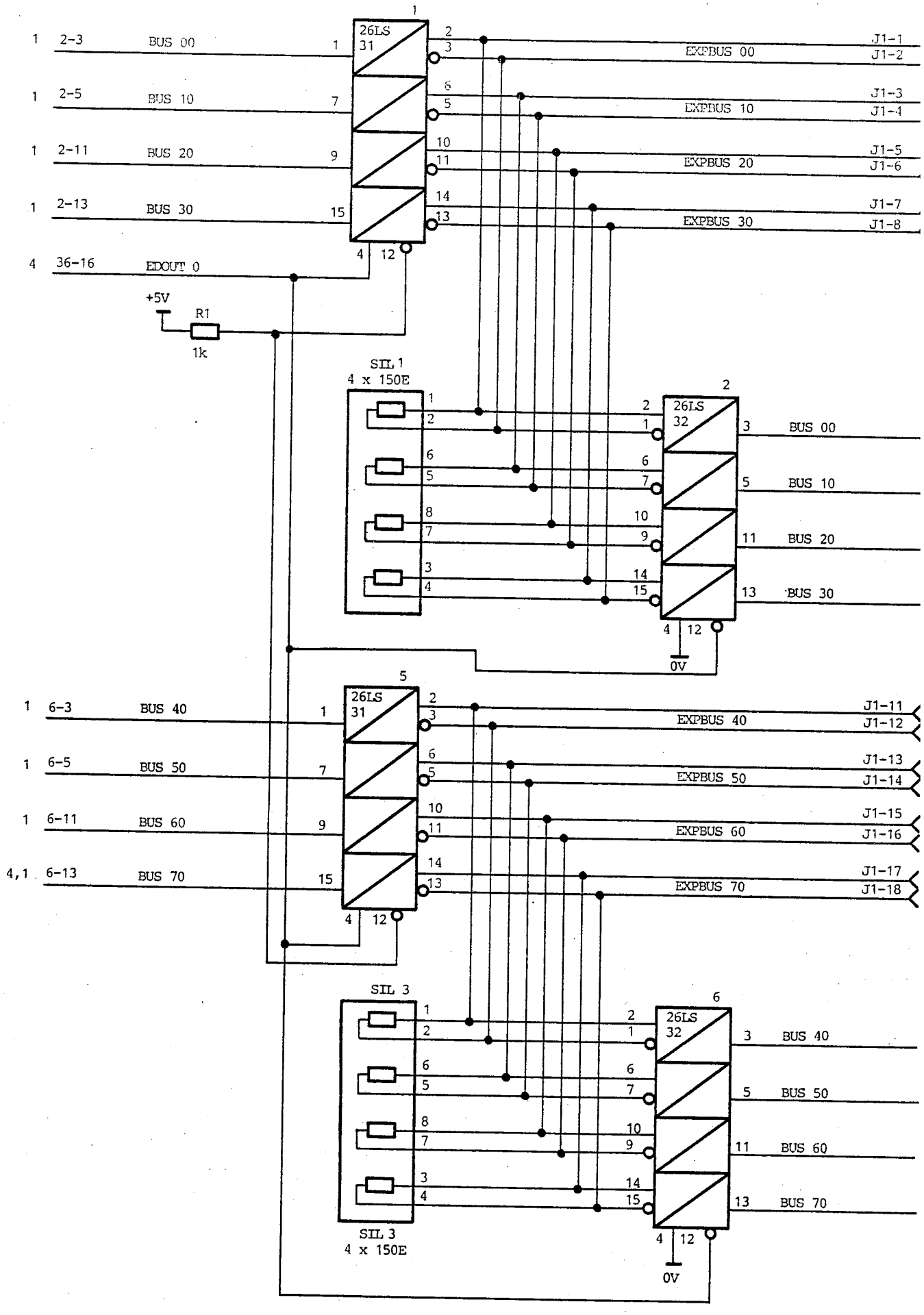


Fig. 10. Location of Floppy Adjust Circuits

5. DPC701 LOGIC DIAGRAMS

Signal	Destination	Description
BUS00-BUS70	p.2 p.3	Local bus for the interface to RC759 number A.
EXP BUS00- EXP BUS70	J1	The balanced bus to RC759 number A.



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DPC 701

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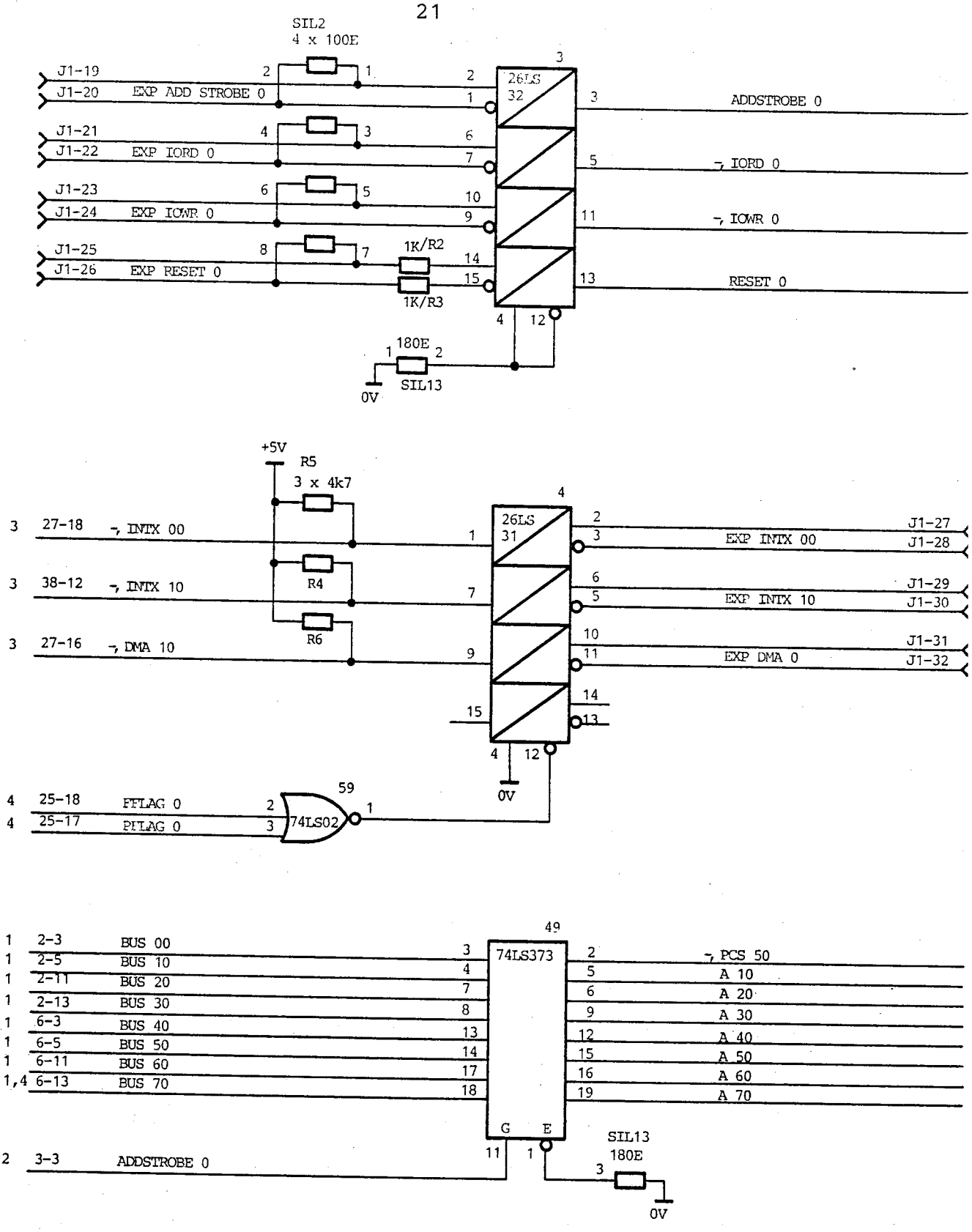
DATA BUS TRANSCEIVERS
CHANNEL 0
CIRCUIT DIAGRAM

Signal	Destination	Description
ADDSTROBE 0	p.2	ADDress STROBE, laching the address supplied on BUS0-7 during the address phase.
A10-A70	p.3 (A10-A20) p.4 (A10-A70)	Address bit 1 to 7.
EXP DMA0	J1	EXPander bus DMA request 0. Used by the Floppy interface.
EXP INTX00, EXP INTX10	J1	EXPander bus INTerrupts. INTX00 equals Floppy interrupts. INTX10 equals Printer interrupts.
/IORD 0	p.3 p.4	Input/Output Read Data strobe.
/IOWR 0	p.3 p.4	Input/Output WRite Strobe.
/PCS50	p.4	Peripheral Chip Select for I/O devices in the address area 280H-2FEH.
RESET 0	p.4	RESET from RC759 number A.



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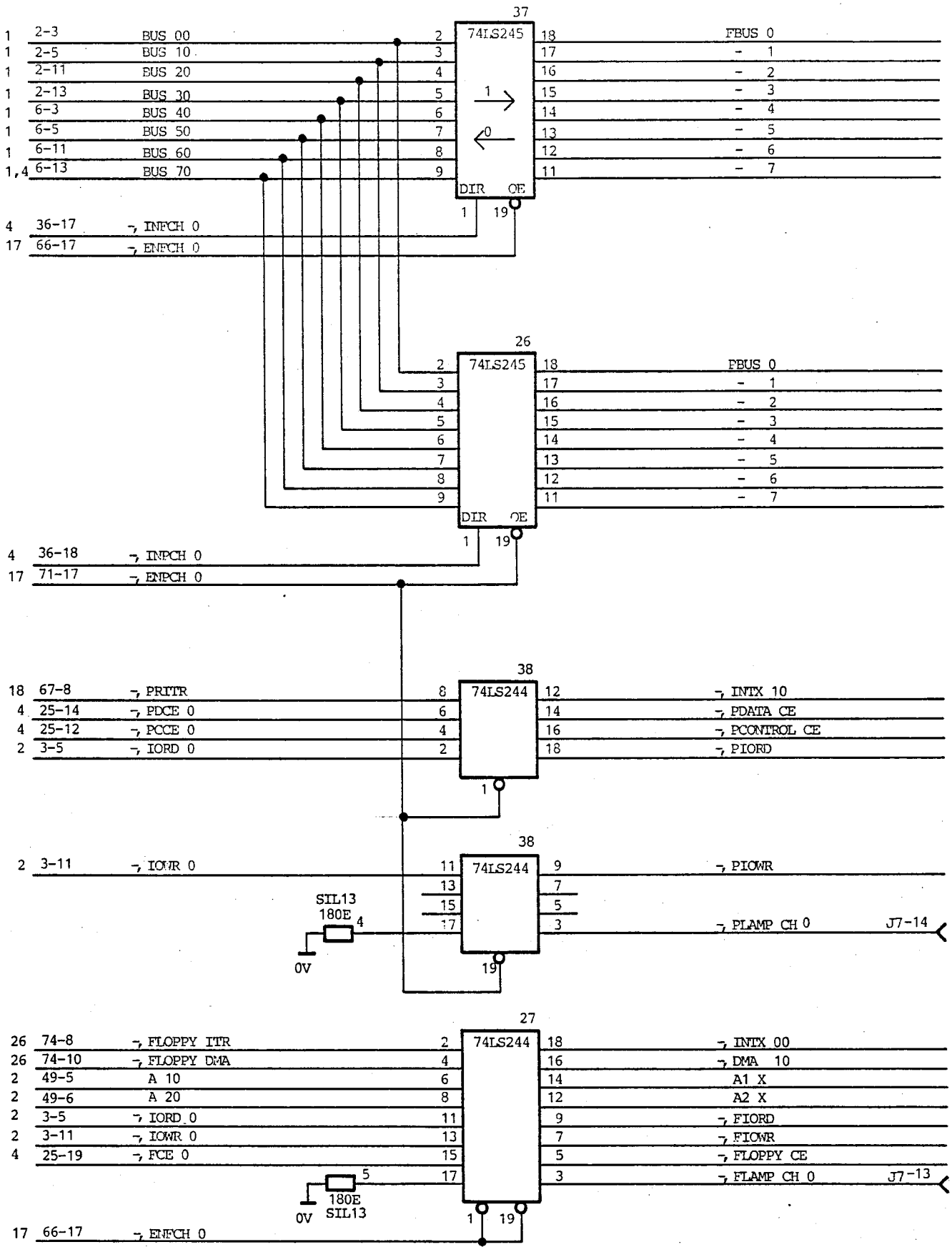
Signal	Destination	Description
A1X-A2X	p.24	Address bit 1 and 2. Enabled by /ENFCH0.
/DMA10	p.2	DMA request from the Floppy interface.
FBUS 0-7	p.22 p.23	Floppy interface BUS 0-7.
/FIORD	p.24	Floppy IORD signal.
/FIOWR	p.24	Floppy IOWR signal.
/Floppy CE	p.23	Floppy Chip Enable. True for I/O devices 280H-286H.
/FLAMP CHO	J7	Floppy LAMP CHannel 0 signal. True when channel 0 (RC759 number A) controls the Floppy Interface.
/INTX00	p.2	Interrupt signal from the Floppy Interface.
PBUS 0-7	p.19 p.20	Printer interface BUS 0-7.
/PDATACE	p.21	Printer DATA Chip Enable (I/O device 28AH).
/P CONTROL CE	p.21	Printer CONTROL Chip Enable (I/O device 28CH).
/PIORD	p.21	Printer IORD signal.
/PIOWR	p.21	Printer IOWR signal.
/P LAMPCHO	J7	Printer LAMP CHannel 0. True when channel 0 (RC759 number A) controls the Printer Interface.



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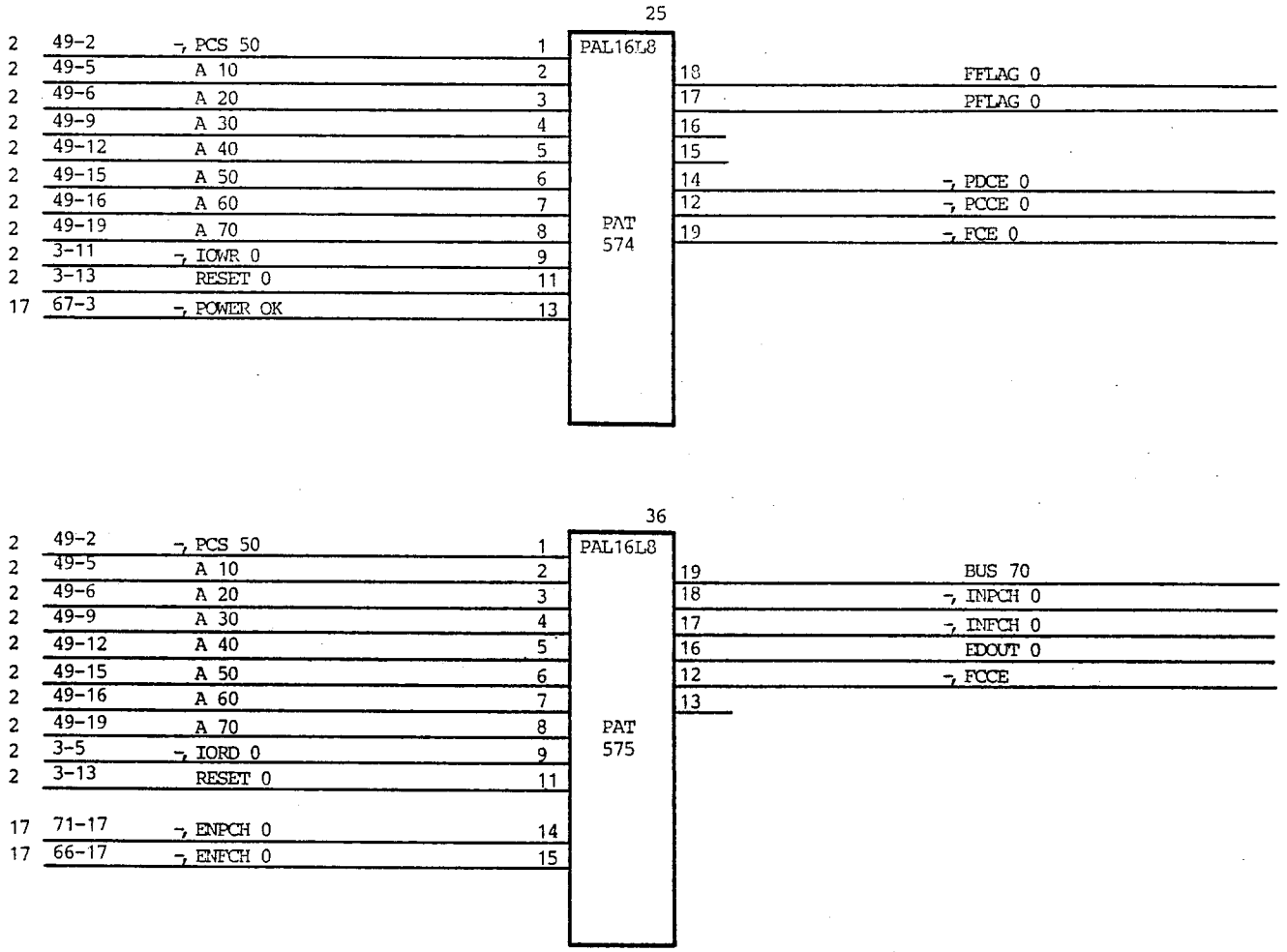
DPC 701
A14656

BUS MULTIPLEXER / CONTROL SIGNAL MULTIPLEXER
CH 0
CIRCUIT DIAGRAM

Signal	Destination	Description
BUS70	p.1 p.2 p.3	BUS bit 7 of the internal bus for interface to RC759 number A. BUS70 is driven by PAT575 during Input from I/O device numbers 28EH and 292 H; indicating acknowledge of Floppy reservation (28EH) and Printer reservation.
EDOUT 0	p.1	Enable Data Out 0. Enable the drivers for the balanced bus to RC759 number A. True when input from I/O devices 280H-286H, 28AH, 28CH, 28EH and 292H.
FFLAG0	p.17 p.2	Floppy FLAG request. Set by Output to device 28EH. Reset by Output to de)c 290H.
/FCE0	p.3	Floppy Chip Enable. True when addressing I/O devices 280-286H (WD 2797-2)
/FCCE	p.23	Floppy Control register Chip Enable. True when addressing I/O device 288H. Enabled by/ENFCH0=0.
/INFCH0	p.3	INput Floppy CHannel 0. True when reading from the Floppy bus FBUS 0-7. Input from I/O devices 280H-286H.
/INPCH0	p.3	INput Printer CHannel 0. True when reading from the Printer bus PBUS 0-7 (I/O devices 28AH and 28CH).
PFLAG0	p.17 p.2	Printer FLAG request. Set by output to 292H. Reset by output to 294H, loc) DPC reset and reset of RC759 number A.
/PDCE0	p.3	Printer Data Channel Enable. True when addressing I/O device 28AH.
/PCCE0	p.3	Printer Control Channel Enable. True when addressing I/O device 28CH.



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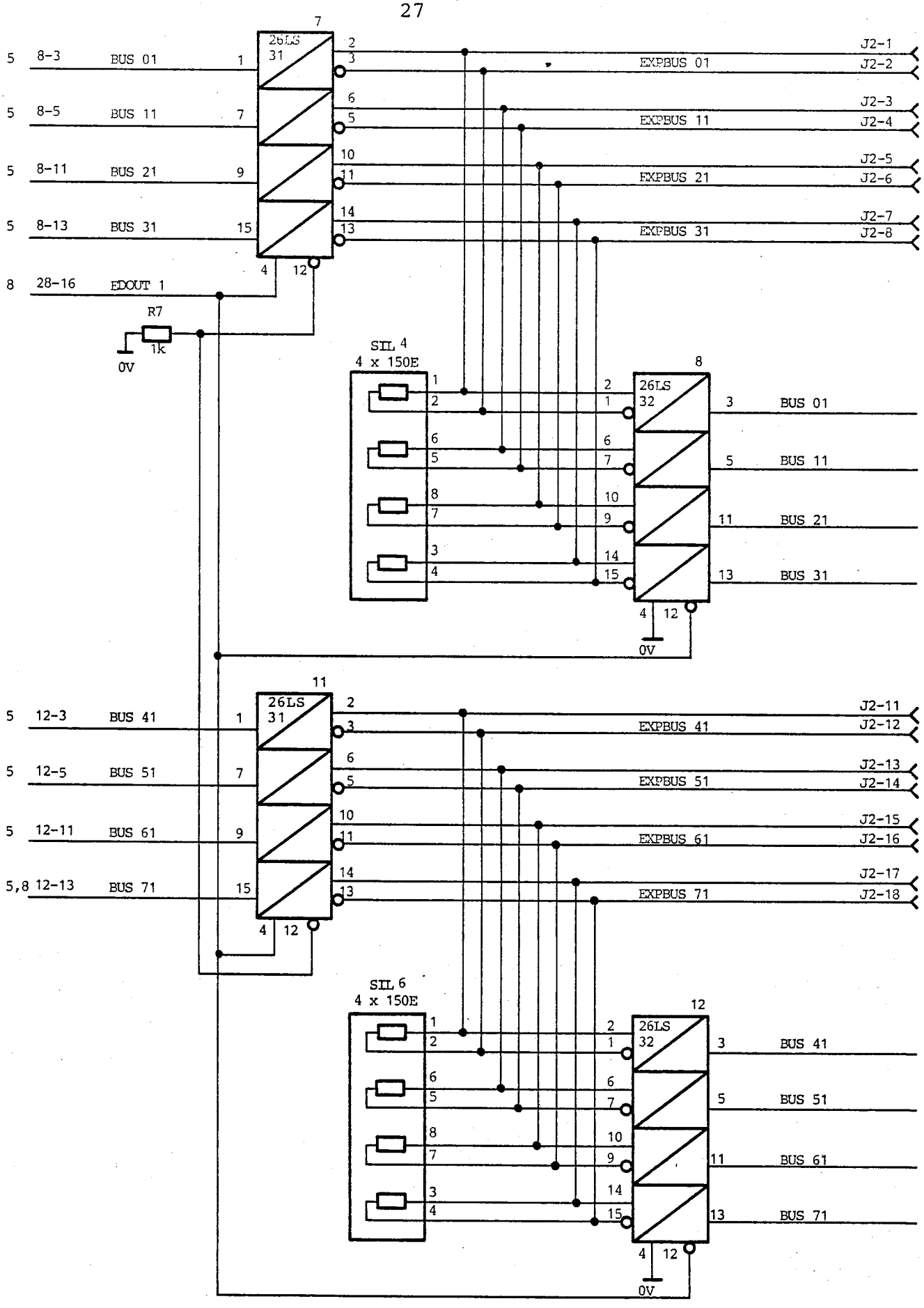
Signal	Destination	Description
BUS01-BUS71	p.6 p.7	Local bus for the interface to RC759 number B.
EXP BUS 01- EXP BUS71	J1	The balanced bus to RC759 number B.



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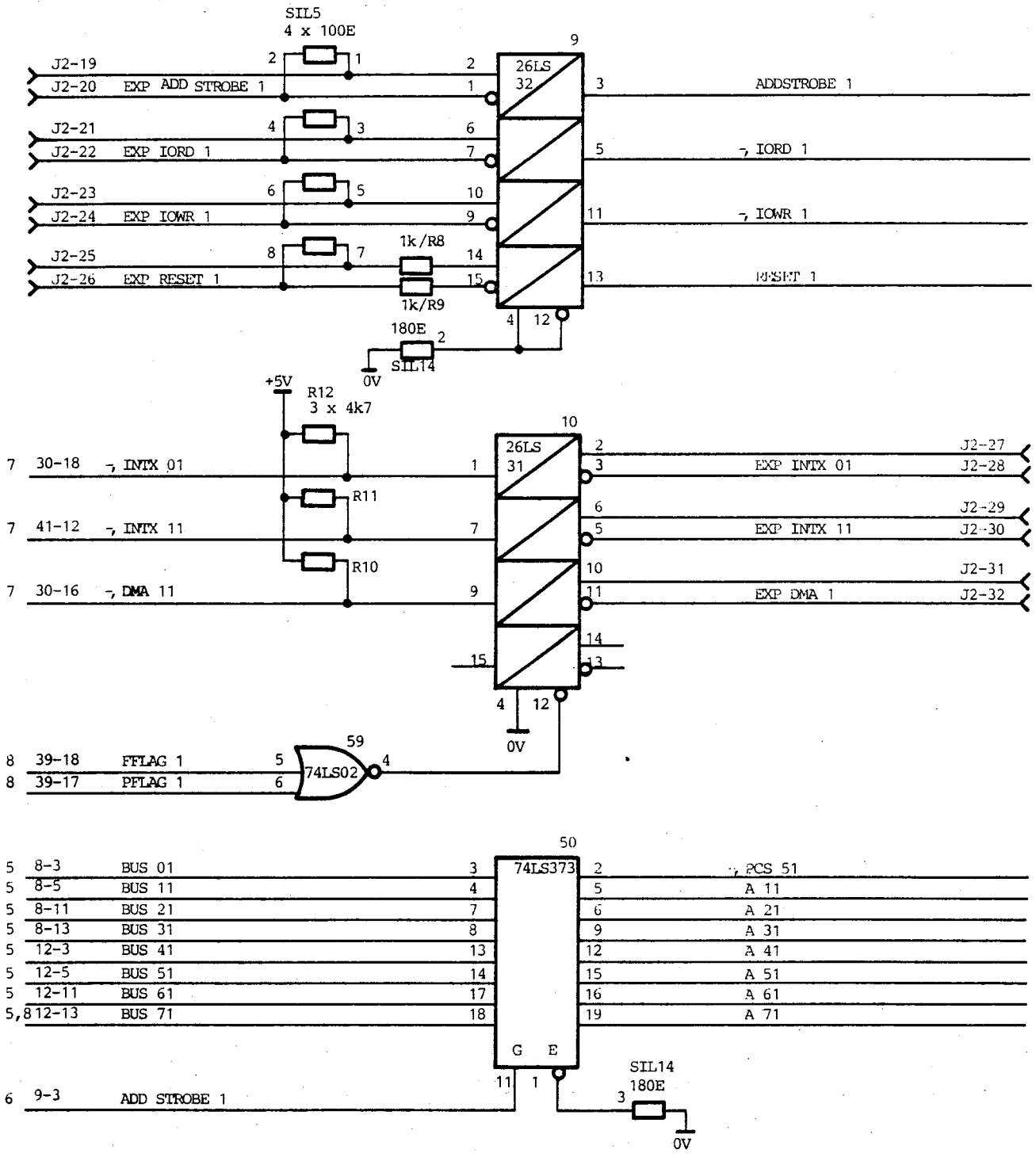
Signal	Destination	Description
ADDSTROBE 1	p.6	ADDress STROBE, Laching the address supplied on BUS 0-7 during the address phase.
A11-A71	p.7 (A10-A20) p.8 (A10-A70)	Address bit 1 to 7.
EXP DMA1	J1	EXPander bus DMA request 1. Used by the Floppy interface.
EXP INTX01, EXP INTX11	J1	EXPander bus INTerrutps. INTX01 equals Floppy interrupts. INTx11 equals Printer interrupts.
/IORD1	p.7 p.8	Input/Output Read Data strobe.
/IOWR1	p.7 p.8	Input/Output WRite Strobe.
/PCS51	p.8	Peripheral Chip Select for I/O devices in the address area 280H - 2FEH.
RESET 1	p.8	RESET from RC759 number B.



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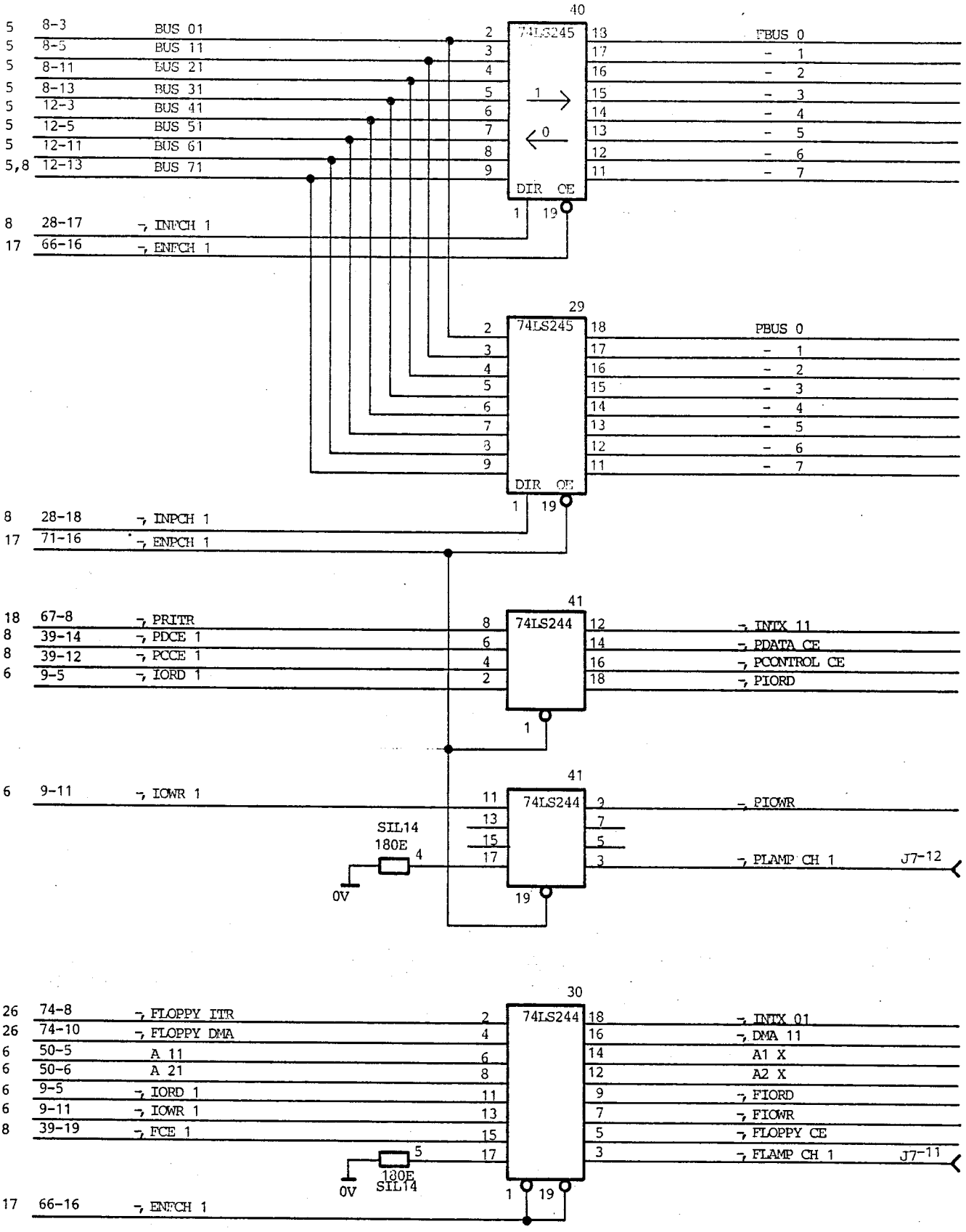
Signal	Destination	Description
A1X-A2X	p.24	Address bit 1 and 2. Enabled by /ENFCH1
/DMA11	p.2	DMA request from the Floppy interface.
FBUS 0-7	p.22 p.23	Floppy interface BUS 0-7.
/FIORD	p.24	Floppy IORD signal.
/FIOWR	p.24	Floppy IOWR signal.
/Floppy CE	p.23	Floppy Chip Enable. True for I/O devices 280H-286H.
/FLAMP CH1	J7	Floppy LAMP CHannel 1 signal. True when channel 1 (RC759 number B) controls the Floppy Interface.
INTX 01	p.2	Interrupt signal from the Floppy Interface.
PBUS 0-7	p.19 p.20	Printer interface BUS 0-7.
/PDATACE	p.21	Printer DATA Chip Enable (I/O device 28AH).
/P CONTROL CE	p.21	Printer CONTROL Chip Enable (I/O device 28CH)
/PIORD	p.21	Printer IORD signal.
/PIOWR	p.21	Printer IOWR signal.
/P LAMPCH 1	J7	Printer LAMP CHannel 1. True when channel 1 (RC759 number B) controls the Printer Interface.



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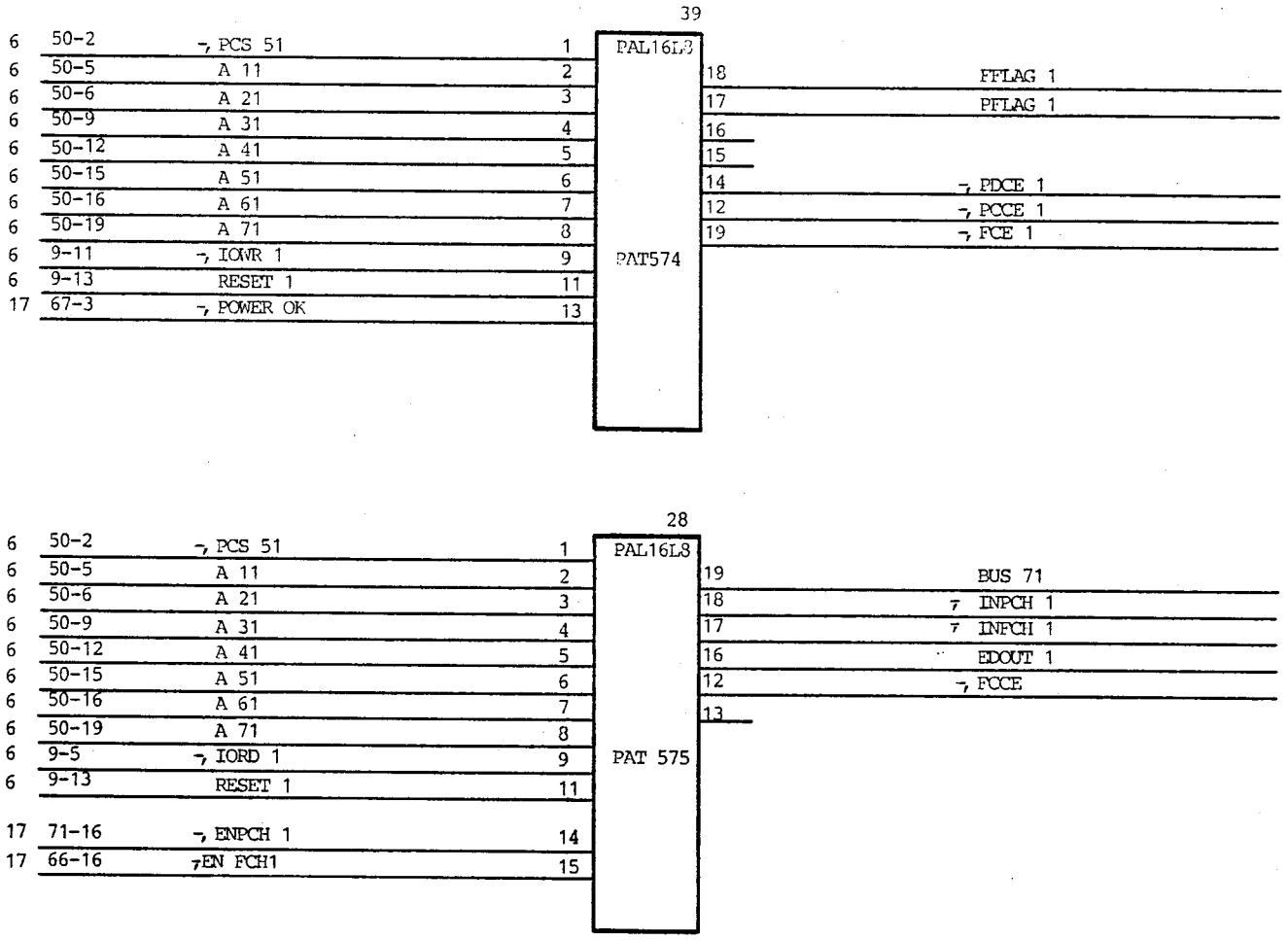
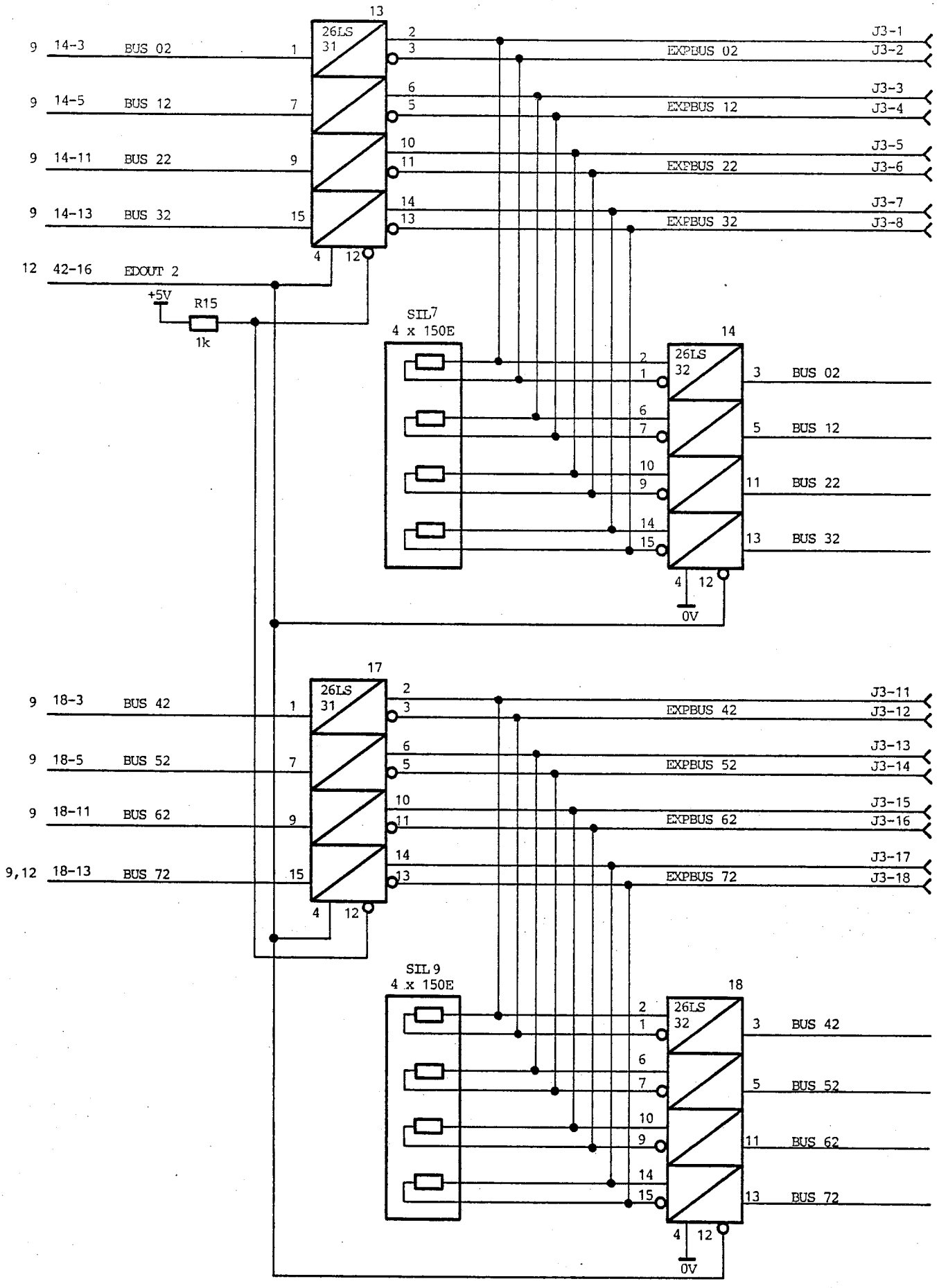
Signal	Destination	Description
BUS 7]	p.5 p.6 p.7	BUS bit 7 of the internal bus for interface to RC759 number B. BUS70 is driven by PAT575 during Input from I/O device numbers 28EH and 292 H; indicating acknowledge of Floppy reservation (28EH) and Printer reservation.
EDOUT]	p.5	Enable Data Out 1. Enable the drivers for the balanced bus to RC759 number B. True when input from I/O devices 280H-286H, 28AH, 28CH, 28EH and 292H.
FFLAG]	p.17 p.6	Floppy FLAG request. Set by Output to device 28EH. Reset by Output to devic 290H, local DPC reset and reset of RC 9 number B.
/FCE]	p.7	Floppy Chip Enable. True when addressing I/O devices 280-286H (WD 2797-2).
/FCCE	p.23	Floppy Control register Chip Enable. True when addressing I/O device 288H. Enabled by/ENFCH1=0.
/INFCH]	p.7	INput Floppy CHannel 1. True when reading from the Floppy bus FBUS 0-7. Input from I/O devices 280 H - 286H.
/INPCH]	p.7	INput Printer CHannel 1. True when reading from the Printer bus PBUS 0-7 (I/O devices 28AH and 28CH).
PFLAG]	p.17 p.6	Printer FLAG request. Set by output to 292H. Reset by output to 294H, local DPC reset and reset of RC759 number B.
/PDCE]	p.7	Printer Data Channel Enable. True when addressing I/O device 28CH.



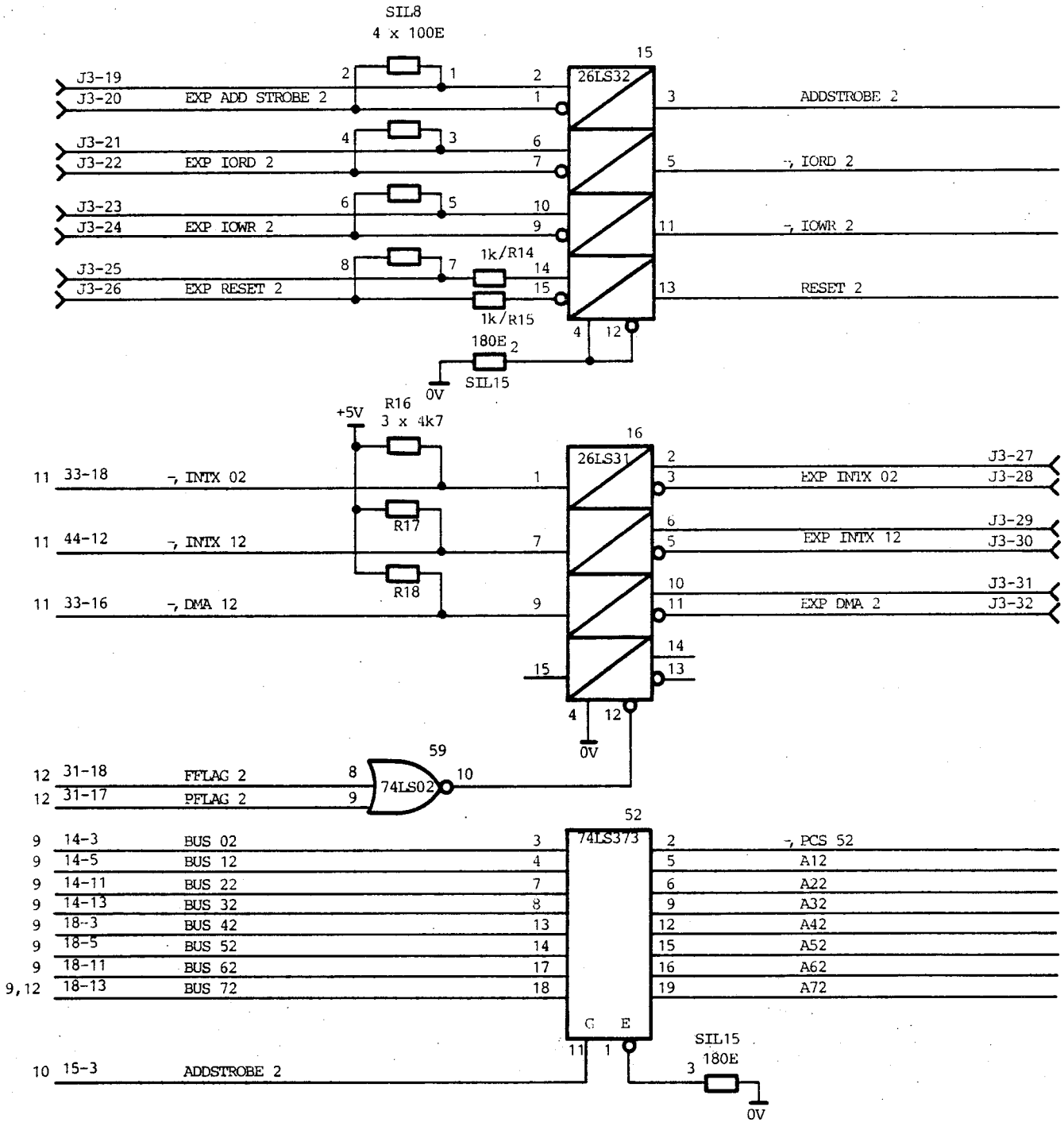
840125/KNEH 840606/AMS

Signal	Destination	Description
BUS 02-BUS 72	p.10 p.11	Local bus for the interface to RC759 number C.
EXP BUS 02- EXP BUS 72	J1	The balanced bus to RC759 number C.



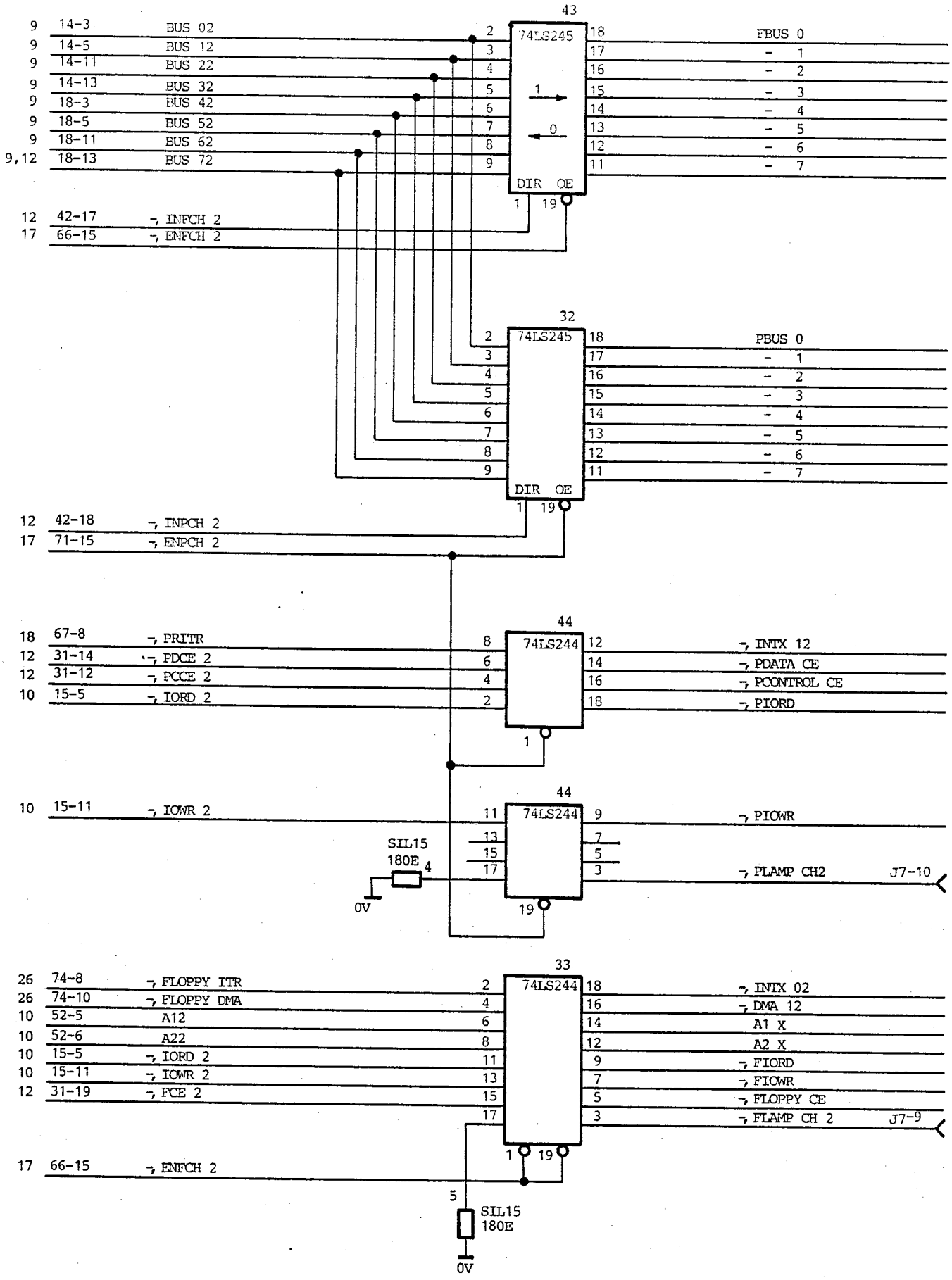
840125/KNEH 840606/AMS

Signal	Destination	Description
ADDSTOBE 2	p.10	ADDress STROBE, Laching the address supplied on BUS0-7 during the address phase.
A12-A72	p.11 (A10-A20) p.12 (A10-A70	Address bit 1 to 7.
EXP DMA 2	J1	EXPander bus DMA request 2. Used by the Floppy interface.
EXP INTX02, EXP INTX12	J1	EXPander bus INTerrupts. INTX02 equals Floppy interrupts. INTX12 equals Printer interrupts.
/IORD2	p.11 p.12	Input/Output Read Data strobe.
/IOWR2	p.11 p.12	Input/Output Write Strobe.
/PCS52	p.12	Peripheral Chip Select for I/O devices in the address area 280H - 2FEH.
RESET 2	p.12	RESET from RC759 number C.



840125/KNEH 840606/AMS

Signal	Destination	Description
A1X-A2X	p.24	Address bit 1 and 2. Enabled by /ENFCH2.
/DMA12	p.10	DMA request from the Floppy interface.
FBUS 0-7	p.22 p.23	Floppy interface Bus 0-7.
/FIORD	p.24	Floppy IORD signal.
/FIOWR	p.24	Floppy IOWR signal.
/Floppy CE	p.23	FLOPPY Chip Enable. True for I/O devices 280H-286H.
/FLAMP CH2	J7	Floppy LAMP CHannel 2 signal. True when channel 2 (RC759 number C) controls the Floppy Interface.
/INTX02	p.10	Interrupt signal from the Floppy Interface.
PBUS 0-7	p.19 p.20	Printer interface BUS 0-7
/PDATA CE	p.21	Printer DATA Chip Enable (I/O device 28AH).
/PCONTROL CE	p.21	Printer CONTROL Chip Enable (I/O device 28CH).
/PIORD	p.21	Printer IORD signal.
/PIOWR	p.21	Printer IOWR signal.
/P LAMPCH2	J7	Printer LAMP CHannel 2. True when channel 2 (RC759 number C) controls the Printer Interface C.



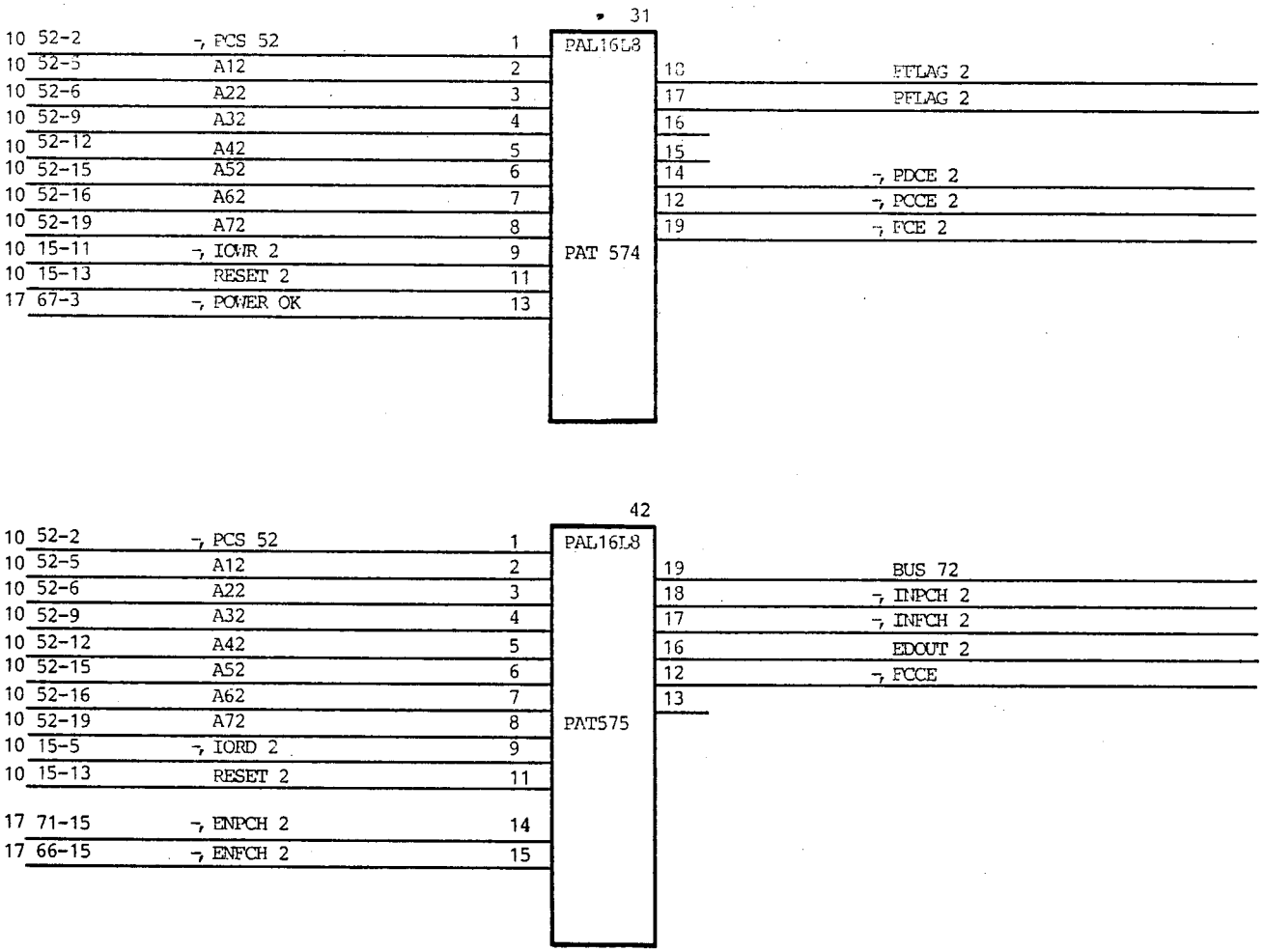
840125/KNEH 840606/AMS

DPC 701

A14664

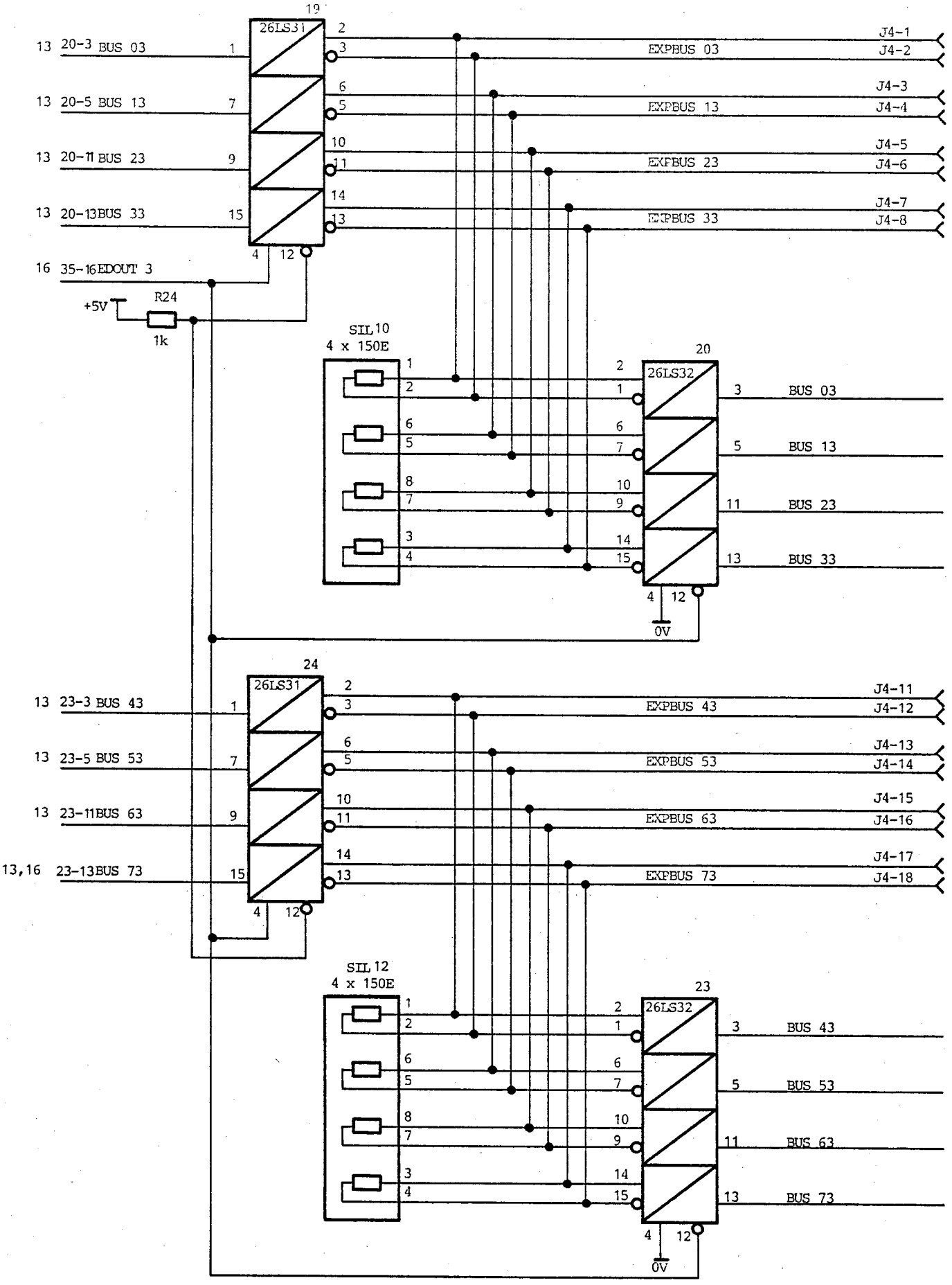
BUS MULTIPLEXER / CONTROL SIGNAL MULTIPLEXER
CHANNEL 2
CIRCUIT DIAGRAM

Signal	Destination	Description
BUS72	p.9 p.10 p.11	BUS bit 7 of the internal bus for interface to RC759 number C. BUS 72 is driven by PAT575 during Input from I/O device numbers 28EH and 292H; indicating acknowledge of Floppy reservation (28EH) and Printer reservation.
EDOUT2	p.9	Enable Data Out 2. Enable the drivers for the balanced bus to RC 759 number C. True when input from I/O devices 280H-286H, 28AH, 28EH and 292H.
FFLAG2	p.17 p.10	Floppy FLAG request. Set by output to device 28EH. Reset by Output to device 290H, local DPC reset and reset of RC759 number C.
/FCE2	p.11	Floppy Chip Enable. True when addressing I/O devices 280-286H (WD 2797-2).
/FCCE	p.23	Floppy Control register Chip Enable. True when addressing I/O device 288H. Enabled by /ENFCH2 = 0.
/INFCH 2	p.11	INput Floppy CHannel 2. True when reading from the Floppy bus FBUS 0-7. Input from I/O devices 280H-286H.
/INPCH2	p.11	INput Printer CHannel 2. True when reading from the Printer bus PBUS 0-7 (I/O devices 28AH and 28CH).
PFLAG2	p.17 p.10	Printer FLAG request. Set by output to 292H. Reset by output to 294H, local DPC reset and reset of RC759 number C.
/PDCE2	p.11	Printer Data Channel Enable. True when addressing I/O device 28AH.
/PCCE2	p.11	Printer Control Channel Enable. True when addressing I/O device 28CH.



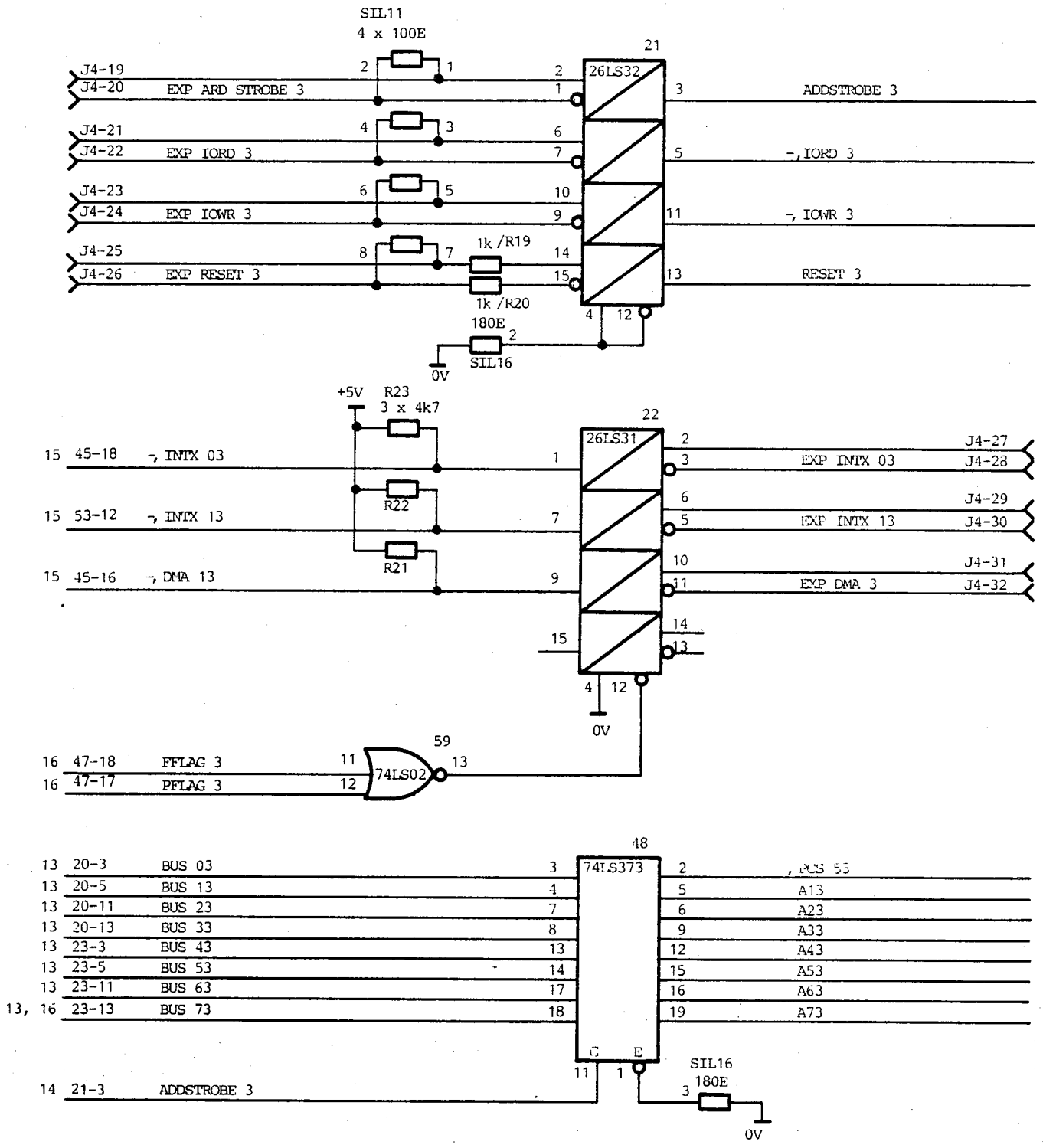
840125/KNEH 840606/AMS

Signal	Destination	Description
BUS03-BUS73	p.14 p.15	Local bus for the interface to RC759 number D.
EXP BUS 03- EXP BUS 73	J1 J1	The balanced bus to RC759 number D.



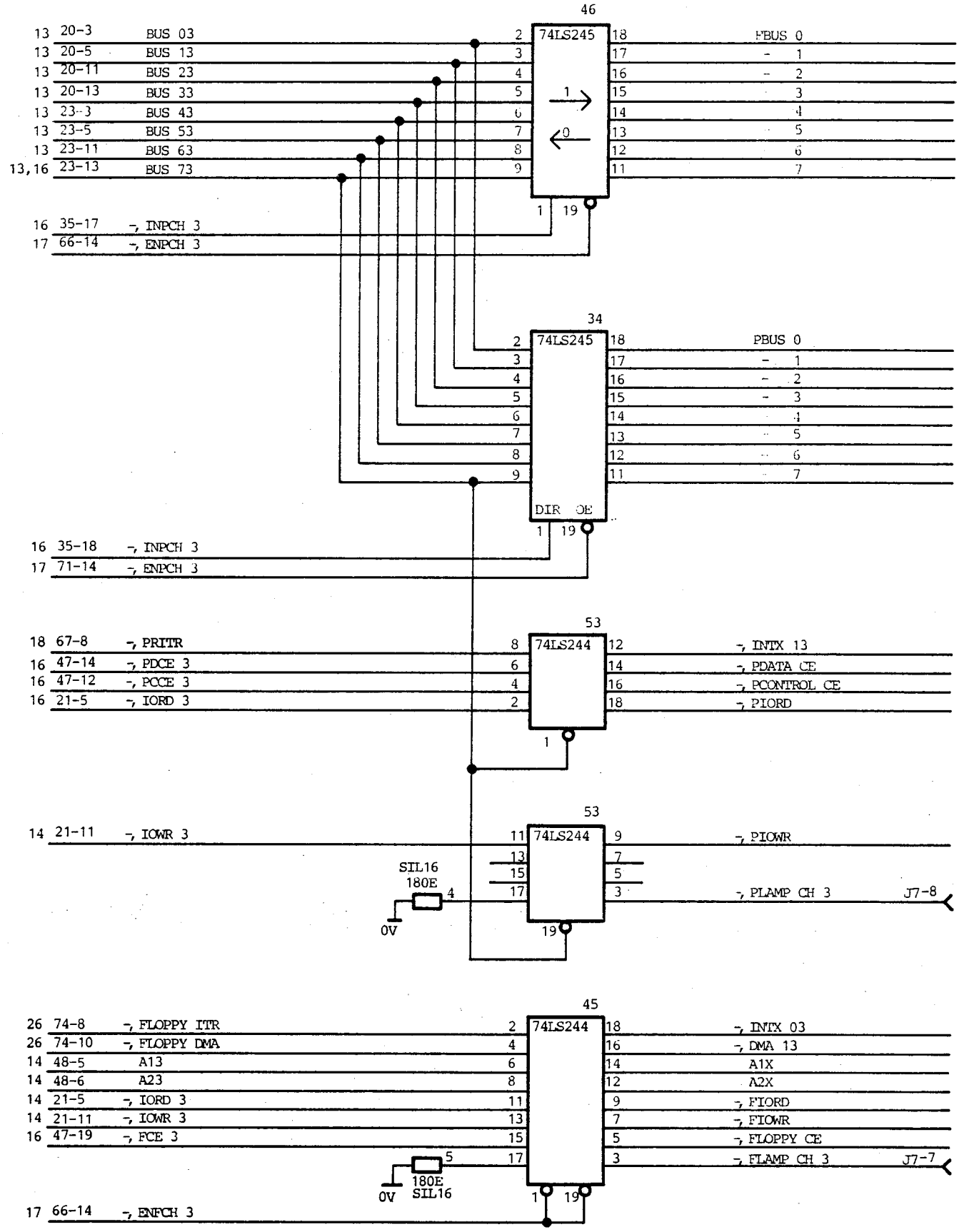
840125/KNEH 840606/AMS

Signal	Destination	Description
ADDSTROBE3	p.16	ADDress STROBE, laching the address supplied on BUS0-7 during the address phase.
A13-A73	p.15 (A10-A20) p.16 (A10-A70)	Address bit 1 to 7.
EXP DMA 3	J1	EXpander bus DMA request 3. Used by the Floppy interface.
EXP INTX03 EXP INTX13	J1	EXPander bus INTerrupts. INTX03 equals Floppy interrupts. INTX13 equals Printer interrupts.
/IORD3	p.15 p.16	Input/Output Read Data strobe.
/IOWR3	p.15 p.16	Input/Output WRite Strobe.
/PCS53	p.16	Peripheral Chip Select for I/O devices in the address area 280H-2FEH.
RESET3	p.16	RESET from RC759 number D.



840125/KNEH 840606/AMS

Signal	Destination	Description
A1X-A2X	p.24	Address bit 1 and 2. Enabled by /ENFCH3.
DMA13	p.14	DMA request from the Floppy interface.
FBUS 0-7	p.22 p.23	Floppy interface BUS0-7.
/FIORD	p.24	Floppy IORD signal.
/FIOWR	p.24	Floppy IOWR signal.
/Floppy CE	p.23	FLOPPY Chip Enable. True for I/O devices 280H-286H.
/FLAMPCH3	J7	Floppy LAMP CHannel 3 signal. True when channel 3 (RC759 number D) controls the Floppy Interface.
/INTX03	p.14	Interrupt signal from the Floppy Interface.
PBUS 0-7	p.19 p.20	Printer interface BUS 0-7.
/PDATA CE	p.21	Printer DATA Chip Enable (I/O device 28AH).
/P CONTROL CE	p.21	Printer CONTROL Chip Enable (I/O device 28CH).
/PIORD	p.21	Printer IORD signal.
/PIOWR	p.21	Printer IOWR signal.
P LAMPCH3	J7	Printer LAMP CHannel 3. True when channel 3 (RC759 numberD)) controls the Printer Interface.



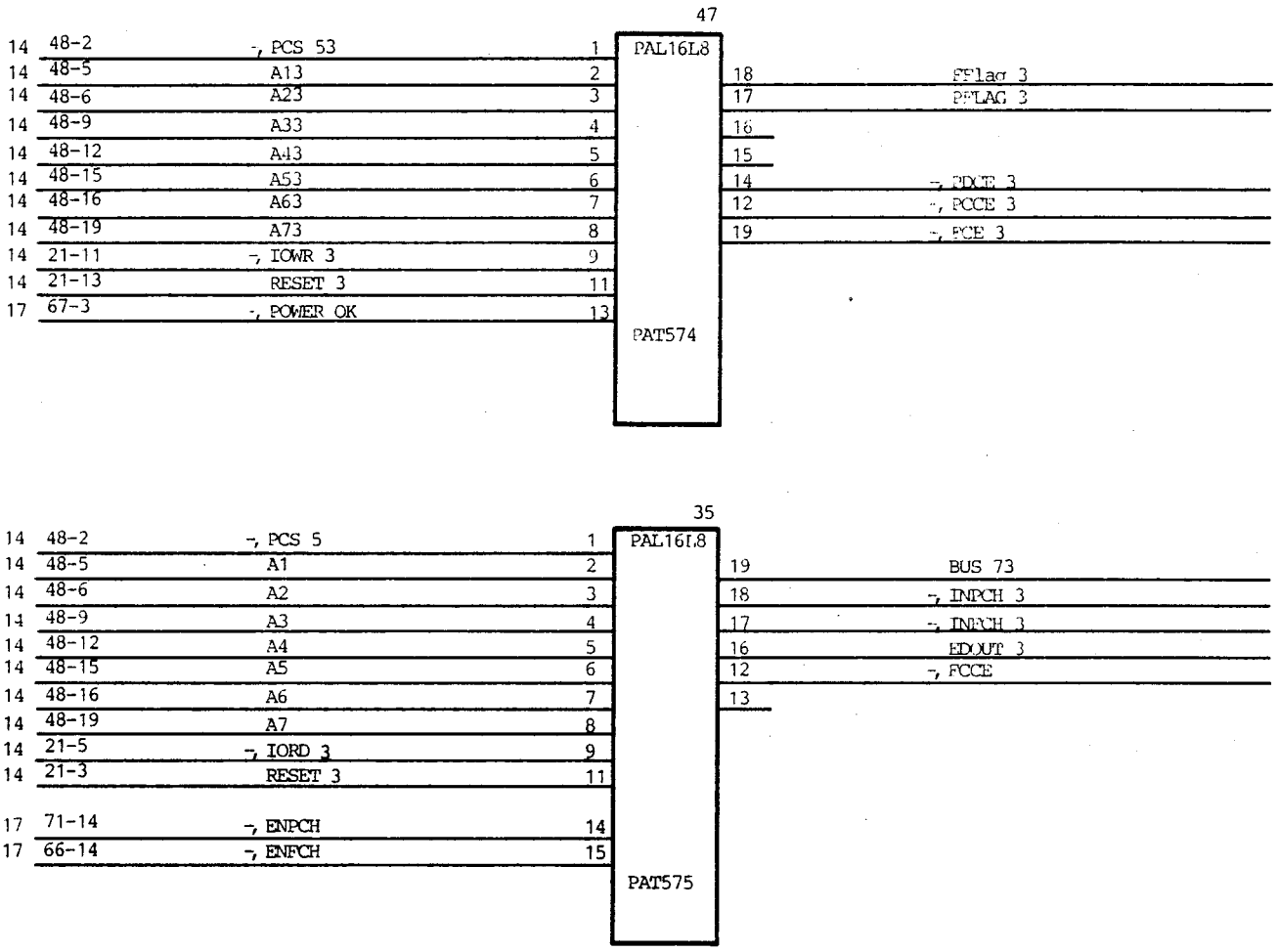
840125/KNEH 840607/AMS

DPC 701

A14668

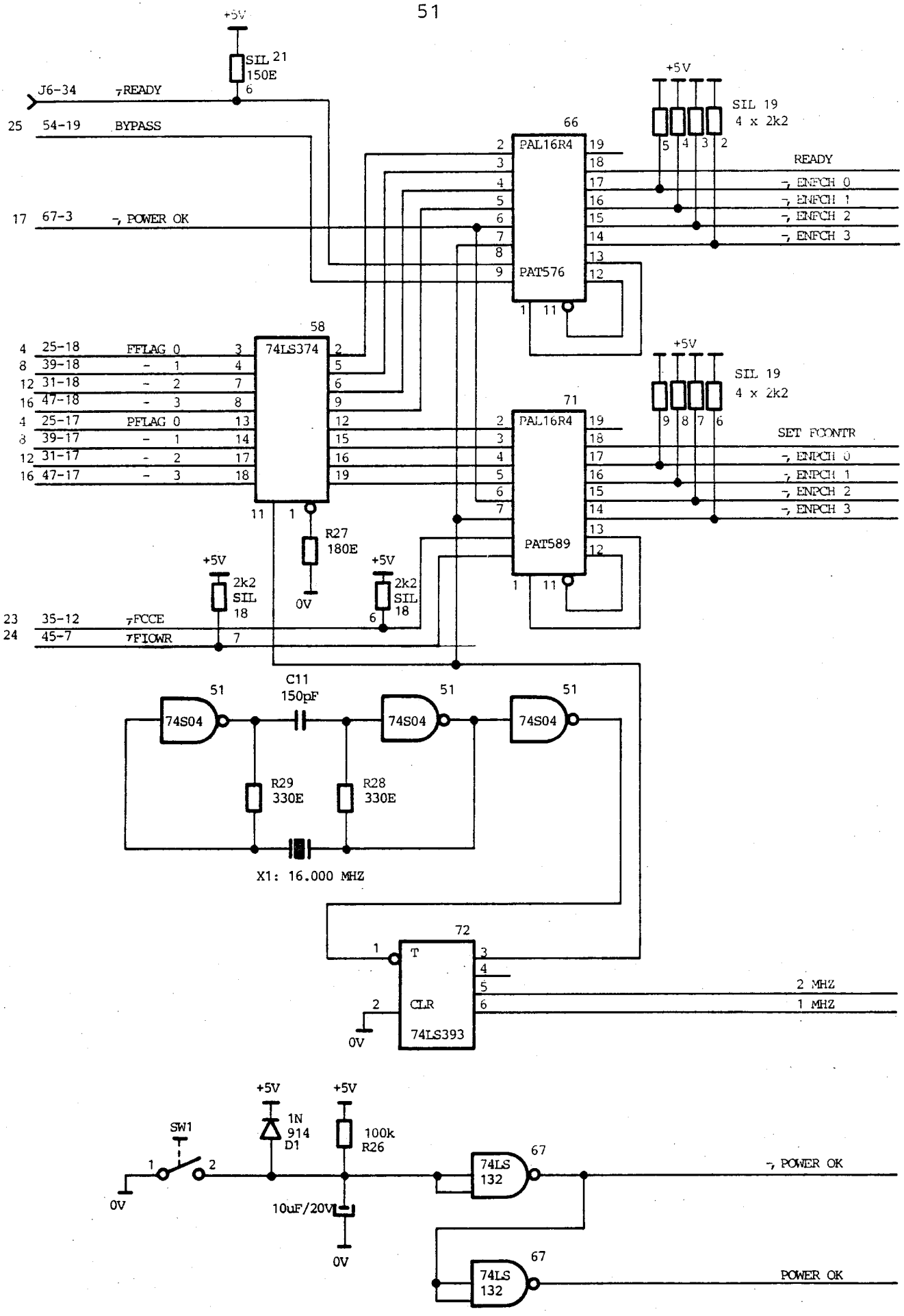
BUS MULTIPLEXER / CONTROL SIGNAL MULTIPLEXER
CHANNEL 3
CIRCUIT DIAGRAM

Signal	Destination	Description
BUS 73	p.13 p.14 p.15	BUS bit 7 of the internal bus for interface to RC759 number D. Bus 73 is driven by PAT575 during Input from I/O device numbers 28EH and 292H; indicating acknowledge of Floppy reservation (28EH) and Printer reservation.
EDOUT3	p.13	Enable Data Out 3. Enable the drivers for the balanced bus to RC759 number D. True when input from I/O devices 280H-286H, 28AH, 28CH and 292H.
FFLAG 3	p.17 p.14	Floppy FLAG request. Set by Output to device 28EH. Reset by Output to device 290H, local DPC reset and reset of RC759 number D.
/FCE3	p.15	Floppy Chip Enable. True When addressing I/O devices 280-286H (WD 2797-2).
/FCCE	p.23	Floppy Control register Chip Enable. True when addressing I/O device 288 E. Enabled by /ENFCH3=0.
/INF CH3	p.15	INput Floppy CHannel 3. True when reading from the Floppy bus FBUS0-7. Input from I/O devices 280H-286H.
/INPCH3	p.15	INput Printer CHannel 3. True when reading from the Printer bus PBUS 0-7 (I/O devices 28AH and 28CH).
PFLAG3	p.17 p.14	Printer FLAG request. Set by output to 292H. Reset by output to 294H, local DPC reset and reset of RC759 . number D.
/PDCE3	p.15	Printer Data Channel Enable. True when addressing I/O device 28AH.
/PCCE3	p.15	Printer Control Channel Enable. True when addressing I/O device 28CH.



840125/KNEH 840607/AMS

Signal	Destination	Description
/ENFCH0	p.3 p.4	ENable Floppy CHannel 0. Output from the arbter indicating that RC759 number A owns the Floppy Interfaces.
/ENFCH1	p.7 p.8	ENable Floppy CHannel 1.
/ENFCH2	p.11 p.12	ENable Floppy CHannel 2.
/ENFCH3	p.15 p.16	ENable Floppy CHannel 3.
/ENPCH0	p.3 p.4	ENable Printer CHannel 0; RC759 number A owns the Printer Interface.
/ENPCH1	p.7 p.8	ENable Printer CHannel 1.
/ENPCH2	p.11 p.12	ENable Printer CHannel 2.
/ENPCH3	p.15 p.16	ENable Printer CHannel 3.
POWER OK	p.25, p.26 p.18	
/POWER OK	p.4 p.8 p.12 p.16 p.17	
READY	p.26	READY signal from the Floppy disc drive.
SET FCONTR	p.25	True when outputting to I/O device 288H.
2MHZ/1MHZ	p.26	Clock signals to the Floppy Controller WD2797. 2MHZ 8"drives and 1 MHZ 51/4



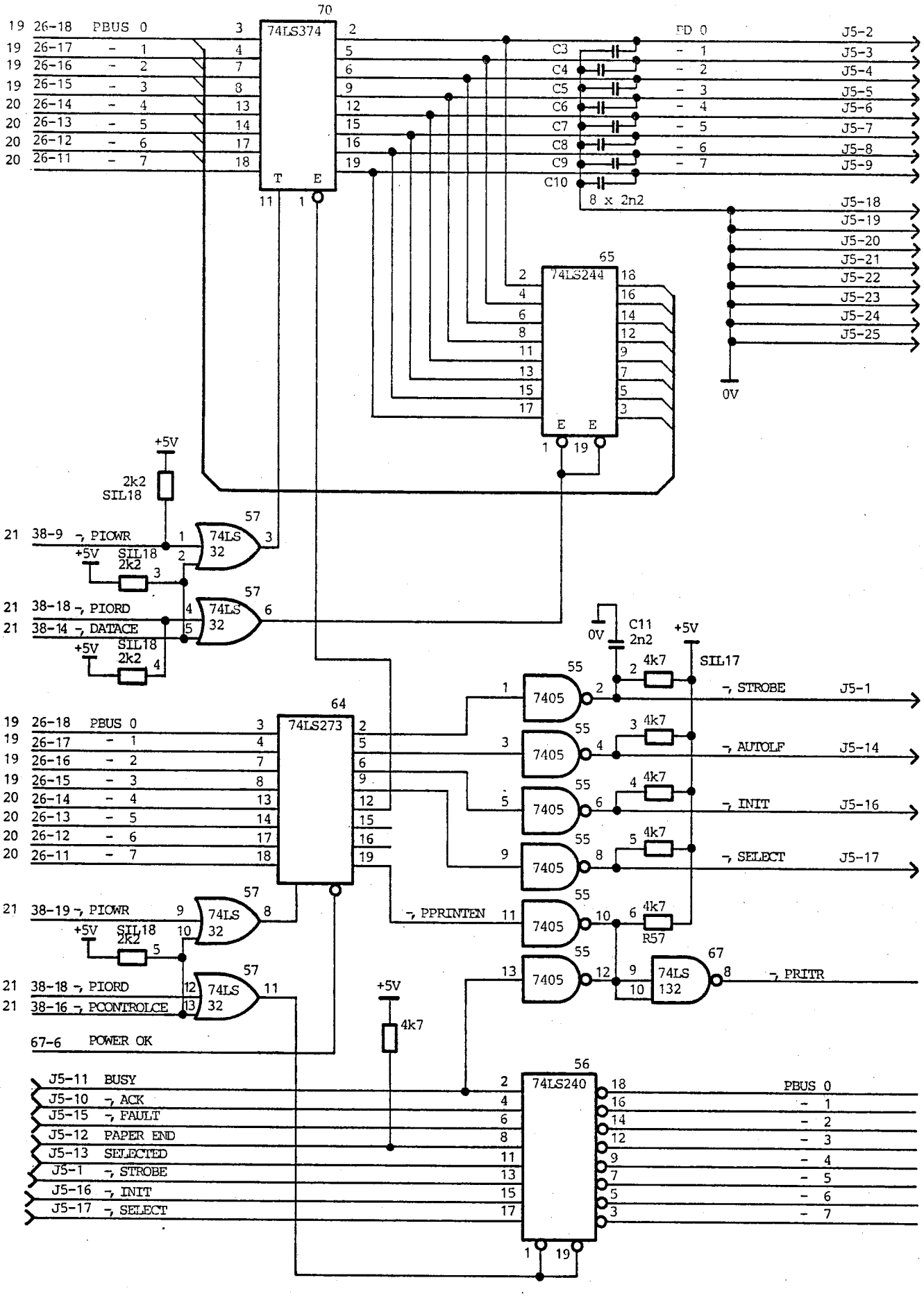
840125/KNEH 840607/AMS

DPC701 FLOPPY REQUEST AND PRINTER REQUEST ARBITERS p. 17

CIRCUIT DIAGRAM

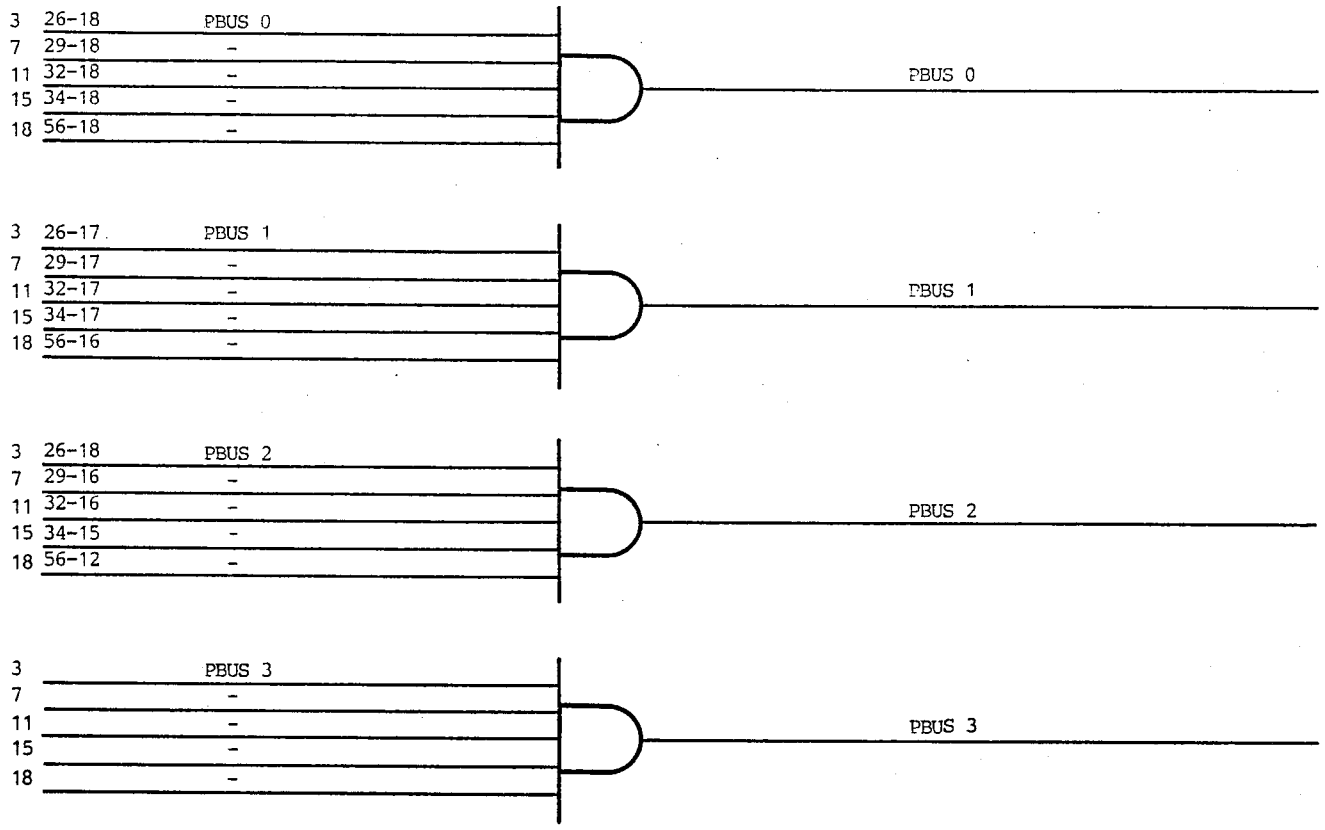
A14670

Signal	Destination	Description
/AUTO LF	J5	AUTO Line Feed control signal.
/INIT	p.18 J5	Reset signal to the printer.
PBUS 0-7	p.19 (PBUS 0-3) p.20 (PBUS 4-7)	internal Printer interface BUS bit 0-7.
PD 0-7	J5	Printer Data bit 0-7.
/PRITR	p.3 p.7 p.11 p.15	Printer InTeRrupt. Generated when the Printer removes BUSY.
/SELECT	p.18 J5	Select signal to the Printer.
/STROBE	p.18 J5.	Data STROBE to the Printer.



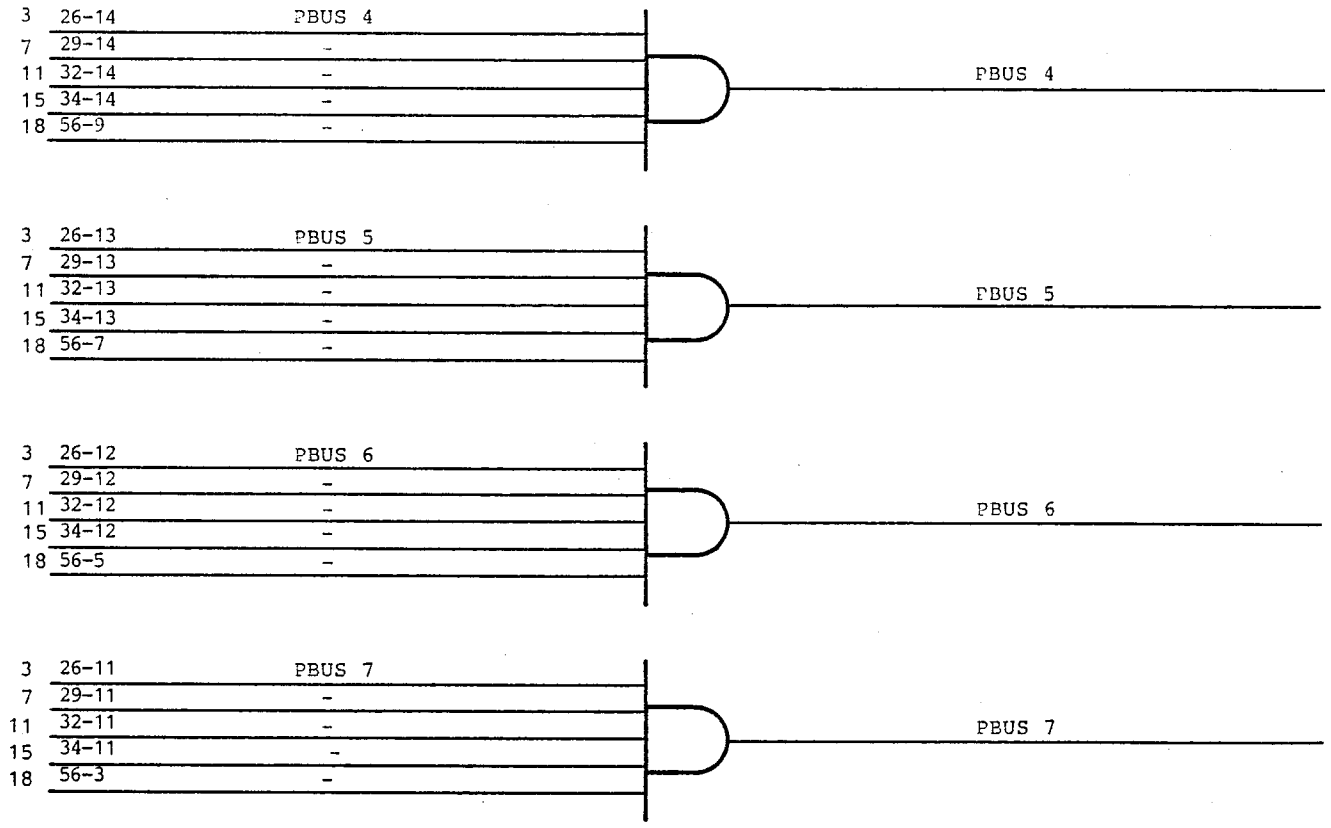
840125/KNEH 840607/AMS

Signal	Destination	Description
PBUS 0-3	p.18	Printer BUS bit 0-3.



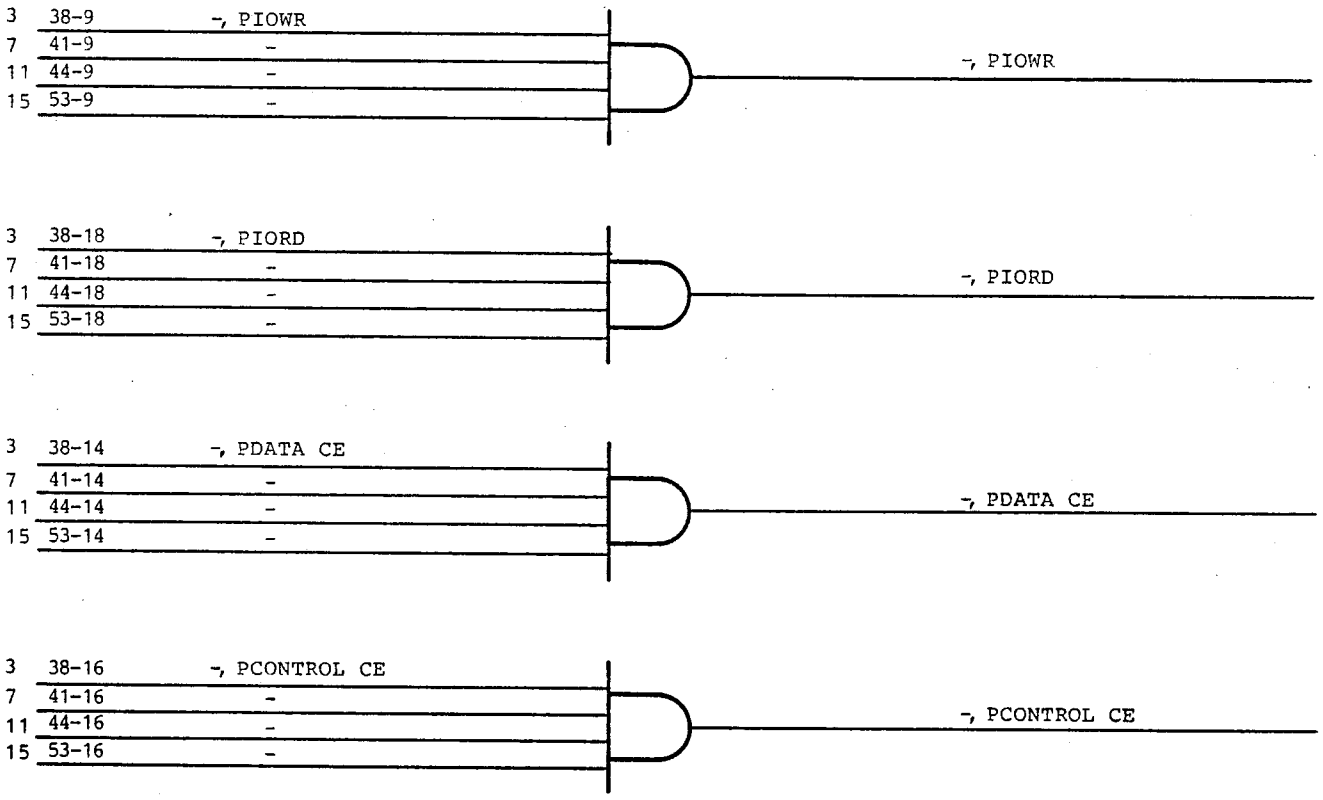
840125/KNEH 840607/AMS

Signal	Destination	Description
PBUS 4-7	p.18	Printer BUS bit 4-7.



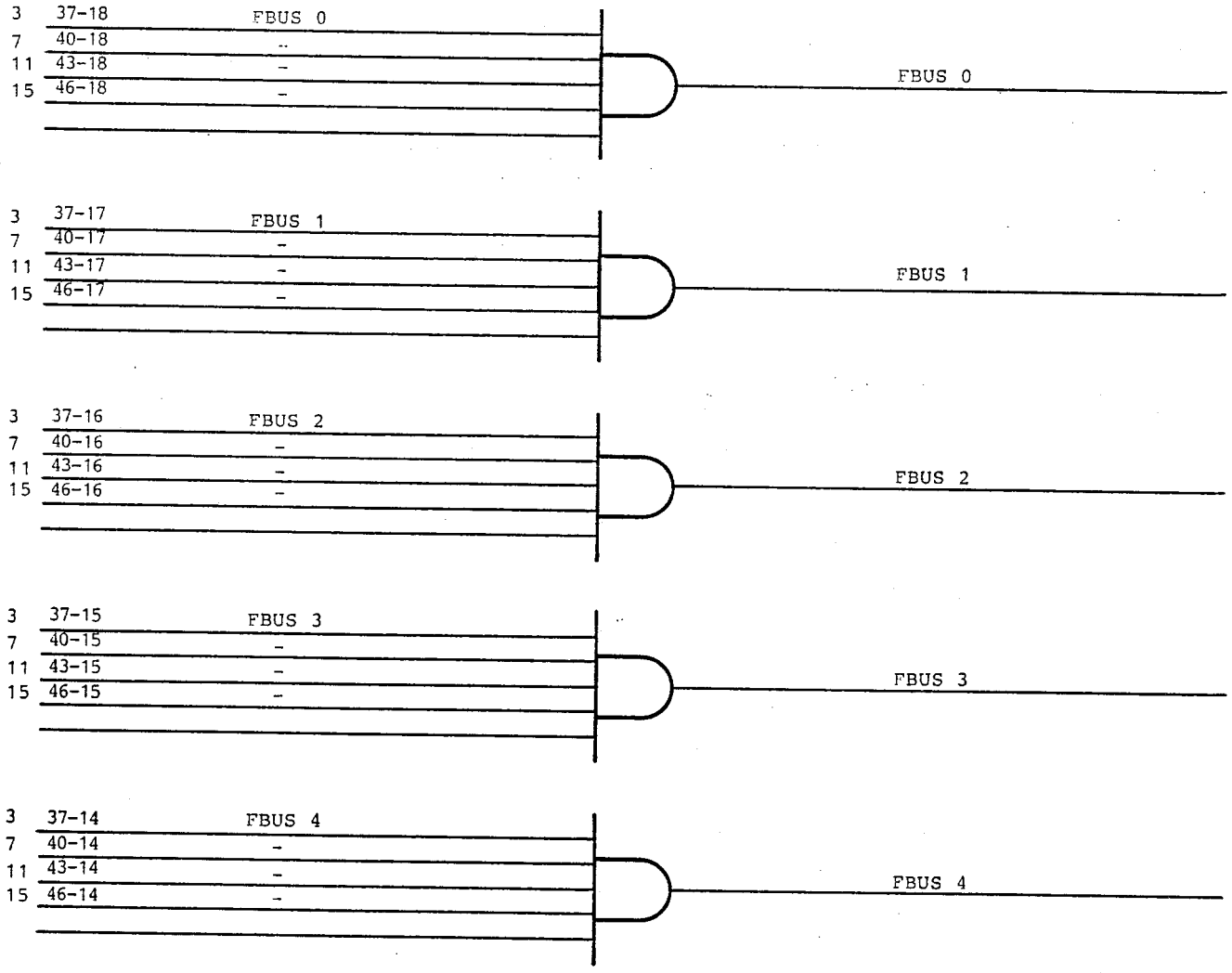
840125/KNEH 840607/AMS

Signal	Destination	Description
/P CONTROL CE	p.18	Printer CONTROL Chip Enable. True when accessing I/O device 28CH.
/PDATACE	p.18	Printer DATA Chip Enable. True when accessing I/O device 28AH.
/PIORD	p.18	Printer IORD signal.
/PIORD	p.18	Printer IOWR signal.



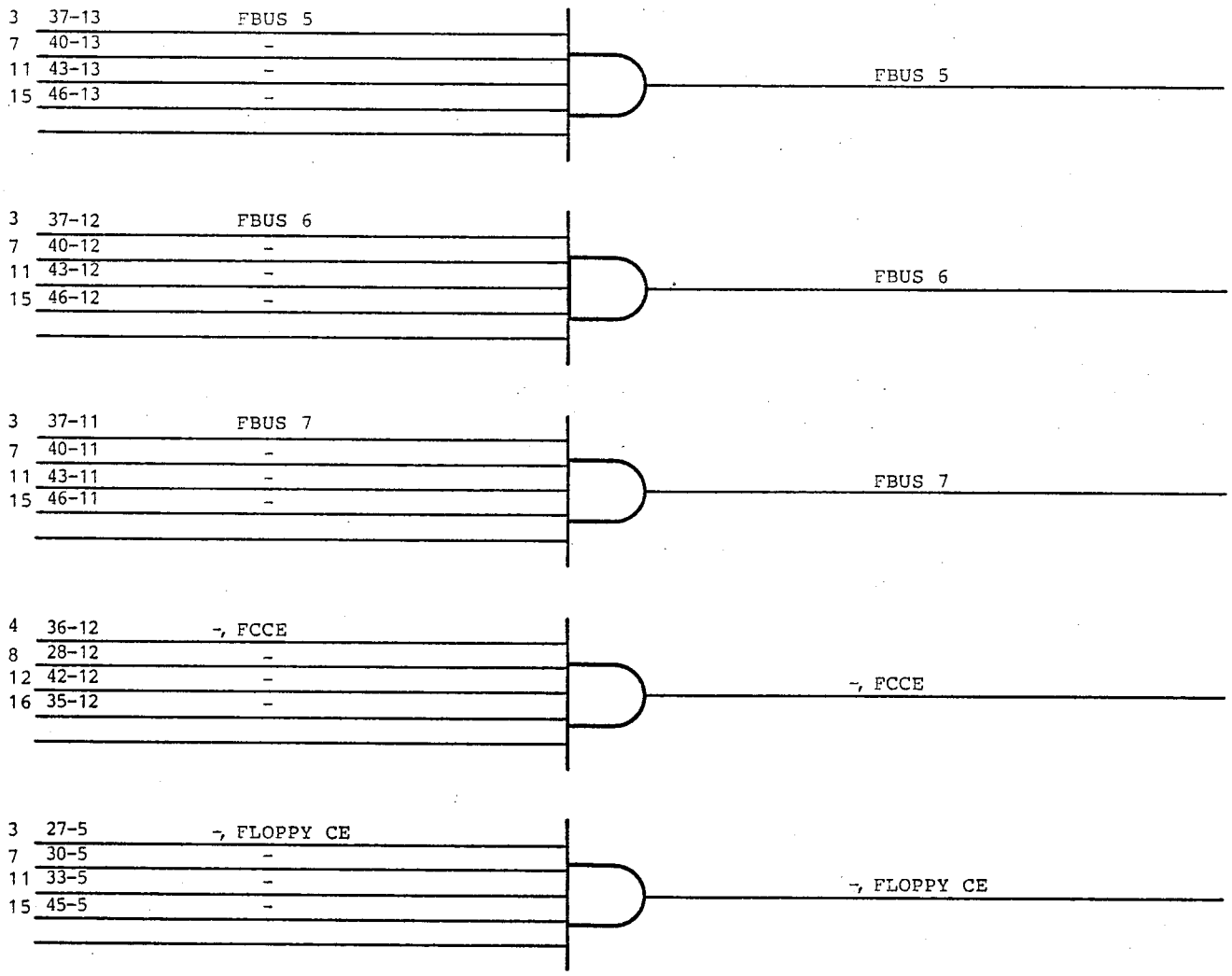
840125/KNEH 840607/AMS

Signal	Destination	Description
PBUS 0-4	p.25 p.26	Floppy interface BUS bit 0-4.



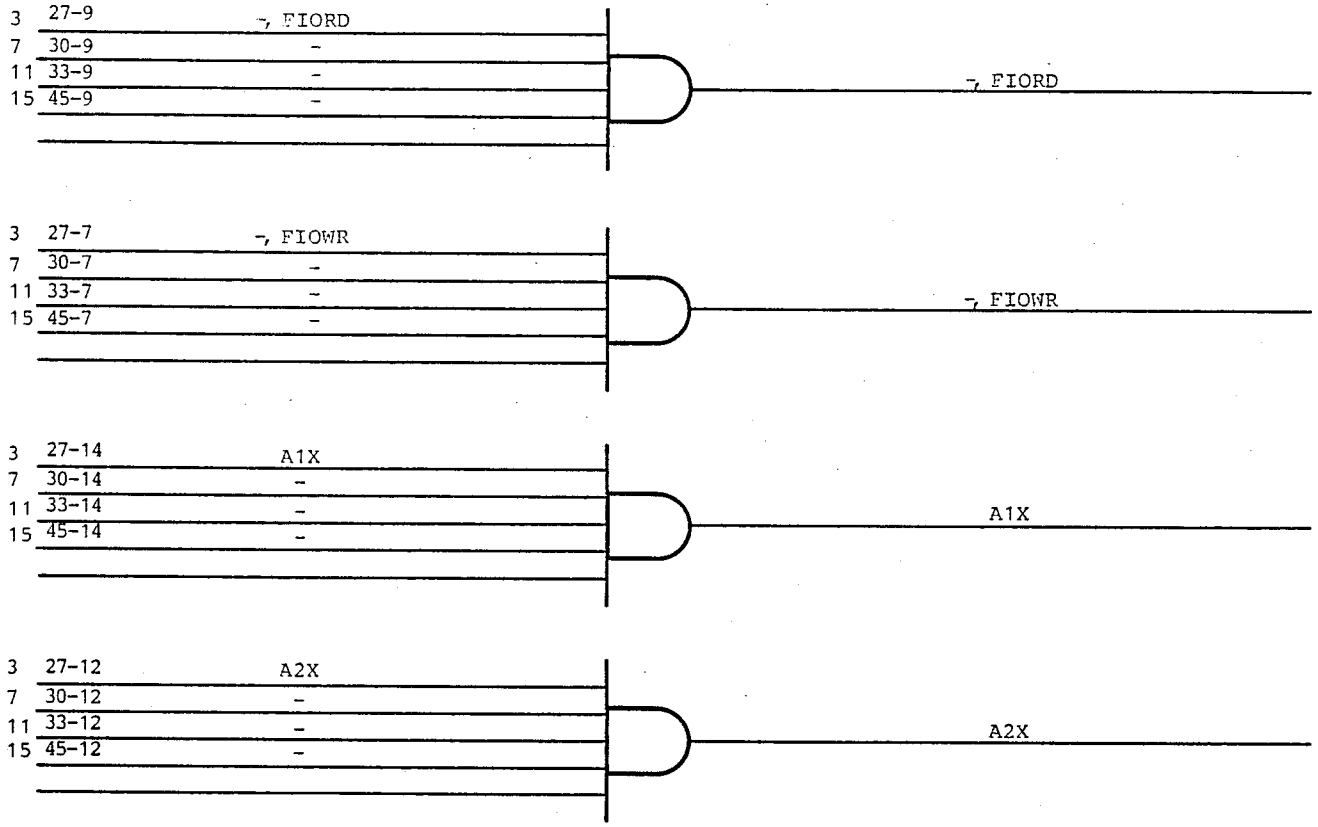
840125/KNEH 840607/AMS

Signal	Destination	Description
FBUS 5-7	p.25 p.26	Floppy interface bit 5-7.
/FCCE	p.17	Floppy Control Chip Enable (i/o device 288H).
/floppy ce	p.26	Floppy controller Chip Enable (I/O devices 280H, 282H, 284H and 286H).



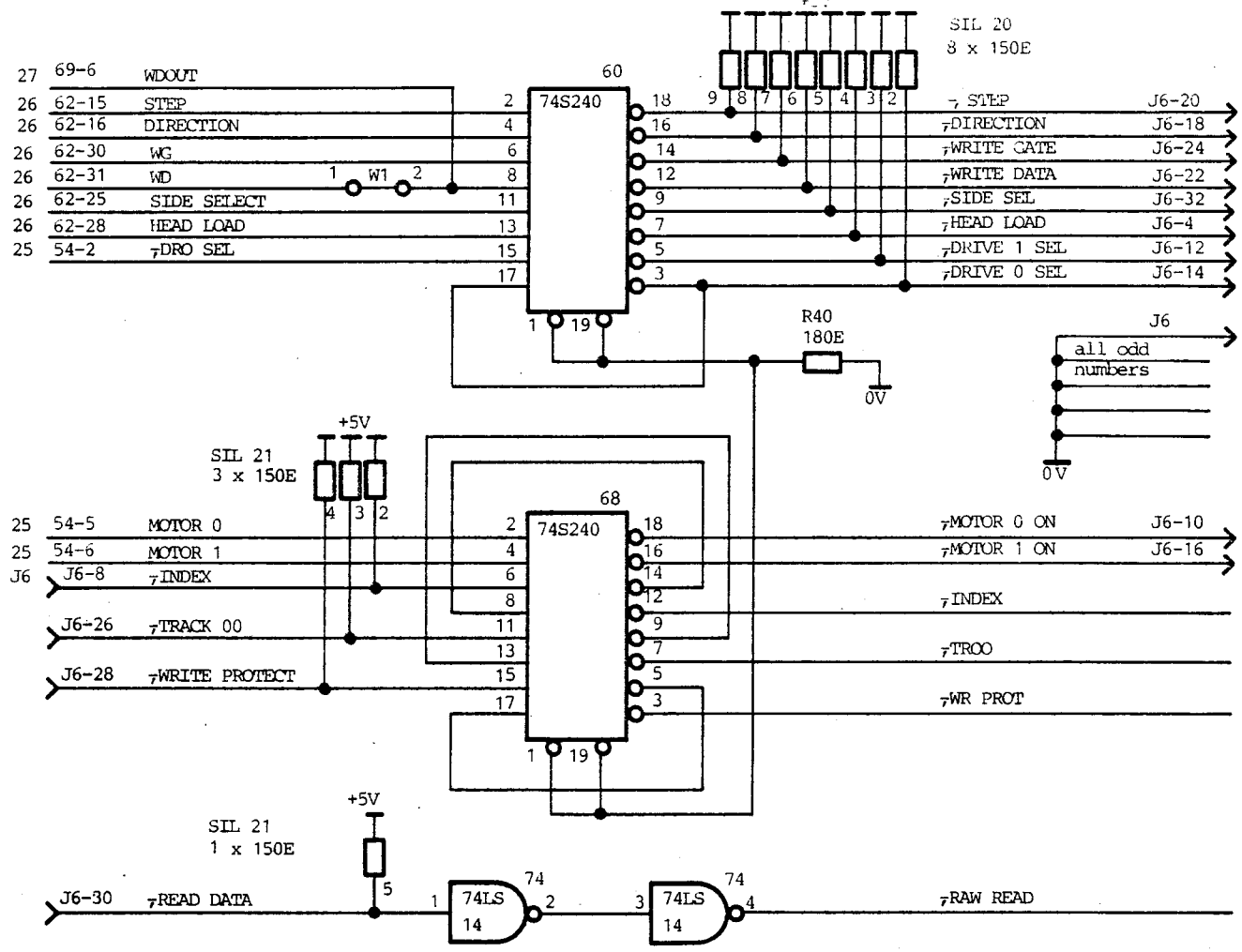
840125/KNEH 840607/AMS

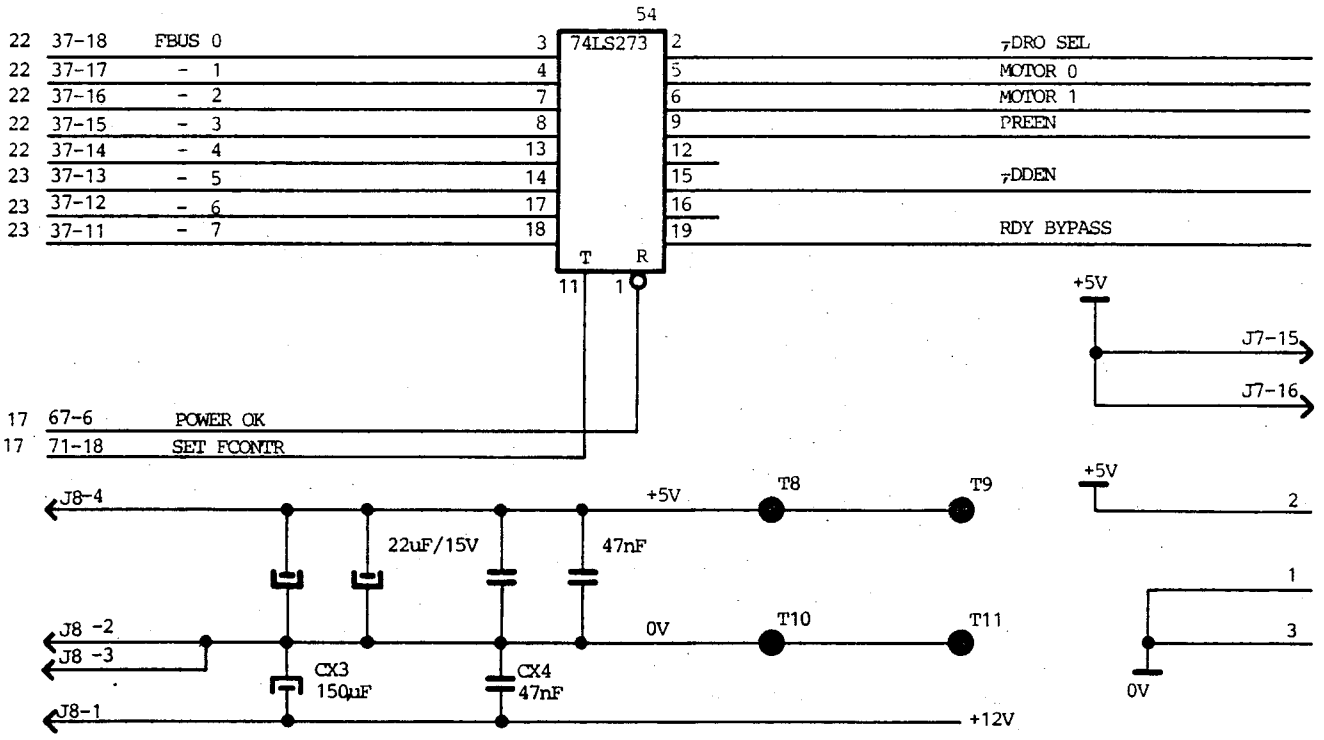
Signal	Destination	Description
A1X - A2X	p.26	I/O address bits 1 and 2.
/FIORD	p.26	Floppy IORD signal.
/FIOWR	p.26 p.17	Floppy IOWR signal.



840125/KNEH 840607/AMS

Signal	Destination	Description
/DDEN	p.27	Dual DENsity
/DIRECTION	J6	Controls the head moving direction. Is true (low) when stepping in.
/DRIVE 0 SEL /DRIVE 1 SEL	J6 J6	DRIVE 0 SELect. DRIVE 1 SELect.
DR 0 SEL	p.25	DRive 0 SELect.
/INDX	p.26	INDeX pulse, when the index hole is encountered on the diskette.
/HEAD LOAD	J6	Loads the Read-Write head against the media.
MOTOR 0	p.25	MOTOR on signal to drive 0.
MOTOR 1	p.25	MOTOR on signal to drive 1.
/MOTOR 0 ON /MOTOR 1 ON	J6 J6	Buffered versions of the signals. above.
PREEN	p.26	PREcompensation ENable.
RDY BYPASS	p.17	ReaDY BYPASS. When true this signal forces the READY input to the Floppy controller (WD2797) to the true state.
/RAW READ	p.26 p.27	The data input signal directly from the drive. This signal has a negative pulse for each recorded flux transition.
/step	j6	step pulse to the head moving control.
/SIDE SEL	J6	/SIDE SELect to the drive to control which side is current in use.
TR00	p.26	Indicates that the Read/Write head is positioned over Track 00.
/WRITE DATA	J6	Output data stream to the Floppy drive.
/WRITE GATE	J6	This signal is valid before writing





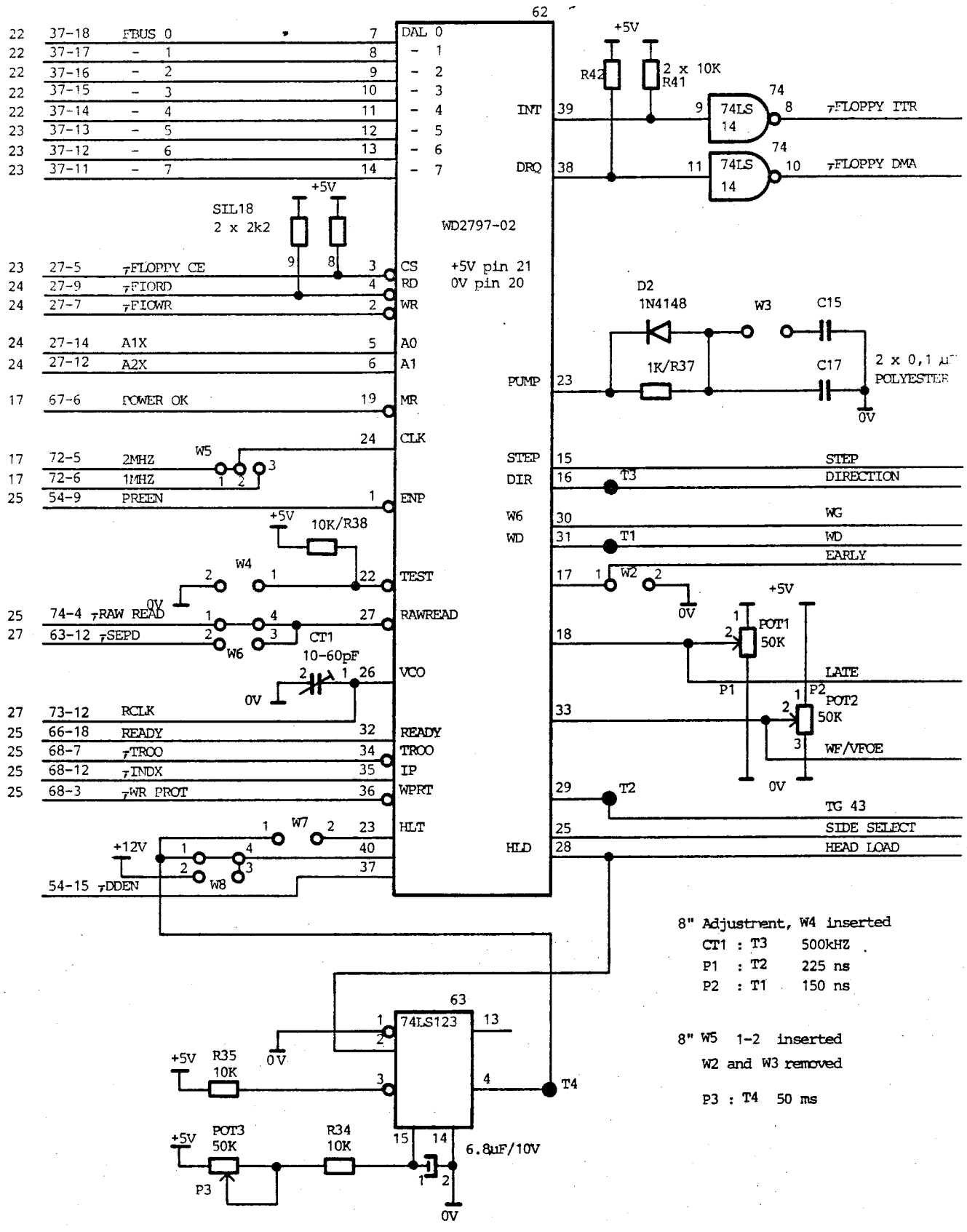
840125/KNEH 840607/AMS

is to be performed on the diskette.

/WR PROT p.26

WRite PROTection signal. This input is sampled whenever a Write Command is

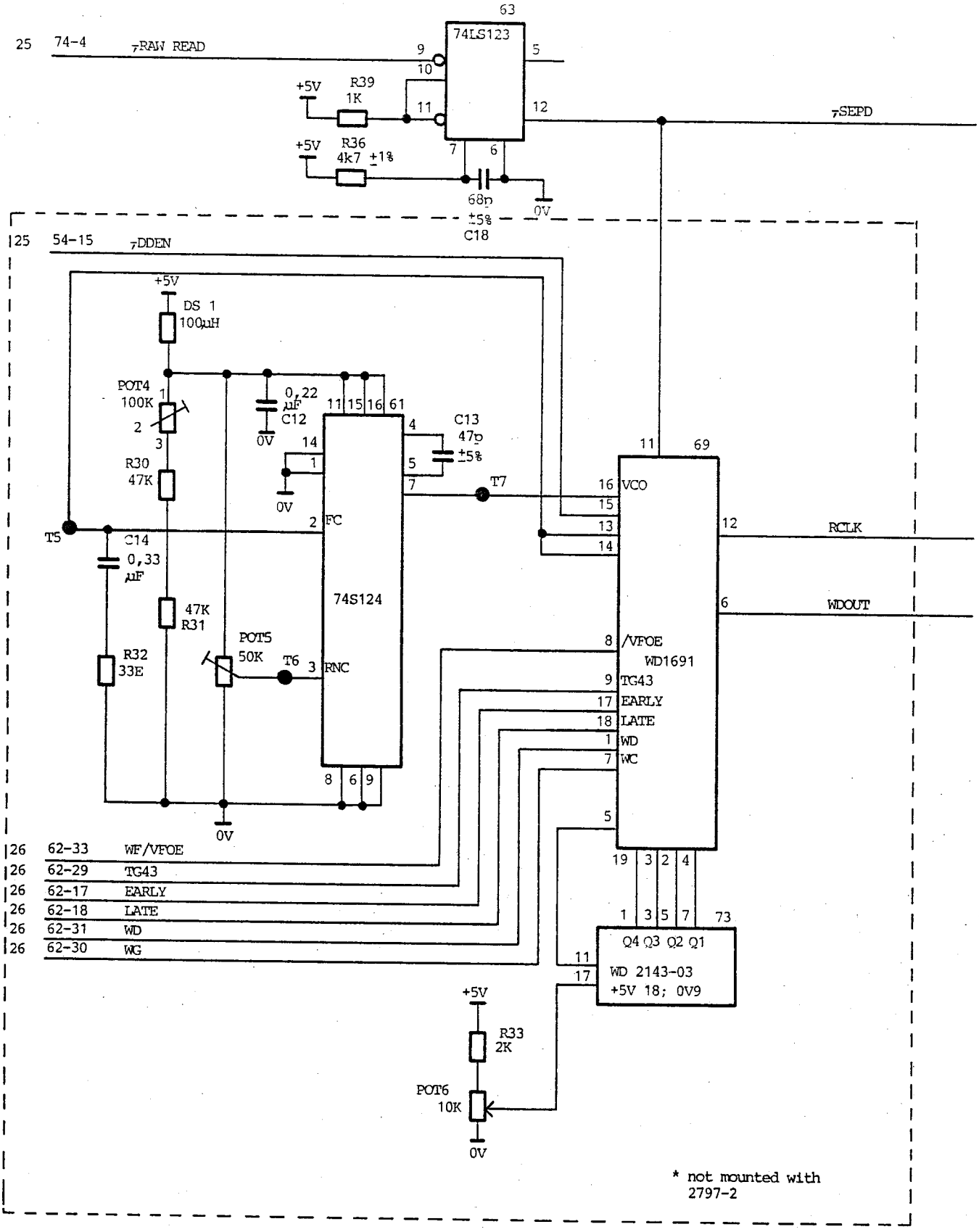
received; A logic low level terminates the command and sets the Write Protect status bit.



840125/KNEH 840607/AMS

Signal	Destination	Description
DIRECTION	p.25	Controls the head moving. Is true (low) when stepping in.
EARLY	p.27	Indicates that the WRITE DATA pulse occuring when Early is active should be shifted early for write precompensation.
/FLOPPY DMA	p.3 p.7 p.11 p.15	FLOPPY DMA request.
/FLOPPY ITR	p.3 p.7 p.11 p.15	FLOPPY InTeRrupt request.
HEAD LOAD	p.25	Loads the Read/Write head against the media.
LATE	p.27	Indicates that the WRITE DATA pulse occuring while LATE is active should be shifted late for write precompensation.
SIDE SELECT	p.25	SIDE SELECT control signal to the drive.
STEP	p.25	STEP pulses to head moving control circuit.
TG43	p.27	This output informs that the Read/Write head is positioned between tracks 44-76.
W6	p.25 p.27	Write Gate.
WD	p.25 p.27	Write Data.
WF/VFOE	p.27	Write Fault/VFO Enable. This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data seperator.

Signal	Destination	Description
/SEPD	p.26	SEParate input Data.
WDOUT	p.25	Write Data OUTput.



840125/KNEH 840607/AMS

6. PAL circuits

This section contains the logical structure of the following PAL-circuits:

```
PAL16L8                    PAL DESIGN SPECIFICATION
PAT574                     1984.02.05,KNEH.
I/O DECODER AND FLAG FLIP-FLOP'S TO DPC701

/PCS5 A1 A2 A3 A4 A5 A6 A7 /IOWR GND
RESET /PCCE /POK /PDCE 15 16 PFLAG FFLAG /FCE VCC

IF (VCC) /FFLAG = RESET+/POK+16
                  +PCS5*A7*/A6*/A5*A4*/A3*/A2*/A1*IOWR
IF (VCC)    /16 = FFLAG
                  +PCS5*A7*/A6*/A5*/A4*A3*A2*A1*IOWR
IF (VCC) /PFLAG = RESET+/POK+15
                  +PCS5*A7*/A6*/A5*A4*/A3*A2*/A1*IOWR
IF (VCC)    /15 = PFLAG
                  +PCS5*A7*/A6*/A5*A4*/A3*/A2*A1*IOWR
IF (VCC)   PDCE = PCS5*A7*/A6*/A5*/A4*A3*/A2*A1*/RESET*POK
IF (VCC)   PCCE = PCS5*A7*/A6*/A5*/A4*A3*A2*/A1*/RESET*POK
IF (VCC)    FCE = PCS5*A7*/A6*/A5*/A4*/A3*/A2*A1*/RESET*POK
                  +PCS5*A7*/A6*/A5*/A4*/A3*A2*/A1*/RESET*POK
                  +PCS5*A7*/A6*/A5*/A4*/A3*A2*A1*/RESET*POK
                  +PCS5*A7*/A6*/A5*/A4*/A3*/A2*/A1*/RESET*POK

DESCRIPTION:

I/O DEVICE NUMBER !   FUNCTION
------------------------------------------------------------------
IOBASE + 280 (HEX)! ADDRESS TO THE FLOPPY DISK CONTROLLER
IOBASE + 282      !       - DO -
IOBASE + 284      !       - DO -
IOBASE + 286      !       - DO -
IOBASE + 28A      ! PRINTER DATA
IOBASE + 28C      ! PRINTER CONTROL
IOBASE + 28E      ! RESERVE FLOPPY(SET FFLAG)
IOBASE + 290      ! RELEASE FLOPPY(RESET FFLAG)
IOBASE + 292      ! RESERVE PRINTER(SET PFLAG)
IOBASE + 294      ! RELEASE PRINTER(RESET PFLAG)
------------------------------------------------------------------

THE FLAGS (PFLAG AND FFLAG) ARE TOO RESET BY "RESET" AND "POK".
```

Fig. 11. PAT574

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PAL16L8                         PAL DESIGN SPECIFICATION
PAT575                          1984.02.06;KNEH
I/O DECODER TO DPC701.

/PCS5 A1 A2 A3 A4 A5 A6 A7 /IORD GND
RESET /FCCE 13 /ENPCH /ENFCH EDOUT /INFCH /INPCH BUS7 VCC

IF (VCC)  INPCH = /RESET*PCS5*/A6*/A5*/A4*A3*/A2*A1*IORD
                  +/RESET*PCS5*/A6*/A5*/A4*A3*A2*/A1*IORD
IF (VCC)  INFCH = /RESET*PCS5*/A6*/A5*/A4*/A3*/A2*/A1*IORD
                  +/RESET*PCS5*/A6*/A5*/A4*/A3*/A2*A1*IORD
                  +/RESET*PCS5*/A6*/A5*/A4*/A3*A2*/A1*IORD
                  +/RESET*PCS5*/A6*/A5*/A4*/A3*A2*A1*IORD
IF (VCC)    /13 = /RESET*PCS5*/A6*/A5*/A4*A3*A2*A1*IORD
                  +/RESET*PCS5*/A6*/A5*A4*/A3*/A2*A1*IORD
IF (VCC) /EDOUT = /INPCH*/INFCH*13
IF (ENFCH) FCCE = /RESET*PCS5*/A6*/A5*/A4*A3*/A2*/A1
IF (/13)   /BUS7 = PCS5*/A6*/A5*/A4*A3*A2*A1*ENFCH
                  +PCS5*/A6*/A5*A4*/A3*/A2*A1*ENPCH

DESCRIPTION:

I/O DEVICE NUMBER !  OUTPUT SIGNALS
-------------------------------------------------------------
IOBASE+280 (HEX)  ! /INFCH=0  AND EDOUT=1
      +282        !   -DO-          -DO-
      +284        !   -DO-          -DO-
      +286        !   -DO-          -DO-
      +28A        ! /INPCH=0 AND EDOUT=1
      +28C        !   -DO-          -DO-
      +28E        ! BUS7=ENFCH    AND EDOUT=1
      +292        ! BOS7=ENPCH     -DO-
      +288        ! /FCCE=0
-------------------------------------------------------------
```

Fig. 12. PAT575

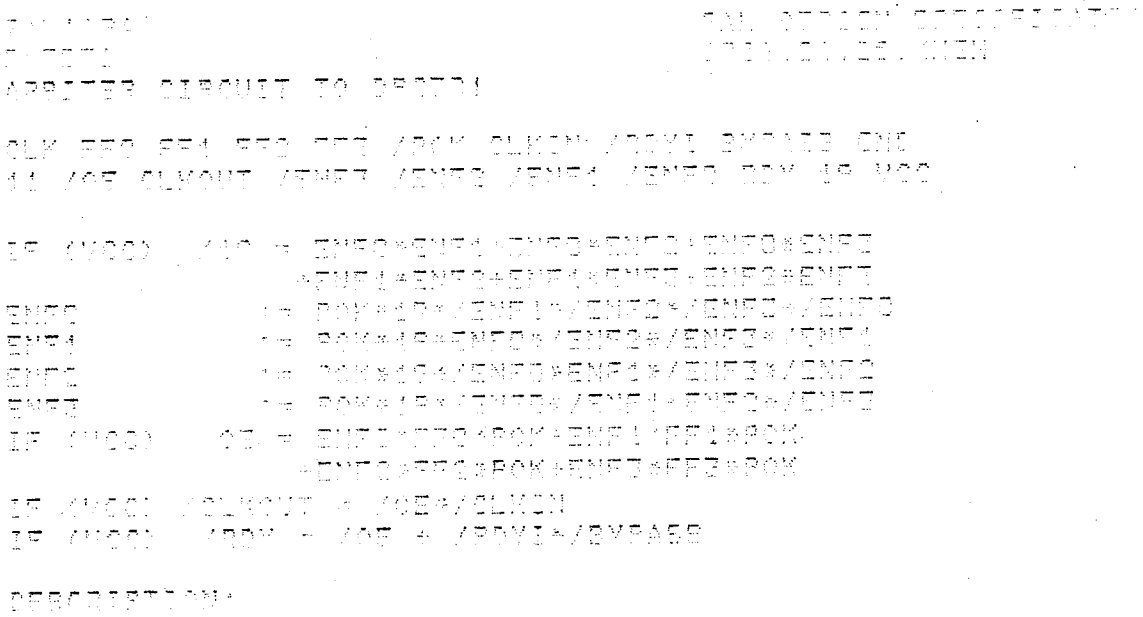


Fig. 13. PAT576

```
PAL16R4                                   PAL DESIGN SPECIFICATION
PAT589                                    1984.04.25;KNEH
ARBITER CIRCUIT TO DPC701.

CLK PF0 PF1 PF2 PF3 /POK CLKIN /FCCE /FWR GND
11 /OE CLKOUT /ENP3 /ENP2 /ENP1 /ENP0 FCONT 19 VCC

IF (VCC)     /19 = ENP0*ENP1+ENP0*ENP2+ENP0*ENP3
                  +ENP1*ENP2+ENP1*ENP3+ENP2*ENP3
ENP0              := POK*19*/ENP1*/ENP2*/ENP3*/ENP0
ENP1              := POK*19*ENP0*/ENP2*/ENP3*/ENP1
ENP2              := POK*19*/ENP0*ENP1*/ENP3*/ENP2
ENP3              := POK*19*/ENP0*/ENP1*ENP2*/ENP3
IF (VCC)      OE = ENP0*PF0*POK+ENP1*PF1*POK
                  +ENP2*PF2*POK+ENP3*PF3*POK
IF (VCC) /CLKOUT= /OE*/CLKIN
IF (VCC) /FCONT = FCCE*FWR

DESCRIPTION:
```

Fig. 14. PAT589

7. INDICATOR PANELS

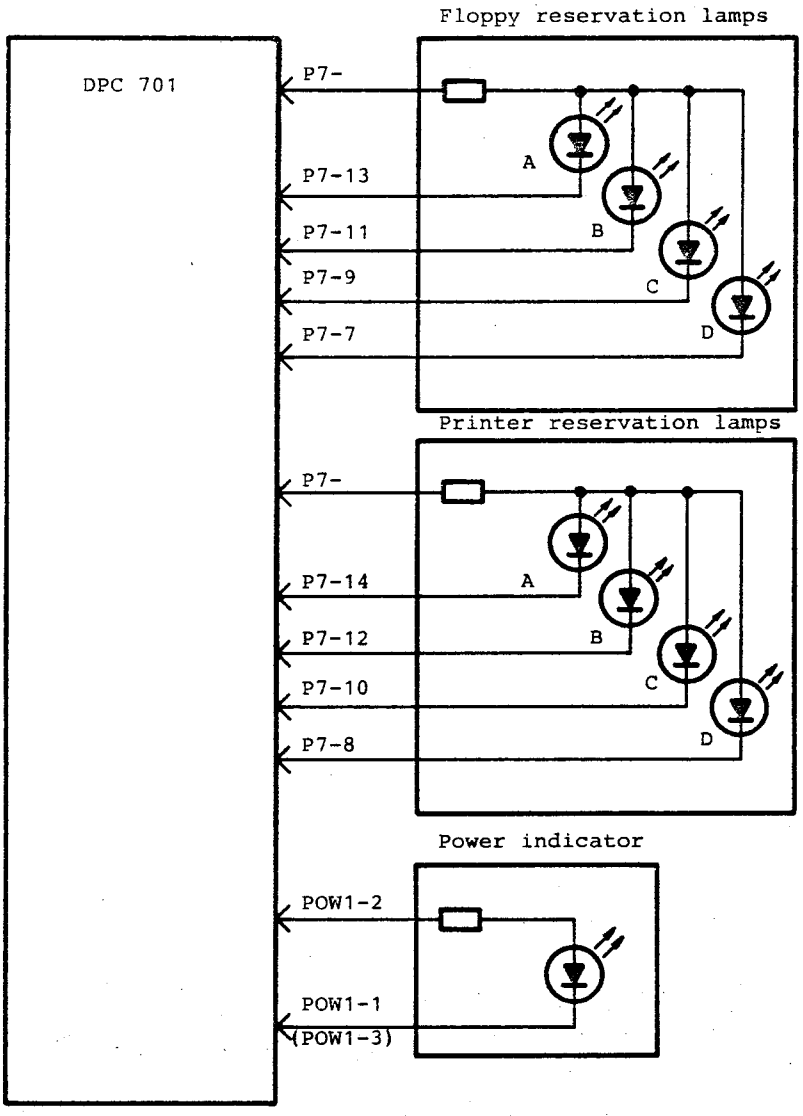
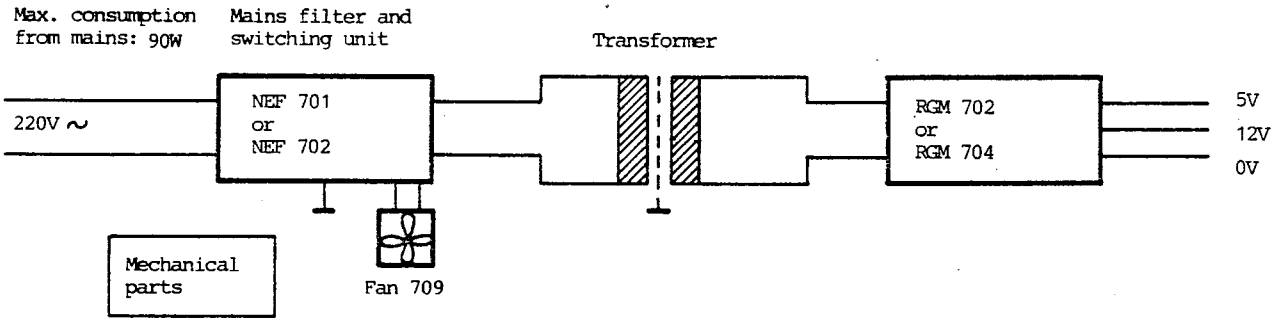


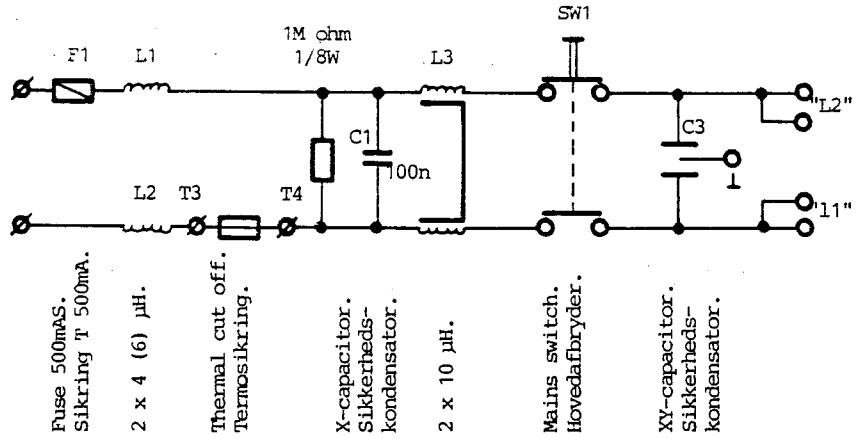
Fig. 15. Indicator Panels

8. POWER SUPPLY 8.



POW 750 is equipped with NEF 701 and RGM 702.
POW 752 is equipped with NEF 702 and RGM 704.
The transformer is introduced with the module name TRF 702. This will be changed to TRF 704 when it has reached its final outlook.

Fig. 16. Module survey of the POW750/752



PARTS LIST / STYKLISTE

RC part No	Description / Beskrivelse.
2101027	Fuse holder
2102024	500 mA fuse (slow 7 træg)
1901168	4 (6) µH coil
2118002	Thermal cut off
2003002	100n X-capacitor
1901167	2 x 10 mH choke
1510029	Mains switch
2003007	XY-capacitor
1402099	Screw terminal

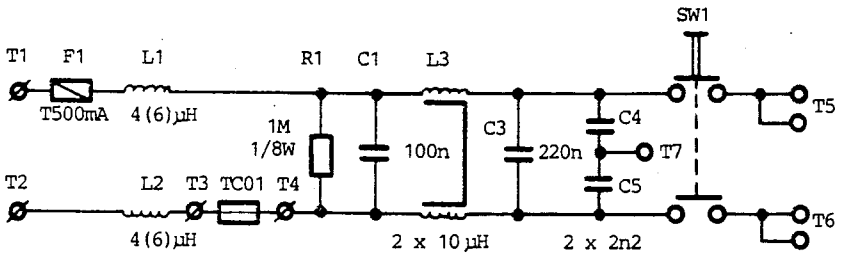
WARNING!

The NEF 701 module has vital influence on the electrical safety of the equipment in which it is mounted. Hence in case of repair it is of importance that defective are only replaced by parts of equivalent quality (see RC part No's in the parts list) and that the module is remounted as original.

ADVARSEL!

Modulet NEF 701 har vital betydning for den elektriske sikkerhed i det apparat det er monteret i. Det er derfor vigtigt, i tilfælde af reparation, at defekte dele kun erstattes med nye dele af tilsvarende kvalitet (se RC-part nr. i styklisten) og at modulet i øvrigt monteres helt som oprindeligt.

Fig. 17. NEF701 Mains Filter Unit



PARTS DESCRIPTION / KOMPONENTBESKRIVELSE

Component	Description	RC part No
F1	Fuse holder / sikringsholder	2101027
	Fuse / sikring 500 mA slow / træg	2102024
L1, L2	4 (6) µH coil / spole	1901168
TC01	Thermal cut off / termosikring 76°C	2118002
R1	1M, 1/8 W resistor / modstand	1103129
C1	X-capacitor / sikkerhedskondensator 100n	2003002
L3	Current compensated shoke / strøm-kompenseret drossel 2 x 10 mH	1901167
C3	X-capacitor / sikkerhedskondensator 220n	2003003
C4, C5	Y-capacitor / sikkerhedskondensator 2n2	2003005
SW1	Mains switch / hovedafbryder	1510029
T1, T2, T3, T4	Screw terminal / skrueterminal	1402099

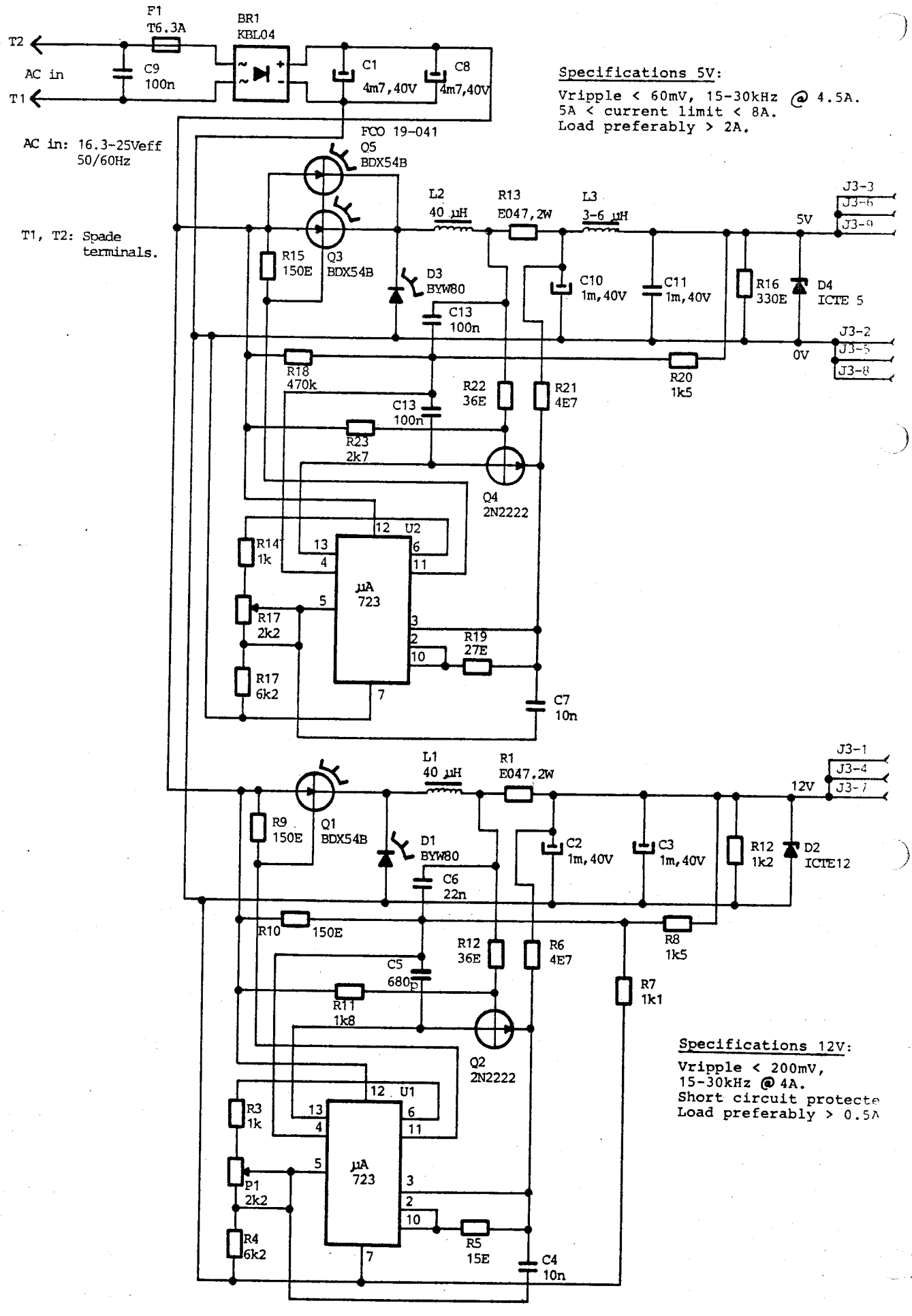
WARNING!

The NEF 702 module has vital influence on the electrical safety of the equipment in which it is mounted. Hence in case of repair it is of importance that defective are only replaced by parts of equivalent quality (see RC part No's in the parts list) and that the module is remounted as original.

ADVARSEL!

Modulet NEF 702 har vital betydning for den elektriske sikkerhed i det apparat det er monteret i. Det er derfor vigtigt, i tilfælde af reparation, at defekte dele kun erstattes med nye dele af tilsvarende kvalitet (se RC-part nr. i styklisten) og at modulet i øvrigt monteres helt som oprindeligt.

Fig. 18. NEF 702 Mains Filter Unit

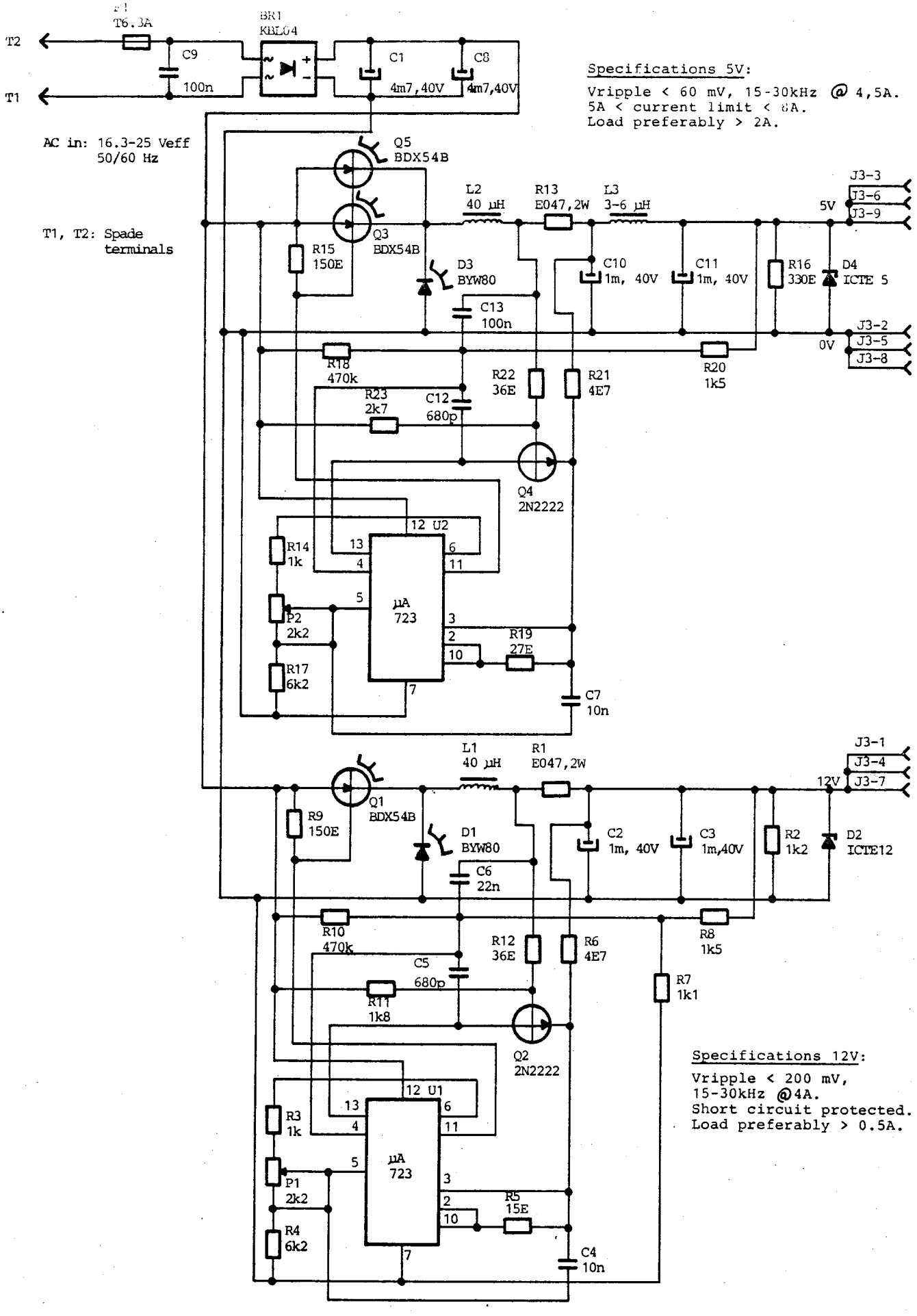


840501 GBJ 840917 MLA

RGM702

A14683

Fig. 19. RGM 702 Schematic Diagram



840501 GBJ 840917 MLA

RGM704

A14682

Fig. 20. RGM704 Schematic Diagram

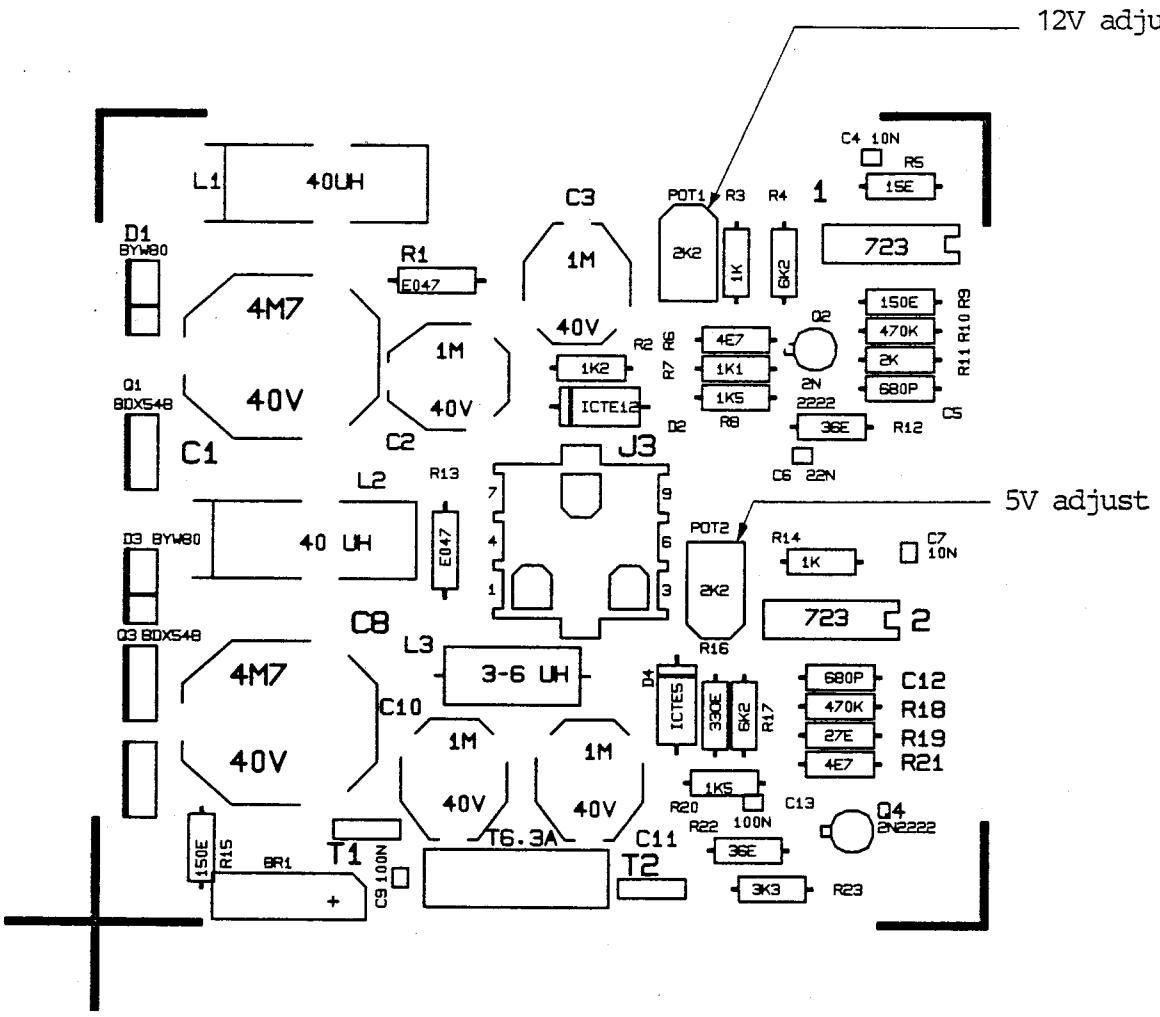


Fig. 21. Assembly Drawing RGM702/RGM704

9. JACK LISTS

Pin number	Signal Name
1	+EXP BUS 0
2	-EXP BUS 0
3	+EXP BUS 1
4	-EXP BUS 1
5	+EXP BUS 2
6	-EXP BUS 2
7	+EXP BUS 3
8	-EXP BUS 3
9	
10	
11	+EXP BUS 4
12	-EXP BUS 4
13	+EXP BUS 5
14	-EXP BUS 5
15	+EXP BUS 6
16	-EXP BUS 6
17	+EXP BUS 7
18	-EXP BUS 7
19	+EXP ADD STROBE
20	-EXP ADD STROBE
21	+EXP IORD
22	-EXP IORD
23	+EXP IOWR
24	-EXP IOWR
25	+EXP RESET
26	-EXP RESET
27	+EXP INTX 0
28	-EXP INTX 0
29	+EXP INTX 1
30	-EXP INTX 1
31	+EXP DMA
32	-EXP DMA

Pin Number	Signal name
1	/STROBE
2	PD0
3	PD1
4	PD2
5	PD3
6	PD4
7	PD5
8	PD6
9	PD7
10	/ACK
11	BUSY
12	PAPER END
13	SELECTED
14	/AUTOLF
15	/FAULT
16	/INIT
17	/SELECT
18	OV
19	OV
20	OV
21	0V
22	OV
23	OV
24	OV
25	OV

Pin number	Signal name
1	OV
2	
3	OV
4	/HEAD LOAD
5	OV
6	
7	OV
8	/INDEX
9	OV
10	/MOTOR 0 ON
11	OV
12	/DRIVE 1 SEL
13	OV
14	/DRIVE 2 SEL
15	OV
16	/MOTOR 1 ON
17	OV
18	/DIRECTION
19	OV
20	/STEP
21	OV
22	/WRITE DATA
23	OV
24	/WRITE GATE
25	OV
26	/TRACK 00
27	OV
28	/WRITE PROTECTION
29	OV
30	/READ DATA
31	OV
32	/SIDE SEL
33	OV
34	/READY

Pin number	Signal name
1	
2	
3	
4	
5	
6	
7	/FLAMP CH3
8	/PLAMP CH3
9	/FLAMP CH2
10	/PLAMP CH2
11	/FLAMP CH1
12	/PLAMP CH1
13	/FLAMP CH0
14	/PLAMP CH0
15	+5V
16	+5V

Pin number	Signal name
1	+12V
2	0V
3	OV
4	+5V

J8 Power connector

Pin number	Signal name
1	0V
2	+5V
3	0v

POW1 Connector

10.

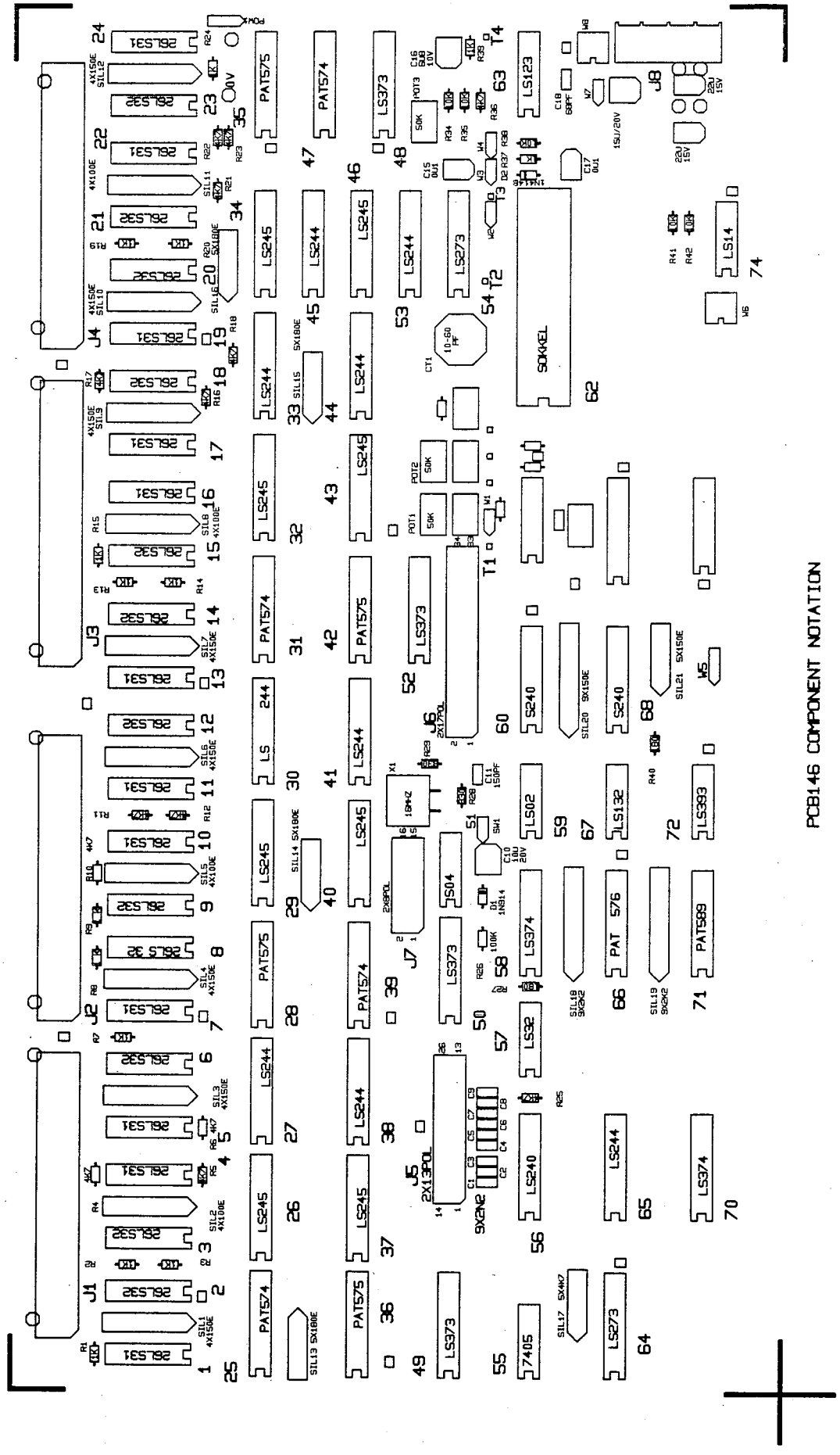


Fig. 22. Assembly Drawing DPC701

A. INDICES A.

A.1 Survey of Figures A.1

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