

Discussion of Rational Hardware

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by Mike Druke

Director of Hardware

Rational Employee #17

I will be talking about something we designed 40 years ago, so forgive this old man's memory!

Well maybe not too old.
These are from the last few days in Copenhagen



To establish my Nerd credentials,
yesterday at Hamlet's Castle I made
a Riddle:



What does
0xD4 have to do
with Hamlet?

D4 = not
2B

Personal Notes:

- Born in Vermont

3 years old, picking potatoes with my Sisters



Dad
at 92
Deer
Hunting



- Found Passion for Hardware at MIT
- Roommate with Dave Bernstein
Rational VP of Engineering
- Designed BFD6900 in 1971
with Dave at Digital Systems Lab
I am as happy doing Hardware now
as I was in this Picture 51 years ago!
- Designed Nova 2 with Dave
at Data General in 1972
- Joined Rational as employee #17
as Director of Hardware in Jan 1982.
Dave was VP Engineering.
Left in 1995.



Mike Druke, 18, Spring 1971 at MIT Digital Systems Laboratory with the "BFD 6900"

Early Rational Culture

- Founded in 1981 by 3 Air Force Academy graduates who saw the potential of ADA:
Paul Levy – President
Mike Devlin – CTO
Grady Booch – Software Architect
- Paul and Mike worked at “The Blue Cube” AF base.
They came to work often in their Captain’s uniforms.
- First financing from Arthur Rock, COB, financier of Intel and Apple.
On a demo of the 1st Prototype, he asked me “Where is the Compiler”,
I pointed to the disk
- Rule #1, no one leaves on Thursday.
Company BBQ followed by Seminars communicating progress in all areas.
Usually lasted past Midnight.
We all knew what each other was working on.
- We went to Grand China together on Friday night. Lots of work done.
- We had company picnics in the summer.
The first one was at the home of William Perry, former DOD Secretary,
board member, father of the cruise missile.

Early Design Decisions

- We would use CAD. This was in its infancy in 1982.
Mike Devlin and I visited Daisy during my job interview and bought 2 on the spot.
- We would go straight to PCB, avoiding time and frustration of Wirewrap or other prototype methodology.
This required a Simulator, no problem, Software R us! Written in ADA.
- We would design powerful Diagnostic capability.
The 8051 based Diagnostic “Archipelago”
This was invaluable for Hardware debugging, Manufacturing, and Service.
- We would have a Backplane and a Foreplane.
This made layout much easier for multiple 64-bit busses.
- We would go with our Strengths and avoid IO design,
This resulted in the World’s most expensive Unibus peripheral!
The first quad processor Series 100 had 4 PDP11 minicomputers.

Diagnostics

- Every board could drive and receive all its external pins. All registers scannable or could load into scannable register.
- We built a Lab Test jig with a ZIF Backplane connector and tested all boards stand alone. This was adapted by manufacturing.
- Chris Jacques wrote the 8051 Experiment interpreter using only 23 bytes of RAM. This allowed for 105 byte Experiment objects.
- Each HW designer wrote over 50K lines of Pascal Diagnostics.
- Hardware would “Freeze” on error and a “Tombstone” file was created for Post Mortem Diagnostics to analyze to identify FRU.
- Our first HW failure was at Lockheed. Our field guy showed up with replacement board BEFORE they knew it crashed!

Board Partitioning and Hardware

Team

- Mike Druke (MBD) did MEM board. Blazed the trail for layout and Daisy.
1st design was 8 Mbytes with 256K X 1 Dynamic Rams.
16 Set Associative design from Logical Address.
This avoided the need for a traditional Address Translation Unit.
The Architecture has no Physical Address.

128 bit bus with ECC.

The PCB fab house rejected initial design because there were way fewer Vias than their formula of Component Pads to Vias predicted.
Example of “Gestalt Design” methodology.

VAL, TYP and FIU boards

- Steve Shroder (SWS) did both VAL and TYP, They had a similar 64-bit ALU and bus structure. It was called a “Monument to MSI”. Steve was High School friend of Mike Devlin, their 1st hire.
- Mark Frappier (MSF) did FIU took 128 bits from Mem, Isolated fields from 1-64 bits, dealt with fields that crossed a 128 bit boundary. Mark worked with me at Data General. 1st occupant of “the Massachusetts Halfway House”

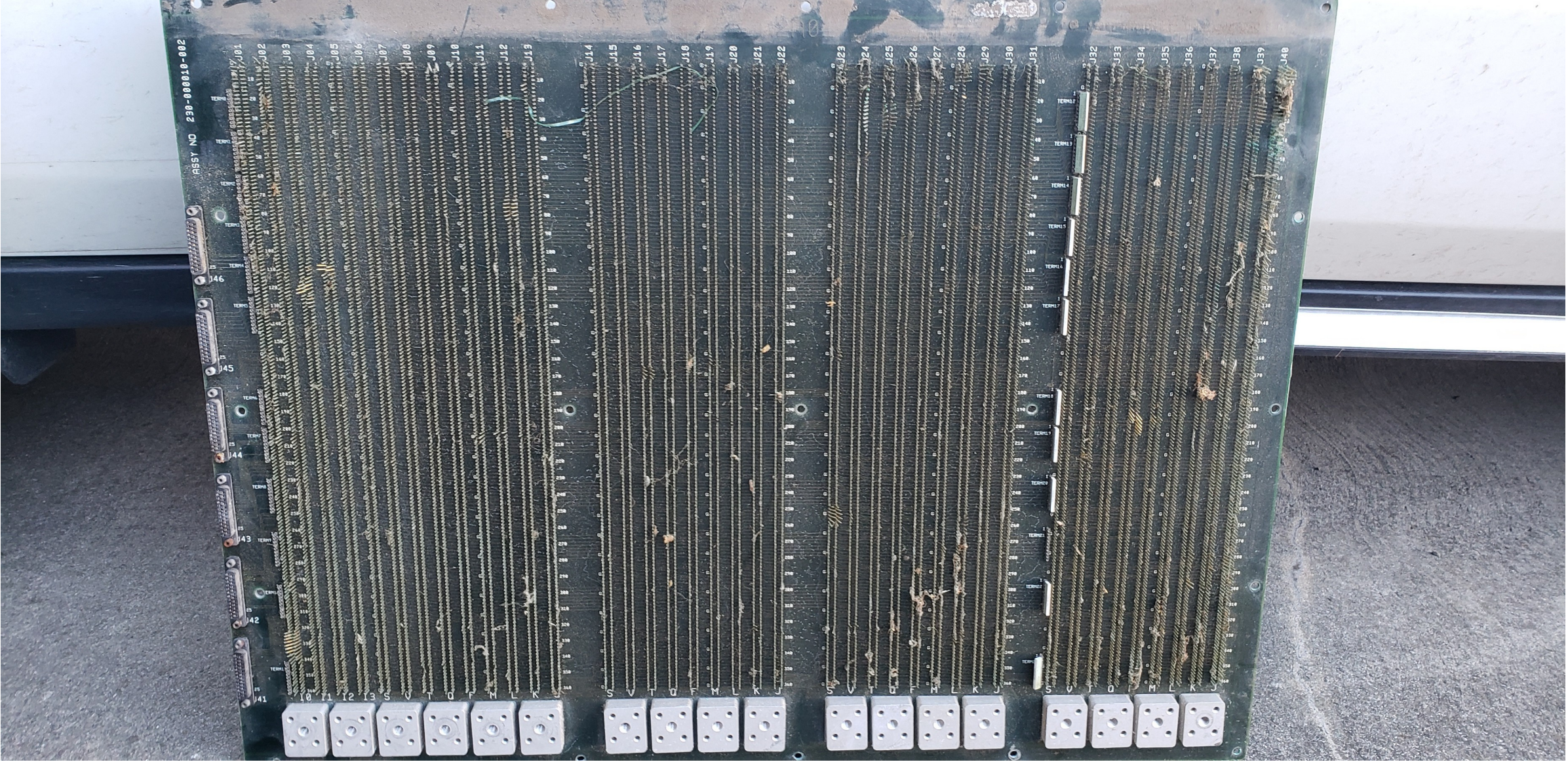
SEQ, SYS and IOA boards

- Ed Paluch (EJP) did SEQ – microprogram Sequencer
Writable Control Store
- Jim Wilson (JAW) did SYS – multiprocessor arbiter, Memory ECC
- Dave Bernstein (DHB) did IOA, produced a Unibus
This was amazing considering he did have other “unreal work”
as VP of Engineering.
ALL managers at Rational did “real work”. We managed by example.
- Chris Jacques (CJJ) did Expmon and 8051 interpreter and Daisy tools.
Every Hardware team needs a software engineer.
I worked with Chris at Data General on the microEclipse IC.

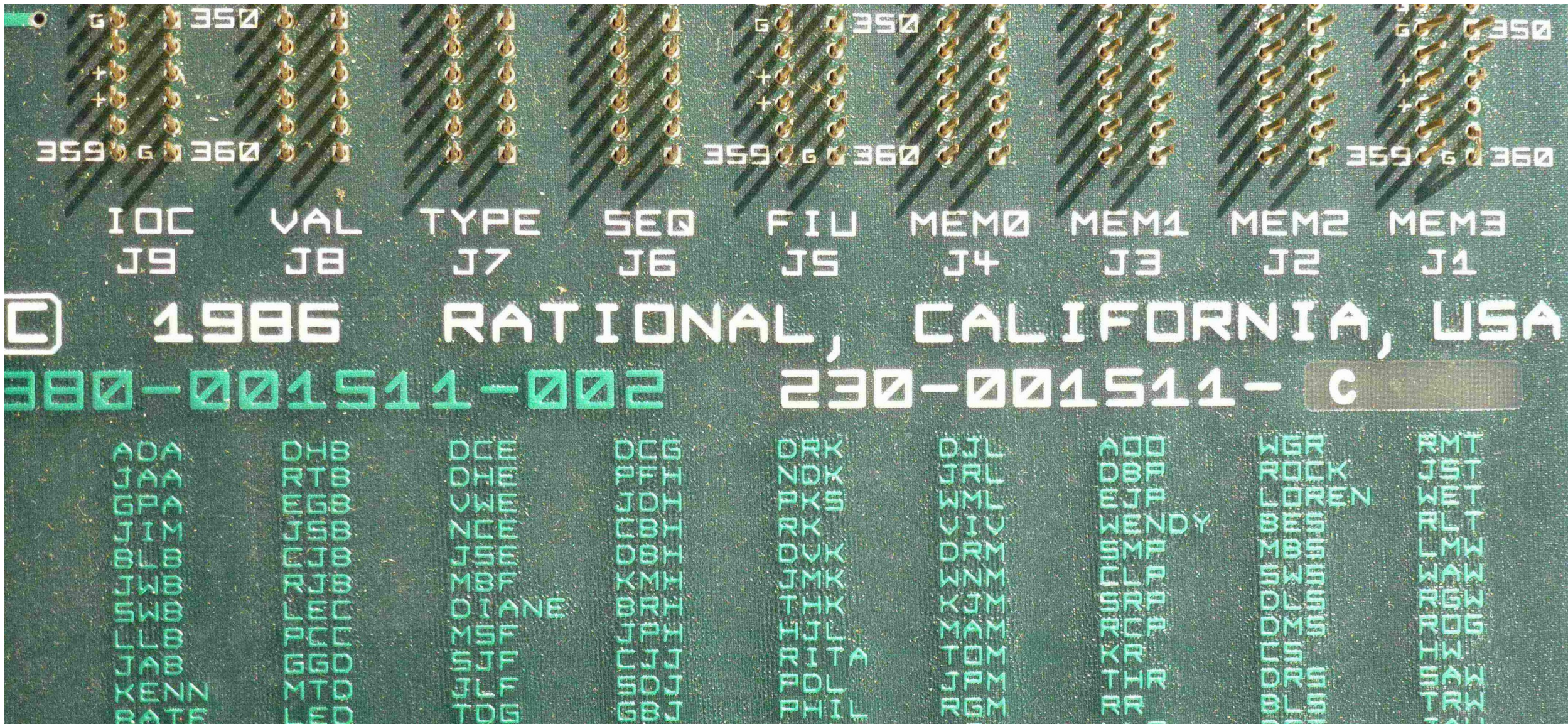
Series 100, 200, 300 and 400

- Series 100 – 1983 Quad Processor, Massive machine
Mike Devlin and I could barely tip it as required by UL tip test.
Price \$1Million
- Series 200 – 1986 Punted multiprocessing, PDP-11
Wayne Meretsky designed IOC with Motorola 6800 processor.
Wayne was from DG and a resident of “Massachusetts Halfway House”
Ken Barton was hired from Tandem to do Mechanical design.
- Series 300 – 1988 “Skin job” much smaller package, updated IO devices
- Series 400 – 1990 Upgraded Memory to 32Mbytes, smaller package
used Exabyte tape rather than Mag Tape drive

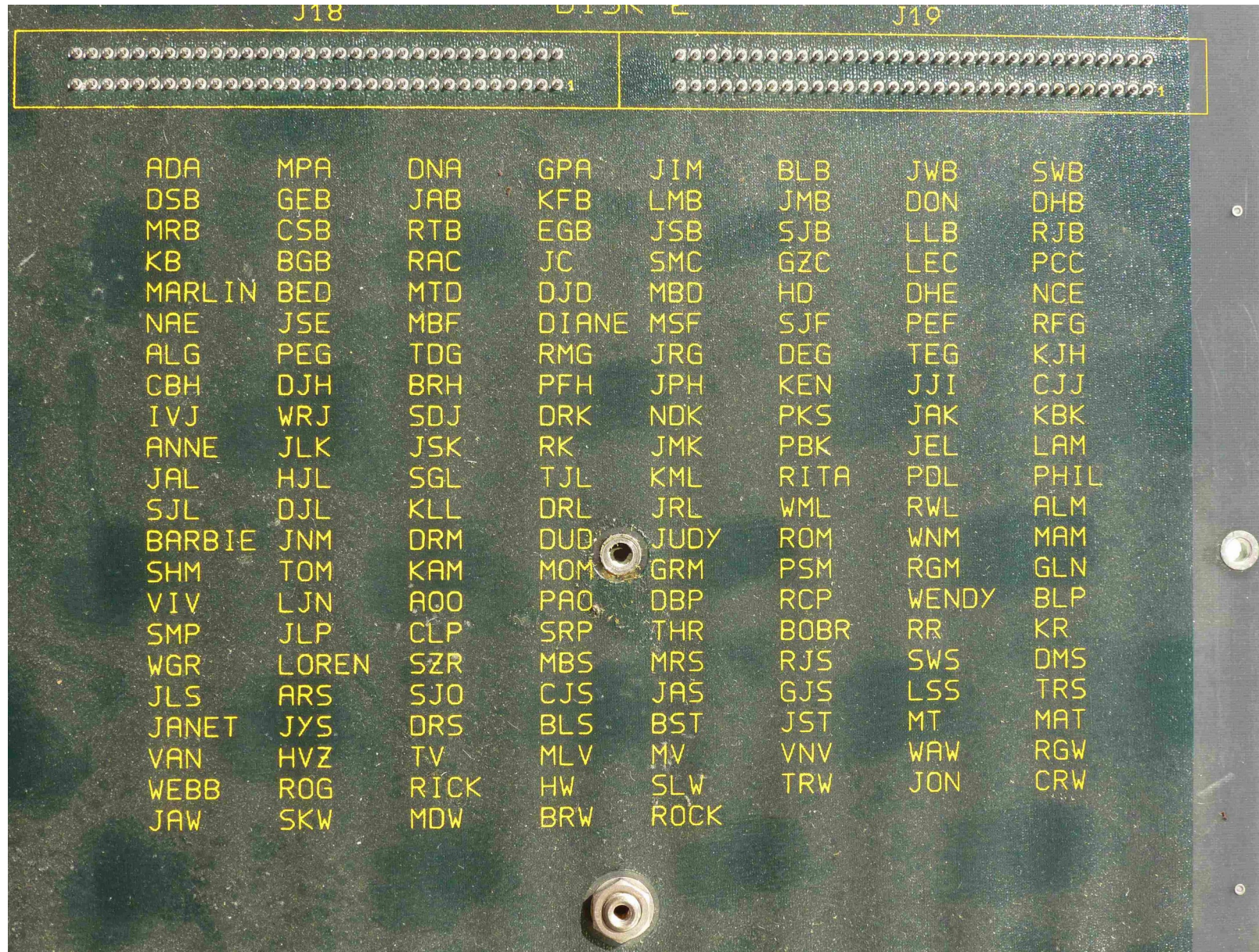
R1000 Backplane



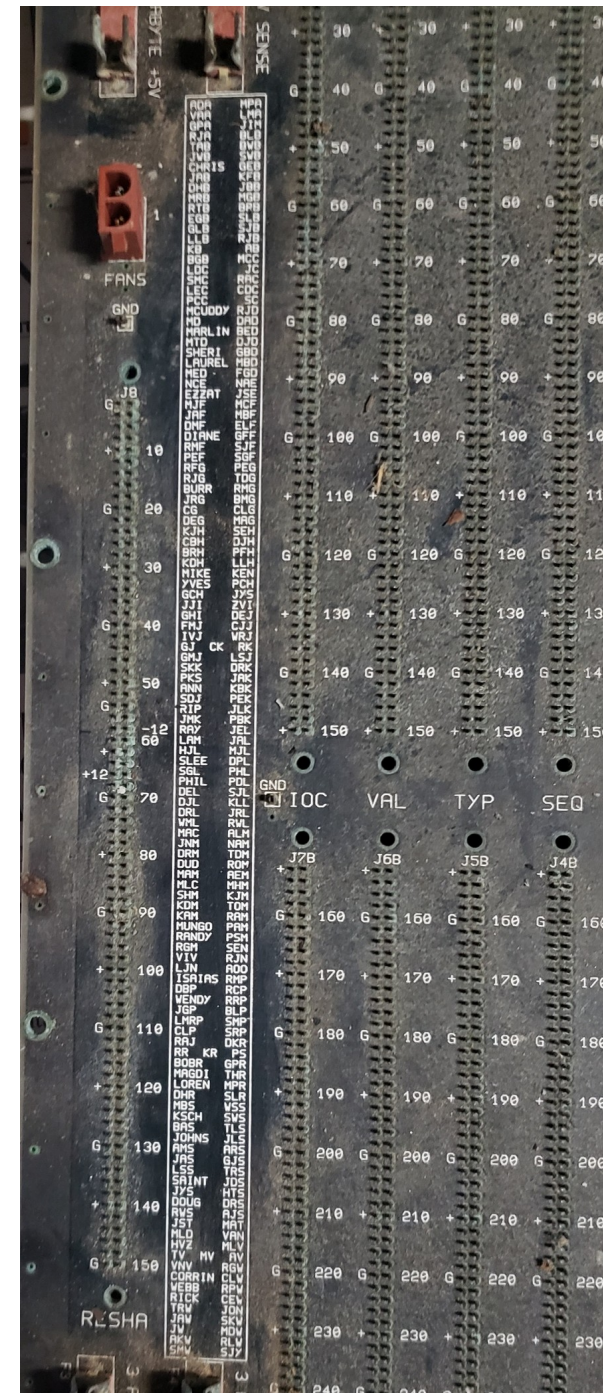
Series 200 Initials



Series 300 Initials



Series 400 Initials



Thank you for this opportunity

Questions?