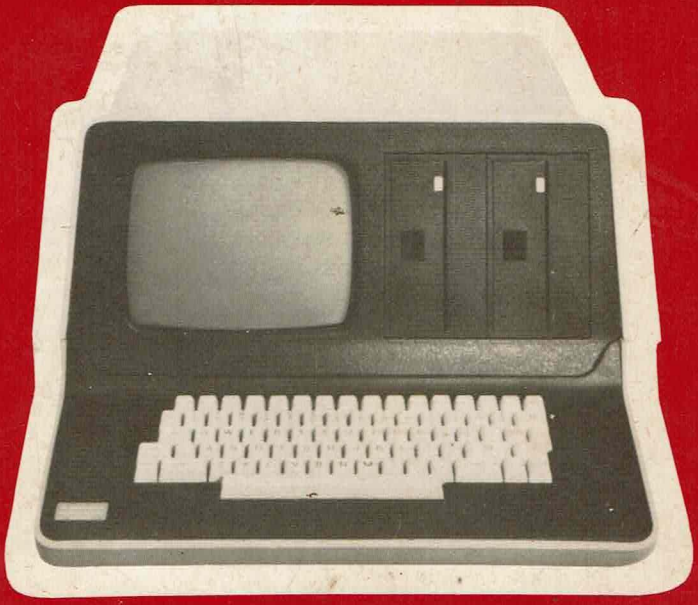
MOTOROLA

microsystems

EXORset 30
User's Guide



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Eks nr 1

EXORset 30
User's Guide

Printed in Switzerland

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

The EXORset is a cost-effective, yet powerful development tool used in the design and development of microcomputer systems.

The EXORset is made up of 6 distinct functional units :

- The EXORset Main Controller Board.
- The 9 " CRT and dual mini-floppy assembly.
- The Floppy Disk Controller and 16K-byte RAM board.
- The ASCII keyboard and function keys assembly.
- The power supply unit.
- The enclosure.

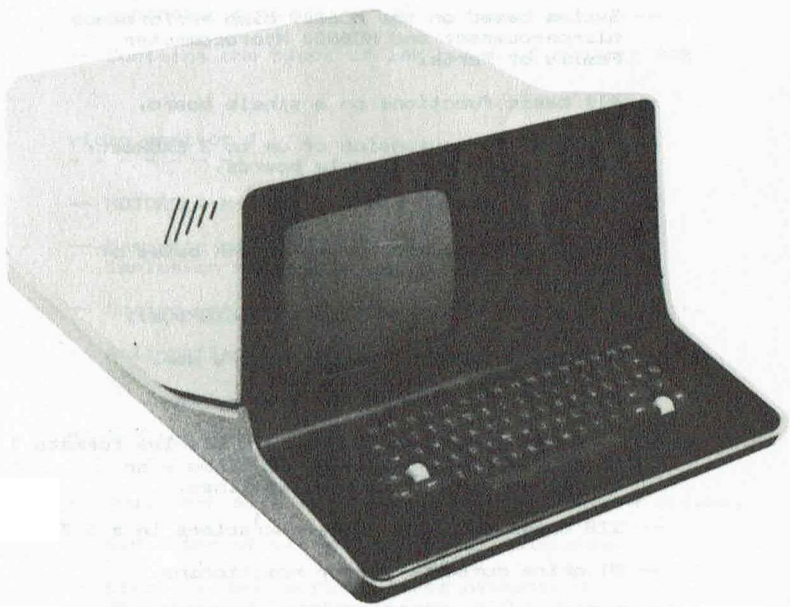


Figure 1-1 Typical EXORset System

1.2 FEATURES

1.2.1 Operational Features

-- Use as a stand-alone system or as a terminal.

-- Design concept that permits additional functions to be incorporated by way of optional hardware and / or software.

-- Software-controlled operation selection.

-- Full ASCII keyboard and 16 user-defined function keys.

1.2.2 Hardware Features

Main controller board :

-- System based on the MC6809 high performance microprocessor and MC6800 Microcomputer Family of Parts.

-- All basic functions on a single board.

-- Provides for expansion of up to 3 EXORset, EXORciser or Micromodule boards.

-- 32K bytes of RAM.

-- 12 E/P/ROM sockets for up to 24K bytes of user code or system firmware.

-- 4K bytes of monitor firmware (EXORbus).

-- User selectable alternate memory map.

-- 2K bytes of alphanumeric display RAM.

-- 2 user-selectable alphanumeric display formats : 80 characters per line by 22 lines , or 40 characters per line by 16 lines.

-- 128 upper and lower case characters in a 5x7 matrix.

-- Blinking cursor - Cursor positioning.

-- Full graphic capability in a 320x256 dot pattern.

-- Alphanumeric and graphic displays may be mixed.

-- 9 " video monitor and / or TV interface.

-- Audible alarm.

-- 61-key ASCII keyboard and 16 function keys interface.

-- Printer interface (parallel, CENTRONICS type).

-- 1200 baud audio-cassette interface.

-- RS-232C serial interface.

-- Provision for Real Time Clock using the built-in MC6840 PTM.

-- RESET switch to restart user operation.

Floppy disk controller board :

-- Uses the MC6843 Floppy Disk Controller.

-- Provides direct control of up to 3 mini-floppy disk drives via resident driver firmware.

-- Provides direct interface with the EXORset expansion bus.

-- Contains one block of 16K bytes of dynamic RAM.

Video monitor :

-- MOTOROLA M-2000 9" CRT display.

-- Magnetic deflection type CRT with integral implosion protection.

-- Coated with P4 (white) or P31 (green) phosphor.

-- Anti-reflective shield.

Mini-floppy drives :

-- Dual BASF 6106 (or equivalent) mini-floppy drives.

-- 80K bytes of storage capacity / diskette.

-- Single sided, soft-sectored diskette : 40 tracks, 16 sectors/track, 128 bytes/sector.

Keyboard assembly :

-- 63-key (61 used) full ASCII.

-- 16 user definable function keys.

-- Encoded on the main controller board.

-- Soft touch feel.

1.2.3 Software features

The EXORbus system development firmware contains the system development and diagnostic programs, as well as the system control routines : display, keyboard, communication and operation control.

1.3 SPECIFICATIONS

The specifications of the various functional units are identified in the following paragraphs.

1.3.1 Main Controller Board Specifications

Power requirements (max)	5V/6A, +12V/1A, -12V/1A
Operating temperature	0 to 50 deg.C
Processor	MC6809
Word size	
Data	8 bits
Address	16 bits
Instructions	8,16,24,32 bits
Instructions	59 instruction mnemonics
Addressing modes	10
Clock cycle time	1 microsecond
Baud rates	110 - 2400
Memory size	up to 32K bytes of RAM and up to 24K bytes of E/ROM available to user.
Serial interface	
Input	EIA RS-232C
Output	EIA RS-232C
Physical Characteristics	
Dimensions (WxD)	248 mm x 504 mm
Board thickness	1.6 mm
I/O connectors	
Parallel interface	50-pin card edge connector
Serial interface	20-pin card edge connector
Cassette	5-pole DIN connector
CRT	Coax connector
Keyboard	ASCII : flex-tail,23-pin or card edge, 50-pin Funct.keys : flex-tail,8-pin or card edge, 20-pin

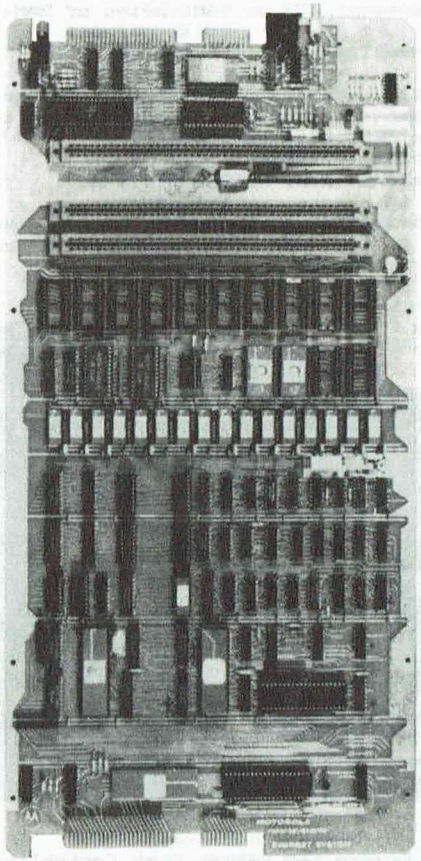


Figure 1-2 Main Controller Board

1.3.2 Floppy Disk Controller Board Specifications

Power requirements (max)	5V/0.8A, +12V/0.2A, -12V/0.15A
Operating temperature	0 to 50 deg.C
Memory size	16K bytes of RAM, 1K bytes of E/ROM (disk driver)
Interface	
Output	TTL open collector
Input	220/330 ohm line terminations
Physical characteristics	
Dimensions (WxD)	248 x 146 mm
Board thickness	1.6 mm
Connector	34-pin card edge connector

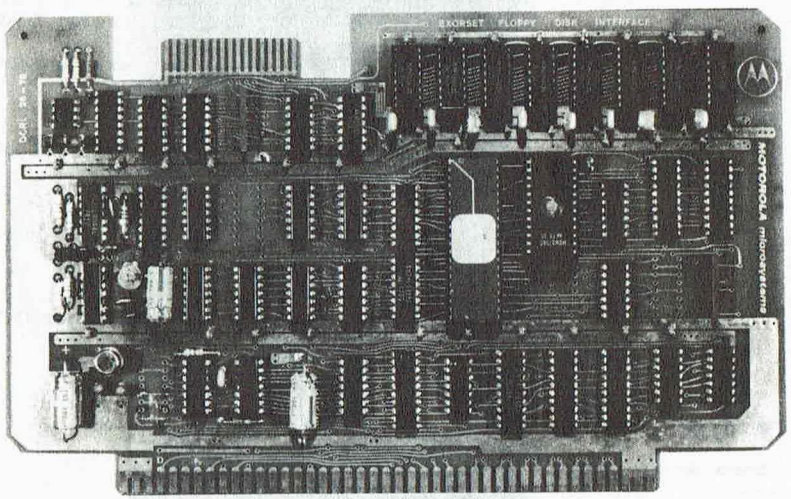


Figure 1-3 Floppy Disk Controller Board

1.3.3 Video Display Specifications

Cathode Ray Tube	9 inches measured diagonally (22.8 cm) - 44 sq.inch viewing area (28.4 sq.cm) - 90 deg. deflection angle - integral implosion protection - P4 (white) or P31 (green) phosphor.
Power input	12 Vdc at 900 milliamperes
Input signals	Composite video , 0.5 to 2.5 V composite P/P , negative sync , input impedance : 75 ohms
Video response	Within 3dB , 10 Hz to 12 MHz
Pulse rise time	20 V rise in 40 nanoseconds
Resolution	650 lines at center , 500 lines at corners
Distorsion/lin.	Less than 2% , measured with standard EIA ball chart and dot pattern
High voltage	9.5 kV at 50 microamp.beam current
Horiz.blanking	11.0 microseconds min (includes retrace and delay)
Scanning freq.	Horiz. 15,750 +/- 500 Hz Vert. 50 / 60 Hz
Controls	Brightness, vertical linearity, horizontal size, raster centering, vertical hold, horizontal hold
Dimensions	7.25 inches high (18.4 cm) - 9.50 inches wide (24.1 cm) - 9.48 inches deep (24.1 cm)
Weight	Net 8 lbs (3.6 kg)
Environment	Operating temperature 0 to 55 deg.C - Storage temp. -40 to +65 deg.C - Operating altitude 10,000 ft max.(3048 m) - Humidity 10% to 90% relative, non-condensing - Approved under spec. 478 (Electronic Data Processing Equipment Components) - Designed to comply with applicable DHEW rules on X-radiation

1.3.4 Optional UHF Modulator Specifications

Type	ASTEC UM1231
Supply voltage	+5 V +/- 0.2 V
Supply current	3.5 mA
Vision carrier	Channel E36, 591.25 MHz +/-5 MHz
RF output (HI)	1.5 mV +/-4 dB, Vmod = 0.6 V
RF output (LO)	-20 dB -6/+2, Vmod = 0.25 V
3 dB bandwidth	8 MHz (1.6 MHz @ 6dB)
Spurious output	<-30 dB
Spurious FM of carrier	5 kHz
Positive mod.charact.	0 V @ pin 2
Negative mod. charact.	0.85 V +/-0.1 V @ pin 2
Oscillator stop voltage	3.5 V
Mod. input impedance	1.5 Kohm @ output HI
RF output impedance	75 ohm
Volt. stand. wave ratio	< 2.0

1.3.5 Mini-floppy Disk Drive Specifications

Type	BASF 6106
Storage capacity	
Formatted	81,920 bytes / disk 40 tracks / disk 2,048 bytes / track 16 sectors / track 128 bytes / sector
Access time	
Latency	200 ms max / 100 ms average
Track to track	12 ms
Average	240 ms
Settling time	50 ms max
Head load time	35 ms max
Rotational speed	300 RPM
Recording density	2768 BPI (inside track)
Flux density	5536 FCI
Track density	48 TPI
Track radius	57.15 mm (2.25 in) (track 0) 36.5125 mm (1.4375 in) (track 39)
Encoding method	FM
Media requirements	BASF 606 or equivalent
Environment	
Operating temp.	10 to 50 deg C
Relative humidity	20 to 80 %
Power requirements	+5 Vdc / 0.5 A max, max 50 mVpp ripple +12 Vdc / 0.6 A max, max 100 mVpp ripple Drive motor start current 1.4 A max, 1.2 A typ.for 50 ms Head load start current 0.7 A for 50 ms
Power dissipation	10.5 W operating 4.0 W stand-by (motor off) 8.0 W motor on and desselect
Mechanical dimensions	
Width	146.1 mm (5.75 in.)
Height	53.5 mm (2.11 in.) drive, 82.5 mm (3.25 in.) front panel
Depth	190.0 mm (7.48 in.)
Weight	1.4 kg

1.3.6 Keyboard Specifications

ASCII keys number	61
Output	8 x 8 + 6 x 1 matrix
Function keys number	16
Output	4 x 4 matrix
Contacts	screened mylar technology or mechanical
"On" resistance	< 200 ohms
Physical dimensions	417 x 160 mm max (outline dim.)

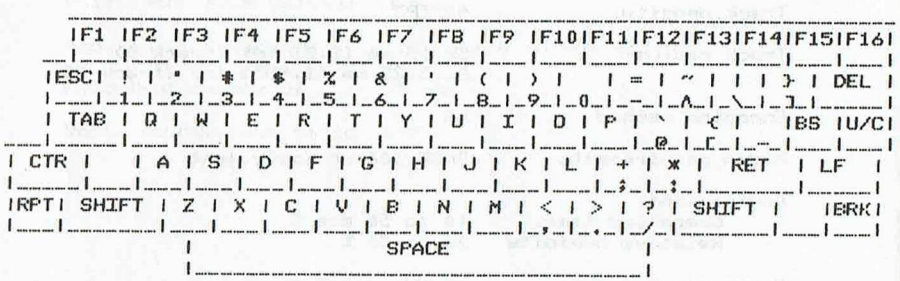


Figure 1-4 Keyboard Assembly

1.3.7 Power Supply Specifications

Input voltage	95 to 125 / 205 to 250 VAC 47 to 420 Hz single phase
Output voltages	+5 Vdc / 10 A, 2mV RMS ripple -12 Vdc / 1.0 A, 1 mV RMS ripple +12 Vdc / 5.0 A, 1 mV RMS ripple
Calibration range	+5 Vdc +/- 0.5 Vdc +/- 12 Vdc +/- 1.0 Vdc
Over-voltage protection	5 Vdc output - output rise to 7 V reduced to 5 V or less within 50 microseconds
Power fail (Transients)	5 Vdc : +7 V / -0.5 V max +12 Vdc : +17 V / -0.3 V max
Remote sense	5 Vdc output - compensate up to 0.5 Vdc drop
Operating temp.	0 to 70 deg C - 70 % derating between 50 and 70 deg C
Dimensions	
Length	241.3 mm (9.5 in.)
Width	158.8 mm (6.25 in.)
Height	127.0 mm (5.0 in.)

1.3.8 Enclosure Specifications

Material	Polyurethane, fire retardant
Dimensions	
Width	465.0 mm (18.3 in.)
Height	280.0 mm (11.0 in.)
Length	640 mm (25.2 in.)
Weight	6.300 kg

1.4 EQUIPMENT SUPPLIED

The EXORset 30 includes the functional units listed in paragraph 1.1 and described in paragraph 1.3 .

1.5 OPTIONAL EQUIPMENT

A number of separately available, optional memory modules, additional interface modules and E/PROM programmer module (up to three) may be added to the system simply by plugging them into the existing connectors of the main controller board. In addition to these modules, the user has the option of purchasing various types of line printers. Note that the use of some of the additional modules may require reprogramming of the EXORset address decoding PROMs. Note also that the modules without VXA/VUA selection jumpers will always respond in the map 2 of the EXORset.

CHAPTER 2

INSTALLATION INSTRUCTIONS AND INTERCONNECTION CONSIDERATIONS

2.1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, and interconnection instructions for the EXORset. This chapter also discusses the EXORset interconnection signals, as well as the jumper wire options.

2.2 UNPACKING INSTRUCTIONS

Unpack the EXORset from its shipping carton and, referring to the packing list, verify that all of the items are present, including any of the options that may have been ordered. Save the packing materials for storing or reshipping of the system. If the shipping carton is damaged upon receipt, request that the carrier's agent be present while the system is being unpacked and inspected.

2.3 INSPECTION

The EXORset should be inspected upon receipt for broken, damaged, or missing parts or any other physical or electrical damage.

BEFORE FIRST APPLYING POWER TO THE SYSTEM, check that all connectors are properly inserted (power, keyboard, floppy-disk, CRT) as well as the floppy-disk Controller Module and the optional modules, if any. Check also that all IC's are properly installed in their sockets.

2.4 INSTALLATION INSTRUCTIONS AND INTERCONNECTIONS

Tables 2-1 to 2-12 list the pin assignments of the various connectors located on the EXORset boards and subassemblies. Refer to Chapter 7 for connectors and jumpers location.

EXORset Main Controller Board :

CONNECTOR	TYPE	NAME	TABLE
J01	23-pin Flex-Tail or 50-pin Card-Edge	ASCII Keyboard	Table 2-4
J02	8-pin Flex-Tail or 20-pin Card-Edge	Function keys	Table 2-5
J03	20-pin Card-Edge	RS-232C	Table 2-3
J04	50-pin Card-Edge	Printer	Table 2-2
J05	DIN	Audio-Cassette	Table 2-6
J06	CINCH	Video Display	Table 2-7
J07	2x43-pin	EXORset Bus	Table 2-1
J08	2x43-pin	EXORset Bus	Table 2-1
J09	2x43-pin	EXORset Bus	Table 2-1
J10	2-pin	Audible Alarm	Table 2-8
PWR	10-pin	Power	Table 2-9

EXORset Mini-Floppy Disk Controller Board :

CONNECTOR	TYPE	NAME	TABLE
P2	34-pin Card-Edge	Disk Interface	Table 2-12
P1	2x43-pin	EXORset Bus	Table 2-1

Mini-Floppy Disk Drive :

CONNECTOR	TYPE	NAME	TABLE
J1	34-pin Card-Edge	Disk Interface	Table 2-12
J2	4-pin	Power	Table 2-11

Video Display :

CONNECTOR	TYPE	NAME	TABLE
P2	10-pin Card-Edge	CRT Input	Table 2-10

Keyboard Assembly :

CONNECTOR	TYPE	NAME	TABLE
ASCII	23-pin Flex-Tail or 50-pin Card-Edge	ASCII Output	Table 2-4
FUNCT	8-pin Flex-Tail or 20-pin Card-Edge	Function Keys	Table 2-5

Table 2-1 EXORset Expansion Bus Signals (J07,J08,J09)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
A	+5 Vdc	+5 Vdc POWER - Used for the system logic circuits and available to the user for prototype module requirements (10 amps tot. max).
B	+5 Vdc	+5 Vdc POWER - Same as above.
C	+5 Vdc	+5 Vdc POWER - Same as above.
D	IRQ	INTERRUPT REQUEST - A low level sensitive input signal to the MPU used to request generation of an MPU interrupt sequence. The MPU will wait until it completes the instruction being executed before it recognizes the request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin executing the interrupt sequence.
E	NMI	NON-MASKABLE INTERRUPT - A low going edge sensitive input signal to the MPU used to request generation of a MPU non-maskable interrupt sequence. The MPU will wait until it completes the instruction being executed before it recognizes the request. At that time, regardless of the logic state of the Interrupt Mask Bit in the MPU Condition Code Register, the MPU will begin executing the non-maskable interrupt.
F	VMA	VALID MEMORY ADDRESS - This signal is connected to +5V in the EXORset.
H	----	NOT USED - Reserved for system expansion.
J	E	ENABLE - Clock signal generated by the clock circuitry on the EXORset Main Controller Board. E is similar to phase 2 clock in 6800 systems.
K	GND	GROUND - Power ground for +/- 12 Vdc.
L	MEMCLK	MEMORY CLOCK - Unbated, TTL level E clock signal.
M	-12Vdc	-12 Vdc POWER - Used for system logic and available to the user for custom designed prototype modules (1.0 A max).
N	----	NOT USED

P	BA	BUS AVAILABLE - This signal, decoded with Bus Status (BS) indicates the MPU state : BS BA 0 0 Normal 0 1 Interrupt Acknowledge 1 0 Sync. Acknowledge 1 1 Halt or Bus Grant
R	MEMRDY	MEMORY READY - Not used in the EXORset.
S	LIC	LAST INSTRUCTION CYCLE - Not used in the EXORset.
T	+12Vdc	+12 Vdc POWER - Used for the system logic and available to the user for custom designed prototype modules (5.0 A max).
U	STANDBY	STANDBY POWER - Not used in the EXORset.
V	PWRFAIL	POWER FAIL - Not used in the EXORset
W	PARITY	PARITY ERROR - Not used in the EXORset.
X	GND	GROUND
Y	GND	GROUND
Z	GND	GROUND
Anot	FIRQ	FAST INTERRUPT - A low level sensitive input to the MPU used to request generation of an MPU fast interrupt sequence. The MPU will wait until it completes the instruction being executed before it recognizes the request. At that time, if the fast interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin executing the fast interrupt sequence.
Bnot	GND	GROUND
Cnot	RAS	ROW ADDRESS STROBE - This signal, generated by the EXORset Main Controler Board is used to control the 16K RAM block located on the Floppy-Disk Controller Board. This signal is only connected to the first (J07) bus expansion connector.
Dnot	CAS	COLUMN ADDRESS STROBE - Same as RAS above.
Enot	EAHL	ADDRESS HIGH/LOW - Same as RAS above .
Fnot	----	USER DEFINED - This signal may be used for custom modules.
Hnot	D3not	DATA (bit 3) - One of 8 bi-directional data lines used to provide a two-way data transfer between the MPU and all other plug-in modules

within the system. The data bus drivers on the other modules are in their off or high impedance state except when selected during a memory read or write operation.

Jnot	D7not	DATA (bit 7) - Same as D3not on pin Hnot.
Knot	D2not	DATA (bit 2) - Same as D3not on pin Hnot.
Lnot	D6not	DATA (bit 6) - Same as D3not on pin Hnot.
Mnot	A14	ADDRESS (bit 14) - One of the 16 address lines from the MPU that permits the MPU to select any addressable memory location within the EXORset.
Nnot	A13	ADDRESS (bit 13) - Same as A14 above.
Pnot	A10	ADDRESS (bit 10) - Same as A14 above.
Rnot	A9	ADDRESS (bit 9) - Same as A14 above.
Snot	A6	ADDRESS (bit 6) - Same as A14 above.
Tnot	A5	ADDRESS (bit 5) - Same as A14 above.
Unot	A2	ADDRESS (bit 2) - Same as A14 above.
Vnot	A1	ADDRESS (bit 1) - Same as A14 above.
Wnot	GND	GROUND
Xnot	GND	GROUND
Ynot	GND	GROUND
1	+5 Vdc	+5 Vdc POWER - Used for the system logic circuits and available to the user for prototype module requirements (10 A total max).
2	+5 Vdc	+5 Vdc POWER - Same as above.
3	+5 Vdc	+5 Vdc POWER - Same as above.
4	G/H	GO/HALT - When this input to the MPU is in the high state, the MPU will fetch the instruction addressed by the program counter and start instruction execution. When low, all activity in the MPU will be halted. This input is level sensitive.
5	RESET	RESET - This buffered input signal to the MPU is used to restart the EXORset when power is initially applied. Restart occurs on the low-to-high transition of the RESTART signal. If the RESTART pushbutton switch, located on the Main Controller Board, is depressed while the system is operating, the low-to-high transition of the RESET signal will cause the

MPU to execute the EXORbus restart routine or the restart routine indicated by the user.

6	R/W	READ/WRITE - This signal is generated by the MPU and indicates to the other modules contained within the system that the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Additionally, when the MPU is halted, this signal will be in the read state.
7	Qout	Qout - A quadrature clock signal generated by the MPU which leads the E (enable) signal.
8	GND	GROUND - Power ground for +/-12Vdc.
9	GND	GROUND - Power ground for +/-12Vdc.
10	VUA	VALID USER'S (ALTERNATE MAP) ADDRESS - This signal, along with VXA, allows all additional modules to respond to either address map 1 or address map 2. This signal is controlled by the EXORbus monitor.
11	-12Vdc	-12Vdc POWER - Used for the system logic circuits and available to the user for custom designed prototypes modules (1.0 A max).
12	REFREQ	REFRESH REQUEST - Not used in the EXORset. Due to its design concept, the EXORset does not provide the capability of stretching the clock, thus do not allow the use of cycle stealing mode of dynamic memory refresh .
13	REFGNT	REFRESH GRANT - Same remark as above.
14	DEBUG	DEBUG - Not used in the EXORset.
15	TSG	THREE-STATE GRANT - Not used in the EXORset.
16	+12Vdc	+12Vdc POWER - Used for the system logic circuits and available to the user for prototype module requirements.
17	STANDBY	STANDBY POWER - Not used in the EXORset.
18	CLOCK	CLOCK - Not used in the EXORset.
19	VXA	VALID EXECUTIVE (ALTERNATE MAP) ADDRESS - This signal, along with VUA, allows all additional modules to respond to either address map 1 or address map 2.
20	GND	GROUND
21	GND	GROUND
22	GND	GROUND

23	BS	BUS STATUS - This signal, decoded with Bus Available (BA) indicates the MPU state : BA BS 0 0 Normal 0 1 Interrupt Acknowledge 1 0 Sync. Acknowledge 1 1 Halt or Bus Grant
24	GND	GROUND
25	---	USER DEFINED - This signal line may be used for custom modules.
26	---	USER DEFINED - Same as above.
27	---	USER DEFINED - Same as above.
28	---	USER DEFINED - Same as above.
29	D1not	DATA (bit 1) - Same as D3not on pin Hnot.
30	D5not	DATA (bit 5) - Same as above.
31	D0not	DATA (bit 0) - Same as above.
32	D4not	DATA (bit 4) - Same as above.
33	A15	ADDRESS (bit 15) - Same as A14 on pin Mnot.
34	A12	ADDRESS (bit 12) - Same as above.
35	A11	ADDRESS (bit 11) - Same as above.
36	A8	ADDRESS (bit 8) - Same as above.
37	A7	ADDRESS (bit 7) - Same as above.
38	A4	ADDRESS (bit 4) - Same as above.
39	A3	ADDRESS (bit 3) - Same as above.
40	A0	ADDRESS (bit 0) - Same as above.
41	GND	GROUND
42	GND	GROUND
43	GND	GROUND

Table 2-2 Parallel I/O Connector Pin Assignments (J04)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1	INPUT	INPUT PRIME - A low-level output signal which clears the printer buffer and initializes the logic. (Not used by all printers).
3	GND	GROUND - Printer interface ground.
5	FAULT	FAULT - A low-level input signal that indicates a printer fault condition such as paper empty, light detect, or a desselect condition. (Not used by all printers).
7	GND	GROUND - Same as pin 3.
9	PB7	PERIPHERAL DATA LINE (PB7) - Audio-cassette Receive Data.
11	PB6	PERIPHERAL DATA LINE (PB6) - Audio-cassette Transmit Data.
13	PB5	PERIPHERAL DATA LINE (PB5) - Free.
15	PB4	PERIPHERAL DATA LINE (PB4) - Free.
17	PB3	PERIPHERAL DATA LINE (PB3) - Free.
19	BUSY	BUSY - An input signal indications that the printer cannot receive data.
21	OUT-PP	OUT OF PAPER - A high-level input indicating the printer is out of paper.
23	SEL	SELECT - A high-level input signal indicating that the printer is selected.
25	PD8	PERIPHERAL DATA LINE (PD8) - Output data to printer from PA7 of PIA.
27	PD7	PERIPHERAL DATA LINE (PD7) - Same as pin 25 except bit A6.
29	PD6	PERIPHERAL DATA LINE (PD6) - Same as pin 25 except bit A5.
31	PD5	PERIPHERAL DATA LINE (PD5) - Same as pin 25 except bit A4.
33	PD4	PERIPHERAL DATA LINE (PD4) - Same as pin 25 except bit A3.
35	PD3	PERIPHERAL DATA LINE (PD3) - Same as pin 25 except bit A2.

37	PD2	PERIPHERAL DATA LINE (PD2) - Same as pin 25 except bit A1.
39	PD1	PERIPHERAL DATA LINE (PD1) - Same as pin 25 except bit A0.
41	GND	GROUND - Same as pin 3.
43	DATASTB	DATA STROBE - A 1.0 microsecond output pulse used to clock data from the MPU to the printer logic.
45	GND	GROUND - Same as pin 3.
47	ACKNLG	ACKNOWLEDGE - A low-level input pulse indicating the input of a character into memory or the end of a functional operation.
49	GND	GROUND - Same as pin 3.

All even numbers (2-50) : GROUND.

MATING CONNECTOR :
3M 3415-0001 or equivalent.

Table 2-3 RS-232C Interface Signals (J03)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1	GND	GROUND
2	----	NOT USED
3	TxDATA	TRANSMITTED DATA - An RS-232C compatible serial data input to the Receive Data (Rx Data) input of the ACIA (modem configuration).
4	----	NOT USED
5	RxDATA	RECEIVED DATA - An RS-232C compatible serial data output from the Transmitted Data (Tx Data) output of the ACIA (modem configuration).
6	----	NOT USED
7	RTS	REQUEST TO SEND - A jumper-enabled RS-232C compatible output used to request that a peripheral or modem begin sending data. This output is connected only when Micromodule 11 is being used to provide a translation from RS-232C to 20 mA neutral current loop.
8	----	NOT USED
9	CTS	CLEAR TO SEND - A high level RS-232C compatible output used to constantly enable the peripheral input/output device.
10	----	NOT USED
11	DSR	DATA SET READY - A high level RS-232C compatible output used to constantly enable the peripheral input/output device.
12	----	NOT USED
13	GND	GROUND
14	DTR	DATA TERMINAL READY - An RS-232C compatible input used to provide automatic control of the transmitting end of a communication link by inhibiting the Transmit Data Register Empty (TDRE) status bit in the ACIA.
15	SIGDET	SIGNAL DETECT - A high level RS-232C compatible output line used to constantly enable the peripheral input/output device.
16	+5V	+5 Vdc - Not normally used. Available for

		Micromodule 11.
17	GND	GROUND
18	-12V	-12 Vdc - Not normally used. Available for Micromodule 11.
19	GND	GROUND
20	+12V	+12 Vdc - Not normally used. Available for Micromodule 11.

MATING CONNECTOR :
3M 3461-0001 or equivalent.

Table 2-4 ASCII Keyboard Connector Pin Assignments
(J01,Keyboard Assembly)

FLEX-TAIL PIN	CARD-EDGE PIN	NAME
1	45	Row 0
2	43	Row 2
3	41	Row 4
4	39	GND for ctrl keys (column 8)
5	37	RPT (Row F)
6	35	Row 6
7	33	CTRL (Row E)
8	31	Row 7
9	29	SHIFT (Row I)
10	27	SHIFT LOCK (Row J) (not used)
11	25	Column 0
12	23	Column 1
13	21	Column 2
14	19	Column 3
15	17	Column 4
16	15	Column 5
17	13	Column 6
18	11	Column 7
19	9	NUM PAD (Row G) (not used)
20	7	U/C (Row H)
21	5	Row 5
22	3	Row 3
23	1	Row 1

MATING CONNECTOR :
Flex-Tail : 23-pin PCI M-1255 or MOLEX 4850 or equivalent
Card-edge : 3M 3415-0001 or equivalent.

Table 2-5 Function Keys Connector Pin Assignments (J02,Keyboard Assembly)

FLEX-TAIL PIN	CARD-EDGE PIN	NAME
1	15	Row A
2	13	Row C
3	11	Row B
4	9	Row D
5	7	Column A
6	5	Column B
7	3	Column D
8	1	Column C

MATING CONNECTOR :
Flex-Tail : 8-pin PCI M-1255 or MOLEX 4850 or equivalent
Card-Edge : 3M 3461-0001 or equivalent.

Table 2-6 Audio-Cassette DIN Connector Pin Assignments (J05)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1,4	REC	RECORD - Audio signal to the audio-cassette
2	GND	GROUND
3,5	PLAY	PLAYBACK - Audio signal from the audio-cassette

MATING CONNECTOR :
DIN 41524 Mas5S (5-role, 180 deg.).

Table 2-7 Composite Video Connector Pin Assignments(J06)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1	VID	VIDEO OUT - Composite video out
2	GND	GROUND

Table 2-8 Audible Alarm Connector Pin Assignments(J10)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1	POS	POSITIVE - Buzzer positive end.
2	NEG	NEGATIVE - Buzzer negative end.

Table 2-9 Main Controller Board Power Connector (PWR)

PIN	SIGNAL	WIRE COLOR
1	+5 Vdc	Red
2	+5 Vdc	Red
3	+5 Vdc sense	Red
4	+12 Vdc return	Orange
5	+5 Vdc sense return	Black
6	-12 Vdc return	Green
7	+5 Vdc return	Black
8	-12 Vdc	Blue
9	+5 Vdc return	Black
10	+12 Vdc	Red / White

MATING CONNECTOR :
AMP 1-480285-0 or equivalent.

Table 2-10 Video Display Connector Pin Assignments (P2)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1	GND	GROUND - Video signal return
2	RB	REMOTE BRIGHTNESS - 200 kohm pot. terminal 1
3	RB	REMOTE BRIGHTNESS - 200 kohm pot. terminal 2
4	RB	REMOTE BRIGHTNESS - 200 kohm pot. cursor
5	____	N.C. - Not connected
6	TTLH	TTL HORIZ. SYNC. IN - Not used.
7	+12V	+12 V - +12 V power in.
8	VID	VIDEO IN - Composite video in.
9	TTLV	TTL VERT. SYNC. IN - Not used.
10	GND	GROUND - +12 V power return

MATING CONNECTOR :
AMP 583299-1 or equivalent.

Table 2-11 Mini-Disk Drive Power Connector Pin Assignments (J5)

PIN	SIGNAL
1	+12 Vdc
2	+12 V return
3	+5 Vdc return
4	+5 V

MATING CONNECTOR :
AMP 1-480424-0 with pins 60619-1 or equivalent.

Table 2-12 Mini-Floppy Disk Drive Signal Connector Pin Assignments (J1)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
2	HDL	HEAD LOAD - This logic low level output signal is used to position the flexible diskette against the recording head.
4	----	NOT USED -
6	RDY	READY - This logic low level signal (generated by the disk drive electronics) is used to indicate that the flexible diskette is inserted correctly into the disk drive, and that the dc voltage levels and disk speed is correct.
8	IDX	INDEX - A logic low level signal from the disk drive used to indicate the beginning of a track. This pulse occurs once per revolution of the diskette (200 ms period).
10	SEL0	SELECT 0 - This logic low level signal is used to select drive 0.
12	SEL1	SELECT 1 - Same as pin 10, except for drive 1.
14	SEL2	SELECT 2 - Same as pin 10, except for drive 2 (not used in the EXORset).
16	MOT	MOTOR ON - This logic low signal is used to turn the drive(s) motor(s) on.
18	DIR	DIRECTION - This signal is used in conjunction with the STEP signal to move the R/W head from track to track. When this signal is a logic low level, the R/W head is moved to the lower numbered tracks (out). When this signal is a logic high level, the head moves to the higher numbered tracks (in). This signal must remain in the desired logic state during the duration of the STEP signal.
20	STP	STEP - This signal is used in conjunction with the DIRECTION signal to move the R/W head from track to track. A logic low level pulse causes the head to be moved one track (step) in the direction indicated by the DIRECTION signal.
22	WDT	WRITE DATA - This signal consists of logic low level pulses representing data to be recorded on the flexible diskette. Write current reverses direction on the leading edge of each pulse.

24	WGT	WRITE GATE - A logic low level signal used to enable recording of data on the flexible diskette. When this signal is a logic high level, reading data from the flexible disk is enabled.
26	TRZ	TRACK 0 - Logic low level signal used to indicate when the R/W head is positioned over track 0.
28	WPT	WRITE PROTECT - A logic low signal indicating that the diskette is write protected (write protect notch of the diskette left open).
30	RDT	READ DATA - Unseparated "Raw Data" (clock and data) read from the diskette.
32	---	NOT USED -
34	---	NOT USED -

All odd pins (1-33) : GROUND

MATING CONNECTOR :
3M 3463-0001 or equivalent.

2.5 JUMPER CONNECTIONS

Table 2-13 lists the jumper connections of the Main Controller Board and Table 2-14 the jumpers connections of the Mini-Floppy Disk Controller Board. Figure 2-1 and Figure 2-2 show the location of the various jumpers on the boards.

Each jumper is pre-wired on the printed circuit, so that a default operation is defined. The printed circuit track should be cut and an alternate jumper installed only if a different function is desired. The pre-wired state of each jumper is given in parenthesis in the tables below.

Table 2-13 EXORset Main Controller Board Jumper Options

JUMPER			FUNCTION
SW1 (OUT)			UHF modulator modulation polarity :
IN			Nesative modulation (CCIR TV standard)
OUT			Positive modulation (French TV standard)
SW2-1 (OUT)	SW2-2 (OUT)		PIA1 data lines :
IN	X		PB6 available on J04 pin 11
X	IN		PB7 available on J04 pin 9
SW3-1 (OUT)	SW3-2 (OUT)	SW3-3 (OUT)	PIA1 B-side interrupt :
IN	OUT	OUT	to MPU NMI
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU IRQ
SW4-1 (OUT)	SW4-2 (OUT)	SW4-3 (OUT)	ACIA interrupt :
IN	OUT	OUT	to MPU NMI
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU IRQ
SW5-1 (OUT)	SW5-2 (OUT)	SW5-3 (OUT)	Micromodule 11 supply :
IN	IN	IN	+5 Vdc, -12 Vdc, +12 Vdc available for Micromodule 11 on J03 pin 16, 18 and 20 respectively
SW6-1 (OUT)	SW6-2 (OUT)	SW6-3 (OUT)	PIA1 A-side interrupt :
IN	OUT	OUT	to MPU NMI
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU IRQ
SW7-1 (IN)	SW7-2 (OUT)	SW7-3 (OUT)	PTM interrupt :
IN	OUT	OUT	to MPU NMI
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU IRQ

SW8-1 (OUT)	SW8-2 (IN)	SW8-3 (OUT)	RS-232C interface :
IN	OUT	OUT	SIGDET is input to ACIA DCD
OUT	IN	OUT	SIGDET is output and high level
OUT	OUT	IN	RTS is available on J03 pin 7
SW9 1-4 (IN)		SW9 2-3 (IN)	Graphic RAM base address :
1-4		1-3	0000
1-4		2-3	4000
2-4		1-3	8000
SW10-1 (OUT)	SW10-2 (IN)		2K/4K E/ROM option :
OUT	IN		2K E/ROM device in socket U14
IN	OUT		4K E/ROM device in socket U14
SW11-1 (OUT)	SW11-2 (IN)		2K/4K E/ROM option :
OUT	IN		2K E/ROM device in socket U16
IN	OUT		4K E/ROM device in socket U16
SW12-1 (OUT)	SW12-2 (IN)		2K/4K E/ROM option :
OUT	IN		2K E/ROM device in socket U18
IN	OUT		4K E/ROM device in socket U18
SW13-1 (OUT)	SW13-2 (IN)		2K/4K E/ROM option :
OUT	IN		2K E/ROM device in socket U20
IN	OUT		4K E/ROM device in socket U20
SW14-1 (OUT)	SW14-2 (IN)		2K/4K E/ROM option :
OUT	IN		2K E/ROM device in socket U31
IN	OUT		4K E/ROM device in socket U31
SW15-1 (OUT)	SW15-2 (IN)		2K/4K E/ROM option :
OUT	IN		2K E/ROM device in socket U22
IN	OUT		4K E/ROM device in socket U22
SW16-1 (OUT)	SW16-2 (IN)		2K/4K E/ROM option :
OUT	IN		2K E/ROM device in socket U33
IN	OUT		4K E/ROM device in socket U33

SW17-1 (IN)	SW17-2 (OUT)	Address decode PROMs select :
IN	OUT	PROM chip select to GND
OUT	IN	PROM only selected during MPU access

SW18-1 (OUT)	SW18-2 (OUT)	SW18-3 (OUT)	EXORset initialization at power-up :
OUT	X	X	80 characters / line display
IN	X	X	40 characters / line display
X	OUT	X	50 Hz (EUR)
X	IN	X	60 Hz (USA)
X	X	OUT	MAP 1
X	X	IN	MAP 2

SW19-1 (OUT)	SW19-2 (IN)	SW19-3 (OUT)	PIA3 A-side interrupt :
IN	OUT	OUT	to MPU FIRQ
OUT	IN	OUT	to MPU NMI
OUT	OUT	IN	to MPU IRQ

SW20-1 (OUT)	SW20-2 (OUT)	SW20-3 (OUT)	PIA3 B-side interrupt :
IN	OUT	OUT	to MPU FIRQ
OUT	IN	OUT	to MPU NMI
OUT	OUT	IN	to MPU IRQ

SW21-1 (OUT)	SW21-2 (OUT)	SW21-3 (OUT)	Keyboard encoder language selection :
OUT	OUT	OUT	English
IN	IN	OUT	Spanish
OUT	OUT	IN	German
IN	OUT	IN	Swedish
OUT	IN	IN	Norwegian / Danish
IN	IN	IN	French

NOTE : for other languages than english (standard), the character generator and the keyboard key tops must be changed accordingly.

SW22-1 (OUT)	SW22-2 (OUT)	SW22-3 (IN)	PIA2 B-side interrupt :
IN	OUT	OUT	to MPU IRQ
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU NMI

SW23-1 (OUT)	SW23-2 (OUT)	SW23-3 (IN)	PIA2 A-side interrupt :
IN	OUT	OUT	to MPU IRQ
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU NMI

SW24-1 (OUT)	SW24-2 (IN)	Audio-cassette playback signal phase selection :
IN	OUT	playback signal not inverted
OUT	IN	playback signal inverted

NOTE : some cassette recorders invert the recorded signal, therefore jumper SW24 allows for proper phase recovering

SW25-1 (OUT)	SW25-2 (OUT)	SW25-3 (OUT)	Non-standard bus signals :
OUT	OUT	OUT	RAS', CAS', EAHL' to J07 only
IN	IN	IN	RAS', CAS', EAHL' to J07, J08, J09

Table 2-14 EXORset Mini-Floppy Disk Controller Board Jumper Options

SWA-1 (OUT)	Low current signal :
IN	to P2 pin 34 (provision for norm. drives)
OUT	if mini-floppy drives are used
SWA-2 (OUT)	Optional drive 3 :
IN	SELECT3 signal to P2 pin 4
OUT	not connected

SWA-5 (OUT)	SWA-6 (IN)	FDC clock select :
IN	OUT	1 MHz clock to FDC (provision for normal drive)
OUT	IN	500 KHz clock to FDC (mini-floppy)

SWA-7 (OUT)	SWA-8 (IN)	MEMCLK / E select :
IN	OUT	MEMCLK signal to FDC / clock divider
OUT	IN	E signal to clock divider

16K RAM base address select :

SWB-4 (OUT)	SWB-3 (IN)	SWB-2 (IN)	SWB-1 (OUT)	
IN	OUT	IN	OUT	0000
IN	OUT	OUT	IN	4000
OUT	IN	IN	OUT	8000
OUT	IN	OUT	IN	C000

FDC and disk driver base address :

SWC-8 (OUT)	SWC-7 (IN)	SWC-6 (OUT)	SWC-5 (IN)	SWC-4 (OUT)	SWC-3 (IN)	SWC-2 (IN)	SWC-1 (OUT)	
IN	OUT	IN	OUT	IN	OUT	IN	OUT	0000
IN	OUT	IN	OUT	IN	OUT	OUT	IN	1000
IN	OUT	IN	OUT	OUT	IN	IN	OUT	2000
IN	OUT	IN	OUT	OUT	IN	OUT	IN	3000
IN	OUT	OUT	IN	IN	OUT	IN	OUT	4000
IN	OUT	OUT	IN	IN	OUT	OUT	IN	5000
IN	OUT	OUT	IN	OUT	IN	IN	OUT	6000
IN	OUT	OUT	IN	OUT	IN	OUT	IN	7000
OUT	IN	IN	OUT	IN	OUT	IN	OUT	8000
OUT	IN	IN	OUT	IN	OUT	OUT	IN	9000
OUT	IN	IN	OUT	OUT	IN	IN	OUT	A000
OUT	IN	IN	OUT	OUT	IN	OUT	IN	B000
OUT	IN	OUT	IN	IN	OUT	IN	OUT	C000
OUT	IN	OUT	IN	IN	OUT	OUT	IN	D000
OUT	IN	OUT	IN	OUT	IN	IN	OUT	E000
OUT	IN	OUT	IN	OUT	IN	OUT	IN	F000

SWD-1 (OUT)	SWD-2 (IN)	READY select :
IN	OUT	READY generated on-board (for drives without READY signal)
OUT	IN	READY signal from the drive

Map assignment :

SWD-3 (OUT)	SWD-4 (OUT)	SWD-7 (OUT)	SWD-8 (IN)	
IN	OUT	IN	OUT	FDC and disk driver in map 1 16K RAM in map 2
IN	OUT	OUT	IN	FDC and disk driver in map 2 16K RAM in map 1
OUT	IN	IN	OUT	FDC and disk driver in map 2 16K RAM in map 2
OUT	IN	OUT	IN	FDC and disk driver in map 1 16K RAM in map 1
OUT	OUT	X	X	FDC and disk driver respond in both maps 16K RAM in map 1 or 2 (depending on SWD-7 and SWD8)
X	X	OUT	OUT	FDC and disk driver in map 1 or 2 (depending on SWD-3 and SWD-4) 16K RAM responds in both maps

2.6 USE AS A TERMINAL

The user has the option of connecting the EXORset to a RS-232C compatible device (e.g. an EXORciser). The switch SW4-1 must be installed. To connect the EXORset to a 20 mA current loop device, use the Micromodule M68MM11 (RS-232C to TTY adapter). Refer to the M68MM11 manual for installation.

For a description of the signals available on the RS-232C connector, refer to Table 2-3.

The necessary cable is a 25-conductor flat cable with, at the EXORset end a :

3M-3461-0001, 2 x 10-pin card edge connector (or equivalent)

(conductors 21 to 25 not used)

and at the peripheral end a :

ANSLEY 501-659-2, 25-pin connector (or equivalent)

To switch the EXORset from the stand-alone mode of operation (off-line) to the terminal mode of operation (on-line), enter the command :

XCOM

To switch the EXORset from the terminal mode of operation (on-line) to the stand-alone mode of operation (off-line), enter the sequence :

ESC-O

CHAPTER 3

OPERATION

3.1 INTRODUCTION

Information in this chapter is intended to familiarize the user with the location and function of the EXORset controls. Directives to control the operation of the EXORset, control or modify the format of displayed data may be entered directly from the keyboard or via the communication interface. These directives are detailed in this chapter.

3.2 RESET CONTROL

The RESET pushbutton is located on the edge of the EXORset Main Controller Board. The RESET switch is used to reinitialize and restart the system. The RESET signal reinitializes also the keyboard encoder microprocessor and desselects the mini-floppy drives.

3.3 OPERATION CONTROLS

Table 3-1 lists the 'ESCAPE' sequences (ESC key followed by the character corresponding to the desired command), the commands, and the special keys used to control the various modes of operation.

Table 3-1 Operation Controls

ESCAPE SEQUENCES :

ESC-B	Background change toggle.
ESC-C	Erase from cursor position.
ESC-E	Erase screen.
ESC-F	Display format toggle : 80 characters per line by 22 lines or 40 characters per line by 16 lines
ESC-G	Bell.
ESC-H	Cursor left one column.
ESC-K	Erase line where the cursor rests.
ESC-L	Cursor home.
ESC-N	Cursor right one column.
ESC-O	Return from the terminal mode to the stand-alone mode of operation.
ESC-S	Alphanumeric mode on.
ESC-T	Alphanumeric mode off.
ESC-U	Cursor up one line.
ESC-V	Cursor down one line.
ESC-Y	Graphic mode on.
ESC-Z	Graphic mode off.

OPERATION COMMANDS :

TMAP	Address map toggle. EXORbus monitor displays a "." when the EXORset operates in map 1, and a ":" when the EXORset operates in map 2 (see CHAPTER 5 for the map 1 / map 2 definition).
XCOM	Switch to the terminal mode of operation.

SPECIAL KEYS :

U/C	UPPER CASE - Upper case / Lower case characters toggle.
RPT	REPEAT - This key depressed together with any other key will cause the character to be repeated at a rate of about 15 Hz.
BRK	BREAK - The BRK key is used to ABORT (exit from) a program in the stand-alone mode of operation. The control returns to EXORbus and prints the contents of the MPU registers. IF THE BREAK KEY HAS BEEN DEPRESSED ONLY ONCE, the aborted program can be re-entered by typing the EXORbus command : ;P This feature is specially important if the BREAK key has been depressed unintentionally !

3.4 MINI-FLOPPY DISK OPERATION

There are no front panel controls on the mini-disk drive. Proper loading of the mini-disk is vital to the operation of the mini-disk and drive. Depress the front door in the middle to open the drive. Insert the mini-disk with label toward the door. Insure that the mini-disk is fully inserted before closing the door. It is important that the mini-disk be handled and stored properly. A damaged or contaminated mini-disk can impair or prevent recovery of data and can result in damage to the read/write head. In order to assure trouble-free operation and enhance the service life of the mini-disk, the following procedure for handling should be observed :

- Return the mini-disk to the protective jacket when not in use.
- Store the mini-disk vertically; do not stack.
- Avoid exposing the mini-disk to any magnetizing force in excess of 50 oersted. (Note : the 50 oersted level of magnetizing force is reached at a distance of approximately 76 mm (3 inches) from a typical source, e.g. motors, generators, transformers).
- Do not store the mini-disk in direct sunlight; warping could result.
- Do not use a lead pencil or ballpoint pen to write on the label; use a felt tip pen and mark lightly on the label.

3.5 OPERATOR TEST PROCEDURE AND SELF-TEST

The basic operation of the EXORset can be validated by an operator- monitored series of checks and tests.

3.5.1 Operation Checks

When the EXORset is powered up, and after a one-minute warmup, the screen should be blank, with following message appearing in the upper left-hand corner of the screen :

.EXORBUG J.k

where J.k is the monitor version and revision number.

The display format and address map in which the EXORset initializes after the first power-on depends of the state of the jumpers SW18 (see CHAPTER 2, paragraph 2.5). With all SW18 jumpers left open (default condition), the EXORset initializes with 80 characters per line, 22 lines, upper case characters, white characters on black background, graphic mode off and address map 1.

Various characters can now be entered to check the character entry and display. Note that the EXORset is under EXORbus control, therefore no more than 19 characters can be entered on one line.

The user can now exercise all ESCAPE sequences, control commands, and special keys described in Table 3-1. Note that the ESC-O sequence can only be exercised when the EXORset is connected to a host computer via the RS-232C link.

When the graphic mode is switched on after the first power-on, the display shows the indeterminate (random) contents of the graphic memory. The graphic memory can be initialized by using the EXORbus "I" command :

```
.55;I
BEG ADDR XXXX 4000
END ADDR YYYY 7FFF
```

where 55 is the pattern to be written into the graphic memory (any other byte can also be chosen) and 4000, 7FFF are the lower and upper addresses of the graphic memory.

3.5.2 Disk Mini-Diagnostics

The disk driver E/ROM includes disk mini-diagnostic routines (described in CHAPTER 5, paragraph 5.3.4) and an interactive disk test program.

The following example illustrates how to invoke and use the interactive disk test program :

.EAD2;G	program entry point
DRV ? 0	enter drive number : 0 or 1
S/C ? S	enter S if the test is to be performed once (single test), enter C if the test is to be performed continuously.
DES ? N	enter N if the test should be non-destructive: read and check data CRC, all diskette, enter Y if the test should be destructive (present contents of the diskette will be lost) : write data pattern E5, then read and check for CRC, all diskette
En pppp tt ss	end of test message : n is the error message number (see CHAPTER 5, Table 5-15) pppp is the pass number (the number of times the test passes - 1) tt is the track nb at the end of the test ss is the sector nb +1 at the end of the test

An error-free, single test, should end with the message:

```
E0 0000 27 11
```

In the continuous mode, the program will only stop at the first error encountered (n not equal to 0).

3.5.3 Self-Test Package

A self test package allows the user to verify system performance, detect internal failures, and aid troubleshooting.

Of course, to run the self-test routines requires some parts of the E/ROM, RAM and a good portion of the processor itself be operating properly. Furthermore, if the diskette diagnostic is to be run, the system must be able to perform basic read/write operations. The disk driver resident interactive test (or the mini-diagnostic routines) may be used as a preliminary test.

3.5.3.1 System Requirements

The diagnostic is designed to run with the following minimum requirements :

- EXORbus system monitor
- The resident disk driver firmware (if the diskette is to be tested)
- RAM memory at locations 0000 through 00FF.
- The self-test programm (E/ROM or disk resident)

3.5.3.2 Test descriptions

The diagnostic can be E/ROM or disk resident. In the case of E/ROM resident test program, the operator enters the program by typing the EXORbus command nnnn;G. The self-test program is position-independent, therefore nnnn corresponds to the first location of the E/ROM socket used.

If the program is disk resident, it can be loaded and executed via the XDOS command SELFTEST. If the user wants to relocate the program prior execution, the XDOS command LOAD SELFTEST.CM should be used, followed by the EXORbus 'MV' (move) command. (Alternatively, the XDOS DUMP command can be used to alter the file's RIB).

Example :

```
=LOAD SELFTEST.CM
.MV
BEG xxxx 3000
END yyyy 37FF
DEST zzzz uuuu
.
```

where 3000 and 37FF are the beginning and ending addresses of the SELFTEST program after loading and uuuu the destination (relocation) address. To execute the program, enter the command : uuuu;G.

In response to the prompt (*), one of six followins tests may be run :

A. Memory CRC check

This test, based upon the cyclic redundancy check, permits to read and characterize the contents of a memory range by sivins a unique sisnature. One can determine if an E/ROM or a loaded program matches with a known sood one.

In response to the prompt, the operator must issue a "C" and then enter the startins and endins addresses of the memory ranse he wants to test.

Example :

```
*
C--CRC CHECK

BEG 1000
END 1FFF
CRC 2D4A

*
```

B. Memory diasnostic

This test permits to identify a bad RAM location. It is divided into three different tests :

- Walkins address test
- Bit pattern test
- Walkins bit test

The walkins address test stores the most sisnificant 8 bits of memory address in the even addressed byte and the least sisnificant 8 bits of memory address in the odd addressed byte. The walkins address test then verifies that all addresses are stored in the proper memory locations.

The bit pattern test stores a bit pattern into each memory location and then verifies the actual memory contents. The test is performed for each of the followins hex patterns: FF, AA, 55, 00.

The walkins bit test first clears all memory locations. One sinsle bit is then set and shifted throushout the memory. After each shift, the bit uniqueness is tested by readins all others bits (which should remain zero).

In response to the prompt, the operator must issue an "M" and then enter the startins and endins addresses of the memory ranse to be tested. If an error occurs durins the test, the wrons location address, the required correct value and the actual value are displayed.

Example :

```
*
M--RAM CHECK

BEG 1000
END 1FFF

 1-WALKING ADD TEST

 2-BIT PATT TEST (FF,AA,55,00)
10F0 FF 23
10F4 AA 18

 3-WALKING BIT TEST

*
```

C. Keyboard test

This test insures that all the keys transmit the correct ASCII code.
In response to the prompt, the operator must issue a "K". The ASCII characters are displayed on the console. The operator must enter the displayed set of characters in any order. They will be deleted as soon as a match occurs.

Example :

```
*
K--KEYBOARD CHECK

TYPE :ABCDEF
```

if the operator enters D, the following will be displayed on the same line :

```
TYPE :ABC EF

*
```

D. Diskette diagnostics

There are five tests which may be run on a selective basis or continuously.

CAUTION : REMOVE XDOS DISKETTE AND INSERT SCRATCH DISKETTE(S) INTO THE DRIVE(S) BEFORE EXECUTING DESTRUCTIVE TESTS !

D.1 Write/Read test (destructive)

Beginning with track #0, sector #1 of the selected drive, pseudo-random data is written/read one sector at a time until all the sectors have been tested. The same process applies to the alternate drive if it is selected. If a verify error occurs, the error message E@ followed by the drive, track and sector number will be displayed.

D.2 Read for CRC (non-destructive)

Starting with track #0, sector #1 of the selected drive, all the sectors are read for CRC only. If selected, the alternate drive will then be tested. If an error occurs, the drive, track and sector numbers are displayed.

D.3 Worse case track/sector access (non-destructive)

This test is used to insure track position reliability under worse case application. Beginning at track #0 sector #1, 10 sectors are read for CRC. Then the last 10 sectors of the last track are read for CRC. This process is repeated for the next 10 sectors in both directions, until all the sectors have been tested. The alternate drive is then checked if it

was selected.
10 sectors are read to insure track overflow. Any error will be displayed as drive, track and sector number .

D.4 Worse case data pattern (destructive)

Beginning with track #0, sector #1 of the first selected drive, all the sectors are written with a worse case bit pattern (4DB2). They are then read back to check their CRC. This is then repeated for the alternate drive if it was selected. Any error will be displayed as drive, track and sector number .

D.5 Sector/drive uniqueness (destructive)

Each contiguous sector is written with its own sector and drive unit number. The head is restored and each sector is read to insure uniqueness. The read partial sector is used to read 8 bytes only. If a uniqueness error occurs, it will display an EA followed by drive, track and sector number. If more than 8 bytes are read, the error code will be EB.

In response to the prompt, the operator issues a "D". The five possible tests are displayed, numbered from 1 to 5. The operator should first select the drive to be tested (0, 1 or Both). The operator must then answer the question "Do you want to run all the tests ?" with a Y or N. A "Y" answer will run all the tests, one after each other, continuously looping until the break key is depressed. An "N" answer permits the operator to choose a specific test by entering the corresponding test number. After its completion, another test may be chosen or control may be returned to another EXORset test.

Example :

```
*
D--DISK CHECK

 1-W/R TEST (DEST)
 2-READ FOR CRC (NON-DEST)
 3-WST CASE TK/ST ACCESS (NON-DEST)
 4-WST CASE DATA PATTERN (DEST)
 5-SCT DRIVE UNIQUENESS (DEST)

WHICH DRIVE (0,1,B) ? 0
ALL THE TESTS (Y/N) ? N

TEST # 1-W/R TEST (DEST)

ANOTHER TEST (Y/N) ? N

*
```

E. ACIA diagnostic

This diagnostic permits to check the send and receive functions of the ACIA. The only requirement is to connect the send and receive line together. The full ASCII character set is sent. After a character is sent, a check is done to verify that this character was correctly transmitted and received. If an error occurs, a message such as "TX-TIMEOUT", "RX-TIMEOUT", or the required correct character and the actual character are displayed.

To run the test, the operator must issue an "A" in response to the prompt.

Example :

```
*
A--ACIA CHECK

TX-TIMEOUT  if a transmit timeout occurs
RX-TIMEOUT  if a receive timeout occurs
3E 3D       if sent and received data do not match

*
```

F. CRT diagnostic

This diagnostic is a visual check of the alphanumeric, graphic, character generation, cursor positioning, background change, and 40 to 80 character toggle functions.
To run the test, the operator must issue a "V" in response to the prompt.Then the following sequence will be executed :

- A draughtboard-like pattern must fill the screen for about 5 seconds ('graphic on' test).
- A set of '#' characters must then be superimposed for about the same time ('graphic & alphanumeric on' test).
- The draughtboard-like pattern must disappear leaving the '#' pattern displayed alone for about 5 seconds ('alphanumeric on' test).
- The screen will be erased and the full printable ASCII character set must be displayed, the same character filling a full line. The ASCII character set will then be displayed with 40 characters per line and the background changed (80 to 40 characters toggle, character generator, background change test).
- Next, the cursor moves around the screen, the first time 80 columns horizontal and 22 lines vertical and next 40 columns horizontal and 16 lines vertical. The cursor should not blink during this test (cursor test).

At the end of the CRT check the prompt is issued and the cursor must blink again.

CHAPTER 4

EXORbus MONITOR

Information in this chapter is intended to familiarize the user of the EXORset with the various functions offered by the EXORbus monitor program. It provides detailed description of the commands, subroutines and entry points that are available to perform system development, evaluation and debugging.

4.1 EXORbus COMMANDS

In addition to the EXbus 2 compatible commands, the EXORbus monitor offers a new set of functions that greatly extend program development and debugging capability of the EXORset over existing systems.

There are five groups of commands :

1. Four-character commands followed by a carriage return
2. Two-character commands followed by a carriage return
3. Single character commands following a semicolon or dollar sign
4. Memory change commands
5. Control commands

The four-character commands allow a program to be saved or recovered to/from an audio cassette recorder, exchange programs with an EXORciser, invoke the disk operating system, display memory blocks, select the memory map, and switch to terminal mode. The user may add four-character commands to the standard set.

Two-character and single character commands control program debug functions, allow to move memory blocks within the EXORset memory and to insert ASCII character strings.

Memory change commands allow memory locations to be examined and changed.

Control commands are used to switch the EXORset from terminal to local mode (on-line/off-line) , erase the display, control cursor movements, to control the alphanumeric and graphic displays, select the display format (80/40 characters per line) and to abort or suspend command execution. A summary of EXORbus commands is found in Table 4-1.

Any command may be entered while EXORbus is displaying one of its prompts (. or :). The two prompts are used to

indicate to the user which is the currently selected memory map. A "." indicates first map, while a ":" indicates second map.

EXORbus accepts both upper and lower case characters. All values entered are assumed to be hexadecimal. If an invalid command or a non-hexadecimal value is entered, EXORbus responds by displaying WHAT ?, ringing the bell, and then issuing another prompt.

Control-X can be used at any time (at command level) to delete the current entry and cause another prompt to be displayed.

When entering hexadecimal values, only the last four digits are taken into account. If less than four digits are entered, leading zeroes are assumed.

Table 4-1 EXORbus Commands

COMMAND	FUNCTION	PAGE
PRNT	Display memory block in HEX & ASCII	04-04
PNCH	Dump memory block to audio cassette	04-05
LOAD	Load an oject tape from audio cassette	04-06
VERF	Verify an object tape against memory	04-07
DUMP	Dump memory block to EXORciser memory	04-08
DWLD	Download an EXORciser memory block	04-08
LINK	Download an EXORciser disk file	04-09
XDOS	Invoke the disk operating system	04-10
TMAP	Toggle memory map	04-10
XCOM	Switch to terminal mode	04-10
RA	Display/change target A accumulator	04-11
RB	" " B accumulator	04-11
RC	" " CC register	04-11
RD	" " D register (A,B accumulator pair).	04-11
RP	Display/change target Direct Page register.	04-12
RL	Display/change target Location counter (program counter).	04-12
RS	Display/change target Hardware Stack pointer.	04-12
RU	" " User stack pointer	04-12
RX	" " X index register	04-12
RY	" " Y index register	04-11
RR	Display all registers	04-11
SM	Select memory location for display trace function and breakpoints.	04-12
SP	Select display speed	04-14
MV	Move memory block	04-14
IS	Insert ASCII string to memory	04-14
EV	Extend breakpoints to WRITE condition	04-13
TC	Enable track change of memory location	04-13
DT	Disable track change of memory location	04-13

nnnn;G	Go to the target program at the specified address.	04-19
;G	Go to the target program through the user RESTART vector.	04-18
nn;I	Initialize memory block with the specified bit pattern.	04-22
;M or $M	Specify the memory search address range and mask.	04-21
nnnn;N	Trace nnnn instructions	04-20
;N	Trace one instruction	04-20
;P	Proceed with program execution	04-20
nnnn;P	Same as ;P but skip nnnn breakpoints	04-20
$T	Enable trace to ending address function	04-17
;T	Disable trace to ending address function	04-18
nnnn;V	Set breakpoint at address nnnn	04-15
;V or $V	Display breakpoints	04-17
nnnn;U	Remove breakpoint at address nnnn	04-17
;U	Remove all breakpoints	04-17
nnnn;W	Search memory for nnnn (1 or 2 bytes)	04-21
;Z	Line printer ON/OFF	04-23
nnnn/	Open location nnnn for memory change function and display contents.	04-23
followed by :		
[nn]LF	Open next memory location, display address & contents on next line.	04-23
[nn]SPACE	Open next memory location, display contents on same line.	04-23
[nn]COMMA	Open next memory location, no display	04-23
[nn]UA	Open previous memory location, display address & contents on next line.	04-24
[nn]SLASH	Reopen current memory location, display address & contents on next line.	04-24
'CHARACTER	Insert one ASCII character	04-23
nnnn;O	Calculate short relative offset to nnnn	04-24
nnnn;L	Calculate long relative offset to nnnn	04-24
[nn]CR	Terminate memory change function	04-23
CTRL-W	Suspend command execution	04-04
CTRL-X	Abort current command or entry	04-04
ESC-B	Display background change	04-26
ESC-C	Clear display from cursor	04-26
ESC-E	Erase screen	04-26
ESC-F	Display format toggle (40/80 characters)	04-25
ESC-G	Sound bell	04-26
ESC-H	Cursor to previous location	04-25
ESC-K	Kill line from cursor	04-26
ESC-L	Cursor home	04-26
ESC-N	Cursor to next location	04-26
ESC-O	Return to stand-alone mode of operation	04-26
ESC-S	Alphanumeric display ON	04-25
ESC-T	Alphanumeric display OFF	04-25
ESC-U	Cursor up one line	04-26
ESC-V	Cursor down one line	04-26
ESC-Y	Graphic display ON	04-25
ESC-Z	Graphic display OFF	04-25

Note : Brackets indicate optional entries

4.1.1 Four-Character Commands

The four-character commands are activated by entering the appropriate four characters followed by a carriage return (CR) on the system keyboard. The four-character commands are described as follows .

PRNT This command displays the specified portion of memory in both hexadecimal and ASCII form.

After the user has entered PRNT followed by a CR, EXORbug responds by displaying BEG nnnn. nnnn is the last beginning address entered. Note that nnnn is initialized to 0000 on system turn-on. If the displayed beginning address is correct, the user should enter a CR. To change the beginning address, the user has to enter the new address followed by a CR. (The command can be aborted at any time by entering a Control-X).

If an incorrect address is entered, the correct address may be entered directly on the same line before the CR is entered. Up to 19 hexadecimal characters can be entered before the CR. Only the last four characters will be used as the address.

If less than four hexadecimal characters have been entered, the unspecified most significant digits are assumed to be zero. For example, entering E CR gives an address of $000E.

After the beginning address has been successfully entered, EXORbug displays END nnnn (where nnnn is the current ending address). Here the user has the same options for entering an ending address as described for the beginning address.

If the entered ending address is less than the beginning address, EXORbug will request the beginning and ending address again. If the ending address is greater than or equal to the beginning addresses, EXORbug will display the requested portion of memory.

The display format depends on whether the EXORset is operating in 40 or 80 characters per line mode.

In 80 characters/line mode, the display format is the one shown in Figure 4-1. Every ten lines,a byte position header, showing the address of every byte within a line is displayed for better visualisation. In 40 characters/line mode, every line generated by PRNT is truncated and appears on

two consecutive display lines. In addition, no byte position header is generated.

While memory is being displayed, entering Control-W will cause the display to be suspended at the end of the current line until another character is entered. Entering Control-X will abort the PRNT command at the end of the current line.

```
.PRNT
BEG 0000 1000
END 0000 1050
     00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
1000 7E F2 AE 7E F0 45 7E F0 6F 7E F0 D5 7E F0 D9 7E  ~r.~pE~po~pU~pY~
1010 F0 88 7E F1 18 7E F2 2A 7E F0 B3 7E F0 AF 7E F0  p.~q.~r*~p3~p/~p
1020 AD 7E F0 3A 7E F0 2D 7E F0 2F 7E F0 B1 8D F2 A6  -~p:~p-~p/~p1.r&
1030 00 81 04 27 37 8D E1 08 20 F5 86 0D 8D DA 86 0A  ...'7.a. u...Z..
1040 8D D6 4F 20 D3 CE FB 99 8D E3 CE FF 0A BD F6 04  .VO SN{..cN..=v.
1050 25 F3 CE FB 9E 8D D6 CE FF 0C BD F6 04 25 F3 CE  %sN{..VN..=v.%sN
.
```

Figure 4-1 PRNT Example

PNCH This command dumps the specified portion of memory onto the audio cassette recorder that can be attached to the DIN connector of the EXORset. The ASCII hexadecimal tape format used by PNCH is described in Figure 4-3.

After the command has been entered, EXORbug requests the beginning and ending addresses as described under the PRNT command. After the beginning and ending addresses have been entered, EXORbug requests the information to be put in the header record. Zero through 17 characters, terminated by a CR, may be entered. If 18 characters, not including a carriage return, are entered, the characters will be ignored and the header information will be requested again. ASCII control characters should not be used in the header.

When the CR terminating the header information is entered, EXORbug will begin the dump sequence. Therefore the cassette recorder should be turned on after the last header character has been entered but before the CR terminating the header is entered. In addition, the user should wait at least 5 seconds from the beginning of the clear leader of the tape before entering the CR (to avoid errors due to splices at the beginning of the tape).

When EXORbus has completed the PNCH function it issues a prompt. At this point, the cassette recorder should be turned off. The data sent to the tape by the PNCH command is not displayed. Figure 4-2 shows an example of the PNCH command.

```
.PNCH
BEG 0000 F000
END 0000 F050
HDR=EXAMPLE4.2
.
```

Figure 4-2 PNCH Example

LOAD The LOAD command reads an ASCII hexadecimal tape from the audio cassette recorder. The required tape format is the one generated by the PNCH command and shown in Figure 4.3.

After the user has entered the command followed by a CR, EXORbus will start to load a single object file. The user should switch the cassette recorder to playback-on at this time.

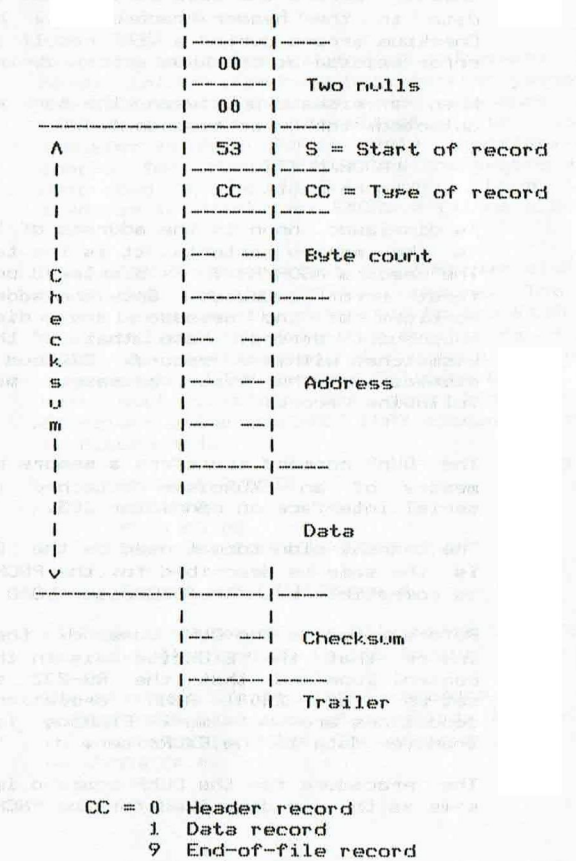
When EXORbus encounters the header record (S0), it will display the header information. It will then load the data held in the data records (S1). Loading will stop when an end-of-file record (S9) is encountered.

If a checksum error is encountered while loading, EXORbus will display CSKM ERROR nnnn (where nnnn is the starting load address of the record in error) and issue another prompt. If the error resides in the loading address itself, nnnn is of no meaning. The user can rewind the tape and start a new LOAD command. If the same error occurs again at the same loading address, it is due to an error on the tape.

As the LOAD command writes each data byte into memory, it reads it back to insure that memory has changed correctly. If memory does not change properly, the message :

```
ADDR/MM/TP
nnnn mm tt
```

will be displayed and the LOAD command is aborted. nnnn is the address of the memory location that did not change correctly. mm is the value that the memory location changed to. tt is the content of the tape for that location.



CC = 0 Header record
1 Data record
9 End-of-file record

The checksum is the one's complement of the summation of 8-bit bytes.

The number of nulls of the trailer is specified in location NULPAD ($E72D)

Figure 4-3 Tape Format

VERF The VERF command verifies the memory with an ASCII hexadecimal tape from the audio cassette recorder. The required tape format is the one described for the PNCH command and shown in Figure 4-3.

The VERF command checks for header record and

checksum errors the same as the LOAD command. The data in the header record will be displayed. Checksum errors during a VERF result in the same error message as checksum errors during a LOAD.

When a mismatch between the tape and memory is detected, the error message :

```
ADDR/MM/TT
nnnn mm tt
```

is displayed. nnnn is the address of the error. mm is the memory contents. tt is the tape contents. The heading ADDR/MM/TT is displayed only for the first error detected. Only the address and data portions of the message are displayed for subsequent errors. Note that if there are many mismatches within a record, EXORbus being busy displaying the error messages, may miss the following record.

DUMP The DUMP command transfers a memory block to the memory of an EXORciser attached to the RS-232 serial interface on connector J03.

The transmission format used by the DUMP command is the same as described for the PNCH command and is compatible with the EXORciser LOAD command.

Before entering the DUMP command, the user must insure that the EXORciser is in the main EXbug control loop and that the RS-232 interface is set-up for 2400 BAUD operation. If these conditions are not met, EXORbus is unable to transfer data to the EXORciser.

The procedure for the DUMP command is exactly the same as the one described for the PNCH command.

DWLD The DWLD command downloads an EXORciser memory-resident program to the EXORset memory.

The transfer is made via RS-232 serial interface (connector J03). As for the DUMP command, the EXORciser must be under EXbug control and the RS-232 interface operating at 2400 BAUD.

After entering the DWLD command, EXORbus sends automatically the PNCH command to the EXORciser. The EXORciser will then request the beginning and ending addresses, and the header information through the EXORset display and keyboard (the EXORset operating as terminal). For detailed procedure description refer to the corresponding EXORciser User's Guide.

Note that if the user makes an error causing the EXORciser to abort the PNCH command and issue its

prompt (*), the PNCH command has to be reinitialized manually.

Once the beginning and ending addresses, and the header information have been entered successfully, the EXORciser starts its punch sequence and the EXORset starts automatically to load the transferred data. During data transfer, EXORbus checks for checksum errors and memory errors as described for the LOAD command. Once the data transfer is completed, EXORbus issues a prompt.

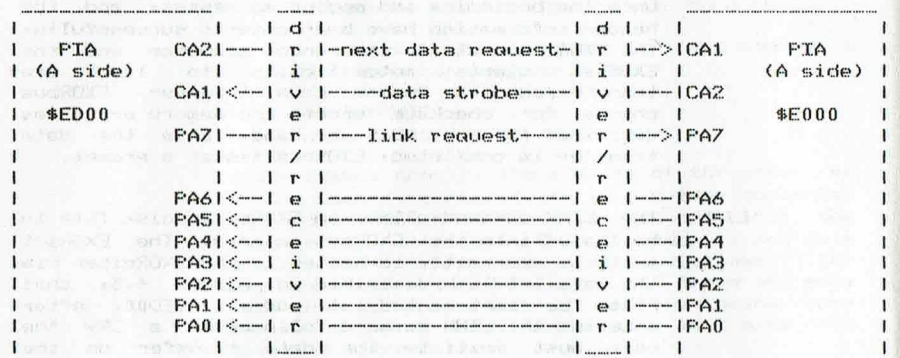
LINK The LINK command allows an EXORciser disk file to be loaded into the EXORset memory. The EXORset must be correctly connected to the EXORciser via the parallel link described in Figure 4.5, that must be implemented at address $ED00. After entering the LINK command followed by a CR, the user must initiate the data transfer on the EXORciser using the MDOS COPY command as described in Figure 4-4.

```
EXBUG 1.2 MAID
*E800;G
MDOS 03.00
=COPY FILE.SF:DV,#UD;D=LINK
```

Figure 4-4 LINK Example

FILE is the name of the file to be transferred. SF is its suffix and DV is its logical drive number.

The program LINK is used to perform the transfer on the EXORciser side of the link, and must reside in a file called LINK. The program LINK is listed in APPENDIX A.



Note : Line drivers/receivers are optional

Figure 4.5 Link Parallel Interface

XDOS The XDOS command is used to envoke the disk operating system.

The control is first transferred to the diskette controller which will initialize the drive electronics and then proceed to read the bootblock into memory. Once the bootblock is loaded, control is transferred to it. The bootblock will then attempt to load into memory the remainder of the resident operating system. If no error is detected (see the XDOS User's Guide for a description of error messages), XDOS will display a sign-on message and is ready for use.

TMAP This command allows to switch from one set of address decoding pattern to the other in the system address decoding PROMs.
The function of these PROMs as well as the available addressing maps are described in paragraph 5.2.4 of this manual. Note that with the original EXORset address decoding PROMs, the two memory pages in which the EXORbus monitor and its peripherals reside ($E000 through $FFFF) are not affected by the TMAP command.

XCOM The XCOM command switches the EXORset in the terminal mode of operation.

4.1.2 Two-Character Commands

The two-character commands are activated by entering the appropriate two characters followed by a CR. Two-character commands fall into three groups : register display and change, breakpoint control, and miscellaneous functions.

4.1.2.1 Register Display and Change

These commands allow the user to display and change the M6809 register values that are used while executing the program under test. There is one command that displays all the register values, while individual commands are used to display and change each register. In addition there is a command to select a memory location for display along with the microprocessor registers during breakpoints or trace operations.

RR This command displays all target registers as shown in Figure 4-6.

The mnemonics L, S, U, Y, X, DP, B, A, and C designate the location (program) counter, hardware stack pointer, user stack pointer, Y index register , X index register, direct page register, B accumulator, A accumulator, and condition code register, respectively.

RA This command displays the target A accumulator value (nn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RB This command displays the target B accumulator value (nn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RC This command displays the target condition code register value (nn) . The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RD This command displays the target D register (A,B accumulator pair) value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RL This command displays the target location counter value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RP This command displays the target direct page register value (nn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RS This command displays the target hardware stack pointer value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RU This command displays the target user stack pointer value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RX This command displays the target X index register value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RY This command displays the target Y index register value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

SM This command allows the user to select a single memory location for display along with the MPU registers during a breakpoint or trace operation.

After the user has entered the SM command, EXORbus displays the address of the memory location being currently selected for display. The default value is 0000. When the address is set to 0000, no memory location is selected. The memory location 0000 can therefore never be selected for display. The user may keep the address unchanged by entering a CR, or enter a new address followed by a CR. An example of SM command utilisation is shown in Figure 4-6.

4.1.2.2 Breakpoint Control

Set, remove and display breakpoints, are functions that are performed by single-character commands (see paragraph 4.1.3). The two-character commands allow the user to extend existing breakpoints to the WRITE condition, to track the

changes of one user defined memory location, and to disable the track change function.

EV This command allows all existing breakpoints to be extended to the WRITE condition. This means that a given breakpoint is active when, and only when, the MC6809 writes data at the corresponding address. This is the case during execution of instructions such as a STA nnnn, where nnnn is a breakpoint address.

On entering the EV command, EXORbus will display "Y/N ?" and wait for a user input. If a Y is entered the extended breakpoint function is enabled. If a N is entered, it is disabled.

TC This command enables the track change-of-memory-location function and to specify the address on which it should operate.

After the user has entered the TC command, EXORbus will display the last memory address that had been entered in a previous TC command (0000 if TC is called for the first time). If the displayed address is correct, the user enters a CR, otherwise it can be modified by entering a new value followed by a CR.

During execution of the target program, whenever the MC6809 references the selected memory location AND modifies its contents, EXORbus will display :

CELL nnnn JUST CHANGED TO mm

where nnnn is the selected memory address and mm is the new contents. The complete microprocessor status, after execution of the instruction that modified the selected memory location, will be displayed on the next line. Execution of the target program will be stopped and a prompt issued to allow the user to enter commands.

As long as the track change-of-memory-location function is enabled, eventual breakpoints are disabled.

During a trace sequence (be it a trace nnnn instructions or a trace to end address), the track change-of-memory-location is disabled.

DT The DT command disables the track change-of-memory-location function. Breakpoints that had eventually been set prior to the TC command, are enabled again. Note that if the TC command had been enabled at the same address than an existing breakpoint, the corresponding breakpoint will be removed by the DT command as it

would be removed by selecting a new address by a another TC command.

4.1.2.3 Miscellaneous Commands

These commands select display speed, move a memory block within the EXORset memory, insert ASCII character strings into memory.

SP This command displays the current delay value used for displaying characters on system CRT. The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

The delay value is initialized at system turn-on to 0000 (maximum speed), which corresponds approximately to 600 characters/second. A value of, for example, 300 will slow down the display to about 120 characters/second.

MV This command moves the content of the specified memory block to the specified destination.

After the user has entered the MV command, EXORbug requests beginning and ending addresses as described for the PRNT command. Once the beginning and ending addresses have been entered successfully, EXORbug will request the destination address by displaying DEST nnnn, where nnnn is the last destination address entered (initialized to 0000 at system turn-on). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR. The destination address cannot be in the beginning-ending address range. If this should be the case, EXORbug requests new beginning, ending, and destination addresses.

If an overlapping move has to be performed, the user should proceed in two steps : first move the memory block to some safe area, and then, move this area to the final destination. This procedure is mandatory to prevent data of being overwritten by the move before being moved.

As data is being moved, EXORbug checks that memory changes correctly. If an attempt is made to move data to a non-RAM or defective RAM area, EXORbug will display "NO CHNG" and abort the command.

IS This command allows ASCII character strings to be inserted directly from the system keyboard to the specified memory area.

After entering the IS command, EXORbug will request the beginning address at which the string should be inserted. The displayed address can be left unchanged by entering a CR, or modified by entering a new address followed by a CR.

All characters following the CR will be inserted in contiguous memory locations starting at the specified beginning address, until a Control-D (EOT) is entered. The EOT character (04) is the last one to be inserted. As every character is inserted into memory, EXORbug checks if memory changes correctly. If a memory location does not change properly, EXORbug will display "NO CHNG" and abort the command.

The ASCII character string that has been inserted using the IS command, being terminated by EOT, is ready to be displayed by the XPDATA or XPDAT1 subroutines (see paragraph 4.3).

4.1.3 Single-Character Commands

The single-character commands control debug functions. These commands are always preceded by a semicolon (;) or a dollar sign ($). Single-character commands fall into various groups : program execution control, program execution, memory search, and miscellaneous functions.

4.1.3.1 Program Execution Control

These commands control the execution of the target program. They allow the user to set, display, and remove breakpoints; enable or disable the Trace to Ending address mode.

Set a breakpoint

FORMAT : addr;V

This command permits the user to specify a breakpoint. A maximum of 4096 breakpoints can be entered. All breakpoints must reside in the same 4K memory page.

The hardware breakpoints concept of the EXORset, allows breakpoints to be set in RAM or ROM and on any byte of an instruction (even on a memory location referenced by an instruction).

During execution of the target program, the

breakpoints are activated. When a breakpoint is encountered, execution of the program is halted to permit visual check, or other performance analysis of the processor's program registers. The breakpoint sequence is :

- The user designates the breakpoint locations using the addr;V command. Since the breakpoints use interrupts (NMI), they should only be applied in portions of the target program where the stack pointer is pointing to a valid stack area. Should a breakpoint be encountered with the stack pointer (SP) pointing to a non-valid area, EXORbug will display the "BAD SP" message.

- The user initiates the target program execution through the use of the program execution commands (;G, addr;G, ;P, or nnnn;P). Note that breakpoints are not enabled during trace operations.

- When a breakpoint is encountered, control is returned to EXORbug and the processor registers as well as the optional memory location selected by the SM command are displayed as shown in Figure 4-6.

```
.100/00 86,33,B7,2,0,4C,20,102;0 FA
 0107  00 FA
.SM 0000 200
.102;V
.RR
L-0000 S-E6FF U-0000 Y-0000 X-0000 DP-00 B-00 A-00 C-D0
.100;G
L-0105 S-E6FF U-0000 Y-0000 X-0000 DP-00 B-00 A-33 C-D0 M-33
.2;P
L-0105 S-E6FF U-0000 Y-0000 X-0000 DP-00 B-00 A-35 C-D0 M-35
.
```

Figure 4-6 Breakpoint Example

NOTE

- When an abort occurs, the breakpoints are NOT removed. During a restart sequence, all breakpoints are removed.

- When a breakpoint is encountered, the processor normally returns control to EXORbug after execution of the instruction on which a breakpoint is set. However, if a breakpoint is set on the

first byte of an instruction preceded by an instruction that uses the look-ahead feature of the MC6809 (like most single byte instructions), control will be returned to EXORbug before execution of the instruction on which the breakpoint is set. The displayed location counter value should be checked to determine where user's program execution has been stopped.

Display the breakpoint addresses

FORMAT : ;V or $V

This command displays the addresses at which breakpoints are set. If no breakpoints have been set (or if they have been removed), EXORbug will display "NO BKPT".

Remove a specified breakpoint

FORMAT : addr;U

This command removes the breakpoint at address addr. If no breakpoint is set at the specified address, EXORbug displays "NO BKPT".

Remove all breakpoints

FORMAT : ;U

This command removes all the breakpoints. If no breakpoint is set, EXORbug displays "NO BKPT".

Specify and enable the trace-to-ending address

FORMAT : $T nnnn [addr] CR

This command enables the trace-to-ending address function, displays the current ending address (nnnn) and allows the user to change it. Once enabled , the trace-to-ending address is initiated by starting program execution with the ;P command. EXORbug will trace the target program, instruction by instruction, until the trace program counter is equal to the ending address. Therefore, the ending address should be set on the first byte of an instruction.

During the trace, entering Control-W will cause the trace to pause until some other character is entered. Entering Control-X will

abort the trace and return control to EXORbus.

Once enabled, the trace-to-ending address remains active until it is disabled or an abort or restart occurs.

Since the trace operation uses an NMI (and the stack), tracing should not be used unless the stack pointer is pointing to a valid stack area.

CWAI instructions cannot be traced because the trace NMI would cause the CWAI to continue and not wait for the user interrupt.

Disable the trace-to-ending address

FORMAT : ;T

This command disables the trace-to-ending address function.

4.1.3.2 Program Execution

These commands permit the user to execute the target program. The various program execution commands permit starting the target program through the restart vector or at a specified address, proceeding with program execution, and tracing one or more instructions.

Start the target program through the restart vector

FORMAT : ;G

This command starts the target program through the user restart vector. The restart vector is obtained from the user's top of memory specified at addresses $E72E and $E72F (see the start-up procedures section.) Therefore, when using ;G, the top of memory address should be set up appropriately otherwise EXORbus will display the "NO VECTORS" message.

This command cannot be used to initiate a trace-to-ending address function. If the trace-to-ending address mode is enabled when the command is entered, EXORbus will display WHAT ? ,sound the bell, and issue another prompt.

The values of the target registers are taken except for the direct page register which is cleared and the I and F masks in the condition code register which are set to emulate an effective restart sequence.

The user should ensure that the stack pointer is pointing to a valid stack area before any debug functions, such as breakpoints or track change of memory location, are encountered in the target program. This can be accomplished by specifying the stack pointer value using the RS command before the ;G command, or by executing an LDS instruction at the beginning of the target program.

Start the target program at a specified address

FORMAT : addr;G

This command starts the target program at the specified address. The processor registers will be loaded from the target registers which contain the last values obtained by EXORbus (during the last breakpoint or trace operation). The values of the target registers can be changed using the register change commands (see paragraph 4.1.2.1). During system turn-on, the target stack pointer is initialized to $E703, the target direct page register is cleared and the I and F masks in the target condition code register are set. All other target registers are cleared.

The user should ensure that the stack pointer is pointing to a valid stack area before any debug functions, such as breakpoints or track change of memory location, are encountered in the target program. This can be accomplished by specifying the stack pointer value using the RS command before entering the addr;G command, or by executing an LDS instruction at the beginning of the target program.

The addr;G command cannot be used to initiate a trace-to-ending address function. If the trace-to-ending address is enabled when this command is entered, EXORbus will display WHAT ?, sound the bell, and issue another prompt.

NOTE

- Some EXORbus routines make use of direct addressing with a direct page register value not equal to 00. Aborting may cause the target direct page register to be set to the EXORbus value. Therefore, if the user program uses direct addressing, it is a good practice to check the target register values before entering the addr;G command.

Proceed with target program execution

FORMAT : [value];P

This command resumes target program execution using the target register values. The value (if entered) specifies the number of breakpoint locations to be passed before a breakpoint returns control to EXORbus. Figure 4-6 shows an example of ;P command utilisation.

A pass value will not be accepted if no breakpoint is set and EXORbus will display "NO BKPT". If a pass value is entered and the track change of memory location is active, EXORbus will display WHAT ?, sound the bell, and issue another prompt.

The value;P command cannot be used to initiate a trace -to-ending address function. Even if the trace-to-ending address is enabled, entering value;P will not cause the target program to be traced.

However, the ;P command can be used to initiate a trace-to-ending address function if a pass value is not entered.

Breakpoints are not active during a trace-to-ending address function.

Trace the next instruction

FORMAT : [value];N

This command traces the next instruction(s). If a value is entered, it specifies the number of instructions to be traced. After each instruction is executed, the registers (and optional memory location) are displayed.

If multiple instructions are traced, entering Control-W will cause the trace to stop until some other character is entered. Entering Control-X will cause the trace to abort.

Since the trace function uses NMI, CWAI instructions should not be traced because CWAI instructions will not wait for the user interrupt, but will continue due to the NMI.

Because the trace NMI uses the stack, tracing should only be done in portions of the target program where the stack pointer is pointing to a valid stack area.

4.1.3.3 Memory Search

These commands control the memory search function. Commands are included to establish the search address range and comparison mask and to initialize the memory search.

Specify search address range and comparison mask

FORMAT : ;M or $M

This command first requests the search address range as described in the PRNT command. Memory will be searched from the beginning address specified through the ending address.

After a valid address range is entered, EXORbus requests the search comparison mask in the following manner :

MASK=nnnn [value] CR

nnnn is the hexadecimal representation of the current mask. If the current mask is correct, the user may enter a CR. Otherwise, a new value followed by a CR can be entered.

The search command (value;W) allowing searches of single or double bytes, the search mask has to be, respectively, a single or double byte.

The mask specifies which bits are to be checked against the search value. For example, a mask of $FFFF would compare each bit (during a double byte search), while a mask of $01 would compare only bit 0, the least significant bit (during a single byte search). All bit positions for which the search mask contains a 0 are don't cares.

Search for single or double byte

FORMAT : value;W

This command searches memory over the specified beginning-ending address range for a match with the value entered. The value entered, can be a single or double byte. Only those bit positions set to one in the last comparison mask entered, are compared during the search.

The same beginning and ending address parameters are used for the PRNT, PNCH, DUMP, IS, I, and the M commands. Therefore, if one of these commands is entered after the M command but before

the W command, the beginning and ending addresses specified for the last such command entered will be used as the search range.

If the value entered for the ;W command is a single byte and if the most significant half of the current mask is not 0, EXORbus will request a new mask to ensure that the user is willing to perform a double byte search. If the user does not modify the mask, a double byte search (where the least significant byte of the search value is the value entered and the most significant byte is 0) will be performed.

If the current mask has a value of 0000 (which means that all bits of the search value are don't cares), EXORbus will request a new mask.

When the memory search finds a match, the address of the match is displayed. Entering Control-W while the search is being performed, causes the search command to wait until some other character is entered. Entering Control-X, causes the search to abort and control to be returned to the EXORbus command level.

4.1.3.4 Miscellaneous

These commands allow the user to initialize memory with a specific bit pattern and to control the line printer operation.

Initialize memory to a specific bit pattern

FORMAT : byte;I

This command initializes random access memory to the specified byte value. After the command is entered, EXORbus requests the beginning and ending addresses of the memory region to be initialized. The beginning and ending addresses are entered as described in the PRNT command.

After valid beginning and ending addresses have been entered, the memory is initialized. The byte value entered is stored in each memory location, starting at the beginning address through the ending address.

As each memory location is initialized, EXORbus reads it back to ensure memory changes properly. Should a memory location not change correctly, EXORbus displays "NO CHNG" and aborts the ;I command.

Enable/disable copy of output to the line printer

FORMAT : ;Z nn [byte]

This command displays the status of the ZFLAG which controls the line printer interface. When the nn value (ZFLAG) is 0, the line printer is not activated and data is only displayed on the system CRT. The nn=0 status is a default condition following a power-up or restart. When the nn value is non-zero (1), the line printer is activated and the CRT output data is also sent to the line printer. The printer output is not paged, but continuous. To select output to the line printer, a "byte" value of 1 must be entered.

User program output, directed through the various EXORbus subroutines, will also be directed to the line printer if the ZFLAG has a value of 1. Note that the ZFLAG is kept in location $E729 and can be modified by program.

4.1.4 Memory Change

The Memory Change function permits the user to examine and change individual memory locations, and to calculate offsets for relative addressing mode instructions. To invoke the Memory Change function, the user enters :

addr/

After the user enters the slash, EXORbus displays a space followed by the contents of the specified memory location in hexadecimal, and then another space. If the contents are to be changed, the user enters a new value in hexadecimal, or an apostroph (') followed by a single character to insert an ASCII character. Next, the user enters one of the following terminators to close the current memory location :

Carriage Return -This ends the Memory Change function and returns control to the EXORbus command level. EXORbus prompts the user.

Line Feed -This causes the next sequential memory location to be opened for memory change. Its address and contents are displayed on the next display line.

Space -This causes the next sequential memory location to be opened for memory change. The contents of the opened location is displayed on the same display line.

Comma -This causes the next sequential memory

location to be opened for memory change. No display is performed.

Up Arrow -This causes the previous sequential memory location to be opened for memory change. Its address and contents are displayed on the next display line.

Slash -This causes the current memory location to be reopened for memory change. Its address and contents are displayed on the next display line.

If an attempt is made to change memory, but the memory does not change properly, EXORbus will issue the "NO CHNG" message, sound the bell, and prompt the user.

The Memory Change function can also be used to calculate the required offset for relative addressing instructions with the addr;O or addr;L commands. To calculate a relative offset, first open the memory location that is to contain the offset or the first byte of the offset in the case of a long branch. (e.g. the second byte of a branch instruction.) Next the destination address is entered, followed by a semicolon and the letter O for a short branch offset, letter L for a long branch offset.

The Memory Change function will indicate that the destination address is out of range by displaying "OUT OF RANGE". If the destination address is in range, the correct offset will be displayed. In both cases, the address and contents of the current location will be redisplayed on the next display line, permitting the user to easily modify it or request another offset calculation.

4.1.5 Control Commands

This paragraph describes the various control commands that can be entered from the system keyboard. All control commands are escape sequences and require two keystrokes. The format for an escape sequence, is the escape code (ESC key) followed by a valid escape character. The valid escape characters are listed in Table 4-1.

The required escape sequences can also be generated by a user program instead of being entered on the keyboard. The escape code ($1B) followed by the selected escape character can be sent to EXORbus via the XOUTCH, XPDATA and XPDAT1 subroutines described in paragraph 4.3.

The various control commands fall into three groups :

- Display control
- Screen control and cursor movements
- Miscellaneous

4.1.5.1 Display Control Commands

The commands in this group allow the user to switch the alphanumeric and graphic displays on and off, and to change the display format.

ESC S This command is used to enable the alphanumeric display. The display format and the alphanumeric display memory are not modified by this command.

ESC T This command disables the alphanumeric display. The screen image is not lost and can be visualized using the ESC S command.

However, all operations performed while the alphanumeric display is switched off will modify the display memory affecting the image obtained with the next ESC S command.

ESC Y This command is used to enable the graphic display. If the display format being currently selected is 80 characters/line, the ESC Y will switch automatically to 40 characters/line and erase the alphanumeric display.

Memory locations $4000 through $7FFF are used as graphic display memory.

ESC Z This command is used to disable the graphic display.

ESC F This command switches the display format. The two available display formats are : 80 characters/22 lines and 40 characters/16 lines.

The graphic display is operational only in the 40 character/line format. Therefore, when switching from 40 to 80 character format, the graphic display is disabled. In addition, the ESC F command erases the alphanumeric display and displays the header information.

4.1.5.2 Screen control and cursor movement commands

The commands in this group allow the whole or portions of the alphanumeric display to be erased and the cursor to be moved in any direction.

ESC H This command moves the alphanumeric display cursor one place to the left (back space).

ESC N This command moves the cursor to the next display location (to the right).

ESC U This command moves the cursor up one line.

ESC V This command moves the cursor down one line.

ESC L This command moves the cursor home (to the first position in the first display line).

ESC K This command kills a line from the current cursor position.

ESC C This command clears the display from the current cursor position.

ESC E This command erases the whole display and moves the cursor home.

4.1.5.3 Miscellaneous Commands

The commands in this group allow the user to switch back to the stand-alone mode of operation, sound the system bell and to invert the display background.

ESC O This command allows to return from the terminal mode of operation to the stand-alone (local) mode of operation.

Note that if a valid escape sequence is received from the serial link, it will be executed by EXORbug. This means that the EXORset can be switched from on-line to local mode of operation by the attached peripheral (i.e an EXORciser).

ESC G This command sounds the system bell.

ESC B This command is used to invert the display background. All visual characters displayed after the ESC B command has been entered, will be displayed with inverted background until another ESC B command is entered.

4.2 ADDING EXORbug COMMANDS

The user has the ability to add as many four character commands as desired. The only limiting factor is memory size. In order to implement this feature, the user must have a table of his commands and the actual commands stored in

memory, and must have told EXORbug where his command table resides. The user command table format must be as follows :

```
Example :  CTBEG  EQU *        Command table beginning
--------          FCC /CMD1/   Four character command
                  FDB CMD1E    Entry address of command
                  FCC /CMD2/   Four character command
                  FDB CMD2E    Entry address of command
                    .  .         .
                    .  .         .
                    .  .         .
                    .  .         .
                  FCC /CMDN/   Four character command
                  FDB CMDNE    Entry address of command
               CTBEND EQU *    Command table end
```

Once the user's command table is stored in memory, EXORbug must be informed of its location by having the beginning address of the table (the value of CTBEG in the above example) put at locations $E730 and $E731; while the ending address of the table (the value of CTBEND in the above example) is put at locations $E732 and $E733. In both of these cases, the addresses are loaded into memory in the order of most significant byte first followed by the least significant byte.

If the command table and commands are loaded from a tape, the tape may contain an object code that will properly initialize these locations. This object code may be generated by the ORG and FDB statments in the source program. For the above example, the source code required to generate the proper object code to initialize these locations would be :

```
Example : ORG $E730
          FDB CTBEG,CTBEND
```

Note that an ORG statment or END statment would be required after the two source lines shown above, so that the object code would not be produced at locations $E734 and beyond.

Pressing the ABORT button will not modify locations $E730 through $E733. However, pressing the RESTART button will cause these locations to be restored to the EXORbug values. These locations will also be restored to the EXORbug values when power is first applied. Thus, following a RESTART, the user must restore the beginning and ending addresses of his command table (if required) in memory locations $E730 through $E733. If the user does not wish to add commands, no operation is needed.

On entry to the user command, the stack pointer will be pointing at $E7F9 ; the X resister will contain the starting address of the user command routine; the other resisters are undefined.

4.3 EXORbus SUBROUTINES AND ENTRY POINTS

This paragraph lists and describes the various subroutines and entry points in EXORbus that are available to the user. Any user program running in the EXORset memory may call the described routines or entry points.

Table 4-2 lists the available routines with their corresponding entry addresses.

The first set of routines as well as their entry addresses are compatible with EXbus 1 and 2. Except as stated in the descriptions, all of these are subroutines, end with an RTS, and should only be called by BSR, LBSR, or JSR instructions. Control will be returned to the instruction after the calling BSR, LBSR or JSR, provided the stack pointer and stack memory area are correctly implemented.

Some routines that involve input from the keyboard (or audio tape) will wait (in a loop) until the character(s) is(are) input before returning to the calling program. Unless indicated otherwise, routines that output to the display are affected by the SP command and by the ↑Z command. That is, output through these routines will be slowed down if SP has not the default value (0000), and will be sent to the line printer, as well as the display, if the Z option is on. The SP value is held in memory locations $E736 and $E737, and can be modified by the user program. The same comment is valid for the ZFLAG at location $E729.

Table 4-2 EXORbus Routines

ENTRY ADDR	NAME	FUNCTION	PAGE
F000	PWRUP	ENTER EXORbus FROM RESTART	04-29
F003	XBEGEN	INPUT BEG & END ADDRESSES	04-29
F006	XCBCDH	CONVERT HEX TO BCD	04-29
F009	XCHEXL	CONVERT MS BCD TO HEX (ASCII)	04-30
F00C	XCHEXR	CONVERT LS BCD TO HEX (ASCII)	04-30
F00F	XINADD	INPUT HEX ADDR INDIRECT (X)	04-30
F012	XINCH	INPUT ONE CHARACTER	04-30
F015	XINCHN	INPUT ONE CHARACTER	04-31
F018	XOUTCH	OUTPUT ONE CHARACTER	04-31
F01B	XOUT2H	DISPLAY 2 HEX CHAR (X)	04-31
F01E	XOUT4H	DISPLAY 4 HEX CHAR (X)	04-31
F021	XPCRLF	DISPLAY CR,LF	04-32
F024	XPDATA	DISPLAY CR,LF,DATA STRING	04-32
F027	XPDAT1	DISPLAY DATA STRING	04-32
F02A	XPSPAC	DISPLAY SPACE	04-33
F02D	XORBUG	EXORbus ENTRY POINT	04-33
F030	XLDA	CROSS MAP LOAD	04-33
F033	XSTA	CROSS MAP STORE	04-33
F036	XTOGL	MAP SWITCHING	04-34
F039	ZAPBKP	REMOVE BREAKPOINTS	04-34
F03C	SAVREC	WRITE RECORD (AUDIO TAPE)	04-34
F03F	GETREC	GET RECORD (AUDIO TAPE)	04-35

F042 | PRINT | OUTPUT 1 CHAR TO LINE PRINTER | 04-35
F045 | CHKBK | CHECK FOR BREAK

Name: PWRUP - Power-up and restart entry

Function: Confisure EXORbus and its peripherals from a restart or power-up condition.

Call: JMP PWRUP

Output: EXORbus parameters are initialized alons with the EXORbus peripheral devices. The EXORbus start-up messase is displayed. Note that control is not returned to the callins prosram, but is siven to the EXORbus command input routine.

* * * * *

Name: XBEGEN -Input start and end addresses

Function: Requests input of besinnins and endins addresses as defined in the PRNT command. Verifies that inputs are hexadecimal characters. Verifies that the entered endins address is larser than the besinnins address.

Call: JSR XBEGEN or (BSR or LBSR)

Output: BEGA ($E71B/$E71C) 16 Bit Besinnins address
ENDA ($E71D/$E71E) 16 Bit Endins address
A, B, and X resisters are modified.

* * * * *

Name: XCBCDH - Convert an hexadecimal character to a binary number.

Function: Verifies that the input is a hexadecimal disit character. Converts the character in Acc A to a 4-bit binary number with hish order 4 bits equal to zero. Sets N (negative) condition code for non-hexadecimal characters.

Call: JSR XCBCDH

Input: Character to convert must be in Acc A

Output: If hexadecimal character input, Acc A contains the 4-bit binary number represented by the input character and the N condition code is cleared. If non-hexadecimal character input, Acc A contains the character input and the N condition code is set. The B, X and Y resisters are preserved.

* * * * *

Name: XCHEXL - Convert binary value to Hex

Function: Converts the most significant 4 bits of Acc A to an ASCII coded hexadecimal digit character.

Call: JSR XCHEXL

Input: Acc A contains the byte to be converted

Output: An ASCII coded hexadecimal digit character in ACC A. The B, X and Y registers are preserved.

* * * * *

Name: XCHEXR - Convert least significant binary value to Hex.

Function: Convert the least significant 4 bits of Acc A to an ASCII coded hexadecimal digit character.

Call: JSR XCHEXR

Input: Acc a contains the byte to be converted

Output: An ASCII coded hexadecimal digit character in ACC A. The B, X and Y registers are preserved.

* * * * *

Name: XINADD - Input an hexadecimal address.

Function: Convert up to 4 input hexadecimal characters to a 16-bit binary number.

Call: JSR XINADD

Input: X index register contains address where to store the result

Output: Most significant 8 bits of resultant 16-bit address will be stored into the memory location pointed at by the X index resister. The least significant bits will be stored into the next hisher memory location. Acc A will contain the last character input.Acc B will contain the number of input characters. X and Y index resisters are unchansed. The subroutine returns to the calling program when an invalid character, or the fifth hexadecimal digit is entered.

* * * * *

Name: XINCH - Input one character

Function: Wait for and accept input of one character from the system keyboard and echo character to the display if

required.

Call: JSR XINCH

Input: There is a "no echo" flag NECHO at address $E714. It must be set non-zero before each call to XINCH for each character that is not to be echoed to the display (and line printer if the Z option is on).

Output: Acc A contains the 8-bit input character as received from the system keyboard. XINCH clears NECHO if it was non-zero. The B, X and Y resisters are preserved.

* * * * *

Name: XINCHN - Same as XINCH

* * * * *

Name: XOUTCH - Output character

Function: Output one character with required speed fill.

Call: JSR XOUTCH

Input: Acc A contains the character to output to the system display (and to the line printer if the Z option is on).

Output: Acc A contains character output. The B, X and Y registers are unchansed.

* * * * *

Name: XOUT2H - Output two hexadecimal characters and a space

Function: Converts the contents of an 8-bit binary byte to two hexadecimal charcetrs and output them followed by a space character to the system display

Call: JSR XOUT2H

Input: X index resister contains the address of the byte to be converted and output.

Output: Acc A contains the last character output. The X index resister is incremented by one. The B and Y resisters are preserved.

* * * * *

Name: XOUT4H - Output 4 hexadecimal characters and a space.

Function: Convert the contents of two consecutive 8-bit binary bytes to four hexadecimal characters and output them followed by a space character to the system display.

Call: JSR XOUT4H

Input: X index register contains address of the first byte to be converted and output.

Output: Acc A contains the last character output. The X index register is incremented by two. Other registers are preserved.

* * * * *

Name: XPCRLF - Display CR/LF

Function: Output a carriage return and a line feed to the system display with required speed fill.

Call: JSR XPCRLF

Output: Acc A is modified. Other registers are preserved.

* * * * *

Name: XPDATA - Display CR/LF/Data string

Function: Output a carriage return, a line feed, and the user specified string of characters to the system display

Call: JSR XPDATA

Input: X index register will contain the starting address of user data string to output. Output string must be terminated by an EOT (04) character.

Output: X index register will contain the address of the EOT character. Acc A will contain the EOT character. Other registers are preserved.

* * * * *

Name: XPDAT1 - Display Data string

Function: Output a user specified string of characters.

Call: JSR XPDAT1

Input: X index register contains the starting address of the user data string to output. The output string is terminated by an EOT (04) character.

Output: X index register will contain the address of the EOT

character. Acc A will contain the EOT character. Other registers are preserved.

* * * * *

Name: XPSPAC - Display space

Function: Output a space character to the system display.

Call: JSR XPSPAC

Output: Acc A will contain the space character. Other registers are preserved.

* * * * *

Name: XORBUG - Reenter EXORbus

Function: Entry point for user programs to re-enter EXORbus.

Call: JMP XORBUG

Output: Control is not returned to the calling program.

* * * * *

Name: XLDA - Cross map load

Function: Loads the A accumulator with the data pointed at by the X index register. The data is fetched from the other memory map.

Call: JSR XLDA

Input: X index register is the data pointer

Output: A accumulator holds data. All other registers are preserved.

Caution: The system stack must be common to both maps.

* * * * *

Name: XSTA - Cross map store

Function: Stores the content of the A accumulator in the location pointed at by the X index register. The destination is in the other memory map.

Call: JSR XSTA

Input: A accumulator holds data to be stored

X index register is the data pointer

Caution: The system stack must be common to both maps.

* * * * *

Name: XTOGL - Memory map switching

Function: Switches from one memory map to the other.

Call: JSR XTOGL

Caution: The system stack must be common to both maps.

* * * * *

Name: ZAPBKP - Remove breakpoints

Function: Clears the breakpoint RAM and disables breakpoints.

Call: JSR ZAPBKP

Output: A, B, X, and Y registers are modified.

* * * * *

Name: SAVREC - Punch record

Function: Sends one record to the audio tape in the ASCII hexadecimal format shown in Figure 4.2. The record is preceded by 2 NULLS and is terminated by the number of NULLS specified in location NULPAD ($E72D).

Call: JSR SAVREC

Input: Location CASSET ($E72C) must be different than 0 (punch on).
Location TEMPA ($E710) must be 0 to indicate output to the audio tape.
B accumulator holds the record type (ASCII 0,1,9 or user defined code).
Location BCONT ($E74B) contains the byte count.
Locations BUF and BUF+1 ($E74C,$E74D) contain the address of the data to be punched.

Output: A, B, and X registers are modified

* * * * *

Name: GETREC - Get record

Function: Loads one record from the audio tape.

Call: JSR GETREC

Output: The data in the record is loaded at the specified address (see LOAD command for detailed description)

A, B, and X registers are modified.

* * * * *

Name: PRINT - Print one character on the line printer

Function: Outputs the character held in A accumulator to the line printer.

Call: JSR PRINT

Input: A accumulator holds the character to be printed.

Output: All registers exept Condition Code register are preserved.

If the printer is not selected or out of paper, then the Carry bit in the Condition Code register is set on return.

CHAPTER 5

THEORY OF OPERATION

5.1 INTRODUCTION

This chapter describes the operation of the EXORset Main Controller Board and Mini-Floppy Disk Controller Board. A simplified block diagram is presented in Figure 5-1.

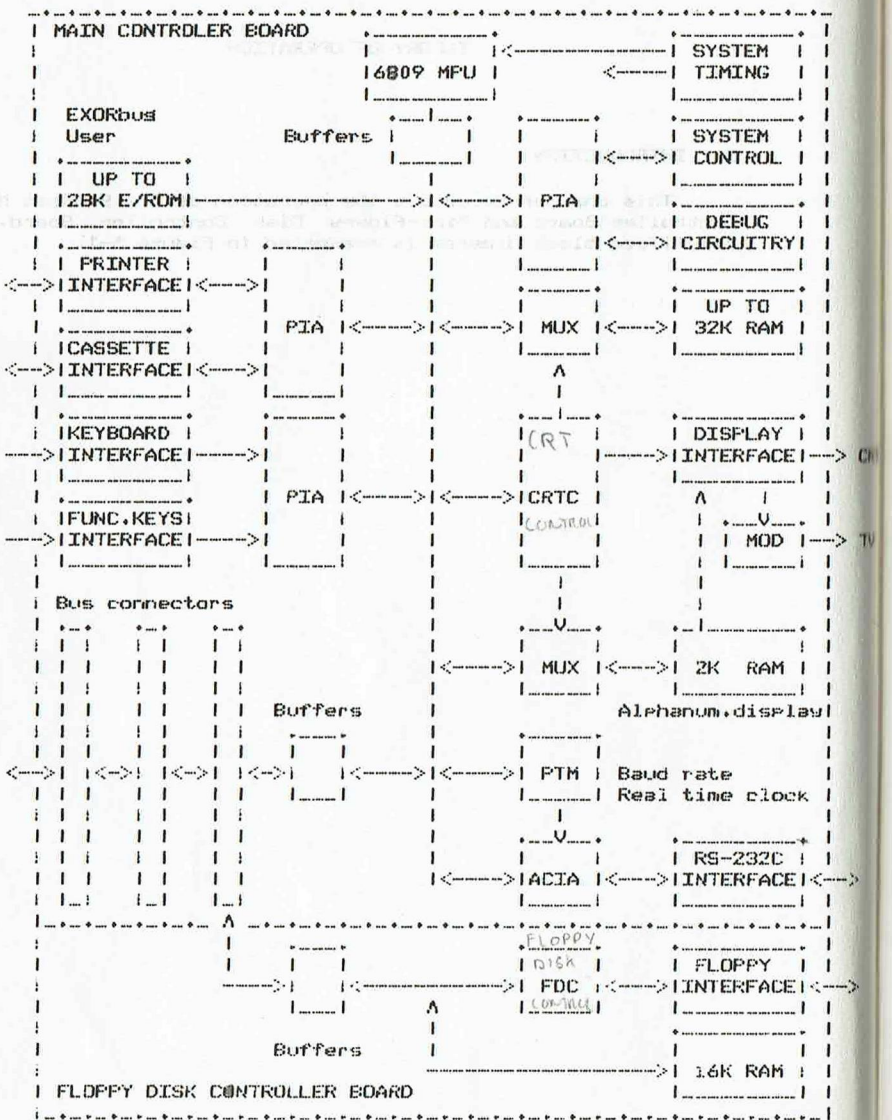


Figure 5-1 EXORset Block Diagram

5.2 MAIN CONTROLLER BOARD

5.2.1 System RESET

An MC1455 (U1) timing device, operated as a monostable multivibrator (one-shot) functions as a restart circuit that generates a low-level RESET signal (approximately 500 ms duration) after power is initially applied to the system. A valid RESET signal (one whose duration is > 8 MPU clock periods) causes the MPU to begin to execute an initialization routine. The RESET signal clears all registers in the PIAs to logic zero (low) so that the PIAs may be configured during system initialization. The RESET signal pre-sets the PTM latches and counters to their maximum count values, disables the counter clocks, clears the status register interrupt flags, and sets the control register internal reset bit which holds all timers in their pre-set state. The RESET signal also restarts the MC3870 Keyboard Encoder Microprocessor. In addition, a debounced RESET switch provides a system reset function. A separate power reset signal (PWRRES) is generated only when power is first applied to the system. This signal is not affected by the RESET switch. PWRRES is used to pre-set the upper case / lower case flip-flop (U104) and the cycles counter flip-flop (U94).

5.2.2 System Timings

One single clock generator generates all signals needed for the MPU, memories, I/O devices, CRT controller and display circuitry. The MPU clock is synchronized with the CRT controller character clock. This allows the use of the same RAM by the CRTC and the MPU in a multiplexed mode without contention (see Figure 5-1). The advantage of this method is that the CRT display refresh is completely transparent to the MPU. Furthermore, dynamic RAM refresh is inherently provided simply by the continuous reading of data by the CRTC.

The MC6809 MPU on-chip oscillator is used as the master clock for the system. A 4 MHz crystal is connected to the EXtal and Xtal inputs of the MPU. The MC6809 Eout (1 MHz) output feeds a phase-lock loop circuitry which generates a 16 MHz signal, the highest frequency of the timing chain. The timing circuitry provides the dot and CRTC clocks, the Row Address Strobe (RAS) and the Column Address Strobe (CAS) for the dynamic RAM, the latch enables, as well as the data bus buffers control signals used to multiplex the RAM access, MPUDR and CRTCDR.

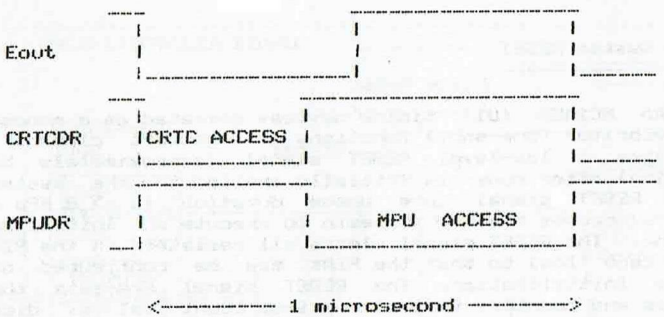


Figure 5-2 Multiplexed Memory Access

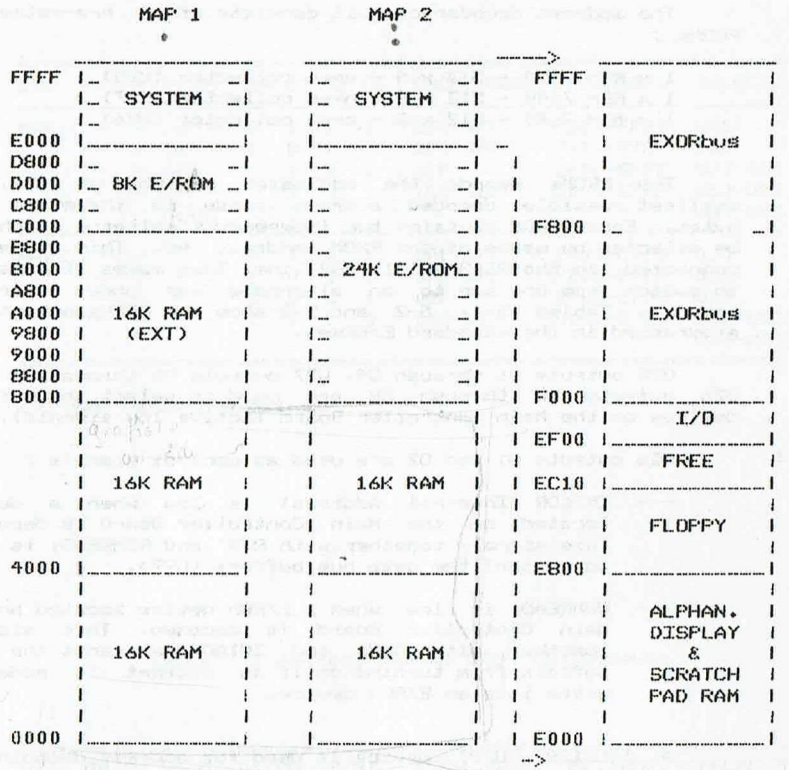
5.2.3 MPU and Bus Buffers

The MPU data lines are buffered, using a 74LS640 device (U88). The resulting inverted data bus is available at the Expansion Bus connectors for external boards. A second 74LS640 device (U97) provides the buffered true data bus for all internal devices. The INTADR' signal, generated by the address decoding circuitry, instructs the data bus buffers to turn on when a device located on the Main Controller Board is selected.

Three 74LS244 devices (U77, U90, U98) buffer the MPU address lines.

5.2.4 Address Map and Address Decoder Circuits

The EXORset Address Map is shown in Figure 5-3. The upper 8K address range is reserved for the system .



SYSTEM

Figure 5-3 EXORset Address Map

The address decoder circuit consists of 3 pre-patterned PROMs :

1 x MCM 7620 - 512 x 4 - open collector (U28)
1 x MCM 7640 - 512 x 8 - open collector (U27)
1 x MCM 7640 - 512 x 8 - open collector (U26)

The PROMs decode the addresses A8' through A15'. The smallest possible decoded address range is therefore 256 bytes. Each PROM contains two independent patterns which can be selected by means of the PROM address A8. This line is connected to the PIA3 (U101) PB0 line. This makes it possible to switch from one map to an alternate map under operator control. Tables 5-1, 5-2 and 5-3 show the PROMs outputs as programmed in the standard EXORset.

U28 outputs O1 through O4, U27 outputs O1 through O8 and U26 outputs O3 through O8 are used to select the various devices on the Main Controller Board (active low signals).

U26 outputs O1 and O2 are used as control signals :

- INTADR (Internal Address) is low when a device located on the Main Controller Board is decoded. This signal, together with R/W' and ROMREAD, is used to control the data bus buffers (U97).

- ROMREAD is low when a E/ROM device located on the Main Controller Board is decoded. This signal, together with R/W' and INTADR prevents the data buffers from turning on if an attempt is made to write into an E/ROM device.

A 74LS138 (U29) device is used for address decoding of the I/O devices. Each output decodes a 32 byte address range, from a base address defined by the PROM U28 O2 output. Each decoder output selects one I/O device, as shown in Table 5-4. The first address of each 32 bytes block is used as base address for the corresponding I/O device.

Table 5-1 Address Decode PROM U28 Outputs

U28	--	--	--	--	D4	O3	O2	O1	PROM ADDR.	DEC.ADDR.	SELECTS
MAP1	-	-	-	-	0	1	1	1	1F8-1FF	F800-FFFF	U30
	-	-	-	-	1	0	1	1	1F0-1F7	F000-F7FF	U31
	-	-	-	-	1	1	0	1	1EF	EF00-EFFF	U29 (*)
	-	-	-	-	1	1	1	0	1E0-1E7	E000-E7FF	U52-U53 U64-U65
MAP2	-	-	-	-	0	1	1	1	0F8-0FF	F800-FFFF	U30
	-	-	-	-	1	0	1	1	0F0-0F7	F000-F7FF	U31
	-	-	-	-	1	1	0	1	0EF	EF00-EFFF	U29
	-	-	-	-	1	1	1	0	0E0-0E7	E000-E7FF	U52-U53 U64-U65

(*) see Table 5-4 below

Table 5-2 Address Decode PROM U27 Outputs

U27	O8	O7	O6	O5	O4	O3	O2	O1	PROM ADDR.	DEC.ADDR.	SELECTS
MAP1	0	1	1	1	1	1	1	1	1D8-1DF	D800-DFFF	U32
	1	0	1	1	1	1	1	1	1D0-1D7	D000-D7FF	U33
	1	1	0	1	1	1	1	1	1C8-1CF	C800-CFFF	U23
	1	1	1	0	1	1	1	1	1C0-1C7	C000-C7FF	U22
MAP2	0	1	1	1	1	1	1	1	0D8-0DF	D800-DFFF	U32
	1	0	1	1	1	1	1	1	0D0-0D7	D000-D7FF	U33
	1	1	0	1	1	1	1	1	0C8-0CF	C800-CFFF	U23
	1	1	1	0	1	1	1	1	0C0-0C7	C000-C7FF	U22
	1	1	1	1	0	1	1	1	0B8-0BF	B800-BFFF	U21
	1	1	1	1	1	0	1	1	0B0-0B7	B000-B7FF	U20
	1	1	1	1	1	1	0	1	0A8-0AF	A800-AFFF	U19
	1	1	1	1	1	1	1	0	0A0-0A7	A000-A7FF	U17

Table 5-3 Address Decode PROM U26 Outputs

U26	O8	O7	O6	O5	O4	O3	O2	O1	PROM ADDR.	DEC.ADDR.	SELECTS
MAP1	1	1	1	1	1	1	0	0	1FO-1FF	FOOO-FFFF	
	1	1	1	1	1	1	1	0	1EF	EFOO-EFFF	
	1	1	1	1	1	1	0	0	1CO-1DF	COOO-DFFF	
	1	1	1	1	1	0	1	0	140-17F	4000-7FFF	U42-U49
	1	1	1	1	0	1	1	0	100-13F	0000-3FFF	U34-U41
MAP2	1	1	1	1	1	1	0	0	0FO-0FF	FOOO-FFFF	
	1	1	1	1	1	1	1	0	0EF	EFOO-EFFF	
	1	1	1	1	1	1	0	0	0A0-0DF	A000-DFFF	
	0	1	1	1	1	1	0	0	098-09F	9800-9FFF	U17
	1	0	1	1	1	1	0	0	090-097	9000-97FF	U16
	1	1	0	1	1	1	0	0	088-08F	8800-8FFF	U15
	1	1	1	0	1	1	0	0	080-087	8000-87FF	U14
	1	1	1	1	1	0	1	0	040-07F	4000-7FFF	U42-U49
	1	1	1	1	0	1	1	0	000-03F	0000-3FFF	U34-U41

Λ Λ
Λ INTADR
Λ
ROMREAD

Table 5-4 I/O Decoder U29 (74LS138) Outputs

U29	O7	O6	O5	O4	O3	O2	O1	O0	DEC.ADDR.	SELECTS DEVICE	
	1	1	1	1	1	1	1	1	EFE0-EFFF	not used	
	1	1	1	1	1	1	1	1	EFC0-EFDF	not used	
	1	1	0	1	1	1	1	1	EFA0-EF8F	PIA3	U101
	1	1	1	0	1	1	1	1	EF80-EF9F	PIA2	U107
	1	1	1	1	0	1	1	1	EF60-EF7F	PIA1	U11
	1	1	1	1	1	0	1	1	EF40-EF5F	ACIA	U6
	1	1	1	1	1	1	0	1	EF20-EF3F	PTM	U12
	1	1	1	1	1	1	1	0	EF00-EF1F	CRTC	U92

Note : the first address of the decoded address range is the base address of each I/O device.

5.2.5 RAM Section

Two blocks of 16K bytes of dynamic RAM using MCM4116 devices are included on the Main Controller Board : U34 through U41 (block 0) and U42 through U49 (block 1). The access of the memory is time- multiplexed between the CRTC and the MPU. Table 5-5 shows the addresses generated by the CRTC and the MPU during each portion of one MPU cycle.

Table 5-5 Multiplexed RAM Addresses

ADDRESSES FROM MPU		FROM CRTC		TO RAM
A13'....		MA9	]	
A12'....		MA8	]	
A11'....		MA7	]	COLUMN
A10'....		MA6	]	
A9'		RA3	]	
A8'		RA2	)	
A7'		RA1	)	ROW
A6'		RA0	)	
A5'		MA5	]	COLUMN
A4'		MA4	)	
A3'		MA3	)	ROW
A2'		MA2	)	
A1'		MA1	)	
A0'		MA0	]	COLUMN

The CRTC generates the memory row address and is therefore used as an inherent refresh counter. All of the 128 rows of each memory device are refreshed within 512 microseconds. The CRTC also generates the RAM column address, providing the graphic capability (see paragraph 5.2.7.3).

5.2.6 E/ROM Section

The EXORset Main Controller Board provides sockets for up to 28K bytes of E/ROM devices. Each socket (U30 through U33 and U14 through U23) accepts 2K x 8 E/ROM devices (MCM2716 single supply EROM or MCM68A316E mask-programmable ROM). Sockets U30 and U31 are normally reserved for the EXORbug monitor. 4K x 8 E/ROM devices (2732 EROM or MCM68A332 ROM) may alternatively be inserted in sockets U14, U16, U18, U20, U22, U33, U31 providing the jumper(s) between pin(s) 18 and 20 is

(are) cut and address line A11' is connected to pin(s) 18. The artwork wiring has provision for the necessary modifications (see paragraph 2.5). The address decode PROM(s) should be reprogrammed to generate chip selects in 4K increments.

5.2.7 Display Section

5.2.7.1 General Description

The display section consists of the MC6845 CRT Controller, the alphanumeric display and scratchpad RAM, the synchronization logic, the alphanumeric and graphic shift registers, the video mixer and the optional UHF modulator.

The 2K-byte alphanumeric display RAM uses 4 x MCM2114 1K x 4 static RAM devices. 1760 bytes (80 characters x 22 lines) are actually used as display memory, leaving 288 bytes free for the system scratchpad. Table 5-6 and Table 5-7 describe the display format and the corresponding CRTC register contents, respectively.

Table 5-6 Alphanumeric Display Format

	50 Hz		60 Hz	
	40 char./line	80 char./line	40 char./line	80 char./line
a.	16	12		
b.	16	22		
c.	256	264		
d.	47	44		
e.	303	308		
f.	50 Hz	50 Hz		
g.	15150 Hz	15400 Hz		
h.	64 (*)	80		
i.	2	50		
j.	66	130		
k.	1 MHz	2 MHz		
l.	8	8		
m.	8 MHz	16 MHz		
n.	4 MHz	8 MHz		

(*) 40 visible, characters 40 to 63 blanked by software

	CRTC REGISTERS :
a. Lines per block	[R9] + 1
b. Total blocks	[R6]
c. Total active lines (a x b)	
d. Vertical blanking in nb of scan lines	((([R4]+1)-[R6])x([R9]+1)+[R5]
e. Active plus blanking lines (c + d)	
f. Vertical refresh	
g. Horiz. frequency (e x f)	
h. Characters per line	[R1]
i. Horiz. retrace in character time	
j. Total characters per line (h + i)	
k. Characters frequency (g x j)	
l. Dots per character	
m. Dot shift frequency	
n. Video frequency	

Table 5-7 CRTC Resisters Values (Hex)

	50 Hz		60 Hz	
	40 char./line	80 char./line	40 char./line	80 char./line
R0	41	81		
R1	40	50		
R2	34	63		
R3	06	0B		
R4	11	1B		
R5	0F	0B		
R6	10	16		
R7	10	16		
R8	00	00		
R9	0F	0B		
R10	4A	4A		
R11	0B	0A		
R12	00	00		
R13	00	00		
R14	00	00		
R15	00	00		

5.2.7.2 Alphanumeric Display

At the display data rate needed to display 80 characters per line, two characters must be removed from the display memory at each MPU cycle. The display memory is split into two blocks, an "odd" block and an "even" block, and interleaved to appear as an array of 2K x 8 bits to the MPU and 1K of 16 bits to the CRTC. The MPU and the CRTC access the display RAM in a multiplexed mode, as shown in Table 5-8.

Table 5-8 Multiplexed Alphanumeric Display RAM Addresses

ADDRESSES FROM MPU		FROM CRTC	TO RAM
A10'	....	MA10	A10"
A9'	....	MA9	A9"
A8'	....	MA8	A8"
A7'	....	MA7	A7"
A6'	....	MA6	A6"
A5'	....	MA5	A5'
A4'	....	MA4	A4'
A3'	....	MA3	A3'
A2'	....	MA2	A2'
A1'	....	MA1	A1'

The MPU address line A0 is not used as part of the alphanumeric memory address, but rather is used to gate the chip select into either the even or odd bank of the array. If address line A0 is low, it will select the even bank of memory, when high it will select the odd bank of memory. Two 74LS640's (U50, U62) form a bidirectional bus switch for the data lines. The R/W' line controls the direction of the data transfer. Two 74LS374 (U63, U51) 8-bit latches latch the 16-bit data flowing to the CRT. The output of these latches is three-state and is controlled by the CRTC MA0 line, delayed by one character (=MA0SYNC).

All the timing is derived from the central oscillator. The frequency of this oscillator is at the dot clock rate and is determined by the system parameters. This clock is 16 MHz for a 80 character per line display and 8 MHz for a 40 character per line display. The one or the other clock signal is selected by means of the 74LS157 (U71) multiplexer, controlled by the PIA3 (U101) PB1 line.

Table 5-9 and Table 5-10 show the relationship between the character position on the screen and its actual address in the alphanumeric RAM (offset from the alphanumeric RAM base address). In the standard EXORset the alphanumeric display RAM base address is E000.

Table 5-9 Alphanumeric Display Characters Location
(hex offset from alphanumeric RAM base address)
40 characters/line by 16 lines format

	COL1	COL2	COL3	.....	COL40	COL50	COL64
ROW1	00	01	02	.....	27	28 ...	3F
ROW2	40	41	42	.....	67	68 ...	7F
ROW3	80	81	82	.....	A7	AB ...	BF
.	.	.	.		.	.	.
.	.	.	.		.	.	.
.	.	.	.		.	.	.
.	.	.	.		.	.	.
.	.	.	.		.	.	.
ROW16	3C0	3C1	3C2	.....	3E7	3EB ...	3FF

<------- DISPLAYED CHARACTERS -------> <-BLANKED->

Table 5-10 Alphanumeric Display Characters Location
(hex offset from alphanumeric RAM base address)
80 characters/line by 22 lines format

	COL1	COL2	COL3	.....	COL80
ROW1	00	01	02	.....	4F
ROW2	50	51	52	.....	9F
ROW3	A0	A1	A2	.....	EF
.	.	.	.		.
.	.	.	.		.
.	.	.	.		.
.	.	.	.		.
.	.	.	.		.
ROW22	690	691	692	.....	6DF

<---------- DISPLAYED CHARACTERS ---------->

5.2.7.3 Graphic Display

The EXORset provides a high resolution full graphic capability, in a raster of 320 dots (40 bytes) by 256 scans.

The CRTC accesses the dynamic RAM cyclically, once per MPU cycle. The RAS signal is generated at each cycle, allowing the dynamic memory refresh to be performed. If a CAS signal is also applied to one of the 16K RAM block, the contents of this RAM block will appear on the data outputs. These data are loaded from the inverted data bus into the 74LS165 (U74) shift register. Provided the graphic function is enabled (PIA3 (U101) PB3 line low), the 8-bit word will be shifted out to the CRT, one memory bit controlling one dot in the graphic matrix. Table 5-11 shows the matrix coordinates and the corresponding byte addresses in the graphic memory.

Note that bytes 40 to 63 (columns 321 to 512) are not displayed and must be filled with blanks (zeroes) by software.

Table 5-11 Graphic Display Matrix
(hex offset from the graphic RAM base address)

	COL1 ... COL8	COL9 ... COL17	.....	COL312 . COL320
	[BIT7 ... BIT0]	[BIT7 ... BIT0]	.....	[BIT7 ... BIT0]
ROW1	00	01	.....	27
ROW2	40	41	.....	67
ROW3	80	81	.....	A7
ROW4	C0	C1	.....	E7
.	.	.		.
.	.	.		.
.	.	.		.
.	.	.		.
.	.	.		.
ROW256	3FC0	3FC1	.....	3FE7

5.2.7.4 Video Mixer

The video mixer combines the horizontal sync, vertical sync, and video data. The video data includes the character data, the row and retrace blanking. The video mixer also combines the graphic and alphanumeric data. If both functions are selected together, the graphic output signal is automatically switched to half-intensity, to make the text easily distinguishable from the graphic pattern.

5.2.7.5 UHF Modulator

The optional UHF modulator UM1231 (U9) allows the use of a standard TV as display unit (channel E36, 591.25 MHz). The UM1231 features a switchable positive or negative modulation, to adapt to different TV standards. Jumper SW1 (see Table 2-13) selects the desired modulation polarity.

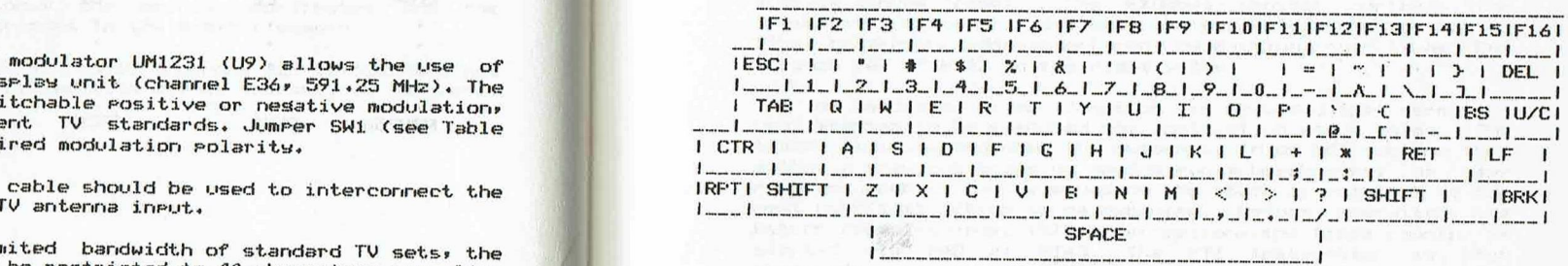
A 75 ohm TV coax cable should be used to interconnect the UHF modulator to the TV antenna input.

Due to the limited bandwidth of standard TV sets, the display format should be restricted to 40 characters per line for acceptable readability.

The UHF modulator specifications are listed in paragraph 1.3.4.

5.2.8 Keyboard and Keyboard Interface

Figure 5-4 shows the keyboard matrix organization. Refer to Table 2-4 and Table 2-5 for pin assignments.



ROW - COLUMN :

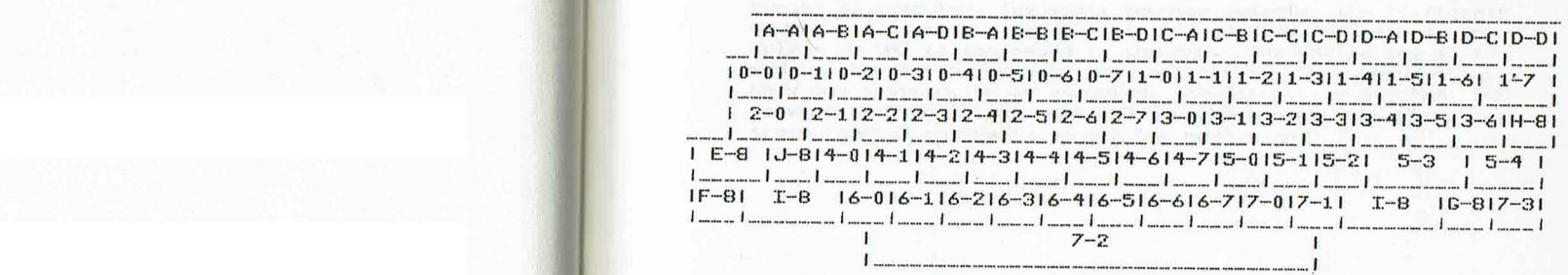


Figure 5-4 Keyboard Matrix Organization

The SC80241P Keyboard Encoder is a pre-programmed MC3870 microprocessor, used to scan a 64 key keyboard. The keyboard is scanned by a 74LS156 open collector 1 of 8 decoder (U105) driven by 3 bits of port 0. The closed keys in the 8 x 8 array are input to port 1, and are debounced and encoded by software. The ASCII code is available at port 4, along with an active low STROBE pulse. The output from port 4 can be restrained if the READY line is held low. An 8-bit FIFO buffers the output until the READY line returns to a high level. In the EXORset, READY is always held high, but PIA2 (U107) PB7 can be used to implement this function, if desired.

5.2.9 Debug Circuitry

The debug circuitry consists basically of the PIA3 (U101) (A-side), the address comparator (U100), the 4K x 1 MCM66L41 breakpoint memory (U78) and the run-one-instruction counter (U102).

The basic idea of the breakpoint circuitry is to provide a ninth bit in parallel with the system memory. A breakpoint is set by writing a zero into the desired memory location of the breakpoint RAM. When the breakpoint address is encountered during user program execution, the breakpoint RAM outputs a zero, which in turn generates an NMI to the processor. Up to 4K breakpoints may be inserted in a 4K address window (page). The EXORbug monitor controls the breakpoint circuitry and sets the page corresponding to the first breakpoint address entered, by setting the lines PA4 through PA7 of PIA3 to the right value.

A hardware trace function is provided that permits a user program to be executed one instruction at a time. The trace is initiated when the system is in an NMI routine from either a previous trace or having run a breakpoint. The user program counter value saved on the stack is pointing to the next user instruction to be executed. Before executing the Return from Interrupt (RTI) instruction, the trace counter is started via PA3 of PIA3. The RTI instruction is then executed, causing the MPU to reload its registers from the stack and begin executing the next user instruction. In the mean time the trace counter is counting machine cycles. The sixteenth cycle after the counter is started will be a fetch of the op-code for the next user instruction (RTI takes 15 cycles to execute). The trace counter detects the fifteenth count and generates a pulse to CA2 of PIA3. After one cycle delay, an NMI is generated to the MPU. The NMI is low at the end of the first cycle of the instruction. This insures that only one instruction is executed. The first task of the NMI service routine is to set PA3 line back high, resetting the trace counter in readiness for the next step.

5.2.10 Serial Interface

The ACIA and line drivers and receivers provide an RS-232C compatible serial I/O interface. Data may be transferred at rates of 110 to 2400 baud. The MC6840 PTM (Programmable Timer Module) timer #3 is used to establish the required baud rate. Table 5-12 shows the hex equivalents of some standard baud rates to be written into PTM timer #3.

Table 5-12 PTM Timer #3 Hex Equivalent of Baud Rate

BAUD RATE	HEX VALUE
110 BAUD	011B
300 BAUD	0067
1200 BAUD	0019
2400 BAUD	000C

5.2.11 Parallel Interface

The parallel interface using the PIA1 (U11) provides the interface between the EXORset and 700 series line printers. The MEX68PIC Printer Interconnect Cable is needed for the transition between the EXORset 50-pin card-edge connector and the 36-pin printer connector.

Data on the PIA1 peripheral interface lines PA0 through PA7 is output through the drivers and appears at connector J04 as PD (Peripheral Data)1 through PD8. This data is clocked by the DATA STROBE active low output pulse from the PIA1 CA2 line. ACKNLG (Acknowledge) is a low-level signal from the printer to the PIA1 CA1 line indicating that a character has been received. Status signals from the printer are received on PB0, PB1, PB2, CB1 and CB2.

5.2.12 Audio Tape Interface

Circuitry for interfacing an audio cassette recorder/player is included on the EXORset Main Controller Board. This circuitry enables the user to store and retrieve data on ordinary audio cassettes at an average of 1333 baud (1333 bits per second).

The audio signal is generated by software (routines are included in the EXORbug monitor). A logical 1 is represented by a one period, 50 % duty cycle, square wave signal, 1 millisecond duration. A logical 0 is represented by a one period, 50 % duty cycle, square wave signal, 500 microseconds duration. The playback signal from the audio tape is recovered using MC3302 comparators (U8). Since some audio tape cassette recorders invert the recorded signal, care should be taken to recover the proper phase . Jumpers SW24 provide for this selection.

5.3 MINI-FLOPPY DISK CONTROLLER BOARD

5.3.1 Introduction

The Mini-Floppy Disk Controller Board consists of a MC6843 Floppy Disk Controller (FDC), a 1024 x 8-bit E/ROM containing the resident driver firmware program, a drive select circuitry, three-state bus interface circuitry, and the necessary address decoding logic to permit accessing from the EXORset bus.

The Mini-Floppy Disk Controller Module occupies 1040 address locations, divided as follows :

--- E800 through EBFF are assigned to the Resident Driver Firmware

--- EC00 through EC07 are assigned to the MC6843 FDC

--- EC08 through EC0F are assigned to the drive select latches

5.3.2 FDC and Data Recovery

The MC6843 FDC (Floppy Disk Controller) (U21) performs all read / write and control operations needed to transfer data to / from the mini-disk drives. Refer to the FDC data sheet for a detailed description of the FDC operation.

A phase locked loop data recovery circuit is used to provide the separated data and clocks needed by the FDC. The PLL data recovery circuit consists of a frequency / phase detector circuit (U15) with filter network, a voltage controlled oscillator (U26), two synchronous 4-bit counters (U2, U16), and five flip-flops (U17, U27, U28). Gate U1 is inserted in the loop only for test purposes. The center frequency of the VCO is normally 4.0 MHz with a lock range of 3.8 to 4.2 MHz. Lockup time will be less than 384 microseconds.

The Raw Data signal from the disk drive unit is a combination of a 250 KHz clock signal and data. This signal is applied to an input flip-flop circuit consisting of two serially connected flip-flops (U17). This circuit generates a negative output pulse with a pulse width equal to one VCO time period (approximately 0.250 microseconds). This negative pulse is used to preset the first reference counter (U16) with a 9 and to set the output of the first data flip-flop to a logic high level.

In the data format used in the disk system, the incoming data stream can have only one consecutive pulse missing. By loading the first reference counter with a 9, it will produce a positive output transition within 15 VCO pulses (3.750 microseconds), thus generating a clock edge even if the data

pulse is missing. This reference counter will also produce a carryout pulse on the 16th VCO pulse (4 microseconds). This pulse is then compared with the carryout output of the second reference counter (U2) by the frequency / phase detector, thus providing a reference for the VCO.

The negative output transitions of the first reference counter are inverted and used to clock the first data flip-flop (U27), causing the output to change to a logic low level. If another data pulse is present in the incoming data stream, then the first data flip-flop is once again set by the input flip-flop circuit. However, if no data is present, then the output of the first data flip-flop will remain at a logic low level until set by a data pulse, which must occur within 64 microseconds of the last data pulse in order to avoid initiating an error message. When the data pulse is set and the first data flip-flop is set, the next output pulse produced by the reference counter causes the second data flip-flop to toggle, producing the NRZ (Non-Return to Zero) data (RDT) required by the FDC.

5.3.3 16K RAM Block

One block of 16K bytes of dynamic RAM using MCM4116 devices is implemented on the Mini-Floppy Disk Controller Board (U7 through U14). The CRTC is used as an inherent refresh counter for the dynamic RAM located on the Main Controller Board (see paragraph 5.2.5). The RAS' (Row Address Strobe), CAS' (Column Address Strobe) and EAHL (high / low address latch) signals are generated on the Main Controller Board and are available for the Mini-Floppy Disk Controller Board through the EXORset expansion bus (pins Cnot, Dnot, Enot respectively).

5.3.4 Mini-Floppy Drives Selection Circuitry

Data bits D0' through D4' are latched into two addressable latches (U20, U29) responding to address EC08 (ambiguous addresses up to EC0F). These five bits are used to select the mini-disk drives and control the drive motors. Table 5-13 shows the function of each bit.

Table 5-13 Mini-Floppy Drives Select Lines

D4'	D3' (1)	D2'	D1'	D0'	FUNCTION
0	X	1	0	0	Drive 0 selected
0	X	1	0	1	Drive 1 selected
0	X	1	1	0	Drive 2 selected (not used)
0	X	1	1	1	Drive 3 selected (not used)
0	X	0	X	X	All drives desselected
1	X	0	X	X	Drive motors off

X = don't care
(1) provision for double-sided diskettes - not used

5.3.5 E/ROM Resident Driver Firmware

The Resident Driver Firmware stored in the E/ROM device is used to control all of the Mini-Floppy Disk System hardware operations.

5.3.5.1 Initialization

When the Mini-Floppy Disk System is initially accessed by the user, a defined initialization procedure must be used. When the Mini-Floppy Disk System is used with XDOS, this initialization procedure is automatically performed when the command XDOS is entered by the user. However, if the Mini-Floppy Disk System is used in conjunction with a user desisned system, the user must include this initialization procedure in his program. Parameters for the initialization procedure are stored in nine sequential bytes, as described in Table 5-14.

5.3.5.2 Error Messages

The ninth byte (FDSTAT) of the initialization procedure contains a hexadecimal error message (from 30 to 39). If no error occurred during the disk operation, then the carry bit will be reset and the FDSTAT byte will contain the hexadecimal number 30 (ASCII 0) : no error. However, if an error does occur, then the carry bit will be set and the FDSTAT byte will contain a hexadecimal number of 31 to 39 (ASCII 1 to 9) that relates to a specific error message. If an error occurs, any disk operation in progress is halted, and control is returned to the user. Each of the error messages (and their corresponding hexadecimal and ASCII characters) is explained in Table 5-15.

Table 5-14 Initialization Parameters for a User Prepared DOS Program

BYTE	NAME	DEFINITION
0	CURDRV	CURRENT DRIVE - This byte contains the number of the selected drive unit (0 or 1).
1,2	STRSCT	STARTING SECTOR - These two bytes contain the physical sector number of the first sector to be used (starting sector). For single density mini-disks, this starting sector number must be between 0 and 27F (hex), inclusive.
3,4	NUMSCT	NUMBER OF SECTORS - These two bytes contain the number of sectors to be used. This number includes a partial sector read, if one is requested. For single density mini-disks, the sum of the numbers contained in the STRSCT byte and the NUMSCT byte cannot be greater than 280 (hex) when read or write operations are requested.
5	LSCTLN	LAST SECTOR LENGTH - This byte, during read into memory operations, contains the number of bytes to be read from the last sector to be used. This number should be between 1 and 128, since each sector contains 128 bytes. If this number is not between 1 and 128 (inclusively), a CRC error will result when the last sector is read.
6,7	CURADR	CURRENT ADDRESS - These two bytes contain the first address from/to which data is to be read/written during disk read/write operations. The Resident Driver Firmware automatically updates this entry after each sector is read/written. During write test operations, these two bytes contain the address of a one byte data buffer.
8	FDSTAT	FLOPPY DISK STATUS - This byte contains a status indicator returned from the Resident Driver Firmware. If an error occurred during a disk operation, the carry bit will be set on return to the caller, and this byte will contain a number indicating the type of error. If no error occurs, then the carry will be reset and this byte will contain the hexadecimal number 30 (ASCII 0).

Table 5-15 Disk Error Messages

FDSTAT (HEX)	ERROR CODE	DESCRIPTION / POSSIBLE CAUSE
30	E0	NO ERRORS - This status indication is returned when no errors have occurred in the disk operation. On return to the user, the carry bit is cleared.
31	E1	DATA CRC ERROR - This status is returned when the CRC following the data is in error. This error would occur after the sector has been read and, if appropriate, written into memory. The CURADR byte will not be updated for the sector with the error. In multiple sector operations, the equation listed at the end of this table can be used to determine the sector number of the physical sector in which the error occured. Possible causes of this error include miswriting and misreading the data and/or CRC. If the error occurred during WRVERF or RWTEST, the sector should be rewritten. Otherwise, another attempt should be made to read the sector. The Disk Driver will attempt to read the sector 5 times before returning this error.
32	E2	DISK WRITE PROTECTED - This status is returned whenever an attempt is made to write to a diskette that is write protected (the diskette has the write protection tab punched out). Note that during XDOS initialization, certain information is written onto the diskette. The write protection tab must be covered with a piece of opaque tape to allow writing on the diskette.
33	E3	DISK NOT READY - This status is returned when an operation is attempted with a disk that is not ready. Possible causes of the not ready status include the drive unit door is not closed, the diskette is not up to speed, the diskette has been inserted into the drive with the wrong orientation, the drive interface cable is not properly inserted.
34	E4	READ DELETED DATA MARK - This status is returned when an attempt is made to read a sector that is prefaced by a deleted data mark. The sector will not be read into memory or written onto the diskette, and the CURADR

byte will not be updated for the sector in error. The equation listed at the end of this table can be used to determine the physical sector in error when this error occurs during a multiple sector operation.

A possible cause of this status is that a deleted data mark was intentionally written to the sector.

35 E5 TIMEOUT - This status is returned when the track address has not been found after five attempts.

Possible causes of this error include attempting to read or write a bad track or sector or an unformatted disk. Reformatting the disk may eliminate this error. This error may also occur as a result of a bad head alignment.

36 E6 INVALID DISK ADDRESS - This error occurs when the sum of the STRSCT and NUMSCT bytes are greater than the number of sectors on the disk. The RESTOR command does not check for this error.

37 E7 SEEK ERROR - This error occurs if a restore is completed incorrectly or track 0 is found before a seek operation is completed. This error may occur during a restore if the drive is not connected to the controller.

38 E8 DATA MARK ERROR - This error occurs if a valid data mark for the sector being read has not been found. This error message occurs before the sector is read, and prevents the sector from being read. The CURADR byte is not updated for the sector in error. The equation provided at the end of this table can be used to determine the number of the physical sector in error, when this error occurs during a multiple sector operation. The Resident Driver Firmware will attempt to read the sector in error five times before returning this error message.

Possible causes of this error include misreading and miswriting the disk.

39 E9 ADDRESS MARK CRC ERROR - This error occurs when the CRC of an address mark is incorrect. This error occurs before the sector is read or written, and stops the operation in progress. The CURADR byte is not updated for the sector in error. The equation provided at the end of this table can be used to determine the sector number in error, when this error occurs in a multiple sector operation.

Possible causes of this error include miswriting the address mark or its CRC when formatting the disk, and misreading the address mark or its CRC. The Resident Driver Firmware will attempt to read the sector in error five times before returning this error message.

EQUATION 1: PSNE = STRSCT + NUMSCT - SCTCNT - 1

where 1: PSNE is the sector number of the physical sector in error.
STRSCT is the contents of the STRSCT byte.
NUMSCT is the contents of the NUMSCT byte.
SCTCNT is the two byte value contained in locations $B and $C. This value is set equal to the contents of the NUMSCT byte at the beginning of a disk read or write operation, and is then decremented before each sector operation.

5.3.5.3 Resident Driver Firmware Entry Points

Various entry points (addresses) are available to the user to perform specific operations contained within the E/ROM Resident Driver Firmware. These entry points are provided in Table 5-16. This table is divided into three parts : the initialization and error check routines part, the disk operation routines part, and the line printer driver routines part. For all of the firmware entry points described below, the content of the resisters is unspecified both upon entry and exit from the subroutine (except where otherwise indicated). Each entry point is accessed by executing a "jump to subroutine" instruction (JSR). The parameters must have been set up in RAM as indicated for each specific function. Upon entry to a disk routine, all MPU resisters are saved, as well as the user's top of memory vector. Before returning from a disk routine, all resisters and the top of memory vector are restored. If an error occurred, the FDSTAT byte will be changed accordingly, and the carry bit set.

Table 5-16 Resident Driver Firmware Entry Points

NAME	ADDR	FUNCTION
		INITIALIZATION AND ERROR CHECK ROUTINES :
OSLOAD	E800	This entry bootloads the disk operating system, initializes the stack pointer and drive electronics, and restores the head position of drive 0 to track 0. The bootloader and operating system's retrieval information block from sectors 23 and 24 (decimal), respectively, of drive 0 are loaded into memory beginning at location 32 (decimal) (20 hex). Control is then passed to the bootloader by jumping to that location. If a disk error occurs, the error number is printed at the system console and control is returned to EXORbus. No user parameters need to be specified when the Resident Driver Firmware is entered at this entry point. The firmware will initialize all the required parameters.
FDINIT	E822	This subroutine initializes the FDC. No user parameters are required by this subroutine and none are modified by it. This subroutine does not change location FDSTAT or the state of the carry bit.
CHKERR	E853	This subroutine checks for a disk error if called immediately after return from a disk operation by checking the carry flag. The subroutine just returns to the user if no error occurred (carry clear). If an error did occur (carry set), then the subroutine prints an E followed by the contents of FDSTAT (in ASCII) and two spaces at the system console. It then gives control to EXORbus. Other than FDSTAT, no user parameters are required. (If a disk error occurs, the Resident Driver Firmware will load the appropriate data into FDSTAT). CHKERR does not modify any user parameters.
PRNTER	E85A	This subroutine prints an E at the system console followed by the contents of FDSTAT (in ASCII) and two spaces. FDSTAT is the only user parameter required by PRNTER. It does not modify any user parameters.

DISK OPERATION ROUTINES :

READSC E869 This entry causes the number of sectors (beginning with STRSCT of CURDRV) to be read from the NUMSCT byte into memory beginning at CURADR. The CURADR byte is updated to the next address to be written to after each sector is read. This entry point initializes the LSCTLN byte to 128 (decimal) so that all of the last sector read will be written to memory. This routine does not change CURDRV, STRSCT, or NUMSCT.

READFS E86D This entry causes the number of sectors (beginning with STRSCT of CURDRV) to be read into memory beginning at CURADR. The CURADR byte is updated to the next address to be written to after each sector is read. This entry point does not change LSCTLN, so that only a portion of the last sector read may be written to memory. This routine does not change CURDRV, STRSCT, NUMSCT, or LSCTLN.

RDCRC E86F This entry causes NUMSCT sectors beginning with STRSCT of CURDRV to be read to check their CRC's. The sectors are not written to memory. This routine does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.

RWTEST E872 This entry point causes the data at CURADR and CURADR+1 to be written to bytes of NUMSCT sectors beginning with STRSCT of CURDRV. After all of the sectors have been written, they are read back to check their CRC's. This routine does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.

RESTOR E875 This entry point causes the head of CURDRV to be restored to track 0. The drive must be ready or restore will return an error. RESTOR does not verify that STRSCT and NUMSCT are valid. RESTOR is used to position the drive's head at known track before using the drive. (The OSLOAD routine restores drive 0). RESTOR does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.

SEEK E878 This entry point causes the head of CURDRV to be positioned at the track containing STRSCT. This routine does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.

WRTEST E87B This entry point causes the byte of data pointed to by the address in CURADR and CURADR+1 to be written to bytes of NUMSCT sectors beginning with STRSCT of CURDRV. This routine does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.

WRDDAM E87E This entry point causes a deleted data address mark to be written to NUMSCT sectors beginning with STRSCT of CURDRV. This routine does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.

WRVERF E8B1 This entry point causes NUMSCT sectors beginning with STRSCT of CURDRV to be written from memory beginning at CURADR. CURADR is updated to the address of the next byte to be read from after each sector has been written. After all of the sectors have been written, they are read back and their CRC's are verified as in RDCRC. This routine does not change CURDRV, STRSCT, NUMSCT, or LSCTLN.

WRITSC E884 This entry point causes NUMSCT sectors beginning with STRSCT of CURDRV to be written from memory beginning at CURADR. CURADR is updated to the address of the next byte to be read from after each sector has been written. This routine does not change CURDRV, STRSCT, NUMSCT, or LSCTLN.

LINE PRINTER ROUTINES :

LPINIT EBC0 This entry point exists only to keep MDOS III compatibility. In MDOS III systems, this subroutine initializes the PIA interfacing with the line printer from a reset condition. In the EXORset, this is done by the EXORbus monitor at RESTART. Therefore LPINIT returns only to the caller program.

LIST EBCC This subroutine sends the contents of the A accumulator to the line printer. If a printer error occurred, carry is set on return to the caller. The LIST routine detects the paper empty and printer not selected conditions as printer errors.

LDATA EBE4 This subroutine sends a character string pointed to by the index register X and terminated by a 04 to the line printer.

LDATA1 EBF2 This subroutine performs the same as LDATA except that this subroutine does not print a carriage return and line feed prior to string. It also uses LIST to send characters to the printer.

5.3.5.4 Disk Mini-Diagnostic Routines

The interactive disk test program included in the disk driver E/ROM is described in CHAPTER 3, paragraph 3.5.2. A Disk Mini-Diagnostic (DMD) routine is also available in the E/ROM resident firmware. This routine permits the user to easily execute any disk function a single time and print the status or to continuously execute disk functions and keep an error count in a RAM location. The locations used by the DMD are listed (by name) in Table 5-17. Both single execution operations and continuous operations are described in the followins steps.

1. Single Execution Operation

In order to execute a disk function one time, set up the locations of CURDRV, STRSCT, NUMSCT, LSCTLN, and LDADDR as required for the function. Next, put the entry point address of the function into EXADDR and a non-zero value in ONECON. Then, by typing the EXORbus command EB98;G, the FDC will be initialized, CURDRV will be restored, and the disk function specified by EXADDR will be executed one time on CURDRV. Upon completion of the disk function or detection of an error, the status is printed at the console (the letter E followed by a single digit 0 to 9), and control is returned to EXORbus. Before starting the DMD, the stack pointer S should be set to a valid area by using the EXORbus command RS. (The EXORbus stack pointer value is acceptable).

Example :

```
.0/xx 00 (LF)     Current drive 0
0001 xx 02 (LF)   Starting sector 200
0002 xx 00 (LF)
0003 xx 00 (LF)   Number of sectors 1
0004 xx 01 (LF)
0005 xx 40 (CR)   Last sector length 40
.20/ xx 01 (LF)   Buffer address 100
0021 xx 00 (LF)
0022 xx E8 (LF)   Read partial sector
0023 xx 6D (LF)
0024 xx FF (CR)   Execute routine once
.EB98;G E0        Execute ; no error
.
```


2. Continuous Execution Operation

In order to continuously execute a disk function, set up locations CURDRV, STRSCT, NUMSCT, LSCTLN and LDADDR as required for the function. Next, put the entry point address of the function into EXADDR and a zero into ONECON. Then, by typing either EB98;G (to start DMD at TOP) or EB90;G (to start DMD at CLRTOP, clear the two byte counters), the FDC will be initialized, CURDRV will be restored, and the disk function specified by EXADDR will be continuously executed on CURDRV until one of the two byte counters is incremented to 0. When a counter reaches 0, an E followed by an indication of the last disk status will be printed at the console, and control will be returned to EXORbus. The user can also cause DMD to stop on the first error of a given type by initializing the corresponding counter to FFFF and entering DMD at TOP.

Table 5-17 Disk Mini-Diagnostic Routines

NAME	ADDR	DEFINITION
CURDRV	00	Same as for normal disk operations.
STRSCT	01	Same as for normal disk operations.
NUMSCT	03	Same as for normal disk operations.
LSCTLN	05	Same as for normal disk operations.
CURADR	06	Set up by DMD from LDADDR before each execution of the requested disk function.
FDSTAT	08	Same as for normal disk operations.
LDADDR	20	These two bytes must be set up by the user with the data he would normally put at CURADR, DMD will update CURADR to LDADDR before each execution of the requested disk function.
EXADDR	22	These two bytes contain the address of the entry point of the disk function (READSC, WRVERF, etc.) to be executed by DMD.
ONECON	24	This byte contains a flag that indicates if the disk function is to be executed once or continuously. If the byte is zero, the disk function will be executed continuously. If the byte is non-zero, the disk function will be executed once.
	60-73	This area contains one two-byte counter for each possible status return from 0 to 9. For example, 60 and 61 contain a two-byte count of the 0 status returns, 62 and 63 contain a two-byte count of the 1 status returns, etc.
CLRTOP	EB90	This location is the entry address of DMD and clears the status counters.
TOP	EB98	This location is the entry address of DMD without clearing the status counters.

5.3.5.5 Recording Format

The format of the data recorded on the diskette is similar to the IBM 3740 format. Data is recorded on the diskette using frequency modulation techniques (each bit recorded on the diskette has an associated clock bit recorded with it). These clock and data bits (if present) are interleaved. By definition, a Bit Cell is the period between the leading edge of one clock bit and the leading edge of the next clock bit. (Thus, the Bit Cell is one clock bit and one data bit if the data bit is present).

When referring to serial data being written to or read from the disk drive, a byte is defined as eight consecutive Bit Cells. The most significant Bit Cell is defined as Bit Cell 0, and the least significant Bit Cell is defined as Bit Cell 7. During a write operation, Bit Cell 0 of each byte is transferred to the diskette first, with Bit Cell 7 being transferred last. Correspondingly, the most significant byte is transferred last. During read operations, Bit Cell 0 of each byte will be read from the diskette first, with Bit Cell 7 last. As with writing, the most significant byte will also be read from the diskette first.

The Mini-Floppy Drives are capable of recording up to 40 tracks of data. The tracks are numbered 0 to 39. Each track is made available to the recording head by moving the head with a stepper motor and carriage assembly controlled by the FDC. The diskette is rotated by the drive motor at a speed of 300 rpm. Table 5-18 shows the mini-disk track format, and Table 5-19 is the track / physical sector number conversion table.

Table 5-18 Mini-Disk Soft Sector Format

PHYSICAL START/END	PATTERN	NAME	
			^
INDEX	16 x FF	Index gap.	| x 1 (3)
			v
	6 x 00	Sync bytes	^
	1 x FE (1)	Address mark	|
	C7 (2)		|
	TRK	Track number	|
	1 x 00		|
	SEC	Sector number	|
	1 x 00		|
	2 x CRC	Address CRC (**)	| x 16 (4)
	11 x FF	Identifier gap	|
	6 x 00	Sync bytes	|
	1 x FB (1)(*)	Data mark	|
	C7 (2)		|
	128 x DATA	Data	|
	2 x CRC	Data CRC (**)	|
	27 x FF	Data gap	v
			^
	101 x FF	Track gap	| x 1 (5)
			v
INDEX			

(1) Data pattern
(2) Clock pattern
(3) This field is written once at start of each track
(4) This field is repeated 16 times (one for each sector)
(5) This field is written once at the end of each track
(*) Deleted data mark : F8
(**) CRC polynomial : XA16 + XA12 + XA5 + 1

Table 5-19 Track / Physical Sector Conversion Table

TRACK DEC	TRACK HEX	PSN HEX	TRACK DEC	TRACK HEX	PSN HEX
00	00	000	20	14	140
01	01	010	21	15	150
02	02	020	22	16	160
03	03	030	23	17	170
04	04	040	24	18	180
05	05	050	25	19	190
06	06	060	26	1A	1A0
07	07	070	27	1B	1B0
08	08	080	28	1C	1C0
09	09	090	29	1D	1D0
10	0A	0A0	30	1E	1E0
11	0B	0B0	31	1F	1F0
12	0C	0C0	32	20	200
13	0D	0D0	33	21	210
14	0E	0E0	34	22	220
15	0F	0F0	35	23	230
16	10	100	36	24	240
17	11	110	37	25	250
18	12	120	38	26	260
19	13	130	39	27	270

CHAPTER 6

TEST POINTS AND TROUBLESHOOTING AIDS

6.1 INTRODUCTION

Several test points are provided on both the Main Controller Board and the Mini-Floppy Disk Controller Board. Some of the test points are outputs used to monitor signals, or as trigger signals. Some of the test points are test inputs to be grounded, in order to disable IC's or sections of the system, as an aid for isolating faulty components.

This chapter also provides the basic references needed to use the signature analysis technique as an aid for testing and troubleshooting the EXORset (e.g. using the HP-5004A Signature Analyzer).

6.2 TEST POINTS

Table 6-1 lists the test points available on the Main Controller Board and Table 6-2 lists the test points available on the Mini-Floppy Disk Controller Board.

Table 6-1 Main Controller Board Test Points

TEST POINT	FUNCTION
TP01	Output - The scope sync feature is used to trigger an oscilloscope to monitor the waveforms associated with a particular point in a program. This trigger pulse is generated when a match occurs with a breakpoint address.
TP02	Output - This test point allows to monitor the PTM O2 output.
TP03	Output - Same as above, except for PTM O1 output.
TP04	Test input - If grounded, this input disables the data bus and the address bus from the MPU.
TP05	Test input - If grounded, this input disables the memory refresh addresses from the CRTC .
TP06	Output - This output is the system timing reference signal.
TP07	Output - This output is the 16 MHz signal, the highest frequency of the timing chain.
TP08	Test input - If grounded, this input allows to adjust the timing PLL circuitry VCM (U112).
TP09	Output - This output is the E (Enable signal), inverted.
TP10	Test input - If grounded, this input enables the MPU address bus buffers even if TP04 is grounded.
TP11	Output - This output is the synchronization signal to be used as the system clock normally connected to the E (Enable) (or phase 2) inputs of the M6800 family peripherals.
TP12	Output - MPU address line A15.
TP13	Output - 4fo (4 MHZ).
TP14	Output - CRTC Hsync not.
TP15	Output - CRTC Vsync not.
TP16	Output - GND.
TP17	Output - GND.

Table 6-2 Mini-Floppy Disk Controller Board Test Points

TEST POINT	FUNCTION
TP01	Test input - If grounded, resets the 74LS161 (U2) 4-bit counter of the data recovery PLL circuitry.
TP02	Output - This output is the 250 KHz DCK (Data Clock) signal to the FDC.
TP03	Test input - If grounded, this input disables the data recovery PLL circuitry feedback loop.

6.3 SIGNATURE ANALYZER REFERENCE SIGNATURES

Signature analysis is based on the "data compression" technique. The data stream available at a logic test node is clocked into a 16-bit feedback shift register during a defined time window. There are 65,536 possible states to which the shift register can become set during a measurement window. These states are decoded and displayed on four hexadecimal indicators, and become a "signature". This signature is then a characteristic number representing time dependent logic activity during a specified measurement interval for a particular circuit node. Any change in the behavior of this node will produce a different signature, indicating a probable circuit malfunction.

Signatures recorded on a known good system, under defined measurement conditions, are given here as reference, and can be compared with the signatures produced by the system under test. The Hewlett-Packard HP5004A Signature Analyzer has been used. Refer to the HP5004A Signature Analyzer Operating and Service manual for a detailed description and operation instructions.

6.3.1 Stimulus

The stimulus for the circuit is supplied by two ways. Either a ROM program exercizes selected portions of the circuit under test, or the processor is forced into a "free-running" mode, cycling through its address range without responding to other instructions. It is absolutely necessary that the stimulus be repetitive.

Free-running enables the test of the address bus, the address decode logic, the data bus, some of the timing circuits and ROM. This portion of the system, excluding the ROM, is called the "kernel".

ROM-resident control programs test the RAM, the PIA's, the ACIA, the PTM and other selected portions of the system. In this case the START and STOP signals must be generated for each test.

6.3.2 Free-running Mode Signature Analysis

6.3.2.1 Free-running Mode Implementation

In the free-run mode, several circuits must be disconnected from the data bus. They are listed hereafter :

U88, U14 through U30, U34 through U49, U107, U106, U52, U53, U64, U65, U101, U6, U11 and U12 on the main board and U21, U22 and U7 through U14 on the FDC board.

The free-running mode can be implemented by forcing a NOP instruction into the MPU. This can be done as follows :

Connect pins 18, 16, 15, 13, 12, 11 of U88 on the main board to ground by means of 10K resistors. Connect pins 17, 14 of U88 to +5V by the same way. Ground test point TP05 on the main board.

6.3.2.2 Free-running Mode Operating Procedure

Connect the inputs of the HP5004A Signature Analyzer as follows :

- GROUND test input to ground.
- CLOCK test input as specified later.
- START/STOP test inputs to U89 pin 23.

- Set the front panel Start, Stop and Clock switches on the falling edge position.

- Turn EXORset power on.

- Turn HP5004A power on.

6.3.2.3 Free-running Mode Signature Table

The signatures that should be read in the free-running mode are listed in Tables 6-3 and 6-4 for the main controller board and in Tables 6-5 and 6-6 for the FDC board.

Table 6-3 Free-running Mode Main Board Signature Table with CLOCK input on U59 pin 6

U96	2	0U16	U110	3	UP73	U83	3	0000	U61	3	UP73
	5	U165		6	P15F		8	0UP8		4	77A4
	8	1U2U		8	UP73		11	PU49		5	UP73
	9	P15F		11	077H					6	CA98
										10	UP73
U66	9	UP73	U70	3	UH74	U71	4	669F		11	HF06
	10	UP73		6	UP73		7	UP73		12	UP73
	11	UP73		8	U165					13	PU49
	12	P15F		11	UP43						
U72	3	0000	U85	3	UP73	U87	4	98PH	U95	1	UP73
	5	0000		5	0U16		7	FH3F		4	0000
	7	98PH		7	98PH		9	U90P			
	9	1U2U		9	3F59		11	0UP8			
	11	89H7		11	98PH		13	89H7			
	13	FH3F		13	0U16						

The FDC board must be disconnected
The signature on the +5V supply must be UP73

Table 6-4 Free-running Mode Main Board Signature Table
with CLOCK input on U85 pin 10

U89	5	0000	U77	3	FFFF	U98	3	0003	U26	9	66C3
	6	0000		5	P763		5	0003		10	U3H6
	8	UUUU		7	0356		7	4FCA	(*)	11	PACH
	9	FFFF		9	U759		9	4868		13	PACU
	10	8484		12	U759		12	9UF1		14	3838
	11	P763		14	1U5P		14	0001		15	7633
	12	1U5P		16	8484		16	6U28		16	160H
	13	0356		18	UUUU		18	0003		17	04UU
	14	U759									
	15	6F9A	U90	3	6F9A	U24	3	AFA5	U27	9	CFHU
	16	7791		5	7791		5	2UPF		10	57HU
	17	6321		7	6321		7	A0CA	(*)	11	96FA
	18	37C5		9	37C5		9	0003		13	546H
	19	6U28		12	37C5		12	1111		14	CA13
	20	4FCA		14	6321		14	F1CH		15	H75C
	21	4868		16	7791		16	P707		16	A3UU
	22	9UF1		18	6F9A		18	5H3U		17	AA68
	23	0001									
	32	0003	U56	6	74U9	U58	1	13PH	U93	6	0003
	34	0003		8	H3P9		4	13PP		8	P257
	35	0003					10	0000		12	0000
U29	10	732H	U28	9	826H	U100	3	P254	U54	1	74U9
	11	A49P		10	6039		4	P254		4	74UA
	12	7302		11	9564		10	P254		10	H3PA
	13	51P2		12	A713		11	P254		13	H3P9
	14	8P04									
	15	5C33	U55	4	UUUF						

The FDC board must be disconnected
The signature on the +5V supply must be 0003

(*) for that measurement U101 pin 10 must be grounded

Table 6-5 Free-running Mode FDC Signature Table
with CLOCK input on U85 pin 10

U24	3	37C5	U40	3	6U28	U41	3	P763	U22	9	3551
	5	4868		5	37C5		5	8484		10	3CCP
	7	0356		7	6321		7	FFFF	(*)	11	8386
	9	6321		9	7791		9	UUUU		13	0385
	12	UUUU		12	4FCA		12	1U5P		14	U0FF
	14	6U28		14	4868		14	0356		15	29CU
	16	0003		16	9UF1		16	U759		16	HP83
	18	4FCA		18	0001		18	6F9A		17	CA03
U43	3	C168	U18	3	0000	U32	3	U3H4	U42	3	P763
	4	C168		8	0000		4	U3H4		4	C168
	10	C168		11	755H		10	U3H4		10	C168
	11	C168					11	U3H4		11	P760
U4	2	0000	U19	3	0003	U31	9	2FF1	U23	3	755P
	6	0000		6	7805		10	7805		4	755P
	8	0000									
	10	0000	U36	6	U3H7						
	12	0000		8	A97A						

The signature on the +5V supply must be 0003

(*) A test PROM (MCM2708) filled with a pattern of 0,1,...,FF through its full address field must be inserted into socket U22

Table 6-6 Free-running Mode FDC Signature Table
with CLOCK input on U59 pin 6

U37	9	UP73	U30	2	UP73	U37	3	89H7	U38	8	UP73
	14	UP73		8	0000		5	98PH			
	16	0U16		10	0211		7	FH3F			
	18	UP73		12	334U		12	1U2U			

The signature on the +5V supply must be UP73

6.3.2.4 Free-running Mode Data Bus Check

The data bus may then be checked by implementing test PROM's into U30 (MCM2716) on the main board and U22 (MCM2708) on the FDC board . The test PROM's are programmed with the pattern 0,1,2,...,FE,FF,0,1,2,...,FF,... for their complete address field.

The operating procedure is the same as described in 6.3.2.2, with the Clock switch on the rising edge position. The signatures that should be read are listed in Table 6-7.

Table 6-7 Data Bus Free-running Mode Signature Table
with CLOCK input on U85 pin 10

U97	2	543A	U88	2	3HF5
	3	1037		3	70P5
	4	99AH		4	U97U
	5	862C		5	P6U9
	6	58C8		6	386A
	7	7F97		7	9F45
	8	981A		8	78F8
	9	PUA4		9	065C

The signature on the +5V supply must be 0003

6.3.3 Program Controlled Mode Signature Analysis

It is time to take a step back and examine where we are. We know that:

- The MPU can run through its address field correctly.
- The address decoding circuit is good.
- The data bus is clear of faults.

6.3.3.1 Program Controlled Mode Implementation

The next thing to do is reconnect the data bus to the MPU and remove the forced free-run instruction. This will be done by :

- Removing the ground from TP05 on the main board.
- Removing the pull up/pull down 10K resistors from the U88 socket on the main board.
- Removing the test PROM's.
- Inserting the test program PROM into U30 on the main board.
- Reconnecting U88 and U101 on the main board.

The different programs used to check selected portions of the system are initiated by the switch SW18 on the main board. They are listed in Table 6-8.

Table 6-8 Test Program Selection

SW18-1	SW18-2	
Open	Open	RAM's & CRT diagnostic
Open	Closed	PTM, ACIA diagnostic
Closed	Open	PIA's diagnostic

6.3.3.2 RAM Check Operating Procedure

Once the RAM test program has been selected according to Table 6-8 and the FDC board implemented, connect the inputs of the HP5004A as follows :

- GROUND test input to ground.
- CLOCK test input to U70 pin 8.
- START/STOP test inputs to U101 pin 15.

- Set the front panel Stop and Clock switches on the rising edge position and the Start switch on the falling edge position.

- Turn EXORset power on.

- Turn HP5004A power on.

6.3.3.3 RAM Check Signature Table

The signatures that should be read are listed in Table 6-9.

Table 6-9 RAM Signature Table

U88	11	F788	U88	11	288U	U88	11	4H32	U89	11	1F24
	12	1UFP		12	5UA1		12	3734		12	2639
(1)	13	P769	(2)	13	68A4	(3)	13	7P95	(4)	13	97PC
	14	109P		14	0243		14	3932		14	CPAH
	15	1C15		15	7APA		15	1296		15	9APC
	16	C5PH		16	P375		16	38FC		16	2C28
	17	H3HC		17	437A		17	11PF		17	7158
	18	8H0U		18	PU22		18			18	

(1) U52,U53,U64 and U65 must be reconnected on the main board
(2) U34 through U41 must be reconnected on the main board
(3) U42 through U49 must be reconnected on the main board
(4) U7 through U14 must be reconnected on the FDC board

The signature on the +5V supply must be C58A

6.3.3.4 CRTC Check Operating Procedure

Connect the inputs of the HP5004A Signature Analyzer as follows :

- GROUND test input to ground.
- CLOCK test input to U92 pin 21.
- START/STOP test inputs to U92 pin 40.

- Set the front panel Start, Stop and Clock on the rising edge position.

- Turn EXORset power on.

- Turn HP5004A power on.

6.3.3.5 CRTC Check Signature Table

The signatures that should be read are listed in Table 6-10.

Table 6-10 CRTC Signature Table

U92	4	1497	U63	2	34FA	U55	2	33CP	U82	6	U479
	5	7989		5	CFF4		6	HF68			
	6	4H28		6	2694		8	0896	U58	11	A7U8
	7	049C		9	024H		10	9UAH			
	8	080F		12	0406		12	4C53	U69	8	P034
	9	31U6		15	18UC						
	10	H7AC		16	6CH5						
	11	U458		19	UA2F						
	12	4730									
	13	UHC8	U75	12	80U0	U57	1	AH58	U76	9	8C5A
	14	0544		13	2A70		5	44CH			
	18	9UAH		14	F7C4		10	P345			
	35	25F1		15	F695						
	36	UCA7		16	3294						
	37	FC08									
	38	971F	U80	2	34FA	U56	3	A7U8	U84	8	9H72
	39	HF68		5	HUHF		13	AH58			
	40	P740		7	PUPP						

The signature on the +5V supply must be H4UP

6.3.3.6 ACIA and PTM Check Operating Procedure

Once the ACIA/PTM test program has been selected according to Table 6-8, and U6, U12 has been plugged in, connect the inputs of the HP5004A as follows :

- GROUND test input to ground.
- START/STOP test inputs to U101 pin 15.
- CLOCK test input as specified later.

- Set the front panel Start and Clock switches on the falling edge position and the Stop switch on the rising edge position.

- Turn EXORset power on.

- Turn HP5004A power on.

6.3.3.7 ACIA/PTM Check Signature Table

The signatures that should be read are listed in Table 6-11.

Table 6-11 ACIA and PTM Signature Table

U5	3	PH9H	U7	3	A32F	U6	5	0000	U12	3	7290
	6	4PC1		6	0000		6	A32F		6	85HP
(1)	8	PH9H	(1)	8	0000	(1)			(2)	27	0000
	11	PH9H									

(1) HP5004A CLOCK input must be on U6 pin 3
(2) HP5004A CLOCK input must be on U85 pin 10 and START/STOP inputs on U12 pin 27

6.3.3.8 PIA's Check Operating Procedure

Once U11, and U107 are reconnected and the PIA check program has been selected according to Table 6-8, connect the inputs of the HP5004A Signature Analyzer as follows :

- GROUND input to ground.
- CLOCK input to U85 pin 10.
- START/STOP inputs to U101 pin 15.

- Set the front panel Start and Clock switches on the falling edge position and Stop on the rising edge position.

- Turn EXORset power on.

- Turn HP5004A power on.

6.3.3.9 PIA's Check Signature Table

The signatures that should be read are listed in Table 6-12.

Table 6-12 PIA's Signature Table

U101	2	7H74	U11	2	3555	U107	2	17765	3		F434
	3	299U		3	9CC6		3	PA12		5	P79U
	4	1048		4	F434		4	H0PP		7	P921
	5	C380		5	P79U		5	A9U3		9	9CC6
	6	0A83		6	P921		6	8986		11	3555
	7	A95F		7	9618		7	U27U		13	89AA
	8	6AF6		8	7U5P		8	8535			
	9	F2C1		9	21U8		9	8UF0	U100	3	C6AP
	10	HA9C		39	89AA						
	11	F371				U108	8	139H	U102	15	A9C7
	12	H728									
	13	1C8H	U2	9	21U8	U93	8	UA04	U95	4	37H6
	14	01C8		11	7U5P		12	745C			
	19	7C7F		13	9618				U85	3	HA9C

The signature on the +5V supply must be 4FAA

CHAPTER 7

DEVICE LOCATION AND SCHEMATICS

This chapter contains the component location diagrams and schematics of the EXORset Main Controller Board and Mini-Floppy Disk Controller Board. Component location diagrams and schematics of the video display monitor, the mini-floppy drives, and the power supply are in their respective maintenance manuals (see APPENDIX A, B, and C).

CHAPTER 8

PARTS LIST

This chapter provides the parts list for the EXORset Main Controller Board and Mini-Floppy Disk Controller Board. The list reflects the latest issue of hardware at the time of printing.

Table 8-1 EXORset Main Controller Board Parts List

0001	01	REF	AR	R	SCHEMATIC DWG	63EW1215X
0002	01	REF	AR	R	ASSEMBLY DWG	01EW1215X01
0010	01	1	EA	B	MAINFRAME PCB	84EW6215X01
0020	01	1	EA	B	CRISTAL QUARZ 4.0 MHZ	48NW9606A22
0030	01	1	EA	B	UHF MODULATOR	ASTEC UM1231
0040	01	6	EA	B	40 PIN DIP SOCKET	28NW9802B09
0050	01	1	EA	B	28 PIN DIP SOCKET	28NW9802C54
0060	01	17	EA	B	24 PIN DIP SOCKET	28NW9802B08
0070	01	6	EA	B	18 PIN DIP SOCKET	28NW9802C04
0080	01	17	EA	B	16 PIN DIP SOCKET	28NW9802B07
0090	01	1	EA	B	2N3904	
0100	01	1	EA	B	2N4401	48NW9610A01
0110	01	1	EA	B	1N4148	
0120	01	2	EA	B	1N914	
0130	01	4	EA	B	SN74LS00N	51NW9615E91
0140	01	1	EA	B	SN74LS01N	51NW9615F62
0150	01	2	EA	B	SN74LS02N	51NW9615C20
0160	01	1	EA	B	SN74LS04N	51NW9615C21
0170	01	1	EA	B	SN74LS08N	51NW9615C22
0180	01	2	EA	B	SN74LS10N	51NW9615E88
0190	01	1	EA	B	SN74LS14N	
0200	01	1	EA	B	SN74LS20N	51NW9615F05
0210	01	1	EA	B	SN74LS30N	51NW9615C23
0220	01	2	EA	B	SN74LS32N	51NW9615C24
0230	01	2	EA	B	SN74LS38N	
0240	01	5	EA	B	SN74LS74AN	51NW9615C25
0250	01	1	EA	B	SN74LS86N	51NW9615F01
0260	01	1	EA	B	SN74LS138N	51NW9615C69
0270	01	1	EA	B	SN74LS139N	51NW9615C70
0280	01	1	EA	B	SN74LS156N	51NW9615E59
0290	01	1	EA	B	SN74LS157N	51NW9615C27
0300	01	1	EA	B	SN74LS161N	51NW9615C28
0310	01	1	EA	B	SN74LS164N	51NW9615F41
0320	01	2	EA	B	SN74LS165N	
0330	01	1	EA	B	SN74LS174N	51NW9615C29
0340	01	8	EA	B	SN74LS244N	
0350	01	1	EA	B	SN74LS266N	51NW9615F09
0360	01	1	EA	B	SN74LS279N	51NW9615E94
0370	01	2	EA	B	SN74LS374N	51NW9615E99
0380	01	4	EA	B	SN74LS640N	51NW9615F63
0390	01	1	EA	B	MC1455	51NW9615B65
0400	01	1	EA	B	MC1488P	51NW9615B29
0410	01	1	EA	B	MC1489P	51NW9615B30
0420	01	1	EA	B	MC3302	
0430	01	1	EA	B	MC4024	51NW9615A28
0440	01	1	EA	B	MC4044	51NW9615B31
0450	01	1	EA	B	MC6809L	51NW9615F86
0460	01	3	EA	B	MC6821	51NW9615B27
0470	01	1	EA	B	MC6840	51NW9615D81
0480	01	1	EA	B	MC6845L	51NW9615F28
0490	01	1	EA	B	MC6850	51NW9615D48
0500	01	4	EA	B	MC6887	51NW9615B71

0510	01	1	EA	B	SCB0241P	
0520	01	1	EA	B	MC79L05G	
0530	01	1	EA	B	MC14017	51NW9615D07
0540	01	4	EA	B	MCM2114L30	51NW9615F47
0550	01	2	EA	B	MCM2716L	
0560	01	16	EA	B	MCM4116	
0570	01	1	EA	B	MCM6641-20	51NW9615F37
0580	01	1	EA	B	MCM6674L	
0590	01	1	EA	B	HM7620	HARRIS
0600	01	2	EA	B	MCM7640DC	
0610	01	93	EA	B	.01 UF CERAMIC	
0620	01	21	EA	B	.10 UF CERAMIC	21NW9702A09
0630	01	2	EA	B	.10 UF POLYESTER	
0640	01	2	EA	B	.10 UF BEAD TANT	
0650	01	5	EA	B	1.0 UF BEAD TANT	
0660	01	1	EA	B	47. UF TANTALUM	
0670	01	2	EA	B	22. PF	
0680	01	1	EA	B	.68 UF POLYESTER	
0690	01	1	EA	B	6-30 PF VARIABLE	
0700	01	1	EA	B	10 PF	
0710	01	3	EA	B	25 UF/16V ELECTRO	23NW9618A33
0720	01	2	EA	B	3.9 K RESISTOR 1/4W	
0730	01	4	EA	B	390 E RESISTOR 1/4W	
0740	01	1	EA	B	680 E RESISTOR 1/4W	
0750	01	5	EA	B	1.0 K RESISTOR 1/4W	
0760	01	8	EA	B	2.2 K RESISTOR 1/4W	
0770	01	2	EA	B	330 K RESISTOR 1/4W	
0780	01	8	EA	B	4.7 K RESISTOR 1/4W	
0790	01	5	EA	B	10. K RESISTOR 1/4W	
0800	01	1	EA	B	820 K RESISTOR 1/4W	
0810	01	1	EA	B	240 E RESISTOR 1/4W	
0820	01	1	EA	B	1.5 K RESISTOR 1/4W	
0830	01	1	EA	B	470 E RESISTOR 1/4W	
0840	01	3	EA	B	39. K RESISTOR 1/4W	
0850	01	1	EA	B	150 E RESISTOR 1/4W	
0860	01	8	EA	B	3.3 K RESISTOR 1/4W	
0870	01	1	EA	B	47. K RESISTOR 1/4W	
0880	01	2	EA	B	560 E RESISTOR 1/4W	
0890	01	1	EA	B	1.0 M RESISTOR 1/4W	
0900	01	1	EA	B	22. K RESISTOR 1/4W	
0910	01	1	EA	B	10. E RESISTOR 1/4W	
0920	01	1	EA	B	820 E RESISTOR 1/4W	
0930	01	1	EA	B	100 E RESISTOR 1/4W	
0940	01	2	EA	B	1 K RES NETWORK SIL10	BOURNS
0950	01	1	EA	B	1 K RES NETWORK SIL8	BOURNS
0960	01	3	EA	B	10K RES NETWORK SIL10	BOURNS
0970	01	1	EA	B	PCB RESET SWITCH	C & K
0980	01	3	EA	B	2X43 PIN PCB CON	28NW9802A72
0990	01	1	EA	B	5 POLES DIN CON	28NW9802C10
1000	01	1	EA	B	23 PIN KEYBOARD CON	
1010	01	1	EA	B	8 PIN KEYBOARD CON	
1020	01	1	EA	B	10 PIN POWER CON	28NW9802B35
1030	01	1	EA	B	BUZZER	SMB-12
1040	01	1	EA	B	VIDEO CON	

Table 8-2 EXORset Mini-Floppy Disk Controller Board Parts List

0001	01	REF	AR	R	SCHEMATIC DWG	62EW1216X
0002	01	REF	AR	R	ASSEMBLY DWG	01EW1216X01
0010	01	1	EA	B	FDC PCB	B4EW1216X01
0020	01	1	EA	B	40 PIN DIP SOCKET	28NW9802B09
0030	01	1	EA	B	24 PIN DIP SOCKET	28NW9802B08
0040	01	8	EA	B	16 PIN DIP SOCKET	28NW9802B07
0050	01	1	EA	B	MP56571	48NW9610A21
0060	01	1	EA	B	SN74LS00N	51NW9615E91
0070	01	2	EA	B	SN74LS04N	51NW9615C21
0080	01	1	EA	B	SN74LS10N	51NW9615E88
0090	01	1	EA	B	SN74LS21N	51NW9615F35
0100	01	1	EA	B	SN74LS30N	51NW9615C23
0110	01	1	EA	B	SN74LS32N	51NW9615C24
0120	01	2	EA	B	SN74LS38N	
0130	01	4	EA	B	SN74LS74AN	51NW9615C25
0140	01	1	EA	B	SN74LS122N	51NW9615E92
0150	01	1	EA	B	SN74LS139N	51NW9615C70
0160	01	2	EA	B	SN74LS161N	51NW9615C28
0170	01	1	EA	B	SN74LS175N	51NW9615F16
0180	01	5	EA	B	SN74LS244N	
0190	01	4	EA	B	SN74LS266N	51NW9615F09
0200	01	1	EA	B	SN74LS640N	51NW9615F63
0210	01	1	EA	B	MC1455	51NW9615B65
0220	01	1	EA	B	MC4024	51NW9615A28
0230	01	1	EA	B	MC4044	51NW9615B31
0240	01	1	EA	B	MC6843L	51NW9615F26
0250	01	1	EA	B	SN7417	51NW9615C75
0260	01	1	EA	B	MC79L05G	
0270	01	8	EA	B	MCM4116	
0280	01	1	EA	B	MCM27A08C	
0290	01	3	EA	B	25. UF/16V ELECTRO	23NW9618A33
0300	01	13	EA	B	0.1 UF CERAMIC	21NW9702A09
0310	01	30	EA	B	.01 UF CERAMIC	
0320	01	3	EA	B	1.0 UF BEAD TANTAL	
0330	01	2	EA	B	0.1 UF BEAD TANTAL	
0340	01	1	EA	B	.01 UF POLYESTER	
0350	01	1	EA	B	6-30 PF VARIABLE	
0360	01	1	EA	B	47 PF	
0370	01	1	EA	B	22 PF	
0380	01	1	EA	B	56 PF	
0390	01	1	EA	B	1.8 K RES NETWORK SIL8	BOURNS
0400	01	1	EA	B	220/330E RES NETWORK SIL8	BOURNS
0410	01	1	EA	B	270 E RESISTOR 1/4W	
0420	01	2	EA	B	820 E RESISTOR 1/4W	
0430	01	1	EA	B	220 E RESISTOR 1/4W	
0440	01	2	EA	B	2.2 K RESISTOR 1/4W	
0450	01	1	EA	B	1.0 K RESISTOR 1/4W	
0460	01	1	EA	B	330 K RESISTOR 1/4W	
0470	01	1	EA	B	1.0 M RESISTOR 1/4W	
0480	01	2	EA	B	22. K RESISTOR 1/4W	
0490	01	2	EA	B	CARD EXTRACTOR	

Table 8-3 EXORset Hardware and Cables Parts List

0001	01	REF	AR	R	ENCLOSURE DWG	15DW198DX
0002	01	REF	AR	R	KEYBOARD DWG	01DW19B1X
0003	01	REF	AR	R	KEYBOARD SUPPORT DWG	
0004	01	REF	AR	R	CRT 9" DWG	01DW1976X
0005	01	REF	AR	R	CRT SHROUD DWG	
0006	01	REF	AR	R	CARD GUIDE SUPPORT DWG	
0007	01	REF	AR	R	POWER SUP DWG	
0008	01	REF	AR	R	DISK DRIVE DWG	01DW1978X
0009	01	REF	AR	R	DISK DRIVE BRACKET DWG	
0010	01	1	EA	B	ENCLOSURE	TEKO
0020	01	1	EA	B	POWER SUPPLY	PLT840 MDD
0030	01	1	EA	B	10 PIN SUPPLY CONNECTOR	
0040	01	1	EA	B	9" CRT	M689MDM9
0050	01	1	EA	B	20 PIN CRT CONNECTOR	AMP 583299-1
0060	01	1	EA	B	CRT SHROUD	
0070	01	1	EA	B	CRT FILTER	HRLG-50-9GR ECKART L
0080	01	2	EA	B	MINI DRIVES	BASF 6106
0090	01	3	EA	B	34 PIN EDGE CONNECTOR	28NW9802B63
0100	01	1	EA	B	(1)FLAT CABLE 34 CONDUCTORS	
0110	01	1	EA	B	(1)PRINTED WIRING BOARD	B4CW6220X01
0120	01	1	EA	B	(1)15/10K RES NETWORK	51NW9626A11
0130	01	1	EA	B	(1)FLAT CABLE 50 CONDUCT	30NW9302A07
0140	01	1	EA	B	(1)36 PIN PLUG CONNECTOR	28NW9802B32
0150	01	1	EA	B	(1)50 PIN PCB TRANSF CONN	28NW9802A08
0160	01	1	EA	B	(1)50 PIN EDGE CONNECTOR	28NW9802A56
0170	01	1	EA	B	(2)20 PIN EDGE CONNECTOR	28NW9802B23
0180	01	1	EA	B	(2)FLAT CABLE	
0190	01	1	EA	B	(2)25 PIN CONNECTOR	501-659-2 ANSLEY
0200	01	1	EA	B	200K POTENTIOMETER	
0210	01	1	EA	B	KEYBOARD	CHOMERICS SIGMA IND.
0220	01	1	EA	B	FAN	ETRI 98XH
0230	01	2	EA	B	CARD GUIDE SUPPORT	
0240	01	6	EA	B	CARD GUIDES	
0250	01	1	EA	B	MAINS MALE PLUG	
0260	01	1	EA	B	POWER SWITCH	
0270	01	1	EA	B	FUSE HOLDER	
0280	01	1	EA	B	FUSE 3A FAST	
0290	01	1	EA	B	MAINS CABLE	
0300	01	1	EA	B	DRIVE MAINTENANCE MANUAL	
0310	01	1	EA	B	LABEL	
0320	01	4	EA	B	BRACKETS	
0330	01	1	EA	B	KEYBOARD SUPPORT	
0340	01	1	EA	B	GUIDE SUPPORT BAR	

(1) Optional Printer Interface Cable (MEX68PIC)
(2) Optional RS-232C Interface Cable

APPENDIX A

M-2000 CRT MAINTENANCE MANUAL

Chapter 7— M68MDM1/M68MDM9
5″ and 9″ Display monitors

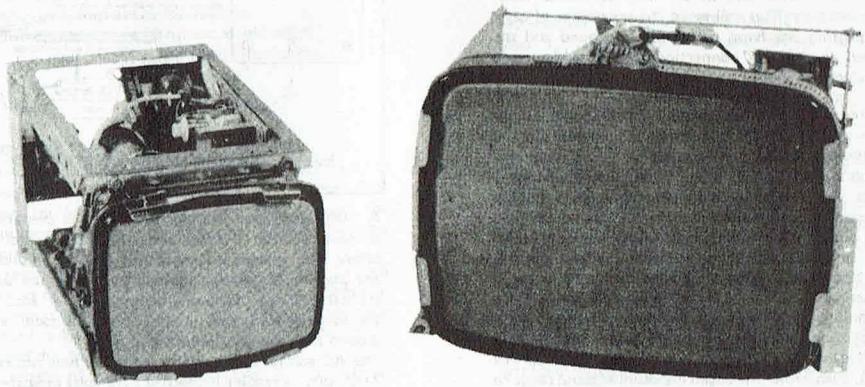


FIGURE 7.0. – DISPLAY: M68MDM1 AND M68MDM9.

7.1. GENERAL INFORMATION

The model described herein is fully transistorized (except CRT) and applicable for displaying alpha-numeric characters. The model M68MDM operates with composite video input as well as with separate TTL synchronisation levels vertical, horizontal and video inputs.,

The CRT'S employed are of the magnetic deflection type with integral implosion protection. An operating voltage of 12 volts DC @ 650 mA (typical) is required from an external power supply.

Input and output connections for the monitor are made through a 10-pin edge connector on the signal circuit card. Inputs consist of video, horizontal/vertical sync, +12 volts and ground. Output connections are provided for an optional remote brightness control.

Two plug-in etched circuits card are utilized, a signal circuit card and a deflection circuit card. Components are mounted on the top of the circuit cards and copper foil on the bottom. Schematic reference numbers are printed on the top and bottom of each circuit card to aid in the location and identification of components for servicing. All standard operating/adjustment controls are mounted in a convenient manner on both circuit cards.

Circuitry consists of four stages for video amplification, six stages for horizontal/vertical sync and deflection processing, and one stage for video blanking during retrace.

CAUTION

No work should be attempted on any exposed monitor chassis by anyone not familiar with servicing procedures and precautions.

7.2. SAFETY WARNING

1. Safety procedures should be developed by habit so that when the technician is rushed with repair work, he automatically takes precautions.

2. A good practice when working on any unit, is to first ground the chassis and to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.

3. Extreme care should be used in **Handling the picture tube** as rough handling may cause it to implode due to atmospheric pressure (14.7 lbs. per sq. in.). Do not nick or scratch glass or subject it to any undue pressure in removal or installation. When handling, safety goggles and heavy gloves should be worn for protection. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode or use a well insulated piece of wire. When servicing or repairing the monitor, if the cathode ray tube is replaced by a type of tube other that specified under the Motorola Part Number as original equipment in this Service Manual, then avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger of personal injury from unnecessary exposure to X-ray radiation may result.

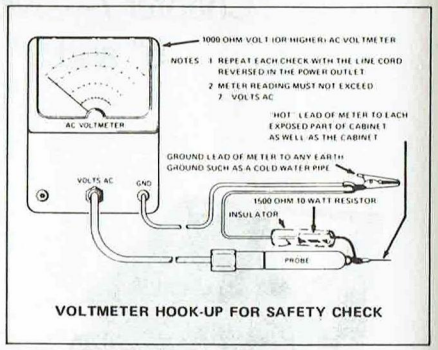
4. An **Isolation transformer** should always be used during the servicing of a unit whose chassis is connected to one side of the power line. Use a transformer of adequate power rating as this protects the serviceman from accidents resulting in personal injury from electrical shocks. It will also protect the chassis and its components from being damaged by accidental shorts of the circuitry that may be inadvertently introduced during the service operation.

5. Always **replace protective devices**, such as fishpaper, isolation resistors and capacitors and shields after working on the unit.

6. If the **high voltage** is adjustable, it should always be **adjusted** to the level recommended by the manufacturer. If the voltage is increased above the normal setting, exposure to unnecessary X-ray radiation could result. High voltage can accurately be measured with a high voltage meter connected from the anode lead to chassis.

7. Before returning a serviced unit, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. **Do not use a line isolation transformer when making this test.**

In addition to practicing the basic and fundamental electrical safety rules, the following test, which is related to the minimum safety requirements of the Underwriters Laboratories should be performed by the service technician before any unit which has been serviced is returned.



VOLTMETER HOOK-UP FOR SAFETY CHECK

A 1000 ohm per volt AC voltmeter is prepared by shunting it with a 1500 ohm, 10 watt resistor. The safety test is made by contacting one meter probe to any portion of the unit exposed to the operator such as the cabinet trim, hardware, controls, knobs, etc., while the other probe is held in contact with a good "earth" ground such as a cold water pipe.
The AC voltage indicated by the meter may not exceed 71/2 volts. A reading exceeding 71/2 volts indicates that a potentially dangerous leakage path exists between the exposed portion of the unit and "earth" ground. Such a unit represents a potentially serious shock hazard to the operator.
The above test should be repeated with the power plug reversed, when applicable.

Never return a monitor which does not pass the safety test until the fault has been located and corrected.

7.3. ELECTRICAL SPECIFICATIONS*

PICTURE TUBE (CRT)	55° deflection angle, P4 phosphor standard	
POWER INPUT	12V DC at 650 mA	
INPUT SIGNALS:	COMPOSITE VIDEO INPUT:	0.5V to 2.5V composite P/P, sync negative (input impedance 74 ohms terminated, 12k ohms unterminated), or
	TTL SEPARATE HORIZONTAL VERTICAL VIDEO:	2.5V to 5.0V P/P, video drive, sync positive at input (input impedance 75 ohms to 250 ohms video termination, >2k ohms vertical and horizontal)
RESOLUTION	650 lines center, 500 lines corners	
VIDEO RESPONSE	Within −3 dB, 10 Hz to 12 MHz	
LINEARITY	Within 2% as measured with standard EIA ball chart and dot pattern	
HIGH VOLTAGE	9.5 kV at 50 uA beam current, nominal	
HORIZONTAL RETRACE TIME	11.0 uSec maximum	
SCANNING FREQUENCY	Horizontal: 15,750 Hz ±500 Hz; Vertical: 50/60 Hz	
ENVIRONMENT	Operating temperature: 0°C to 50°C Storage temperature: −40°C to +65°C Operating altitude: 10,000 feet maximum (3048 meters) Designed to comply with applicable DHEW rules on X Radiation Designed to enable listing under UL Specification 478	

* Specifications subject to change without notice.

7.4. SERVICE NOTES

CIRCUIT TRACING

Component reference numbers are printed on the top and bottom of the plug–in circuit cards to facilitate circuit tracing. In addition, control names and circuit card terminal numbers are also shown and referenced on the schematic diagrams in this manual.
Transistor elements are identified as follows:
E – emitter, B – base, and C – collector.

COMPONENT REMOVAL

Removing components from an etched circuit card is facilitated by the fact that the circuitry (copper foil) appears on one side of the circuit card only and the component leads are inserted straight through the holes and are not bent or crimped.
It is recommended that a solder extracting gun be used to aid in component removal. An iron with a temperature controlled heating element would be desirable since it would reduce the possibility of damaging the circuit card foil due to over–heating.
The nozzle of the solder extracting gun is inserted directly over the component lead and when sufficiently heated, the solder is drawn away leaving the lead free from the copper foil. This method is particularly suitable in removing multiterminal components.

POWER TRANSISTOR REPLACEMENT

When replacing the "plug–in" transistor, please observe the following precautions:
1. The transistor heat sink is not "captive", which means that the transistor mounting screws also secure the heat sink. When installing the transistor, the heat sink must be held in its proper location.
2. When replacing the plug–in transistor, silicone grease (Motorola Part No. 11M490487) should be applied evenly to the top of the heat sink and bottom of the transistor.
3. The transistor mounting nuts must be tight before applying power to the monitor. This insures proper cooling and electrical connections. **Non compliance with these instructions can result in failure of the transistor and/or its related components.**

Note: Use caution when tightening transistor mounting nuts. If the screw three are stripped by excessive pressure, a poor electrical and mechanical connection will result.

CRT REPLACEMENT

Use extreme care in handling the CRT as rough handling may cause it to implode due to high vacuum. Do not nick or scratch glass or subject it to any undue pressure in removal or installation. Use goggles and heavy gloves for protection. In addition, be sure to disconnect the monitor from all external voltage sources.

1. Discharge CRT by shorting 2nd anode to ground; then remove the CRT socket, deflection yoke and 2nd anode lead.
2. Remove CRT from chassis by loosening the one screw that secures the CRT mounting strap or retaining ring.

HORIZONTAL OSCILLATOR ADJUSTMENT

Step 1. Turn on monitor and set up for normal operation.

Step 2. Locate the HORIZ, HOLD control, R35, on the Signal circuit card.

Step 3. Begin rotating R35 CCW until the video display is out of horizontal sync. At this point rotate R35 back CW until the video display just locks in horizontally; then stop. Using tape, mark the left-hand edge of the video display (not the raster edge) of the CRT faceplate.

Step 4. Continue rotating R35 CW until the video display is out of horizontal sync again in the opposite direction. At this point rotate R35 back CCW until the video just locks in horizontally; then stop. Mark the left-hand edge of the video display on the CRT faceplate again.

Step 5. Observe the distance between the two marks on the CRT faceplate. The object is to rotate the HORIZ. HOLD control, R35, until the left-hand edge of the video display is centered between the two marks on the CRT faceplate.

VIDEO BIAS ADJUSTMENT

Step 1. With the monitor operating, rotate the CONTRAST control, R6, for minimum contrast; then disconnect the input signal(s).

Step 2. Connect a voltmeter across R18 (negative probe toward the collector of Q4).

Step 3. Adjust the VIDEO BIAS control, R14 for a +1.0 ±.05 volt indicated.

Step 4. Disconnect the voltmeter.

Step 5. Reconnect the input signal(s) and adjust the CONTRAST control, R6, for desired contrast.

HORIZONTAL LINEARITY ADJUSTMENT

Note: This adjustment procedure is required only when a CRT and/or deflection yoke have been replaced.

PROCEDURE

Step 1. Disconnect monitor from power supply.

Step 2. (Refer to Figure 7.1.) Loosen the deflection yoke clamp screw just enough to permit sliding the copper sleeve on the CRT neck back and forth.

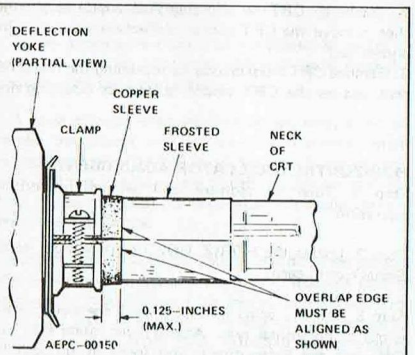


FIGURE 7.1. – PARTIAL VIEW OF CRT NECK/DEFLECTION YOKE FOR HORIZONTAL LINEARITY ADJUSTMENT

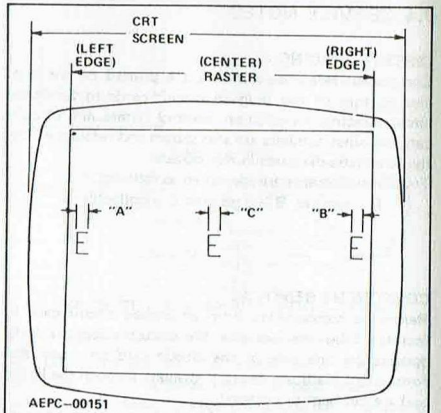


FIGURE 7.2. – PARTIAL CRT RASTER DISPLAY OF CHARACTERS FOR ADJUSTMENT

Step 3. (Refer to Figure 7.1.) Position the copper sleeve so that only 1/8" (.125") extends out past the rear lip of the deflection yoke. In addition, be sure that the overlap edge of the copper sleeve is aligned properly and not twisted.

Step 4. Tighten the clamp screw carefully so as not to disturb the yoke position.

Step 5. Connect the monitor to its power supply and set up for normal operation.

Step 6. (Refer to Figure 7.2.) Observe the extreme left-hand edge characters (designated "A" in Figure 7.2). Its width should be equal to the width of the right-hand edge characters (designated "B" in Figure 7.2). If character "A" is wider than character "B", the copper sleeve is extending out too far. If "A" is narrower than "B", the copper sleeve should be pulled out further. In any event, the copper sleeve may have to be repositioned by trial and error if the 0.125-inch dimension does not provide desired linearity. Continue until the width of character "A" is equal to the width of character "B".

7.5. M68MDM BLOCK DIAGRAM

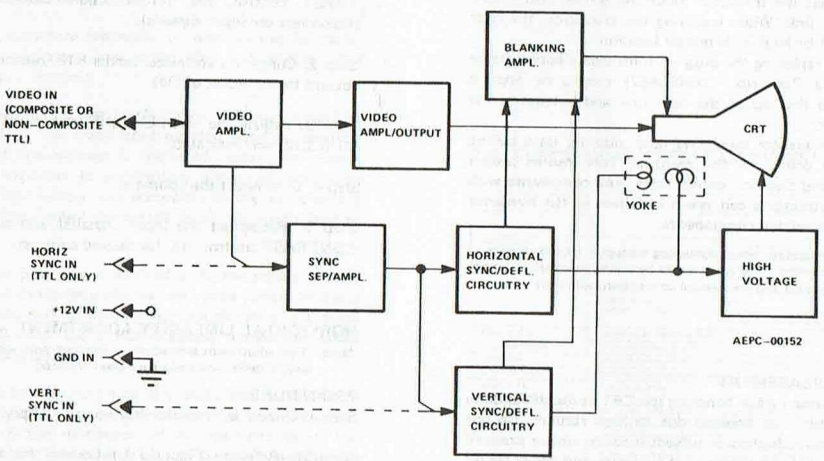


FIGURE 7.3. – M68MDM BLOCK DIAGRAM

7.6. THEORY OF OPERATION

GENERAL

The following circuit description is applicable to monitors using a composite video signal as its input. For monitors using TTL inputs, the description is basically the same. However, the horizontal and vertical sync pulses are coupled from an external source through separate inputs, as is the non-composite video. In addition, jumpers JU1 and JU2 will be inserted in the TTL position.

VIDEO AMPLIFIER CIRCUIT (Reference Figure 7.4)

The video amplifier consists of four stages that include Q1, Q2, Q3 and Q4. The first stage, Q1, functions as an emitter follower. The low output impedance of this first stage permits use of a low resistance CONTRAST control, R6, which furnishes flat video response over its entire range without the need for compensation. The collector output of Q1 is used to drive the sync separator, Q5. Capacitor C2 provides high frequency roll-off to limit the collector output to the bandwidth required to pass synchronization signals.

Transistors Q2 and Q3 form a direct coupled amplifier with frequency compensation provided by C40 and C41. The output from Q3 is capacitively coupled (C5) to the base of Q4, video output stage. The video bias control, R14, is used to set the quiescent collector current of Q4. Frequency compensation is provided by R17 and C6. The combined action of clamping diode D1 and capacitor C5 provide DC restoration for the video signal.

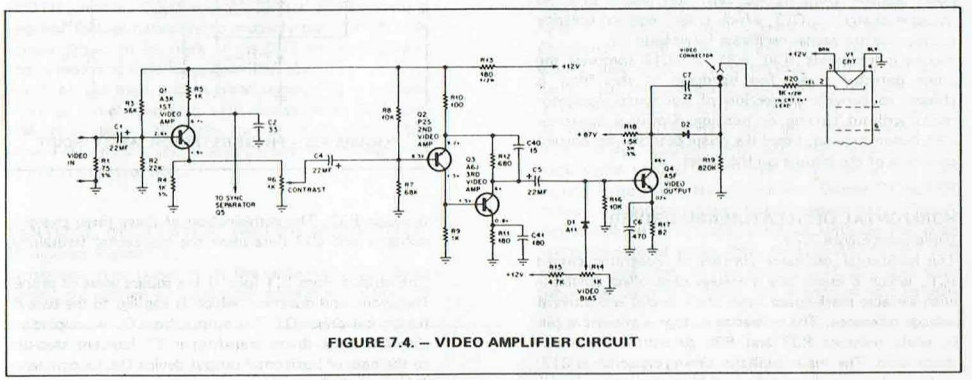


FIGURE 7.4. – VIDEO AMPLIFIER CIRCUIT

Components C7, D2 and R19 provide CRT beam current limiting. Diode D2 normally forward-biased; therefore, as Q4 conducts, its collector voltage drops. This causes a larger beam current to flow through R19, which in turn causes its voltage drop to rise. If excessive beam current flows, the voltage developed across R19 becomes greater than the collector voltage of Q4. This action reverse-biases D2, which prevents a further increase in beam current. Capacitor C7 helps couple video to the CRT cathode, pin 2, through R20. Resistor R20 is used to isolate Q4 from transients that may occur as a result of CRT arcing.

SYNC SEPARATOR/AMPLIFIER CIRCUIT

(Reference Figure 7.5.)

The sync separator employs two stages. Transistor Q5 is the sync separator and Q6 is the sync amplifier. The video input to the sync separator is black positive. Capacitor C3 is charged by the peak base current that flows when the positive peak of the input takes Q5 to saturation. This charge depends on the peak to peak input to Q5 and thus makes the bias for Q5 track the amplitude of the input signal. As a result, Q5 amplifies only the positive peaks of the input signal. The initial bias current through R23 sets the clipping level.

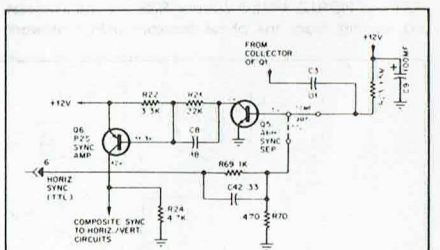


FIGURE 7.5. – SYNC SEPARATOR/AMPLIFIER CIRCUIT

PHASE DETECTOR (AFC)

(Reference Figure 7.6.)

The phase detector control consists of two diodes (D3 & D13) in a keyed clamp circuit. Two inputs are required to generate the required output, one from the sync amplifier, Q6, and one from the horizontal output circuit, Q8. The required output must be of the proper polarity and amplitude to correct phase differences between the input horizontal sync pulses and the

horizontal time base. The horizontal output (Q8) collector pulse is integrated into a sawtooth by R28, C13 and R29. During horizontal sync time, both diodes conduct, which shorts C13 to ground. This effectively clamps the sawtooth on C13 to ground at sync time. If the horizontal time base is in phase with the sync (waveform A), the sync pulse will occur when the sawtooth is passing through its AC axis and the net charge on C13 will be zero (waveform B). If the horizontal time base is lagging the sync, the sawtooth on C13 will be clamped to ground at a point negative from the AC axis. This will result in a positive DC charge on C13 (waveform C). This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag. Likewise, if the horizontal time base is leading the sync, the sawtooth on C13 will be clamped at a point positive from its AC axis. This results in a net negative charge on C13, which is the required polarity to slow the horizontal oscillator (waveform D).

Passive components R30, R31 and C16 comprise the phase detector filter. The bandpass of this filter is chosen to provide correction of horizontal oscillator phase without ringing or hunting. Optional capacitor C14 (when present) times the phase detector for correct centering of the picture on the raster.

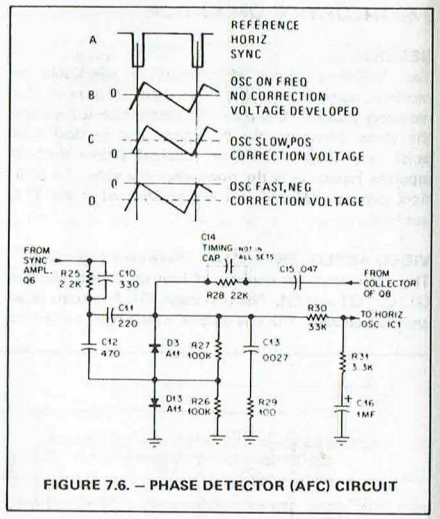


FIGURE 7.6. – PHASE DETECTOR (AFC) CIRCUIT

HORIZONTAL OSCILLATOR AND DRIVER

(Reference Figure 7.7.)

The horizontal oscillator consists of integrated circuit IC1., which is essentially a voltage controlled oscillator with variable mark-space ratio (duty cycle) and internal voltage reference. The reference voltage is present at pin 6, while resistors R37 and R38 determine the mark-space ratio. The main oscillator timing capacitor is C17, with its charging current derived from three sources: (a) a fixed current from R33, (b) a variable current from R34 and HORIZ. HOLD control R35, (c) and a correcting current from the phase detector (AFC) network through R32. The combination of these three charging currents and C17 determine the horizontal frequency.

The output from IC1 (pin 1) is a square wave of proper frequency and duration, which is applied to the base of horizontal driver Q7. The output from Q7 is coupled via the horizontal driver transformer T1 (current step-up) to the base of horizontal output device Q8. Components R41 and C19 provide current limiting, while components R40 and C18 provide transformer damping to suppress ringing in the primary of T2 when Q7 goes into cutoff.

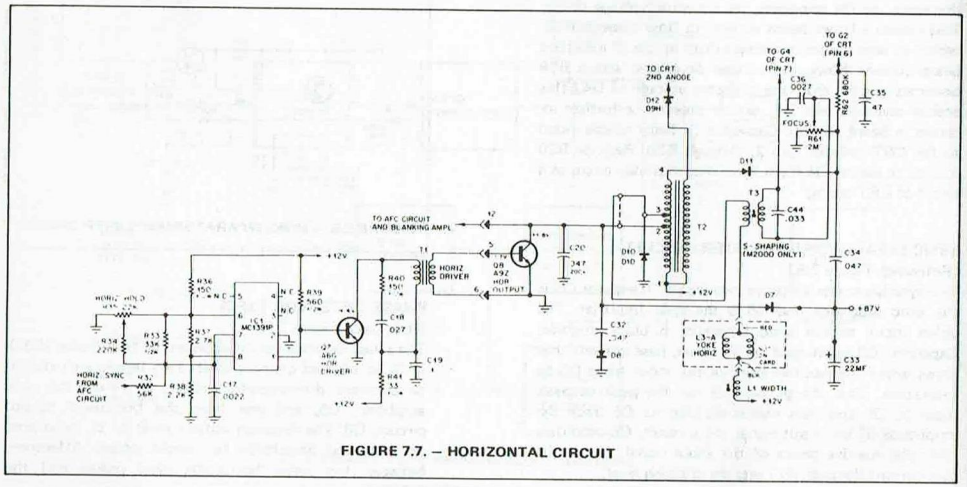


FIGURE 7.7. – HORIZONTAL CIRCUIT

HORIZONTAL OUTPUT (Reference Figure 7.7.)

The secondary of T1 provides the required low drive impedance for Q8. Once during each horizontal period, Q8 operates as a switch that connects the supply voltage across the parallel combination of the horizontal deflection yoke (L3-A) and the primary of the high voltage transformer, T2. The required sawtooth deflection current (through the horizontal yoke) is formed by the L-R time constant of the yoke and primary winding of transformer T2. The horizontal retrace pulse charges C33 through D7 to provide +87V. Momentary transients at the collector of Q8, should they occur, are limited to the voltage on C33 since D7 will conduct if the collector voltage exceeds this value. The damper diode, D10, conducts during the period between retrace and turn on of Q8. Capacitor C20 is the retrace tuning capacitor. Coil L1 is a series HORIZ. WIDTH control. Components C32 and D8 generate a negative voltage necessary to properly bias the CRT. A copper sleeve on the neck of the CRT shapes the horizontal magnetic field for proper linearity.

Pin 4 of the high voltage transformer, T2, is a boost winding, which together with components D11 and C34, develops a +400 volts for G2 of the CRT. This same +400 volts is also always present on the high side of FOCUS control R61.

VERTICAL OSCILLATOR, DRIVER AND OUTPUT

(Reference Figure 7.8.)

Composite sync pulses from the collector of Q6, Sync Ampl., are applied to the double integrating network of R45, C23, R46 and C24. The horizontal component of the sync signal is removed, leaving only the vertical sync pulses. The vertical sync pulses are coupled to the free running vertical oscillator stage, Q10, by C25 and R47. Transistors Q10 and Q12 are connected as a multivibrator. Transistor Q11 is used as an emitter follower that provides a low impedance drive for the vertical output stage, Q12. The series combination of capacitors C27 and C28 are initially charged to the supply voltage through R53 and the VERT. Size control, R52, which generates an exponential ramp of voltage.

When a positive vertical sync pulse is applied to the base of Q10, it begins conducting, which immediately discharges C27 and C28. This action turns off Q11 and causes a sudden decrease in the collector current of Q12, which also decreases the vertical deflection current through deflection yoke (L3-B) and vertical yoke (L2). The resultant rapidly collapsing field in L2 generates a large voltage spike that is used for vertical retrace. Components R58, C29, R51 and C26 shape this spike to ensure that Q10 remains conducting until retrace is carried out to completion. Diode D4 couples the shaped spike to the base of Q10. At this point, Q10 reverts to its non-conducting state and the cycle repeats. The VERT HOLD control, R49, and R48, provide a feedback signal to Q10 to maintain oscillation in the event vertical sync pulses are not present. Diodes D5 and D6 provide the proper voltage drops to operate Q12 class A. Vertical linearity is maintained by applying the ramp voltage generated across R59, through R57 (VERT LIN control) and R54, to the junction of C27 and C28. Since this path is resistive, the waveform will be inte-

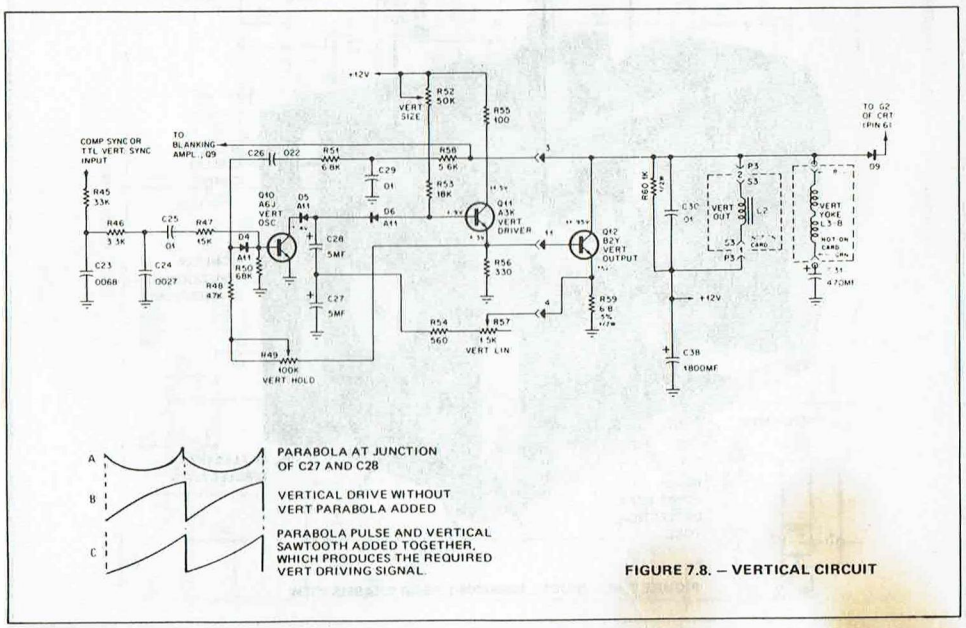


FIGURE 7.8. – VERTICAL CIRCUIT

grated into a parabola by C27 (waveform A). This results in a predistortion of the ramp waveform (waveform C.) (Waveform B illustrates the drive sawtooth without parabola shaping.) Parabolic shaping is necessary to compensate for the non-linear charging of C27 and C28, and the impedance change occuring in L2 with current. Capacitor C31 serves to remove the DC component of the vertical deflection yoke current. Diode D9 clamps the collector voltage of Q12 to a safe level.

RETRACE BLANKING (Reference Figure 7.9.)
Retrace blanking is provided by negative-going horizontal and vertical rate pulses applied to G1 of the CRT. The collector pulse from the horizontal output stage, Q8, is developed across R43 through R42 and C22. The collector pulse from the vertical output stage, Q12, is differentiated by C21 to remove the sawtooth portion of the waveform. The remaining pulse appears across R43. The mixed vertical and horizontal pulses on R43 are amplified and inverted by the blanking amplifier, Q9, and applied to G1 of the CRT.

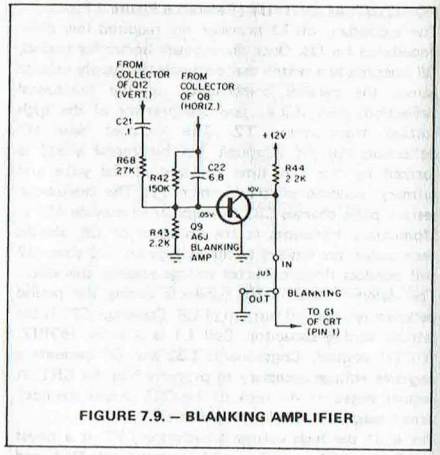


FIGURE 7.9. – BLANKING AMPLIFIER

7.7. M68MDM-1 CHASSIS PARTS LOCATION

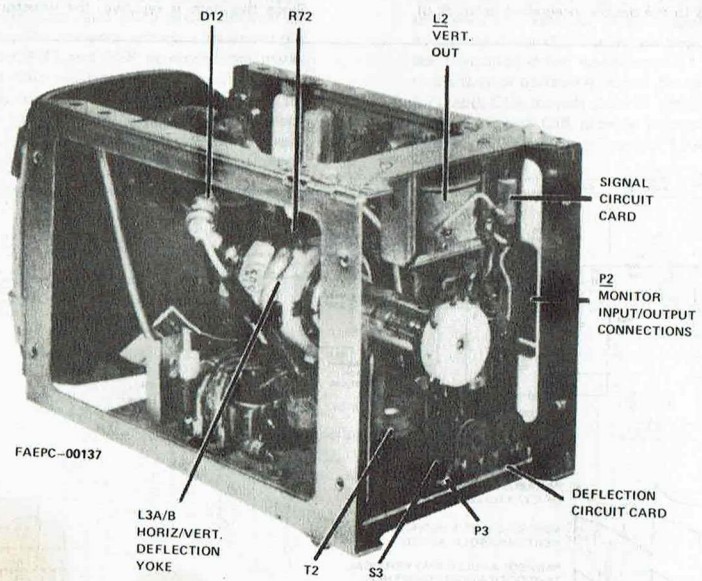


FIGURE 7.10. – MODEL M68MDM-1 REAR CHASSIS VIEW

7.8. M68MDM SCHEMATIC

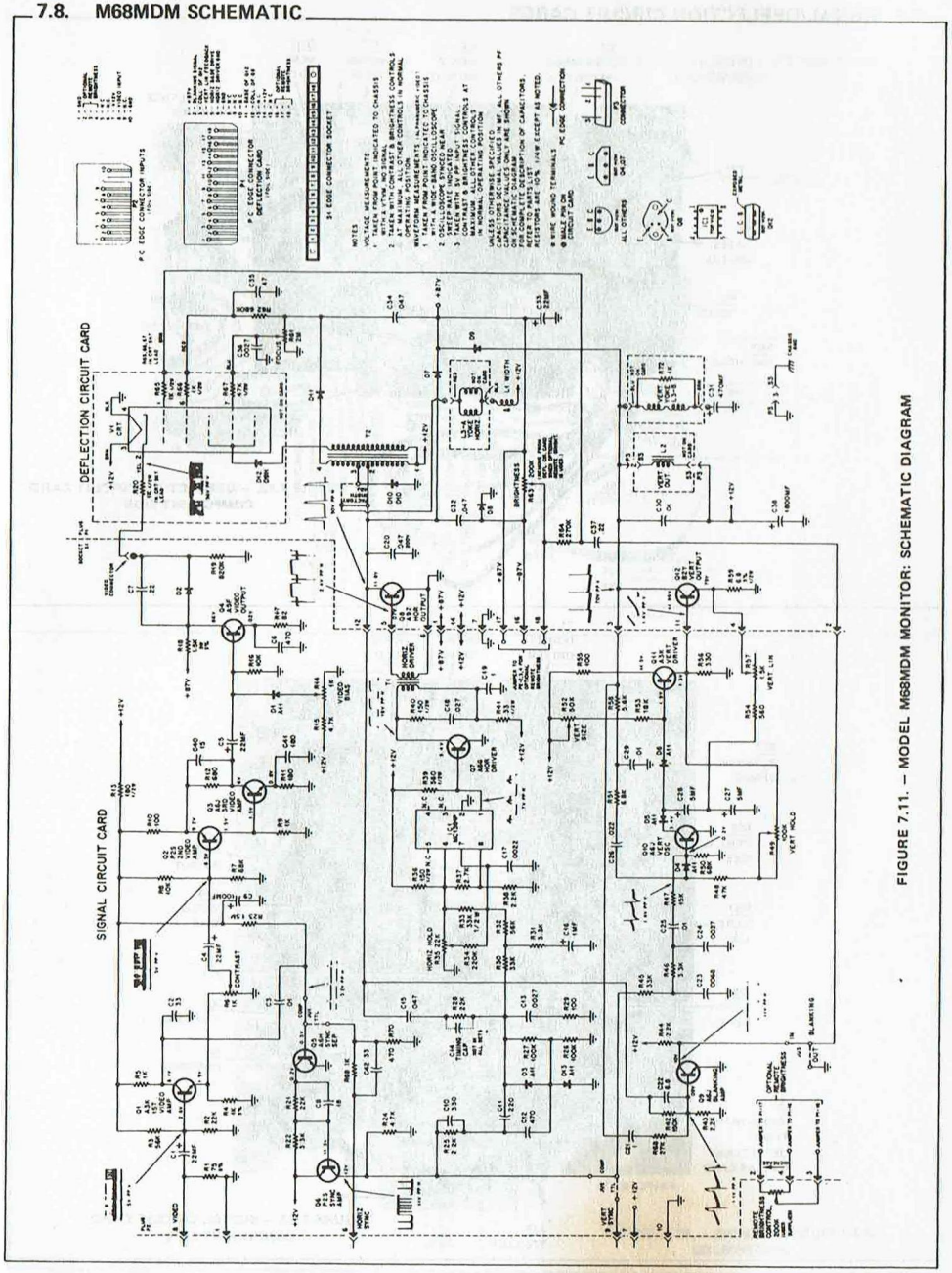


FIGURE 7.11. – MODEL M68MDM MONITOR: SCHEMATIC DIAGRAM

7.9. SIGNAL/DEFLECTION CIRCUIT CARDS

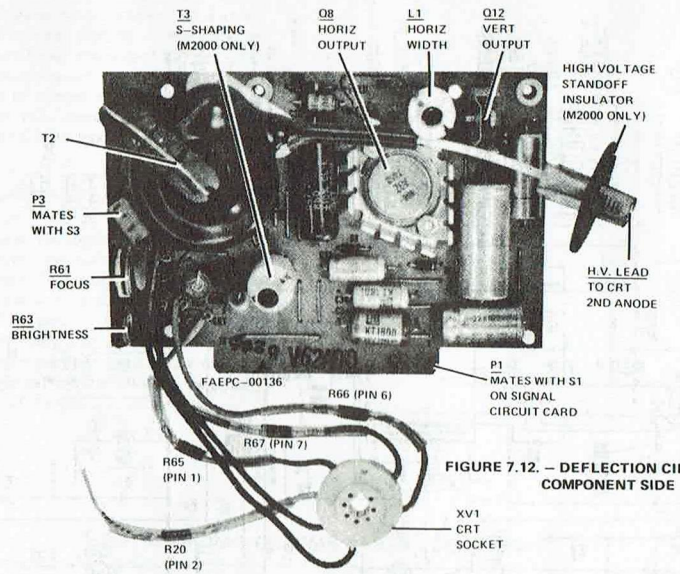


FIGURE 7.12. – DEFLECTION CIRCUIT CARD COMPONENT SIDE

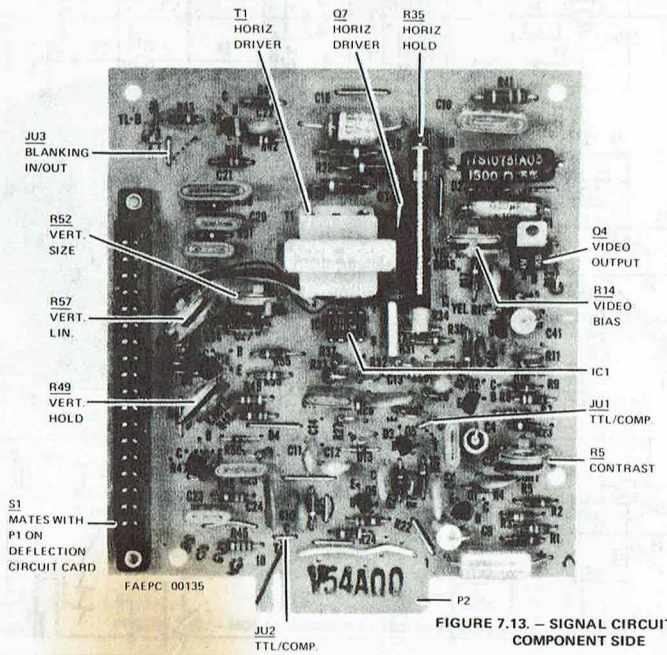


FIGURE 7.13. – SIGNAL CIRCUIT CARD COMPONENT SIDE

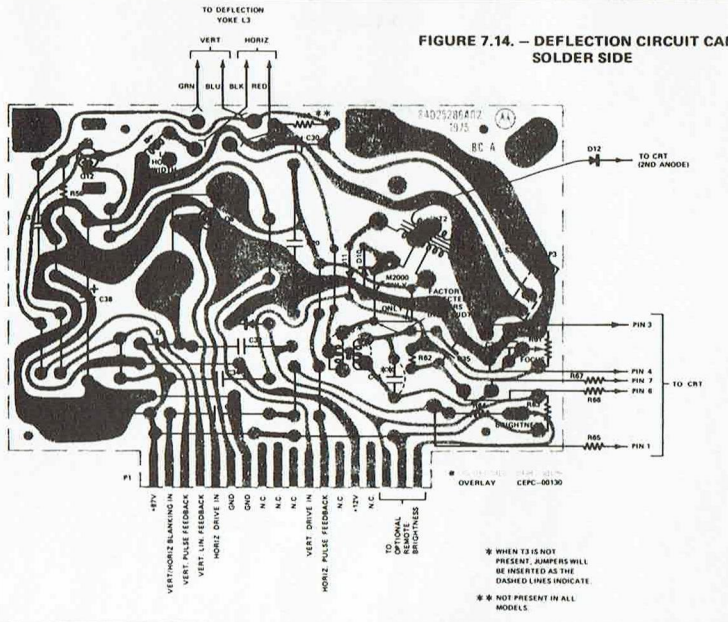


FIGURE 7.14. – DEFLECTION CIRCUIT CARD SOLDER SIDE

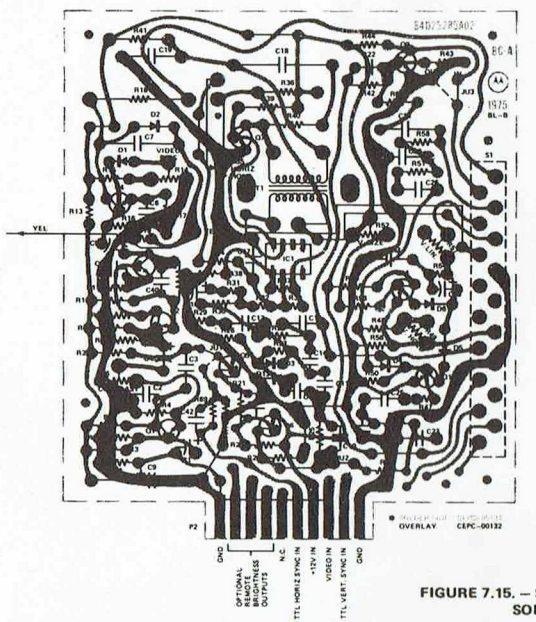
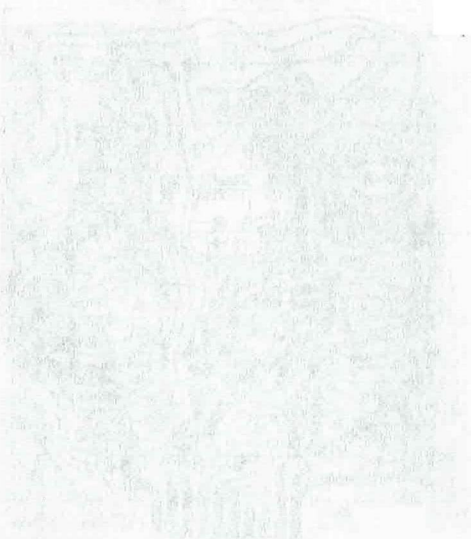


FIGURE 7.15. – SIGNAL CIRCUIT CARD SOLDER SIDE



APPENDIX B

BASF 6106 MAINTENANCE MANUAL

3.2. OPERATION

3.2.1. GENERAL

There are no front panel controls on the BASF 6106. All power and control functions are handled through the interface. Operating procedures consist primarily of loading and unloading the mini disk.

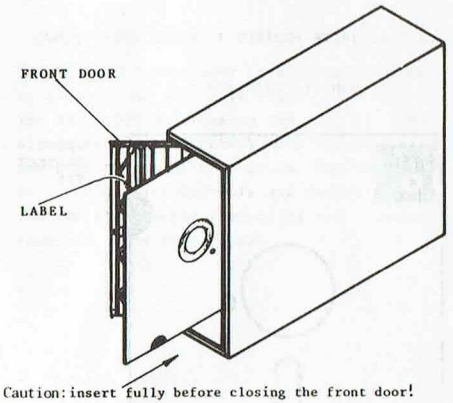


FIGURE 3 - 11. MINI DISK LOADING

3.2.2. MINI DISK STORAGE AND HANDLING

The following are essential requirements for mini disk storage and handling:

- The mini disk should be stored in an enviroment that is clean and free from all magnetic influences.
- The mini disk should be in same temperature and humidity enviroment as the disk drive for a minimum of five minutes prior to use.
- Return mini disk to protective envelope when not in use.
- Never place heavy objects on the mini disk cartridge.
- Never touch the mini disk trough the cartridge opening when handling.
- Never attempt to clean the mini disk.
- Do not bend or fold the mini disk.
- Do not use rubber bands or paper clips on the mini disk.
- Never write on cartridge (use labels).
- Do not expose mini disk to excessive heat or sunlight.

STEP	ACTION
1	Press front door to open position
2	Insert minidisk fully with label towards front door
3	Close front door

TABLE 3 - 11 . MINI DISK LOADING

Proper loading of the mini disk is vital to the operation of the mini disk and drive. Figure 3-11 shows the proper loading of the mini disk.

STEP	ACTION
1	Press front door to open position
2	Remove mini disk

TABLE 3 - 12 . MINI DISK UNLOADING

Procedures for loading and unloading the mini disk drive are given in Tables 3-11and 3-12 respectively.

3.2.3. WRITE PROTECT

There are two fashions usual to protect a mini disk from writing:

a) Write Protect if Notch open (ECMA)

b) Write Protect if Notch covered (Shugart)

3.2.3.1. WRITE PROTECT IF NOTCH OPEN (ECMA)

Jumper: JJ3 : 3 - 4

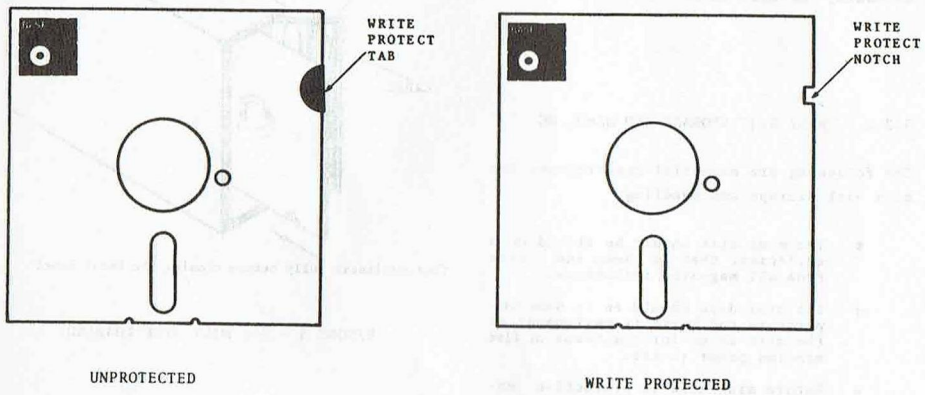


FIGURE 3 - 12 . WRITE PROTECT FEATURE (ECMA)

3.2.3.2. WRITE PROTECT IF NOTCH COVERED (SHUGART)

Jumper : JJ3 : 5 - 6
JJ4 : 3 - 4

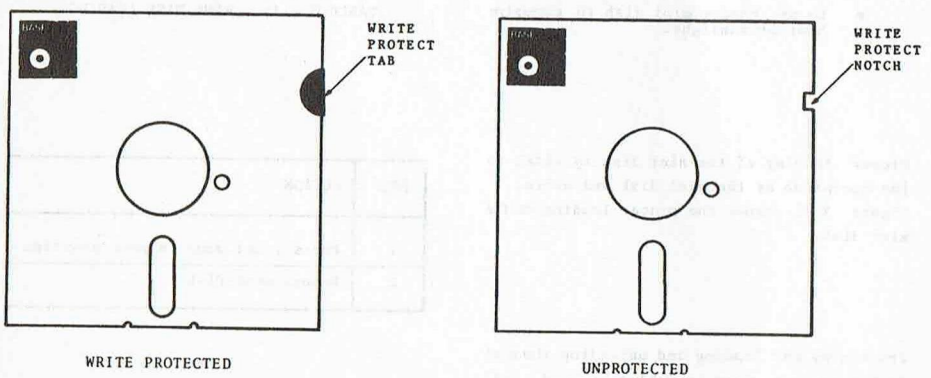


FIGURE 3 - 13 . WRITE PROTECT FEATURE (SHUGART)

SECTION 4

MAINTENANCE

4.1. GENERAL

This section contains the procedures to performing preventive maintenance, operational checks, alignments and adjustments for the model 6106 mini disk drive.

The BASF 2007 exerciser is a portable unit to operate the mini disk drive off- line. The BASF 2007 will enable the user to make all adjustments and check outs required on the BASF 6106 mini disk drive. The exerciser is provided with controls and indicators to execute all control operations and simulate read and write operations.

4.2. TOOLS AND TEST EQUIPMENT

To perform proper maintenance of the mini disk drive, certain tools, test equipment and supplies are required. A list of standard tools and test equipment is provided in table 4-1. Special tools and test equipment are listed in table 4-2.

Common hand tools Freon Cotton tipped swabs (Q-tips) Soft lint- free cloth (gauze) Voltohmmeter Oscillosscope Inspection Mirror Frequency Counter Dial Gauge (Belt Tension)

TABLE 4 - 1 . STANDARD TOOLS AND TEST EQUIPMENT

BASF - CE - Mini Disk BASF - CLEANING Mini Disk Exerciser BASF 2007

TABLE 4 - 2 . SPECIAL TOOLS AND TEST EQUIPMENT

4.3. CHECKS, ADJUSTMENTS AND REPLACEMENTS

4.3.1. PCB REPLACEMENT

a. Turn off DC voltages.

b. Remove P1, P2, P3, P4, P5, P6.

c. Remove the 4 mounting screws.

d. To reinstall, reverse the above.

e. Check and readjust the INDEX-detector.

f. Readjust the drive motor speed and jitter, if a new PCB was installed.

4.3.2. SPINDLE DRIVE SYSTEM

The spindle drive system consists of the drive motor, the drive motor pulley, the spindle drive belt and the spindle drive pulley.

4.3.3.1. DRIVE MOTOR AND DRIVE BELT CHECKS

a. Turn off the DC input power

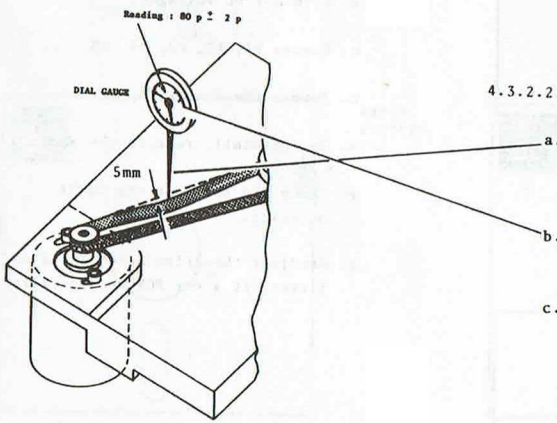
b. Rotate drive motor manuelly and inspect- drive belt for wear , cracks or fraying edges.
Replace drive belt, if necessary.

c. Rotate motor manuelly and inspect for bearing noises or binding. Replace drive motor, if nenessary.
(Ref. to Drive Motor Replacement Procedure)

d. Turn on DC power to mini disk drive

e. Start drive motor (MOTOR ON/ active)

f. Verify that drive motor and drive belt operates normally and that drive belt tracks evenly and smoothly in center of both pulleys.

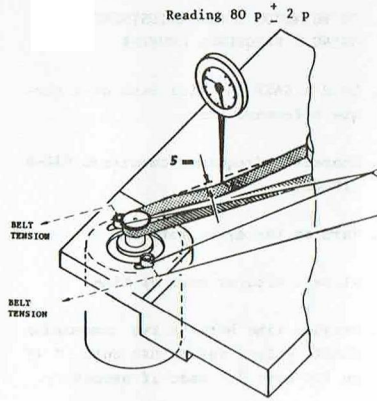


4.3.2.2. DRIVE BELT TENSION CHECK

a. Take a dial gauge and press it against the drive belt until the deflection of the belt is 5 mm.

b. The reading on the gauge must be ~ 80 p

c. If the measured value is out of limits perform drive belt tension adjustment.



4.3.2.3. DRIVE BELT TENSION ADJUSTMENT

a. Slighty loose the drive motor setscrews.

b. Adjust the drive belt tension for a Reading of 80 p on the dial gauge , when the drive belt is 5 mm deflected.

c. Thighten the drive motor setscrews.

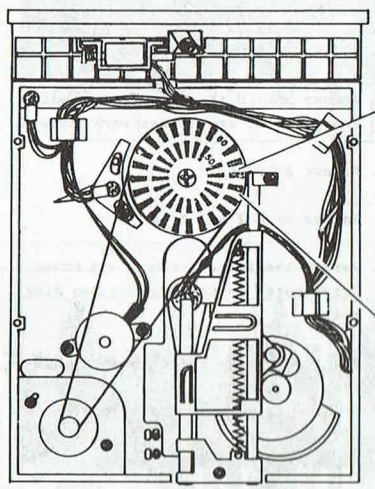
4.3.2.4. DRIVE MOTOR SPEED CHECK

a. Load a BASF CE Mini Disk or a torque reference disk.

b. Turn on drive motor

c. Allow 5 minutes warm up time.

d. Check that the dark lines of the tacho disk on the spindle pulley appear motionless. Use the inside ring for 50 Hz and the outside ring for 60 Hz. *



4.3.2.5. DRIVE MOTOR SPEED ADJUSTMENT

a. Load a BASF CE Mini Disk or a torque reference disk.

b. Turn on drive motor.

c. Allow 5 minutes warm up time.

d. Turn the potentiometer R 47 until the dark lines of the tacho disk on the spindle pulley appear motionless. Use the inside ring for 50 Hz and the outside ring for 60 Hz. *

* This adjustment is only possible in an area where flourescent light exists. Otherwise provide the adjustment or check as shown in 4.3.2.6.

4.3.2.6. DRIVE MOTOR SPEED ADJUSTMENT USING A FREQUENCY COUNTER

a. Load a BASF CE- Mini Disk or a torque reference disk.

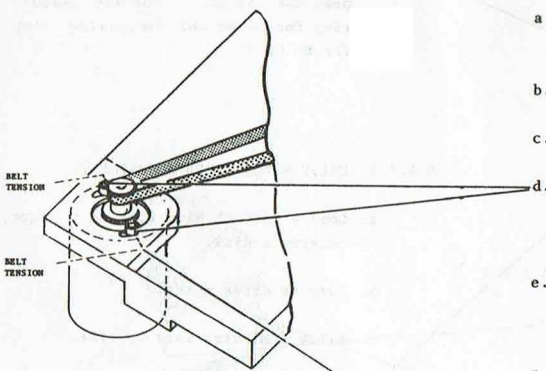
b. Connect a frequency counter to TJ2-8 (INDEX)

c. Turn on the drive motor.

d. Allow 5 minutes warm up time.

e. Measure time between two consecutive INDEX- pulses and adjust poti R 47 to 200 msec $\pm$ 1 msec if necessary.

4.3.2.7. DRIVE MOTOR REPLACEMENT



a. Remove mini disk drive from mounting, and place it on a clean work surface.

b. Remove drive belt.

c. Remove wire 2 and 4 of P6.

d. Remove the two drive motor set screws. Drive motor is now loosened from disk drive.

e. Place new drive motor in same position and fasten it slightly. Tighten drive motor setscrews.

f. Re install wire 2 and 6 P6.

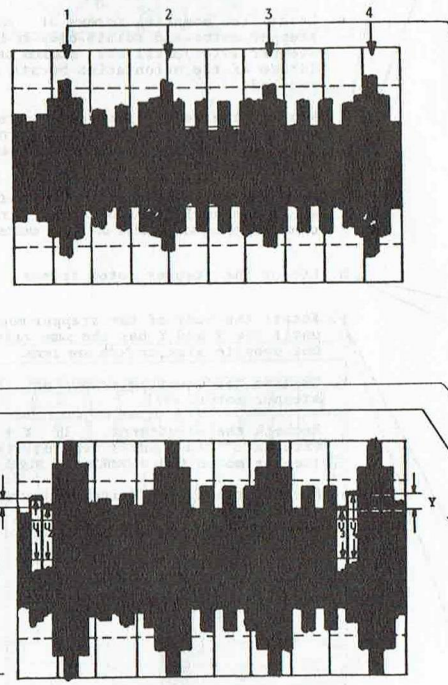
g. Install drive belt and verify correct tracking.

h. Provide drive belt tension adjustment procedure (4.4.2.3).

4.3.3. POSITIONING SYSTEM

The positioning system consists of the stepper motor with spiral wheel, the head carriage assembly and the track 00 microswitch.

4.3.3.1. TRACK ADJUSTMENT CHECK



a. Load a BASF - CE Mini Disk

b. Start the drive motor and select the mini disk drive.

c. Allow 10 minutes warm up time, then step the carriage to track 16.

d. Measure with oscilloscope:

SYNC : EXT. POS. TJ2-8 INDEX

CH 1 : AC 50 mV uncalibrated inverted TJ1-7

CH 2 : AC 50 mV uncalibrated TJ1-9

MODE : ADD

TIME BASE : 10 ms/ Div.uncalibrated

e. Monitor the read signal on the screen and adjust the time base of the scope until four orientation bursts are shown.

f. Turn the variable gain potentiometer until the amplitude of the first orientation burst reaches 60 scale units.

g. Determine X and Y. (see Example!)

$X = U_1 - U_2$ Caution: Pay attention to sign

$Y = U_3 - U_4$

h. Calculate Z

$Z = X + Y$

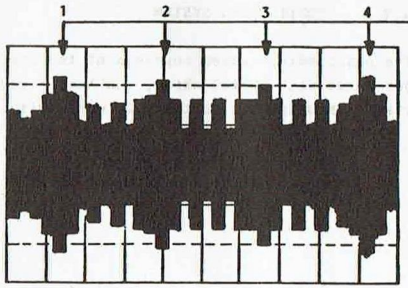
i. If Z exceeds 15 scale units proceed with point e. of track adjustment procedure (4.4.3.2.).

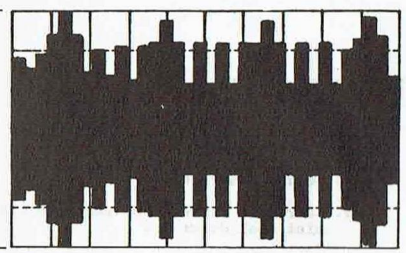
EXAMPLE:

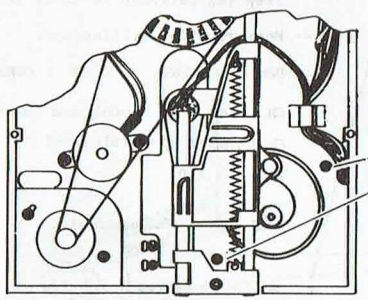
$X = U_1 - U_2 = +2$ scale units

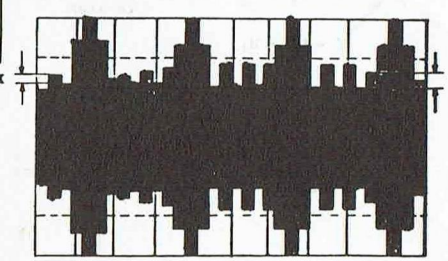
$Y = U_3 - U_4 = -4$ scale units

$Z = X + Y = +2 - 4 = -2$ scale units









4.3.3.2. TRACK ADJUSTMENT

a. Load a BASF CE Mini Disk

b. Start the drive motor and select the mini disk drive.

c. Allow 10 minutes warm up time then step the carriage to track 16.

d. Measure with oscilloscope

SYNC : EXT. POS. TJ2-8 INDEX

CH 1 : AC 50 mV uncalibrated inverted TJ1-7

CH 2 : AC 50 mV uncalibrated TJ1-9

MODE : ADD

Time
Base : 10 msec/Div. uncalibrated

e. Loosen the mounting screws of the stepper motor and rotate body of the stepper motor until the maximum amplitude of the orientation bursts is reached.

f. Monitor the read signal on the screen and adjust the time base of the scope until four orientation bursts are shown.

g. Turn the variable gain potentiometer until the amplitudes of the first orientation burst reaches 60 scale units.

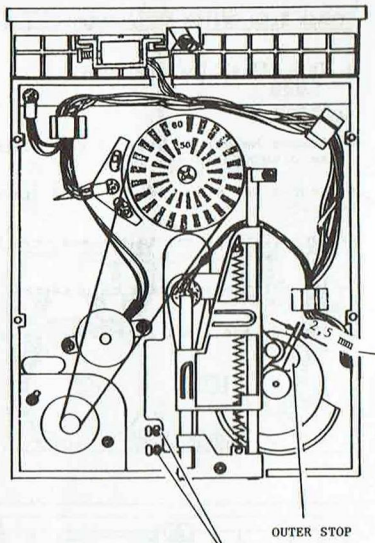
h. Loosen the stepper motor screws.

j. Rotate the body of the stepper motor until the X and Y has the same value but oposite sign, or both are zero.

k. Tighten the mounting screws of the stepper motor.

l. Recheck the adjustment. If X + Y exceeds 3 scale units readjust the stepper motor (Pay attention to sign!).

m. Perform track zero switch adjustment check (4.4.3.3.).



4.3.3.3. TRACK ZERO SWITCH ADJUSTMENT CHECK

a. Select mini disk drive and start drive motor.

b. Monitor TJ2-3 (TRACK ZERO SWITCH)

SYNC : AUTO

CH 1 : 2 V / Div. TJ2-3

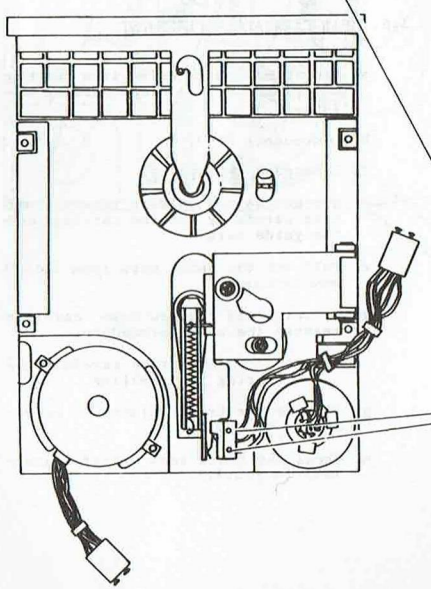
MODE : CH 1 only

TIME
BASE : 10 msec/ Div.

c. Step out to track 0

d. Check space between head carriage and outer stop for ~ 2.5 mm.
If the space is not correct provide track zero switch adjustment.

e. Check if track zero switch closes (TJ2-3 → low) between track 3 and 2 when stepping towards track zero and opens (TJ2-3 → high) between track 2 and 3 when stepping from track 0 to track 4. If the track zero switch will not change within these limits provide track zero switch adjustment.



4.3.3.4. TRACK ZERO SWITCH ADJUSTMENT

a. Load Test Disk

b. Select mini disk drive and start drive motor.

c. Measure with Oscilloscope.

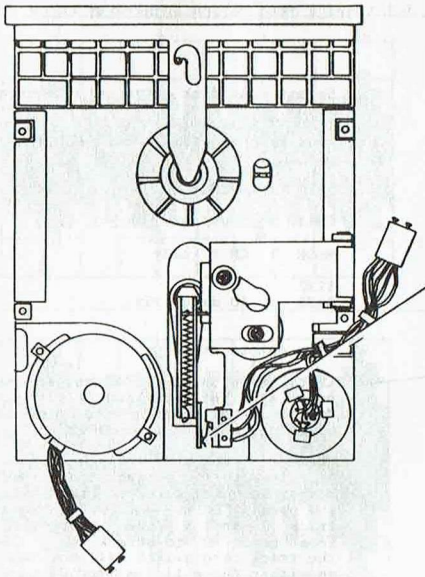
SYNC : AUTO
CH 1 : 2V/DIV TJ2-6
(TRACK 00)
CH 2 : 2V/DIV TJ2-3
(TRACK 0 - SWITCH)
MODE : Chopped

TIME
BASE : 10 msec/DIV

d. Step the head carriage out until the head carriage touches the outer stop.

e. Step in until CH1 goes high (normally one step in). Now the head carriage is positioned at track 0.

f. Loosen the track o switch and adjust it that it will close (TJ2-3: high → low) between track 3 and 2 when the head carriage is moved towards track 0 and will open (TJ2-3: low → high) between track 2 and 3 when the head carriage is stepped from track 0 to track 4.



4.3.3.5. TRACK ZERO SWITCH REPLACEMENT

a. Turn off all DC input power.

b. Remove PCB.

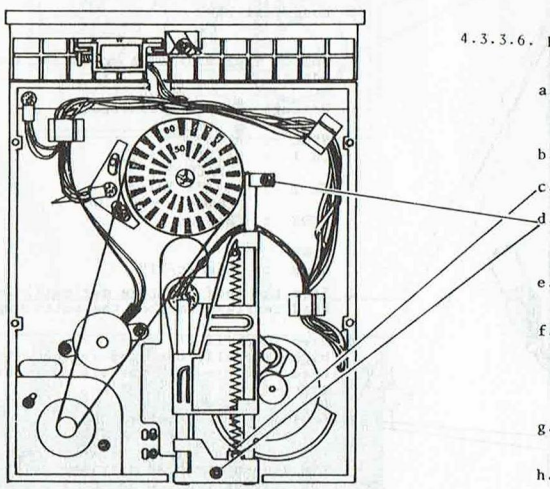
c. Remove holding screws of the track zero switch (on the rear).

d. Remove the wires of the track zero switch.

e. Connect the wires to the new track zero switch.

f. Install the new track zero switch and the PCB.

g. Provide the track zero switch adjustment.



4.3.3.6. HEAD CARRIAGE REPLACEMENT

a. Remove mini disk drive from mounting and place it on a clean working surface.

b. Disconnect P2.

c. Disengage the spring.

d. Loosen the two holding screws and take carefully out the carriage with the guide bars.

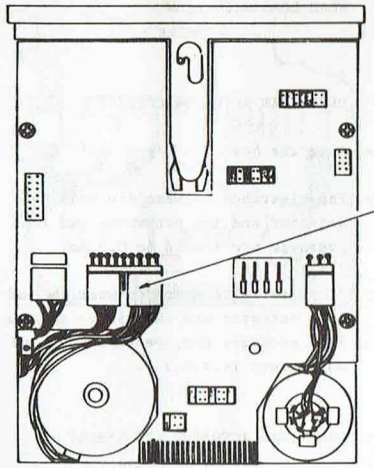
e. Pull out the guide bars from the R/W head carriage.

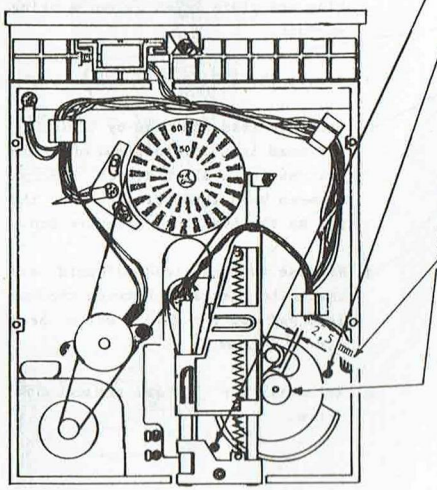
f. To reinstall the new head carriage reverse the above procedure.

Caution: Handle spring carefully during reinstalling

g. Provide the track adjustment accordingly (4.4.3.2).

h. Check the track zero switch adjustment (4.4.3.3.).





4.3.3.7. STEPPER MOTOR REPLACEMENT

(Only applicable with Alu- Spiral-Cam).

a. Remove mini disk drive from mounting and place it on a clean working surface.

b. Disconnect P4

c. Loosen the spiral wheel setsrew.

d. Loosen the stepper motor holding screws and remove the stepper motor.

e. To reinstall the new stepper motor reverse the above procedure.

f. Monitor TRACK 0

SYNC	:	AUTO
CH 1	:	2V/DIV TJ2-6
MODE	:	CH 1 ONLY
TIME BASE	:	10 msec / DIV

g. Step out to track 0.

h. Step to track 36

i. Provide the track adjustment accordingly (4.4.3.2.).

4.3.3.8. SPIRAL WHEEL REPLACEMENT

(Only applicable with Alu-Spiral-Cam).

a. Remove the stepper motor (see 4.4.3.7.).

b. Remove the spiral wheel.

c. Reinstall the stepper motor and the new spiral wheel.

d. Continue with point f. of the stepper motor replacement procedure (4.4.3.7.).

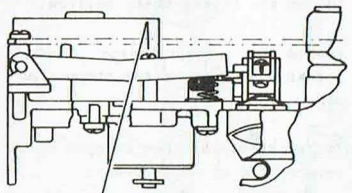
4.3.4. HEAD LOAD MECHANISM

4.3.4.1. HEAD LOAD ACTUATOR CHECK

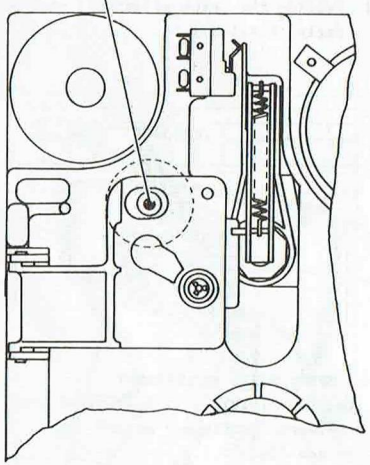
a. Load the head

b. The clearance between the head load actuator and the pin on the head load pressure arm should be 0,5 mm.

c. If there is no space between the head load actuator and the pin on the head load pressure arm, perform head load adjustment (4.4.4.2.).



SETSCREW



4.3.4.2. HEAD LOAD ACTUATOR ADJUSTMENT

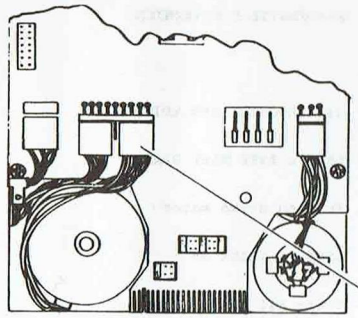
a. Remove the mini disk drive from mounting and place it on a clean working surface.

b. Remove the PCB(see 4.4.1.1.).

c. Manuelly load the head by pulling the head load solenoid and adjust the setcrew for a clearance of 0,5 mm between head load actuator and the pin on the head load pressure arm.

d. Release the head load solenoid and check the clearance between the head load pad and the read / write head for 4 ÷ 5 mm.

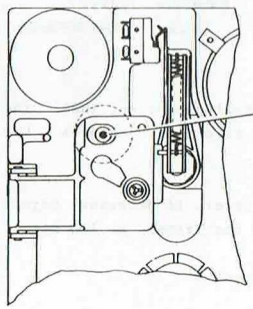
e. Reinstall the PCB and the mini disk drive.



4.3.4.3. HEAD LOAD SOLENOID REPLACEMENT

a. Remove mini disk drive from mounting and place it on a clean working surface.

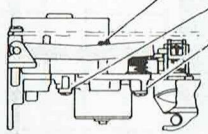
b. Extract wire 1 and 3 from connector P3.

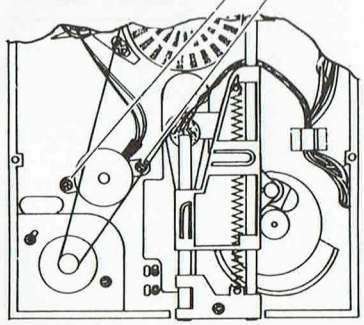


c. Remove the screw on the head load actuator.

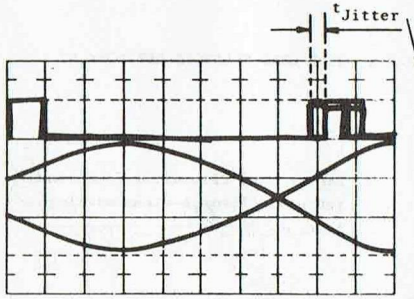
d. Loosen the two holding screws and remove the head load solenoid.

e. To reinstall the head load solenoid reverse the above.

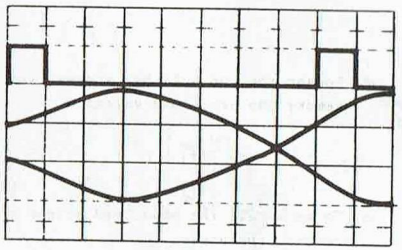




4.3.5. READ/WRITE ELECTRONICS



Before Adjustment



4.3.5.1 JITTER CHECK AND ADJUSTMENT

a. Load a BASF Mini Disk

b. Turn on drive motor

c. Step to track 39

d. Write all " ones "

e. Measure with oscilloscope

SYNC INT. POS. CH1

CH1 AC 200mV/div TJ1-7
CH2 DC 2V/div 1D-9 READDATA

f. Trigger Oscilloscope so, that the read data signal as " cateyes " are displayed.

g. Measure jitter. If necessary adjust poti R 69 for jitter $\measuredangle$ 100 nsec.

h. Step to track 0

i. Check for jitter $\leq$ 500 nsec
If this value is exceeded replace the R/W- Control PCB

4.3.6 PHOTO TRANSISTORS AND LED's.

4.3.6.1. PHOTO TRANSISTOR REPLACEMENT

a. Disconnect plug of defect photo transistor.

b. Remove photo transistor

c. Insert new photo transistor

d. Reconnect plug

e. Check the function of the photo transistor

d. Provide the Index detector adjustment, if the Index photo transistor have been changed.

4.3.6.2 LED - Replacement

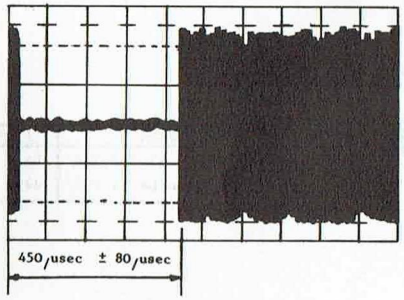
a. Solder out the LED

b. Put in the new LED

c. Check the function of the LED

d. Provide the index detector adjustment if the Index LED have been changed.

4.3.6.3. INDEX DETECTOR ADJUSTMENT CHECK



a. Load a BASF - CE mini disk

b. Start the drive motor and select the mini disk drive

c. Step to track 0

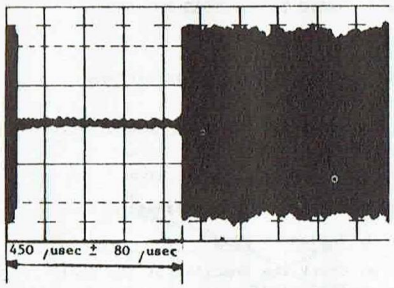
d. Measure with oscilloscope:

SYNC : EXT. POS. TJ2-8

CH1 : AC 100 mV inverted TJ1-7
CH2 : AC 100 mV TJ1-9
MODE : ADD
TIME
BASE : 100 µsec / Div

e. Check the timing between start of the sweep and the data burst for 450 µsec ± 80 µsec

f. Provide the index detector adjustment (4.4.6.4.) if necessary.



4.3.6.4. INDEX DETECTOR ADJUSTMENT

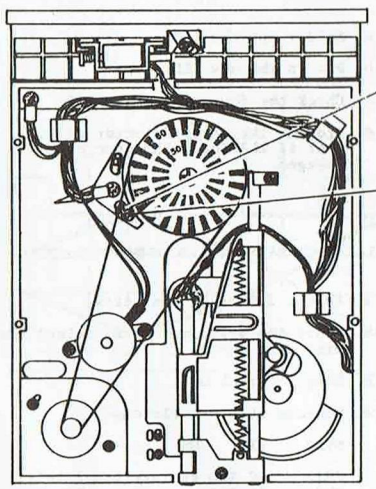
a. Load a BASF - CE Mini Disk

b. Start the drive motor and select the mini disk drive-

c. Step to track 0

d. Messure with oscilloscope:

SYNC	:	EXT. POS. TJ2-8 INDEX
CH 1	:	AC 100 mV inverted TJ1-7
CH 2	:	AC 100 mV TJ1-9
MODE	:	100 µsec /Div.
TIME BASE	:	100 µsec / Div.

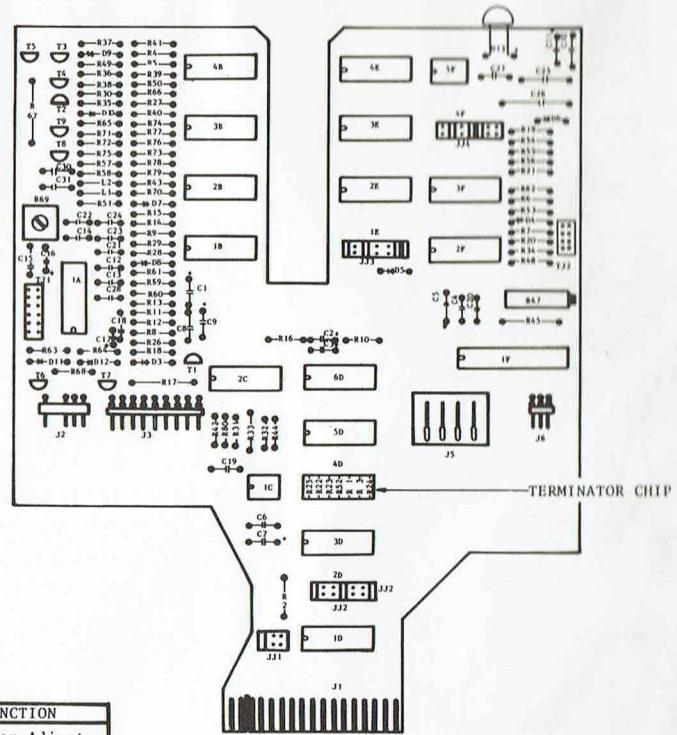


e. Loosen the set screw of the index - holder

f. Adjust the time delay between start of the sweep and the data burst to 450 µsec ± 80 µsec.

g. Tighten the index holder set screw.

4.4. LOCATION OF TESTPOINTS, IC's, POTENTIOMETERS AND CONNECTORS



POTI	FUNCTION
R 47	Drive Motor Adjust
R 69	Jitter Adjust

Connector		Function
J1		Signal - Interface
J2		Read/Write - Head
J3	1,3	Head Load Solenoid
	2,4	Door Lock Solenoid
	5,6	Write Protect Phototransistor
	7,8	Index Phototransistor
	11-18	Stepper Motor
J5		DC- Connector
J6	2,4	Drive Motor
	3,5,6	Track Zero Switch

Test Points		Signal
TJ1	1,2	Write Current Signal
	3,5	Read Signal (Preamp. Output)
	6	GND
	7,9	Read Signal (Differentiator Input)
	8	Jitter Voltage
	10	Erase Current T.P.
	11,12	Write Current T.P.
TJ2	1	DISK CHANGE FF/
	2	PWRONRESET/
	3	N.O. TRACK ZERO SWITCH
	4	IN USE- FF
	5	MOTOR ON
	6	TRACK 00
	7	GND
	8	INDEX

APPENDIX C

MMPS-1 POWER SUPPLY MANUAL

M68MMPS1(D1)
JANUARY 1979

M68MMPS1-1
POWER SUPPLY

First Edition

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

POWER SUPPLY

INTRODUCTION

This manual provides information on the power supply that can be used in Micromodule and EXORciser systems. A schematic is supplied for each model. A cable is supplied for connection to the motherboard.

GENERAL DESCRIPTION

The power supply will operate on 110 or 220 VAC input. This capability is provided by a jumper arrangement on TB1. Overload protection and power fail regulation are provided on all DC outputs. Over-voltage protection is also provided on the 5 VDC output. Calibration pots allow the outputs and the over-voltage protection to be adjusted. Table 1 lists the specifications for the power supply.

TABLE 1. Power Supply Specifications

CHARACTERISTIC	SPECIFICATION
Input Voltage	95 to 125/205 to 250 VAC 47 to 420 Hz Single Phase
Output Voltage	+5 VDC ± 0.1%, 15 Amp., 2 mV RMS ripple -12 VDC ± 0.1%, 1.5 Amp., 1 mV RMS ripple +12 VDC ± 0.1%, 2.5 Amp., 1 mV RMS ripple 8 VAC, 0.1 Amp. (not used in this application)
Calibration Range	5 VDC - ± 0.5 VDC 12 VDC - ± 1.0 VDC
Over-Voltage Protection	5 VDC output - output rise to 7 volts reduced to 5 volts or less within 50 µsec.
Power Fail (Turn on/turn off transients)	5 VDC output: +7.0 V (max) -0.5 V (max) +12 VDC output: +17.0 V (max) -0.3 V (max)
Remote Sense	5 VDC output - compensate up to 0.5 VDC drop.
Operating Temperature	0 to 70° C - 70% derating between 50 and 70° C.
Dimensions	
Length	9.5 inches
Width	6.25 inches
Height	5.0 inches

As shown in Figure 1, the input terminals are push-on type, and the output is a 12-pin connector. The schematic diagrams for Power-One Model and for the Motorola Model are illustrated in Figures 2 and 3, respectively.

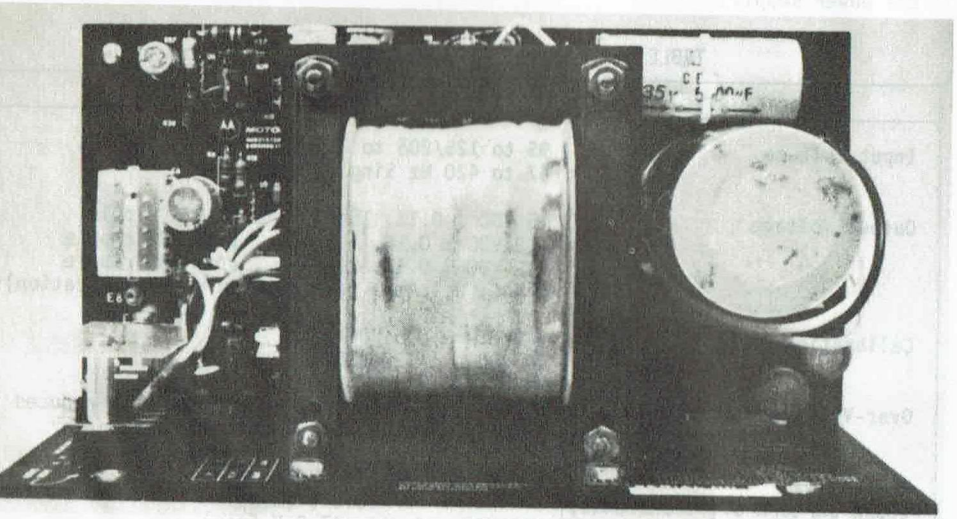


FIGURE 1. M68MMPS1-1 Power Supply

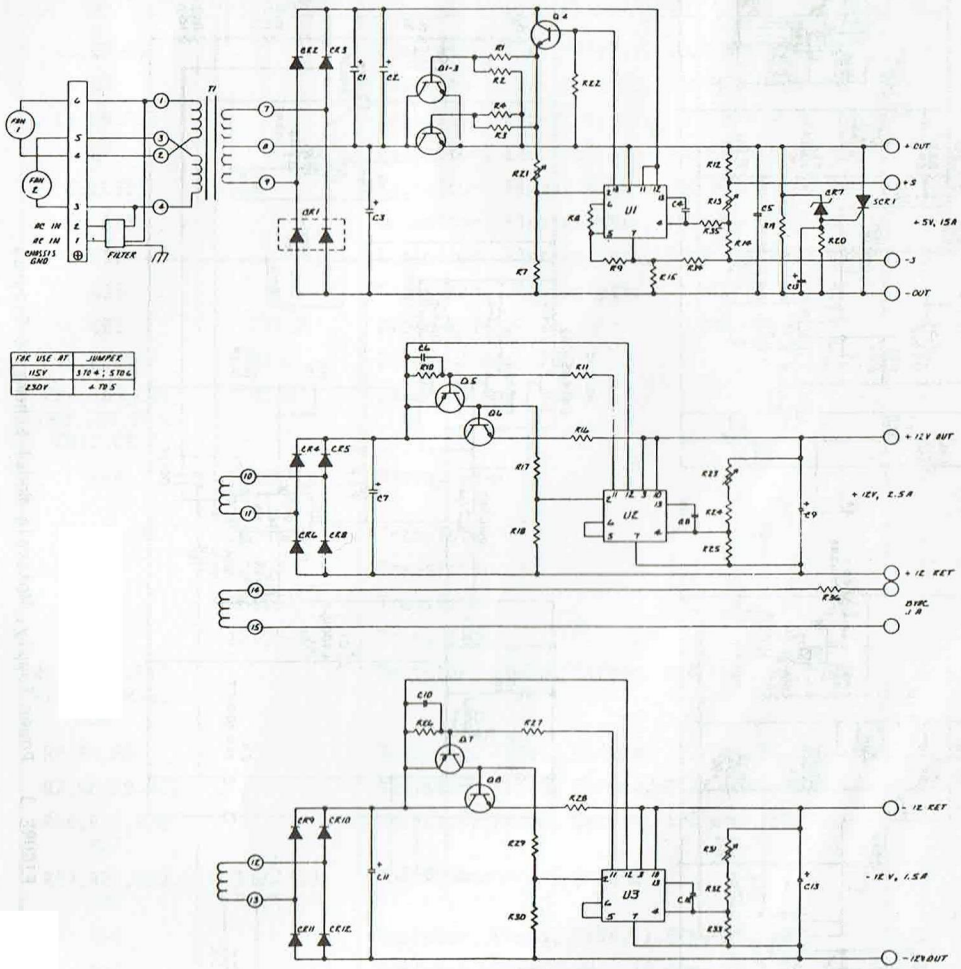


FIGURE 2. Power Supply, Power-One Model Schematic Diagram

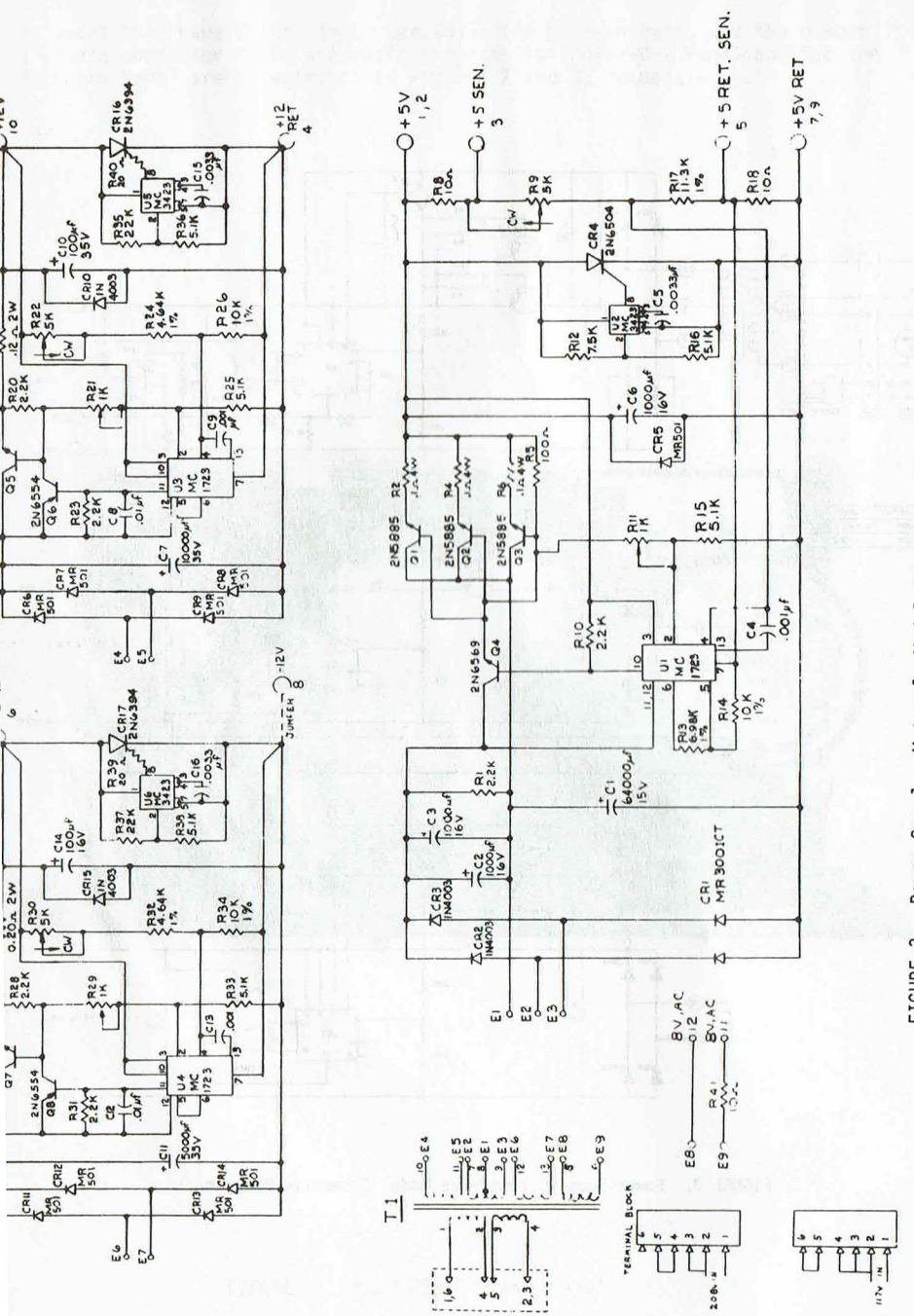


FIGURE 3. Power Supply, Motorola Model Schematic Diagram

This paragraph provides the parts lists for the power supply. These parts lists reflect the latest issue of hardware at the time of printing:

TABLE 2. Power-One Power Supply Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFECTIVITY
C1,C2,C5		Capacitor, Electrolytic, 1000 MFD @ 16 VDC	L
C3		Capacitor, Electrolytic, 64K MFD @ 15 VDC	L
C4,C6,C10		Capacitor, Fixed, Mylar, .001 MFD @ 100 VDC	L
C7		Capacitor, Electrolytic, 7300 MFD @ 35 VDC	L
C8,C12		Capacitor, Fixed, Mylar, .01 MFD @ 100 VDC	L
C9,C13		Capacitor, Electrolytic, 100 MFD @ 35 VDC	L
C11		Capacitor, Electrolytic, 3300 MFD @ 35 VDC	L
C13		Capacitor, Electrolytic, .1 MFD at 50 VDC	L
CR1	R711A	Diode Bridge	L
CR2,CR3	AE1C	Diode, 1 Amp, 200 V	L
CR4,CR5,CR6, CR8,CR9,CR10, CR11,CR12	AE3B	Diode, 3 Amp, 100 V	L
CR7	IN968A or IN753A	Diode, Zener	L
Q1,Q2,Q3	12505-2	Transistor	L
Q4	12500-5	Transistor	L
Q5,Q7	2N6554	Transistor	L
Q6,Q8	12505-3	Transistor	L
R1,R3,R5,R12, R15,R34,R35, R36		Resistor, Fixed, Carbon, 6.8 ohm, 5%, ½W	L
R2,R4,R6		Resistor, Fixed, Carbon, 22 ohm, 5%, ½W	L
R7,R8,R9,R22		Resistor, Fixed, Carbon, 2.2K ohm, 5%, ½W	L
R10,R11,R26 R27		Resistor, Fixed, Carbon, 180 ohm, 5%, ½W	L
R13,R21,R23, R31	BE54719 (CTS)	Potentiometer, 1.5K ohm	L
R14		Resistor, Fixed, Film, 1.62K, 2%, ¼W	L
R16		Resistor, Fixed, WW, .12 ohm, 2W	L
R17,R29		Resistor, Fixed, Carbon, 270 ohm, 5%, ½W	L
R18,R30		Resistor, Fixed, Carbon, 4.7K ohm, 5%, ½W	L

TABLE 2. Power-One Power Supply Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
R19,R20		Resistor, Fixed, Carbon, 47 ohm, 5%, ½W	L
R24,R32		Resistor, Fixed, Film, 1.2K ohm, 2%, ¼W	L
R25,R33		Resistor, Fixed, Film, 2.2K ohm, 2%, ¼W	L
R28		Resistor, Fixed, WW, .22 ohm, 2W	L
SCR1	SD315L	Silicon Controlled Rectifier	L
T1	13402	Transformer, Power	L
U1,U2,U3	Ua723	Voltage Regulator	L

TABLE 3. Motorola Power Supply Parts List

REFERENCE ESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
C1	21ATH0081A001	Capacitor, Electrolytic, 64K MFD @ 15 VDC
C2,C3,C6		Capacitor, Electrolytic, 1000 MFD @ 16 VDC
C4,C9,C13		Capacitor, Fixed, Mylar, .001 MFD @ 100 VDC
C5,C15,C16		Capacitor, Fixed, Ceramic, .0033 MFD @ 50 VDC
C7		Capacitor, Electrolytic, 10K MFD @ 35 VDC
C8,C12		Capacitor, Fixed, Ceramic, .01 MFD @ 50 VDC
C10		Capacitor, Electrolytic, 100 MFD @ 35 VDC
C11		Capacitor, Electrolytic, 5000 MFD @ 35 VDC
C14		Capacitor, Electrolytic, 100 MFD @ 16 VDC
CR1	MR300ICT	Diode Bridge
CR2,CR3 CR10,CR15	IN4003	Diode, Rectifier, 1 Amp, 200 V
CR4	2N6405	SCR, 16 Amp, 800 V
R5,CR6,CR7 R8,CR9,CR11, 12,CR13,CR14	MR501	Diode, Rectifier, 3 Amp, 100 V
CR16,CR17	2N6394	SCR, 12 Amp, 50 V
Q1,Q2,Q3	2N5885	Transistor, Power, 60 V, 200 W
Q4,Q5,Q7	2N6569	Transistor, Power
Q6,Q8	2N6554	Transistor, Power
1,R10,R20 23,R28,R31		Resistor, Fixed, Carbon, 2.2K ohm, 5%, ½W
R2,R4,R6		Resistor, Fixed, WW, 0.1 ohm, 4W
R5		Resistor, Fixed, Carbon, 100 ohm, 5%, ½W
8,R18,R41		Resistor, Fixed, Carbon, 10 ohm, 5%, ½W

TABLE 3. Motorola Power Supply Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R9,R22,R30		Potentiometer, 5K ohm
R11,R21,R29		Potentiometer, 1K ohm
R12		Resistor, Fixed, Carbon, 7.5K ohm, 5%, ½W
R13		Resistor, Fixed, Film, 6.95K ohm, 1%, ½W
R14,R26,R34		Resistor, Fixed, Film, 10K ohm, 1%, ½W
R15,R16,R25, R33,R36,R38		Resistor, Fixed, Carbon, 5.1K ohm, 5%, ½W
R17		Resistor, Fixed, Film, 11.3K ohm, 1%, ½W
R24,R32		Resistor, Fixed, Film, 4.64K ohm, 1%, ½W
R27		Resistor, Fixed, Carbon, 0.20 ohm, 5%, 1W
R35,R37		Resistor, Fixed, Carbon, 22K ohm, 5%, ½W
R39,R40		Resistor, Fixed, Carbon, 20 ohm, 5%, ½W
T1	24TH03146A001	Transformer, Power
U1,U3,U4	MC1723	Voltage Regulator
U2,U4,U6	MC3423	Overvoltage Sensing Circuit

TABLE 4. Power Supply Cable Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
J1	15NW9806A30	Housing, Connector, 10 Contact, Positive Lock	K
J2	15NW9806A97	Housing, Connector, 12 Contact, Positive Lock	K
	29NW9805A87	Contact, Socket, 20-14 AWG (20 required; use in J1 and J2)	K
	29NW9805A51	Contact, Socket, 20-14 AWG (Alternate)	K
	29NW9805A77	Terminal, Ring, Vinyl Insulated, 22-16 AWG (1 required)	K

APPENDIX D

ASCII CHARACTER SET

BITS 4 TO 6 ---------->	0	1	2	3	4	5	6	7
	0	NUL	DLE	SP	0	@	P	`	p
	1	SOH	DC1	!	1	A	Q	a	q
	2	STX	DC2	"	2	B	R	b	r
	3	ETX	DC3	#	3	C	S	c	s
	4	EOT	DC4	$	4	D	T	d	t
	5	ENQ	NAK	%	5	E	U	e	u
	6	ACK	SYN	&	6	F	V	f	v
BITS 0 TO 3	7	BEL	ETB	'	7	G	W	g	w
	8	BS	CAN	(	8	H	X	h	x
	9	HT	EM	)	9	I	Y	i	y
	A	LF	SUB	*	:	J	Z	j	z
	B	VT	ESC	+	;	K	[	k	{
	C	FF	FS	,	<	L	\	l	|
	D	CR	GS	-	=	M	]	m	}
	E	SO	RS	.	>	N	^	n	~
	F	SI	US	/	?	O	_	o	DEL