Dansk Data Elektronik A/S

Non-Operator Diagnostic Programs for the Supermax®

User's Manual
Version 5.6

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1 INTRODUCTION

Diagnostic Programs

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DIAGNOSTIC PROGRAMS

Introduction

All intelligent units in a Supermax computer are supplied with a service port. The service port is an RS 232-C interface modified to support parallel connection between all units.

The Diagnostic Programs run separately in each unit. Consequently it is possible to start programs on all units controlled by one terminal. The main purpose of the Diagnostic Program is to locate a failing unit. If any errors are found the failing unit should be removed from the system and be repaired. It is not the purpose of the Diagnostic Program to specifically point out where on the unit the error was found. An exception from this is the memory test in the CPU Diagnostic Programs, which under certain circumstances is able to point out the failing memory component.

The Diagnostic Programs are available on one diskette, 3½" or 5¼". The diskette contains Diagnostic Programs for all intelligent units in the Supermax. When the diskette is inserted into the floppy disk drive and the computer is reset, the Diagnostic Programs are loaded into the different units. If winchester boot is installed on the Supermax, it is possible to load the Diagnostic Programs from the winchester disk. The Diagnostic Programs can run in two different modes, **Operator Mode** and **Non-Operator Mode**. This depends on whether the Diagnostic Programs are loaded from the floppy disk drive or from the winchester disk. These two modes are described later in this chapter.

Selecting and deselecting units

To ensure that only one service port sends messages to the terminal, only one unit is selected at a given time. All units are deselected upon start of the Diagnostic Programs. To select a specific unit, type one of the two sequences shown below.

<ESC>
#
0 - F *(unit number)*
<CR>

If your terminal has function keys, it is possible to use the keys *F1-F16* to select the 16 units in a system. The function keys must send the following sequence of characters, when activated:

<Ctrl A>
@ - O
<CR>

Unit number 0 is selected by the key *F16* and unit number 1 to F by the keys *F1* to *F15*.

It is not possible to deselect all units by using select sequences. In order to deselect all units in a system, type **ESC** or **Ctrl A**.

If a Service Computer is installed your Supermax, the Service Computer will use so called **POLL** sequences in order to get the current status on all Supermax modules. The **POLL** sequence is shown below.

<ESC>
?
0 - F *(unit number)*
<CR>

If a unit does not respond to the select sequence the cause of the trouble might be one of the following:

- The unit is not installed in the system.
- The unit is not connected to the service port.
- The Diagnostic Program is not loaded into the unit.
- If a Service Computer is installed, it is possible that it is not connected to the service port.
- The unit has failed in a way that makes it unable to run the Diagnostic Program.

Program control

It is possible to control program execution by using some special control characters as mentioned below.

- **Ctrl C.** This is used to cancel a running test. Program execution stops and the prompt will be displayed on the terminal. It only affects the unit currently selected.
- **Ctrl D.** This is used to place the Diagnostic Programs in the **Non-Operator Mode**. It affects all units, whether they are selected or deselected. All units will restart the test. If booted from the floppy disk, the error messages will be displayed on the terminal only. The error message will be shown when a unit is selected. If booted from the winchester disk the programs will run as mentioned under **Non-Operator Mode**.
- **Ctrl E.** If running **Non-Operator Mode**, this is used to stop the **Non-Operator** tests. Program execution stops and all units will be idle. It affects all units in the system, regardless of whether they are selected or not. If not running **Non-Operator Mode**, this is used to soft cancel a peripheral unit test. It only affects the unit currently selected. Refer to the chapters for peripheral test, to see which peripheral tests make use of the soft cancel feature.

- **Ctrl S.** This is used to send an *XOFF* character to the program, which will stop printing on the terminal. If the unit is selected, the program will stop while trying to print on the terminal and an *XON* character must be received to continue. If the unit is deselected, it will remember the *XOFF* character when selected and an *XON* character must be received to continue.
- **Ctrl Q.** This is used to send an *XON* character to the program, which will start printing again. This affects all units whether selected or not.
- **Ctrl N.** This is used to stop printing on the terminal, but program execution continues. If an error is occurred, the error will always be displayed.
- **Ctrl P.** This is used to start printing again after a **Ctrl N** has been pressed.

The **<DEL>** or **<RUB>** key can be used in the following situations:

- **Editing a command line**
  It will delete all inputs in the current command line and issue a new prompt.
- **Editing a number**
  It will select the default number.
- **Editing a text**
  It will select the default text.

Getting started

The following procedure is recommended when using the Diagnostic Programs. Normally a complete test of the system will be started. This is done by booting the Diagnostic Programs and then pressing **Ctrl D**. This will make the units go through a complete test including the bus test. If the test is OK, then the system does not have any

hardware errors and is able to continue normal operation. If the test fails, then the tests should be run manually in order to isolate the failing unit(s).

The first thing to do is to test each unit with the programs only concerning itself. Making sure that all units have successfully completed those tests, the bus test can be started. Start this test *slowly*. Begin by allowing one unit to test the others and observe printout on the terminal. When completed, continue to the next unit, repeating the process, and continue so on until the procedure is completed for all units. Then the Supermax is ready to run again.

Winchester boot

If winchester boot is installed on the system, it is possible to boot the Diagnostic Programs from the winchester also. Refer to the description of the utilities **mkwboot**(1M) and **boot**(1M) in Section 1 of the *System V Reference Manual*. The boot sector information is located on the physical winchester disk in address 0x300 to 0x3FF.

Operator Mode

The Diagnostic Programs will, when booted from the floppy disk, enter the **Operator Mode**. All units will be idle until an operator types the select sequence of a unit on the terminal connected to the service port. The unit will respond by writing a prompt on the terminal, indicating that it is ready to take input from the terminal. Now the operator is able to start the tests corresponding to the selected unit. When the Diagnostic Programs are running in **Operator Mode**, it is possible to enter the **Non-Operator Mode**.

Non-Operator Mode

The Diagnostic Programs will, when booted from the winchester disk, enter the **Non-Operator Mode**. All units will automatically perform an internal test and a bus test involving all units in the system. Each unit will stop, when locating any errors. Upon completion of the test, the **Non-Operator** error buffer will be updated, and the computer will be reset.

Service Computer

If a Service Computer is installed in the Supermax, the access to the service port is made through the Service Computer. When loading the Diagnostic Programs, the master DIOC will display the version of the Diagnostic Programs and information about all modules in the Supermax system. This information will always be displayed on the terminal.

In order to run the Diagnostic Programs from the service port terminal, a logical connection between the Service Computer and the service port must be established. First login to the Service Computer and then issue the **tty** command. When the connection is made, it is possible to communicate with the Supermax modules running the Diagnostic Programs. Refer to a detailed description of the Service Computer in "Supermax Service Computer Users Manual" stock no. 94026911.

NOTE

If no characters are received from the Supermax modules in appx. 60 second, the Service Computer will automatically start sending **POLL** commands to the Supermax modules, resulting in a deselection of all modules. If you do not want to be disturbed by the **POLL** command, issue the **tty** command with the **-off** option.

2 NON-OPERATOR MODE

Non-Operator Mode

NON-OPERATOR MODE

Introduction

The Diagnostic Programs will, when booted from the winchester disk, enter the **Non-Operator Mode**. All units will automatically perform an internal test and a bus test involving all units in the system. Each unit will stop, when locating any errors. Upon completion of the test, the **Non-Operator** error buffer will be updated, and the computer will be reset.

Start/Cancel Non-Operator Mode

In order to start the **Non-Operator** test, press **Ctrl D**. It affects all units, whether they are selected or deselected. All units will restart the test.

In order to cancel the **Non-Operator** test, type **Ctrl E**. All units will stop the test.

How does it work

When in **Non-Operator Mode** the units will run in two different modes, **Master** or **Slave**.

Master The Master unit is the DIOC which has booted the Diagnostic Programs from the floppy disk or the winchester disk. The Master unit controls all other units by activating or deactivating the **Error In Unit Line (EIUL)** in the Supermax I/O bus. It also takes care of calculating the internal test time and the bus test time. If the Diagnostic Programs are booted from the winchester disk, the DIOC will save the test results on the winchester.

Slave Slave units are all other units apart from the Master unit. All Slave units are controlled by the Master unit. When the Master unit activates the **EIUL**, all units go into a *status mode* and all Slave units will write status information to the Master unit. When the Master unit deactivates the **EIUL**, all units go into a *test mode* and they will continue the test.

Step	Unit	Description
1	Master	Activate the **EIUL** and load a timeout counter.
2	Master	Set the boot pointer to the temporary boot pointer on the winchester disk and get the test time from the Non-Operator sector on the winchester.[2)]
3	Master/Slave	Calculate internal test time and bus test time.
4	Master/Slave	Write status and calculated test time to the Master unit.
5	Master/Slave	Wait for all units to write status to the Master unit.[2)]
6	Master	Calculate default test time. Deactivate the **EIUL** and load the timer with internal test time.
7	Master/Slave	Running internal test and winchester test.

Table 2-1-1: Non-Operator Mode running (1 of 3)

Step	Unit	Description
8	Master	When the time has passed the master will activate the **EIUL** and load a timeout counter.
9	Master/Slave	Write internal test status to the Master unit and initialize bus test as a passive unit.
10	Master/Slave	Wait for all units to write status to the Master unit.[1)]
11	Master	Deactivate the **EIUL** and load the timer with bus test time.
12	Master/Slave	Running active bus test.
13	Master	When the time has passed the master will activate the **EIUL** and load a timeout counter.
14	Master/Slave	Write bus test status to the Master unit.
15	Master/Slave	Wait for all units to write status to the Master unit.[1)]
16	Master	Set the boot pointer to the temporary boot pointer and save the default test time and test results on the winchester.[2)]
17	Master/Slave	Cancel the Non-Operator Mode.
18	Master/Slave	Reset the Supermax.[2)]

Table 2-1-1: Non-Operator Mode running (2 of 3)

Step	Unit	Description
19	Master	Wait to be selected. Write status OK or FAIL.
20	Master	Deactivate the **EIUL**

Table 2-1-1: Non-Operator Mode running (3 of 3)

1) In step 1 the timeout time set to 10 min. In step 8 and 13 the timeout time set to 2 min. If timeout occurs the Master unit goes to step 16.

2) Only used if the Master unit is booted from the winchester.

Internal test time and bus test time

The time used by the Diagnostic Programs when testing in **Non-Operator Mode** can be selected in two ways. It is possible to use the default time on internal test and bus test. In that case all units will automatically go through at least one pass of their internal test, and after that at least one pass of the bus test, involving all units in the system. A table of the default values for internal test time and bus test time can be found in "Chapter 2 – 4 Test times". It is also possible to specify the time manually and thereby setting a time for the internal test and a time for the bus test. This is done in the following way:

- Select the Master unit and press **Ctrl C**.
- Select the entry **"Set test time for Non-Operator Mode"**.
- Set the time.
- Press **Ctrl D** to start **Non-Operator** test.

If you select the Master unit when running **Non-Operator** test, the time, still remaining of the test, will be displayed.

When starting **Non-Operator** from winchester disk, the test time, will be loaded from **Non-Operator** status buffer on the disk. The test times are located on physical address 0x530 to 0x537 on the disk. If you want to setup specified test time, instead of default times, you must modify the test times in the **Non-Operator** status buffer. Before doing that, the buffer must content the valid text string.

Tests for Non-Operator Mode

When running **Non-Operator test** the test is running two different tests, internal test and bus test. The internal test always uses the entry **"Test all"** on all Supermax modules and the bus test runs all units against all units.
It is possible to run CRC test or verify mirrored disks, on winchester disks mounted on DIOC3 modules. It is also possible to select internal loopback/external loopback on MIOC submodules. This is done by selecting the Master unit and select the entry **"Set tests for Non-Operator Mode"**.[1)]

When starting **Non-Operator** from winchester disk, the test type will be loaded from the **Non-Operator** status buffer on the disk. The test type is located in physical address 0x508 to 0x50B on the disk. Winchester disks mounted on a DIOC3, will always be tested with CRC test, when starting **Non-Operator** from winchester disk.

Error when running Non-Operator Mode

Each unit will stop, when locating any errors and upon completion of the test, the error status will be written on the winchester disk.[2)] During this **Non-Operator** test it is possible to select the units from a terminal connected to the service port, and thereby see the test running. If a unit has discovered an error, it will be displayed on the terminal as well as written on the winchester disk.[2)]

1) Only DIOC3 will support this setup.

2) Only if winchester boot.

Running Non-Operator Mode from the Supermax Operating System

When running the **Supermax Operating System**, it is possible to start the **Non-operator** test and after completion see the result of the test. This is done by using the following utilities which are described in Section 1 of the *System V Reference Manual*.

mkwboot Used to install winchester boot on the system.

hwstatus Used to interpret the test results. Also used to set the test times on the winchester disk and to specify whether to use these settings or to use the default settings.

init Used to change the state of the system. **init 5** will reboot the system with the Diagnostic Programs. Refer to **Appendix A** to see the installation procedure.

Status buffer

The Non-Operator status buffer contains information about the result of the **Non-Operator** test. The status buffer is located on the physical winchester disk address 0x400 to 0x5FF. The utility **hwstatus** is used to interpret the status buffer. The example on the following page shows how the status buffer from the **Non-Operator** Diagnostic Programs may look after a test has been successfully completed. It also shows, that a default internal test time and a bus test time of 64 minutes has been used and that the Ethernet and ISDN submodules on the MIOC has been tested with external loopback.

A detailed description of the content of the error buffer and Supermax module type can be found in "Chapter 2 – 2 Error buffer" and "Chapter 2 – 3 Supermax module type".

```
      0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
400   A1 00 70 00 00 00 00 00 00 00 00 02 00 00 00 0D  ..p.............
410   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
420   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
430   A1 00 70 00 00 00 00 00 00 00 00 02 00 00 00 0D  ..p.............
440   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
450   A1 00 60 00 00 00 00 00 00 00 00 02 00 00 00 06  ..'.............
460   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
470   A1 00 80 00 00 00 00 00 00 00 00 02 00 00 00 0A  ................
480   A1 00 20 00 00 00 00 00 00 00 00 02 00 00 00 02  .. .............
490   A1 00 C0 00 00 00 00 00 00 00 00 02 00 00 00 02  ................
4A0   A1 00 30 00 00 00 00 00 00 00 00 02 00 00 00 02  ..0.............
4B0   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
4C0   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
4D0   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
4E0   A1 00 50 00 00 00 00 00 00 00 00 02 00 00 00 02  ..P.............
4F0   A1 00 40 00 00 00 00 00 00 00 00 02 00 00 00 02  ..@.............
500   4E 4F 4D 2D 53 54 41 54 00 00 00 01 00 00 00 00  NOM-STAT........
510   35 2E 31 20 20 20 20 20 39 32 2E 31 32 2E 30 31  5.1     92.12.01
520   07 00 00 07 00 06 00 08 02 00 03 00 00 00 05 04  ................
530   FF FF FF FF 00 00 00 40 00 00 00 0D 00 00 00 10  ................
540   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
550   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
560   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
570   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
580   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
590   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
5A0   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
5B0   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
5C0   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
5D0   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
5E0   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
5F0   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
```

Figure 2-1-1: Non-Operator status buffer

Address	Content
0x400-0x4FF	Error buffer for all units. Each unit occupies 16 bytes in the error buffer. The buffer for unit number 0 starts in address 0x400, unit number 1 starts in 0x410, and so on.
0x500-0x507	This text string indicates to the Diagnostic Program that the addresses from 0x500 to 0x5FF are valid.
0x508-0x50B	Test field for the Diagnostic Programs. Bit(0) = External loopback on all MIOC (TERM, HDLC) submodules. Bit(1) = External loopback on all MIOC (Ethernet, ISDN) submodules. Bit(3) = Verify mirrored disks connected to DIOC3 modules.
0x50C-0x50F	Status field for the utility **hwstatus**
0x510-0x517	Version of the Diagnostic Programs.
0x518-0x51F	Date of the Diagnostic Programs.
0x520-0x52F	Supermax module type table.
0x530-0x533	Internal test time. If 0xFFFFFFFF, then the default internal test time is used.
0x534-0x537	Bus test time. If 0xFFFFFFFF, then the default bus test time is used.
0x538-0x53B	Default time for internal test calculated by the Master unit.
0x53C-0x53F	Default time for bus test calculated by the Master unit.
0x540-0x5FF	Not used.

Table 2-1-2: Non-Operator status buffer

NON-OPERATOR MODE

Error buffer

On the following pages a description of the content of the Non-Operator error buffer is shown for each of the units, that might be in a system. Refer to "Chapter 2-1 Non-Operator Mode", to see the description of the Non-Operator status buffer.

Address	Name	Content
0x00	TSTAT	Test status
0x01	ERCD	Error code
0x02	TEST	Test code
0x03	SCODE	Special status
0x04 - 0x07	ADD(3 - 0)	Error address
0x08 - 0x0B	WDT(3 - 0)	Write data
0x0C - 0x0F	RDT(3 - 0)	Read data

Table 2-2-1: Non-Operator error buffer

TSTAT value	Description
0xFF	Fatal error
0xE4	Error in internal test
0xE2	Error in bus test
0xE1	Error in peripheral test
0xA4	Internal test
0xA2	Bus test
0xA1	Test ended OK

Table 2-2-2: Test status for Non-Operator

Value	Description
0x10	No tests.
0x11	Test RAM. High speed.
0x12	Test RAM. Bit test.
0x13	Test RAM. Address bit test.
0x14	Test RAM. Galloping ones and zeroes.
0x15	Test RAM. Byte write.
0x16	Test RAM. Read modify write.
0x17	Test MMU memory.
0x18	Test MMU adder.
0x19	Test ASN register.
0x1A	Test MMU ASN con SEG.
0x1B	Test MMU comparator.
0x1C	Test interrupts.
0x1D	Bus test.

Table 2-2-3: Test codes for CPU 68000

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x01	EAR	SYN(15-0)	–	–	Single bit error in memory
0x10	–	Address	Write	Read	Error in high speed test
0x11	–	Address	Write	Read	Error in bit test
0x12	–	Address	Write	Read	Error in address bit test
0x13	–	Address	Write	Read	Error in galloping test
0x14	–	Address	Write	Read	Error in byte write test
0x15	–	Address	Write	Read	Error in R – M – W test
0x30	–	–	–	–	Error in ASR test
0x31	–	Address	Write	Read	Error in MMU init test
0x32	–	–	–	–	Error in MMU adder test
0x33	–	–	–	–	Error in ASN – SEG test
0x34	–	–	–	–	Error in comparator test
0x40	–	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x42	–	–	–	–	Wrong interrupt level
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte

Table 2-2-4: Error codes for CPU 68000 (1 of 2)

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x77	Unit no	I/O add	–	–	TAS did not change byte
0x78	Unit no	I/O add	–	–	Byte was set before TAS
0x79	Unit no	I/O add	Write	Read	Error in bus test
0xE0	Unit no	STATUS	–	–	Bus error
0xF0	–	–	–	–	Address error

Table 2-2-4: Error codes for CPU 68000 (2 of 2)

Value	Description
0x20	No tests.
0x21	Test memory 0x4000 to 0xF000.
0x22	Test memory mapper.
0x23	Test timer interrupt.
0x24	Bus test.

Table 2-2-5: Test codes for SIOC1

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x10	–	Address	Write	Read	Memory error
0x30	–	Map add	Write	Read	Memory mapper error
0x40	Int. level	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x79	Unit no	I/O add	Write	Read	Error in bus test
0xE0	ESR	Unit no	–	–	Error occurred. ESR = XX

Table 2-2-6: Error codes for SIOC1

Value	Description
0x30	No tests.
0x31	Test memory 0xA000 to 0xF000.
0x32	Test memory mapper.
0x33	Test timer interrupt.
0x34	Bus test.
0x35	Test DMA.
0x36	Test peripheral interface.

Table 2-2-7: Test codes for DIOC1

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x10	–	Address	Write	Read	Memory error
0x30	–	Map add	Write	Read	Memory mapper error
0x40	Int. level	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x79	Unit no	I/O add	Write	Read	Error in bus test
0x7A	Unit no	I/O add	Write	Read	Error in bus test, BTU access
0x80	–	–	–	–	Error in SCSI interface
0x81	–	–	–	–	Error in Streamer interface
0x82	–	–	–	–	Error in Floppy interface
0x83	–	–	–	–	Error in DMA
0xE0	ESR	Unit no	–	–	Error occurred. ESR = XX

Table 2-2-8: Error codes for DIOC1

Value	Description
0x40	No tests.
0x41	Test memory 0x4000 to 0xF000.
0x42	Test memory mapper.
0x43	Test timer interrupt.
0x44	Bus test.
0x45	Test DMA and memory move.

Table 2-2-9: Test codes for CIOC

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x10	–	Address	Write	Read	Memory error
0x30	–	Map add	Write	Read	Memory mapper error
0x40	Int. level	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x79	Unit no	I/O add	Write	Read	Error in bus test
0x7A	Unit no	I/O add	Write	Read	Error in bus test, BTU access
0xE0	ESR	Unit no	–	–	Error occurred. ESR = XX

Table 2-2-10: Error codes for CIOC

Value	Description
0x50	No tests.
0x51	Test memory.
0x52	Test memory mapper.
0x53	Test DMA memory.
0x54	Test bus interrupt, and timer interrupt.
0x55	Test peripheral interface.
0x56	Bus test.

Table 2-2-11: Test codes for DIOC2

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x10	X (ASCII)	Address	Write	Read	Memory error bank X
0x11	X (ASCII)	Address	Write	Read	DMA memory error bank X
0x30	–	Map add	Write	Read	Memory mapper error
0x40	Int. level	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x42	–	–	–	–	Error in bus interrupt
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x79	Unit no	I/O add	Write	Read	Error in bus test
0x7A	Unit no	I/O add	Write	Read	Error in bus test, BTU bank 0
0x7B	Unit no	I/O add	Write	Read	Error in bus test, BTU bank 1
0x7C	Unit no	I/O add	Write	Read	Error in bus test, BTU bank 2
0x7D	Unit no	I/O add	Write	Read	Error in bus test, BTU bank 3
0x80	–	–	–	–	Error in BTU interface
0x81	–	–	–	–	Error in Tape interface
0x82	–	–	–	–	Error in Floppy interface
0xE0	ESR	Unit no	–	–	Error occurred. ESR = XX

Table 2-2-12: Error codes for DIOC2

Value	Description
0x60	No tests.
0x61	Test main memory.
0x62	Test buffer memory.
0x63	Test MMU memory.
0x65	Test LAN controller without transceiver.
0x66	Test MMU ASN – SEG
0x67	Test MMU size field check.
0x68	Test interrupt.
0x69	Bus test.

Table 2-2-13: Test codes for NIOC/SIOC2

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x10	–	Address	Write	Read	Error in high speed test
0x11	–	Address	Write	Read	Error in bit test
0x12	–	Address	Write	Read	Error in address bit test
0x13	–	Address	Write	Read	Error in galloping test
0x15	–	Address	Write	Read	Error in R – M – W test
0x16	–	–	–	–	Parity error in buffer memory
0x31	–	Address	Write	Read	Error in MMU init test
0x33	–	–	–	–	Error in ASN – SEG test
0x34	–	–	–	–	Error in size field check
0x40	–	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x42	–	–	–	–	Wrong interrupt level
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x77	Unit no	I/O add	–	–	TAS did not change byte
0x78	Unit no	I/O add	–	–	Byte was set before TAS
0x79	Unit no	I/O add	Write	Read	Error in bus test

Table 2-2-14: Error codes for NIOC/SIOC2 (1 of 2)

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0xB0	–	Address	Write	Read	Data error in received buffer
0xB2	–	–	SCB cmd	SCB stt	Time-out during wait for receive unit
0xB3	–	–	SCB cmd	SCB stt	Time-out during command execution
0xB4	–	–	CBL cmd	CBL stt	Command status failed.
0xB5	–	–	–	–	Received frame faulty
0xB6	–	–	SCB cmd	SCB stt	Reset failed
0xB7	-	–	SCB cmd	SCB stt	Time-out during reset
0xB8	–	–	SCB cmd	SCB stt	Time-out during acknowledge to the cont.
0xB9	–	–	SCB cmd	SCB stt	Time-out during wait for command interrupt
0xBA	–	–	CBL cmd	CBL stt	Transmission failed
0xBB	–	–	SCB cmd	SCB stt	Acknowledge to the controller failed
0xE0	Unit no	STATUS	–	–	Bus error
0xF0	–	–	–	–	Address error

Table 2-2-14: Error codes for NIOC/SIOC2 (2 of 2)

Value	Description
0x70	No tests.
0x71	Test RAM. High speed.
0x72	Test RAM. Bit test.
0x73	Test RAM. Address bit test.
0x74	Test RAM. Galloping ones and zeroes.
0x75	Test RAM. Byte write.
0x76	Test RAM. Read modify write.
0x77	Test MMU memory.
0x78	Test MMU adder.
0x79	Test ASN register.
0x7A	Test MMU ASN con SEG.
0x7B	Test MMU comparator.
0x7C	Test interrupts.
0x7D	Bus test.
0x7E	Cache test.

Table 2-2-15: Test codes for CPU 68020

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x01	SYN(7-0)	EAR	–	–	Single bit error in memory
0x10	–	Address	Write	Read	Error in high speed test
0x11	–	Address	Write	Read	Error in bit test
0x12	–	Address	Write	Read	Error in address bit test
0x13	–	Address	Write	Read	Error in galloping test
0x14	–	Address	Write	Read	Error in byte write test
0x15	–	Address	Write	Read	Error in R-M-W test
0x20	–	Address	Write	Read	Error in cache memory
0x21	–	Address	Write	Read	Error in cache test
0x22	–	Address	Write	Read	Error in physical cache test
0x30	–	–	–	–	Error in ASR test
0x31	–	Address	Write	Read	Error in MMU init test
0x32	–	–	–	–	Error in MMU adder test
0x33	–	–	–	–	Error in ASN - SEG test
0x34	–	–	–	–	Error in comparator test
0x40	–	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x42	–	–	–	–	Wrong interrupt level
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte

Table 2-2-16: Error codes for CPU 68020 (1 of 2)

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x77	Unit no	I/O add	–	–	TAS did not change byte
0x78	Unit no	I/O add	–	–	Byte was set before TAS
0x79	Unit no	I/O add	Write	Read	Error in bus test, short access
0x7A	Unit no	I/O add	Write	Read	Error in bus test, long access
0xE0	Unit no	STATUS	–	–	Bus error
0xF0	–	–	–	–	Address error
0xF1	–	–	–	–	Exception error
0xF2	–	–	–	–	Fatal error during boot PROM self test

Table 2-2-16: Error codes for CPU 68020 (2 of 2)

Value	Description
0x90	No tests.
0x91	Test program memory.
0x92	Test cache memory.
0x93	Test SRAM memory.
0x94	Test SRAM mapping.
0x95	Test BTU transport.
0x96	Test interrupts.
0x97	Bus test.
0x98	Winchester test.
0x99	SCSI test.

Table 2-2-17: Test codes for DIOC3

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x10	–	Address	Write	Read	Error in high speed test
0x11	–	Address	Write	Read	Error in bit test
0x12	–	Address	Write	Read	Error in address bit test
0x13	–	Address	Write	Read	Error in galloping test
0x14	–	Address	Write	Read	Error in byte write test
0x15	–	Address	Write	Read	Error in R – M – W test
0x16	SR1	–	–	–	Parity error in cache memory
0x30	–	–	–	–	Error when mapping
0x31	–	Address	Write	Read	Error in SRAM init test
0x40	–	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x42	–	–	–	–	Wrong interrupt level
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x77	Unit no	I/O add	–	–	TAS did not change byte
0x78	Unit no	I/O add	–	–	Byte was set before TAS
0x79	Unit no	I/O add	Write	Read	Error in bus test
0x7A	Unit no	I/O add	Write	Read	Error in bus test, BTU access

Table 2-2-18: Error codes for DIOC3 (1 of 2)

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0xD0	SCSI/ID no	–	–	–	Timeout in reset SCSI
0xD1	SCSI/ID no	Timeout code	–	–	Timeout on SCSI interface
0xD2	SCSI/ID no	–	–	–	Invalid disk parameters
0xD3	SCSI/ID no	Address	Error code	–	Disk drive error
0xE0	Unit no	SR0	–	–	Bus error
0xE1	Unit no	SR1	–	–	BTU bus error
0xF0	–	–	–	–	Address error
0xF1	–	–	–	–	Exception error

Table 2-2-18: Error codes for DIOC3 (2 of 2)

Value	Description
0xA0	No tests.
0xA1	Test RAM. High speed.
0xA2	Test RAM. Bit test.
0xA3	Test RAM. Address bit test.
0xA4	Test RAM. Galloping ones and zeroes.
0xA5	Test RAM. Byte write.
0xA6	Test RAM. Read modify write.
0xA7	Test AMMU memory.
0xA8	Test PMMU memory.
0xA9	Test AMMU mapping.
0xAA	Test PMMU mapping.
0xAB	Test interrupts.
0xAC	Cache test.
0xAD	Bus test.

Table 2-2-19: Test codes for CPU 68030

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x01	SYN(7-0)	EAR	–	–	Single bit error in memory
0x10	–	Address	Write	Read	Error in high speed test
0x11	–	Address	Write	Read	Error in bit test
0x12	–	Address	Write	Read	Error in address bit test
0x13	–	Address	Write	Read	Error in galloping test
0x14	–	Address	Write	Read	Error in byte write test
0x15	–	Address	Write	Read	Error in R – M – W test
0x20	–	Address	Write	Read	Error in cache memory
0x21	–	Address	Write	Read	Error in cache test
0x35	–	Index	–	–	Error when testing AMMU mapping
0x36	–	Index	–	–	Error when testing PMMU mapping
0x40	–	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x42	–	–	–	–	Wrong interrupt level
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x77	Unit no	I/O add	–	–	TAS did not change byte
0x78	Unit no	I/O add	–	–	Byte was set before TAS

Table 2-2-20: Error codes for CPU 68030 (1 of 2)

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x79	Unit no	I/O add	Write	Read	Error in bus test
0x7A	Unit no	I/O add	Write	Read	Error in bus test, Write Bus
0xE0	Unit no	STATUS	–	–	Bus error
0xF0	–	–	–	–	Address error
0xF1	–	–	–	–	Exception error
0xF2	–	–	–	–	Fatal error during boot PROM self test

Table 2-2-20: Error codes for CPU 68030 (2 of 2)

Value	Description
0xB0	No tests.
0xB1	Test RAM. High speed.
0xB2	Test RAM. Bit test.
0xB3	Test RAM. Address bit test.
0xB4	Test RAM. Galloping ones and zeroes.
0xB5	Test RAM. Byte write.
0xB6	Test RAM. Read modify write.
0xB7	Test AMMU memory.
0xB8	Test PMMU memory.
0xB9	Test AMMU mapping.
0xBA	Test PMMU mapping.
0xBB	Test interrupts.
0xBC	Cache test.
0xBD	Bus test.
0xBE	Write Buffer test.
0xBF	Floating Point Accelerator test.

Table 2-2-21: Test codes for CPU R3000

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x01	SYN(7-0)	EAR	–	–	Single bit error in memory
0x10	–	Address	Write	Read	Error in high speed test
0x11	–	Address	Write	Read	Error in bit test
0x12	–	Address	Write	Read	Error in address bit test
0x13	–	Address	Write	Read	Error in galloping test
0x14	–	Address	Write	Read	Error in byte write test
0x15	–	Address	Write	Read	Error in R – M – W test
0x20	–	Address	Write	Read	Error in cache memory
0x21	–	Address	Write	Read	Error in cache test
0x23	–	–	–	–	Cache parity error
0x35	–	Index	–	–	Error when testing AMMU mapping
0x36	–	Index	–	–	Error when testing PMMU mapping
0x37	Test	–	–	–	Error when testing Write Buffer
0x40	–	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x42	–	–	–	–	Wrong interrupt level
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte

Table 2-2-22: Error Codes for CPU R3000 (1 of 2)

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x77	Unit no	I/O add	–	–	TAS did not change byte
0x78	Unit no	I/O add	–	–	Byte was set before TAS
0x79	Unit no	I/O add	Write	Read	Error in bus test
0x7A	Unit no	I/O add	Write	Read	Error in bus test, Write Bus
0x7B	Unit no	I/O add	Write	Read	Error in bus test, special access no. 1
0x7C	Unit no	I/O add	Write	Read	Error in bus test, special access no. 2
0x80	Test	–	–	–	Error when testing FPA
0xE0	Unit no	STATUS	–	–	Bus error
0xF0	–	–	–	–	Address error
0xF1	–	–	–	–	Exception error
0xF2	–	–	–	–	Fatal error during boot PROM self test

Table 2-2-22: Error codes for CPU R3000 (2 of 2)

Value	Description
0xC0	No tests.
0xC1	Test main memory.
0xC2	Test parity circuit.
0xC3	Test hard register.
0xC4	Test interrupts.
0xC5	Bus test.
0xC6	Submodule test.

Table 2-2-23: Test codes for MIOC

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x10	–	Address	Write	Read	Error in high speed test
0x11	–	Address	Write	Read	Error in bit test
0x12	–	Address	Write	Read	Error in address bit test
0x13	–	Address	Write	Read	Error in galloping test
0x14	–	Address	Write	Read	Error in byte write test
0x15	–	Address	Write	Read	Error in R-M-W test
0x16	–	–	–	–	Parity circuitry does not work
0x38	–	Address	Write	Read	Hard register error
0x40	–	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x42	–	–	–	–	Wrong interrupt level
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x77	Unit no	I/O add	–	–	TAS did not change byte
0x78	Unit no	I/O add	–	–	Byte was set before TAS
0x79	Unit no	I/O add	Write	Read	Error in bus test, short access
0x7A	Unit no	I/O add	Write	Read	Error in bus test, long access
0xE0	Unit no	STATUS	–	–	Bus error or fault interrupt
0xF0	–	–	–	–	Address error
0xF1	–	–	–	–	Exception error
0xF2	–	–	–	–	Fatal error during boot PROM self test

Table 2-2-24: Error codes for MIOC

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0xB0	Module	Add	Write	Read	Data error in received buffer
0xB1	Module	Add	Write	Read	Diagnose failed
0xB2	Module	–	SCB cmd	SCB stt	Time-out during wait for receive unit
0xB3	Module	–	SCB cmd	SCB stt	Time-out during command execution
0xB4	Module	–	CBL cmd	CBL stt	Command status failed.
0xB5	Module	–	–	–	Received frame faulty
0xB6	Module	–	SCB cmd	SCB stt	Reset failed
0xB7	Module	–	SCB cmd	SCB stt	Time-out during reset
0xB8	Module	–	SCB cmd	SCB stt	Time-out during acknowledge to the controller
0xB9	Module	–	SCB cmd	SCB stt	Time-out during wait for command interrupt
0xBA	Module	–	CBL cmd	CBL stt	Transmission failed
0xBB	Module	–	SCB cmd	SCB stt	Acknowledge to the controller failed
0xBC	Module	Add	Write	Read	Time-out during LAN diagnose
0xBD	Module	–	–	Status	Time Domain Reflectometer command failed

Table 2-2-25: Error codes for MIOC, Ethernet submodule

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0xB0	Module	Port no	Write	Read	Diagnose test failed
0xB1	Module	Port no	–	REC status	Receive error
0xB2	Module	Port no	–	HDLC status	Transmit error
0xB3	Module	Port no	Write	Read	Data error in received buffer
0xB4	Module	Port no	–	Test/error no	Modem signal test failed
0xB5	Module	Port no	–	Test/error no	Interrupt test failed
0xB6	Module	Port no	–	ISR1/ISR0	Receive interrupt error
0xB7	Module	Port no	–	ISR1/ISR0	Transmit interrupt error
0xB8	Module	Port no	–	–	Time-out during command execution
0xB9	Module	Port no	–	–	Time-out during wait for receive complete
0xBA	Module	Port no	–	–	Time-out during wait for transmit complete
0xBB	Module	Port no	–	HDLC status	Time-out during wait for transmit buffer ready

Table 2-2-26: Error codes for MIOC, HDLC submodule

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0xB0	Module	Port no	Write	Read	Diagnose test failed
0xB1	Module	Port no	–	UART status	Receive error
0xB2	Module	Port no	Write	Read	Data error in received buffer
0xB3	Module	Port no	–	Test/error no	Modem signal test failed
0xB4	Module	Port no	–	Test/error no	Interrupt test failed
0xB5	Module	Port no	–	–	Time-out during wait for receiver
0xB6	Module	Port no	–	–	Time-out during wait for transmitter
0xB7	Module	Port no	–	–	Fiber optical communication failed

Table 2-2-27: Error codes for MIOC, TERM submodule

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0xB0	Module	Add	Write	Read	Data error in memory
0xB1	Module	Add	Write	Read	Error when testing access types in memory
0xB2	Module	Add	Write	Read	Register error in Primary rate controller
0xB3	Module	Add	Write	Read	Register error in Basic rate controller
0xB4	Module	Add	Write	Read	Data error in the received frame
0xB5	Module	–	–	–	Time-out during wait for reset complete
0xB6	Module	–	–	–	Time-out during wait for transmit complete
0xB7	Module	–	–	–	Time-out during wait for receive complete
0xB8	Module	–	–	–	Time-out during wait for interrupt
0xB9	Module	–	Com	–	Time-out during wait for command complete
0xBA	Module	Add	Error	status	Time-out during wait for D-channel complete
0xBB	Module	Add	Error	–	Transmit frame status failed
0xBC	Module	Add	Error	–	Receive frame status failed
0xBD	Module	Add	Error	Status	D-channel frame status failed
0xBE	Module	–	–	–	Illegal interrupt occurred
0xBF	Module	–	–	–	ISDN interface failed

Table 2-2-28: Error codes for MIOC, ISDN submodule

Module value	Submodule number	Submodule type
0x02 or 0x03	0	Ethernet submodule
0x82 or 0x83	1	Ethernet submodule
0x04	0	HDLC submodule
0x84	1	HDLC submodule
0x05	0	TERM8 submodule
0x85	1	TERM8 submodule
0x06	0	TERM32 submodule
0x86	1	TERM32 submodule
0x07	0	ISDN submodule
0x87	1	ISDN submodule

Table 2-2-29: Module values for MIOC submodules

Value	Description
0xE0	No tests.
0xE1	Test RAM. High speed.
0xE2	Test RAM. Bit test.
0xE3	Test RAM. Address bit test.
0xE4	Test RAM. Galloping ones and zeroes.
0xE5	Test RAM. Byte write.
0xE6	Test RAM. Read modify write.
0xE7	Test AMMU memory.
0xE8	Test PMMU memory.
0xE9	Test AMMU mapping.
0xEA	Test PMMU mapping.
0xEB	Test interrupts.
0xEC	Cache test.
0xED	Bus test.
0xEE	Write Buffer test.
0xEF	Floating Point Unit test or ECC test.

Table 2-2-30: Test codes for CPU R4000

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x01	SYN(7-0)	EAR	–	–	Single bit error in memory
0x02	Error code	Address	–	–	Error in ECC test
0x10	–	Address	Write	Read	Error in high speed test
0x11	–	Address	Write	Read	Error in bit test
0x12	–	Address	Write	Read	Error in address bit test
0x13	–	Address	Write	Read	Error in galloping test
0x14	–	Address	Write	Read	Error in byte write test
0x15	–	Address	Write	Read	Error in R – M – W test
0x20	–	Address	Write	Read	Error in cache memory
0x21	–	Address	Write	Read	Error in cache test
0x24	–	Address	Write	Read	Error in cache tag memory
0x25	–	PC	Cache	ECC	Cache ECC error detected
0x35	–	Index	–	–	Error when testing AMMU mapping
0x36	–	Index	–	–	Error when testing PMMU mapping
0x37	Test	–	–	–	Error when testing Write Buffer
0x40	–	–	–	–	Interrupt error
0x41	–	–	–	–	Missing timer interrupt
0x42	–	–	–	–	Wrong interrupt level
0x70	Unit no	–	–	–	Unit not present
0x71	Unit no	–	–	–	Unit illegal test table
0x72	Unit no	–	–	–	Bus test not completed
0x73	Unit no	–	–	–	Overrun in test table

Table 2-2-31: Error Codes for CPU R4000 (1 of 2)

ERCD	SCODE	ADD (3-0)	WDT (3-0)	RDT (3-0)	Description
0x74	Unit no	–	–	–	Sum check error in test table
0x75	Unit no	I/O add	Write	Read	Error in request byte
0x76	Unit no	I/O add	Write	Read	Error in acknowledge byte
0x77	Unit no	I/O add	–	–	TAS did not change byte
0x78	Unit no	I/O add	–	–	Byte was set before TAS
0x79	Unit no	I/O add	Write	Read	Error in bus test
0x7A	Unit no	I/O add	Write	Read	Error in bus test, Write Bus
0x7B	Unit no	I/O add	Write	Read	Error in bus test, special access no. 1
0x7C	Unit no	I/O add	Write	Read	Error in bus test, special access no. 2
0x80	Test	–	–	–	Error when testing FPU
0xE0	Unit no	STATUS	–	–	Bus error
0xF0	–	–	–	–	Address error
0xF1	–	–	–	–	Exception error
0xF2	–	–	–	–	Fatal error during boot PROM self test

Table 2-2-31: Error codes for CPU R4000 (2 of 2)

NON-OPERATOR MODE

Supermax module type

On the following page a description of the content of the Non-Operator module type is shown for each of the units, that might be in a system. Refer to "Chapter 2-1 Non-Operator Mode", to see the description of the Non-Operator status buffer.

Module number	Supermax module type
0x01	CPU 68000
0x02	SIOC1
0x03	DIOC1
0x04	CIOC
0x05	DIOC2
0x06	NIOC
0x07	CPU 68020
0x08	SIOC2
0x09	DIOC3
0x0A	CPU 68030
0x0B	CPU R3000
0x0C	MIOC
0x0D	NIOCB (NIOC 1600/3600)
0x0E	CPU R4000

Table 2-3-1: Non-Operator Supermax module types

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NON-OPERATOR MODE

Test times

The time necessary to complete the test for each unit is shown in the table. The total time necessary to complete the whole test is calculated by the master unit in the following manner:

- The maximum value of the columns Internal test + Winchester.
- The sum of the values in the column Bus test.

When this time is calculated the master unit will control the other units and make sure they will start the bus test at the same time.

Module	Internal test	Bus test	Winchester
CPU 68000	1 min + 12 min/Mb	2 min	
SIOC1	2 min	2 min	
DIOC1	2 min	2 min	
CIOC	2 min	2 min	
DIOC2	2 min	2 min	
NIOC	2 min + 8 min/Mb	2 min	
CPU 68020	1 min + 4 min/Mb	2 min	
SIOC2	2 min + 8 min/Mb	2 min	
DIOC3	2 min + 3 min/Mb	2 min	(Cyl * head)/1024 min, if 2 or more winchesters then time/2
CPU 68030	2 min + 3 min/Mb	2 min	
CPU R3000	1 min + 1.5 min/Mb	5 min	
MIOC	2 min + 3 min/Mb	2 min	
CPU R4000	1 min + 1 min/Mb	5 min	

Table 2-4-1: Non-Operator Mode default time

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3 SUPERMAX MODULES

Supermax modules

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SUPERMAX MODULES

CPU 68000

The purpose of this program is to evaluate the basic functions of the CPU 68000 module and the dynamic memory connected to it. The following functions can be tested with this program:

- The dynamic RAM connected to the CPU.
- The Memory Management Unit (MMU).
- All interrupts.
- All R/W registers.
- The Error Detection and Correction unit.

The Diagnostic Program is able to run on a CPU with standard mounted straps.

Initialization

After pressing reset you will see **'bO'** in the display. When the Diagnostic Program is loaded into the CPU, the front panel display will count 00, 04, 08, 0C, 10, etc., indicating that an initialization of memory is performed.

Display codes

The CPU is ready to be selected when the display is turned off. If an error occurs the display will change depending upon the error. There are some additional display values used in Diagnostic Programs.

- **bE** in the display indicates a bus error.
- **AE** in the display indicates an address error.
- **Er** in the display indicates any other error.

If one of the error messages has been displayed it might be possible to get some more information about the error, by typing the select sequence on the terminal.

Running the Diagnostic Program

When the initialization is successfully completed, the CPU is ready to proceed with the more sophisticated parts of the test. After typing the select sequence for the CPU, that is going to be tested it should respond with the following message on the terminal:

cpu u > _ (**u** *is the unit number*)

When this prompt is displayed on the terminal, the CPU is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the CPU.

The example shows the menu from a CPU with unit number 3:

```
cpu   3   > M
 2.00 Mb memory
A - Test RAM High Speed
B - Test RAM Bit Test
C - Test RAM Address Bit Test
D - Test RAM Galloping Ones And Zeroes
E - Test RAM Byte Write
F - Test RAM Read Modify Write
G - Test MMU Memory
J - Test MMU Adder
K - Test MMU ASN con SEG
L - Test MMU Comparator
I - Test Interrupts
O - Repeat test(s)
S - Test All
X - Bustest. Passive unit
Y - Bustest. Active unit
P - Set test parameters
M - Menu
V - Version
Q - Debugger
Z - Boot
cpu   3   >
```

Figure 3-1-1: Menu for CPU 68000

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test RAM. High Speed

This routine performs a fast test of the main memory connected to the CPU module. It takes the low order word of the current address and shifts it one bit to the right and writes that value in the memory. Then the memory content is read and compared to the value written and errors are indicated. All of this is repeated using the high order word of the current address. The high order word is not shifted as the low order word. The Error Detection and Correction circuitry is switched **ON** during this test.

B – Test RAM. Bit Test

During this test every single bit in the main memory will be written with both *true* and *inverted* values. This is carried out by using long word operations, but on a word basis with the following values.

Pass	Write value
1	0x00010001
2	0xFFFEFFFE
3	0x00020002
4	0xFFFDFFFD
--	----------
31	0x80008000
32	0x7FFF7FFF

All in all 32 passes. A plus (+) is written on the terminal for each pass. The Error Detection and Correction circuitry is switched **OFF** during this test.

C – Test RAM. Address Bit Test

During this test every single address bit is tested. This is done by writing one value in the current address if the selected address bit is zero and another value if the address bit is one. The test is performed for address bits in the range 1–19 and the test runs four times, each time with two new write values.

Address bit	Pass 1	Pass 2	Pass 3	Pass 4
0	0x0000	0xFFFF	0x0000	0x8001
1	0xFFFF	0x0000	0x8001	0x0000

The reason for the value 0x8001 during pass 3 and 4 is to be sure that the bits concerning the Error Detection and Correction circuitry, which during this test is switched **ON**, also will be tested.

D – Test RAM. Galloping Ones And Zeroes

This test is also performed 4 times. First of all the memory is initialized with a default value. Then a galloping value is written in a certain address. Then all addresses which are neighbours to that first address are tested. They must still contain the default value. A neighbour is an address, which only differs in one bit from the original address. When all neighbours are tested the default value is written back in the original address. This is repeated for all addresses. The Error Detection and Correction circuitry is switched **ON** during this test.

Value	Pass 1	Pass 2	Pass 3	Pass 4
Default	0x0000	0xFFFF	0x0000	0x8001
Galloping	0xFFFF	0x0000	0x8001	0x0000

E – Test RAM. Byte Write

Because of the error correcting code it is much more difficult to write a byte in memory than it is to write a word. 16 bits are used to contain data and 6 bits contain the ECC code belonging to that data. If one byte (8 bits) is to be written you have to read the whole 16 bit word into a register, then write the new byte into the register and then write the whole word back in memory. During this test memory is initialized by writing a byte counter. Then the value 0x55 is written in all even memory locations and the whole memory is tested for correct content. The memory is then initialized again and the value 0x55 is written in all odd bytes. The whole memory is again tested for correct content. All write functions use byte write operations.

F – Test RAM. Read Modify Write

The MC68000 microprocessor has a feature which makes it possible in one operation to read a byte in memory, test the byte, set one bit in the byte and to write it back again. This is called *Read-Modify-Write* and this test will initialize memory with a default value and then perform the *Test And Set (TAS)* instruction on all memory locations and then check for correct memory content.

G – Test MMU Memory

The MMU memory consists of eight 1024x4 static RAMs. This memory can be tested using the same routines as those for the dynamic RAM, except the two using byte write operations. When selecting this test the above mentioned tests A, B, C and D will be performed on the MMU memory.

J – Test MMU Adder

The 16 bit adder is built from four 4 bit adders, which can be tested separately. This routine tests each 4 bit section of the adder in the MMU. The main memory is initialized in such a way that each double word in memory contains its own physical address. The memory is accessed using the relocating capabilities of the MMU. The physical address is calculated by adding the offset stored in the MMU to the logical address used when accessing the main memory. The calculated physical address is compared to the real physical address as read in the main memory.

K – Test MMU ASN con SEG

This routine tests that the MMU is addressed correctly by Address Space Number and Segment Number. The content of the main memory is initialized with physical addresses. The MMU memory is initialized with increasing offsets. For all Address Space Numbers and Segment Numbers the main memory is accessed using the relocating capabilities of the MMU. The calculated physical address is compared to the real physical address as read in the main memory.

L – Test MMU Comparator

This routine tests the 12 bit comparator used in the MMU. The routine accesses main memory using different Block Numbers (**BN**) and different **Sizes** in the MMU while the checking facilities of the MMU are enabled. Whenever **BN > Size** the memory access is illegal and a bus error should occur and if **BN < = Size** the memory access is legal and no bus error should occur.

I – Test Interrupts

This routine tests the interrupt circuit by setting all eight levels of external interrupts and checking that they activate the bits in the Interrupt Status Register. The timer interrupt is also tested and you can calculate the time between timer interrupts by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. Normally you should end up with 40 ms.

O – Repeat test(s)

All of the above mentioned tests will run one time through when selected. If, when selecting test(s), this one (*O*) is also selected, the test(s) will repeat itself (themselves) until otherwise canceled. It is not possible to select *X* and *Y* together with *O*.

S – Test All

This test will run one time through test A, B, C, D, E, F, G, J, K, L and I. It is possible to add the *Repeat test* option *(O)* to this one. This test does not include the bus test *X* or *Y*.

X – Bustest. Passive unit

Refer to "Chapter 4 – 1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

P – Set test parameters

This entry is used to set start address and end address for the memory tests. The start and end address has to be on hexadecimal form. If nothing is entered, the program will use the default values shown on the terminal. Entering illegal addresses will not be allowed.

M – Menu

Display the menu on the terminal. The first line contains the actual memory size.

V – Version

Display version, date and elapsed time from last reset, on the form hh:mm:ss.

Q – Debugger

Go to debugging program. Return to Diagnostic Program by entering **RT <CR>**.

Z – Boot

Give master reset to the system.

Status register

If a bus error occurs, the status register contains information about the reason of the bus error.

Status bit	Description
STATUS(0)	Illegal user
STATUS(1)	Illegal bus
STATUS(2)	Illegal write
STATUS(3)	Segment too long
STATUS(4)	Time out
STATUS(5)	No memory
STATUS(6)	Error from bus
STATUS(7)	Double fault in memory
STATUS(8)	Single fault in memory
STATUS(9)	Timer interrupt
STATUS(10)	Error in unit
STATUS(11)	Power fail
STATUS(12)	RxRdy
STATUS(13)	TxRdy
STATUS(15:14)	Not used

Table 3-1-1: Status register on CPU 68000

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SUPERMAX MODULES

SIOC1

The purpose of this program is to evaluate the basic functions of the SIOC1 module 0300, which is the Serial Input Output Controller in the Supermax card family. The following functions can be tested using this program:

- Baud rate generators
- USART channels
- RS-232C interface
- RS-422 interface
- USART interrupts
- Timer interrupt
- Memory mapper
- Memory

The program is able to run on a SIOC1 with standard mounted straps. However, if the serial lines are to be tested, the 60 pin flat cable between the SIOC1 back panel and the SIOC1 module must be connected. If the RS-422 interface is to be tested, also the 50 pin flat cable must be connected. 8 special plugs must be placed in the SIOC1 back panel 25 pin connectors in order to test the RS-232C serial lines, and two special plugs must be placed in the 15 pin connectors in order to test the RS-422 serial lines. The plugs are described at the end of this chapter.

Running the Diagnostic Program

After pressing reset LED no. 4 will light. When the Diagnostic Program is loaded into the SIOC1, the LED will turn off and the SIOC1 is ready to be selected, and to start execution of the tests. After typing the select sequence for the SIOC1, that is going to be tested it should respond with the following message on the terminal:

sioc1 u > _ (**u** *is the unit number*)

When this prompt is displayed on the terminal, the SIOC1 is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the SIOC1.

The example shows the menu from a SIOC1 with unit number 8:

```
siocl 8   > M
Hard test of SIOC1

A - Test baudrate generators
B - Test USART channels
C - Test USART interrupts
D - Test timer interrupt
E - Test memory mapper
F - Test RS-422
G - Test all
H - Test memory from 0x4000 to 0xF000
O - Repeat test(s)
Q - Call DEBUG
S - Select USART channels to be tested
X - Bustest. Passive unit
Y - Bustest. Active unit
M - Menu
V - Version

siocl 8   >
```

Figure 3-2-1: Menu for SIOC1

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test Baud Rate Generators

This test works in conjunction with the one mentioned in B. It checks the 8 baud rate generators and the USART channels with baud rates from 19200 to 300 baud. For every baud rate it transmits and receives all possible characters on the channels, which were selected in *S*.

B – Test USART channels

This test transmits and receives all possible characters ranging from 0x00 to 0xFF, on the USART's, which you select. It receives on the same channel as it transmits. The baud rate during this test is 9600 baud.

C – Test USART interrupts

During this test all RxRDY interrupts from the eight USART's are tested. At the same time the Interrupt Mask Register and the Receiver Mask Register are checked for correct function.

D – Test Timer Interrupt

The internally generated timer interrupt is checked for correct function. You can calculate the timer interrupt interval by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. The SIOC1 should be strapped to 20 ms.

E – Test memory mapper

The memory mapper consists of six 16x4 static RAMS which are organized as 48 map registers each 8 bits wide. During test of the mapper all registers are initialized with 0x00, and each bit is set separately. When a bit is set all registers are read back and checked.

F – Test RS-422

The serial RS-422 lines are checked for correct function running at a baud rate of 9600 baud. Channel 6 and 7 are the RS-422 USART's. The routines from test B are used to test this interface.

G – Test all

This test will run one time through test H, E, and D.

H – Test memory

Memory area from 0x4000 to 0xF000 is tested as described below. A 16-bit counter (start value 0x0000) is written in the RAM area which is to be tested. Then the RAM area is read back and the content is checked against the written value in order to locate any errors. After this test a counter with start value 0xFFFF (count down) is written and read back.

O – Repeat test(s)

All of the above mentioned tests will run one time through when selected. If, when selecting test(s), this one (*O*) is also selected, the test(s) will repeat itself (themselves) until otherwise canceled. It is not possible to select *X* and *Y* together with *O*.

Q – Call debug

Go to debugging program. Return to Diagnostic Program by entering **<CR>1XG**.

S – Select USART channels to be tested

When the USART's are going to be tested the program will need information about which channels are to be tested. If not going through this **S** command the default is all channels. It is possible to select the channels by typing numbers from 0 – 7 or type A for all.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

M – Menu

Display the menu on the terminal.

V – Version

Display version, date and elapsed time from last reset, on the form hh:mm.

Special plugs

In order to test the USART's you must use eight 25 pin Cannon connectors strapped as shown to the left. Place them in the SIOC1 back panel. If you are going to test the RS-422 lines you must use two 15 pin Cannon connectors strapped as shown to the right, and place them in the SIOC1 back panel.

RS-232C plug 25 pin	RS-422 plug 15 pin
2 ←→ 3	2 ←→ 4
4 ←→ 5	3 ←→ 5
6 ←→ 20	9 ←→ 11
	10 ←→ 12

Table 3-2-1: Special plugs to test the SIOC1

Status register

If an error occurs, the status register contains information about the reason of the error.

Status bit	Description
ESR(0)	Time out
ESR(1)	Bus error out
ESR(2)	Bus error in
ESR(3)	Parity error
ESR(4)	ERROR signal in I/O bus
ESR(5)	Internal error signal
ESR(6)	Not used
ESR(7)	BUSY signal from parallel printer

Table 3-2-2: Status register on SIOC1

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SUPERMAX MODULES

DIOC1

The purpose of this program is to evaluate the basic functions of the DIOC1 module 0400, which is the Disk Input Output Controller in the Supermax card family. The following functions can be tested using this program:

- DMA channels
- Peripheral interface
- Timer interrupt
- Memory mapper
- Memory
- Peripheral units

The program is able to run on a DIOC1 with standard mounted straps.

Running the Diagnostic Program

After pressing reset LED no. 4 will light. When the Diagnostic Program is loaded into the DIOC1, the LED will turn off and the DIOC1 is ready to be selected, and to start execution of the different tests. After typing the select sequence for the DIOC1, that is going to be tested it should respond with the following message on the terminal:

`dioc1 u` **`>`** **`_`** (**u** *is the unit number*)

When this prompt is displayed on the terminal, the DIOC1 is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the DIOC1.

The example shows the menu from a DIOC1 with unit number E:

```
diocl E   > M
Hard test of DIOC1

A - Test memory mapper
B - Test DMA
C - Test all
D - Test peripheral units
E - Test peripheral interface
F - Test timer interrupt
G - Test memory 0xA000 to 0xF000
O - Repeat test(s)
Q - Call debug
X - Bustest. Passive unit
Y - Bustest. Active unit
M - Menu
V - Version

diocl E   >
```

Figure 3-3-1: Menu for DIOC1

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Memory mapper

The memory mapper consists of six 16x4 static RAMS which are organized as 48 map registers each 8 bits wide. During test of the mapper all registers are initialized with 0x00, and each bit is set separately. When a bit is set all registers are read back and checked.

B – Test DMA

The DMA test only checks the communication with the AM9517 four channel DMA controller. Test of the four channels will be performed during execution of other test programs. Before test, the 9517 is given a master clear. Then the status register and the temporary register are read. These registers must contain 0x00 after reset. All address and word count registers are initialized with 0x00, and each bit is set separately. When a bit is set all registers are read back and checked.

C – Test all

This test will run one time through test A, B, E, F, and G.

D – Test peripheral units

The Diagnostic Program for Peripheral Units will always be resident in the DIOC1, except after running the bus test *X* or *Y*. Refer to "Chapter 6–1 Peripheral test for DIOC1/DIOC2", to see the detailed description of the peripheral test.

E – Test Peripheral Interface

This test consist of 3 parts:

- **Floppy Disk Interface.** A counter is written in the track register and the sector register of the FD 1795 floppy disk controller and read back. The test only checks the communication with the FD 1795 and not the interface to the drive.
- **Streaming Tape Interface.** The test checks the data bus in the interface. A counter is written in a register in the interface and read back.
- **Winchester Disk Interface.** The test checks the data bus in the interface. A counter is written in a register in the interface and read back.

F – Test timer interrupt

The internally generated timer interrupt is checked for correct function. You can calculate the timer interrupt interval by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. The timer frequency is strapable, and has one of the following values: 1.3, 6.4, 12.8, 64.0 or 128 milliseconds. The DIOC1 should be strapped to 128 ms.

G – Test memory

Memory area from 0xA000 to 0xF000 is tested as described below. A 16-bit counter (start value 0x0000) is written in the RAM area which is to be tested. Then the RAM area is read back and the content is checked against the written value in order to locate any errors. After this test a counter with start value 0xFFFF (count down) is written and read back.

O – Repeat test(s)

All of the above mentioned tests will run one time through when selected. If, when selecting test(s), this one (*O*) is also selected, the test(s) will repeat itself (themselves) until otherwise canceled. It is not possible to select *X* and *Y* together with *O*.

Q – Call debug

Go to debugging program. Return to Diagnostic Program by entering **<CR>1XG**.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

M – Menu

Display the menu on the terminal.

V – Version

Display version, date and elapsed time from last reset, on the form hh:mm.

Status register

If an error occurs, the status register contains information about the reason of the error.

Status bits	Description
ESR(0)	Time out
ESR(1)	Bus error out
ESR(2)	Bus error in
ESR(3)	Parity error
ESR(4)	Error signal in I/O bus
ESR(5)	BTU time out
ESR(6)	BTU bus error in
ESR(7)	DMA parity error

Table 3-3-1: Status register on DIOC1

SUPERMAX MODULES

CIOC

The purpose of this program is to evaluate the basic functions of the CIOC module 0900, which is the Communication Input Output Controller in the Supermax card family. The following functions can be tested using this program:

- Baud rate generators
- USART channels
- USART interrupts
- DMA channels
- Line interface signals
- HDLC channels
- Timer interrupt
- Memory mapper
- Memory

The program, except for test **E**, is able to run on a CIOC with standard mounted straps. However, if the communication lines are to be tested, the 50 pin flat cable between the CIOC back panel and the CIOC module must be connected. Two special plugs must be placed in the CIOC back panel 25 pin connectors, and two special plugs must be placed in the CIOC back panel 15 pin connectors before testing.

Running the Diagnostic Program

After pressing reset LED no. 4 will light. When the Diagnostic Program is loaded into the CIOC, the LED will turn off and the CIOC is ready to be selected, and to start execution of the tests. After typing the select sequence for the CIOC, that is going to be tested it should respond with the following message on the terminal:

`cioc u > _` (**u** *is the unit number*)

When this prompt is displayed on the terminal, the CIOC is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the CIOC.

The example shows the menu from a CIOC with unit number F:

```
cioc  F   > M
Hard test of CIOC

A - Test memory mapper
B - Test DMA and memory move
C - Test all
D - Test USARTs
E - Test USARTs with modem clocks
F - Test HDLC-0
G - Test HDLC-1
I - Test memory from 0x4000 to 0xF000
H - Test timer interrupt
O - Repeat test(s)
Q - Call DEBUG
X - Bustest. Passive unit
Y - Bustest. Active unit
M - Menu
V - Version

cioc  F   >
```

Figure 3-4-1: Menu for CIOC

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test memory mapper

The memory mapper consists of six 16x4 static RAM's which are organized as 48 map registers each 8 bits wide. During test of the mapper all registers are initialized with 0x00, and each bit is set separately. When a bit is set all registers are read back and checked.

B – Test DMA and memory move

On the CIOC there are two DMA controllers AM9517 each with four channels. One of the channels is cascaded to the other controller giving a total of 7 channels. The DMA test only checks the communication with the two AM9517 DMA controllers. Before testing, the 9517 is given a master clear. Then the status register and the temporary register are read. These registers must contain 0x00 after reset. All address and word count registers are initialized with 0x00, and each bit is set separately. When a bit is set all registers are read back and checked. The memory move feature is tested by writing a counter in a part of the memory and then move this part of the memory to another part of the memory using DMA transfer. Then the second part of the memory is tested for correct content. After that the test is repeated, but this time moving from the second part of the memory to the first part.

C – Test all

This test will run one time through test I, A, B, and H.

D – Test USARTs

During this test the four USART's are tested. The baud rate during all tests is 9600 baud. During the test the Communication Select Register, Communication Interrupt Register, and Interrupt Mask Register are checked for correct function.

This test consists of 4 parts:

- All line interface signals are checked. USART-D is used to test RS-232C interface and USART-X is used to test RS-422 interface.
- All RxRDY and TxRDY interrupts from the four USART's are tested.
- USART – X is tested with RxRDY and TxRDY interrupts. This test transmits and receives all possible characters ranging from 0x00 to 0xFF, on the USART's. Interface RS-422 is used for this test.
- Testing USART – D channel with DMA controller 1. This test transmits and receives all possible characters ranging from 0x00 to 0xFF, on the DMA/USART's. All DMA interrupts will be tested. Interface RS-232C is used for this test.

In order to test the serial channels there must be 4 special plugs in the back panel. The plugs are described at the end of this chapter.

E – Test USARTs with modem clocks

During this test receiver/transmitter clocks on the RS-232C interface and the Signal Element Timing on RS-422 interface are tested. Before testing set the straps STX0, SRX0, STX1, and SRX1 to CIOC driving the modem clocks (Position 2-3). The routines from test D are used to test the USARTs with modem clocks.

F – Test HDLC-0

During this test the HDLC-0 is tested. It checks the two baud rate generators RxClk and TxClk on the HDLC channel with baud rates from 19200 to 300 baud. During the test the Communication Select Register, Communication Interrupt Register, and Interrupt Mask Register are checked for correct function. Line interface RS-232C is used during this test.

This test consists of 3 parts:

- Testing reset and initializing the HDLC-chip.
- Testing modem signals on the HDLC-chip.
- Testing HDLC channel with DMA controller 1. This test transmits and receives all possible characters ranging from 0x00 to 0xFF, on the DMA/HDLC. Interrupts RxINT and TxINT will be tested.

In order to test the serial channels there must be 2 special plugs in the back panel. The plugs are described at the end of this chapter.

G – Test HDLC-1

The routines from test F are used to test HDLC-1.

I – Test memory

Memory area from 0x4000 to 0xF000 is tested as described below. A 16-bit counter (start value 0x0000) is written in the RAM area which is to be tested. Then the RAM area is read back and the content is checked against the written value in order to locate any errors. After this test a counter with start value 0xFFFF (count down) is written and read back.

H – Test timer interrupt

The internally generated timer interrupt is checked for correct function. You can calculate the timer interrupt interval by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. The CIOC should be strapped to 12 ms.

O – Repeat test(s)

All of the above mentioned tests will run one time through when selected. If, when selecting test(s), this one (*O*) is also selected, the test(s) will repeat itself (themselves) until otherwise canceled. It is not possible to select *X* and *Y* together with *O*.

Q – Call debug

Go to debugging program. Return to Diagnostic Program by entering **<CR>1XG**.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

M – Menu

Display the menu on the terminal.

V – Version

Display version, date and elapsed time from last reset, on the form hh:mm.

Special plugs

In order to test the CIOC you must use two 25 pin Cannon connectors strapped as shown to the left, and two 15 pin Cannon connectors strapped as shown to the right, and place them in the CIOC back panel.

RS-232C plug 25 pin	RS-422 plug 15 pin
2 ←→ 3	2 ←→ 4
4 ←→ 5	3 ←→ 5
4 ←→ 8	9 ←→ 11
6 ←→ 20	10 ←→ 12

Table 3-4-1: Special plugs to test the CIOC

Status register

If an error occurs, the status register contains information about the reason of the error.

Status bit	Description
ESR(0)	Time out
ESR(1)	Bus error out
ESR(2)	Bus error in
ESR(3)	Parity error
ESR(4)	Error signal in I/O bus
ESR(5)	BTU time out
ESR(6)	BTU bus error in
ESR(7)	DMA parity error

Table 3-4-2: Status register on CIOC

SUPERMAX MODULES

DIOC2

The purpose of this program is to evaluate the basic functions of the DIOC2 module 1100, which is the second version of the Disk Input Output Controller in the Supermax card family. The following functions can be tested using this program:

- DMA channels
- DMA memory
- Peripheral interface
- Timer interrupt
- Memory mapper
- Memory
- Peripheral units

The program is able to run on a DIOC2 with standard mounted straps.

Initialization

During the initial 15 seconds after reset an internal test and initialization is performed. First the DIOC2 runs in the EPROM and tests a part of the memory before it makes a copy of the EPROM to that part of memory. If any errors are detected during this test the program will stay in the EPROM, LED 3 and LED 2 will light and an error message will be displayed on the terminal.

After copying the EPROM the memory mapper is tested, then the rest of the program memory is initialized and tested and finally the DMA memory is initialized and tested. If any errors are found LED 3 will never turn off. If no errors are found LED 3 will turn off after about 15 seconds and the DIOC2 will start to boot the system.

If there is a hard error on the floppy disk or the winchester disk LED 2 will light, and the DIOC2 will keep trying to load the programs. When all Diagnostic Programs are loaded into the respective units, all LED's on the DIOC2 will be turned off.

Running the Diagnostic Program

When the initialization is successfully completed, the DIOC2 is ready to proceed with the more sophisticated parts of the test. After typing the select sequence for the DIOC2, that is going to be tested it should respond with the following message on the terminal:

`dioc2 u  > _` (**u** *is the unit number*)

When this prompt is displayed on the terminal, the DIOC2 is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the DIOC2.

The example shows the menu from a DIOC2 with unit number E:

```
dioc2 E   > M
Hard test of DIOC2

A - Test memory mapper
B - Test memory
C - Test all
D - Test peripheral units
E - Test peripheral interface
F - Test bus interrupt and timer interrupt
G - Test DMA memory
H - Test DUARTs
O - Repeat test(s)
P - Set boot pointer
Q - Call DEBUG
S - Set test time for Non-Operator Mode
U - Display configuration
X - Bustest. Passive unit
Y - Bustest. Active unit
M - Menu
V - Version

dioc2 E   >
```

Figure 3-5-1: Menu for DIOC2

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test memory mapper

The memory mapper consists of six 16x4 static RAM's which are organized as 48 map registers each 8 bits wide. During test of the mapper all registers are initialized with 0x00, and each bit is set separately. When a bit is set all registers are read back and checked.

B – Test memory

Memory area from 0x10000 to 0x40000 is tested as described below. A 16-bit counter (start value 0x0000) is written in the RAM area which is to be tested. Then the RAM area is read back and the content is checked against the written value in order to locate any errors. After this test a counter with start value 0xFFFF (count down) is written and read back.

C – Test all

This test will run one time through test B, A, G, E, and F.

D – Test peripheral units

The Diagnostic Program for peripheral units will always be resident in the DIOC2. Refer to "Chapter 6–1 Peripheral test for DIOC1/DIOC2", to see the detailed description of the peripheral test.

E – Test peripheral interface

This test consist of 3 parts:

- **Floppy Disk Interface**. A counter is written in the track register and the sector register of the FD 2795 floppy disk controller and read back. The test only checks the communication with the FD 2795 and not the interface to the drive.
- **Streaming Tape Interface**. The test checks the tape word count register by writing a counter in the two registers in the interface and read back.

- **BTU word count register**. The test checks the BTU word count register by writing a counter in the two registers in the interface and read back.

F – Test bus interrupt and timer interrupt

The internally generated timer interrupt is checked for correct function. You can calculate the timer interrupt interval by measuring the time between two writings of 'Timer interrupt' on the terminal and then divide that time by 100. The timer frequency is strapable, and has one of the following values: 10, 20, 40, 80 milliseconds. 80 milliseconds is default. Also an internal setting of external interrupts is tested.

G – Test DMA memory

DMA memory area from 0x0000 to 0x10000 for all four banks (256 Kb) is tested as described in **B**.

H – Test DUART's

On the DIOC2 there are two DUART's giving four serial channels. This test consists of 3 parts:

- All channels are tested by writing all values from 0x00 – 0xFF from one channel to the same channel at four different baud rates, 1200, 4800, 9600 and 38400, checking that the received character is the same as the one send.
- It is checked that it is possible to get an interrupt from all four channels when receiving a character.
- It is checked that the DUART's are able to set and reset all the modem signals.

In order to test the serial channels there must be 4 special plugs in the DIOC2 back panel. The plugs are described at the end of this chapter.

O – Repeat test(s)

All of the above mentioned tests will run one time through when selected. If, when selecting test(s), this one (*O*) is also selected, the test(s) will repeat itself (themselves) until otherwise canceled. It is not possible to select *X* and *Y* together with *O*.

P – Set boot pointer

If the Diagnostic Programs are booted from a disk located on this DIOC2, it is possible to change the boot pointer, which is a pointer to a logical disk where the boot programs are located. There are up to 4 pointers, which can be selected. Normally **Pointer 0** points to the **Supermax Operating System** and **Pointer 1** points to the **Diagnostic Programs** and **Pointer 2 and 3** are not used. Selecting **Default** will set the pointer to the temporary pointer which normally contains the one that was active before the Diagnostic Programs were loaded. It is also possible to clear the boot pointer, if winchester boot is not wanted.

Q – Call debug

Go to debugging program. Return to Diagnostic Program by entering **<CR>1XG**.

S – Set test time for Non-Operator Mode

This is used if the time for running in **Non-Operator Mode** is to be changed. Both the time for the internal test and the time for the bus test can be set individually. The program will ask if you want to use the default time. If the answer is **No**, you will be asked to type in the new values. It is not possible to use this command on a DIOC2, which is **not** the Master unit.

U – Display configuration

A configuration list will be written on the terminal, containing information about Diagnostic Programs version and which units, type and unit number, were in the system when it was booted. It is not possible to use this command on a DIOC2, which is **not** the Master unit.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

M – Menu.

Display the menu on the terminal.

V – Version

Display version, date and elapsed time from last reset, on the form hh:mm.

Special plugs

In order to run the DIOC2 serial channel Diagnostic Program you must use four 25 pin Cannon connectors strapped as shown below and place them in the back panel.

RS-232C plug 25 pin
2 ←→ 3
4 ←→ 5
6 ←→ 20

Table 3-5-1: Special plugs to test the DIOC2

Status register

If an error occurs, the status register contains information about the reason of the error.

Status bit	Description
ESR(0)	Error signal in I/O bus
ESR(1)	BTU bus error
ESR(2)	Parity error in DMA memory
ESR(3)	Time out during a BTU transfer
ESR(4)	Bus error
ESR(5)	Parity error in program memory
ESR(6)	Time out during an I/O bus cycle
ESR(7)	Time out because 8085 halt

Table 3-5-2: Status register on DIOC2

SUPERMAX MODULES

NIOC/SIOC2

The purpose of this program is to evaluate the basic functions of the NIOC module 1600 – 3600 and the SIOC2 module 3600 in the Supermax card family. The following functions can be tested with this program:

- The dynamic memory.
- The Memory Management Unit (MMU).
- All interrupts.
- The DUART modules.
- The Local Area Network (*LAN*) controller.
- The EEPROM.

The Diagnostic Program is able to run on a NIOC/SIOC2 with standard mounted straps. It is the same program running on both the NIOC 1600 – 3600 and the SIOC2 3600. The program will determine what module it is running on and only the tests concerning that module can be selected.

Initialization

Included in the boot prom of the NIOC/SIOC2 is a thorough self test, which includes the following items:

- MC68000 internal confidence test.
- High speed MMU memory test.
- Address Space Register test.
- Interrupt Mask Register test.

- Initialize and test memory from 0x0 – 0x80000, before copying the content of the prom to the memory.
- Initialize and test memory to top of memory, which is read in the configuration table in the EEPROM. If nothing or illegal value written in the EEPROM only memory up to 0x80000 will be tested.
- Initialize and test the buffer memory if installed. This is read in the configuration table in the EEPROM. If nothing or illegal value written in the EEPROM no test will be performed.

If all the mentioned tests run without any errors LED no. 4, indicating Error In Unit, will be turned off and the NIOC/SIOC2 is ready to be booted. If the LED does not turn off within appx. 15 seconds, it is because of an error during the self test. The NIOC/SIOC2 will not be booted if any error occurred. If this happens you should try to type the select sequence. Depending upon the error it is possible that you might get some information about the error when selecting the NIOC/SIOC2. When the LED is turned off and the NIOC/SIOC2 has been booted with the Diagnostic Program, you can proceed with the execution of those programs.

Running the Diagnostic Program

When the initialization is successfully completed, and the NIOC/SIOC2 is booted, the NIOC/SIOC2 is ready to proceed with the more sophisticated parts of the test. After typing the select sequence for the NIOC/SIOC2, that is going to be tested it should respond with a message on the terminal, depending upon what module it is.

If it is a NIOC 1600 it will respond:

nioc1 u > _ (**u** *is the unit number*)

If it is a NIOC 3600 it will respond:

nioc2 u > _ (**u** *is the unit number*)

If it is a SIOC2 3600 it will respond:

sioc2 u > _ (**u** *is the unit number*)

When one of these prompts are displayed on the terminal, the NIOC/SIOC2 is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the NIOC/SIOC2. The example shows the menu from a SIOC2 with unit number 5:

```
sioc2 5   > M
A - Test Main memory
B - Test Buffer memory
C - Test MMU memory
D - Test MMU. ASN - SEG
E - Test MMU. Size field check
F - Test DUART's. External loop back
G - Test DUART's. Internal loop back
H - Test LAN controller without Transceiver
K - Test LAN controller with Transceiver
I - Test Interrupt
J - Test EEPROM. Content will be saved
O - Repeat test(s)
S - Test All
X - Bustest. Passive unit
Y - Bustest. Active unit
N - Network monitor
W - Read/Write Network address in EEPROM
T - Insert Hardware configuration in EEPROM
P - Set test parameters       U - Write to parallel printer
M - Menu                      V - Version
Q - Debugger                  Z - Boot
sioc2 5   >
```

Figure 3-6-1: Menu for NIOC/SIOC2

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test main memory

This is a test of the main memory on the NIOC/SIOC2. It is possible to have either 512 kB or 1 MB of main memory. The program will only test as much memory as mounted. The following 5 tests will be executed in the order mentioned.

- **High Speed**. This routine performs a fast test of the dynamic memory mounted on the NIOC/SIOC2 module. It takes the low order word of the current address and shifts it one bit to the right and writes that value in memory. Then the memory content is read and compared to the value written and errors are indicated. All of this is repeated using the high order word of the current address. The high order word is not shifted as the low order word.

- **Bit Test**. During this test every single bit in the main memory will be written with both *true* and *inverted* values. This is carried out by using long word operations but on a word basis with the following values.

Pass	Write value
1	0x00010001
2	0xFFFEFFFE
3	0x00020002
4	0xFFFDFFFD
--	----------
31	0x80008000
32	0x7FFF7FFF

  All in all 32 passes. A plus (+) is written on the terminal for each pass.

- **Address Bit Test**. During this test every single address bit is tested. This is done by writing one value in the current address if the selected address bit is zero and another value if the address bit is one.

Address bit	Pass 1	Pass 2
0	0x0000	0xFFFF
1	0xFFFF	0x0000

The test is performed for address bits in the range 1-19 and the test runs two times, each time with two new write values.

- **Galloping Ones And Zeroes**. This test is also performed two times. First of all the memory is initialized with a default value. Then a galloping value is written in a certain address. Then all addresses which are neighbours to that first address are tested. They must still contain the default value. A neighbour is an address which only differs in one bit from the original address. When all neighbours have been tested the default value is written back in the original address. This is repeated for all addresses.

Value	Pass 1	Pass 2
0	0x0000	0xFFFF
1	0xFFFF	0x0000

- **Read-Modify-Write**. The MC68000 microprocessor has a feature which makes it possible in one operation to read a byte in memory, test the byte, set one bit in the byte and to write it back again. This is called read modify write and this test will initialize memory with a default value and then perform the Test And Set (TAS) instruction on all memory locations and then check for correct memory content.

B – Test buffer memory

The buffer memory consists of 256 kB dynamic memory and will be tested using the same 5 routines as those for the main memory. The buffer memory is only mounted on NIOC modules.

- **High Speed.**
- **Bit Test.**
- **Address Bit Test.**
- **Galloping Ones And Zeroes.**
- **Read-Modify-Write.**

C – Test MMU Memory

The MMU memory consists of 2 kB static RAM. This memory will be tested using 4 of the routines mentioned above.

- **High Speed.**
- **Bit Test.**
- **Address Bit Test.**
- **Galloping Ones And Zeroes.**

D – Test MMU. ASN – SEG

This routine tests that the MMU is addressed correctly by Address Space Number and Segment Number. The main memory is initialized with physical addresses. The MMU memory is initialized with increasing offsets. For all Address Space Numbers and Segment Numbers the main memory is accessed using the relocating capabilities of the MMU. The calculated physical address is compared to the real physical address as read in the main memory.

E – Test MMU. Size field check

This routine tests the bit swapping and bit field test facilities in the memory protection capabilities of the MMU. It accesses main memory using different logical addresses and different Sizes while the checking facilities of the MMU are enabled. If the value of the Size field is called **Z** and the logical address is called **LADR**, then we have that whenever **LADR(19:10+Z) < > 0** then the memory access is illegal and a bus error should occur and if **LADR(19:10+Z) = 0** then the memory access is legal and no bus error should occur.

F – Test DUART's. External loop

On the SIOC2 there is a local bus, on which it is possible to connect from 1 to 8 DUART modules, each having 8 serial channels. All DUART modules are tested one by one using the following 3 tests:

- All channels are tested by transmitting characters with values from 0x00 – 0xFF from one channel to the same channel at two different baud rates, 9600 and 38400, checking that the received character is the same as the one transmitted.
- It is checked that it is possible to get an interrupt from all 8 channels when receiving a character.
- It is checked that the DUART's are able to set and reset all the modem signals.

In order to test the serial channels with external loop you must insert 8 special plugs in each DUART back panel. The plugs are described at the end of this chapter.

G – Test DUART's. Internal loop

It is possible to configure the DUART's to a mode called internal loop. When doing that the DUART's will make an internal connection of the transmit and receive data pins. This enables the program to run the test without using the special plugs required in test **F**. However, it is not possible to test the modem signals in internal loop, so only the first and second test mentioned above will be made during this test.

H – Test LAN controller without Transceiver

The Local Area Network (*LAN*) module, which is an Ethernet interface, is based on Intel 82586 and SEEQ 8023A. The 82586 is the Ethernet controller and the 8023A is the manchester encoder/decoder. Communication between the 68000 and the 82586 is made through the buffer memory. A certain part of that memory is used to exchange commands and status information. The LAN test will only run on NIOC modules.

This entry is used to check the Ethernet controller. The Ethernet controller will run in internal loop back and will transmit and receive packages to/from the buffer memory. The following Ethernet tests are used.

- Controller test
- Controller data transmission. The test will run 2048 times.
- Internal data transmission. The test will run 2048 times.

Refer to "Chapter 5 – 1 Ethernet test", to see the detailed description of the Ethernet test.

K – Test LAN controller with Transceiver

This entry is used to check the Ethernet controller. The Ethernet controller will run in external loop back (in the transceiver) and will transmit and receive packages to/from the buffer memory. The following Ethernet tests are used.

- Controller test
- Controller data transmission. The test will run 2048 times.
- External data transmission. The test will run 2048 times.

Refer to "Chapter 5 – 1 Ethernet test", to see the detailed description of the Ethernet test.

I – Test interrupt

This routine tests the interrupt circuit by setting all eight levels of external interrupts and checking that they activate the bits in the Interrupt Status Register. The timer interrupt is also tested and you can calculate the time between timer interrupts by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. Normally you should end up with 10 ms.

J – Test EEPROM. Content will be saved

All the network parameters are stored in the EEPROM. Because of that the content of the EEPROM is saved in main memory before testing it. The EEPROM is tested by writing 0x00 and 0xFF into it. After that the original content is written back. The NIOC/SIOC2 will not respond to any interrupts from the service port during this test. This means that you should not try to select any other units, because that operation will not deselect the NIOC/SIOC2. An EEPROM is only able to perform appx. 10000 write operations, before it is destroyed and because of that you will not be allowed to run this test continuously, and you should not run it more than once when testing a NIOC/SIOC2.

O – Repeat test(s)

All of the above mentioned tests will run one time through when selected. If, when selecting test(s), this one *(O)* is also selected, the test(s) will repeat itself (themselves) until otherwise canceled.

S – Test all

This test will run one time through test A, B, C, D, E, G, H and I. It is possible to add the *Repeat test* option *(O)* to this one.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

N – Network monitor

This entry is used to check the local area network. The Ethernet controller will receive all packages on the network cable. Refer to "Chapter 5–1 Ethernet test", to see the detailed description of the Ethernet test. The following Ethernet tests are used.

- Controller test
- Monitor mode. The test run continuously.

W – Read/Write Network address in EEPROM

The individual address, assigned to all controllers connected to a Local Area Network, is located in the EEPROM. This address must be written in the EEPROM, otherwise the NIOC software will not work properly. This entrance in the Diagnostic Program will show you the 6 byte address including a checksum verification. Then it is possible to insert a network address, to change the old one or just to exit without any change. Please note, that it is impossible to change the first 3 bytes of the address. They must be 0x080075 in all networking equipment from DDE.

NOTE

All numbers typed will be right adjusted when written in the EEPROM.

T – Insert hardware configuration in EEPROM

The Hardware configuration of the NIOC/SIOC2 is stored in the EEPROM. It is possible to display and change the configuration. The configuration table is used by the boot prom when running the initial self test and when initializing the type of NIOC/SIOC2 load modules. which is used when loading the NIOC/SIOC2.

The following modules can be initialized.

- Load module **nioc**.
- Load module **niocb**, only used by the **Supermax Operating System**.
- Load module **sioc2**.

The configuration should normally not be changed. A typical configuration for a NIOC 1600 looks like this:

```
Main memory (80000/100000):  0x100000
Buffer memory  (Y/N):        Yes
82586 installed  (Y/N):      Yes
Number of DUART modules 0-8: 0
NIOC or NIOCB (N/B):         N
```

Figure 3-6-2: Submenu for insert hardware configuration

P – Set test parameters

This entry is used to tell the program how many of the DUART modules that should be tested, when running test **F** or **G**.

U – Write to parallel printer

This test will write the menu text to the parallel printer interface. The operator must visually inspect, if the written text is correct.

M – Menu

Display the menu on the terminal.

V – Version

Display version of Diagnostic Program, version of boot prom (if possible) and elapsed time from last reset.

Q – Debugger

Go to debugging program. Return to Diagnostic Program by entering **GO <CR>**.

Z – Boot

Give master reset to the system. This will not work on the NIOC 1600.

Special plugs

In order to test one DUART module you must use eight 25 pin Cannon connectors strapped as shown to the left or eight 15 pin Cannon connectors strapped as shown to the right.

RS-232C plug 25 pin	RS-422 plug 15 pin
2 ←→ 3	2 ←→ 4
4 ←→ 5	3 ←→ 5
6 ←→ 20	9 ←→ 11
	10 ←→ 12

Table 3-6-1: Special plugs to test the SIOC2

Status register

If a bus error occurs, the status register contains information about the reason of the bus error.

Status bit	Description
STATUS(0)	Illegal bus
STATUS(1)	Illegal write
STATUS(2)	Segment too long
STATUS(3)	Bus error from bus
STATUS(4)	Time out
STATUS(7:5)	Not used

Table 3-6-2: Status register on NIOC/SIOC2

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SUPERMAX MODULES

CPU 68020

The purpose of this program is to evaluate the basic functions of the CPU 68020 module and the dynamic memory connected to it. The following functions can be tested with this program:

- The dynamic RAM connected to the CPU.
- The Memory Management Unit (MMU).
- All interrupts.
- All R/W registers.
- The Error Detection and Correction unit.
- The Program and Data cache.

The Diagnostic Program is able to run on a CPU with standard mounted straps.

Initialization

Included in the boot prom of the CPU 68020 is a thorough self test, which includes the following items:

- Running MC 68020 internal confidence test.
- Testing the Address Space Register.
- Testing the MMU memory, high speed.
- Initializing and testing memory from 0x0 – 0x100000, before copying the content of the prom to the memory.
- Determining the actual memory size.
- Initializing and testing memory from 0x100000 to top of memory.

- Testing program cache, data cache and physical address cache comparator.
- Running MC 68881 FPC internal confidence test.

Display codes

During the self test the front panel display will change according to the test currently running and the status of the test. The following table shows the possible display codes. F*n* means test *n* failed. P*n* means test *n* passed. When the display shows **Pd**, the CPU will enable the I/O bus in and then be ready to be booted. However it will continue the self test until finished. If any errors occur the display will keep the error code, but still try to run the program that has been loaded.

If no errors occur the CPU will start the program, which could be either the **Supermax Operating System** or the **Diagnostic Programs**. If it is the Diagnostic Programs the CPU is ready to be selected, when the display is turned off. If any errors occur, which means the display is not turned off, it is possible to get further information about the error, by typing the select sequence.

Passed	Failed	Test
P0	**F0**	Test stuck at high or low bits
P1	**F1**	Test data registers
P2	**F2**	Test control registers
P3	**F3**	Test address registers
P4	**F4**	Test status bits
P5	**F5**	68020 instruction test
P7	**F7**	Address Space Register
P8	**F8**	MMU memory
P9	**F9**	Testing memory 0x0 – 0x100000
PA		Just before copying prom
PC		Just after copying prom
Pd		Test caches
PE		Determine memory size
PF		Test memory to top
bo		Test MC 68881 FPC
	FA	Data error in memory
	FC	Single error in memory
	Fd	Error in cache test
	FE	Double fault in memory

Table 3-7-1: Display codes on CPU 68020

There are some additional display values used in the Diagnostic Programs.

- **bE** in the display indicates a bus error.
- **AE** in the display indicates an address error.
- **EE** in the display indicates any other exception.
- **Er** in the display indicates any other error.

Running the Diagnostic Program

When the initialization is successfully completed, and the CPU is booted, the CPU is ready to proceed with the more sophisticated parts of the test. After typing the select sequence for the CPU, that is going to be tested it should respond with the following message on the terminal:

cpu20 u > _ (**u** *is the unit number*)

When this prompt is displayed on the terminal, the CPU is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the CPU.

The following example shows the menu from a CPU with unit number 3:

```
cpu20 3   > M
 2 Mb memory. 68020 cache    = 'Enable'
              Program cache = 'Disable'. Data cache = 'Disable'
A - Test RAM High Speed
B - Test RAM Bit Test
C - Test RAM Address Bit Test
D - Test RAM Galloping Ones And Zeroes
E - Test RAM Byte Write
F - Test RAM Read Modify Write
G - Test MMU Memory
J - Test MMU Adder
K - Test MMU ASN - SEG
L - Test MMU Comparator
I - Test Interrupts
H - Test Cache
O - Repeat test(s)
S - Test All
X - Bustest. Passive unit
Y - Bustest. Active unit
M - Menu
V - Version
P - Set test parameters
Q - Debugger
Z - Boot
cpu20 3   >
```

Figure 3-7-1: Menu for CPU 68020

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test RAM. High Speed

This routine performs a fast test of the dynamic memory connected to the CPU module. It writes the value of the current address in memory. Then the memory content is read and compared to the value written and errors are indicated. All of this is repeated using the inverted value of the current address. The Error Detection and Correction circuitry is switched **ON** during this test.

B – Test RAM Bit Test

During this test every single bit in the main memory will be written with both *true* and *inverted* values. This is carried out by using long word operations with the following values.

Pass	Write value
1	0x00000001
2	0xFFFFFFFE
3	0x00000002
4	0xFFFFFFFD
--	----------
63	0x80000000
64	0x7FFFFFFF

All in all 64 passes. A plus (+) is written on the terminal for each pass. The Error Detection and Correction circuitry is switched **OFF** during this test.

C – Test RAM. Address Bit Test

During this test every single address bit is tested. This is done by writing one value in the current address if the selected address bit is zero and another value if the address bit is one. After that the memory is checked for correct content. The test is performed for address bits in the range 2-23 and the test runs four times, each time with two new write values.

Address bit	Pass 1	Pass 2	Pass 3	Pass 4
0	0x00000000	0xFFFFFFFF	0x00000000	0x42070220
1	0xFFFFFFFF	0x00000000	0x42070220	0x00000000

The reason for the value 0x42070220 during pass 3 and 4 is to make sure that the bits concerning the Error Detection and Correction circuitry, which is switched **ON** during this test, also will be tested.

D – Test RAM. Galloping Ones And Zeroes

This test is also performed 4 times. First of all the memory space is initialized with a default value. Then a galloping value is written in a certain address. Then all addresses which are neighbours to that first address are tested. They must still contain the default value. A neighbour is an address, which only differs in one bit from the original address. When all neighbours are tested the default value is written back in the original address. This is repeated for all addresses. The Error Detection and Correction circuitry is switched **ON** during this test.

Value	Pass 1	Pass 2	Pass 3	Pass 4
Default	0x00000000	0xFFFFFFFF	0x00000000	0x42070220
Galloping	0xFFFFFFFF	0x00000000	0x42070220	0x00000000

E – Test RAM. Byte Write

Because of the error correcting code it is much more difficult to write a byte (*8 bits*) or a word (*16 bits*) in memory, than it is to write a long word (*32 bits*). 32 bits are used to contain data and 7 bits contain the ECC code belonging to that data. If one byte or one word is to be written the CPU module will have to read a whole long word into a register, then write the new byte or word into the register and then write the long word back in memory. The 68020 is able to do a long word operation even though the address being referenced is not on a long word boundary. This is called **Dynamic Bus Sizing**.

In other words, if the 68020 writes to an address on a long word boundary, the long word will be written in one operation. But if the address is not on a long word boundary, the operation will be split into two operations as shown below:

Boundary	1. operation	2. operation
0	1 long word	
1	3 bytes	1 byte
2	1 word	1 word
3	1 byte	3 bytes

This test will write the long word 0xFFAA5500 using long word operations, but using the four different boundaries. By doing that both byte, word and long word operations will be performed.

F – Test RAM. Read Modify Write

The MC68020 microprocessor has a feature which makes it possible in one operation to read a byte in memory, test the byte, set one bit in the byte and to write it back again. This is called *Read-Modify-Write* and this test will initialize memory with a default value and then perform the *Test And Set (TAS)* instruction on all memory locations and then check for correct memory content.

G – Test MMU Memory

The MMU memory consists of 16 kB static RAM. This memory can be tested using the same routines as those for the dynamic RAM. When you select this test the above mentioned tests A, B, C and D will be performed on the MMU memory.

J – Test MMU Adder

The 16 bit adder is built from four 4 bit adders, which can be tested separately. This routine tests each 4 bit section of the adder in the MMU. The main memory is initialized in such a way that each double word in memory contains its own logical address. The memory is accessed using the relocating capabilities of the MMU. The physical address is calculated by adding the offset stored in the MMU to the logical address used when accessing the main memory. The calculated physical address is compared to the real physical address as read in the main memory.

K – Test MMU ASN – SEG

This routine tests that the MMU is addressed correctly by Address Space Number (ASN) and Segment Number (SEG). The segment descriptor in the MMU memory, pointed to by one combination of ASN and SEG, will point to one specific memory location, which will be initialized with one value. All other segment descriptors will point to another location, initialized with a different value. Then a memory access is made using the relocating capabilities of the MMU, and using the specific ASN and SEG, and the value read is compared to the expected value. This is repeated using all combinations of ASN and SEG.

L – Test MMU Comparator

This routine tests the 7 bit comparator used in the memory protection capabilities of the MMU. It accesses main memory using different Block Numbers (BN) and different Sizes in the MMU while the checking facilities of the MMU are enabled. This is done in two different ways:

- **Normal Length Check.**

  Whenever BN > Size the memory access is illegal and a bus error should occur and if BN < = Size the memory access is legal and no bus error should occur.

- **Stack Length Check.**
  Whenever BN < = Size the memory access is illegal and a bus error should occur and if BN > Size the memory access is legal and no bus error should occur.

Besides the comparator test there is an access code test. This one also runs in two different ways:

- When the segment is used to access internal memory, it is tested that the following four conditions will give the expected bus errors.
  - Supervisor read allowed
  - Supervisor write allowed
  - User read allowed
  - User write allowed
- When the segment is used to access the I/O bus, it is tested that the following four conditions will give the expected bus errors.
  - Supervisor program allowed
  - User program allowed
  - User data allowed
  - User address reference allowed

I – Test Interrupts

This routine tests the interrupt circuit by setting all 2048 external interrupts and enabling all four interrupt levels and then checking that the circuitry can decode all interrupts. This is repeated, but only enabling three levels checking that the three levels are decoded and the last one is not. After that, two levels and then one level are tested in the same way.

The timer interrupt is also tested and you can calculate the time between timer interrupts by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. Normally you should end up with 40 ms.

H – Test Cache

On the 68020 CPU board there are two caches, a program cache and a data cache. The size of the caches depends upon the memory board connected to the CPU and on some straps on the CPU board. Before testing, the program will determine the cache size and print the information on the terminal when starting the test.

First, the program cache is used as a data cache and the test will exercise the cache memory by reading data into it and test the content. After that the cache comparator will be tested. That is done by initializing the tag fields in the comparator and testing one field for *hit* and all neighbour fields for *no hit*, repeating this for all fields. Second, the data cache goes through the same test as above.

Third the cache comparator located on the physical address bus is tested. This is done by initializing the tag field with consecutive physical addresses and then reading and writing the field again to see if there is a match from the comparator. The time used for the third test depends upon the actual memory size.

O – Repeat test(s)

All of the above mentioned tests will run one time through when selected. If, when selecting test(s), this one (O) is also selected, the test(s) will repeat itself (themselves) until otherwise canceled.

S – Test all

When selecting this command, the following tests will be executed in the order written. A, B, C, D, E, F, G, J, K, L, I and H. It is possible to add the *Repeat test* option *(O)* to this one.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

M – Menu

Display the menu on the terminal. The first line contains the actual memory size.

V – Version

Display version, date and elapsed time from last reset, on the form hh:mm:ss.

P – Set test parameters

This entry is used to set start address and end address for the memory tests and to set the state of the different caches during the tests. The start and end address has to be on hexadecimal form. If nothing is entered, the program will use the default values shown on the terminal. Entering illegal addresses will not be allowed.

After reset the three caches have the following status:

- Program cache 'Disabled'
- Data cache 'Disabled'
- 68020 cache 'Enabled'

These values will be in effect on all tests except *H* (test cache). It is possible to enable or disable the three caches individually by selecting *P*. The cache status is shown whenever the menu is displayed.

NOTE

If the external cache is enabled the maximum amount of memory that can be tested is 16 Mb. In order to test more than 16 Mb you must disable the external cache. During Non-operator mode only 16 Mb will be tested.

Q – Debugger

Go to debugging program. Return to Diagnostic Program by entering **GO <CR>**.

Z – Boot

Give master reset to the system.

Status register

If a bus error occurs, the status register contains information about the reason of the bus error.

Status bit	Description
STATUS(0)	Illegal user read
STATUS(1)	Illegal user write
STATUS(2)	Illegal user data access to the I/O bus
STATUS(3)	Illegal user address reference
STATUS(4)	Illegal supervisor read
STATUS(5)	Illegal supervisor write
STATUS(6)	Illegal supervisor program access to the I/O bus
STATUS(7)	Illegal user program access to the I/O bus
STATUS(8)	Segment too long, normal length check
STATUS(9)	Segment too long, stack length check
STATUS(10)	Double fault in memory
STATUS(11)	No memory
STATUS(12)	No floating point unit installed
STATUS(13)	Time out
STATUS(14)	Bus error from bus
STATUS(15)	Illegal read modify write cycle to the I/O bus

Table 3-7-2: Status register on CPU 68020

NOTE

The bits in STATUS(15:0) are active low.

SUPERMAX MODULES

DIOC3

The purpose of this program is to evaluate the basic functions of the DIOC3 4000 module, which is the third version of the Disk Input Output Controller in the Supermax card family. The following functions can be tested using this program:

- Program memory
- Cache memory
- Memory mapper (SRAM)
- Block Transport Unit (BTU)
- Peripheral interface
- Interrupt
- Peripheral units

The program is able to run on a DIOC3 with standard mounted straps.

Initialization

Included in the boot prom of the DIOC3 is a thorough self test, which includes the following items:

- Running MC 68020 internal confidence test.
- Testing the SRAM memory.
- Initializing and testing memory from 0x0 – 0x100000, before copying the content of the EPROM to the memory.
- Determining the actual size of the cache memory. Initializing and testing the cache memory.

After reset the red LED3 will be turned **ON**. The self test runs for appx. 25 seconds and if it runs without any errors, the red LED3 will be turned **OFF**, and the DIOC3 will start the boot procedure. If any errors are found the red LED3 will stay **ON** and information about the error can be obtained when selecting the DIOC3 on the service port. The DIOC3 boot prom version 4.0 90.09.01 has the following boot procedure:

- If the DIOC3 discovers, that another DIOC in the system has booted the system, it will start the program loaded into its memory. If the DIOC3 has not been loaded it will try to boot the system.
- First it tries to access the 5¼" floppy disk located on id 1, using DDE 560 kbyte or PC/AT 1.2 Mbyte diskette format, in order to boot from that unit.
- Then it tries to access the 3½" floppy disk located on id 0, using PC/AT 720 kbyte or PC/AT 1.44 Mbyte diskette format, in order to boot from that unit.
- If no floppy disk is installed it tries to access all the winchester disks, located on SCSI 0 and 1 in order to boot from a winchester disk. The boot prom supports boot from mirrored, striped and dual host disk systems.
- If the DIOC3 discovers a hard error on the floppy disk or the winchester disk or no boot information is found, the red LED3 will be turned **ON**.
- If boot information is not located on neither the floppy disk nor the winchester disk, the DIOC3 will not load any programs, but still the DIOC3 can be loaded from another DIOC in the system.
- When all units have been booted the DIOC3 starts its own program which can be either the **Supermax Operating System** or the **Diagnostic Programs**.

Running the Diagnostic Program

When the initialization is successfully completed, the DIOC3 is ready to proceed with the more sophisticated parts of the test. After typing the select sequence for the DIOC3, that is going to be tested it should respond with the following message on the terminal:

`dioc3 u  > _` (**u** *is the unit number*)

When this prompt is displayed on the terminal, the DIOC3 is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the DIOC3.

The example shows the menu from a DIOC3 with unit number E:

```
dioc3 E   > M
1 Mbyte program memory. 08 Mbyte cache memory.

A - Test program memory
B - Test cache memory
C - Test SRAM memory
D - Test SRAM mapping
E - Test BTU transport
F - Test BTU and SCSI transport
G - Test interrupt
S - Test all
O - Repeat test(s)
X - Bustest. Passive unit
Y - Bustest. Active unit
K - Set boot pointer on winchester
L - Set test time for Non-Operator Mode
N - Set tests for Non-Operator Mode
P - Set test parameters
T - Test peripheral units
U - Display configuration
Q - Debugger
V - Version
M - Menu

dioc3 E   >
```

Figure 3-8-1: Menu for DIOC3

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test program memory

The program memory consists of minimum 1 Mb dynamic ram. This memory will be tested using the different tests mentioned below. It is possible to select one or more tests to be performed if selecting *P*.

- **High Speed.** This routine performs a fast test of the dynamic memory. It writes the value of the current address in the memory. Then the memory content is read and compared to the value written and errors are indicated. All of this is repeated using the inverted value of the current address.
- **Bit Test.** During this test every single bit in the main memory will be written with both *true* and *inverted* values. This is carried out by using long word operations with the following values. All in all 64 passes. A plus (+) is written on the terminal for each pass.

Pass	Write value
1	0x00000001
2	0xFFFFFFFE
3	0x00000002
4	0xFFFFFFFD
--	----------

- **Address Bit Test.** During this test every single address bit is tested. This is done by writing one value in the current address if the selected address bit is zero and another value if the address bit is one.

Address bit	Pass 1	Pass 2
0	0x00000000	0xFFFFFFFF
1	0xFFFFFFFF	0x00000000

After that the memory is checked for correct content. The test is performed for address bits in the range 2-24 and the test runs two times, each time with two new write values.

- **Galloping Ones And Zeroes.** This test is also performed 2 times. First of all the memory space is initialized with a default value. Then a galloping value is written in a certain address. Then all addresses which are neighbours to that first address are tested. They must still contain the default value. A neighbour is an address, which only differs in one bit from the original address.

  When all neighbours are tested the default value is written back in the original address. This is repeated for all addresses.

Value	Pass 1	Pass 2
Default	0x00000000	0xFFFFFFFF
Galloping	0xFFFFFFFF	0x00000000

- **Byte Write.** The MC68020 is able to do a long word operation even though the address being referenced is not on a long word boundary. This is called **Dynamic Bus Sizing**. In other words, if the MC68020 writes to an address on a long word boundary, the long word will be written in one operation. But if the address is not on a long word boundary, the operation will be split into two operations as shown below.

Boundary	1. operation	2. operation
0	1 long word	
1	3 bytes	1 byte
2	1 word	1 word
3	1 byte	3 bytes

  This test will write the long word 0xFFAA5500 using long word operations, but using the four different boundaries. By doing that both byte, word and long word operations will be performed.

- **Read-Modify-Write.** The MC68020 microprocessor has a feature which makes it possible in one operation to read a byte in memory, test the byte, set one bit in the byte and to write it back again.

This is called *Read-Modify-Write* and this test will initialize memory with a default value and then perform the *Test And Set (TAS)* instruction on all memory locations and then check for correct memory content.

B – Test cache memory

The cache memory consists of between 4 Mb and 32 Mb of dynamic memory. This memory will be tested using the following routines as described in test *A*.

- **High Speed.**
- **Bit Test.**
- **Address Bit Test.**
- **Galloping Ones And Zeroes.**
- **Byte Write.**
- **Read Modify Write.**

It is possible to select one or more tests to be performed if selecting *P*.

C – Test SRAM memory

The SRAM consists of 4 kb static memory. This memory will be tested using the following routines as described in test *A*.

- **High Speed.**
- **Bit Test.**
- **Address Bit Test.**
- **Galloping Ones And Zeroes.**

D – Test SRAM mapping

This test will check that the SRAM memory mapper can map correctly. A counter is written in the SRAM and each long word in the cache memory is written with the address of that long word. Then accesses are made to the cache memory through the memory mapper, and it is checked that the reference goes to the correct location in the memory.

E – Test BTU transport

The BTU (Block Transport Unit) is tested for correct function. The BTU will move a block of data from the cache memory through the I/O bus and back into the cache memory.

256 kb of the cache memory is initialized with an incrementing counter. This block is moved using the BTU to a location 256 kb further up in the memory space. Then it is checked that the block has been moved correctly. Then a new counter is written in the beginning of the cache memory. This block is moved to a location 512 kb further up in the memory space and it is checked. This will be repeated until no more cache memory is available. The whole sequence will then be repeated using a decrementing counter. While the BTU is moving the block of data, the MC68020 will access the cache memory in order to make sure that the MC68020 and the BTU can share the memory accesses.

The test will run two times, each with different burst counts. Burst count is the number of long words transferred in one I/O bus access. Normally that number is 1, but on the DIOC3 it can be changed in order to increase performance. The default values used in this test are 1 and 16. The last value can be changed if selecting *P*.

F – Test BTU and SCSI transport

The purpose of this test is primarily to check the two SCSI channels, SCSI 0 and SCSI 1, on the DIOC3. Secondly to check the concurrent running of the DMA channels concerning the BTU, SCSI 0 and SCSI 1. In order to run this test you must connect a 50 pin flat cable between SCSI 0 and SCSI 1. The test actually runs as two independent processes, one for the SCSI test and one for the BTU test.

SCSI test — During this test the SCSI 0 is the initiator and SCSI 1 is the target. SCSI 0 will transfer data to and from SCSI 1, as if SCSI 1 was any standard SCSI unit, issuing read and write commands.

BTU test — The BTU will move a block of data from the cache memory through the I/O bus and back into the cache memory.

The two tests use the same algorithm when testing.

- Initialize block 1.
- Move block 1 to block 2 using a write command.
- Move block 2 to block 3 using a read command.
- Compare block 1 and block 3.

The test is completed when both the SCSI test and the BTU test is completed.

G – Test interrupt

This routine tests the interrupt circuit by setting all four external interrupts and enabling all four interrupt levels and then checking that the circuitry can decode all interrupts. This is repeated, but only enabling three levels checking that the three levels are decoded and the last one is not. After that, two levels and then one level are tested in the same way.

The timer interrupt is also tested and you can calculate the time between timer interrupts by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. Normally you should end up with 50 ms.

S – Test all

When selecting this command, the following tests will be executed in the order written: A, B, C, D, E and G. It is possible to add the **Repeat test** option *(O)* to this one.

O – Repeat test(s)

All of the above mentioned tests will run one time through when selected. If, when selecting test(s), this one *(O)* is also selected, the test(s) will repeat itself (themselves) until otherwise canceled.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

K – Set boot pointer on winchester

It is possible to change the boot pointer on the winchester disk on SCSI 0 ID 0. The boot pointer is a pointer to a logical disk where the boot programs are located. If the winchester disk on SCSI 0 ID 0 is part of a mirrored disk system, the boot pointer will also be saved on the winchester located on SCSI 1 ID 0.
There are up to 4 pointers, which can be selected. Normally **Pointer 0** points to the **Supermax Operating System** and **Pointer 1** points to the **Diagnostic Programs** and **Pointer 2 and 3** are not used. Selecting **Default** will set the pointer to the temporary pointer, which normally contains the one that was active before the Diagnostic Programs were loaded. It is also possible to clear the boot pointer, if winchester boot is not wanted.

L – Set test time for Non-Operator Mode

This is used if the time for running in **Non-Operator Mode** is to be changed. Both the time for the internal test and the time for the bus test can be set individually. The program will ask if you want to use the default time. If the answer is **No**, you will be asked to type in the new values. It is not possible to use this command on a DIOC3, which is **not** the Master unit.

N – Set tests for Non-Operator Mode

This command is used to tell the program, which tests should be added, when running Non-Operator Mode. The test are changed on all DIOC3 and MIOC modules. The following test can be added to the Non-Operator test:

- Test winchester disk(s) mounted on DIOC3 modules. The test can be either CRC test or verify mirrored disks.
  If the Diagnostic Programs were booted from the winchester disk, the default is CRC test. If the Diagnostic Programs were booted from the floppy disk, the default is no disk test, and if you change that to test disk(s), you have to check the error buffer manually, because no errors are reported to the terminal.
- External loopback on MIOC (TERM, HDLC) submodule. Default is **No**
- External loopback on MIOC (Ethernet, ISDN) submodule. Default is **No**.

It is not possible to use this command on a DIOC3, which is **not** the Master unit.

P – Set test parameters

This entry is used to set up various parameters for the different tests. The following list shows what can be changed.

- Start address and end address for the memory tests.
- Which memory tests will be performed.
- BTU burst count.
- Set MC68020 cache enable/disable.
- Write Bus access.

T – Test peripheral units

The Diagnostic Program for peripheral units will always be resident in the DIOC3. Refer to "Chapter 7–1 Peripheral test for DIOC3", to see the detailed description of the peripheral test.

U – Display configuration

A configuration list will be written on the terminal, containing information about Diagnostic Programs version and which units, type and unit number, were in the system when it was booted. It is not possible to use this command on a DIOC3, which is **not** the Master unit.

Q – Debugger

Go to debugging program. Return to Diagnostic Program by entering **GO <CR>**.

V – Version

Display version of Diagnostic Program, version of boot prom (if possible) and elapsed time from last reset.

M – Menu

Display the menu on the terminal.

Status register

If a bus error occurs, the status register contains information about the reason of the bus error.

Status bit	Description
SR0(0)	Parity error in local memory
SR0(1)	The ERROR signal in the I/O bus is active
SR0(2)	Time out
SR0(3)	Illegal Read-Modify-Write
SR0(4)	Bus error from I/O bus
SR0(5)	Parity error in cache memory
SR0(6)	The POWER FAIL signal is active
SR0(7)	Selected floppy disk drive is ready
SR1(0)	Parity error in cache memory.
SR1(1)	Parity error in cache memory during a BTU transport.
SR1(2)	Parity error in cache memory during a SCSI0 transport.
SR1(3)	Parity error in cache memory during a SCSI1 transport.
SR1(4)	Parity error in cache memory during a floppy transport.
SR1(5)	Time out during a BTU cycle.
SR1(6)	Bus error received during a BTU cycle.
SR1(7)	BTU error, SR1(6) or SR1(5) is active.

Table 3-8-1: Status register 0 and 1 on DIOC3

SUPERMAX MODULES

CPU 68030

The purpose of this program is to evaluate the basic functions of the CPU 68030 4100 module and the dynamic memory connected to it. The following functions can be tested with this program:

- The dynamic RAM connected to the CPU.
- The Active Memory Management Unit (AMMU).
- The Passive Memory Management Unit (PMMU).
- All interrupts.
- The Error Detection and Correction unit.
- The external physical cache.

The Diagnostic Program is able to run on a CPU with standard mounted straps.

Initialization

Included in the boot prom of the CPU 68030 is a thorough self test, which includes the following items:

- Running MC 68030 internal confidence test.
- Testing the PMMU/AMMU memory, high speed.
- Initializing and testing memory from 0x0 – 0x100000, before copying the content of the prom to the memory.
- Determining the actual memory size.
- Initializing and testing memory from 0x100000 to top of memory.

- Testing the external cache.
- Running MC 68881/68882 FPC internal confidence test.

Display codes

During the self test the front panel display will change according to the test currently running and the status of the test. The following table shows the possible display codes. F*n* means test *n* failed. P*n* means test *n* passed. When the display shows **Pd**, the CPU will enable the I/O bus in and then be ready to be booted. However it will continue the self test until finished. If any errors occur the display will keep the error code, but still try to run the program that has been loaded.

If no errors occur the CPU will start the program, which could be either the **UNIX Operating System** or the **Diagnostic Programs**. If it is the Diagnostic Programs the CPU is ready to be selected, when the display is turned off. If any errors occur, which means the display is not turned off, it is possible to get further information about the error, by typing the select sequence.

Passed	Failed	Test
P0	**F0**	Test stuck at high or low bits
P1	**F1**	Test data registers
P2	**F2**	Test control registers
P3	**F3**	Test address registers
P4	**F4**	Test status bits
P5	**F5**	68030 instruction test
P7		USART initialized
P8	**F8**	PMMU/AMMU memory
P9	**F9**	Testing memory 0x0 – 0x100000
PC		Just after copying eprom
Pd		Test caches
PE		Determine memory size
PF		Test memory to top
bo	**FF**	Test MC 68881/68882 FPC
	FA	Data error in memory
	FC	Single error in memory
	Fd	Error in cache test
	FE	Double fault in memory

Table 3-9-1: Display codes on CPU 68030

There are some additional display values used in the Diagnostic Programs.

- **bE** in the display indicates a bus error exception.
- **AE** in the display indicates an address error exception.
- **EE** in the display indicates any other exception.
- **Er** in the display indicates any other error.

Running the Diagnostic Program

When the initialization is successfully completed, and the CPU is booted, the CPU is ready to proceed with the more sophisticated parts of the test. After typing the select sequence for the CPU, that is going to be tested it should respond with the following message on the terminal:

cpu30 u > _ (**u** *is the unit number*)

When this prompt is displayed on the terminal, the CPU is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the CPU.

The example shows the menu from a CPU with unit number 3, 4 Mb of memory and CPU clock frequency of 33.3 MHz:

```
cpu30 3   > M
04 Mb memory. External cache  = 'Disable'
33.3 MHz       68030 prg.cache = 'Enable' 68030 data cache = 'Disable'
A - Test RAM High Speed
B - Test RAM Bit Test
C - Test RAM Address Bit Test
D - Test RAM Galloping Ones And Zeroes
E - Test RAM Byte Write
F - Test RAM Read Modify Write
G - Test AMMU Memory
J - Test PMMU Memory
K - Test AMMU Mapping
L - Test PMMU Mapping
I - Test Interrupt
H - Test External Cache
S - Test All
O - Repeat test(s)
X - Bustest. Passive unit
Y - Bustest. Active unit
P - Set test parameters
Q - Debugger
V - Version
Z - Boot
M - Menu
cpu30 3   >
```

Figure 3-9-1: Menu for CPU 68030

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test RAM. High Speed

This routine performs a fast test of the dynamic memory connected to the CPU module. It writes the value of the current address in memory. Then the memory content is read and compared to the value written and errors are indicated. All of this is repeated using the inverted value of the current address. The Error Detection and Correction circuitry is switched **ON** during this test.

B – Test RAM Bit Test

During this test every single bit in the main memory will be written with both *true* and *inverted* values. This is carried out by using long word operations with the following values.

Pass	Write value
1	0x00000001
2	0xFFFFFFFE
3	0x00000002
4	0xFFFFFFFD
--	----------
63	0x80000000
64	0x7FFFFFFF

All in all 64 passes. A plus (+) is written on the terminal for each pass. The Error Detection and Correction circuitry is switched **OFF** during this test.

C – Test RAM. Address Bit Test

During this test every single address bit is tested. This is done by writing one value in the current address if the selected address bit is zero and another value if the address bit is one. After that the memory is checked for correct content. The test is performed for address bits in the range 2-27 and the test runs four times, each time with two new write values.

Address bit	Pass 1	Pass 2	Pass 3	Pass 4
0	0x00000000	0xFFFFFFFF	0x00000000	0x42070220
1	0xFFFFFFFF	0x00000000	0x42070220	0x00000000

The reason for the value 0x42070220 during pass 3 and 4 is to make sure that the bits concerning the Error Detection and Correction circuitry, which is switched **ON** during this test, also will be tested.

D – Test RAM. Galloping Ones And Zeroes

This test is also performed 4 times. First of all the memory space is initialized with a default value. Then a galloping value is written in a certain address. Then all addresses which are neighbours to that first address are tested. They must still contain the default value. A neighbour is an address, which only differs in one bit from the original address. When all neighbours are tested the default value is written back in the original address. This is repeated for all addresses. The Error Detection and Correction circuitry is switched **ON** during this test.

Value	Pass 1	Pass 2	Pass 3	Pass 4
Default	0x00000000	0xFFFFFFFF	0x00000000	0x42070220
Galloping	0xFFFFFFFF	0x00000000	0x42070220	0x00000000

E – Test RAM. Byte Write

Because of the error correcting code it is much more difficult to write a byte (*8 bits*) or a word (*16 bits*) in memory, than it is to write a long word (*32 bits*). 32 bits are used to contain data and 7 bits contain the ECC code belonging to that data. If one byte or one word is to be written the CPU module will have to read a whole long word into a register, then write the new byte or word into the register and then write the long word back in memory.

The 68030 is able to do a long word operation even though the address being referenced is not on a long word boundary. This is called **Dynamic Bus Sizing**. In other words, if the 68030 writes to an address on a long word boundary, the long word will be written in one operation. But if the address is not on a long word boundary, the operation will be split into two operations as shown below.

Boundary	1. operation	2. operation
0	1 long word	
1	3 bytes	1 byte
2	1 word	1 word
3	1 byte	3 bytes

This test will write the long word 0xFFAA5500 using long word operations, but using the four different boundaries. By doing that both byte, word and long word operations will be performed.

F – Test RAM. Read Modify Write

The MC68030 microprocessor has a feature which makes it possible in one operation to read a byte in memory, test the byte, set one bit in the byte and to write it back again. This is called *Read-Modify-Write* and this test will initialize memory with a default value and then perform the *Test And Set (TAS)* instruction on all memory locations and then check for correct memory content.

G – Test AMMU Memory

The AMMU memory consists of 2 kB static RAM. This memory can be tested using the same routines as those for the dynamic RAM. When you select this test the above mentioned tests A, B, C and D will be performed on the AMMU memory.

J – Test PMMU Memory

The PMMU memory consists of 32 kB static RAM. This memory can be tested using the same routines as those for the dynamic RAM. When you select this test the above mentioned tests A, B, C and D will be performed on the PMMU memory.

K – Test AMMU Mapping

One entry at a time is set up in the AMMU. This entry points to a valid memory location all other entries points to invalid memory locations. Then an I/O bus access to the unit itself is made. This access goes through the AMMU to the I/O bus and back into the unit and into the memory. Then it is checked that the access went to the valid memory location. This is repeated using 256 different values in the memory location. All this is repeated for 1024 entries in the AMMU.

L – Test PMMU Mapping

One entry at a time is set up in the PMMU. This entry points to a valid memory location all other entries points to invalid memory locations. Then an I/O bus access to the unit itself is made. This access goes through the AMMU to the I/O bus and back into the unit, through the PMMU and into the memory. Then it is checked that the access went to the valid memory location. This is repeated using 256 different values in the memory location. All this is repeated for all 16384 entries in the PMMU.

I – Test Interrupt

This routine tests the interrupt circuit by setting all 2048 external interrupts and enabling all four interrupt levels and then checking that the circuitry can decode all interrupts. This is repeated, but only enabling three levels checking that the three levels are decoded and the last one is not. After that, two levels and then one level are tested in the same way. The test is performed for both start address 0x2000 and 0x10000.

The timer interrupt is also tested and you can calculate the time between timer interrupts by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. Normally you should end up with 40 ms.

H – Test Cache

On the 68030 CPU board there are three caches, an on-chip program cache, an on-chip data cache and an external cache, normally used as a physical cache. When testing the external cache, it is programmed to be a data cache only. The size of the external cache is either 64 kb or 128 kb. Before testing, the program will determine the cache size and print the information on the terminal when starting the test.

The test will exercise the cache memory by reading data into it and then test the content. After that the cache comparators will be tested. That is done by initializing the tag fields in the comparator and testing one field for *hit* and all neighbour fields for *no hit*, repeating this for all fields. The time used for the test depends upon the actual memory size.

S – Test all

When selecting this command, the following tests will be executed in the order written. A, B, C, D, E, F, G, J, K, L, I and H. It is possible to add the *Repeat test* option *(O)* to this one.

O – Repeat test(s)

All of the above mentioned tests will run one time through when selected. If, when selecting test(s), this one *(O)* is also selected, the test(s) will repeat itself (themselves) until otherwise canceled.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

P – Set test parameters

This entry is used to set start address and end address for the memory tests and to set the state of the different caches during the tests. The start and end address has to be on hexadecimal form. If nothing is entered, the program will use the default values shown on the terminal. Entering illegal addresses will not be allowed.

After reset the three caches have the following status:

- 68030 program cache 'Enabled'
- 68030 data cache 'Disabled'
- External cache 'Disabled'

These values will be in effect on all tests except *H* (test cache). It is possible to enable or disable the three caches individually by selecting *P*. When the external cache is enabled it is possible to select it as a physical cache or as a data cache only. The cache status is shown whenever the menu is displayed.

Q – Debugger

Go to debugging program. Return to Diagnostic Program by entering **GO <CR>**.

V – Version

Display version, date and elapsed time from last reset.

Z – Boot

Give master reset to the system.

M – Menu

Display the menu on the terminal. The first line contains information about the actual memory size and the state of all the caches.

Status register

If a bus error occurs, the status register contains information about the reason of the bus error.

Status bit	Description
STR(0)	Not used
STR(1)	Not used
STR(2)	Double fault in memory
STR(3)	Double fault in memory from a cache entry
STR(4)	Time out
STR(5)	No memory
STR(6)	Illegal read/modify/write cycle to the I/O bus
STR(7)	Bus error from the I/O bus
STR(8)	FPC not present
STR(9)	FPC disabled
STR(10)	Illegal breakpoint address
STR(11)	Illegal coprocessor address
STR(12)	Not used
STR(13)	Not used
STR(14)	Not used
STR(15)	Not used

Table 3-9-2: Status register on CPU 68030

NOTE

The bits in STR(7:2) are active high. The bits in STR(11:8) are active low.

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SUPERMAX MODULES

CPU R3000

The purpose of this program is to evaluate the basic functions of the CPU R3000 4500 module and the dynamic memory connected to it. The following parts can be tested with this program:

- The dynamic memory connected to the CPU.
- The Active Memory Management Unit (AMMU).
- The Passive Memory Management Unit (PMMU).
- All interrupts.
- The Error Detection and Correction unit.
- The instruction cache.
- The data cache.
- The Floating Point Accelerator, FPA.
- The Translation Lookaside Buffer, TLB.
- The Write Buffers.

Initialization

Included in the boot prom of the CPU R3000 is a thorough self test, which includes the following items:

- Initializing and testing memory from 0x0 – 0x200000.
- Testing the Instruction and Data Cache.
- Testing the Write Buffer.
- Testing the Translation Lookaside Buffer.

- Testing the Address Mapping Register, AMR.
- Testing the Interrupt Mask Register, IMR.
- Testing the PMMU/AMMU memory, high speed.
- Determining the actual memory size.
- Testing the Floating Point Accelerator.
- Initializing and testing memory from 0x200000 to top of memory.

Display codes

During the self test the front panel display will change according to the test currently running and the status of the test. The following table shows the possible display codes. F*n* means test *n* failed. P*n* means test *n* passed. When the display shows **PA**, the CPU will enable the *I/O Bus In* and then be ready to be booted. However the self test will continue until completed. If any errors occur the display maintains the error code, and the CPU still attempting to run the program, which has been loaded.

If no errors occur the CPU will start the program, which could be either the **Supermax Operating System** or the **Diagnostic Programs**. If it is the Diagnostic Programs, the CPU is ready to be selected, when the display is turned off. If any errors occur, which means the display is not turned off, it is possible to obtain further information about the error, by typing the select sequence.

Passed	Failed	Test
P0		Writing hello message
P1	**F1**	Test memory 0 – 2 Mb
P2	**F2**	Test cache
P3	**F3**	Test write buffer
P4	**F4**	Test block refill
P5	**F5**	Test TLB
P6	**F6**	Test IMR
P7	**F7**	Test AMR
P8	**F8**	Test AMMU memory
P9	**F9**	Test PMMU memory
PA		Ready to boot
	FA	Single fault in memory
PC	**FC**	Test FPC
Pd	**Fd**	Test main memory > 2 Mb
	FE	UTLB exception error
	FF	Normal exception error
bo		Self test completed
r3		Running debugger

Table 3-10-1: Display codes on CPU R3000

There are some additional display values used in the Diagnostic Programs.

- **bE** in the display indicates a bus error exception.
- **AE** in the display indicates an address error exception.
- **EE** in the display indicates any other exception.
- **Er** in the display indicates any other error.

Running the Diagnostic Program

When the initialization is successfully completed, and the CPU is booted, the CPU is ready to proceed with the more sophisticated parts of the test. After typing the select sequence for the CPU, which will be tested, it should respond with the following message on the terminal:

r3000 u > _ (**u** *is the unit number*)

When this prompt is displayed on the terminal, the CPU is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the CPU.

The example shows the menu from a CPU with unit number 3 and 8 Mb of memory:

```
r3000 3   > M
8 Mb memory. Instruction cache = 'Disable' Data cache = 'Disable'
A - Test RAM High Speed
B - Test RAM Bit Test
C - Test RAM Address Bit Test
D - Test RAM Galloping Ones And Zeroes
E - Test RAM Byte Write
F - Test RAM Read Modify Write
G - Test AMMU Memory
J - Test PMMU Memory
K - Test AMMU Mapping
L - Test PMMU Mapping
I - Test Interrupt
H - Test Instruction/Data cache
N - Test Write Buffer
T - Test FPA
S - Test All
O - Repeat test(s)
X - Bustest. Passive unit
Y - Bustest. Active unit
P - Set test parameters
Z - Boot    Q - Debugger
M - Menu    V - Version
r3000 3   >
```

Figure 3-10-1: Menu for CPU R3000

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test RAM. High Speed

This routine performs a fast test of the dynamic memory connected to the CPU module. The value of the current address is written in the memory. The memory content is then read and compared to the value written and errors are indicated. All of this is repeated using the inverted value of the current address. The Error Detection and Correction circuitry is switched **ON** during this test.

B – Test RAM Bit Test

During this test every single bit in the main memory will be written with both *true* and *inverted* values. This is carried out by using long word operations with the following values.

Pass	Write value
1	0x00000001
2	0xFFFFFFFE
3	0x00000002
4	0xFFFFFFFD
--	----------
63	0x80000000
64	0x7FFFFFFF

All in all 64 passes. A plus (+) is written on the terminal for each pass. The Error Detection and Correction circuitry is switched **OFF** during this test.

C – Test RAM. Address Bit Test

During this test every single address bit is tested. This is done by writing one value in the current address if the selected address bit is zero and another value if the address bit is one. After that the memory is checked for correct content. The test is performed for address bits in the range 2-27 and the test runs four times, each time with two new write values.

Address bit	Pass 1	Pass 2	Pass 3	Pass 4
0	0x00000000	0xFFFFFFFF	0x00000000	0x42070220
1	0xFFFFFFFF	0x00000000	0x42070220	0x00000000

The reason for the value 0x42070220 during pass 3 and 4 is to make sure that the bits concerning the Error Detection and Correction circuitry, which is switched **ON** during this test, also will be tested.

D – Test RAM. Galloping Ones And Zeroes

This test is also performed 4 times. First of all the memory space is initialized with a default value. Then a galloping value is written in a certain address. Then all addresses which are neighbours to that first address are tested. They must still contain the default value. A neighbour is an address, which only differs in one bit from the original address. When all neighbours are tested the default value is written back in the original address.

This is repeated for all addresses. The Error Detection and Correction circuitry is switched **ON** during this test.

Value	Pass 1	Pass 2	Pass 3	Pass 4
Default	0x00000000	0xFFFFFFFF	0x00000000	0x42070220
Galloping	0xFFFFFFFF	0x00000000	0x42070220	0x00000000

E – Test RAM. Byte Write

Because of the error correcting code it is much more difficult to write a byte (*8 bits*) or a word (*16 bits*) in memory, than it is to write a long word (*32 bits*). 32 bits are used to contain data and 7 bits contain the ECC code belonging to that data. If one byte or one word is to be written the CPU module will have to read a whole long word into a register, then write the new byte or word into the register and then write the long word back in memory.

This test is carried out by using byte operations. One byte in each long word in the whole memory is written using the value 0xFF. Then all four bytes in each long word is checked. The memory is cleared before each pass, using long word operations.

Pass	Byte number
1	Byte 0
2	Byte 1
3	Byte 2
4	Byte 3

F – Test RAM. Read Modify Write

The CPU R3000 module has a feature which makes it possible to lock the memory. This enables the programmer to simulate a *Read-Modify-Write* cycle by doing the following:

- Lock the memory.
- Read data in memory.
- Check and modify the data.
- Write the data back.

The write operation will automatically unlock the memory again. This test will initialize memory with a default value and then simulate the *Test And Set (TAS)* instruction on all memory locations and then check for correct memory content.

NOTE

If the instruction cache is disabled it is not possible to simulate the *Read-Modify-Write* cycle correctly. In that case the test is carried out, without locking the memory.

G – Test AMMU Memory

The AMMU memory consists of 2 Kb static RAM. The memory is organized as 2 K × 8 bit, but each byte occupies 4 bytes in the address space. This memory can be tested using the same routines as those for the dynamic RAM. When you select this test the above mentioned tests A, B, C and D will be performed on the AMMU memory.

J – Test PMMU Memory

The PMMU memory consists of 32 Kb static RAM. The memory is organized as 16 K × 16 bit, but each word occupies 4 bytes in the address space. This memory can be tested using the same routines as those for the dynamic RAM. When this test is selected the above mentioned tests A, B, C and D will be performed on the PMMU memory.

K – Test AMMU Mapping

One entry at a time is set up in the AMMU. This entry points to a valid memory location and all other entries point to invalid memory locations. Then an I/O bus access to the unit itself is made. This access is made through the AMMU to the I/O bus and back into the unit and into the memory. Then it is checked that the access was made to the right memory location. This is repeated using 256 different values in the memory location. All this is repeated for 1024 entries in the AMMU. The Address Mapping Register, AMR is also checked during this test.

L – Test PMMU Mapping

One entry at a time is set up in the PMMU. This entry points to a valid memory location all other entries points to invalid memory locations. Then an I/O bus access to the unit itself is made. This access is made through the AMMU to the I/O bus and back into the unit, through the PMMU and into the memory. Then it is checked that the access was made to the right memory location. This is repeated using 256 different values in the memory location. All this is repeated for all 16384 entries in the PMMU.

I – Test Interrupt

The Interrupt Mask Register, IMR, is tested by writing a counter and checking each value. Then the interrupt circuitry is tested by setting all 2048 external interrupts and enabling the interrupt level and then checking that the circuitry can decode all interrupts.

The timer interrupt is also tested and the time between timer interrupts can be calculated by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. The result should be 40 ms.

H – Test Instruction/Data cache

On the R3000 CPU board there are two caches, one 64 Kb instruction cache and one 64 Kb data cache. This test is divided into 4 parts for both the instruction and the data cache.

1. The basic function of the cache is tested.
2. The 64 Kb of cache memory is tested using a pseudo random test pattern.
3. The tag field is tested. This is done for a logical address space of 512 Mb with increments of 64 Kb. The test will check data and "*hit*" on all addresses, one at a time.
4. The cache *hit* and *no hit* function and the cache block refill function are tested. The test is carried out using a 64 Kb address space in the main memory.

N – Test Write Buffer

This test goes through 153 sub tests. In each test the write buffer is filled and various combinations of load and store operations are performed. This will check that the Write Buffer is working correctly. Furthermore the timeout circuitry is checked.

T – Test FPA

This test goes through 42 different floating point tests, checking that the FPA is working correctly and that the communication between the CPU and FPA is working.

S – Test all

When selecting this command, the following tests will be executed in the order written. A, B, C, D, E, F, G, J, K, L, I, H, N and T. It is possible to add the *Repeat test* option *(O)* to this one.

O – Repeat test(s)

All of the above mentioned tests will run once, when selected. If, when selecting test(s), this one *(O)* is also selected, the test(s) will repeat itself (themselves) until otherwise canceled.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

P – Set test parameters

This entry is used to set start address and end address for the memory tests and to set the state of the caches during the tests. The start and end address has to be on hexadecimal form. If nothing is entered, the program will use the default values shown on the terminal. Entering illegal addresses will not be allowed.

After reset the two caches have the following status:

- R3000 instruction cache 'Disabled'
- R3000 data cache 'Disabled'
- Swap caches 'No'

These values will be in effect on all tests except *H* (Test Instruction/Data cache). It is possible to enable or disable the two caches individually and also to swap the two caches by selecting *P*. The cache status is shown whenever the menu is displayed.

Z – Boot

Execute master reset to the system.

Q – Debugger

Go to debugging program. Return to Diagnostic Program by entering **go <CR>**.

M – Menu

Display the menu on the terminal. The first line contains information about the actual memory size and the state of the caches.

V – Version

Display version of Diagnostic Program, version of the boot prom and elapsed time from last reset.

Status register

If a bus error occurs, the status register contains information about the reason of the bus error.

Status bit	Description
STR(0)	Double fault in memory
STR(1)	No memory
STR(2)	Time out
STR(3)	Bus error from the I/O bus
STR(7-4)	Not used
STR(8)	Time out during internal write cycle
STR(9)	Time out. Write to I/O bus. 1st Write Buffer.
STR(10)	Time out. Write to I/O bus. 2nd Write Buffer.
STR(11)	Bus error. Write to I/O bus. 1st Write Buffer.
STR(12)	Bus error. Write to I/O bus. 2nd Write Buffer.
STR(15-13)	Not used

Table 3-10-2: Status register on CPU R3000

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SUPERMAX MODULES

MIOC

The purpose of this program is to evaluate the basic functions of the MIOC 4600 module, which is the Multiple Input Output Controller in the Supermax card family. The following functions can be tested with this program:

- The dynamic main memory.
- Parity circuitry.
- Registers.
- All interrupts.
- I/O bus.
- Both submodules.

Initialization

Included in the boot prom of the MIOC is a thorough self test, which includes the following items:

- MC68030 internal confidence test.
- Determining actual memory size.
- Testing and initializing memory.
- Determining submodule configuration.

Running the Diagnostic Program

When the initialization is successfully completed, and the MIOC is booted, the MIOC is ready to proceed with the more sophisticated parts of the test. After typing the select sequence for the MIOC, that is going to be tested it should respond with a message on the terminal.

```
mioc  u   > _   (u is the unit number)
```

When this prompt is displayed on the terminal, the MIOC is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the MIOC.

The example shows the menu from a MIOC with unit number 5:

```
mioc  5   > M
02 Mb memory. 68030 prg.cache = 'Enable'. 68030 data cache = 'Disable'
No. Submodule type.   Revision.         Network address.      Test state.
0   Ethernet (CA)     000               0x080075800001        'Enable'
1   Not installed

A - Test main memory
B - Test parity circuit
C - Test registers
D - Test interrupt
E - Controller test on submodule(s). Diagnose
F - Controller test on submodule(s). Internal loopback
S - Test All
G - Controller test on submodule(s). External loopback
O - Repeat test(s)
H - Controller test on submodule(s). Monitor mode
X - Bustest. Passive unit
Y - Bustest. Active unit
P - Set test parameters
Q - Debugger
V - Version
M - Menu
mioc  5   >
```

Figure 3-11-1: Menu for MIOC

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test main memory

The main memory consists of minimum 2 Mb dynamic ram. This memory will be tested using the different tests mentioned below. It is possible to select one or more tests to be performed if selecting *P*.

- **High Speed.** This routine performs a fast test of the dynamic memory. It writes the value of the current address in the memory. Then the memory content is read and compared to the value written and errors are indicated. All of this is repeated using the inverted value of the current address.
- **Bit Test.** During this test every single bit in the main memory will be written with both *true* and *inverted* values. This is done using long word operations with the following values. During pass one the value written is 0x00000001, during pass 2 it is 0xFFFFFFFE, during pass 3 it is 0x00000002, during pass 4 it is 0xFFFFFFFD etc. All in all 64 passes. A plus (+) is written on the terminal for each pass.
- **Address Bit Test.** During this test every single address bit is tested. This is done by writing one value in the current address if the selected address bit is zero and another value if the address bit is one. After that the memory is checked for correct content. The test is performed for address bits in the range 2-20 and the test runs two times, each time with two new write values.

Address bit	Pass 1	Pass 2
0	0x00000000	0xFFFFFFFF
1	0xFFFFFFFF	0x00000000

- **Galloping Ones And Zeroes.** This test is also performed 2 times. First of all the memory space is initialized with a default value. Then a galloping value is written in a certain address. Then all addresses which are neighbours to that first address are tested. They must still contain the default value. A neighbour is an address, which only differs in one bit from the original address. When all neighbours are tested the default value is

written back in the original address. This is repeated for all addresses.

Value	Pass 1	Pass 2
Default	0x00000000	0xFFFFFFFF
Galloping	0xFFFFFFFF	0x00000000

- **Byte Write.** The MC68030 is able to do a long word operation even though the address being referenced is not on a long word boundary. This is called **Dynamic Bus Sizing**. In other words, if the MC68030 writes to an address on a long word boundary, the long word will be written in one operation. But if the address is not on a long word boundary, the operation will be split into two operations as shown below.

Boundary	1. operation	2. operation
0	1 long word	
1	3 bytes	1 byte
2	1 word	1 word
3	1 byte	3 bytes

This test will write the long word 0xFFAA5500 using long word operations, but using the four different boundaries. By doing that both byte, word and long word operations will be performed.

- **Read-Modify-Write.** The MC68030 microprocessor has a feature which makes it possible in one operation to read a byte in memory, test the byte, set one bit in the byte and to write it back again. This is called *Read-Modify-Write* and this test will initialize memory with a default value and then perform the *Test And Set (TAS)* instruction on all memory locations and then check for correct memory content.

B – Test parity circuit

The parity circuit is tested by deliberately introducing a parity fault in the main memory and checking that a fault interrupt is generated.

C – Test registers

The on-board registers on the MIOC, used for access to the I/O bus are tested.

- The Short Bus Access Register, SBAR is tested by writing a counter and checking each value.
- The Long Bus Access Register, LBAR is tested by writing a counter and checking each value.

D – Test interrupt

This test is divided into 4 parts.

- The Interrupt Mask Register, IMR is tested by writing a counter and checking each value.
- The external interrupt circuit is tested. The test is done by making an I/O bus access to the unit itself and then checking that the external interrupt is active in the Interrupt Pending Register. All this is repeated for 2048 entries in main memory.
- The timer interrupt is tested and the time between timer interrupts can be calculated by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. The result should be 10 ms.
- The profile interrupt is tested by enabling the corresponding level and then checking that the circuitry can decode the interrupt. The profile interrupt is running at a clock frequency of 56.25 Hz.

E – Controller test on submodule(s). Diagnose

Refer to the description of the specific submodule.

F – Controller test on submodule(s). Internal loopback

Refer to the description of the specific submodule.

S – Test all

This test will run one time through test A, B, C, D, E and F. It is possible to add the *Repeat test* option *(O)* to this one.

G – Controller test on submodule(s). External loopback

Refer to the description of the specific submodule.

O – Repeat test(s)

All of the above mentioned tests will run one time through when selected. If, when selecting test(s), this one *(O)* is also selected, the test(s) will repeat itself (themselves) until otherwise canceled.

H – Controller test on submodule(s). Monitor mode

Refer to the description of the specific submodule.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

P – Set test parameters

This entry is used to set up various parameters for the different tests. The following list shows what can be changed.

- Set MC68030 program cache enable/disable.
- Set MC68030 data cache enable/disable.
- Start address and end address for the main memory tests.
- Which main memory tests will be performed.
- Set test state and parameter on submodule number 0.
- Set test state and parameter on submodule number 1.

Q – Debugger

Go to debugging program. Return to Diagnostic Program by entering **GO <CR>**.

V – Version

Display version of Diagnostic Program, version of the boot prom and elapsed time from last reset.

M – Menu

Display the menu on the terminal. The first lines contain information about the actual memory size, the state of the caches and the configuration of the two submodules.

Status register

If a bus error occurs, the status register contains information about the reason of the bus error.

Status bit	Description
STATUS(0)	Time out during a CPU cycle.
STATUS(1)	Time out during access in main memory.
STATUS(2)	Time out during access in submodule.
STATUS(3)	CPU connected to the memory when error occurred.
STATUS(4)	Submodule connected to the memory when error occurred.
STATUS(5)	Main memory segment 0 or 1.
STATUS(6)	Parity error in main memory.
STATUS(7)	Not used

Table 3-11-1: Status register on MIOC

Submodule

The MIOC contains two general purpose interfaces for connection of one or two I/O submodules. A submodule usually consists of an intelligent I/O controller and a physical interface. The two submodules can be of different types and the tests will run concurrently on both submodules.
Then you display the menu, you can see the configuration of the two submodules. The following information concerning the submodules is displayed.

- The submodule type.
- Revision of the submodule.
- Address on the network, if it is a network submodule.
- The test state of the submodules. In **disable** state, no test will be performed, when running submodule tests. In **enable** state, tests will be performed, when running submodule tests. The test state can be disabled or enabled, by selecting *P*.

In order to test the submodule(s), four general tests are used.

- **Diagnose**
  This test will usually perform simple diagnostics of the submodule.
- **Internal loopback**
  This test will usually perform a data transport to/from the controller, without using the interface (special plugs or links).
- **External loopback**
  This test will usually perform a data transport to/from the controller, using the interface (special plugs or links).
- **Monitor mode**
  This test will usually monitor the interface cable(s) on the submodule and can report the status of the interface. When running this test, the interface cable(s) must be connected to the submodule. In monitor mode the test runs continuously.

Statistics

As explained in the chapter concerning each submodule, some statistic information is available from the submodules. Since the test is able to run concurrently on both submodules on the MIOC there is a way to select from which of the submodules the information should come. This is implemented as a switch. When a **0** is typed on the keyboard all subsequent statistical information is from submodule 0. When a **1** is typed on the keyboard all subsequent statistical information is from submodule 1. Upon start of a test the switch will be set to the submodule which has the highest module number.

Ethernet Submodule

The Ethernet submodule, which is a Local Area Network (*LAN*) interface is based on Intel 82596DX or Intel 82596CA and Intel 82C501. The 82596 is the Ethernet controller and the 82C501 is the manchester encoder/decoder. Communication between the 68030 and the 82596 is made through the main memory. The following tests can be used to test the Ethernet submodule. Refer to "Chapter 5 – 1 Ethernet test", to see the detailed description of the ethernet test.

- **Controller test on submodule(s). Diagnose test.**
  This test is used to check the Ethernet controller. The Ethernet controller will run a diagnose test. The test will use Ethernet diagnose test. The test will run 8192 times.
- **Controller test on submodule(s). Internal loopback.**
  This test is used to check the Ethernet controller. The Ethernet controller will run in internal loop back and will transmit and receive packages to/from the memory. The following Ethernet tests are used.[1)]
  - Controller test
  - Controller data transmission. The test will run 2048 times.
  - Internal data transmission. The test will run 2048 times.
- **Controller test on submodule(s). External loopback.**
  This test is used to check the Ethernet controller. The Ethernet controller will run in external loop back (in the transceiver) and will transmit and receive packages to/from the memory.

The following Ethernet tests are used.[1)]

- Controller test
- Controller data transmission. The test will run 2048 times.
- External data transmission. The test will run 2048 times.

- **Controller test on submodule(s). Monitor mode.**
  This test is used to check the local area network. The Ethernet controller will receive all packages on the network cable. The following Ethernet tests are used.[1)]
  - Controller test
  - Monitor mode. The test run continuously.

[1)] Even if you have two different submodules on the MIOC, the tests on both submodules will run concurrently.

HDLC Submodule

The High level Data Link Control (HDLC) submodule has four serial ports, built around two communication controllers, SAB82532. Two of the serial ports supports V.24 interface and two of the serial ports supports V.36/V.11 interface. It is possible to test each port individually by changing the test parameters. The default parameter is all ports. The following tests can be used to test the HDLC submodule. Refer to "Chapter 5 – 2 HDLC test", to see the detailed description of the HDLC test.

- **Controller test on submodule(s). Diagnose test.**

  This test is used to check the HDLC controllers. The program will perform a write/read register test on both HDLC controllers. The test will use HDLC diagnose test.

- **Controller test on submodule(s). Internal loopback.**

  This test is used to check the HDLC controllers. The test will transmit and receive characters in internal loop back and test interrupts. The following HDLC tests are used.[1)]

  - Data transmission with 9600 baud. Internal loopback.
  - Data transmission with 64K baud. Internal loopback.
  - Interrupt test.

  All tests will run 8 times.

- **Controller test on submodule(s). External loopback.**

  This test is used to check the HDLC controllers and the interface drivers. The test will check modem signals and external clock signals and it will transmit and receive characters in external loopback and test interrupts. When running this test, loopback plugs must be mounted in the interface connectors. The following HDLC tests are used.[1)]

- Modem signal test. Interface loop back.[2)]
- Clock signal test. Interface loop back.
- Data transmission with 9600 baud. Interface loop back.
- Data transmission with 64K baud. Interface loop back.
- Interrupt test.

All tests will run 8 times.

- **Controller test on submodule(s). Monitor mode.**
  This test is used to monitor the serial connection. All external clock and modem signals are monitored. The test will use HDLC monitor test, which will run continuously.[1)2)]

1) Even if you have two different submodules on the MIOC, the tests on both submodules will run concurrently.

2) Modem signal **RI** is not used on the V.11 interface, port 2 and 3.

Special plugs needed to test the HDLC submodule

In order to test one HDLC submodule you must use four DB25 plugs, strapped as shown below.

V24 interface, Port 0 – 1	V11 interface, Port 2 – 3
Port 0, pin 17 ←→ Port 1, pin 16	Port 2, pin 18 ←→ Port 3, pin 3
Port 0, pin 16 ←→ Port 1, pin 17	Port 2, pin 15 ←→ Port 3, pin 6
Port 0, pin 15 ←→ Port 1, pin 14	Port 2, pin 6 ←→ Port 3, pin 15
Port 0, pin 14 ←→ Port 1, pin 15	Port 2, pin 3 ←→ Port 3, pin 18
6 ←→ 8 ←→20	22 ←→ 23 ←→ 24
4 ←→ 5 ←→22	10 ←→ 11 ←→ 12
2 ←→ 3	17 ←→ 20
	14 ←→ 16
	5 ←→ 8
	2 ←→ 4

Table 3-11-2: Special plugs to test the HDLC submodule

TERM 8 Submodule

The TERM 8 submodule has 8 serial ports with RS232C interface. TERM 8 is built around 1 Octal Universal Asynchronous Receiver/Transmitter (*OUART* or 8 *UART's*), SCC2698. It is possible to test each port individually by changing the test parameters. The default parameter is all ports. The following tests can be used to test the TERM 8 submodule. Refer to "Chapter 5 – 3 UART test", to see the detailed description of the UART test.

- **Controller test on submodule(s). Diagnose test.**

  This test is used to check the OUART. The program will make a write/read register test on the OUART. The test will use UART diagnose test.

- **Controller test on submodule(s). Internal loopback.**

  This test is used to check the OUART controller. The test will transmit and receive characters in internal loop back and test interrupts. The following UART tests are used.[1)]

  - Data transmission with 9600 baud. Internal loop back.
  - Data transmission with 38400 baud. Internal loop back.
  - Interrupt test.

  All tests will run 32 times.

- **Controller test on submodule(s). External loopback.**

  This test is used to check the OUART controller and the RS-232C interface drivers. The test will check modem signals and it will transmit and receive characters in external loopback and test interrupts. When running this test, loopback plugs must be mounted in the interface connectors.

The following UART tests are used.[1)]

- Modem signal test. Interface loop back.
- Data transmission with 9600 baud. Interface loop back.
- Data transmission with 38400 baud. Interface loop back.
- Interrupt test.

All tests will run 32 times.

- **Controller test on submodule(s). Monitor mode.**
  This test is used to check the serial connection. All ports will receive characters from the serial line (terminals) and if the character is received without errors, the character will be written back to the serial line. The test will use UART monitor test, which will run continuously.[1)]

1) Even if you have two different submodules on the MIOC, the tests on both submodules will run concurrently.

Special plugs needed to test the TERM 8 submodule

In order to test one TERM 8 submodule you must use eight DB25 connectors strapped as shown below.

RS-232C plug
2 ←→ 3
4 ←→ 5
6 ←→ 8 ←→ 20

Table 3-11-3: Special plugs to test the TERM 8 submodule

TERM 32 Submodule

The TERM 32 submodule has 32 serial ports. The TERM 32 submodule is built around 4 Octal Universal Asynchronous Receiver/Transmitter (4 *OUART* or 32 *UART's*), SCC2698 and a fiber optical link. The fiber optical link is the interface to the TERM 32 remote box, which contains the 32 serial ports with RS232C interface. It is possible to test 8 ports individually by changing the test parameters. The default parameter is all ports. The following tests can be used to test the TERM 32 submodule. Refer to "Chapter 5 – 3 UART test", to see the detailed description of the UART test.

- **Controller test on submodule(s). Diagnose test.**

  This test is used to check the OUART. The program will make a write/read register test on the OUART. The test will use UART diagnose test.

- **Controller test on submodule(s). Internal loopback.**

  This test is used to check the OUART controller. The test will transmit and receive characters in internal loop back and test interrupts. The following UART tests are used.[1)]

  - Data transmission with 9600 baud. Internal loop back.
  - Data transmission with 38400 baud. Internal loop back.
  - Interrupt test.

  All tests will run 32 times.

- **Controller test on submodule(s). External loopback.**

  This test is used to check the OUART controller, the remote box and the RS-232C interface drivers. The test will check modem signals and it will transmit and receive characters in external loopback and test interrupts. If loop back on the RS-232C interface is selected loopback plugs must be mounted in the interface.

The following UART tests are used.[1)]

- Link test will test the link communication between the TERM 32 submodule and the remote box. This is done, by checking link status on the TERM 32 submodule.
- Modem signal test. Interface loop back.
- Data transmission with 9600 baud. Interface loop back.
- Data transmission with 38400 baud. Interface loop back.
- Interrupt test.

All tests will run 8 times.

- **Controller test on submodule(s). Monitor mode.**

  This test is used to check the serial connection. All ports will receive characters from the serial line (terminals) and if the character is received without errors, the character will be written back to the serial line.

  This test will also test the link communication between TERM 32 submodule and remote box. This is done, by checking link status on the TERM 32 submodule. The test will use UART monitor test, which will run continuously.[1)]

1) Even if you have two different submodules on the MIOC, the tests on both submodules will run concurrently.

Special plugs needed to test the TERM 32 submodule

In order to test one TERM 32 submodule you must use 32 DB25 connectors strapped as shown below.

RS-232C plug
2 ←→ 3
4 ←→ 5
6 ←→ 8 ←→ 20

Table 3-11-4: Special plugs to test the TERM 32 submodule

ISDN Submodule

The ISDN submodule enables a Supermax to communicate via the Integrated Services Digital Network (**ISDN**), either using the Basic Rate with line speed of 192 kbits/s (2 B-channels 64kbit, one D-channel 16kbit), or using Primary Rate, line speed of 2 Mbits/s (30 B-channels 64kbit, one D-channel 64kbit). The type of ISDN depends upon the type of back panel mounted on the ISDN submodule.

The ISDN submodule is build up of 512 Kbyte local memory, one Synchronous Protocol Data Formatter, which is a DMA controller, one Basic Rate Data (**BRD**) controller and one Primary Access (**PA**) controller. A line interface controller is mounted on the PA controller. Communication between the MIOC and the DMA controller is made through the local memory. The communication to the BRD controller and the PA controller is performed directly from the MIOC. The following tests can be used to test the ISDN submodule. Refer to "Chapter 5 – 4 ISDN test", to see the detailed description of the ISDN test.

- **Controller test on submodule(s). Diagnose test.**
  This test will test the local memory and DMA, Basic Rate Data and Primary Access controllers on the ISDN module. The following ISDN tests are used.
  - Memory test
  - Basic rate controller test
  - Primary rate controller test
  - Data transmission test

- **Controller test on submodule(s). Internal loopback.**
  This test will transmit and receive data in both Basic and Primary rate ISDN, with loopback on board. The following ISDN tests are used.[1)]
  - Basic rate transmission test. The test will run 4 times.
  - Primary rate transmission test. The test will run 4 times.
  - D-channel transmission test. The test will run 8 times.
- **Controller test on submodule(s). External loopback.**
  Not implemented.
- **Controller test on submodule(s). Monitor mode.**
  Not implemented.

1) Even if you have two different submodules on the MIOC, the tests on both submodules will run concurrently.

SUPERMAX MODULES

CPU R4000

The purpose of this program is to evaluate the basic functions of the CPU R4000 4700 module and the dynamic memory connected to it. The following parts can be tested with this program:

- The dynamic memory connected to the CPU.
- The Active Memory Management Unit (AMMU).
- The Passive Memory Management Unit (PMMU).
- All interrupts.
- The Error Detection and Correction unit.
- The primary/secondary instruction/data cache.
- The Floating Point Unit, FPU.
- The Translation Lookaside Buffer, TLB.
- The Write Buffers.

Initialization

Included in the boot prom of the CPU R4000 is a thorough self test, which includes the following items:

- Initializing and testing memory from 0x0 – 0x200000.
- Testing the Secondary Cache.
- Testing the Write Buffer.
- Testing the Address Mapping Register, AMR.
- Testing the Interrupt Mask Register, IMR.

- Testing the PMMU/AMMU memory, high speed.
- Determining the actual memory size.
- Testing the Floating Point Unit.
- Initializing and testing memory from 0x200000 to top of memory.

Display codes

During the self test the front panel display will change according to the test currently running and the status of the test. The following table shows the possible display codes. F*n* means test *n* failed. P*n* means test *n* passed. When the display shows **PA**, the CPU will enable the *I/O Bus In* and then be ready to be booted. However the self test will continue until completed. If any errors occur the display maintains the error code, and the CPU still attempting to run the program, which has been loaded.
The boot prom supports fast boot, which is supported in the cabinets SM4, SM6, SM12 and SM24. The main memory is not tested, but it is initialized. This happens during the following condition:

- Key switch in **SYSTEM.**
- **SHUTDOWN** push button activated and **START** push button activated.
- **SHUTDOWN** push button **must** be activated until the display shows P0.

If no errors occur the CPU will start the program, which could be either the **Supermax Operating System** or the **Diagnostic Programs**. If it is the Diagnostic Programs, the CPU is ready to be selected, when the display is turned off. If any errors occur, which means the display is not turned off, it is possible to obtain further information about the error, by typing the select sequence.

Passed	Failed	Test
P0		Writing hello message
P1	**F1**	Test memory 0 – 2 Mb
P2	**F2**	Test secondary cache tag bits
P3	**F3**	Test write buffer
P4	**F4**	Test secondary cache data bits
P6	**F6**	Test IMR
P7	**F7**	Test AMR
P8	**F8**	Test AMMU memory
P9	**F9**	Test PMMU memory
PA		Ready to boot
	FA	Single fault in memory
PC	**FC**	Test FPU
Pd	**Fd**	Test main memory > 2 Mb
	FE	Cache exception error
	FF	Exception error
bo		Self test completed
r4		Running debugger

Table 3-12-1: Display codes on CPU R4000

There are some additional display values used in the Diagnostic Programs.

- **bE** in the display indicates a bus error exception.
- **AE** in the display indicates an address error exception.
- **EE** in the display indicates any other exception.
- **Er** in the display indicates any other error.

Running the Diagnostic Program

When the initialization is successfully completed, and the CPU is booted, the CPU is ready to proceed with the more sophisticated parts of the test. After typing the select sequence for the CPU, which will be tested, it should respond with the following message on the terminal:

r4000 u > _ (**u** *is the unit number*)

When this prompt is displayed on the terminal, the CPU is ready to take commands. When typing **M <CR>** the menu will be displayed. The menu shows all the possible tests, that might be performed on the CPU.

The example shows the menu from a CPU with unit number 3 and 32 Mb of memory:

```
r3000 3   > M
032 Mb memory. Instruction cache = 'Disable' Program data cache = 'Disable'
               Data cache = 'Disable'        Cache exception = 'Disable'
A - Test RAM High Speed
B - Test RAM Bit Test
C - Test RAM Address Bit Test
D - Test RAM Galloping Ones And Zeroes
E - Test RAM Byte Write
F - Test RAM Read Modify Write
G - Test AMMU Memory
J - Test PMMU Memory
K - Test AMMU Mapping
L - Test PMMU Mapping
I - Test Interrupt
H - Test Secondary cache
N - Test Write Buffer
T - Test FPU  W - Test ECC
S - Test All
O - Repeat test(s)
X - Bustest. Passive unit
Y - Bustest. Active unit
P - Set test parameters
Z - Boot    Q - Debugger
M - Menu    V - Version
r3000 3   >
```

Figure 3-12-1: Menu for CPU R4000

When the prompt is displayed on the terminal, tests can be selected by typing in the corresponding letter.

A – Test RAM. High Speed

This routine performs a fast test of the dynamic memory connected to the CPU module. The value of the current address is written in the memory. The memory content is then read and compared to the value written and errors are indicated. All of this is repeated using the inverted value of the current address. The Error Detection and Correction circuitry is switched **ON** during this test.

B – Test RAM Bit Test

During this test every single bit in the main memory will be written with both *true* and *inverted* values. This is carried out by using long word operations with the following values.

Pass	Write value
1	0x00000001
2	0xFFFFFFFE
3	0x00000002
4	0xFFFFFFFD
--	----------
63	0x80000000
64	0x7FFFFFFF

All in all 64 passes. A plus (+) is written on the terminal for each pass. The Error Detection and Correction circuitry is switched **OFF** during this test.

C – Test RAM. Address Bit Test

During this test every single address bit is tested. This is done by writing one value in the current address if the selected address bit is zero and another value if the address bit is one. After that the memory is checked for correct content. The test is performed for address bits in the range 2-27 and the test runs four times, each time with two new write values.

Address bit	Pass 1	Pass 2	Pass 3	Pass 4
0	0x00000000	0xFFFFFFFF	0x00000000	0x42070220
1	0xFFFFFFFF	0x00000000	0x42070220	0x00000000

The reason for the value 0x42070220 during pass 3 and 4 is to make sure that the bits concerning the Error Detection and Correction circuitry, which is switched **ON** during this test, also will be tested.

D – Test RAM. Galloping Ones And Zeroes

This test is also performed 4 times. First of all the memory space is initialized with a default value. Then a galloping value is written in a certain address. Then all addresses which are neighbours to that first address are tested. They must still contain the default value. A neighbour is an address, which only differs in one bit from the original address. When all neighbours are tested the default value is written back in the original address.

This is repeated for all addresses. The Error Detection and Correction circuitry is switched **ON** during this test.

Value	Pass 1	Pass 2	Pass 3	Pass 4
Default	0x00000000	0xFFFFFFFF	0x00000000	0x42070220
Galloping	0xFFFFFFFF	0x00000000	0x42070220	0x00000000

E – Test RAM. Byte Write

Because of the error correcting code it is much more difficult to write a byte (*8 bits*) or a word (*16 bits*) in memory, than it is to write a long word (*32 bits*). 32 bits are used to contain data and 7 bits contain the ECC code belonging to that data. If one byte or one word is to be written the CPU module will have to read a whole long word into a register, then write the new byte or word into the register and then write the long word back in memory.

This test is carried out by using byte operations. One byte in each long word in the whole memory is written using the value 0xFF. Then all four bytes in each long word is checked. The memory is cleared before each pass, using long word operations. The data cache is disabled during this test.

Pass	Byte number
1	Byte 0
2	Byte 1
3	Byte 2
4	Byte 3

F – Test RAM. Read Modify Write

The CPU R4000 module has a feature which makes it possible to lock the memory. This enables the programmer to simulate a *Read-Modify-Write* cycle by doing the following:

- Lock the memory.
- Read data in memory.
- Check and modify the data.
- Write the data back.

The write operation will automatically unlock the memory again.
This test will initialize memory with a default value and then simulate the *Test And Set (TAS)* instruction on all memory locations and then check for correct memory content. The data cache is disabled during this test.

NOTE

If the instruction cache is disabled it is not possible to simulate the *Read-Modify-Write* cycle correctly. In that case the test is carried out, without locking the memory.

G – Test AMMU Memory

The AMMU memory consists of 2 Kb static RAM. The memory is organized as 2 K × 8 bit, but each byte occupies 4 bytes in the address space. This memory can be tested using the same routines as those for the dynamic RAM. When you select this test the above mentioned tests A, B, C and D will be performed on the AMMU memory.

J – Test PMMU Memory

The PMMU memory consists of 32 Kb static RAM. The memory is organized as 16 K × 16 bit, but each word occupies 4 bytes in the address space. This memory can be tested using the same routines as those for the dynamic RAM. When this test is selected the above mentioned tests A, B, C and D will be performed on the PMMU memory.

K – Test AMMU Mapping

One entry at a time is set up in the AMMU. This entry points to a valid memory location and all other entries point to invalid memory locations. Then an I/O bus access to the unit itself is made. This access is made through the AMMU to the I/O bus and back into the unit and into the memory. Then it is checked that the access was made to the right memory location. This is repeated using 256 different values in the memory location. All this is repeated for 1024 entries in the AMMU. The Address Mapping Register, AMR is also checked during this test.

L – Test PMMU Mapping

One entry at a time is set up in the PMMU. This entry points to a valid memory location all other entries points to invalid memory locations. Then an I/O bus access to the unit itself is made. This access is made through the AMMU to the I/O bus and back into the unit, through the PMMU and into the memory. Then it is checked that the access was made to the right memory location. This is repeated using 256 different values in the memory location. All this is repeated for all 16384 entries in the PMMU.

I – Test Interrupt

The Interrupt Mask Register, IMR, is tested by writing a counter and checking each value. Then the interrupt circuitry is tested by setting all 2048 external interrupts and enabling the interrupt level and then checking that the circuitry can decode all interrupts.

The timer interrupt is also tested and the time between timer interrupts can be calculated by measuring the time between two writings of **Timer interrupt** on the terminal and then divide that time by 100. The result should be 40 ms.

H - Test Secondary cache

On the R4000 CPU board there is three caches, two on-chip caches (8 Kb primary program and 8 Kb primary data cache) and one external cache (1 Mbyte secondary cache). This test is divided into 3 parts for the secondary cache only.

1. The secondary cache tag field memory is tested. The test will write all tag fields in the cache with different data. After that all tag fields will be checked. All this will be done, by using a special R4000 CACHE instruction.
2. The secondary cache data memory is tested. The test will write all data in the cache with different data. After that all data will be checked.

3. The primary data cache and the secondary cache are tested for correct function. That is done, by using 9 different types of cache access modes. on each 32 bit data in the secondary cache. The test is carried out using two 1 Mbyte address spaces in the main memory, test and flush space.

N – Test Write Buffer

This test goes through 153 sub tests. In each test the write buffer is filled and various combinations of load and store operations are performed. This will check that the Write Buffer is working correctly. Furthermore the timeout circuitry is checked.

T – Test FPU

This test goes through 42 different floating point tests, checking that the built-in FPU of the R4000 is working correctly. Furthermore the 64 bit memory interface is checked. This is done by using FPU double word load and store operations.

W – Test ECC

The test will check the ECC circuit for correct function. This is done by generating a single bit fault in the main memory and checking that the fault is detected and that data is corrected. The test also checks that correct status about the error is saved. The test is performed on all data bits using different memory addresses. The test is performed 2 times. The first pass uses a background data pattern of `0x00000000`, the second pass uses `0xFFFFFFFF`. The test is repeated for each 1 Mbyte memory block and finial the whole test is repeated 16 times.

S – Test all

When selecting this command, the following tests will be executed in the order written. A, B, C, D, E, F, G, J, K, L, I, H, N, T and W. It is possible to add the *Repeat test* option *(O)* to this one.

O – Repeat test(s)

All of the above mentioned tests will run once, when selected. If, when selecting test(s), this one *(O)* is also selected, the test(s) will repeat itself (themselves) until otherwise cancelled.

X – Bustest. Passive unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

Y – Bustest. Active unit

Refer to "Chapter 4–1 Bus test", to see the detailed description of the bus test.

P – Set test parameters

This entry is used to set start address and end address for the memory tests and to set the state of the caches during the tests. The start and end address has to be on hexadecimal form. If nothing is entered, the program will use the default values shown on the terminal. Entering illegal addresses will not be allowed.

It is possible to enable or disable the caches individually and also to disable or enable the cache exception. The cache exception occurs when an ECC error is detected in the cache memory. These values will be in effect on all tests except E, F and H (Byte write test, Read-Modify-Write test and Test Secondary cache). In test *E* and *F*, the data cache is always disabled.

After reset the caches have the following status:

- Cache on instructions 'Disabled'.
- Cache on program data 'Disabled'.
- Cache on data 'Disabled'.
- Cache exception 'Disabled'

The actual memory size and cache status is shown whenever the menu is displayed or when selecting this setup.

Z – Boot

Execute master reset to the system.

Q – Debugger

Go to debugging program. Return to Diagnostic Program by entering **go <CR>**.

M – Menu

Display the menu on the terminal. The first line contains information about the actual memory size and the state of the caches.

V – Version

Display version of Diagnostic Program, version of the boot prom and elapsed time from last reset.

Status register

If a bus error occurs, the status register contains information about the reason of the bus error.

Status bit	Description
STR(0)	Double fault in memory
STR(1)	No memory
STR(2)	Time out
STR(3)	Bus error from the I/O bus
STR(7-4)	Not used
STR(8)	Time out during internal write cycle
STR(9)	Time out. Write to I/O bus. 1st Write Buffer.
STR(10)	Time out. Write to I/O bus. 2nd Write Buffer.
STR(11)	Bus error. Write to I/O bus. 1st Write Buffer.
STR(12)	Bus error. Write to I/O bus. 2nd Write Buffer.
STR(15-13)	Not used

Table 3-12-2: Status register on CPU R4000

4 BUS TEST

Bus test

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BUS TEST

Introduction

This is a common part of all Diagnostic Programs and is used to test the communication between units connected to the common I/O bus on the mother board in a Supermax system. A unit which is running a bus test will access another unit and perform a memory test in the memory of the other unit. You should have in mind that a unit is not allowed to perform any other test when it is participating in a bus test.

Passive bus test

The first time you select this test the unit will initialize itself to take part in a bus test as a passive unit. This means that it will allow other units to test its memory and it will take care of the arbitration between units who want to test its memory. When selecting this test again the unit will remove itself from the passive state, and it cannot be accessed from the I/O bus any more. Whenever a unit is passive the letter **X** appears in the prompt:

```
cpu20 3 X > _
```

NOTE When running active bus test from a module that supports Write Bus access, all other modules must be in passive bus test mode. Otherwise, it is possible to cause a time-out (Bus Error) on the active module.

Active bus test

This test will make the unit the active part in a bus test. When selecting this test the program will ask for the unit numbers of the units, that are going to be tested, and then the unit will perform a memory test on those units.

Before making a unit active be sure that all units that are going to be tested are placed in the passive state. A unit can be both passive and active at the same time, which makes it possible for you to let all units in a system test all the other units. Most units are not able to test themselves but some are. This will be told in the paragraph concerning the different units. Whenever a unit is active the letter **Y** appears in the prompt:

```
cpu20 3   Y> _
```

Instead of typing in all unit numbers, it is possible to type the character *. In that case the unit will use the unit numbers of all units recognized, when the Diagnostic Programs were loaded. That information can be read in a configuration table located in the master unit, which is the DIOC that loaded the system, and all units in the system will be tested. An example is shown:

```
cpu20 0 X > Y
cpu20 0 X >
Unit numbers to be tested: *
cpu20 0 XY>
Unit numbers to be tested: 3 5 8 E
cpu20 0 XY>
Now testing unit number: 3 5 8 E
```

Figure 4-1-1: Active and passive bus test

Concept of testing

In order to perform a complete test of the I/O bus it is necessary to test every address line in the 34 bit address bus and every data line in the 32 bit data bus. In order to reduce the amount of memory necessary to do that the relocating capabilities of the modules are used. On all modules up to and including the CPU 68020, the 34 bit I/O bus address is interpreted in the following manner:

Unit	ASN	SEG	Address
UUUU	NNNNNN	SSSS	AAAA AAAA AAAA AAAA AAAA

Table 4-1-1: 34 Bit I/O bus address, old type

On all modules starting with the DIOC3, CPU 68030, CPU R3000 and the MIOC, the 34 bit I/O bus address is interpreted in the following manner:

Unit	Address
UUUU	**AA AAAA AAAA AAAA AAAA AAAA AAAA AAAA**

Table 4-1-2: 34 Bit I/O bus address, new type

By testing one unit you can verify that it is possible to drive the bits concerning the unit number for that unit. This leaves us with 30 address bits. It would take 1 Gb of memory in order to test that completely. But *(un)fortunately* there is not that much memory available, so there must be another way to do it.

Each unit will not use all of the 30 address bits, when they are accessed from the I/O bus. Some will only use the 16 least significant bits, like the SIOC1, and some will use all 30 bits, like the CPU 68020. The least significant bits are tested using a linear block of memory, approximately of the size given by the number of address bits. Whenever a unit uses more than 20 bits of the address, it has some kind of a mapping facility in order to translate the I/O bus address into local memory addresses.

When testing the most significant bits, this is done by isolating one bit at a time, testing a linear block of memory with that bit set to both 0 and 1 and then continue by isolating the next bit. By doing that, the amount of memory needed to test a unit is reduced to a size equaling the size of the linear block used to test each bit, because the relocating facilities of the units will use the same physical memory block during each test.

Request/Acknowledge table

When one unit is testing another unit we must be sure that no other units are testing the same unit at the same time. This is done in a way, that the passive unit manages its own memory, and grants permission to an active unit, when the memory is free to be tested by that unit. The passive unit makes sure that only one active unit at a time gets an acknowledge. An active unit requests a passive unit for permission to test it. This is done by writing in the Request byte and then interrupting the passive unit by writing in the interrupt address.

When the request is asked, the active unit will wait until permission is granted, and then the test will be performed. All this is done using a 32 bytes table in each passive unit.

Address	Byte	Byte	Description
0x00	REQ0	ACK0	Request and acknowledge for unit 0
0x02	REQ1	ACK1	Request and acknowledge for unit 1
0x04	REQ2	ACK2	Request and acknowledge for unit 2
0x06	REQ3	ACK3	Request and acknowledge for unit 3
0x08	REQ4	ACK4	Request and acknowledge for unit 4
0x0A	REQ5	ACK5	Request and acknowledge for unit 5
0x0C	REQ6	ACK6	Request and acknowledge for unit 6
0x0E	REQ7	ACK7	Request and acknowledge for unit 7
0x10	REQ8	ACK8	Request and acknowledge for unit 8
0x12	REQ9	ACK9	Request and acknowledge for unit 9
0x14	REQA	ACKA	Request and acknowledge for unit 10
0x16	REQB	ACKB	Request and acknowledge for unit 11
0x18	REQC	ACKC	Request and acknowledge for unit 12
0x1A	REQD	ACKD	Request and acknowledge for unit 13
0x1C	REQE	ACKE	Request and acknowledge for unit 14
0x1E	REQF	ACKF	Request and acknowledge for unit 15

Table 4-1-3: Request and acknowledge table

REQ(0-F) must contain 0x00 when not active.

REQ(0-F) must contain 0x50 + (unit number) when active.

ACK(0-F) must contain 0x00 when not active.

ACK(0-F) must contain 0xA0 + (unit number) when active.

Error messages will be displayed if the values are not correct.

Bus test table

The bus test concept is built in a way, that each unit has a test table containing all necessary information to the active units about how it should be tested. All units have this test table on I/O bus address 0x01003c00, which is the only fixed address, specified to the units. Prior to testing a unit the active unit will read this table and initialize the bus test to run with the parameters from the test table. The table contains the following information:

Name	Content	Size	Description
Table	Valid	long	Table valid = 'BUST'
	Count	word	Number of bytes to read
			Including valid and check
	Config	word	0x0001 = Byte
			0x0002 = Word
			0x0004 = Long
			0x0008 = RMW (Read-Modify-Write)
			0x0010 = WB (Write Bus)
			0x0100 = BURST (BTU burst mode)
	Req/Ack	long	Request/acknowledge start address
	BINTADR	long	Bus interrupt address
	WBtab1	word	Offset to Write Bus table (Write)
	WBtab2	word	Offset to Write Bus table (Read)
	NUMTAB	word	Number of tables below
	Tab1	word	Offset to table 1 (Test 1, Write)
	Tab2	word	Offset to table 2 (Test 1, Read)
	Tab3	word	Offset to table 3 (Test 2, Write)
	...	...	...
	TabN	word	Offset to table N (Test N, Read)

Table 4-1-4: Bus test table (1 of 3)

The size and content of the next part of the table depends very much on which unit it concerns.

The second part of the table contains the following:

Name	Content	Size	Description
Table 1	Size1	long	Block size of addresses in table 1
	Count1	word	Number of addresses in table 1
	Addr11	long	Table 1 Address 1
	Addr12	long	Table 1 Address 2
	Addr13	long	Table 1 Address 3
	Addr14	long	Table 1 Address 4
	. . .	. . .	. . .
	Addr1N	long	Table 1 Address N
Table 2	Size2	long	Block size of addresses in table 2
	Count2	word	Number of addresses in table 2
	Addr21	long	Table 2 Address 1
	Addr22	long	Table 2 Address 2
	Addr23	long	Table 2 Address 3
	Addr24	long	Table 2 Address 4
	. . .	. . .	. . .
	Addr2N	long	Table 2 Address N
Table 3	Size3	long	Block size of addresses in table 3
	Count3	word	Number of addresses in table 3
	Addr31	long	Table 3 Address 1
	Addr32	long	Table 3 Address 2
	Addr33	long	Table 3 Address 3
	Addr34	long	Table 3 Address 4
	. . .	. . .	. . .
	Addr3N	long	Table 3 Address N
. . .	. . .	. . .	. . .
Table N	SizeN	long	Block size of addresses in table N
	CountN	word	Number of addresses in table N

Table 4-1-4: Bus test table (2 of 3)

Name	Content	Size	Description
	AddrN1	long	Table N Address 1
	AddrN2	long	Table N Address 2
	AddrN3	long	Table N Address 3
	AddrN4	long	Table N Address 4
	...	...	...
	AddrNN	long	Table N Address N
	Check	word	Checksum of table.

Table 4-1-4: Bus test table (3 of 3)

To understand the function of the test table the following is an example concerning the SIOC1.

Name	Content	Value	Description
Table	Valid	0x42555354	Table valid = 'BUST'
	Count	0x0026	Number of bytes to read
	Config	0x000B	0x0001 = Byte 0x0002 = Word 0x0008 = RMW (Read-Modify-Write)
	Req/Ack	0x00003FD0	Request/acknowledge start address
	BINTADR	0x000000A4	Bus interrupt address
	WBtab1	0x0000	Offset to Write Bus table (Write)
	WBtab2	0x0000	Offset to Write Bus table (Read)
	NUMTAB	0x0002	Number of tables below
	Tab1	0x001A	Offset to table 1 (Test 1, Write)
	Tab2	0x001A	Offset to table 2 (Test 1, Read)
Table 1	Size1	0x0000b000	Block size of address in table 1
	Count1	0x0001	Number of addresses in table 1
	Addr11	0x00005000	Table 1 Address 1
	Check	0x297B	Checksum of table.

Table 4-1-5: Bus test table for SIOC1

Valid	This text string, 'BUST' indicates to the active unit that the table is initialized and valid.
Count	This number indicates that the total length of the table is 0x26 bytes.
Config	The value 0x000B, which contains 3 bits set to **One**, indicates that the unit will accept the following accesses: – Byte access. – Word access. – Read-Modify-Write access. If the active unit can perform these accesses to the I/O bus, it should test the passive unit using these accesses.
Req/Ack	0x00003FD0 is the I/O bus start address in the SIOC1 of the Request/Acknowledge table. That is the table used to arbitrate between active units, who wants to test the SIOC1.
BINTADR	0x000000A4 is the I/O bus address in the SIOC1, where the active unit must write in order to interrupt the SIOC1.
WBtab1	This entry is not used on the SIOC1, because it does not have the Write Bus facility.
WBtab2	This entry is not used on the SIOC1, because it does not have the Write Bus facility.
NUMTAB	Indicates that the total number of tables to be used, when testing a SIOC1 is 2.
Tab1	Indicates that the offset from **table**, where **Table 1** is found is 0x001a.

Tab2	Indicates that the offset from **table**, where **Table 2** is found is 0x001a. **Note** that Tab1 and Tab2 points to the same table. This means that **table 1** and **Table 2** are the same.
Size1	0x0000b000 is the number of bytes to be tested, when using the address in this table.
Count1	This is the number of addresses in **Table 1**. In this case there is only one address.
Addr11	0x00005000 is the I/O bus start address used when testing the SIOC1.
Check	0x297B is the check sum of the test table in a SIOC1. The value is calculated in such a way that the sum of all words in the table, including the check sum, must be 0.

I/O bus accesses

A unit is able to make certain kind of accesses to the I/O bus and the I/O bus is able to make certain kind of accesses to a unit. The following kinds of accesses are possible on the I/O bus. Note that not all units are able to perform all kinds of accesses. A detailed description of access for all units can be found in "Chapter 4 – 2 I/O bus access table".

Byte

The active unit is able to perform a Byte access on the I/O bus or the passive unit is able to answer to a Byte access from the I/O bus. During the test of Byte accesses a byte counter is written in the passive unit and then checked.

Word

The active unit is able to perform a Word access on the I/O bus or the passive unit is able to answer to a Word access from the I/O bus. During the test of Word accesses a word counter is written in the passive unit and then checked.

Long Word

The active unit is able to perform a Long Word access on the I/O bus or the passive unit is able to answer to a Long Word access from the I/O bus. During the test of Long Word accesses a long word counter is written in the passive unit and then checked.

Read-Modify-Write

The active unit is able to perform a Read-Modify-Write access on the I/O bus or the passive unit is able to answer to a Read-Modify-Write access from the I/O bus. During the test of RMW accesses, bytes are initialized and the *Test and Set* instruction is performed on all bytes, checking for correct function.

Write Bus

The active unit is able to perform a Write Bus access on the I/O bus and the passive unit is able to answer to a Write Bus access from the I/O bus. The Write Bus test is performed using all kinds of accesses, that is understood by the passive unit. A counter is written to the Write Bus and goes into all units, that are able to do Write Bus accesses. An address range, that depends on the unit number of the passive unit, is then checked.

BTU

The active unit is equipped with a BTU (*Block Transport Unit*), and will test other units using the BTU. The BTU is a high speed DMA channel. When using the BTU to transfer data, all 32 bits of the data bus are used, and the passive unit must be able to answer to long word accesses. The BTU test operates as follows:

- The active unit writes a counter in its own memory.
- The BTU transfers this counter to the passive unit.
- The active unit clears its own memory.
- The BTU transfers the counter from the passive unit to the active unit.
- The active unit checks the counter.
- The active unit clears the memory.

While this operation is in progress the active unit will do a programmed read operation in the passive unit.

BTU burst

The active unit is able to perform a BTU burst access to the I/O bus or the passive unit is able to answer to a BTU burst access from the I/O bus. During this test the BTU will transfer data in bursts, which means that more than one data transfer is made in one I/O bus access.

BUS TEST

I/O bus access table

On the following pages a description of passive and active I/O bus accesses type is shown for each of the units, that might be in a system. Refer to "Chapter 4 – 1 Bus test", to see the I/O bus accesses.

CPU 68000

When a CPU 68000 is the active unit in a bus test, it will access the passive unit through Address Space Number 0 Segment 2 in the MMU.

The following accesses can be made to/from the CPU 68000:

Passive accesses	Active accesses
Byte Word Long Word Read-Modify-Write	Byte Word Read-Modify-Write

Table 4-2-1: I/O bus accesses on CPU 68000

SIOC1

When a SIOC1 is the active unit in a bus test, it will use the first entry to the memory mapper. One entry is able to address 1 Kb of memory on the I/O bus.

The following accesses can be made to/from the SIOC1:

Passive accesses	Active accesses
Byte Word Read-Modify-Write	Byte

Table 4-2-2: I/O bus accesses on SIOC1

DIOC1

When a DIOC1 is the active unit in a bus test, it will use the first entry to the memory mapper. One entry is able to address 1 Kb of memory on the I/O bus.

The following accesses can be made to/from the DIOC1:

Passive accesses	Active accesses
Byte Word Read-Modify-Write	Byte BTU

Table 4-2-3: I/O bus accesses on DIOC1

CIOC

When a CIOC is the active unit in a bus test, it will use the first entry to the memory mapper. One entry is able to address 1 Kb of memory on the I/O bus.

The following accesses can be made to/from the CIOC:

Passive accesses	Active accesses
Byte Word Read-Modify-Write	Byte BTU

Table 4-2-4: I/O bus accesses on CIOC

DIOC2

When a DIOC2 is the active unit in a bus test, it will use entry number 12 to the memory mapper. Each entry is able to address 4 Kb of memory on the I/O bus.

The following accesses can be made to/from the DIOC2:

Passive accesses	Active accesses
Byte Word Read-Modify-Write	Byte BTU

Table 4-2-5: I/O bus accesses on DIOC2

NIOC/SIOC2

When a NIOC/SIOC2 is the active unit in a bus test, it will access the passive unit through Address Space Number 0 Segment 2 in the MMU.

The following accesses can be made to/from the NIOC/SIOC2:

Passive accesses	Active accesses
Byte Word Long Word Read-Modify-Write	Byte Word Read-Modify-Write

Table 4-2-6: I/O bus accesses on NIOC/SIOC2

CPU 68020

When a CPU 68020 is the active unit in a bus test, it will access the passive unit using the so called *short bus accesses* and then using the so called *long bus accesses* through Address Space Number 0 Segment 2 in the MMU.

The following accesses can be made to/from the CPU 68020:

Passive accesses	Active accesses
Byte	Byte
Word	Word
Long Word	Long Word
Read-Modify-Write	Read-Modify-Write
BTU burst	

Table 4-2-7: I/O bus accesses on CPU 68020

DIOC3

When a DIOC3 is the active unit in a bus test, it will access the passive unit using direct addresses to the I/O bus.

The following accesses can be made to/from the DIOC3:

Passive accesses	Active accesses
Byte	Byte
Word	Word
Long Word	Long Word
Read-Modify-Write	Read-Modify-Write
BTU burst	Write Bus
	BTU
	BTU burst

Table 4-2-8: I/O bus accesses on DIOC3

CPU 68030

When a CPU 68030 is the active unit in a bus test, it will access the passive unit using different entries in the AMMU. The CPU 68030 is able to test itself using the I/O bus.

The following accesses can be made to/from the CPU 68030:

Passive accesses	Active accesses
Byte	Byte
Word	Word
Long Word	Long Word
Read-Modify-Write	Read-Modify-Write
Write Bus	Write Bus
BTU burst	

Table 4-2-9: I/O bus accesses on CPU 68030

CPU R3000

When a CPU R3000 is the active unit in a bus test, it will access the passive unit using different entries in the AMMU. The CPU R3000 is able to test itself using the I/O bus.

The following accesses can be made to/from the CPU R3000:

Passive accesses	Active accesses
Byte	Byte
Word	Word
Long Word	Long Word
Read-Modify-Write	Read-Modify-Write
Write Bus	Write Bus
BTU burst	

Table 4-2-10: I/O bus accesses on CPU R3000

MIOC

When a MIOC is the active unit in a bus test, it will access the passive unit using the so called *short bus accesses*, which uses the register SBAR and then using the so called *long bus accesses*, which uses the register LBAR.

The following accesses can be made to/from the MIOC:

Passive accesses	Active accesses
Byte	Byte
Word	Word
Long Word	Long Word
Read-Modify-Write	Read-Modify-Write
BTU burst	

Table 4-2-11: I/O bus accesses on MIOC

CPU R4000

When a CPU R4000 is the active unit in a bus test, it will access the passive unit using different entries in the AMMU. The CPU R4000 is able to test itself using the I/O bus.

The following accesses can be made to/from the CPU R4000:

Passive accesses	Active accesses
Byte	Byte
Word	Word
Long Word	Long Word
Read-Modify-Write	Read-Modify-Write
Write Bus	Write Bus
BTU burst	

Table 4-2-12: I/O bus accesses on CPU R4000

Short form I/O bus access table

The following tables gives you an overview of the accesses from and to the different units.

Unit	Byte	Word	Long	RMW	WB	BTU burst
CPU 68000	×	×	×	×		
SIOC1	×	×		×		
DIOC1	×	×		×		
CIOC	×	×		×		
DIOC2	×	×		×		
NIOC/SIOC2	×	×	×	×		
CPU 68020	×	×	×	×		×
DIOC3	×	×	×	×		×
CPU 68030	×	×	×	×	×	×
CPU R3000	×	×	×	×	×	×
MIOC	×	×	×	×		×
CPU R4000	×	×	×	×	×	×

Table 4-2-13: Passive I/O bus accesses

Unit	Byte	Word	Long	RMW	WB	BTU	BTU burst
CPU 68000	×	×		×			
SIOC1	×						
DIOC1	×					×	
CIOC	×					×	
DIOC2	×					×	
NIOC/SIOC2	×	×		×			
CPU 68020	×	×	×	×			
DIOC3	×	×	×	×	×	×	×
CPU 68030	×	×	×	×	×		
CPU R3000	×	×	×	×	×		
MIOC	×	×	×	×			
CPU R4000	×	×	×	×	×		

Table 4-2-14: Active I/O bus accesses

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5 GENERAL DIAGNOSTIC TEST

General diagnostic test

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GENERAL DIAGNOSTIC TEST

Ethernet test

The Ethernet interface, which is a Local Area Network (*LAN*) interface, can be either thick Ethernet or thin Ethernet (Cheapernet). The communication between the CPU and Ethernet controller is done by using the memory to exchange commands, status information and descriptors in order to enable the controller to receive and transmit frames on the network. If an error occurs, no further testing will be done, the error will be reported and the program will return to the menu. The Ethernet test suite is a combination of different tests. The following tests can be executed.

Controller test

The communication between the processor and the Ethernet controller is tested by executing the following commands: NOP, MC-SETUP, IA-SETUP and DIAGNOSE.

Controller data transmission

The Ethernet controller is configured to internal loop back and will transmit a package of 1 kB taken from the transmit buffer, receive the data and put them in the receive buffer. The program will check status from the controller and compare received data with transmitted data.

Internal data transmission

The Ethernet controller is configured to external loop back and the manchester encoder/decoder is configured to loop back. Now the transmitted data will be gated to receive data by the manchester encoder/decoder. When configured like this the controller is only able to handle packages of 18 bytes[1)]. Status and data are checked.

[1)] When the Ethernet controller is an Intel 82596 it is able to handle packages of 64 bytes.

External data transmission

The Ethernet controller is configured to external loop back and the manchester encoder/decoder is configured to no loop back. Now the transmitted data will be gated to receive data by the transceiver. This means that during this test there will be activity on the Network cable. When configured like this the controller is only able to handle packages of 18 bytes[1]. Status and data are checked. During heavy load conditions on the network, there is a possibility of transmission errors or missing a frame.

Monitor mode

Monitor mode is used to check the local area network. The Ethernet controller is configured to receive all frames on the network. It is possible to see statistics of the received frames by selecting the Ethernet statistic information. While displaying the statistics on the terminal, the program will not be able to maintain monitoring the network and frames might be lost. This means that the statistic counters are not correct.

Network test

The Ethernet controller is running a Time Domain Reflectometry (TDR) command. This is a mechanism to detect open or short circuits on the network and to measure their distance from the diagnosing station.[2]

Diagnose test

The Ethernet controller has a diagnose test function. The diagnose test is activated by writing in a certain register in the controller. The result will be written in a different memory location for each pass.[2]

1) When the Ethernet controller is an Intel 82596 it is able to handle packages of 64 bytes.

2) Only used when the Ethernet controller is an Intel 82596.

Statistic information

When the Ethernet transmission test or monitor mode is running, it is possible to display various information about the reception and transmission on the network. The following commands can be used.

Command	Function
R	Display current receive statistics.
S	Display current receive and transmit statistics.
A	Display network address of the current receive buffer.
E	Display network address of bad received frames.
C	Check the Ethernet/transceiver cable on the network. Using network test.[2)]

Table 5-1-1: Commands used for Ethernet statistic information

If there is no immediate response, when you type a letter, it is because the processor is busy executing the tests. Just be patient and the statistics will be displayed.

2) Only used when the Ethernet controller is an Intel 82596.

The following table describes the receive statistic.

Statistic name	Means
Receive OK packet	Number of correctly received frames.
Receive bad packet	Number of bad frame received. Includes short frames, and other errors. Only valid when running monitor mode.
Alignment errors	Number of frames that are both misaligned and contain a CRC error.
CRC errors	Number of aligned frames with CRC error.
Overrun errors	Number of DMA overrun failure to acquire the system bus.
Collisions detected	Number of collisions detected during frame reception.[2)]

Table 5-1-2: Ethernet receive statistic

[2)] Only used when the Ethernet controller is an Intel 82596.

The following table describes the transmission statistic.

Statistic name	Means
Transmit OK packet	Number of frames transmitted without errors.
Heartbeat missing	Number of missing heart beats during frame transmission. Some transceivers do not supply the heart beat signal and this number will equal the number of transmitted frames to the transceiver.
Defer to traffic	Number of transmissions, that had to defer to traffic on the link.
Number of collisions	Number of collisions detected during frame transmission.
Distribution of number of collisions	Distribution of number of collisions per frame, during transmission.

Table 5-1-3: Ethernet transmission statistic

The following table describes the network address.

Statistic name	Means
Source add	Source address on the network
Destination add	Destination address on the network
RFD status	Receive status.
Bit(15)	Completion of frame reception.
Bit(14)	Busy receiving this frame.
Bit(13)	Frame received sucessfully.
Bit(12)	Length error.
Bit(11)	CRC error in an aligned frame.
Bit(10)	Alignment error, CRC error in a misaligned frame.
Bit(9)	Ran out of buffer space, no resources.
Bit(8)	DMA Overrun failure to acquire the system bus.
Bit(7)	Frame too short.
Bit(6)	No EOP flag.
Bit(1)	Multicast address received [2)]
Bit(0)	Receive collision, a collision is detected during reception [2)]

Table 5-1-4: Ethernet network address

[2)] Only used when the Ethernet controller is an Intel 82596.

The following table describes the result of the TDR command. [2)]

Bits	Means
15	No cable problem.
14	Short or open on the Transceiver cable.
13	Open on the Ethernet cable.
12	Short on the Ethernet cable.
0-11	The distance to the cable failure. Distance ~ value × 10 meters.

Table 5-1-5: Ethernet TDR command

[2)] Only used when the Ethernet controller is an Intel 82596.

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GENERAL DIAGNOSTIC TEST

HDLC test

When running the HDLC tests and an error occurs, the error will be reported and the program will continue testing until the last channel is tested. Then the program will return to the menu. The following tests can be executed.

- Diagnose test
- Modem signal test
- Clock signal test
- Interrupt test
- Data transmission test
- Monitor test

Diagnose test

The diagnose test will test the communication between the CPU and HDLC controllers. This is done by writing a byte counter in the timer register of the HDLC controller and checking data after each write. Between the write and read access, a zero will be written to another register of the HDLC controller. The test runs 16 times and each port are tested one by one.

Modem signal test

The test will test all modem signals between the HDLC controllers and the interface. Modem output signals from the HDLC controller are **RTS** and **DTR**. Modem input signals are **CTS**, **DSR**, **CD** and **RI**. In order to test the modem signals the output signals must be connected to the input signals. This is done using the loopback connectors.

The test will activate and deactivate output signals and check the input signals for correct level. The test runs according to the following table:

Test no.	RTS	DTR	CTS	DSR	CD	RI
1	Active	Active	Active	Active	Active	Active
2	Passive	Active	Passive	Active	Active	Passive
3	Passive	Passive	Passive	Passive	Passive	Passive
4	Active	Passive	Active	Passive	Passive	Active
5	Active	Active	Active	Active	Active	Active

Table 5-2-1: HDLC modem signal test no.

If the test fails, the test no. and an error code are displayed. The following table shows the possible error codes.

Error code	Description
Bit(0)	CTS signal failed
Bit(1)	DSR signal failed
Bit(2)	CD signal failed
Bit(3)	RI signal failed

Table 5-2-2: HDLC modem signal error codes

The modem signal test will run on all HDLC ports before signals are changed.

Clock signal test

This test will test all clock signals between the HDLC controller and the interface. The clock signals from the HDLC controller are **TxC** and **RxC**, which can be either input or output, selected by the software.
In order to test the clock signals, the loopback connectors must be mounted. The test runs according to the following table:

Test no.	Port even	Port odd
6	Input	Output
7	Input	Output
8	Output	Input
9	Output	Input

Table 5-2-3: HDLC clock signal test no.

If the test fails, the test no. and an error code are displayed. The following table shows the possible error codes.

Error code	Description
bit(4)	Transmit clock failed
bit(5)	Receive clock failed

Table 5-2-4: HDLC clock signal error codes

The clock signal test will run on all HDLC ports before signals are changed.

Interrupt test

The interrupt test is used to test, that an interrupt from the HDLC controllers can be received by the CPU. The program will first test that there are no interrupts from the HDLC controllers. After that the program will initiate an interrupt from all HDLC controllers and test that the interrupt is made. Finally the program will initiate an interrupt one by one from the HDLC controllers and test that the interrupt is made. The interrupt test is running according to the following table:

Test no.	Interrupts
1	No interrupt
2	Interrupt on all ports
3	Set interrupt on the first port
4	Set interrupt on the second port
-	----------
n	Set interrupt on the last even port

Table 5-2-5: HDLC interrupt test no.

The program tests for real interrupts on the CPU and for interrupts pending in the interrupt status register. All interrupts from the HDLC controllers are made by using the internal timer function on the HDLC controller. The following table shows the possible error codes.

Error code	Error
Bit(0)	Missing interrupt from the HDLC module
Bit(1)	Unexpected interrupt from the HDLC module

Table 5-2-6: HDLC interrupt error codes

Data transmission test

When data is transmitted, the controller is running in HDLC mode. This means that the controller automatically adds CRC bits to the transmitted data. All ports are tested by transmitting characters within the range from 0x00 to 0xff, from one port to the same port and checking that the received character is the same as the one transmitted.
The program will transmit 31 characters plus one control byte on the first port and then transmit 31 different characters plus one control byte on the next port and so on. When all the ports have transmitted the characters, the program will check the characters on the first port and then check the characters on the next port and so on. Before checking received data, the program will check for CRC errors. All this is done 9 times.

Monitor test

Monitor test is used when the Supermax is installed and it only monitors all modem signals.

Status information

When the monitor mode is running, it is possible to display various information about the interface line. The following commands can be used.

Command	Function
S	Display all current HDLC modem signal information.

Table 5-2-7: Command used for HDLC status information

If there is no immediate response, when you type a letter, it is because the processor is busy executing the tests. Just be patient and the status will be displayed.

Status name	Means
PORT	Serial port number
CTS	Current status on Clear To Send (0 = passive, 1 = active)
DSR	Current status on Data Set Ready (0 = passive, 1 = active)
CD	Current status on Carrier Detect (0 = passive, 1 = active)
RI	Current status on Ring Indicator (0 = passive, 1 = active)
CLOCK	Current status on external clock (no = no clock, yes = clock received)

Table 5-2-8: HDLC status information

GENERAL DIAGNOSTIC TEST

UART test

When running the UART tests and an error occurs, the error will be reported and the program will continue testing until the last channel is tested. Then the program will return to the menu. The following tests can be executed.

- Diagnose test
- Modem signal test
- Interrupt test
- Data transmission test
- Monitor test

Diagnose test

The diagnose test will test the communication between the CPU and UART controllers. This is done by writing a byte counter in the mode register of the UART and checking data after each write. Between the write and read access, a zero will be written to another register of the UART. The test runs 16 times and each port are tested one by one.

Modem signal test

The test will test all modem signals between the UART's and the interface. Modem output signals from the UART's are **RTS** and **DTR**. Modem input signals are **CTS**, **DSR** and **CD**. In order to test the modem signals the output signals must be connected to the input signals. This is done using the loopback connectors.

The test will activate and deactivate output signals and check the input signals for correct level. The test runs according to the following table:

Test no.	RTS	DTR	CTS	DSR	CD
1	Active	Active	Active	Active	Active
2	Passive	Active	Passive	Active	Active
3	Passive	Passive	Passive	Passive	Passive
4	Active	Passive	Active	Passive	Passive
5	Active	Active	Active	Active	Active

Table 5-3-1: UART modem signal test no.

If the test fails, the test no. and an error code are displayed. The following table shows the possible error codes.

Error code	Description
Bit(0)	CTS signal failed
Bit(1)	DSR signal failed
Bit(2)	CD signal failed
Bit(3)	DTR read back failed

Table 5-3-2: UART modem signal error codes

The modem signal test will run on all UART ports before signals are changed.

Interrupt test

The interrupt test is used to test, that an interrupt from the UART's can be received by the CPU. The program will first test that there are no interrupts from the UART's. After that the program will initiate an interrupt from all UART's and test that the interrupt is made. Finally the program will initiate an interrupt one by one from the UART's and test that the interrupt is made. The interrupt test is running according to the following table:

Test no.	Interrupts
1	No interrupt
2	Interrupt on all ports
3	Set interrupt on the first port
4	Set interrupt on the second port
-	----------
n	Set interrupt on the last even port

Table 5-3-3: UART interrupt test no.

The program tests for real interrupts on the CPU and for interrupts pending in the interrupt status register. All interrupts from the UART's are made by using the internal timer function on the UART's. The following table shows the possible error codes.

Error code	Description
Bit(0)	Missing interrupt from the UART
Bit(1)	Unexpected interrupt from the UART

Table 5-3-4: UART interrupt error codes

Data transmission test

All ports are tested by transmitting characters within the range from 0x00 to 0xff, from one port to the same port and checking that the received character is the same as the one transmitted.

The program will transmit a character on the first port and then transmit a different character on the next port and so on. When all the ports have transmitted the character, the program will check the character on the first port and then check the character on the next port and so on. All this is done 256 times.

Monitor test

Monitor test is used when the Supermax is installed and all the terminals and printers are connected to the Supermax modules. From the terminals it is possible to test the connection between the terminal and the Supermax module, with transmit and receive characters.

In order to select correct serial set-up (baudrate, data bits, stop bits, parity) on the UART, it is necessary to type the character **f**, on the terminal keyboard, until it is shown on the terminal CRT. When this is done, type the character **s**, until it is shown on the terminal CRT.

Now the UART has the correct serial set-up and all characters (0 - 126) typed on the terminal keyboard will be transmitted to the UART port and the program will transmit the character back to the terminal CRT. While displaying the status information on the terminal, the program will not be able to maintain monitoring the serial port and characters might be lost. This means that the statistic counters are not correct.

The following terminal set-up, can used when running monitor test.

Baudrate	Data bits	Stop bits	Parity
9600	7	1 or 2	even
9600	7	1 or 2	odd
9600	7	1 or 2	none
9600	8	1 or 2	even
9600	8	1 or 2	odd
9600	8	1 or 2	none
19200	7	1 or 2	even
19200	7	1 or 2	odd
19200	7	1 or 2	none
19200	8	1 or 2	even
19200	8	1 or 2	odd
19200	8	1 or 2	none
38400	7	1 or 2	even
38400	7	1 or 2	odd
38400	7	1 or 2	none
38400	8	1 or 2	even
38400	8	1 or 2	odd
38400	8	1 or 2	none

Table 5-3-5: Terminal set-up used for UART monitor test

Status information

When the monitor mode is running, it is possible to display various information about the interface line. The following commands can be used.

Command	Function
C	Set default serial set-up and clear statistics.
S	Display current UART serial set-up, modem status and statistic information.
D	Enable displaying of current serial set-up and modem status when receiving a character from a serial port. To disable this function press any other character.

Table 5-3-6: Commands used for UART status information

If there is no immediate response, when you type a letter, it is because the processor is busy executing the tests. Just be patient and the status will be displayed.

The following table describes the status information.

Status name	Means
PORT	Serial port number
BAUD	Current baudrate (9600,19200,38400)
BITS	Current data bits (7,8)
STOP	Current stop bits (1)
PAR	Current parity status (even,non,odd)
CTS	Current modem status on Clear To Send (0 = passive,1 = active)
DSR	Current modem status on Data Set Ready (0 = passive,1 = active)
CD	Current modem status on Carrier Detect (0 = passive,1 = active)
DATA	Status about the latest received character.
Number of received data	Number of received characters from all serial ports.
Number of overruns	Number of lost characters from all serial ports.

Table 5-3-7: UART status information

The following table describes status on the latest received character.

Received status	Means
Received error	The receiver has received a character with break, frame or parity error.
Illegal data	The receiver has received a character in the range 0x7f-0xff.
No data	The receiver has not yet received any characters.
Wrong data	The receiver has received a character, but not **f** or **s** to select correct set-up.
Data ok	The receiver has received a character without errors and the UART has selected correct set-up. The character is transmitted back to the port.

Table 5-3-8: UART status information about received characters

GENERAL DIAGNOSTIC TEST

ISDN test

The Integrated Services Digital Network (**ISDN**), which is a Wide Area Network (*WAN*) interface, can be either Basic Rate or Primary Rate interface.
The Basic Rate interface has a line speed of 192 kbits/s (2 B-channels 64kbit, one D-channel 16kbit) and the interface is connected to 2 twisted pairs.
The Primary Rate interface has a line speed of 2.048 Mbits/s (30 B-channels 64kbit, one D-channel 64kbit) and the interface is connected to twisted pair G.703.
The ISDN hardware is build up of a local memory, a DMA controller, a Basic Rate Data (**BRD**) controller and a Primary Access (**PA**) controller. A Line interface controller is mounted on the Primary Access controller.
The communication between the CPU and DMA controller is done by using the local memory to exchange commands, status information and descriptors in order to enable the controller to receive and transmit frames on the network. The communication to the Basic Rate Data (BRD) and Primary Access controller (**PA**) is done from the CPU directly.
If an error occurs, no further testing will be done, the error will be reported and the program will return to the menu. The ISDN test suite is a combination of different tests. The following tests can be executed.

Memory test

The local ISDN memory is tested. This is done by writing different data in the memory and then check that the data in the memory is correct. The test will be repeated with inverted data. After the memory test is completed, the memory will be tested for different CPU access types. The data will be a byte counter in the first 256 bytes of the memory.

The test runs according to the following table:

Test no.	Write Offset	Write Access type	Read Access type
0x02-0x00	0	Long word	Byte, Word, Long word
0x06-0x04	1	Long word	Byte, Word, Long word
0x0A-0x08	2	Long word	Byte, Word, Long word
0x0E-0x0C	3	Long word	Byte, Word, Long word
0x12-0x10	0	Word	Byte, Word, Long word
0x16-0x14	1	Word	Byte, Word, Long word
0x1A-0x18	0	Byte	Byte, Word, Long word

Table 5-4-1: Access test on ISDN local memory

Basic rate controller test

This test will test the communication between the CPU and Basic Rate Data controller. This is done by writing a word counter in the FRAR, SRAR and TAR registers of the Basic Rate Data controller. The registers will be checked for correct content after each write. The test continues until the end of the word counter.

Primary rate controller test

This test will test the communication between the CPU and Primary Access controller. This is done by writing a byte counter in PR16 – PR31 registers of the Primary Access controller. The registers will be checked for correct content after each write. The test continues until the end of the byte counter.

Data transmission test

This test will test the DMA controller for correct function. The DMA controller is configured to internal loop back with one super channel. The test will transmit 128 packages of 1 kB taken from the transmit buffer, receive the data and put them in the receive buffer. The program will check status from the DMA controller and compare received data with transmitted data.

Basic rate transmission test

This test will test the communication between the DMA and BRD controller. This is done by configuring the DMA controller to external loop back with two B-channels and the BRD controller is configured to internal loop back. Now the transmitted data will be gated to receive data by the BRD controller.
The test will transmit 16 packages of 1 kB taken from the transmit buffer, receive the data and put them in the receive buffer. The test runs on both channels simultaneously. The program will check status from the DMA controller and compare received data with transmitted data.

Primary rate transmission test

This test will test the PA controller for correct function. This is done by configuring the DMA and PA controller to external loop back with 30 B-channels and the Primary Line Interface is configured to internal loop back. Now the transmitted data will be gated to receive data by the Line Interface controller.
The test will transmit 4 packages of 1 kB taken from the transmit buffer, receive the data and put them in the receive buffer. The test runs on all 30 channels simultaneously. The program will check status from the DMA controller, check status from the PA controller and compare received data with transmitted data.

D-channel transmission test

This test will test the BRD controller for correct function. This is done by configuring the BRD controller to internal loop back on the D-channel.
The test will transmit 32 packages of 8 bytes transmitted to the D-channel, receive the data back from the D-channel, the received data is compared with transmitted data and receive status is checked for correct content.

6 PERIPHERAL TEST FOR DIOC1-2

Peripheral test for DIOC1/DIOC2

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PERIPHERAL TEST FOR DIOC1/DIOC2

Introduction to peripheral test

The Diagnostic Program for peripheral units is also loaded into the DIOC1/DIOC2 when loading the Diagnostic Programs. On the DIOC1 the program will be destroyed, when running the bus test. Otherwise it will always be resident. On the DIOC2 the program will always be resident.

In order to run the program just type **D <CR>** when the DIOC1/DIOC2 is in the menu. When doing that the prompt will change. A letter indicating the subprogram currently running will be in the prompt. The following letters might appear.

Letter	Subprogram
P	Peripheral Units
W	Winchester test
F	Floppy test
S	Streamer test
T	Tape drive test

Table 6-1-1: Prompt letter for subprogram

Typing **M <CR>** will show the menu of the current subprogram.

The example shows what happens on a DIOC2.

```
dioc2 E   > D
dioc2 E P >M
Test of peripheral units
S - Test streamer
W - Test winchester
F - Test floppy
T - Test tape drive
R - Return to main menu
M - Menu
V - Version
dioc2 E P >
```

Figure 6-1-1: Menu for peripheral tests

S – Test streamer

This entry gives you the subprogram used to test streamer drives.

W – Test winchester

This entry gives you the subprogram used to test winchester disk drives.

F – Test floppy

This entry gives you the subprogram used to test floppy disk drives.

T – Test tape drive

This entry gives you the subprogram used to test tape drives.

R – Return to main menu

This entry will return the DIOC1/DIOC2 to the main menu.

M – Menu

This entry will show the menu on the terminal.

V – Version

This entry will show the version of the program.

Cancel a running test

When running peripheral unit test, it is recommended to use **Ctrl E** (soft cancel) to cancel a running test. When **Ctrl E** is present, the program will cancel the test, as soon as the command to the drive has completed, and then return to the menu. **Ctrl E** only affects the following tests:

Commands	Subprogram
B, C, I, M, L	Winchester test.
B, C, D, F, G	Floppy test.
C, I, W	Streamer test.
B, C, F	Tape test.

Table 6-1-2: Soft cancel a running test

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PERIPHERAL TEST FOR DIOC1/DIOC2

Floppy test

The DIOC1 0400 module in the Supermax card family is equipped with the FD1795-02 floppy disk formatter/controller. The DIOC2 1100 module in the Supermax card family is equipped with the FD2795-02 floppy disk formatter/controller. The Diagnostic Program for Floppy Disk Drives is able to handle two types of drives.

- 5¼" drive. 560 kb diskette (double side, double density).
- 8" drive. 1 Mb diskette (double side, double density).

All tests start by issuing a restore command to the drive. If the drive is not ready or the track 00 flag is not set the test stops and the error is reported. If other types of errors occur during a restore command the error is reported to the error buffer and the test is continued.

```
dioc2 E F >M
Diagnostic program for floppy drives

A - Define parameters
B - Write/read test
C - CRC test
D - Seek/read test
E - Display error buffer
F - Format disk
G - Exerciser
H - Display sectors
M - Menu
R - Return to main menu

dioc2 E F >
```

Figure 6-2-1: Menu for floppy test

A – Define parameters

Upon start of the program always select A. The following parameters can be defined to the program.

Drive number	Drive 0, 1, 2 or 3 is selected. Normally drive 1 is used, if only one floppy disk drive is connected to the DIOC.
Number of cylinders	Defaults to 80 cylinders
Number of sectors	Defaults to 16 sectors
Start of write precomp	Defaults to cylinder 43
Step rate	Defaults to step rate 0

NOTE

All drives connected to the Supermax are specified to step rate 0.

Parameters used by the program must be set according to the drive type. These parameters are:

Drive type	**5¼"**	**8"**
Number of cylinders	80	77
Number of sectors	16	26
Step rate	0 (6 ms)	0 (3 ms)

Table 6-2-1: Floppy parameters

B – Write/read test

The following test pattern is written in all sectors of the diskette:

Byte	Pattern
0	Head number (00 head 0, 01 head 1)
1	Cylinder number (0 to maximum cylinder)
2	Sector number (1 to maximum sector)
3 – 255	63 Hex

Table 6-2-2: Floppy write/read pattern

The test writes from cylinder 0 to maximum cylinder, then reads from maximum cylinder to cylinder 0. Head number, cylinder number and sector number in all sectors on each track are verified and the error buffer is updated if any errors occur.

C – CRC test

All cylinders from cylinder 0 to maximum cylinder are read, a restore command is issued and the test starts again. The error buffer is updated if any errors occur.

D – Seek test

This test starts by reading data on cylinder 0, head number 0, then reads data on maximum cylinder, head number 0, then reads on cylinder n, head number 0, then reads on maximum cylinder – n, head number 0, where n has a value in the range from 1 to maximum cylinder. Then the test is repeated for head number 1. All errors reported from the controller are stored in the error buffer.

E – Display error buffer

All errors obtained from write/read test, CRC-test, seek test, exerciser or the formatting command are displayed. The error buffer is cleared if one of these tests are selected. Maximum number of errors in the buffer is 128. If this number is exceeded an overrun is detected, and the buffer is refilled from the start. Informations from the error buffer are:

Name	Description
Command	Command code
Status	Status is displayed in binary code
Cylinder	Cylinder address
Sector	Sector address
Pass	The pass in which the error from the controller occurred

Table 6-2-3: Floppy error buffer

The following table describes the command code.

Code	Command
R	Read
W	Write
F	Format
S	Restore
P	Step
K	Seek

Table 6-2-4: Command codes for floppy error buffer

The following table describes the status code.

Bit	Name	Description
7	Not ready	If set, drive is not ready.
6	Write protect	If set, write protect is activated.
5	Head loaded	If set, head is loaded.
4	Seek error	If set, the desired track was not verified.
3	CRC error	CRC error encountered in the ID field.
2	Track 00	If set, head is positioned in track 00.
1	Index	If set, index mark detected from drive.
0	Busy	If set, command is in progress.

Table 6-2-5: Floppy status code for restore, seek and step commands

Bit	Name	Description
7	Not ready	If set, drive is not ready.
6	Write protect	If set, write protect is activated.
5	Write fault	If set, indicates a write fault.
4	Record not found	If set, the desired track, sector or side were not found.
3	CRC error	If bit 4 is set, an error is found in then ID field, otherwise error in the data field.
2	Lost data	If set, indicates that the DMA did not respond on data request in one byte time.
1	Data request	This bit is a copy of the DRQ output from the FD1795.
0	Busy	If set, command is under execution.

Table 6-2-6: Floppy status code for write, read and format commands

F – Format disk

The floppy disk is formatted. After formatting a track, the entire track is read. All errors reported from the controller are stored in the error buffer.

G – Exerciser

Upon start of the exerciser, the drive will restore and no read operation is performed. When selecting X all sectors are read on the selected track. Errors are stored in the error buffer. The exerciser keeps on reading the selected track until another track is selected or until selecting Y.

Key	Command
Ctrl K	Select head 1
Ctrl J	Select head 0
Ctrl H	Decrement cylinder number
Ctrl L	Increment cylinder number
X	Select read operation
Y	Select no read operation
R	Restore drive

Table 6-2-7: Floppy exerciser commands

In combination with an alignment diskette the exerciser can be used to test track alignment, head alignment etc.

H – Display sectors

Is used in combination with the exerciser. The track selected by the exerciser is displayed sector by sector.

H – Format track

The selected track is formatted. This command is only valid if XEBEC controller is used. Data from the track is read sector by sector and stored in memory. When the track is formatted, the data is rewritten. Only data in failing sectors are lost. Information about these sectors is displayed on the terminal.

I – Seek test

This test starts by reading data on minimum cylinder, head number 0, then reads data on maximum cylinder, head number 0, then reads on minimum cylinder + n, head number 0, then reads on maximum cylinder – n, head number 0 where n has a value in the range from 1 to maximum cylinder. Then the test is repeated for head numbers from 1 to maximum head. All errors reported from the controller are stored in the error buffer.

J – Read skiplist

If the controller is not able to read the skiplist, the error information is displayed.

K – Write skiplist

The format of the skiplist is checked. If the format is illegal the skiplist is not written, and an error is reported.

L – Random write/read

Random write/read test will keep track skiplist, but data is destroyed. All errors obtained from controller are stored in the error buffer. When you select this test you will be asked for a number of sectors ranging from 1 to 32. This is the number of sectors each time written with a continuous counter and then read back and checked for correct content. The sector address is calculated on a pseudo random basis.

Q – Exerciser

Sectors are read one by one on the selected track. Errors are stored in the error buffer. The exerciser keeps on reading the selected track until another track is selected or **Ctrl E** is pressed.

Key	Command
Ctrl K	Increment head number
Ctrl J	Decrement head number
Ctrl H	Decrement cylinder number
Ctrl L	Increment cylinder number
X	Select read operation
Y	Select no read operation
R	Restore drive

Table 6-4-3: Winchester exerciser commands

N – Set command

This feature enables the user to send commands to controllers. Only commands without data transfer from or to the drive may be set. The first byte must contain the number of command bytes transmitted to the controller. Only use Set command to exercise the controller, not the drive.

NOTE

During normal test conditions it is **NOT** necessary to use this feature.

PERIPHERAL TEST FOR DIOC1/DIOC2

Streamer test

The streamer Diagnostic Program is able to test any streamer, that are compatible with the QIC-02 interface descriptions for streaming tape cartridge drives. The program does not use any commands that are classified as optional or vendor unique in the QIC-02 interface proposal. If the user wants to apply any of these commands (eg. a self test command), it can be done by selecting **H** (set command) in the menu. The following shows the menu from the streamer Diagnostic Program.

```
dioc1 E S >M
Diagnostic program for streamers

A - Reset drive and interface
B - Begining of tape
C - Continuous write/read
D - Display status buffer
E - Erase
F - Write file mark
G - Set test pattern
H - Set command
I - Read tape
J - Search to file mark
T - Retension
W - Write tape
M - Menu
R - Return to main menu

dioc1 E S >
```

Figure 6-3-1: Menu for streamer test

A – Reset drive and interface

This command resets the drive and clears the interface registers. Upon start of the program this reset is done automatically. If the drive is not ready a timeout is reported.

B – Begining of tape

Rewinds the tape cartridge to the beginning of the tape.

C – Continuous write/read

The number of blocks selected by the user is written on the tape. The two first bytes in each block contains the block number, the rest of the block contains the byte pattern selected by the user. When the last block is written a file mark is written and the tape is rewinded. Then a read command is issued. When reading the program checks the block number in each block. If any errors occur, the program stops and reports **Data error**.

After each read or write operation the status is read from the drive and this information is stored in the status buffer. The test stops after 64 passes (then 128 status informations are in the buffer and it is filled up). The user can also stop the test by typing **Ctrl E**. **Ctrl E** only interrupts the test if it is typed during read or write operations otherwise **Ctrl C** can be used.

D – Display status buffer

Status information obtained from the drive during a write/read test is displayed. The status buffer is cleared when write/read test is selected.

The error buffer contain the following information:

- **Command**
  Write or read command.
- **Status 1**
  Refer to the description of the status format.
- **Status 0**
  Refer to the description of the status format.
- **Data error counter**
  The data error counter accumulates the number of blocks rewritten for write operations and the number of soft read errors during read operations.

  As data is written on the tape, a read after write check is performed. If a CRC error occurs the data block is rewritten without stopping the tape. If this operation is successful, writing continues and the data error counter is incremented. The drive will make 16 attempts to write the block in error before declaring a hard error.

  During a read operation the drive verifies each block. If an error occurs, the drive will read the next two blocks to see if the block was rewritten without error. If not, the drive stops the tape, backs up and tries to read the block a second time. The drive will make 16 attempts to re-read before declaring a hard error. The number of re-reads is reported to the data error counter.
- **Underrun counter**
  The underrun counter accumulates the number of times that streaming was interrupted because the host failed to maintain the minimum data transfer rate.

E – Erase

The entire tape is erased.

F – Write file mark

A file mark is written on the tape at the current tape position.

G – Set test pattern

The write buffer is set with the bit pattern selected by the user. Upon start of the program the bit pattern defaults to 29 hex.

H – Set Command

This feature enables the user to send commands to the controller. Only commands without data transfer from or to the drive may be set. If a read or write file mark command is issued remember to set on-line.

I – Read tape

Drive reads the tape from the current tape position, until an exception occurs. If **Ctrl E** is typed the drive rewinds the tape before status is displayed.

J – Search to file mark

The drive reads the tape searching for a file mark. When a file mark is found exception is asserted.

T – Retension

This command rewinds the tape to the beginning, then winds to the end and then rewinds to the beginning again.

W – Write tape

The number of blocks selected by the user is written on the tape from the current tape position. Each block contains the byte pattern selected by the user. When the selected number of blocks are written, or when **Ctrl E** is typed, a file mark is written and the tape motion stops.

M – Menu

Display the menu on the terminal.

R – Return to the main menu

Return to menu for the peripheral units.

The status format

After execution of all commands in the menu, except the write/read test, the status from the drive is reported. The status is either:

Exception did not occur

or

Exception occurred

Exception is not an error signal, but is used to inform the host about the condition that caused termination of a command. The termination may be a normal completion or an interrupt due to an encountered fault (hard errors, write protected, etc).

The status bytes from the drive contain the following information:

Bit	Name	Description
0	FIL	This bit is set when a file mark is detected during a read data or a read file mark sequence.
1	BNL	Block in error not located is set when an unrecoverable read data error occurs, and the controller can not confirm, that the last block transmitted was the block in error.
2	UDE	Unrecoverable data bit is set when the controller detects a hard error during a read or a write operation.
3	EOM	End of media bit is set when the logical warning hole of the last track is detected during a write operation.
4	WRP	Write protected bit is set if the cartridge is write protected.
5	USL	Drive unselected bit is set if the selected drive is not connected or is not receiving power.
6	CNI	Cartridge not in place bit is set if a cartridge is not inserted into the drive.
7	ST0	Is set, if any other bit in status byte 0 is set.

Table 6-3-1: Streamer status byte 0

Bit	Name	Description
0	POR	The power on reset bit is set after the host asserts **RESET** or when the controller is powered up.
1	RES	Reserved
2	RES	Reserved
3	BOM	Beginning of media bit is set whenever the cartridge is at the beginning of the tape. This bit does not set **EXCEPTION** .
4	MBD	Marginal block detected is set when 8 or more retries were required during the read of a data block.
5	NDT	No data detected is set when an unrecoverable data error occurs due to a lack of recorded data.
6	ILL	Illegal command.
7	ST1	Is set, if any other bit in status byte 1 is set.

Table 6-3-2: Streamer status byte 1

Data formats

All ¼-inch streaming drives used on the Supermax are intelligent drives, that automatically formats each data block as it is written on the tape.

Type	Archive 3020	Archive 3020L	Archive 9045L
Tracks	4	4	9
Tape speed	30 ips	30 ips	90 ips
Write format	QIC-11	QIC-11/24	QIC-11/24
Read format	QIC-11 4 track	QIC-11/24 4 track	QIC-11/24 4, 9 track

Table 6-3-3: Streamer data formats

Archive tape drive type 3020L/9045L will use the QIC-11 standard when they are reset, but during normal operation the Archive 9045 runs the QIC-24 standard. This means that you should switch from QIC-11 to QIC-24 whenever you are going to test an Archive 9045. This is done by giving the command 0x27 to the drive. Use the **H** command from the Diagnostic Program to do that.

PERIPHERAL TEST FOR DIOC1/DIOC2

Winchester test

The winchester Diagnostic Program is able to handle all known winchester disk drives and different SASI/SCSI controllers. In order to obtain this flexibility several parameters must be set by the user. If these parameters are incorrectly set, the program will not work properly. Therefore it is important to know which controller and disk type you are going to test. Refer to "Chapter 8-2 Winchester drive parameters" to see description of the different types of controllers used by DDE, as well as a complete list of parameters for all winchester drives. Please notice that the parameter list is a combination of controller-, winchester-, and DIOC type. Timeout is implemented in all handshake routines. If timeout occurs the error is reported.

```
dioc2 E W >M
Diagnostic programs for winchesters

A - Define parameters
B - Write read test
C - CRC test
D - Display skiplist
E - Display error buffer
F - Format drive
G - Format drive retaining skiplist
H - Format track
I - Seek test
J - Read skiplist
K - Write skiplist
L - Random write/read
Q - Exerciser
N - Set command
O - Read single sector and display
P - Reset controller
S - Reassign block
U - Performance test
M - Menu

dioc2 E W >
```

Figure 6-4-1: Menu for winchester test

A – Define parameters

You will only be asked to type in the parameters, needed by the specified controller. Upon start of program always select **A**.

The following parameters can be defined to the program.

Parameter	Comment
Controller number	Controller 0 to 7
Drive number	Drive number 0 to 7
Controller type	
Number of cylinders	
Minimum cylinder	Is the lowest cylinder used in the tests.
Number of heads	
Number of sectors	If number of sectors is incorrectly set, all conversion from logical address to cylinder, head, sector address (and vice versa) is invalid.
ECC error length	
Step period	
Reduced write current	
Write precompensation	
Control byte	Refer to description of controllers
Bytes/track	

Table 6-4-1: Winchester parameters

B – Write/read test

Write/read test will keep the track skiplist, but the data will be destroyed. All errors obtained from the controller are stored in the error buffer. The user selects whether the skiplist should be updated with bad tracks or not. Data fields are written with 0x63 in first pass, complement in next pass(0x9C), then 0x9D, then 0x62, 0x63, 0x9C, and so on.

The test writes an entire track, then reads an entire track. The track number is written in the two first bytes in each sector. When reading a track, the program checks the track number, and if an error occurs (transmission or memory error) write/read test is stopped and the program reports error 0x0F. The test runs from minimum cylinder to maximum cylinder.

C – CRC test

The CRC test reads one track in a command. All errors obtained from the controller are stored in the error buffer. The test runs from minimum cylinder to maximum cylinder.

D – Display skiplist

The skiplist is displayed from memory. If read skiplist or write/ read test has been selected, the skiplist is valid, otherwise the skiplist contains only 0xFF. If format drive is selected an empty skiplist is written on the drive. The empty skiplist contains drive parameters, but of course no bad tracks.

Letter	Command	Description
M	Modify	Double bytes in the skiplist can be modified. The program stays in this mode until an unmodified double byte is written to the skiplist.
N	Next	Display the next sector of the skiplist.
I	Insert	Insert bad tracks in the skiplist. The program stays in this mode until the user tries to insert track 0.
D	Delete	Delete tracks from the skiplist. The program stays in this mode until the user tries to delete track 0.
S	Serial no.	Insert/replace serial number of the disk drive.
W	Write	The 1 Kb skiplist is written on the disk drive.
R	Return	Return to the menu.

Table 6-4-2: Winchester skiplist display commands

NOTE

Editing in the skiplist does not change the skiplist on the drive. Only if write skiplist is selected the modified skiplist is written on the drive.

E – Display error buffer

All errors obtained from write/read test, CRC-test, Seek test or exerciser are displayed. Error buffer is cleared if one of these tests are selected. Maximum number of errors in buffer is 128, if this number is exceeded an overrun is detected, and the buffer is refilled from start. Informations from error buffer are:

Error	Error code in hex form reported from the controller.
Cylinder	Cylinder address (only if address valid).
Head	Head address (only if address valid).
Sector	Sector address (only if address valid).
Track	Track address in HEX code. This information makes it possible to check with the skiplist.
Pass	The pass in which error from the controller occurred.

F – Format drive

Drive will be formatted and an empty skiplist with the correct parameters will be written on the drive. You will be asked for the interleave factor and the physical disk size, which will be written in sector 4 of the skiplist.

G – Format drive retaining skiplist

Drive will be formatted retaining the 1 Kb skiplist. You will be asked for the interleave factor. If there has been a change to any parameters concerning the skiplist, they will also be updated in the skiplist.

H – Format track

The selected track is formatted. This command is only valid if XEBEC controller is used. Data from the track is read sector by sector and stored in memory. When the track is formatted, the data is rewritten. Only data in failing sectors are lost. Information about these sectors is displayed on the terminal.

I – Seek test

This test starts by reading data on minimum cylinder, head number 0, then reads data on maximum cylinder, head number 0, then reads on minimum cylinder + n, head number 0, then reads on maximum cylinder – n, head number 0 where n has a value in the range from 1 to maximum cylinder. Then the test is repeated for head numbers from 1 to maximum head. All errors reported from the controller are stored in the error buffer.

J – Read skiplist

If the controller is not able to read the skiplist, the error information is displayed.

K – Write skiplist

The format of the skiplist is checked. If the format is illegal the skiplist is not written, and an error is reported.

L – Random write/read

Random write/read test will keep track skiplist, but data is destroyed. All errors obtained from controller are stored in the error buffer. When you select this test you will be asked for a number of sectors ranging from 1 to 32. This is the number of sectors each time written with a continuous counter and then read back and checked for correct content. The sector address is calculated on a pseudo random basis.

Q – Exerciser

Sectors are read one by one on the selected track. Errors are stored in the error buffer. The exerciser keeps on reading the selected track until another track is selected or control E is pressed.

Key	Command
↑	Increment head number
↓	Decrement head number
←	Decrement cylinder number
→	Increment cylinder number
X	Select read operation
Y	Select no read operation
R	Restore drive

Table 6-4-3: Winchester exerciser commands

N – Set command

This feature enables the user to send commands to controllers. Only commands without data transfer from or to the drive may be set. The first byte must contain the number of command bytes transmitted to the controller. Only use Set command to exercise the controller, not the drive.

NOTE

During normal test conditions it is **NOT** necessary to use this feature.

O – Read single sector and display

The selected sector is read into memory and displayed on the terminal. The following may be used:

Letter	Cmd	Description
M	Modify	Modify bytes in the sector
N	Next	Read next sector
W	Write	Write current sector
P	Previous	Read previous sector
D	Display	Display next part of the sector if the sector size is 256, part 0 is valid if the sector size is 512, part 0,1 are valid if the sector size is 1024, part 0,1,2,3 are valid
A	Address	Read a new sector address

Table 6-4-4: Winchester sector display commands

P – Reset controller

All controllers on the SCSI bus are reset.

S – Reassign block

This command is only implemented on the embedded disk controllers. The Reassign block command requests the drive to reassign a defective block to a spare block reserved for this purpose. If a spare block is available on the track, where the defect block is located, this block will be used, otherwise a spare block on a other track will be used. The defect block address is added to the grown defect list. It is not necessary to reformat the drive after using the reassign block command, and only one block of data is corrupted. If the drive is reformatted it will use the grown defect list, and the primary defect list to map out all defect blocks so the media appears error free.

It is possible to use either a sector address or the cylinder, head and sector number as input to the command. Sector 1 of the skiplist will be updated with the sector address. This information is not used by any programs.

U – Performance test

This command can be used to measure the performance of the disk drive. When the test is completed the actual time used is the number written on the terminal times 80 ms.

M – Menu

Display the menu on the terminal.

R – Return to main menu

Return to the menu of peripheral units.

Skiplist

The skiplist contains information about the physical parameters of the drive, and the type of controller. This information is used to initialize the disk controller, if necessary. The skiplist also contains information about all the bad tracks on the drive, and is used by the disk driver program to skip the tracks if the address of that track is included in the disk command issued by the operating system. The track skipping is invisible for the operating system. Track skipping is not used on winchesters with embedded controller.

Address	Content
0x00-0x3D	Two bytes for every bad track on the drive. The numbers must be arranged in increasing order, and the list must be continued with 0xFF until byte number 0x3F is reached.(byte 0x3E and 0x3F must be 0xFF hex). If the first two bytes in the skiplist are 0xFFFE, sector 2 and sector 3 of the skiplist contain the bad tracks.
0x3E	Must contain 0xFF.
0x3F	Must contain 0xFF.
0x40	Number of heads.
0x41	MSB of number of cylinders.
0x42	LSB of number of cylinders.
0x43	Number of sectors on a track.
0x44	Interleave factor.
0x45	Hard sector flag. (must contain 0xFF)
0x46	Not used

Table 6-4-5: Winchester skiplist address 0x00 – 0xFF (1 of 2)

Address	Content
0x47	Not used
0x48	Not used
0x49	Control byte for controller.
0x4A	MSB of starting cylinder for reduced write current.
0x4B	LSB of starting cylinder for reduced write current.
0x4C	MSB of starting cylinder for write precompensation.
0x4D	LSB of starting cylinder for write precompensation.
0x4E	Not used
0x4F	Controller type. Must contain 0x02 if XEBEC S1410 is used. Must contain 0x01 if DTC 600 is used. Must contain 0x08 if ADAPTEC ACB 4000 is used. Must contain 0x08 if ADAPTEC ACB 5580 is used. Must contain 0x08 if XEBEC S1490 is used. Must contain 0x04 if NEC DS800B is used. Must contain 0x09 if EMBEDDED CONTROLLER is used.
0x50	Sector size. For all types except embedded controller the sector size is 256 (0x01). For embedded controller the sector size is 512 (0x02) or 1024 (0x04).
0x51-0xEF	Not used
0xF0-0xFF	Serial number

Table 6-4-5: Winchester skiplist address 0x00 – 0xFF (2 of 2)

Skiplist address 0x100 – 0x1FF
Only used if the two first bytes in sector 1 contain 0xFFFE. Entire sector contains bad tracks or 0xFFFF. If embedded controller is used, this sector contains block addresses on blocks that have been reassigned. The block address contains of 4 bytes MSB...LSB. Msb is always 0x00.

Skiplist address 0x200 – 0x2FF
Only used if the two first bytes in sector 1 contain 0xFFFE, and the entire 2. sector contains bad tracks. The entire sector contains bad tracks or 0xFFFF. If the entire sector is used for bad tracks the two last bytes must contain 0xFFFF.

Skiplist address 0x300 – 0x3FF
This sector is used by the operating system, and describes the configuration of a winchester disk. The sector is a part of the skiplist.

```
      0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
300   03 F4 00 00 01 10 00 00 00 A0 00 00 00 A0 00 00  ........ ... ..
310   00 10 00 00 00 04 00 00 00 00 00 00 00 00 00 00  ................
320   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
330   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
340   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
350   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
360   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
370   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
380   00 00 00 00 73 75 62 64 69 73 6B 32 20 70 72 65  ....subdisk2 pre
390   73 65 6E 74 FF FF FF FF FF FF FF FF FF FF FF FF  sent............
3A0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ................
3B0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ................
3C0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ................
3D0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ................
3E0   02 50 00 00 02 60 00 00 FF FF FF FF FF FF FF FF  .P...'..........
3F0   FF FF FF FF FF FF FF FF 02 50 00 00 02 50 00 00  .........P...P..
```

Figure 6-4-2: Display of configuration table on a winchester disk.

Address	Content
0x300-0x303	Four bytes containing the hexadecimal value of the physical disk size, in this example a 63 Mb disk.
0x304-0x383	32 times four bytes containing the size of each logical disk on the physical disk. The maximum number of logical disks on a physical disk is 32. In this example there are 5 logical disks, 17Mb, 10Mb, 10Mb, 1Mb and 0.25Mb. Please note that a logical disk size set to 0x00000000, indicates that the logical disk is not used.
0x384-0x393	This text string indicates to the operating system that the sector is valid.
0x394-0x3DF	Not used.
0x3E0-0x3EF	Four times four bytes used for boot pointers 0 through 3. Each pointer contains the hexadecimal address on the winchester disk, where the boot information is found. Normally pointer 0 points to the **Supermax Operating System** and pointer 1 points to the Diagnostic Programs. 0xFFFFFFFF indicates that the pointer is not used.
0x3F0-0x3F7	Not used.
0x3F8-0x3FB	This is a temporary pointer used by the Diagnostic Program.
0x3FC-0x3FF	This is the actual boot pointer used by the boot prom on the DIOC. This is the address on the winchester disk from where to load the system.

Table 6-4-6: Winchester configuration sector.

Controllers used on the Supermax

One of the parameters used by the test program is the controller type. If you select unknown type no initialize command will be issued, and you will be unable to format the drive.

Seen from the program the controllers differ in two ways:

1) The way they handle initialize and format commands.
2) The function of the control byte. The control byte (set by the user) is the last byte in all commands to the controllers. This byte must be set to match the specific controller.

XEBEC S1410

The XEBEC S1410 controller can control up to two 5.25 inch winchester disk drives with ST-506 interface. Please note that the two drives must have the same parameters. When all parameters are set under **A** in the menu (Set Parameters) the controller is initialized with the following parameters:

Number of cylinders
Number of heads
Starting cylinder for reduced write current
Starting cylinder for write precompensation
ECC data burst length. If set to zero no error correction is attempted, max. set to 11.

Control byte: r0000sss (8 bits)

r 1 – Disable the four retries on all disk access commands.
0 – Enable the four retries on all disk access commands.
During drive test and formatting, this bit should be set to 1.

sss Set to 111 for max. step speed.

During test, control byte is normally set to 87 Hex.
Number of sectors/track is always 32 when XEBEC S1410 is used.

DTC 610

The DTC-610 controller can control up to four CDC 9410 series winchester disk drives. The controller is initialized only with number of heads. In case this controller is used, all other disk parameters (except interleave factor) only affects the program and not the controller.

Control byte: abc00000

- **a** 1 – Disable retry
  - 0 – Enable retry
- **b** 1 – Disable error correction
  - 0 – Enable error correction
- **c** 1 – Disable overlap seek
  - 0 – Enable overlap seek

During test, control byte is normally set to 0xC0 Hex.

Number of sectors/track is always 42 when DTC 610 is used.

ADAPTEC ACB 4000

The ADAPTEC ACB 4000 controller can control up to two 5.25 inch winchester disk drives with ST-506 interface. The controller is not initialized by the program. At reset time the controller reads the disk parameters from the disk. Therefore, the program is able to read the disk parameters from the controller. If the controller is unable to read the parameters, the program will report an error. The following disk parameters are read by the program from the controller or typed in by the user:

Number of cylinders
Number of heads
Starting reduced write current
Starting write precompensation
Step period

If the user wants to modify these parameters, it will only affect the controller if the drive is formatted.

The control byte must always be set to 00. Error correction and retries cannot be disabled.

NOTE The ADAPTEC controller has 33 sectors/track when using interleave factor 2 or more, but only 32 sectors/track using interleave factor 1.

XEBEC S1490

The XEBEC S1490 controller can control up to two winchester disk drives that are compatible with the SMD interface. The controller is not initialized by the program. At reset time the controller reads the disk parameters on the disk. Therefore, the program is able to read the disk parameters from the controller. If the controller is unable to read the parameters, the program will show an error. The following disk parameters are read by the program or typed in by the user:

Number of cylinders
Number of heads
Number of sectors/track
Number of bytes/track
Maximum burst error correction

If the user wants to modify these parameters, it will only affect the controller if the drive is formatted. If format retaining old skiplist is selected, it is possible to change drive parameters without formatting the drive.

Control byte: r000ss00

r 1 – Disable the retry after errors on all disk access commands.
0 – Enable the retry after errors on all disk access commands.

ss Head strobe
00 – normal
01 – strobe late
10 – strobe early

Control byte is normally set to 0x80 Hex during test.

NOTE

The controller reserves cylinder 0 on each drive for internal use. This means that the actual track address of the disk have a track displacement matching the number of heads of the disk drive. This is especially important when talking about bad tracks and the skiplist. The actual bad track is in fact the *number of heads* added to the track written in the skiplist. When you have to change the XEBEC S1490 controller with one that does not reserve cylinder 0, you must update the skiplist.

NEC DS800B

The NEC DS800B controller can control up to four winchester disk drives, that are compatible with the SMD interface. Upon reset the controller must be initialized with the following parameters, which must be set by the user.

Number of heads
Number of cylinders
Number of sectors/track

The controller cannot read anything from the disk drive unless initialized by the program.

Control byte: rc000000 (8 bits)

r 1 – Disable the retry after errors on all disk access commands.
0 – Enable the retry after errors on all disk access commands.
c 0 – Automatic correction of correctable errors.
1 – No correction of correctable errors.

Control byte is normally set to 0xC0 Hex during test.

ADAPTEC ACB 5580

The ADAPTEC ACB 5580 controller can control up to four SMD compatible disk drives. The controller is not initialized by the program. At reset time the controller reads the disk parameters from the disk. Therefore, the program is able to read the disk parameters from the controller. If the controller is unable to read the parameters, the program will report an error. The following disk parameters are read by the program from the controller or typed in by the user:

Number of cylinders
Number of heads
Number of sectors

If the user wants to modify these parameters, it will only affect the controller if the drive is formatted. The control byte must always be set to 00. Error correction and retries cannot be disabled.

EMBEDDED controller

The SCSI controller is embedded in the drive electronics. The controller is able to handle media defects. When the drive is formatted it uses two different sets of defect information:

- **Primary defect list.**
  This list is supplied by the manufacturer and is resident on the drive.
- **Grown defect list.**
  This list contains defects which have been identified to the drive using the reassign block command.

Normally the drive is formatted using both lists, but it is possible to clear the grown defect list during the format procedure. If a hard error occurs during operation, it is recommended to use the reassign block command. It is not necessary to format the drive after using the reassign block command.

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PERIPHERAL TEST FOR DIOC1/DIOC2

Tape test

The tape drive Diagnostic Program is able to test any tape drive, which conforms to the SCSI standard for tape drives.

When typing **M <CR>** the menu of the current subprogram will be displayed on the terminal. The example shows the menu from the tape drive Diagnostic Program.

```
dioc2 E T >M
Diagnostic program for tape drives

A - Define parameters
B - Write/read test
C - Read tape
D - Rewind
E - Display error buffer
F - Write tape
H - Write variable block mode
I - Read variable block mode
J - Write file mark
P - Reset controller
R - Return to main menu
M - Menu

dioc2 E T >
```

Figure 6-5-1: Menu for tape test

Whenever the prompt is displayed on the terminal it is possible to select tests.

A – Define parameters

The following parameters can be defined to the program.

- Controller number
- Tape speed
- Tape density
- Block size
- Number of blocks in each command

Normally the default values shown on the terminal should be used. Otherwise you should consult the data sheet of the unit you are going to test.

B – Continuous write/read

The number of blocks selected by the user is written on the tape. When the last block is written the tape is rewound. Then a read command is issued. When reading, the program checks the data pattern if requested by the user. If any errors occur, the error buffer is updated.

C – Read tape

The drive reads the tape from the current tape position, until a file mark is found, a hard error occurs, end of tape occurs, etc. If **Ctrl E** is pressed the drive stops and the program reports the number of commands issued.

D – Rewind

Rewinds the tape to the beginning of the tape.

E – Display error buffer

The error buffer contains information about all errors obtained from the controller. An example of the error buffer looks like this:

```
Sense byte  00  02  17  18
            XX  YZ  WW  WW
```

Code	Means
XX	Must be 0x70 or 0xF0.
Y	The 4 bits with the following information Bit 7 is File mark detected. Bit 6 is End Of Medium. Bit 5 is Incorrect Length Indicator. Bit 4 is Always 0.
Z	Tape error code.
WWWW	Retry counter.

Table 6-5-1: Tape error buffer

F – Write tape

The drive writes the tape from the current tape position, until a hard error occurs, end of tape or **Ctrl E** is pressed. Then the tape motion stops, and the program reports the number of commands issued.

H – Write variable block mode

NOTE

During normal test conditions it is **NOT** necessary to use this feature.

I – Read variable block mode

NOTE

During normal test conditions it is **NOT** necessary to use this feature.

J – Write file mark

A file mark is written on the tape at the current tape position.

P – Reset controller

A reset of the SCSI controller will be performed.

R – Return to the main menu

Return to menu for the peripheral units.

M – Menu

Display the menu on the terminal.

7 PERIPHERAL TEST FOR DIOC3

Peripheral test for DIOC3

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PERIPHERAL TEST FOR DIOC3

Introduction to peripheral test

The Diagnostic Program for peripheral units is also loaded into the DIOC3 when loading the Diagnostic Programs. In order to run the program just type **T <CR>** when the DIOC3 is in the main menu. When doing that the prompt will change. A letter indicating the subprogram currently running will be in the prompt. The following letters might appear.

Letter	Subprogram
P	Peripheral Units
W	Winchester test
F	Floppy test
T	Tape drive test
M	Multiple select

Table 7-1-1: Prompt letter for subprogram

Typing **M <CR>** will show the menu of the current subprogram.

The example shows the first submenu on the DIOC3.

```
dioc3 E P > M
Diagnostic program for peripheral units

A - Select all units on SCSI interface 0
B - Select all units on SCSI interface 1
E - Display errors on all peripheral units
F - Test floppy drive
T - Test tape drive
W - Test winchester drive
R - Return to main menu
M - Menu

dioc3 E P >
```

Figure 7-1-1: Menu for peripheral tests

A – Select all units on SCSI interface 0

When selecting this entry the following will be performed:

- Reset SCSI interface 0.
- Read from ID 0 to ID 6 to find out which units are connected to SCSI interface 0.
- If a unit is found to be present on the interface, then the manufacturers name, type, model and revision is read and displayed.
- If the type is a winchester then the parameters are read from the configuration table in the first track of the winchester. This configuration table is written on the winchester by the Diagnostic Program, when formatting it.

- If the type is a tape drive, then the parameters are read from the drive.

When all this is done a message is written on the terminal.

The following is an example of a DIOC3 with two winchesters on ID 0 and ID 1.

```
dioc3 E P > A
Reset SCSI interface: 0
SCSI channel: 0 ID number: 0            Unit type: Winchester
Name: MAXTOR  XT-3280                   Revision:  E.3
SCSI channel: 0 ID number: 1            Unit type: Winchester
Name: MAXTOR  XT-3280                   Revision:  E.3
No unit on SCSI channel: 0  ID number: 2
No unit on SCSI channel: 0  ID number: 3
No unit on SCSI channel: 0  ID number: 4
No unit on SCSI channel: 0  ID number: 5
No unit on SCSI channel: 0  ID number: 6
dioc3 E P >
```

Figure 7-1-2: Display of SCSI devices on the SCSI channels

B – Select all units on SCSI interface 1

This entry performs the same as *A*, except that SCSI interface 1 is used.

E – Display errors on all peripheral units

This entry will write the error buffers concerning all units on the terminal. One unit at a time will be displayed. This is an easy way to get an overview of the test results. Otherwise each unit would have to be selected one at a time in order to display the error buffer concerning that unit.

F – Test floppy drive

This entry gives you the subprogram used to test floppy disk drives.

T – Test tape drive

This entry gives you the subprogram used to test tape drives.

W – Test winchester drive

This entry gives you the subprogram used to test winchester disk drives.

R – Return to main menu

This entry will return the DIOC3 to the main menu.

M – Menu

This entry will show the menu on the terminal.

Cancel a running test

When running peripheral unit test, it is recommended to use **Ctrl E** (soft cancel) to cancel a running test. When **Ctrl E** is present, the program will cancel the test, as soon as the command to the drive has completed, and then return to the menu. **Ctrl E** only affects the following tests:

Commands	Subprogram
A, B, C, D, I, K	Winchester drive test.
A, B, C, D, F, G, H, I	Tape drive test.
A, B, C, F, K	Floppy drive test.

Table 7-1-2: Soft cancel a running test

PERIPHERAL TEST FOR DIOC3

Floppy test

The DIOC3 4000 module in the Supermax card family is equipped with the National DP8473 floppy disk controller. The Diagnostic Program for Floppy Disk Drives is able to handle all kinds of formats on 3½" and 5¼" disk drives.

When typing **M <CR>** the menu of the current subprogram will be displayed on the terminal. The example shows the menu of the floppy diagnostic program, where floppy disk drive number 0 is selected.

```
dioc3 E F > M
Diagnostic program for floppy

              ID number: 0            Unit type: Floppy
A - Seek test
B - Write/read test
C - CRC test
F - Format disk
O - Repeat test(s)
G - Format track
K - Exerciser
L - Read single sector and display
S - Set command
P - Set floppy parameters
E - Display error buffer
N - Select new floppy
T - Enable test of both floppy drives
Z - Reset floppy interface
R - Return to main menu
M - Menu

dioc3 E F >
```

Figure 7-2-1: Menu for floppy test

All tests start by issuing a restore command to the drive. If the drive is not ready, the test stops and the error is reported. If other kinds of errors occur during a restore command the error is reported to the error buffer and the test is continued.

A – Seek test

This test starts by reading data on cylinder 0, head number 0, then reads data on maximum cylinder, head number 0, then reads on cylinder n, head number 0, then reads on maximum cylinder – n, head number 0, where n has a value in the range from 1 to maximum cylinder. Then the test is repeated for head number 1. All errors reported from the controller are stored in the error buffer.

B – Write/read test

The test writes from track 0 to maximum track, then reads from maximum track to track 0. Head number, cylinder number and sector number in all sectors on each track are verified and the error buffer is updated if any errors occur. The following test pattern is written in all sectors of the diskette:

Byte	Pattern
0	Head number (00 head 0, 01 head 1)
1	Cylinder number (0 to maximum cylinder)
2	Sector number (1 to maximum sector)
3 – Sector size	Pattern 0x63

Table 7-2-1: Floppy write/read pattern

C – CRC test

All tracks from track 0 to maximum track are read. The error buffer is updated if any errors occur.

F – Format disk

The floppy disk is formatted. After formatting one track, the entire track is read. All errors reported from the controller are stored in the error buffer.

O – Repeat test(s)

If you add this option to the test(s) mentioned above, the test(s) will repeat itself (themselves) until otherwise canceled.

G – Format track

One track can be selected and that track will be formatted. After formatting the track, the entire track is read. All errors reported from the controller are stored in the error buffer.

K – Exerciser

Upon start of the exerciser, the drive will restore and no read operation is performed. When typing X all sectors are read on the selected track one by one. Errors are stored in the error buffer. The exerciser keeps on reading the selected track until another track is selected or until typing Y. The following commands can be given to the the exerciser.

Key	Command
Ctrl K	Select head 1
Ctrl J	Select head 0
Ctrl H	Decrement cylinder number
Ctrl L	Increment cylinder number
X	Select read operation
Y	Select no read operation
R	Restore drive

Table 7-2-2: Floppy exerciser commands

In combination with an alignment diskette the exerciser can be used to test track alignment, head alignment etc.

L – Read single sector and display

The selected sector is read into memory and displayed on the terminal. The following commands may be given to the program:

Letter	Command	Description
R	Return	Return to menu
A	Address	Select a new disk address
S	Sector	Select a new sector address
C	Cylinder	Select a new cylinder number
D	Display	Display next part of the sector. Is used to display part of the sector that lies beyond the first 256 bytes.
N	Next	Read next sector
P	Previous	Read previous sector
M	Modify	Modify bytes in the sector[1)]
W	Write	Write current sector

Table 7-2-3: Floppy sector display commands

1) The modified bytes are not written on the floppy disk until a write command is issued

S – Set command

This feature enables the user to send commands to the drive.

NOTE

During normal test conditions it is **NOT** necessary to use this feature.

P – Set floppy parameters

The floppy parameters can be set or changed, when running the different tests. The default floppy parameters will be initialized to the following diskette format:

ID	Floppy	Diskette format
0	3½"	PC/AT 720 kb
1	5¼"	DDE 560 kb

Table 7-2-4: Default floppy parameters

There are four standard parameter settings, two for 5¼" floppy disk, format DDE 560 kb or PC/AT 1.2 Mb and two for 3½" floppy disk format PC/AT 744 kb or PC/AT 1.44 Mb. If you want to use any other floppy disk standard, the parameters can be changed manually.

Parameter	560 kb	1.2 Mb	720 kb	1.44 Mb
Sector size	256	512	512	512
Number of sectors/track	16	15	9	18
Number of cylinders	80	80	80	80
Density	L	H	L	H
Step rate[1)]	0x0E	0x0C	0x0E	0x0C
Head settling time[2)]	0x02	0x04	0x02	0x04
Gap length	0x20	0x20	0x1B	0x1B
Gap format	0x32	0x32	0x54	0x54

Table 7-2-5: Floppy parameters

1) (0x10-value)millisec × 2

2) value × 2 millisec

E – Display error buffer

All errors obtained from the floppy disk drive during one or more tests are displayed. The error buffer is cleared every time one of these tests are selected from the menu. If a test is selected to be repeated the error buffer will only be cleared before the first pass. The maximum number of errors in the error buffer are 128. If this number is exceeded an overrun is detected, and the first 127 errors are saved. Any additional errors will replace each other at location 128. Information from the error buffer are:

Name	Description
ID	Drive number
Com	Command code. 0x04 = Format command. 0x08 = Read command. 0x0a = Write command. 0x0b = Seek command.
Stat2	See status register 2
Stat1	See status register 1
Stat0	See status register 0
Cylinder	Cylinder address.
Head	Head address.
Sector	Sector address.
Pass	The pass in which the error from the floppy controller occurred.
Time from reset	The time from reset when the error from the floppy controller occurred.

Table 7-2-6: Floppy error buffer

Bit	Name	Description
7	Nc	Not used.
6	Control mark	Floppy controller tried to read a sector which contained a deleted data address mark.
5	CRC error	Valid only if bit 5 of ST1 is set. 0 = CRC error detected in the address field. 1 = CRC error detected in the data field.
4	Wrong track	The floppy controller cannot find the track.
3	Scan equal hit	Not used.
2	Scan not satisfied	Not used.
1	Bad track	Bad track on the disk.
0	Missing address mark	Valid only if bit 0 of ST1 is set. 0 = Cannot find address field address mark. 1 = Cannot find data field address mark.

Table 7-2-7: Floppy status register 2

Bit	Name	Description
7	End of track	Floppy controller transferred the last byte of the last sector, without the TC pin becoming active.
6	Nc	Not used.
5	CRC error	CRC error detected, see ST2 bit 5.
4	Overrun	DMA did not respond to data request in one byte time.
3	Nc	Not used.
2	No data	Cannot find the sector.
1	Not writable	Write protect pin is active.
0	Missing address mark	The controller cannot find the address or data field mark, see ST2 bit 0.

Table 7-2-8: Floppy status register 1

Bit	Name	Description
7 – 6	Interrupt code	00 = Normal termination of command. 01 = Abnormal termination of command. 10 = Invalid command issue. 11 = Ready changed state.
5	Seek end	Seek or recalibrate command completed.
4	Equipment check	After a recalibrate command, track 0 signal failed to occur.
3	Not ready	Ready pin is inactive.
2	Head address	0 = head 0 selected. 1 = head 1 selected.
1 – 0	Drive number	00 = drive 0 selected. 01 = drive 1 selected.

Table 7-2-9: Floppy status register 0

N – Select new floppy

This is used to select the other drive on the floppy disk interface. You will be asked about the ID number.

T – Enable test of both floppy drives

This is used to tell the program to test both floppy disk drives. When selecting this one for the first time a **M** will appear in the prompt indicating that multiple test is enabled. When selecting any of the tests A, B, C, or F, that test will be performed on both floppy disk drives. Any errors obtained from the test will be saved in each units own error buffer. If selecting *T* again the **M** will disappear from the prompt, indicating that multiple test is disabled. The two drives **must** use the same format on the diskette.

Z – Reset floppy interface

This command will issue a reset to the floppy interface and will initialize parameters for the controller. If the default parameters should be used it is enough to issue this command. If the parameters must be changed you should use the command **P**.

R – Return to main menu

Return to the menu for peripheral units.

M – Menu

Display the menu on the terminal.

Internal error codes

During execution of a command the floppy controller goes through different phases. If the controller enters an unexpected phase it is considered an error and the test is terminated. The following error codes are not included in the standard error codes, but are internally generated error codes.

Error code	Means
0x10 – 0x1F	Floppy controller not ready.
0x20 – 0x2F	Unexpected interrupt from the floppy controller.
0x30 – 0x3F	No interrupt occurred from the floppy controller.
0x40 – 0x4F	Data buffer not ready during reset command.
0x50 – 0x5F	Data buffer not ready during seek command.
0x60 – 0x6F	Data buffer not ready during format command.
0x70 – 0x7F	Data buffer not ready during write/read command.
0x80 – 0x8F	Wrong status occurred from the floppy controller.
0xF0	Floppy interface not implemented.
0xF1	Illegal command to the floppy controller.
0xF2	Illegal sector size to the floppy controller.
0xF3	Floppy disk not ready.

Table 7-2-10: Floppy internally generated error codes

PERIPHERAL TEST FOR DIOC3

Tape test

The tape drive Diagnostic Program for the DIOC3 is able to test any tape drive, that are compatible with the SCSI interface descriptions for tape drives. This includes the streaming tape drives.

When typing **M <CR>** the menu of the current subprogram will be displayed on the terminal.

The example shows the menu of the tape drive diagnostic program.

```
dioc3 E T > M
Diagnostic program for tape drives

SCSI channel: 1 ID number: 6          Unit type: Tape
Name: EXABYTE  EXB-8200               Revision:  241D
A - Rewind
B - Write tape
C - Read tape
D - Write/read test
F - Erase
G - Retension
H - Write file mark
I - Search to file mark
O - Repeat test(s)
J - Read parameters from tape drive
L - Read single block and display
S - Set command
P - Set tape drive parameters
E - Display error buffer
N - Select new tape drive
T - Enable test of all tape drives
Z - Reset SCSI interface
R - Return to main menu
M - Menu

dioc3 E T >
```

Figure 7-3-1: Menu for tape test

Whenever the prompt is displayed on the terminal it is possible to select tests. Before running any tests one must be sure that the SCSI interface has been reset and that the program knows the parameters of the units, that are going to be tested.

A – Rewind

Rewinds the tape to the beginning of the tape.

B – Write tape

The number of blocks selected by the user is written on the tape from the current tape position. The four first bytes in each block contains the SCSI number, the ID number and the block number and the rest of the block contains the byte pattern selected by the user. When the selected number of blocks are written, or when **Ctrl E** is pressed, a file mark is written and the tape motion stops.

C – Read tape

The drive reads the tape from the current tape position, until a file mark occurs. If any errors occur the error buffer is updated.

D – Write/read test

The number of blocks selected by the user is written on the tape. The four first bytes in each block contains the SCSI number, the ID number and the block number and the rest of the block contains the byte pattern selected by the user. When the last block is written a file mark is written and the tape is rewinded. Then a read command is issued. When reading, the program checks the header field in each block. If any errors occur, the error buffer is updated.

F – Erase

The entire tape is erased.

G – Retension

This command rewinds the tape to the beginning, then winds it to the end and then rewinds it to the beginning again.

H – Write file mark

A file mark is written on the tape at the current tape position.

I – Search to file mark

The drive reads the tape searching for a file mark. When a file mark is found tape motion stops.

O – Repeat test(s)

If, when selecting test(s) A, B, C, D, F, G, H, I, this option is also added, the test(s) will repeat itself (themselves) until otherwise canceled.

J – Read parameters from tape drive

Parameters are read from the tape drive, in order to find out what type it is and in order to set default parameters for the tests.

L – Read single block and display

The program will always start by reading block 0 into the memory and display it on the terminal. The following commands may be used:

Letter	Command	Description
R	Return	Return to the menu
A	Address	Select a new tape address
B	Block	Select a new block number
D	Display	Display next part of the block. Is used to display part of the block that lies beyond the first 256 bytes.
N	Next	Read next block
P	Previous	Read previous block

Table 7-3-1: Tape block display commands

S – Set command

This feature enables the user to send commands to the controller. The first byte must contain the number of command bytes transmitted to the drive. During normal test conditions it is **NOT** necessary to use this feature.

P – Set tape drive parameters

The following tape drive parameters must be set before running any tests. Not all parameters affect all tests.

- Block size.
- Number of blocks to transfer in one command.
- Number of blocks to write.
- Pattern for test.
- Select continue or stop test, if an error occurs.
- Command delay, used for testing non-streaming mode. A value between 0x10-0x20 is a typical delay value for non-streaming mode.
- Disconnect/Reconnect option. Defaults to 0x03 which enables the D/R option. Type 0x00 in order to disable the D/R option. Disconnect/Reconnect is a feature in the SCSI interface that enables the target to free the SCSI bus during execution of a command. Consequently the DIOC3 is able to have pending commands to each device on the SCSI bus.

E – Display error buffer

All errors obtained from the tape drive during one or more tests are displayed. The error buffer is cleared every time one of these tests are selected from the menu. If a test is selected to be repeated the error buffer will only be cleared before the first pass. The maximum number of errors in the error buffer are 128. If this number is exceeded an overrun is detected, and the first 127 errors are saved. Any additional errors will replace each other at location 128.

Information from the error buffer are:

Name	Description
SCSI	SCSI channel number.
ID	Drive number.
Com	SCSI standard command. 0x00 means Test unit ready 0x01 means Rewind 0x03 means Request sense 0x08 means Read 0x0A means Write 0x10 means Write file mark 0x11 means Searching for file mark 0x12 means Inquiry 0x19 means Erase 0x1A means Mode sense 0x1B means Retension
Error	Error code in hex form reported from the drive. Bit(7) File mark Bit(6) EOM. End of media Bit(5) ILI. Incorrect length indicator Bit(4) Not used Bit(0-3) Error code
Status	Status code in hex form reported from the drive. Must be 0x70 or 0xF0.
Block	Block address (only if address valid ˝ status code = 0xF0).
Pass	The pass in which the error from drive occurred.
Time from reset	The time from reset when the error from the drive occurred.

Table 7-3-2: Tape error buffer

N – Select new tape drive

This is used to select another drive on one of the SCSI interfaces. You will be asked about SCSI channel number and ID number.

T – Enable test of all tape drives

This is used to tell the program to test all tape drives connected to both SCSI interfaces. When selecting this one for the first time a **M** will appear in the prompt indicating that multiple test is enabled. When selecting any of the tests A, B, C, D, F, G, H or I, that test will be performed on all tape drives which have had their parameters read by the program. The test starts on SCSI 0 ID 0 and ends on SCSI 1 ID 6. If the Disconnect/Reconnect option is enabled the test will run simultaneously on all tape drives. Any errors obtained from the test will be saved in each units own error buffer. If selecting *T* again the **M** will disappear from the prompt, indicating that multiple test is disabled.

Z – Reset SCSI interface

A reset will be performed on the SCSI interface currently in use.

R – Return to main menu

Return to the menu for the peripheral units.

M – Menu

Display the menu on the terminal. If *J* has been selected the first two lines of the menu will tell about the selected tape drive.

Different data formats

All ¼-inch streaming drives used on the Supermax are intelligent drives, that automatically formats each data block as it is written on the tape. Different drives use different formats, but in general drives are backward compatible, which means newer drives are able to read the format written by older drives.

Internal error codes

During execution of an SCSI command the SCSI controller goes through different phases. If the controller enters an unexpected phase it is considered an error and the test is terminated. The following error codes are not included in the standard SCSI command format, but are internally generated error codes. If any of those errors are encountered a Reset SCSI command must be performed.

Error codes	Means
0x00 – 0x0F	Time out in handshake between SCSI controller and drive.
0x10 – 0x1F	Wrong interrupt (Only when Disconnect or Reconnect enabled)
0x80 – 0x8F	Illegal interrupt.
0xA0 – 0xAF	Illegal interrupt.

Table 7-3-3: Tape internal generated error codes

PERIPHERAL TEST FOR DIOC3

Winchester test

The winchester Diagnostic Program for the DIOC3 is able to handle all embedded winchester disk drives, which are supported by DDE. In order to format a winchester disk some parameters must be set. Therefore it is important to know which winchester disk drive you are going to format. In Chapter 8 – 2 of this manual you will find a description of the different types of winchester disk drives used by DDE, as well as a complete list of parameters for the disk drives. Please notice that the parameter list is a combination of controller-, winchester-, and DIOC type. Only use the parameters indicated for DIOC3.

When typing **M <CR>** the menu of the current subprogram will be displayed.

The example shows the menu of the winchester test program.

```
dioc3 E W > M
Diagnostic program for winchester

SCSI channel: 0 ID number: 0          Unit type: Tape
Name: MICROP  1528-15MD1052406        Revision:  AS25
A - Seek test
B - Write/read test
C - CRC test
D - Random write/read
H - Verify mirrored disks
O - Repeat test(s)
F - Format drive
G - Reassign block
I - Performance test
J - Read parameter from winchester
K - Exerciser
L - Read single sector and display
S - Set command
P - Set winchester parameter
W - Set-up of disk system
E - Display error buffer
N - Select new winchester
T - Enable test of all winchester units
Z - Reset SCSI interface
R - Return to main menu
M - Menu

dioc3 E W >
```

Figure 7-4-1: Menu for winchester test

When the prompt is displayed on the terminal, tests can be selected

by typing in the corresponding letter.

A – Seek test

This test starts by reading data on cylinder 0, head number 0, then reads data on maximum cylinder, head number 0, then reads on cylinder *n*, head number 0, then reads on maximum cylinder – *n*, head number 0 where *n* has a value in the range from 1 to maximum cylinder. Then the test is repeated for head numbers from 1 to maximum head. All errors reported from the drive are stored in the error buffer.

B – Write/read test

Write/read test will keep the configuration table, but the data on the disk drive will be destroyed. All errors obtained from the drive are stored in the error buffer.

The test writes on the entire disk, then reads the entire disk. The program will write and read a number of sectors in each command. This number can be changed by selecting the *P* entry. The test runs from minimum cylinder to maximum cylinder.

The data is initialized with a counter, starting with the value of the first sector address in each command. When reading the sectors, the program checks all data.

C – CRC test

The CRC test reads one track/command from the disk drive. When doing that a CRC test is performed. All errors obtained from the controller are stored in the error buffer. The test runs from cylinder 0 to maximum cylinder.

D – Random write/read

Random write/read test will keep the configuration table, but the data on the disk drive is destroyed. All errors obtained from the drive are stored in the error buffer.

The program will write a number of sectors on the disk drive. This number can be changed when selecting *P* entry. The number of sectors will be written with the SCSI number, the ID number and the sector number followed by a continuous counter and then read back and checked for correct content. Between the write and the read operation, the drive will read from track 0 before seeking back. The sector address is calculated on a pseudo random basis.

H – Verify mirrored disks

This test will verify that the data is the same on two mirrored disks. This is done by reading from both disk and comparing the data. If data are not the same, an error 0x0f is stored in the error buffer, all errors obtained from the disk drives are also stored in the error buffer.
If a disk is not mirrored or the disk is not OK or the mirrored disk is not installed, a CRC test will be performed instead. Before starting this test, the enable test of all winchester units must be done first.
The test runs from disk address 0x2000 to the end of the system disk (calculated from the physical disk size). If the CRC test is performed, the test will run to the maximum disk address. The program will read a number of sectors on the disk drive. This number can be changed when selecting *P* entry.

O – Repeat test(s)

If, when selecting test(s) A, B, C, D, H, this one (O) is also selected, the test(s) will repeat itself (themselves) until otherwise cancelled.

F – Format drive

Before selecting this entry the disk parameters must have been set by selecting the *P* entry. The manufacturer, the type and preferably the serial number of the disk drive must be known, in order to answer the questions asked by the program. The following will be printed on the terminal, when selecting this entry.

```
F - Format drive
G - Format drive retaining the configuration table
W - Write a new SMOS configuration table on the disk
S - Write a new SVR4 configuration table on the disk
R - Return to menu
Select command:
```

Figure 7-4-2: Submenu for format drive

The following can be selected from the format submenu:

- Selecting *F* will format the drive and a new configuration table with the correct parameters will be written on the disk drive.
- Selecting *G* will format the drive and the old configuration table will be written on the disk drive.
- Selecting *W* will write a new configuration table with the correct parameters on the disk drive. This entry is used when the Supermax running **SMOS** operating system.
- Selecting *S* will write a new configuration table with the correct parameters and it will clear the **SVR4 VTOC** table on the disk drive. This entry is only used when the Supermax running **SVR4** operating system.
- Selecting *R* will return to the menu for winchester test.

If selecting *F* or *G* entry and the multiple test is set to enable, the program can format all the drives, which are enabled. In order to do that the manufacturer and the type of the disk drive must be the same on all

drives.

G – Reassign block

The Reassign block command requests the drive to reassign a defective block to a spare block reserved for this purpose. If a spare block is available on the track, where the defect block is located, this block will be used, otherwise a spare block on a other track will be used. The defect block address is added to the grown defect list. It is not necessary to reformat the drive after using the reassign block command, and only one block of data is corrupted.

If the drive is reformatted it will use the grown defect list, and the primary defect list to map out all defect blocks so the media appears error free. It is possible to use either a sector address or the cylinder, head and sector number as input to the command. The parameter configuration table will be updated with the sector address. of the reassigned block. This information is not used by any programs.

I – Performance test

This command can be used to measure the performance of the disk drive. The following tests can be measured.

- Read test.
- Write test.
- Seek test.

When the test is completed the actual time used for the test is the number written on the terminal times 50 ms. If selected write performance test it will keep the configuration table, but the data on the disk drive is destroyed. All errors obtained from the drive are stored in the error buffer.

J – Read parameters from winchester

Parameters are read from the configuration table on the winchester. If the parameters are invalid they will not be used. Instead the program will use the default parameters read from the disk drive itself.

K – Exerciser

Sectors are read one by one on the selected track. When the exerciser is started it seeks to the selected track and does not read until you type *X*. After that the exerciser keeps on reading the selected track until another track is selected or you type *Y*. All errors obtained from the drive are stored in the error buffer. The following exerciser commands may be used:

Key	Command
Ctrl K	Increment head number
Ctrl J	Decrement head number
Ctrl H	Decrement cylinder number
Ctrl L	Increment cylinder number
X	Select read operation
Y	Select no read operation
R	Restore drive
Ctrl E	Exit

Table 7-4-1: Winchester exerciser commands

L – Read single sector and display

The selected sector is read into memory and displayed on the terminal. The following commands may be used:

Letter	Command	Description
R	Return	Return to menu
A	Address	Select a new disk address
S	Sector	Select a new sector address
C	Cylinder	Select a new cylinder number
D	Display	Display next part of the sector. Is used to display part of the sector that lies beyond the first 256 bytes.
N	Next	Read next sector
P	Previous	Read previous sector
M	Modify	Modify bytes in the sector[1)]
W	Write	Write current sector

Table 7-4-2: Winchester sector display commands

[1)] The modified bytes are not written on the winchester disk until a write command is issued.

S – Set command

This feature enables the user to send commands to the drive. The first byte must contain the number of command bytes transmitted to the drive.

NOTE

During normal test conditions it is **NOT** necessary to use this feature.

P – Set winchester parameters

The following parameters can be set or changed when running the different tests. Not all parameters affect all tests.

- Sector size
- Number of sectors/track
- Number of heads
- Number of cylinders
- Physical disk size
- Min. cylinder for write
- No. of sectors in write/read tests
- Disconnect/Reconnect option.

  Defaults to 0x03 which enables the D/R option. Type 0x00 in order to disable the D/R option. Disconnect/Reconnect is a feature in the SCSI interface that enables the target to free the SCSI bus during execution of a command. Consequently the DIOC3 is able to have pending commands to each device on the SCSI bus.

The *P* command will print SCSI channel, disk name, revision and if the disk is formatted with cylinder-oriented sparing, it will display number of spare sectors per cylinder.

W – Set-up of disk system

Prior to selecting this entry, all units on both SCSI interfaces must have been selected. The following submenu will be printed on the terminal:

```
Set-up of disk system
P - List overview of disk information on all disks
1 - List mirrored and striped disk information on all disks
2 - List subsystem disk and dual host information on all disks
3 - List physical disk size on all disks
E - Enable disk information
D - Disable disk information
M - Manual set-up of disk information
C - Change physical disk size
R - Return to menu
Select command:
```

Figure 7-4-3: Submenu for set-up of disk system

The following information can be disabled, enabled or changed:

- Mirrored information.
- Striped information.
- Dual host information.
- Subsystem hard disk information.
- Physical disk size.

All of this information is located in address 0x1000 – 0x10FF of all the physical winchester disks.

P – List overview of disk information on all disks

This entry will display an overview of all information available from the disks. The example shows a 3 Gbyte disk system (mirrored, striped, subsystem and dual host).

```
SCSI    Device  Mirrored        Striped         Subsystem       Dual host
CH/ID   type    information     information     information     information
0  0    Disk    OK              OK              OK              OK
1  0    Disk    OK              OK              OK              OK
0  1    Disk    OK              OK              --              OK
1  1    Disk    OK              OK              --              OK
0  2    Disk    OK              OK              --              OK
1  2    Disk    OK              OK              --              OK
0  3    Disk    OK              OK              --              OK
1  3    Disk    OK              OK              --              OK
0  4    None
1  4    None
0  5    None
1  5    None
0  6    None
1  6    Tape
Press return to continue
```

Figure 7-4-4: Display of all disk information

The following table is a description of the previous command:

Text	Description
SCSI CH/ID:	SCSI channel and SCSI ID number
Device type:	Device type (None, Disk, Tape)
Mirrored:	
OK:	Mirrored information is enabled and valid
Not valid:	Magic no. on the disks are different
Disk new:	The disk is new
Disk failed:	This disk has failed
Partner failed:	The partner disk has failed
Disk dirty:	Write not completed
Striped:	
OK:	Striped information is enabled and valid
Not valid:	The striped information is invalid
Dual host:	
OK:	Dual host information is enabled
Subsystem:	
OK:	Subsystem information is enabled and valid
– –:	Subsystem information is available from the first striped disk
Not valid:	The configuration table is not created on all subsystems
Not used:	Subsystem information is available, but ignored because information from the first striped disk is used

Table 7-4-3: Description of list overview of disk information

1 – List mirrored and striped disk information on all disks

This entry will display the mirrored and striped disk information available from all the disks. The example shows a 3 Gbyte disk system (mirrored, striped, subsystem and dual host).

```
SCSI    Mirrored information.      Striped information.
CH/ID   Magic no.   N/P/E/D/C      Magic no.   Status   Block size
0  0    0x44820201          X      0x44820201  1/4      0x020000
1  0    0x44820201          X      0x44820201  1/4      0x020000
0  1    0x44820233          X      0x44820201  2/4      0x020000
1  1    0x44820233          X      0x44820201  2/4      0x020000
0  2    0x44820180          X      0x44820201  3/4      0x020000
1  2    0x44820180          X      0x44820201  3/4      0x020000
0  3    0x44820122          X      0x44820201  4/4      0x020000
1  3    0x44820122          X      0x44820201  4/4      0x020000
Press return to continue
```

Figure 7-4-5: Display of mirrored, striped disk information

Text	Description
SCSI CH/ID:	SCSI channel and SCSI ID number
Mirrored information. Magic number: Status field:	 Magic number for the mirrored disk N – Bit(4) – The disk is new P – Bit(3) – The partner disk has failed E – Bit(2) – This disk has failed D – Bit(1) – Write not completed C – Bit(0) – Disk is OK
Striped information. Magic number: Status field: Block size:	 Magic number for the striped disks Contains disk number/amount of disks The block size for the striped disks

Table 7-4-4: Description of list mirrored, striped disk information

2 – List subsystem disk and dual host information on all disks

This entry will display the subsystem hard disk and dual hosted information available from all the disks. The example shows a 3 Gbyte disk system (mirrored, striped, subsystem and dual host).

```
SCSI   Dual host information.     Subsystem information.
CH/ID  DIOC Owner  DIOC SCSI      Number  Offset (kb)  Length (kb)
0  0   Unit E      ID 5           0       0x00000000   0x00050400
                                  1       0x00050408   0x00050400
1  0   Unit E      ID 5           0       0x00000000   0x00050400
                                  1       0x00050408   0x00050400
0  1   Unit E      ID 5
1  1   Unit E      ID 5
0  2   Unit E      ID 5
1  2   Unit E      ID 5
0  3   Unit E      ID 5
1  3   Unit E      ID 5
Press return to continue
```

Figure 7-4-6: Display of the subsystem hard disk, dual hosted information

Text	Description
SCSI CH/ID:	SCSI number and SCSI ID number
Dual host information.	
DIOC Owner:	The unit number of the DIOC3 that owns the disk
DIOC SCSI:	The SCSI ID of the DIOC3 holding the odd unit number
Subsystem information.	
Number:	Subsystem number (0-3)
Offset (kb):	The physical disk address, on where the subsystem starts
Length (kb):	The length of the subsystem

Table 7-4-5: Description of list subsystem, dual hosted disk information

3 – List physical disk size on all disks

This command will list the disk size information available from all the disks. The example shows a 3 Gbyte disk system (mirrored, striped, subsystem and dual host).

```
SCSI    Actual        Physical      Subsystem disk        Striped disk system
CH/ID   disk size     disk size     No. Disk size         Number  System size
0  0    0643 Mbyte    1284 Mbyte    0   1284 Mbyte
                      1284 Mbyte    1   1284 Mbyte        4 disks 2568 Mbyte
1  0    0643 Mbyte    1284 Mbyte    0   1284 Mbyte
                      1284 Mbyte    1   1284 Mbyte        4 disks 2568 Mbyte
0  1    0643 Mbyte    0643 Mbyte
1  1    0643 Mbyte    0643 Mbyte
0  2    0643 Mbyte    0643 Mbyte
1  2    0643 Mbyte    0643 Mbyte
0  3    0643 Mbyte    0643 Mbyte
1  3    0643 Mbyte    0643 Mbyte
Press return to continue
```

Figure 7-4-7: Display of disk size information

The following table is a description of the previous command:

Text	Description
SCSI CH/ID:	SCSI channel and SCSI ID number
Actual disk size:	This is a calculated maximum size for the physical hard disk
Physical disk size:	The physical disk size is taken from the configuration table on the disk
Subsystem disk. No: Disk size:	 Number of the subsystem Length of the subsystem. If the subsystem is a striped disk system the length is calculated from the subsystem length field on the first disk multiplied with the number of disks used in the striped disk system
Striped disk. Number: System size:	 Number of disks used in the striped disk system This is the calculated size of the disk system

Table 7-4-6: Description of list physical disk size

E – Enable disk information

This entry will enable (initialize) information to the disk(s). The program will guide you through the procedure by asking you about the information, that it needs.
If you select mirrored information you will only need to enter the ID number of one disk and both mirrored disks will automatically be selected.
If you select striped information you will only need to enter the SCSI channel and ID number of the first disk and the SCSI ID numbers **ID** to **ID** + 3 will automatically be selected.

The following describes the necessary information, depending upon the selected information type.

- **Mirrored information**

  The program will ask for the magic number and the type of installation for the two mirrored disks. The program will automatically set mirrored status field.

- **Striped information**

  The program will ask for the magic number. The program will automatically set an amount of 4 disks and a block size of 0x20000.

- **Dual hosted disk information**

  The program will ask for the unit number of the disk owner. The program will automatically set SCSI ID of the DIOC3 holding the odd unit number to ID 5.

- **Subsystem hard disk information**

  The program will ask for the size of the subsystems on a disk. The program will automatically calculate the offset and length of all the subsystems.

D – Disable disk information

This entry will disable information from the disk(s). The program will guide you through the procedure by asking you about the information, that it needs.
If you select mirrored information you will only need to enter the ID number of one disk and both mirrored disks will automatically be selected.
If you select striped information you will only need to enter the SCSI channel and ID number of the first disk and the SCSI ID numbers **ID** to **ID** + 3 will automatically be selected.

M – Manual set-up of disk information

This entry is used to manually set-up the disk information on one winchester. The following information must be entered:

- The type of information you want to set-up.
- SCSI channel and ID number of the disk you want to save the information on.
- Information depending upon the selected information type.

The following describes the necessary information, depending upon the selected information type.

- **Mirrored information**

  The program will ask if the information is to be disabled or enabled. If you want to enable the information, you must enter the magic number and the status of the mirrored disk.

- **Striped information**

  The program will ask if the information is to be disabled or enabled. If you want to enable the information, you must enter the magic number, the disk number/amount of disks and the block size.

- **Dual hosted disk information**

  The program will ask if the information is to be disabled or enabled. If you want to enable the information, you must enter SCSI ID of the DIOC3 holding the odd unit number and the unit number of the DIOC3 that owns the disk.

- **Subsystem hard disk information**

  The program will ask if the information is to be disabled or enabled. If you want to enable the information, you must enter subsystem number, offset to the subsystem and length of the subsystem, for each subsystem.

C – Change physical disk size

This entry is used to change the physical disk size located in address 0x300 of the configuration table on the disk(s). The program will ask about SCSI channel and ID number of the disk, and ask if the mirrored disk should be changed also and ask about the physical disk size.

Change physical disk size on a disk must be done, when one of the following conditions are true:

- **Disable or enable striped information.**

  When you disable the striped information on the disks, the physical disk size must be set to the actual size of the disk. If you enable the striped information, the physical disk size must be set to 4 times the actual size of the disks. The physical disk size is located in the configuration table of the first disk in a disk system.

- **Disable or enable subsystem disk information or after a write test on the disk with subsystem enabled.**

  When you disable the subsystem disk information on the disks, the physical disk size must be set to the actual size of the disk. If you enable, the physical disk size must be set on each subsystems. The program will ask for the physical disk size on each subsystem. If the configuration table is not located on the subsystem offset on the hard disk, the program will create a configuration table on the hard disk, located on the subsystem offset. The physical disk size is the length of the subsystem. If the disk is a striped disk system the size is multiplied with the number of disks used in the striped disk system.
  The physical disk size is located in the configuration table. If striped disks are enabled, the physical disk size is only used on the first ID number in a disk system.

R – Return to menu

Return to the menu for winchester test.

E – Display error buffer

All errors obtained from the disk drive during one or more tests are displayed. The error buffer is cleared every time one of these tests are selected from the menu. If a test is selected to be repeated the error buffer will only be cleared before the first pass. The maximum number of errors in the error buffer are 128. If this number is exceeded an overrun is detected, and the first 127 errors are saved. Any additional errors will replace each other at location 128. Information from the error buffer is:

Name	Description
SCSI	SCSI channel number.
ID	Drive number 0 – 6.
Com	SCSI standard command. 0x00 means Test unit ready 0x03 means Request sense 0x04 means Format 0x07 means Reassign 0x08 means Read 0x0A means Write 0x0B means Seek 0x12 means Inquiry 0x15 means Mode select 0x1A means Mode sense
Error	Error code in hex form reported from the drive.
Cylinder	Cylinder address (only if address valid).
Head	Head address (only if address valid).
Sector	Sector address (only if address valid).
Pass	The pass in which the error occurred.
Time from reset	The time from reset, when the error occurred.

Table 7-4-7: Winchester error buffer

N – Select new winchester

This is used to select another drive on one of the SCSI interfaces. You will be asked about SCSI channel number and ID number.

T – Enable test of all winchester units

This is used to tell the program to test all winchester units connected to both SCSI interfaces. When selecting this one for the first time a *M* will appear in the prompt indicating that multiple test is enabled. When selecting any of the tests A, B, C, D, F, H or I now, that test will be performed on all winchesters which have had their parameters read by the program. The test starts on SCSI 0 ID 0 and ends on SCSI 1 ID 6. If the Disconnect/Reconnect option is enabled the test will run simultaneously on all disks. Any errors obtained from the test will be saved in each units own error buffer. If selecting *T* again the *M* will disappear from the prompt indicating that multiple test is disabled.

Z – Reset SCSI interface

A reset will be performed on the SCSI interface currently in use.

R – Return to main menu

Return to the menu of peripheral units.

M – Menu

Display the menu on the terminal. If *J* has been selected the first two lines of the menu will tell about the selected winchester drive.

Embedded controller

The SCSI controller is embedded in the drive electronics. The controller is able to handle media defects. When the drive is formatted it uses two different sets of defect information:

- **Primary defect list.** This list is supplied by the manufacturer and is resident on the drive.
- **Grown defect list.** This list contains defects, which have been identified to the drive using the reassign block command.

Normally the drive is formatted using both lists, but it is possible to clear the grown defect list during the format procedure. If a hard error occurs during operation, you must use the reassign block command. It is **NOT** necessary to format the drive after using the reassign block command.

Disk drives are formatted in three different ways:

- **Track-oriented sparing.**

  One spare sector is located on each track. If a bad sector is found on a track and the sector is reassigned, the spare sector on that track will be used. The following equations are used to calculate between sector address and head, cylinder and sector numbers.

$$sec = sec\_add \text{ MOD } sec\_no$$

$$head = \text{INT}\left[\frac{sec\_add}{sec\_no}\right] \text{ MOD } head\_no$$

$$cyl = \text{INT}\left[\frac{\left[\frac{sec\_add}{sec\_no}\right]}{head\_no}\right]$$

$$sec\_add = sec + head \times sec\_no + cyl \times head\_no \times sec\_no$$

- **Cylinder-oriented sparing.**
  Spare sectors are located on the last track on each cylinder. If a bad sector is found on a cylinder and the sector is reassigned, one of the spare sectors on that cylinder will be used.
  The following equations are used to calculate between sector address and head, cylinder and sector numbers.

$$tmp = sec\_add + \mathrm{INT}\left[\frac{sec\_add}{head\_no \times sec\_no - spar\_no}\right] \times spar\_no$$

$$sec = tmp \ \mathrm{MOD} \ sec\_no$$

$$head = \mathrm{INT}\left[\frac{tmp}{sec\_no}\right] \ \mathrm{MOD} \ head\_no$$

$$cyl = \mathrm{INT}\left[\frac{\left[\frac{tmp}{sec\_no}\right]}{head\_no}\right]$$

$$sec\_add = sec + head \times sec\_no + cyl \times head\_no \times sec\_no - cyl \times spar\_no$$

- **Cylinder-oriented sparing with Multi Zone Recording**
  Some disk drives use Multi Zone Recording (MZR). These disk drives have greater capacity and a faster data rate. A disk drive has typically 8 zones on the disk.
  In each zone, the number of sectors per track is the same. In different zones, the number of sectors per track are different. The highest number of sectors per track is in the first zone, located on the outermost tracks on the disk. The lowest number of sectors per track is in the last zone, located on the innermost tracks on the disk.
  Spare sectors are located on the last track on each cylinder. If a bad sector is found on a cylinder and the sector is reassigned, one of the spare sectors on that cylinder will be used.

NOTE When running test on Multi Zone Recording winchester disks, the program will not calculate physical cylinder, head and sector position correctly.

sec_add --> sector address on the disk.
sec_no --> number of sectors per track
head_no --> number of data heads
spar_no --> number of spare sectors per cylinder

Internal error codes

During execution of an SCSI command the SCSI controller goes through different phases. If the controller enters an unexpected phase it is considered an error and the test is terminated. The following error codes are not included in the standard SCSI command format, but are internally generated error codes. If any of those errors are encountered a reset SCSI command must be performed.

Error code	Description
0x00 – 0x0F	Time out in handshake between SCSI controller and drive.
0x10 – 0x1F	Wrong interrupt (Only when Disconnect/Reconnect enabled)
0x80 – 0x8F	Illegal interrupt.
0xA0 – 0xAF	Illegal interrupt.

Table 7-4-8: SCSI internal generated error codes

Configuration table

The configuration table is located in the first 5 kbyte from address 0x0000 to 0x13FF on the winchester disk drive. It contains information about the physical parameters of the drive and information used by the Diagnostic Programs and information used by the **Supermax Operating System**.

Address	Content
0x0000-0x02FF	This address space is used by the Diagnostic Programs, and contains information about the physical parameters of the drive, and block addresses on blocks, that have been reassigned.
0x0300-0x03FF	This address space is used by the **Supermax Operating System**, and describes the configuration of a winchester disk.
0x0400-0x05FF	This address space is used by the Diagnostic Programs to save status about the Non-Operator tests.
0x1000-0x10FF	Address space used by the **Supermax Operating System** describing the information configuration table.

Table 7-4-9: Winchester configuration table

Parameter configuration table

This address space is used by the Diagnostic Programs, and contains information about the physical parameters of the drive, and block addresses on blocks that have been reassigned.

Address	Content
0x000-0x03F	Not used.
0x040	Number of heads.
0x041	MSB of number of cylinders.
0x042	LSB of number of cylinders.
0x043	Number of sectors on a track.
0x044	Interleave factor.
0x045	Hard sector flag. Must contain 0xFF.
0x046-0x047	Not used
0x048	0x00 – Track sparing Others – Cylinder sparing. Number of sectors per cylinder.
0x049-0x04E	Not used
0x04F	Controller type. Must contain 0x09.
0x050	Sector size. This number times 256 bytes is the sector size.
0x051-0x0EF	Not used
0x0F0-0x0FF	Serial number
0x100-0x2FF	This address space contains block addresses on blocks that have been reassigned. The block address consists of 4 bytes MSB...LSB. MSB is always 00.

Table 7-4-10: Parameter configuration table

Disk configuration table

This address space is used by the operating system, and describes the physical disk size, each logical disk and the boot pointers.

```
      0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
300   03 F4 00 00 01 10 00 00 00 A0 00 00 00 A0 00 00  ......... ... ..
310   00 10 00 00 00 04 00 00 00 00 00 00 00 00 00 00  ................
320   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
330   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
340   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
350   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
360   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
370   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
380   00 00 00 00 73 75 62 64 69 73 6B 32 20 70 72 65  ....subdisk2 pre
390   73 65 6E 74 FF FF FF FF FF FF FF FF FF FF FF FF  sent............
3A0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ................
3B0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ................
3C0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ................
3D0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ................
3E0   02 50 00 00 02 60 00 00 FF FF FF FF FF FF FF FF  .P...'..........
3F0   FF FF FF FF FF FF FF FF 02 50 00 00 02 50 00 00  .........P...P..
```

Figure 7-4-8: Disk configuration table

Address	Content
0x300-0x303	Four bytes containing the hexadecimal value of the physical disk size, in this example a 63 Mb disk.
0x304-0x383	32 times four bytes containing the size of each logical disk on the physical disk. The maximum number of logical disks on a physical disk is 32. In this example there are 5 logical disks, 17Mb, 10Mb, 10Mb, 1Mb and 0.25Mb. Please note that a logical disk size set to 0, indicates that the logical disk is not used.
0x384-0x393	This text string indicates to the operating system that the sector is valid.
0x394-0x3DB	Not used.
0x3DC-0x3DF	Reserved.
0x3E0-0x3EF	Four times four bytes used for boot pointers 0 through 3. Each pointer contains the hexadecimal address on the winchester disk, where the boot information is found. Normally pointer 0 points to the **Supermax Operating System** and pointer 1 points to the Diagnostic Programs. 0xFFFFFFFF indicates that the pointer is not used.
0x3F0-0x3F7	Not used.
0x3F8-0x3FB	This is a temporary pointer used by the Diagnostic Programs.
0x3FC-0x3FF	This is the actual boot pointer used by the boot prom on the DIOC. This is the address on the winchester disk from where to load the system.

Table 7-4-11: Disk configuration table

Information configuration table

The information configuration table is used when booting the operating system. The information configuration table on the winchester disks must contain information about the validity of the following information:

- Mirrored disk system.
- Striped disk system.
- Dual hosted disk system.
- Subsystem hard disk.

NOTE When a winchester disk is removed from the Supermax, delete all information in the information configuration table.

All of this information is located in address 0x1000 – 0x10FF of all the physical winchester disks.

```
      0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
1000  4D 49 52 4F 7F 32 61 4F 00 00 00 01 00 00 00 00  MIRO 2aO........
1010  53 54 52 50 7F 32 61 4F 00 00 00 41 00 02 00 00  STRP 2aO...A....
1020  44 55 41 4C 00 00 00 05 00 00 00 0E 00 00 00 00  DUAL............
1030  53 55 42 53 00 00 00 00 00 00 00 00 00 05 04 00  SUBS............
1040  53 55 42 53 00 00 00 01 00 05 04 08 00 05 04 00  SUBS............
1050  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
1060  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
```

Figure 7-4-9: Information configuration table

Mirrored disk system

The purpose of mirrored disks is to keep the Supermax computer running, even if a disk fails. The two disks in a mirrored disk system must have the same ID number and must be installed on one DIOC3, one on each SCSI interface. The two disks must have the same sector size. The following table shows the information about mirrored disks:

Address	Content
0x1000-0x1003	Four bytes containing the ascii equivalent of "MIRO", 0x4D49524F.
0x1004-0x1007	Contains a magic number, which must be the same on the two mirrored disks.
0x1008-0x100B	This is the status field for the mirrored disk. Note that more than one bit can be set. 0x00000010 (Bit 4) The disk is new. 0x00000008 (Bit 3) The partner disk has failed. 0x00000004 (Bit 2) This disk has failed. 0x00000002 (Bit 1) Write not completed. 0x00000001 (Bit 0) Disk is OK.
0x100C-0x100F	Reserved for future use. Must be 0x00000000.

Table 7-4-12: Mirrored disks

Striped disk system

The purpose of a striped disk system is to combine a number of hard disks into 1 large partition. The disks in a striped disk system must have consecutive ID numbers and must be installed on the same SCSI interface. The following table shows the information about striped disks:

Address	Content
0x1010-0x1013	Four bytes containing the ascii equivalent of "STRP", 0x53545250.
0x1014-0x1017	Contains a magic number, which must be the same on all disks in the striped disk system.
0x1018-0x101B	This is the status field for the striped disk. Bit(7-4) indicates the amount of disks in the striped disk system. Bit(3-0) indicates the number of the disk in the striped disk system.
0x101C-0x101F	Four bytes containing the block size of the striped disk system. This number must be the same on all disks.

Table 7-4-13: Striped disks

NOTE When you disable or enable the striped information on the disks, it is necessary to change the physical disk size in the disk configuration table. The configuration table is located on the first ID number in a disk system. In order to change the physical disk size, use the *C* command in the submenu "Set-up of disk system".

Dual host disk system

The purpose of dual hosted disks is to use two Supermax computers as a fault tolerant system. The two DIOC3's that are connected to a dual hosted disk system must be configured with different unit numbers, one unit number must be even and the other odd. The following table shows the information about a dual hosted system:

Address	Content
0x1020-0x1023	Four bytes containing the ascii equivalent of "DUAL", 0x4455414C.
0x1024-0x1027	Four bytes containing the SCSI ID of the DIOC3 holding the odd unit number (0-6).
0x1028-0x102B	Four bytes containing the unit number of the DIOC3 that owns the disk (0x8-0xf).
0x102C-0x102F	Reserved for future use. Must be 0x00000000.

Table 7-4-14: Dual hosted disk

NOTE

Dual host information must be on all disks connected to the SCSI interface, even if the disk is a mirrored or striped system.

Subsystem hard disk

The purpose of subsystem hard disk is to spilt a large (more than 2 Gbyte) disk system into smaller disk systems. The problem with large disk systems is that the 32 bit address becomes negative when passing the 2 Gbyte limit. Up to four subsystems can be created on one hard disk. The following table shows the information about subsystem hard disk:

Address [1]	Content
0x1030-0x1033	Four bytes containing the ascii equivalent of "SUBS", 0x53554253.
0x1034-0x1037	Four bytes containing the subsystem number (0-3).
0x1038-0x103B	The disk address, on where the subsystem starts. The disk address is in kbytes. Because of 8 kbytes reserved for the configuration table this number is 8 greater than the length of the subsystem.
0x103C-0x103F	Length of the subsystem on each physical disk. The length is in kbytes.

Table 7-4-15: Subsystem hard disk information

[1] For each subsystem, create subsystem information in the configuration table from 0x1030 to 0x106F.

NOTE

When you have made this information, it is necessary to make the information about physical and logical disk sizes in the disk configuration table on all subsystems, where the offset is different from zero. The configuration table is accessed on the offset address. In order to make the configuration table, use the *C* command in the submenu "Set-up of disk system". If you run a write test on the disk, the disk configuration table on all the subsystems (with offset different from zero) are destroyed. Remember to make the disk configuration table again.

8 PERIPHERAL PARAMETER AND ERROR CODES

Peripheral parameter and error codes

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PERIPHERAL PARAMETER AND ERROR CODES

Error code for SCSI drives

On the following pages error codes belonging to the different SCSI controllers used on the Supermax are shown.

Error code	Description
0x00	No error detected (command completed OK).
0x01	No index detected from disk drive.
0x02	No seek complete from disk drive.
0x03	Write fault from disk drive.
0x04	Drive not ready after it was selected.
0x05	Not used.
0x06	Track 00 not found.
0x07 – 0x0F	Not used.
0x10	ID field read error.
0x11	Uncorrectable data error.
0x12	Address mark not found.
0x13	Not used.
0x14	Target sector not found.
0x15	Seek error.
0x16 – 0x17	Not used.
0x18	Correctable data error.
0x19	Bad track flag detected.
0x1A	Format error.
0x1B – 0x1F	Not used.
0x20	Invalid command.
0x21	Illegal disk address.
0x22 – 0x2F	Not used.
0x30	Ram diagnostic failure.
0x31	Program memory checksum error.
0x32	ECC diagnostic failure.
0x33 – 0x3F	Not used.

Table 8-1-1. Error codes for XEBEC S1410

Error code	Description
0x00	No error.
0x01	No index from drive.
0x02	No seek complete.
0x03	Write fault.
0x04	Drive not ready.
0x05	Drive not selected.
0x06	Return to zero not successful.
0x07	Multiple drives selected.
0x08 – 0x09	Not used.
0x0A	Drive fault.
0x0B	No data transition received from 9410 drives.
0x0C – 0x0F	Not used.
0x10	ID read error. ECC error in ID field.
0x11	Uncorrectable data error.
0x12 – 0x13	Not used.
0x14	Record not found.
0x15	Seek error.
0x16	Not used.
0x17	Write protected sector.
0x18	Correctable data error.
0x19	Bad sector found.
0x1A	Track format error.
0x1B	Not used.
0x1C	Unable to read the alternate track address.
0x1D – 0x1F	Not used.
0x20	Invalid command.
0x21	Illegal disk address.
0x22	Invalid function for the present drive type.
0x23 – 0x2F	Not used.
0x30	Ram error.
0x31 – 0x3F	Not used.

Table 8-1-2: Error codes for DTC 610

Error code	Description
0x00	No sense.
0x01	No index signal.
0x02	No seek complete.
0x03	Write fault.
0x04	Drive not ready.
0x05	Not used.
0x06	Track 00 not found.
0x07 – 0x0F	Not used.
0x10	ID CRC error.
0x11	Uncorrectable data error.
0x12	ID address mark not found.
0x13	Data address mark not found.
0x14	Record not found.
0x15	Seek error.
0x16 – 0x17	Not used.
0x18	Data check in no retry mode.
0x19	ECC error during verify.
0x1A	Interleave error.
0x1B	Not used.
0x1C	Unformatted or bad format on drive.
0x1D	Self test failed.
0x1E	Defective track (media errors).
0x1F	Not used.
0x20	Invalid command.
0x21	Illegal block address.
0x22	Not used.
0x23	Volume overflow.
0x24	Bad argument.
0x25	Invalid logical unit number.
0x26 – 0x3F	Not used.

Table 8-1-3: Error codes for ADAPTEC ACB 4000

Error code	Description
0x00	No error detected (command completed OK).
0x01	No index detected from disk drive.
0x02	No seek complete from disk drive.
0x03	Write fault from disk drive.
0x04	Drive not ready after it was selected.
0x05	Drive not select.
0x06	Seek error from drive.
0x07	Drive write protected.
0x08	Disk drive still seeking.
0x09	Drive busy.
0x0A	Drive not initialized.
0x0B	Time out error.
0x0C	Set wrong sector # per track on drive.
0x0D – 0x0F	Not used.
0x10	Sector ECC error.
0x11	Uncorrectable data error.
0x12 – 0x13	Not used.
0x14	Target sector not found.
0x15	Seek error.
0x16	Data miscompare error.
0x17	Not used.
0x18	Correctable data error.
0x19	Bad track flag detected.
0x1A – 0x1B	Not used.
0x1C	Direct access to alternate track.
0x1D	Alternate track already assigned.
0x1E	Assigned alternate track not found.
0x1F	Alternate and defective track point to the same.

Table 8-1-4: Error codes for XEBEC S1490 (SMD) (1 of 2)

Error code	Description
0x20	Invalid command.
0x21	Illegal disk address.
0x22	Illegal parameter on initialize format command.
0x23 – 0x2F	Not used.
0x30	Ram diagnostic failure.
0x31	Program memory checksum error.
0x32	ECC diagnostic failure.
0x33 – 0x3F	Not used.

Table 8-1-4: Error codes for XEBEC S1490 (SMD) (2 of 2)

Error code	Description
0x00	No error detected (command completed OK).
0x01	No index detected from disk drive.
0x02	No seek complete from disk drive.
0x03	Fault.
0x04	Drive not ready.
0x05	Drive not select.
0x06	Not used.
0x07	Multiple drive selected.
0x08 – 0x0B	Not used.
0x0C	Drive is write protected.
0x0D	Seek in progress.
0x0E – 0x0F	Not used.
0x10	ID read error.
0x11	Uncorrectable data error during read.
0x12 – 0x13	Not used.
0x14	Record not found.
0x15	Seek error.
0x16	No valid alternate sector found.
0x17	Not used.
0x18	Correctable data field error.
0x19	Bad block found.
0x1A	Format error.
0x1B – 0x1E	Not used.
0x1F	Time out or handshake error.
0x20	Invalid command.
0x21	Illegal disk address.
0x22 – 0x2F	Not used.
0x30 – 0x3F	Not used.

Table 8-1-5: Error codes for NEC DS800B (SMD)

Error code	Description
0x00	No sense.
0x01	No index signal.
0x02	No seek complete.
0x03	Write fault.
0x04	Drive not ready.
0x05	Selection failure.
0x06 – 0x0F	Not used.
0x10	ID CRC error.
0x11	Uncorrectable data error.
0x12	ID address mark not found.
0x13 – 0x14	Not used.
0x15	Seek error.
0x16 – 0x17	Not used.
0x18	Data check in no retry mode.
0x19	ECC error during verify.
0x1A – 0x1B	Not used.
0x1C	Unformatted or bad format on drive.
0x1D – 0x1F	Not used.
0x20	Invalid command.
0x21	Illegal block address.
0x22	Not used.
0x23	Volume overflow.
0x24	Bad argument.
0x25	Invalid logical unit number.
0x26	Not used.
0x27	Write protect.
0x28	Cartridge changed.
0x29	Media error.

Table 8-1-6: Error codes for ADAPTEC ACB 5580 (1 of 2)

Error code	Description
0x2A	Not used.
0x2B	Set limit violation.
0x2C	Error count overflow.
0x2D	SCSI initiator detected error.
0x2E	SCSI bus out parity check.
0x2F	ADAPTER parity check.

Table 8-1-6: Error codes for ADAPTEC ACB 5580 (2 of 2)

Error code	Description
0x00	No sense.
0x01	No index/sector signal.
0x02	No seek complete.
0x03	Write fault.
0x04	Drive not ready.
0x05	Selection failure.
0x06	No track zero found.
0x07	Multiple drives selected.
0x08	Logical unit communication failure.
0x09	Track following error.
0x0A – 0x0E	Not used.
0x0F	Data compare error, generated by the Diagnostic Program
0x10	ID CRC/ECC error.
0x11	Uncorrectable data error.
0x12	No address mark found in ID field.
0x13	No address mark found in data field.
0x14	No record found.
0x15	Seek error.
0x16	Data synchronization mark error.
0x17	Recovered read data with retries (without ECC).
0x18	Recovered read data with ECC.(without retries).
0x19	Defect list error.
0x1A	Parameter overrun.
0x1B	Synchronous transfer error.
0x1C	Primary defect list not found.
0x1D	Compare error.
0x1E	Recovered ID with ECC correction.
0x1F	Not used
0x20	Invalid command.

Table 8-1-7: Error codes for EMBEDDED CONTROLLERS (1 of 2)

Error code	Description
0x21	Illegal block address.
0x22	Illegal function for device type.
0x23	Not used.
0x24	Illegal field in CDB.
0x25	Invalid logical unit number.
0x26	Invalid field in parameter list.
0x27	Write protect.
0x28	Cartridge changed.
0x29	Power on, reset, or bus device reset.
0x2A	Mode select parameters changed.
0x2B – 0x2F	Not used.
0x30	Incompatible cartridge.
0x31	Medium format corrupted.
0x32	No defect spare location available.
0x33 – 0x3F	Not used.
0x40	Ram failure.
0x41	Data path diagnostic failure.
0x42	Power on diagnostic failure.
0x43	Message reject error.
0x44	Internal controller error.
0x45	Select/reselect failed.
0x46	Unsuccessful soft reset.
0x47	SCSI interface parity error.
0x48	Initiator detected error.
0x49	Illegal message.
0x4A – 0x8F	Not used.

Table 8-1-7: Error codes for EMBEDDED CONTROLLERS (2 of 2)

Error code	Description
0x00	No sense
0x01	Recovered error
0x02	Not ready
0x03	Medium error
0x04	Hardware error
0x05	Illegal request
0x06	Unit attention
0x07	Data protect
0x08	Blank check
0x09	Vendor unique (not used)
0x0A	Copy aborted
0x0B	Aborted command
0x0C	Reserved
0x0D	Volume overflow
0x0E	Not used
0x0F	Data compare error, generated by the Diagnostic Program

Table 8-1-8: Error codes for CIPHER ½" Magtape

Error code	Description
0x00	No sense
0x01	Not used
0x02	Not ready
0x03	Medium error
0x04	Hardware error
0x05	Illegal request
0x06	Unit attention
0x07	Data protect
0x08	Blank check
0x09	Vendor unique (not used)
0x0A	Copy aborted
0x0B	Aborted command
0x0C	Reserved
0x0D	Volume overflow
0x0E	Not used
0x0F	Data compare error, generated by the Diagnostic Program

Table 8-1-9: Error codes for TAPE AND VIDEO DRIVES

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PERIPHERAL PARAMETER AND ERROR CODES

Winchester drive parameters

On the following pages you will find a list of disk drive parameters for all winchester disk drives, that might be used in a Supermax computer.

The parameters depend on both the DIOC and the controller.

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	4	4
Cylinders	320	320
Sectors	33	32
Reduced Write Current	not used	not used
Precompensation	128	128
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x9C0000	0x9C0000
Max number of skip	31	31

DIOC2	ADAPTEC ACB 4000	
Heads	4	
Cylinders	320	
Sectors	32	
Reduced Write Current	not used	
Precompensation	128	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x9C0000	
Max number of skip	31	

Table 8-2-1: Drive parameters for NEC D5224 (10Mb)

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	4	4
Cylinders	320	320
Sectors	33	32
Reduced Write Current	132	132
Precompensation	0	0
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x9C0000	0x9C0000
Max number of skip	31	31

DIOC2	ADAPTEC ACB 4000	
Heads	4	
Cylinders	320	
Sectors	32	
Reduced Write Current	132	
Precompensation	0	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x9C0000	
Max number of skip	31	

Table 8-2-2: Drive parameters for RODIME RO 202 (10Mb)

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	8	8
Cylinders	320	320
Sectors	33	32
Reduced Write Current	not used	not used
Precompensation	128	128
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x12F0000	0x12F0000
Max number of skip	31	31

DIOC2	ADAPTEC ACB 4000	
Heads	8	
Cylinders	320	
Sectors	32	
Reduced Write Current	not used	
Precompensation	128	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x12F0000	
Max number of skip	31	

Table 8-2-3: Drive parameters for FUJITSU M2235 (20Mb)

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	8	8
Cylinders	320	320
Sectors	33	32
Reduced Write Current	not used	not used
Precompensation	128	128
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x12F0000	0x12F0000
Max number of skip	31	31

DIOC2	ADAPTEC ACB 4000	
Heads	8	
Cylinders	320	
Sectors	32	
Reduced Write Current	not used	
Precompensation	128	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x12F0000	
Max number of skip	31	

Table 8-2-4: Drive parameters for NEC D5244 (20Mb)

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	4	4
Cylinders	640	640
Sectors	33	32
Reduced Write Current	not used	not used
Precompensation	128	128
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x12F0000	0x12F0000
Max number of skip	31	31

DIOC2	ADAPTEC ACB 4000	
Heads	4	
Cylinders	640	
Sectors	32	
Reduced Write Current	not used	
Precompensation	128	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x12F0000	
Max number of skip	31	

Table 8-2-5: Drive parameters for NEC D5126 (20Mb)

DIOC1	DTC 610	
Heads	4	
Cylinders	605	
Sectors	42	
Control byte	00	
Interleave factor	5	
Physical disk size	0x1870000	
Max number of skip	31	

DIOC2	DTC 610	
Heads	4	
Cylinders	605	
Sectors	42	
Control byte	00	
Interleave factor	14	
Physical disk size	0x1870000	
Max number of skip	31	

Table 8-2-6: Drive parameters for FINCH 9410 (25Mb)

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	7	7
Cylinders	645	645
Sectors	33	32
Reduced Write Current	not used	not used
Precompensation	319	319
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x22C0000	0x22C0000
Max number of skip	64	64

DIOC2	ADAPTEC ACB 4000
Heads	7
Cylinders	645
Sectors	32
Reduced Write Current	not used
Precompensation	319
Control byte	00
Step period	02
Interleave factor	1
Physical disk size	0x22C0000
Max number of skip	64

Table 8-2-7: Drive parameters for ATASI 3046 (36Mb)

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	7	7
Cylinders	699	699
Sectors	33	32
Reduced Write Current	not used	not used
Precompensation	256	256
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x22C0000	0x22C0000
Max number of skip	64	64

DIOC2	ADAPTEC ACB 4000	
Heads	7	
Cylinders	699	
Sectors	32	
Reduced Write Current	not used	
Precompensation	256	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x22C0000	
Max number of skip	64	

Table 8-2-8: Drive parameters for HITACHI DK511-5 (36Mb)

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	10	10
Cylinders	823	823
Sectors	33	32
Reduced Write Current	not used	not used
Precompensation	823	823
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x3F40000	0x3F40000
Max number of skip	125	125

DIOC2	ADAPTEC ACB 4000	
Heads	10	
Cylinders	823	
Sectors	32	
Reduced Write Current	not used	
Precompensation	823	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x3F40000	
Max number of skip	125	

Table 8-2-9: Drive parameters for HITACHI DK511-8 (63Mb)

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	8	8
Cylinders	1024	1024
Sectors	33	32
Reduced Write Current	not used	not used
Precompensation	1024	1024
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x3F40000	0x3F40000
Max number of skip	94	94

DIOC2	ADAPTEC ACB 4000	
Heads	8	
Cylinders	1024	
Sectors	32	
Reduced Write Current	not used	
Precompensation	1024	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x3F40000	
Max number of skip	94	

Table 8-2-10: Drive parameters for MICROPOLIS 1325 (63Mb)

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	7	7
Cylinders	1166	1166
Sectors	33	32
Reduced Write Current	not used	not used
Precompensation	1166	1166
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x3F40000	0x3F40000
Max number of skip	64	64

DIOC2	ADAPTEC ACB 4000	
Heads	7	
Cylinders	1166	
Sectors	32	
Reduced Write Current	not used	
Precompensation	1166	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x3F40000	
Max number of skip	64	

Table 8-2-11: Drive parameters for VERTEX V185 (63Mb)

DIOC1	XEBEC SMD	
Heads	8	
Cylinders	1024	
Sectors	56	
ECC burst error	0	
Control byte	00	
Interleave factor	not used	
Bytes/track	5000	
Physical disk size	0x6E20000	
Max number of skip	125	

DIOC2	NEC DS 800B SMD	
Heads	8	
Cylinders	1024	
Sectors	64	
Control byte	00	
Interleave factor	1	
Physical disk size	0x7E00000	
Max number of skip	125	

Table 8-2-12: Drive parameters for NEC D2257 (120Mb)

DIOC2	ADAPTEC ACB 5580	
Heads	10	
Cylinders	1649	
Sectors	62	
Control byte	00	
Interleave factor	1	
Physical disk size	0xF690000	
Max number of skip	198	

Table 8-2-13: Drive parameters for PERTEC DX332 (240Mb)

DIOC1	ADAPTEC ACB 4000	XEBEC S1410
Heads	7	7
Cylinders	714	714
Sectors	33	32
Reduced Write Current	not used	not used
Precompensation	256	256
ECC burst error	not used	6
Control byte	00	07
Step period	02	not used
Interleave factor	2	7
Physical disk size	0x2630000	0x2630000
Max number of skip	64	64

DIOC2	ADAPTEC ACB 4000	
Heads	7	
Cylinders	714	
Sectors	32	
Reduced Write Current	not used	
Precompensation	256	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x2630000	
Max number of skip	64	

Table 8-2-14: Drive parameters for HITACHI DK511-5 (40Mb)

DIOC1	ADAPTEC ACB 4000	
Heads	8	
Cylinders	615	
Sectors	33	
Reduced Write Current	not used	
Precompensation	128	
ECC burst error	not used	
Control byte	00	
Step period	02	
Interleave factor	2	
Physical disk size	0x2630000	
Max number of skip	31	

DIOC2	ADAPTEC ACB 4000	
Heads	8	
Cylinders	615	
Sectors	32	
Reduced Write Current	not used	
Precompensation	128	
Control byte	00	
Step period	02	
Interleave factor	1	
Physical disk size	0x2630000	
Max number of skip	31	

Table 8-2-15: Drive parameters for NEC D5146H (40Mb)

DIOC2	Embedded controller
Heads	15
Cylinders	1220
Sectors	13 (1024 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0xE850000
Max number of skip	not used

DIOC3	Embedded controller
Heads	15
Cylinders	1220
Sectors	13
Bytes/sector	1024
Physical disk size	0xE850000

Table 8-2-16: Drive parameters for MAXTOR XT 3280 (240Mb)

DIOC2	Embedded controller
Heads	8
Cylinders	1015
Sectors	35 (512 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x8B20000
Max number of skip	not used

DIOC3	Embedded controller
Heads	8
Cylinders	1015
Sectors	35
Bytes/sector	512
Physical disk size	0x8B20000

Table 8-2-17: Drive parameters for MICROPOLIS 1375 (130Mb)

DIOC2	Embedded controller
Heads	9
Cylinders	967
Sectors	35 (512 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x8B20000
Max number of skip	not used

DIOC3	Embedded controller
Heads	9
Cylinders	967
Sectors	35
Bytes/sector	512
Physical disk size	0x8B20000

Table 8-2-18: Drive parameters for WREN III (130Mb)

DIOC2	Embedded controller
Heads	7
Cylinders	1210
Sectors	18 (1024 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x8B20000
Max number of skip	not used

DIOC3	Embedded controller
Heads	7
Cylinders	1210
Sectors	18
Bytes/sector	1024
Physical disk size	0x8B20000

Table 8-2-19: Drive parameters for PRIAM 717 (130Mb)

DIOC2	Embedded controller
Heads	11
Cylinders	1210
Sectors	18 (1024 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0xE850000
Max number of skip	not used

DIOC3	Embedded controller
Heads	11
Cylinders	1210
Sectors	18
Bytes/sector	1024
Physical disk size	0xE850000

Table 8-2-20: Drive parameters for PRIAM 728 (240Mb)

DIOC2	Embedded controller
Heads	15
Cylinders	1218
Sectors	18 (1024 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x14100000
Max number of skip	not used

DIOC3	Embedded controller
Heads	15
Cylinders	1218
Sectors	18
Bytes/sector	1024
Physical disk size	0x14100000

Table 8-2-21: Drive parameters for PRIAM 738 (320Mb)

DIOC2	Embedded controller
Heads	15
Cylinders	1218
Sectors	18 (1024 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x14100000
Max number of skip	not used

DIOC3	Embedded controller
Heads	15
Cylinders	1218
Sectors	18
Bytes/sector	1024
Physical disk size	0x14100000

Table 8-2-22: Drive parameters for MICROPOLIS 1578 (320Mb)

DIOC2	Embedded controller
Heads	4
Cylinders	1015
Sectors	35 (512 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x3F40000
Max number of skip	not used

DIOC3	Embedded controller
Heads	4
Cylinders	1015
Sectors	35
Bytes/sector	512
Physical disk size	0x3F40000

Table 8-2-23: Drive parameters for MICROPOLIS 1373 (65Mb)

DIOC2	Embedded controller
Heads	7
Cylinders	1239
Sectors	18 (1024 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x8B20000
Max number of skip	not used

DIOC3	Embedded controller
Heads	7
Cylinders	1239
Sectors	18
Bytes/sector	1024
Physical disk size	0x8B20000

Table 8-2-24: Drive parameters for MICROPOLIS 1674 (130Mb)

DIOC2	Embedded controller
Heads	15
Cylinders	1626
Sectors	27 (1024 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x28300000
Max number of skip	not used

DIOC3	Embedded controller
Heads	15
Cylinders	1626
Sectors	27
Bytes/sector	1024
Physical disk size	0x28300000

Table 8-2-25: Drive parameters for MICROPOLIS 1588 (640Mb)

DIOC2	Embedded controller
Heads	15
Cylinders	1626
Sectors	27 (1024 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x28300000
Max number of skip	not used

DIOC3	Embedded controller
Heads	15
Cylinders	1626
Sectors	27
Bytes/sector	1024
Physical disk size	0x28300000

Table 8-2-26: Drive parameters for MAXTOR XT 8760 (640Mb)

DIOC2	Embedded controller
Heads	15
Cylinders	1626
Sectors	27 (1024 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x28300000
Max number of skip	not used

DIOC3	Embedded controller
Heads	15
Cylinders	1626
Sectors	27
Bytes/sector	1024
Physical disk size	0x28300000

Table 8-2-27: Drive parameters for WREN VI (640Mb)

DIOC2	Embedded controller
Heads	7
Cylinders	1770
Sectors	27 (1024 bytes/sector)
Control byte	00
Interleave factor	1
Physical disk size	0x14100000
Max number of skip	not used

DIOC3	Embedded controller
Heads	7
Cylinders	1770
Sectors	27
Bytes/sector	1024
Physical disk size	0x14100000

Table 8-2-28: Drive parameters for MICROPOLIS 1684 (320Mb)

DIOC3	Embedded controller
Heads	15
Cylinders	2094
Sectors	44
Bytes/sector	1024
Physical disk size	0x53540000
No. of cylinder sparing	8

Table 8-2-29: Drive parameters for MICROPOLIS 1528 (1.53Gb)

DIOC3	Embedded controller
Heads	21
Cylinders	2467
Sectors	41
Bytes/sector	1024
Physical disk size	0x7FF00000
No. of cylinder sparing	11
No. of zone recording (MZR)	8

Table 8-2-30: Drive parameters for MICROPOLIS 1924 (2.4Gb)

DIOC3	Embedded controller
Heads	8
Cylinders	1728
Sectors	42
Bytes/sector	1024
Physical disk size	0x20000000
No. of cylinder sparing	4
No. of zone recording (MZR)	8

Table 8-2-31: Drive parameters for MICROPOLIS 2105 (560Mb)

NOTE

The Diagnostic program will not calculate the physical cylinder, head and sector position correctly on Multi Zone Recording (MZR) disks. The values for cylinders and sectors above are not the correct values. They are calculated values that will give the correct disk size, when used by the Diagnostic Program in calculating the disk size.

DIOC3	Embedded controller
Heads	15
Cylinders	1771
Sectors	41
Bytes/sector	1024
Physical disk size	0x3e800000
No. of cylinder sparing	8
No. of zone recording (MZR)	8

Table 8-2-32: Drive parameters for MICROPOLIS 2112 (1.2Gb)

DIOC3	Embedded controller
Heads	13
Cylinders	1975
Sectors	40
Bytes/sector	1024
Physical disk size	0x3e800000
No. of cylinder sparing	0
No. of zone recording (MZR)	8

Table 8-2-33: Drive parameters for HP C2247 (1.2Gb)

NOTE

The Diagnostic program will not calculate the physical cylinder, head and sector position correctly on Multi Zone Recording (MZR) disks. The values for cylinders and sectors above are not the correct values. They are calculated values that will give the correct disk size, when used by the Diagnostic Program in calculating the disk size.

DIOC3	Embedded controller
Heads	7
Cylinders	1975
Sectors	40
Bytes/sector	1024
Physical disk size	0x20000000
No. of cylinder sparing	0
No. of zone recording (MZR)	8

Table 8-2-34: Drive parameters for HP C2244 (560Mb)

DIOC3	Embedded controller
Heads	19
Cylinders	2657
Sectors	42
Bytes/sector	1024
Physical disk size	0x7ff00000
No. of cylinder sparing	16
No. of zone recording (MZR)	8

Table 8-2-35: Drive parameters for Seagate 12550 (2.4Gb)

NOTE

The Diagnostic program will not calculate the physical cylinder, head and sector position correctly on Multi Zone Recording (MZR) disks. The values for cylinders and sectors above are not the correct values. They are calculated values that will give the correct disk size, when used by the Diagnostic Program in calculating the disk size.

DIOC3	Embedded controller
Heads	11
Cylinders	3454
Sectors	56
Bytes/sector	1024
Physical disk size	0x7ff00000
No. of cylinder sparing	9
No. of zone recording (MZR)	8

Table 8-2-36: Drive parameters for Seagate 32550 (2.4Gb)

DIOC3	Embedded controller
Heads	7
Cylinders	2933
Sectors	50
Bytes/sector	1024
Physical disk size	0x3e800000
No. of cylinder sparing	0
No. of zone recording (MZR)	8

Table 8-2-37: Drive parameters for HP C3323 (1,2Gb)

NOTE

The Diagnostic program will not calculate the physical cylinder, head and sector position correctly on Multi Zone Recording (MZR) disks. The values for cylinders and sectors above are not the correct values. They are calculated values that will give the correct disk size, when used by the Diagnostic Program in calculating the disk size.

DIOC3	Embedded controller
Heads	4
Cylinders	4385
Sectors	64
Bytes/sector	1024
Physical disk size	0x3e800000
No. of cylinder sparing	9
No. of zone recording (MZR)	10

Table 8-2-38: Drive parameters for IBM DFHS S1F (1.2Gb)

DIOC3	Embedded controller
Heads	8
Cylinders	4253
Sectors	64
Bytes/sector	1024
Physical disk size	0x7ff00000
No. of cylinder sparing	19
No. of zone recording (MZR)	10

Table 8-2-39: Drive parameters for IBM DFHS S2F (2.4Gb)

NOTE

The Diagnostic program will not calculate the physical cylinder, head and sector position correctly on Multi Zone Recording (MZR) disks. The values for cylinders and sectors above are not the correct values. They are calculated values that will give the correct disk size, when used by the Diagnostic Program in calculating the disk size.

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DIOC3	Embedded controller
Heads	5
Cylinders	3495
Sectors	60
Bytes/sector	1024
Physical disk size	0x3e800000
No. of cylinder sparing	0
No. of zone recording (MZR)	6

Table 8-2-42: Drive parameters for HP C3724 (1.2Gb)

DIOC3	Embedded controller
Heads	4
Cylinders	4190
Sectors	126
Bytes/sector	512
Physical disk size	0x3e800000
No. of cylinder sparing	10
No. of zone recording (MZR)	6

Table 8-2-43: Drive parameters for Seagate 31051 (1Gb)

NOTE

The Diagnostic program will not calculate the physical cylinder, head and sector position correctly on Multi Zone Recording (MZR) disks. The values for cylinders and sectors above are not the correct values. They are calculated values that will give the correct disk size, when used by the Diagnostic Program in calculating the disk size.

DIOC3	Embedded controller
Heads	10
Cylinders	3810
Sectors	64
Bytes/sector	1024
Physical disk size	1024
No. of cylinder sparing	62
No. of zone recording (MZR)	?

Table 8-2-44: Drive parameters for Seagte 32171 (2.1Gb)

DIOC3	Embedded controller
Heads	10
Cylinders	6661
Sectors	128
Bytes/sector	512
Physical disk size	0xfff00000
No. of cylinder sparing	80
No. of zone recording (MZR)	?

Table 8-2-45: Drive parameters for Seagate 34371 (4.3Gb)

NOTE

The Diagnostic program will not calculate the physical cylinder, head and sector position correctly on Multi Zone Recording (MZR) disks. The values for cylinders and sectors above are not the correct values. They are calculated values that will give the correct disk size, when used by the Diagnostic Program in calculating the disk size.

DIOC3	Embedded controller
Heads	20
Cylinders	7217
Sectors	128
Bytes/sector	512
Physical disk size	0xfff00001 (0x1fff00000)
No. of cylinder sparing	96
No. of zone recording (MZR)	?

Table 8-2-46: Drive parameters for Seagte 19171 (8.4Gb)

NOTE

The Diagnostic program will not calculate the physical cylinder, head and sector position correctly on Multi Zone Recording (MZR) disks. The values for cylinders and sectors above are not the correct values. They are calculated values that will give the correct disk size, when used by the Diagnostic Program in calculating the disk size.

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PERIPHERAL PARAMETER AND ERROR CODES

Tape drive parameters

On the following pages you will find a list of tape drive parameters for all tape drives, that might be used in a Supermax computer.

Format type	Bytes		Blocks (512 byte)	Blocks (1024 byte)
QIC – 11	0x01340000	≏ 20 Mb	0x009A00	0x004D00
QIC – 24	0x02AE0000	≏ 45 Mb	0x015700	0x00AB80
QIC – 120	0x07800000	≏ 120 Mb	0x03C000	0x01E000
QIC – 150	0x09600000	≏ 150 Mb	0x04B000	0x025800
QIC – 320	0x14000000	≏ 320 Mb	0x0A0000	0x050000
QIC – 525	0x20D00000	≏ 525 Mb	0x106800	0x083400
Video 2Gb	0x7D000000	≏ 2000 Mb	0x3E8000	0x1F4000
Video 5Gb	0x138800000	≏ 5000 Mb	0x9C4000	0x4E2000

Table 8-3-1: Size on different tape formats

Parameter	Description
Interface type	QIC – 02
Write format	QIC – 11
Read format	QIC – 11
Block size	512 Bytes
Number of blocks	Maximum 0x9a00 blocks ≙ 20Mb

Table 8-3-2: Tape parameters for ARCHIVE 3020

Parameter	Description
Interface type	QIC – 02
Write format	QIC – 11 / QIC – 24
Read format	QIC – 11 / QIC – 24
Block size	512 Bytes
Number of blocks	Maximum 0x15700 blocks ≙ 45Mb

Table 8-3-3: Tape parameters for ARCHIVE 3020L

Parameter	Description
Interface type	QIC – 02
Write format	QIC – 11 / QIC – 24
Read format	QIC – 11 / QIC – 24
Block size	512 Bytes
Number of blocks	Maximum 0x15700 blocks ≙ 45Mb

Table 8-3-4: Tape parameters for ARCHIVE 9045L

Parameter	Description
Interface type	QIC – 02
Write format	
DC600A	QIC – 24
DC300XLP	QIC – 24
Read format	
DC600A	QIC – 24
DC300XLP	QIC – 24
Block size	512 Bytes
Number of blocks	Maximum 0x15700 blocks ≙ 45Mb

Table 8-3-5: Tape parameters for ARCHIVE VIPER 2060L

Parameter	Description
Interface type	QIC – 02
Write format	
DC600A	QIC – 120
DC600XTD	QIC – 120/QIC – 150
Read format	
DC300XLP	QIC – 24
DC600A	QIC – 24/QIC – 120
DC600XTD	QIC – 24/QIC – 120/QIC – 150
Block size	512 Bytes
Number of blocks	Maximum 0x4B000 blocks ≙ 150Mb

Table 8-3-6: Tape parameters for ARCHIVE VIPER 2150L

Parameter	Description
Interface type	QIC – 02
Write format	
DC300XLP	QIC – 24
DC600A	QIC – 24
DC600XTD	QIC – 24
Read format	
DC300XLP	QIC – 11/QIC – 24
DC600A	QIC – 11/QIC – 24
DC600XTD	QIC – 11/QIC – 24
Block size	512 Bytes
Number of blocks	Maximum 0x15700 blocks ≙ 45Mb

Table 8-3-7: Tape parameters for TANDBERG 3319

Parameter	Description
Interface type	QIC – 02
Write format	
DC600XTD	QIC – 120
Read format	
DC600A	QIC – 11/QIC – 24/QIC – 120
DC600XTD	QIC – 11/QIC – 24/QIC – 120
Block size	512 Bytes
Number of blocks	Maximum 0x3C000 blocks ≙ 120Mb

Table 8-3-8: Tape parameters for TANDBERG 3320

Parameter	Description
Interface type	QIC – 02
Write format	
DC300XLP	QIC – 24
DC600A	QIC – 24
DC6150	QIC – 24
Read format	
DC300XLP	QIC – 11/QIC/-24
DC600A	QIC – 11/QIC/-24
DC6150	QIC – 11/QIC/-24
Block size	512 Bytes
Number of blocks	Maximum 0x15700 blocks ≙ 45Mb

Table 8-3-9: Tape parameters for TANDBERG 3610

Parameter	Description
Interface type	SCSI
Write format	
DC300XLP	QIC – 24
DC600A	QIC – 24
DC6150	QIC – 24
Read format	
DC300XLP	QIC – 11/QIC – 24
DC600A	QIC – 11/QIC – 24
DC6150	QIC – 11/QIC – 24
Block size	512 Bytes
Number of blocks	Maximum 0x15700 blocks ≙ 45Mb

Table 8-3-10: Tape parameters for TANDBERG 3620

Parameter	Description
Interface types	QIC – 02
Write format	
DC600A	QIC – 120
DC6150	QIC – 120
Read format	
DC300XLP	QIC – 11/QIC – 24/QIC – 120
DC600A	QIC – 11/QIC – 24/QIC – 120
DC6150	QIC – 11/QIC – 24/QIC – 120
Block size	512
Number of blocks	Maximum 0x3C000 blocks ≏ 120Mb

Table 8-3-11: Tape parameters for TANDBERG 3630

Parameter	Description
Interface type	SCSI
Write format	
DC600A	QIC – 120
DC6150	QIC – 120
Read format	
DC300XLP	QIC – 11/QIC – 24/QIC – 120
DC600A	QIC – 11/QIC – 24/QIC – 120
DC6150	QIC – 11/QIC – 24/QIC – 120
Block size	512
Number of blocks	Maximum 0x3C000 blocks ≏ 120Mb

Table 8-3-12: Tape parameters for TANDBERG 3640

Parameter	Description
Interface type	QIC – 02
Write format	
DC6150	QIC – 150
Read format	
DC300XLP	QIC – 11/QIC – 24/QIC – 120/QIC – 150
DC600A	QIC – 11/QIC – 24/QIC – 120/QIC – 150
DC6150	QIC – 11/QIC – 24/QIC – 120/QIC – 150
Block size	512
Number of blocks	Maximum 0x4B000 blocks ≙ 150Mb

Table 8-3-13: Tape parameters for TANDBERG 3650

Parameter	Description
Interface type	SCSI
Write format	
DC6150	QIC – 150
Read format	
DC300XLP	QIC – 11/QIC – 24/QIC – 120/QIC – 150
DC600A	QIC – 11/QIC – 24/QIC – 120/QIC – 150
DC6150	QIC – 11/QIC – 24/QIC – 120/QIC – 150
Block size	512
Number of blocks	Maximum 0x4B000 blocks ≙ 150Mb

Table 8-3-14: Tape parameters for TANDBERG 3660

Parameter	Description
Interface type	SCSI
Write format	
DC600A	QIC – 120
DC6150	QIC – 150
DC6320	QIC – 525
DC6525	QIC – 525
Read format	
DC600A	QIC – 24/QIC – 120/QIC – 150/QIC – 525
DC6150	QIC – 24/QIC – 120/QIC – 150/QIC – 525
DC6320	QIC – 24/QIC – 120/QIC – 150/QIC – 525
DC6525	QIC – 24/QIC – 120/QIC – 150/QIC – 525
Block size	1024
Number of blocks	Maximum 0x83400 blocks ≈ 525Mb

Table 8-3-15: Tape parameters for TANDBERG 3800

Parameter	Description
Interface type	SCSI
Write format	2000Mb
Read format	2000Mb
Block size	1024
Number of blocks	Maximum 0x1F4000 blocks ≙ 2000Mb

Table 8-3-16: Tape parameters for EXABYTE EXB-820x

Parameter	Description
Interface type	SCSI
Write format	5000Mb
Read format	2000Mb/5000Mb
Block size	1024
Number of blocks	Maximum 0x4E2000 blocks ≙ 5000Mb

Table 8-3-17: Tape parameters for EXABYTE EXB-850x

Parameter	Description
Write format	
DC600A	QIC – 120
DC6150	QIC – 150
DC6320	QIC – 525
DC6525	QIC – 525
QD9250	QIC – 2GB
Read format	
DC600A	QIC – 24/QIC – 120/QIC – 150/QIC – 525
DC6150	QIC – 24/QIC – 120/QIC – 150/QIC – 525
DC6320	QIC – 24/QIC – 120/QIC – 150/QIC – 525
DC6525	QIC – 24/QIC – 120/QIC – 150/QIC – 525
QD9250	QIC – 2GB
Block size	512
Number of blocks	Maximum 0x47E000 blocks ≈ 2300Mb

Table 8-3-18: Tape parameters for TANDBERG 4220

Parameter	Description
Interface type	SCSI
Write format	3800Mb
Read format	3800Mb
Block size	1024
Number of blocks	Maximum 0x3B6000 blocks ≈ 3800Mb

Table 8-3-19: Tape parameters for HP C1533A DAT

Parameter	Description
Interface type	SCSI
Write format	20000Mb
Read format	2000Mb/5000Mb/20000Mb
Block size	1024
Number of blocks	Maximum 0x125c000 blocks ≈ 18800Mb

Table 8-3-20: Tape parameters for EXABYTE EXB-8900

Parameter	Description
Write format	
DC600A	QIC–120
DC6150	QIC–150
DC6320	QIC–525
DC6525	QIC–525
QD9250	QIC–2GB
3M Imation	QIC–13GB
Read format	
DC600A	QIC–24/QIC–120/QIC–150/QIC–525
DC6150	QIC–24/QIC–120/QIC–150/QIC–525
DC6320	QIC–24/QIC–120/QIC–150/QIC–525
DC6525	QIC–24/QIC–120/QIC–150/QIC–525
QD9250	QIC–2GB
3M Imation	QIC–13GB
Block size	512
Number of blocks	Maximum 0x1838000 blocks ≈ 12400Mb

Table 8-3-21: Tape parameters for TANDBERG MLR1

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1 APPENDIX

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APPENDIX A

Installation guide for Non-Operator Diagnostic Programs

Introduced with the version 5.0 of the Diagnostic Programs is the **Non-Operator Mode** of the programs. This guide will show you how to install the Diagnostic Programs on the winchester disk and how to update your system in order to use the facility.

Create two logical disks on a physical winchester with an SCSI ID of 0. In most cases it will be on DIOC no. 14 channel no. 8. The first one is used for the **Supermax Operating System** and its size should be 1 Mb. The second one is used for the Diagnostic Programs and its size should be 1 Mb.

Use the utility **mkwboot** to install winchester boot on the system. Refer to the *System V Reference Manual Section 1* for a description on how to use **mkwboot**. If the two logical disks have subdisk numbers 3 and 4, the following example shows you what to do.

```
# mkwboot -b0 -a -s/dev/dsk/u14c8s3
# mkwboot -b1 -s/dev/dsk/u14c8s4
```

Normally there should be a link between

`/dev/dsk/u14c8s3` and `/dev/boot.0`

and a link between

`/dev/dsk/u14c8s4` and `/dev/boot.1`

Install the **Supermax Operating System** on `/dev/boot.0`

Insert the diskette containing the the Diagnostic Programs into the floppy disk drive and copy it to `/dev/boot.1`. If the special file `/dev/flop` points to the floppy disk in your system this example shows you one way to copy the diskette to the winchester disk.

```
# cp /dev/flop /dev/boot.1
```

Now winchester boot is installed on your system. In order to use the Diagnostic Programs some changes in **/etc/inittab** must be made. These lines might already exist in your file.

The following lines are changed or added to the existing file **/etc/inittab**.

```
f1:056:wait:/etc/led -f >/dev/console 2>&1
                        </dev/console (changed)
s0:056:wait:/etc/rc0 >/dev/console 2>&1
                        </dev/console (changed)
DP:5:wait:echo "\nDiagnostics will be started."
                        >/dev/console 2>&1 (added)
dp:5:wait:/etc/boot 1 >/dev/console 2>&1
                        < /dev/console (added)
```

In this case *init run level 5* will flash the LED's, shut down the system, change the boot pointer on the winchester disk from the **Supermax Operating System** to the Diagnostic Programs and then reset the system, which now will be booted with the Diagnostic Programs. They will run for a certain time, depending upon the configuration of your system. Upon completion the boot pointer will be changed from the Diagnostic Programs to the **Supermax Operating System** and the system will be reset, and now the **Supermax Operating System** will be restarted.

APPENDIX B

Release Note

Product name:	Supermax Diagnostic Programs
Stock number:	40030001
Version:	5.6
Date:	97.09.25
Completed by:	OK/BD

Please read this release note when you receive the package.

Package List

First Installation:

Floppy disks:

40030001 1 5¼" 560 kb diskette. Supermax Diagnostic Programs 5.6
40030001 1 3½" 1.44 Mb diskette. Supermax Diagnostic Programs 5.6

Documents:

1 Release Note (this document)
94400311 1 Diagnostic Programs for the Supermax 5.6

Installation Update:

Floppy disks:

40030001 1 5¼" 560 kb diskette. Supermax Diagnostic Programs 5.6
40030001 1 3½" 1.44 Mb diskette. Supermax Diagnostic Programs 5.6

Documents:

1 Release note (this document)
1 Update for Diagnostic Programs 5.6 (17 pages)

Label on floppy disk

```
Supermax Diagnostic Programs
Version 5.6     Date 97.07.15
Stock Number    40030001
© Dansk Data Elektronik A/S      1(1)
```

Product Features

The Diagnostic Program will test the Supermax hardware modules.

Requirements

Disk Space:

None.

Release Information

Changes since latest release:

- The DIOC3 test program supports formatting of a Seagate 19171 (8 Gbyte) winchester disk.
- The DIOC3 test program supports setup of a new configuration table, that also clears the **SVR4 VTOC** table on the disk. This is used when the Supermax is a Business Server.

Errors corrected since latest release:

- None.

Recognized errors or inconveniences:

- When a disk on a DIOC3 is configured with dual host option, only one DIOC3 is allowed to access the winchester on the SCSI cable when using the Diagnostic Programs.
- The DIOC3 test program cannot reassign blocks on PRIAM winchester. (A firmware error on the PRIAM winchester causes the error). If an error occurs on a disk and it is necessary to reassign block on the disk, then use a DIOC2 module instead to reassign the block or send the disk to DDE repair center.
- When running active bus test from DIOC3, CPU 68030, CPU R3000 and CPU R4000 modules, all modules must be in passive bus test mode. Otherwise, it is possible to cause a time-out (Bus error) on the active modules.
- When running test on Multi Zone Recording winchester disks, the program will not calculate the physical cylinder, head and sector position correctly.
- Do not run parity circuit test on MIOC4800 module, the test will fail. It is because the parity circuit is removed from the MIOC4800 module.
- Non-Operator test cannot be installed on a SVR4 platform (Business Server).
- When running HDLC submodule internal/external loop back test on a HDLC submodule with a HDLC controller (82532 version V2.2), the MIOC test program some times reports a fault "Time-out during wait for receive complete" or "Data error in received buffer". This is not actually an error and can be ignored.

Comments

This Diagnostic Programs contains versions of the programs for:

- SIOC 0300 Version 5.0
- CIOC 0900 Version 5.0
- NIOC 1600-3600 / SIOC2 3600 Version 5.0.2
- MIOC 4600 Version 5.2.2
- DIOC1 0400 Version 5.0.1
- DIOC2 1100 Version 5.0.1
- DIOC3 4000 Version 5.6
- CPU 68000 0100 Version 5.0
- CPU 68020 3400 Version 5.0
- CPU 68030 4100 Version 5.0
- CPU R3000 4500 Version 5.0.2
- CPU R4000 4700 Version 5.2.3

First Installation

Please read the user's guide prior to product installation.
Then follow the procedure described under 'Installation Guide'.

Installation Update

Please read the user's guide prior to product installation.
Then follow the procedure described under 'Installation Update Guide'.

Installation Guide

Diagnostic Programs version 5.6:

- Manual, version 5.6 included.

Installation Update Guide

In order to update your manual you should add or replace the following pages in the old manual version 5.5:

- Title page.
- Table of contents.
- Figures and tables.
- Peripheral test for DIOC3, Winchester test. Page 7-4-5 and 7-4-6
- Table of contents chapter 8.
- Peripheral parameter and error codes, Winchester drive parameters. Page 8-2-39 and 8-2-40
- Peripheral parameter and error codes, Tape drive parameters. Page 8-3-11 and 8-3-12.
- Table of contents Appendix.
- Appendix B (Release note). Pages B-1 to B-6

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Dansk Data Elektronik A/S

U P D A T I N G

Supermax

Non-Operator

Diagnostic Programs

User's Manual Version 5.1

Stock Number: 94400311

Dear customer!

You are kindly requested to ensure that this supplemental new and updated documentation containing revised and new manual pages for

Supermax Non-Operator Diagnostic Programs, Version 5.1

is properly inserted. If you have earlier received the Supermax Non-Operator Diagnostic Programs package, Version 5.0, please be sure to replace the manual pages with the enclosed pages as follows:

Remove Page:	**Replace with or insert:**	
Title page (5.0)	New title page (5.1)	Revised Mar.1993
Table of Contents (5.0)	Table of Contents (5.1)	Revised Mar.1993

Chapter 2, Non-Operator Mode

Remove Page:	**Replace with or insert:**	
Table of Contents (5.0)	Table of Contents (5.1)	Revised Mar.1993
Page 2-1-1 to 8 (5.0)	New pages 1-8 (5.1)	Revised Mar.1993
Page 2-2-31 to 36 (5.0)	New pages 31-36 (5.1)	Revised Mar.1993
Page 2-3-1 to 2 (5.0)	New Pages 1-2 (5.1)	Revised Mar.1993
Page 2-4-1 to 2 (5.0)	New Pages 1-2 (5.1)	Revised Mar.1993

Chapter 3, Supermax Modules

Remove Page:	Replace with or insert:	
Table of Contents (5.0)	Table of Contents (5.1)	Revised Mar.1993
Page 3-8-11 to 14 (5.0)	New pages 11-14 (5.1)	Revised Mar.1993
Page 3-11-21 to 22 (5.0)	New Pages 21-22 (5.1)	Revised Mar.1993
Page 3-12-1 to 14 (5.0)	New Pages 1-14 (5.1)	Revised Mar.1993

Chapter 4, Bus Test

Remove Page:	Replace with or insert:	
Table of Contents (5.0)	Table of Contents (5.1)	Revised Mar.1993
Page 4-2-7 to 10	New pages 7-10 (5.1)	Revised Mar.1993

Chapter 5, General Diagnostic Test

Remove Page:	Replace with or insert:	
Table of Contents (5.0)	Table of Contents (5.1)	Revised Mar.1993
Page 5-4-1 to 4 (5.0)	New pages 1-4 (5.1)	Revised Mar.1993

Chapter 6, Peripheral Test for DIOC1-2

Remove Page:	Replace with or insert:	
Table of Contents (5.0)	Table of Contents (5.1)	Revised Mar.1993
Page 6-2-5 to 6 (5.0)	New Pages 5-6 (5.1)	Revised Mar.1993
Page 6-4-7 to 8 (5.0)	New Pages 7-8 (5.1)	Revised Mar.1993

Chapter 7, Peripheral Test for DIOC3

Remove Page:	Replace with or insert:	
Table of Contents (5.0)	Table of Contents (5.1)	Revised Mar.1993
Page 7-2-3 to 4 (5.0)	New Pages 3-4 (5.1)	Revised Mar.1993
Page 7-3-5 to 6 (5.0)	New Pages 5-6 (5.1)	Revised Mar.1993
Page 7-4-1 to 36 (5.0)	New Pages 1-36 (5.1)	Revised Mar.1993

Chapter 8, Peripheral Parameter and Error Codes

Remove Page:	Replace with or insert:	
Table of Contents (5.0)	Table of Contents (5.1)	Revised Mar.1993
Page 8-1-9 to 14 (5.0)	New Pages 9-14 (5.1)	Revised Mar.1993
Page 8-2-17 to 18 (5.0)	New Pages 17-18 (5.1)	Revised Mar.1993
Page 8-2-31 to 32 (5.0)	New Pages 31-32 (5.1)	Revised Mar.1993
Page 8-3-1 to 2 (5.0)	New Pages 1-2 (5.1)	Revised Mar.1993
Page 8-3-7 to 8 (5.0)	New Pages 7-8 (5.1)	Revised Mar.1993

Stock no.: 94400311

NOTICE

The information in this document is subject to change without notice. Dansk Data Elektronik A/S, Denmark assumes no responsibility for any errors that may appear in this document.

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APPENDIX B

Release Note

Product name:	Supermax Diagnostic Programs
Stock number:	40030001
Version:	5.2.3
Date:	94.06.15
Completed by:	OK/BD

Please read this release note when you receive the package.

Package List

First Installation:

Floppy disks:

40030001 1 5¼" 560 kb diskette. Supermax Diagnostic Programs 5.2.3

40030001 1 3½" 1.44 Mb diskette. Supermax Diagnostic Programs 5.2.3

Documents:

1 Release Note (this document)

94400311 1 Diagnostic Programs for the Supermax 5.2.

Installation Update:

Floppy disks:

40030001 1 5¼" 560 kb diskette. Supermax Diagnostic Programs 5.2.3

40030001 1 3½" 1.44 Mb diskette. Supermax Diagnostic Programs 5.2.3

Documents:

1 Release note (this document)
1 Update for Diagnostic Programs 5.2 (17 pages)

Label on floppy disk

```
Supermax Diagnostic Programs
Version 5.2.3  Date 94.04.13
Stock Number   40030001
© Dansk Data Elektronik A/S      1(1)
```

Product Features

The Diagnostic Program will test the Supermax hardware modules.

Requirements

Disk Space:

None.

Release Information

Changes since latest release:

- The Diagnostic Program supports the MCU4700 module with the R4400SC CPU chip (MCU4700-4400/50 or MCU4700-4400/75 module).
- The Diagnostic Program supports the MIOC module with 50 MHz clock (MIOC4800). When select the *Test All* entry in the menu, the parity circuit test will not be selected, because the parity circuit is removed from the MIOC4800 module.

- The DIOC3 test program supports formatting of two new winchester disks. HP C2244 (560 Mbyte) and Seagate 12550 (2.4 Gbyte).
- When running ISDN submodule intern loop back on the MIOC, the loop back on Primary Line Interface controller is changed from digital loop back to analog loop back.

Errors corrected since latest release:

- When running Non-Operator mode from winchester disk, the result of the Non-Operator test contains a wrong module type for the R4000 CPU Supermax module.
- When running verify mirrored disks test on the DIOC3 and the status field in mirror information on a disk contains undefined information, then the test will only execute a CRC test on the disks.

Recognized errors or inconveniences:

- When a disk on a DIOC3 is configured with dual host option, only one DIOC3 is allowed to access the winchester on the SCSI cable when using the Diagnostic Programs.
- The DIOC3 test program cannot reassign blocks on PRIAM winchester. (A firmware error on the PRIAM winchester causes the error). If an error occurs on a disk and it is necessary to reassign block on the disk, then use a DIOC2 module instead to reassign the block or send the disk to DDE repair center.
- When running active bus test from DIOC3, CPU 68030, CPU R3000 and CPU R4000 modules, all modules must be in passive bus test mode. Otherwise, it is possible to cause a time-out (Bus error) on the active modules.

- When running test on Multi Zone Recording winchester disks, the program will not calculate the physical cylinder, head and sector position correctly.
- Do not run parity circuit test on MIOC4800 module, the test will fail. It is because the parity circuit is removed from the MIOC4800 module.

Comments:

This Diagnostic Programs contains versions of the programs for:

- SIOC 0300 Version 5.0
- CIOC 0900 Version 5.0
- NIOC 1600-3600 / SIOC2 3600 Version 5.0.2
- MIOC 4600 Version 5.2.2
- DIOC1 0400 Version 5.0.1
- DIOC2 1100 Version 5.0.1
- DIOC3 4000 Version 5.2
- CPU 68000 0100 Version 5.0
- CPU 68020 3400 Version 5.0
- CPU 68030 4100 Version 5.0
- CPU R3000 4500 Version 5.0.2
- CPU R4000 4700 Version 5.2.3

First Installation

Please read the user's guide prior to product installation.
Then follow the procedure described under 'Installation Guide'.

Installation Update

Please read the user's guide prior to product installation.
Then follow the procedure described under 'Installation Update Guide'.

Installation Guide

Diagnostic Programs version 5.2.3:

- Manual, version 5.2 included.

Installation Update Guide

In order to update your manual you should replace the following page in the old manual version 5.1:

- Title page.
- Table of contents.
- Figures and tables.
- Table of contents on chapter 2.
- Non-Operator Mode, Supermax module type. Page 2-3-1 and 2-3-2
- Table of contents on chapter 8.
- Peripheral parameter and error codes, Winchester drive parameter. Page 8-2-31 and 8-2-34
- Table of contents on Appendix.

Add the following chapters in the old manual version 5.1:

- Appendix B (Release note). Pages B-1 to B-6

Release Note
Package No. 40030001
Dansk Data Elektronik A/S

Product name:	Supermax Diagnostic Programs
Stock number:	40030001
Version:	5.5
Date:	97.03.19
Completed by:	OK/BD

Please read this release note when you receive the package.

Package List

First Installation:

Floppy disks:
40030001 1 5¼" 560 kb diskette. Supermax Diagnostic Programs 5.5
40030001 1 3½" 1.44 Mb diskette. Supermax Diagnostic Programs 5.5

Documents:
1 Release Note (this document)
94400311 1 Diagnostic Programs for the Supermax 5.5

Installation Update:

Floppy disks:
40030001 1 5¼" 560 kb diskette. Supermax Diagnostic Programs 5.5
40030001 1 3½" 1.44 Mb diskette. Supermax Diagnostic Programs 5.5

Documents:
1 Release note (this document)
1 Update for Diagnostic Programs 5.5 (15 pages)

Labeling

Label on floppy disk:

```
Supermax Diagnostic Programs
Version 5.5     Date 97.03.19
Stock Number    40030001
© Dansk Data Elektronik A/S      1(1)
```

Product Features

The Diagnostic Program will test the Supermax hardware modules.

Requirements

Disk Space:

None.

Release Information

Changes since latest release:

- The DIOC3 test program supports formatting of three new winchester disks. Seagate ST31051N (1 Gbyte), Seagate ST32171N (2.1 Gbyte) and Seagate ST34371N (4.3 Gbyte).

Errors corrected since latest release:

- None.

Recognized errors or inconveniences:

- When a disk on a DIOC3 is configured with dual host option, only one DIOC3 is allowed to access the winchester on the SCSI cable when using the Diagnostic Programs.
- The DIOC3 test program cannot reassign blocks on PRIAM winchester. (A firmware error on the PRIAM winchester causes the error). If an error occurs on a disk and it is necessary to reassign block on the disk, then use a DIOC2 module instead to reassign the block or send the disk to DDE repair center.
- When running active bus test from DIOC3, CPU 68030, CPU R3000 and CPU R4000 modules, all modules must be in passive bus test mode. Otherwise, it is possible to cause a time-out (Bus error) on the active modules.
- When running test on Multi Zone Recording winchester disks, the program will not calculate the physical cylinder, head and sector position correctly.
- Do not run parity circuit test on MIOC4800 module, the test will fail. It is because the parity circuit is removed from the MIOC4800 module.
- Non-Operator test cannot be installed on a SVR4 platform.
- When running HDLC submodule internal/external loop back test on a HDLC submodule with a HDLC controller (82532 version V2.2), the MIOC test program some times reports a fault "Time-out during wait for receive complete" or "Data error in received buffer". This is not actually an error and can be ignored.

Comments

This Diagnostic Programs contains versions of the programs for:

- SIOC 0300 Version 5.0
- CIOC 0900 Version 5.0
- NIOC 1600-3600 / SIOC2 3600 Version 5.0.2
- MIOC 4600 Version 5.2.2
- DIOC1 0400 Version 5.0.1
- DIOC2 1100 Version 5.0.1
- DIOC3 4000 Version 5.5
- CPU 68000 0100 Version 5.0
- CPU 68020 3400 Version 5.0
- CPU 68030 4100 Version 5.0
- CPU R3000 4500 Version 5.0.2
- CPU R4000 4700 Version 5.2.3

First Installation

Please read the user's guide prior to product installation.
Then follow the procedure described under 'Installation Guide'.

Installation Update

Please read the user's guide prior to product installation.
Then follow the procedure described under 'Installation Update Guide'.

Installation Guide

Diagnostic Programs version 5.5:

- Manual, version 5.5 included.

Installation Update Guide

In order to update your manual you should replace the following page in the old manual version 5.4:

- Title page.
- Table of contents.
- Figures and tables.
- Table of contents on chapter 8.
- Peripheral parameter and error codes, Winchester drive parameters. Page 8-2-37 and 8-2-38
- Table of contents on Appendix.
- Appendix B (Release note). Pages B-1 to B-6

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