408 504
5 702236 210059

1 SCHEMATICS
Level 1

2 SCHEMATICS
Level 2

3 SCHEMATICS
Level 3

4 RAM

5 CLOCK DISTRIBUTION
DELAY CALCULATIONS

6 PACKAGE PINOUT
SSO CALCULATIONS

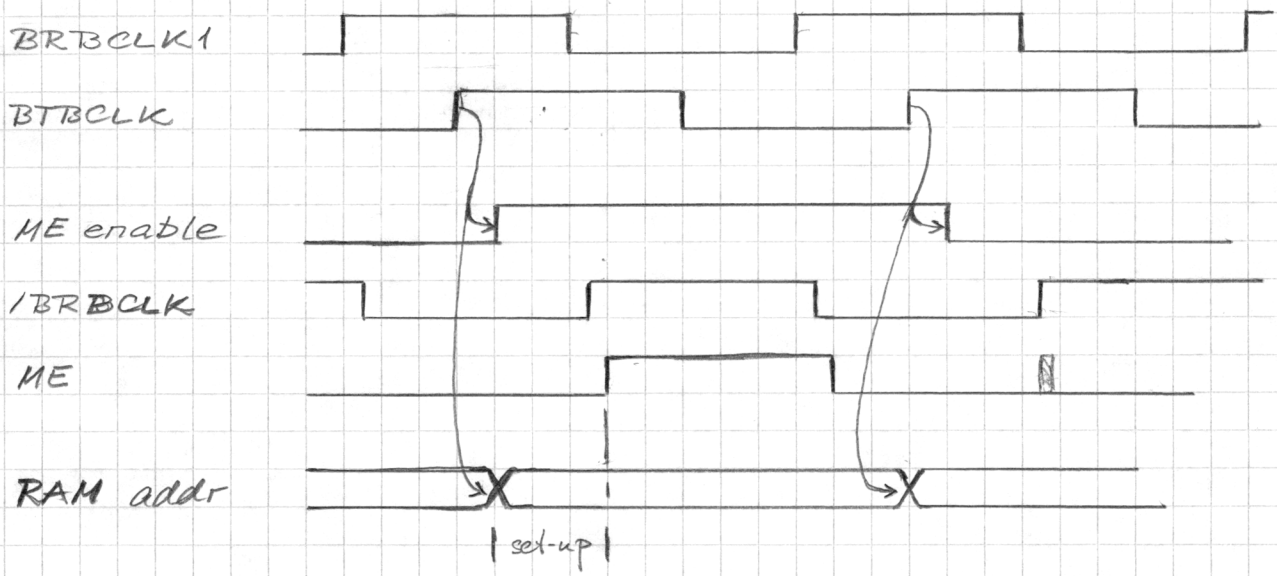
7 POWER CONSUMPTION

8 CA302 DESIGN DOCUMENT

9 ES2 DESIGN SYSTEM

10 BUS ACCESS CONTROL LOGIC

6210
Bantex
DENMARK



33,33	MHz	T/2	=	15 ns	
32	MHz	T/2	=	15.62 ns	(+ 0.62 ns)
30	MHz	T/2	=	16.67 -	(+ 1.67 ns) ←
31	MHz	T/2	=	16.13 -	(+ 1.13 ns)

Nom:

RCLK	+ 3 ns	
TCLK	+ 5.3 ns	(3 + 2.3)

Max: (+1.6 ns)

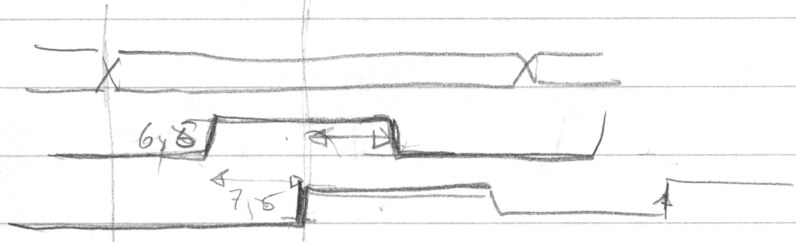
RCLK	+ 3 ns	
TCLK	+ 6.9 ns + 5.9	(3 + 2.3 + 1.6) (-1 ns)

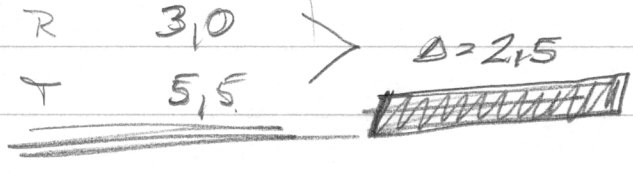
Min: (-1.6)

RCLK	+ 3 ns	
TCLK	+ 3.7 ns	(3 + 2.3 - 1.6)

0.7 - 2.9 -

2.3

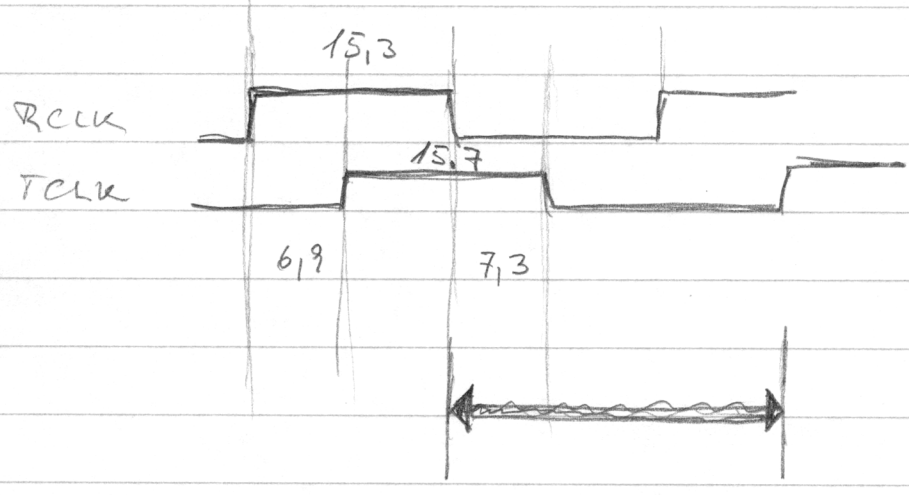




1,15 × 6 = 6,9

1,15 × 4 = 4,6

1,15 × 2 = 2,3



AAJ / 95-05-17

BUS CLOCK FREQUENCY

BUS CLOCK	RCLK to TCLK ×6	×4	×2
33 MHz	6.92 ns	4.62 ns	2.30 ns
32 MHz	7.21 ns	4.81 ns	
31 MHz	7.44 ns	4.96 ns	
30 MHz	7.69 ns	5.13 ns	2.54 ns
29 MHz	7.96 ns	5.31 ns	
28 MHz	8.24 ns	5.49 ns	
35 MHz	6.59 ns	4.40 ns	2.20 ns

R to T clock delay

30 MHz : T/2 = 16.67 ns

ΔR/T = 7.69 ns

RAM set-up = 8.98 ns ok (grænsen)

33 MHz ; T/2 = 15 ns

ΔR/T = 4.62 ns

RAM set-up = 10.38 ns ok

RAM access = 15 + 4.62 = 19.62 ns

33 MHz : T/2 = 15 ns

ΔR/T = 6.92 ns

RAM set-up = 8.08 ns not ok

33 MHz : T/2 = 15 ns

ΔR/T = 2.30 ns

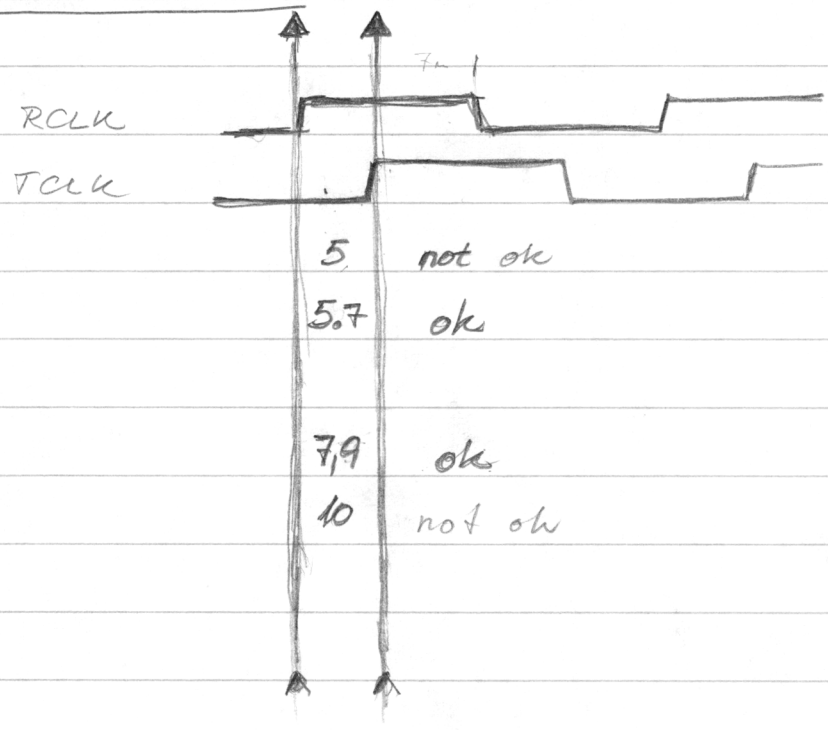
RAM set-up = 12.7 ns ok

RAM access = 15 + 2.30 = 17.30 ns

MIN. DELAYS

RCLK to TCLK 13 ns ok

MAX. DELAYS



5 not ok

5.7 ok 0.7

7,9 ok 3

10 not ok

MTBF 400-500 000 timer

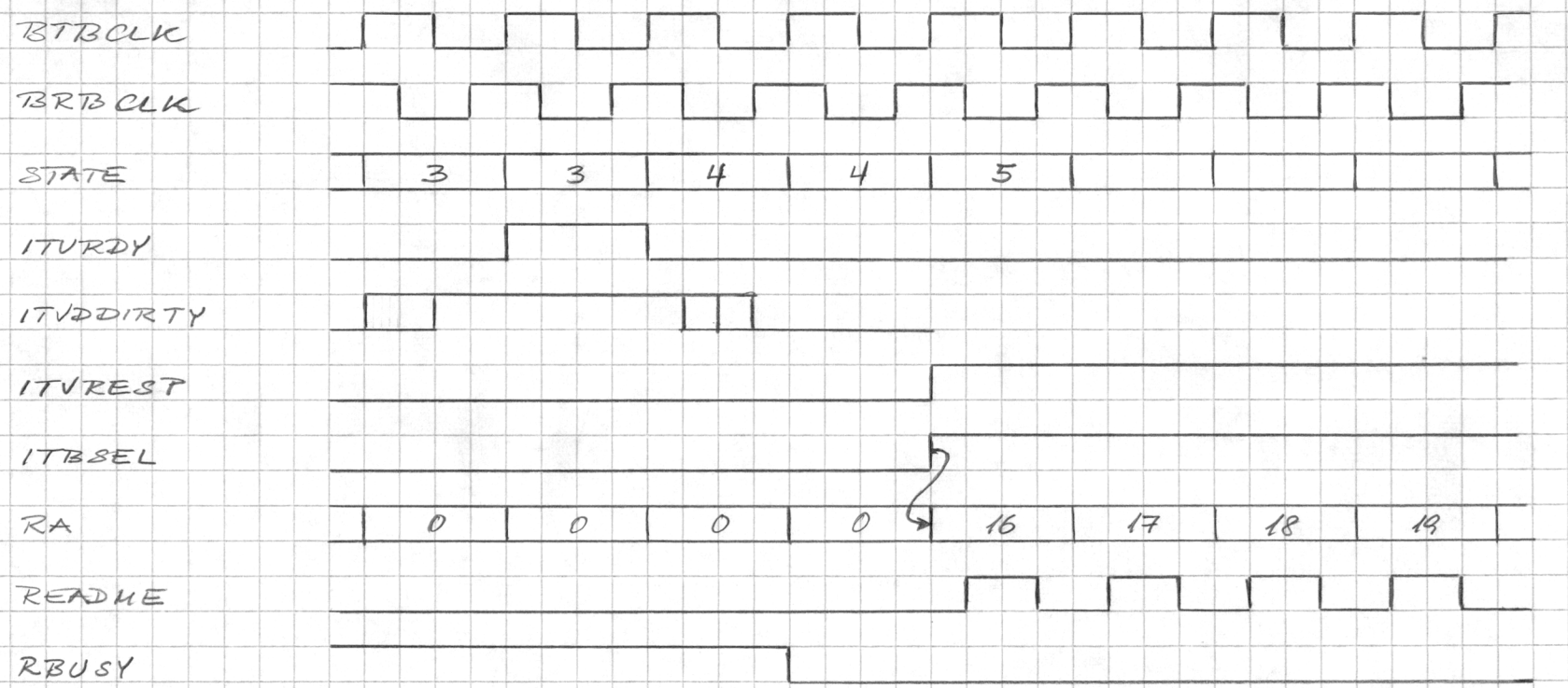
33 MHz PROBLEM

1. TCLK / RCLK timing på bussiden ?

2. Krav til RCLK / TCLK timing ved simulering af intervention response

Simpel testopstilling med 1 CPU, hvor RMO genererer intervention requests.

INTERVENTION RESPONSE - INTERVENTION BUFFER READ



Set-up from ITBSEL to README - min. time from TBCLK↑ to RBCLK↓

INTERVENTION BUFFER READ

ITBSEL → RA4; mest betydende adressebit - vælger mellem ITV og WRI buffer.

WIBRD; Enabler / resetter RA counter, Enabler READ ME til RAM.

ITBSEL = ITVRESP & ITVDDIRTY

ITVRESP = state 5 i Bus Slave Control Logic

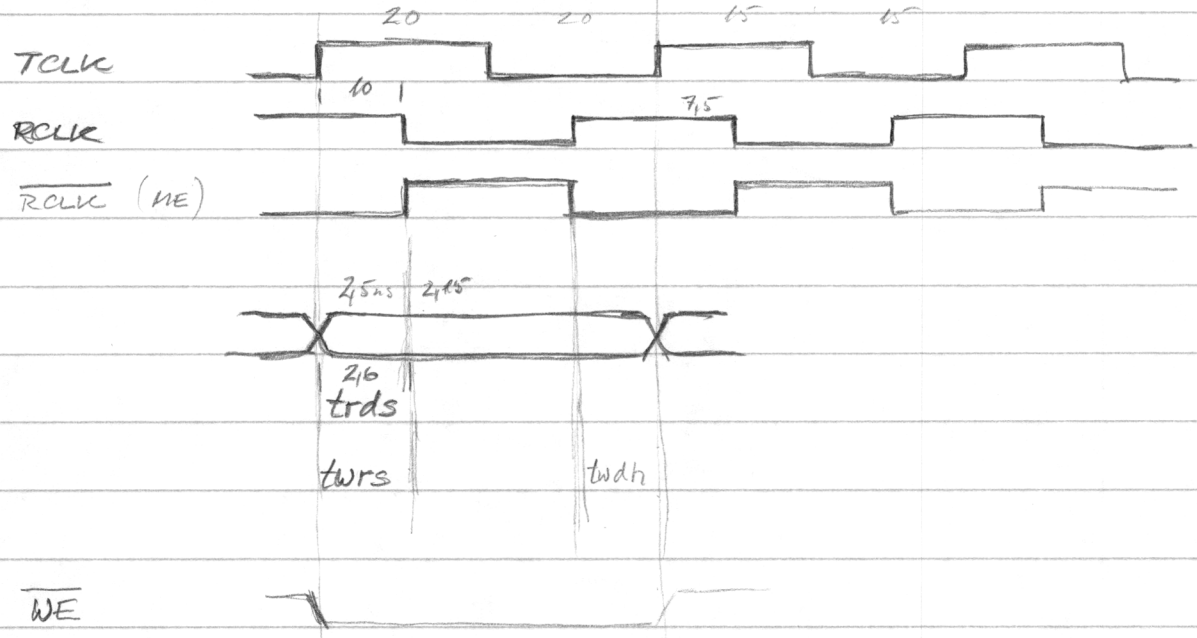
WIBRD = ITVRESP

INTERVENTION BUFFER WRITE

N_ITVDSEL → /ITBINIT; resets WA(3:0)
sets WA(4)
sker fler clockcycler før data fra R4000

ITBLD = LDITVD = ITVRQ buf & CMD8 & VALIN

RAM READ CYCLE



Til ohm.
cc: aaj

Paller til CPU300 og 1 uden den fancy rettelse:

/wd/mudv2/lbp/spc3/pal/cpu301/snoopa.jed til U138
/wd/mudv2/lbp/spc3/pal/cpu301/snoopb.jed til U139 og U141

Paller til CPU300 og 1 med den fancy rettelse:

CH = 49 07D

/wd/mudv2/lbp/spc3/pal/cpu301/newa.jed til U138
/wd/mudv2/lbp/spc3/pal/cpu301/newb.jed til U139 og U141 CH = 3D0C

Lars

Til ohm.
cc: aaj

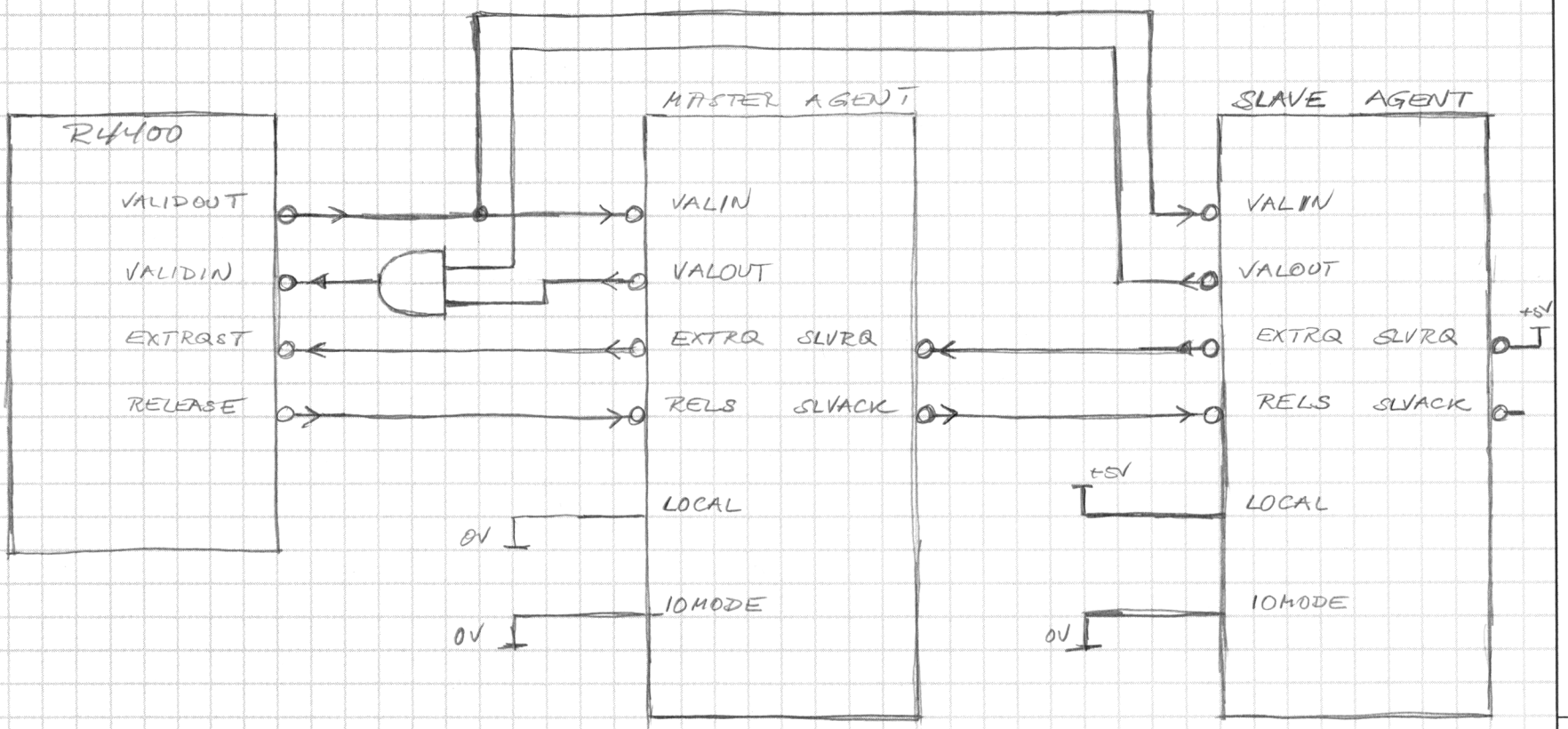
Paller til CPU300 og 1 uden den fancy rettelse:

/wd/mudv2/lbp/spc3/pal/cpu301/snoopa.jed til U138
/wd/mudv2/lbp/spc3/pal/cpu301/snoopb.jed til U139 og U141

Paller til CPU300 og 1 med den fancy rettelse:

/wd/mudv2/lbp/spc3/pal/cpu301/newa.jed til U138
/wd/mudv2/lbp/spc3/pal/cpu301/newb.jed til U139 og U141

Lars



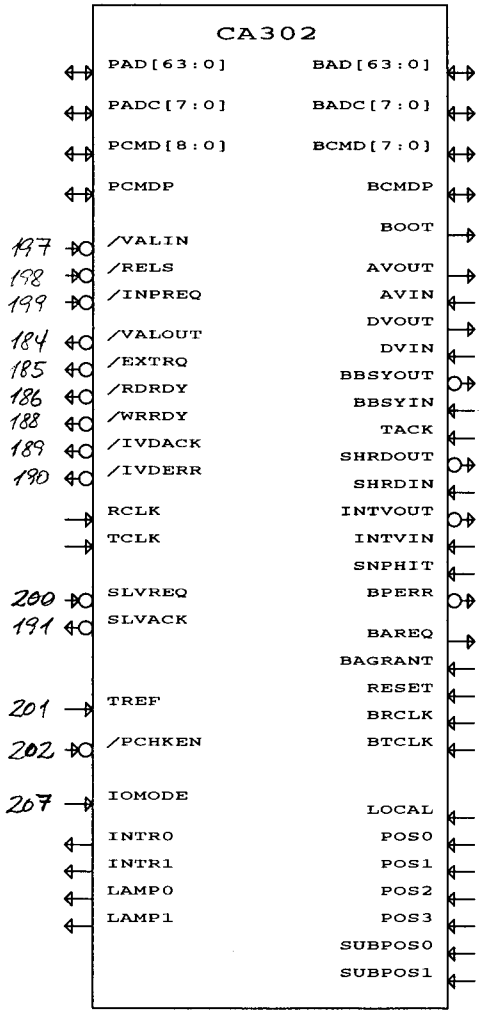
dde Dansk Data Elektronik A/S

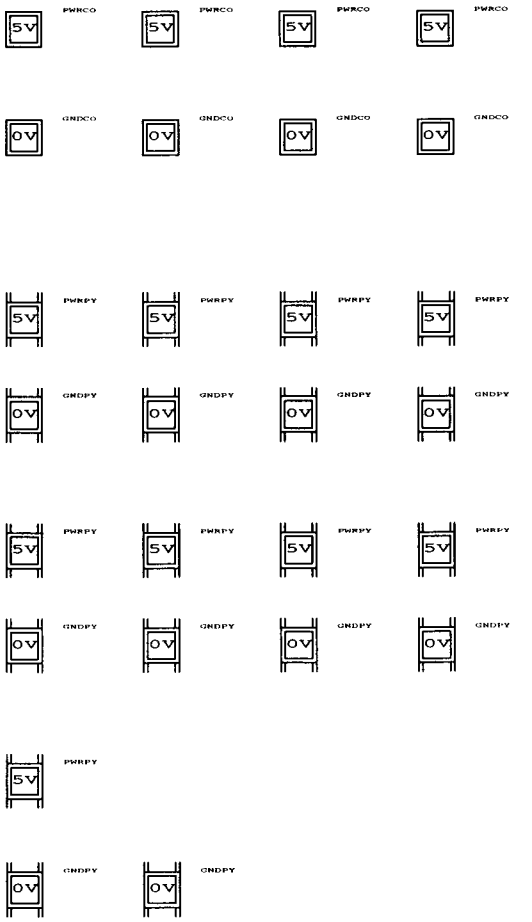
Initials

Date

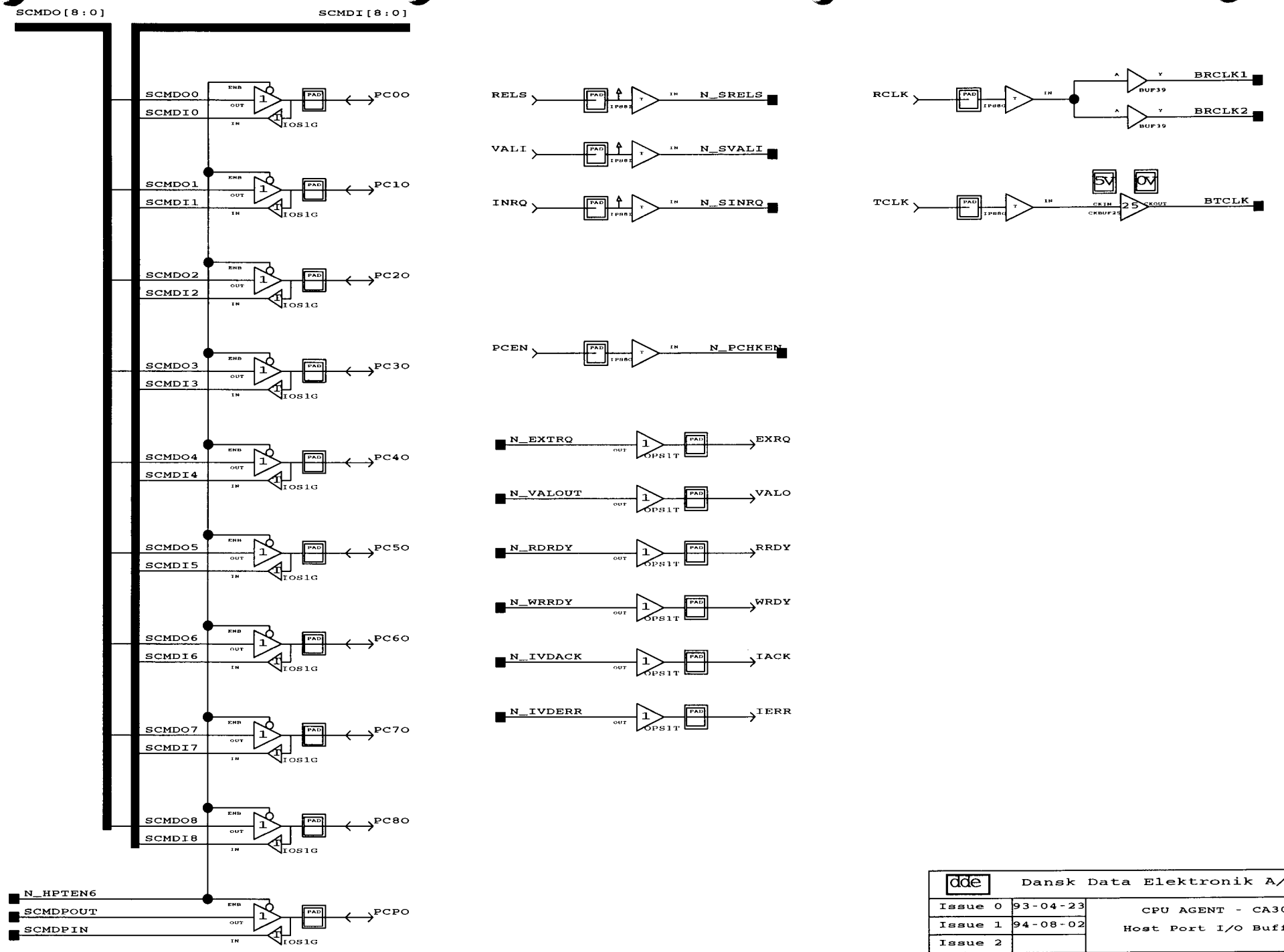
Page

Project

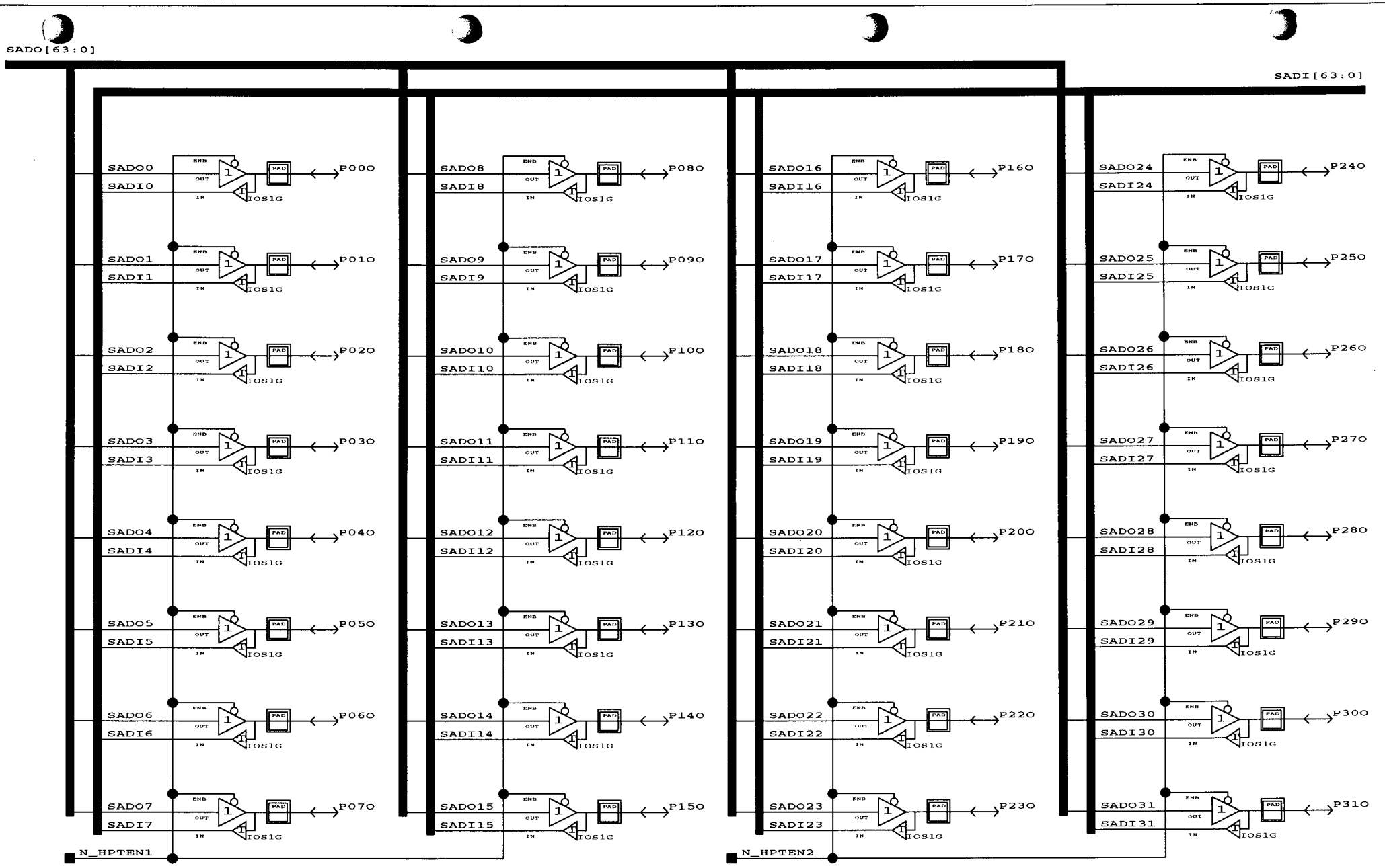




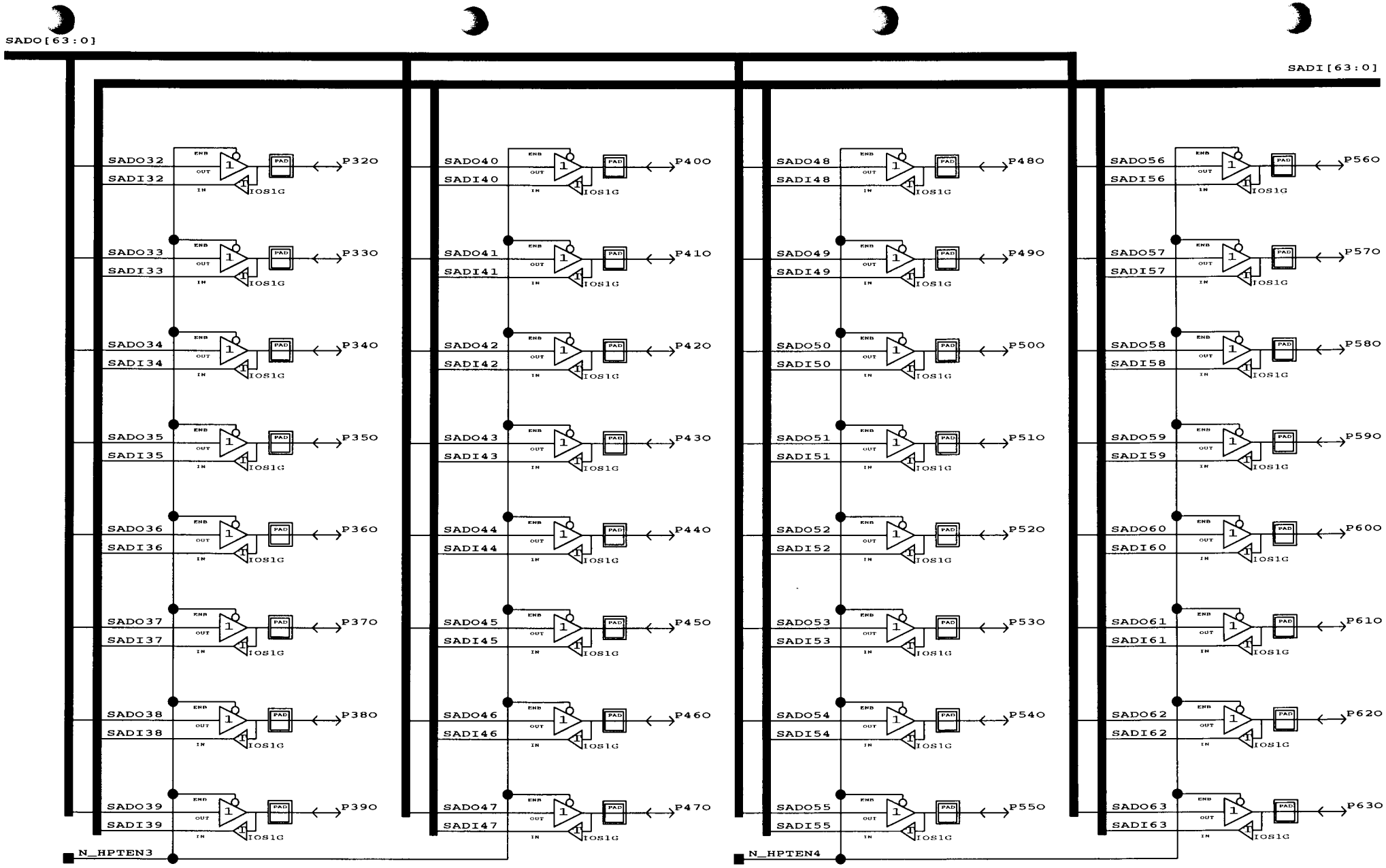
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-02	Power Pads
Issue 2		
Issue 3		File: cpa.1 Page:1 of 42



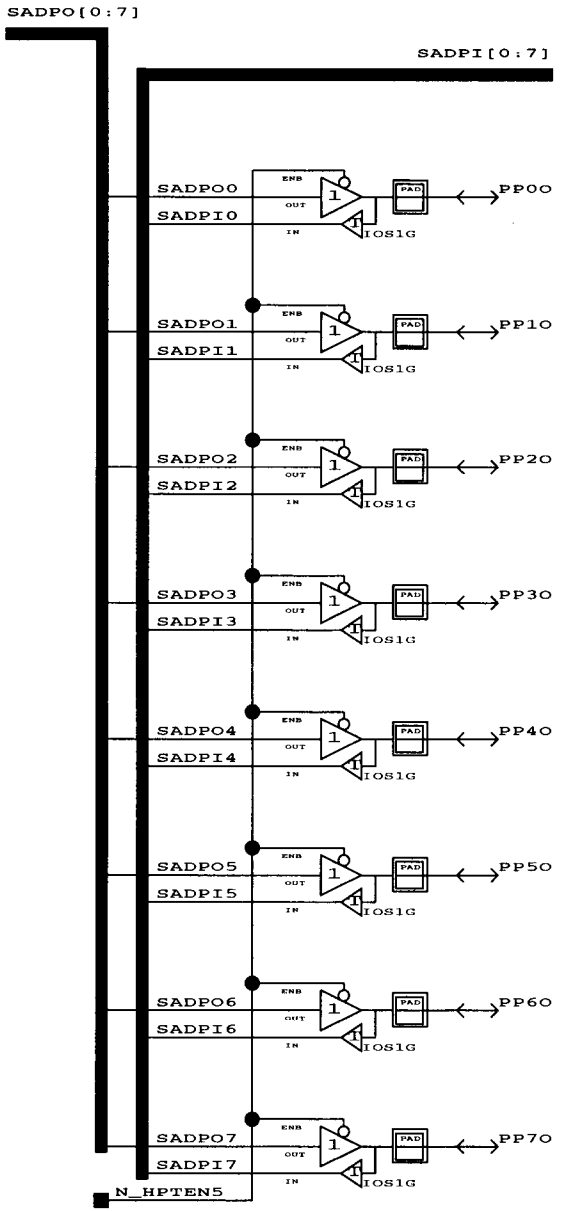
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-02	Host Port I/O Buffers
Issue 2		
Issue 3		File: cpa.2 Page:2 of 42

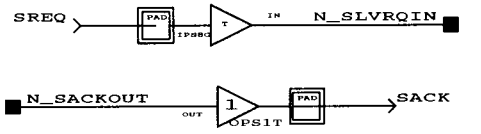


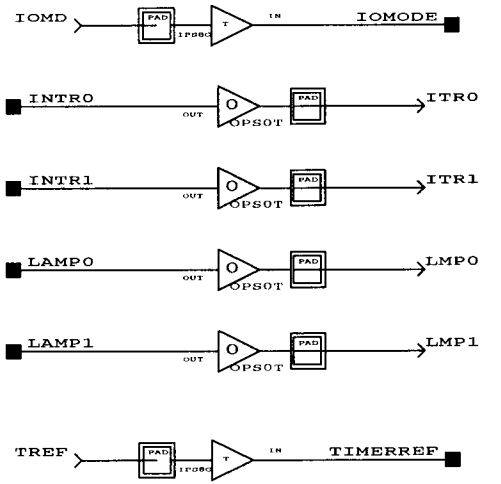
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-02	Host Port I/O Buffers
Issue 2		
Issue 3		File: cpa.3 Page:3 of 42



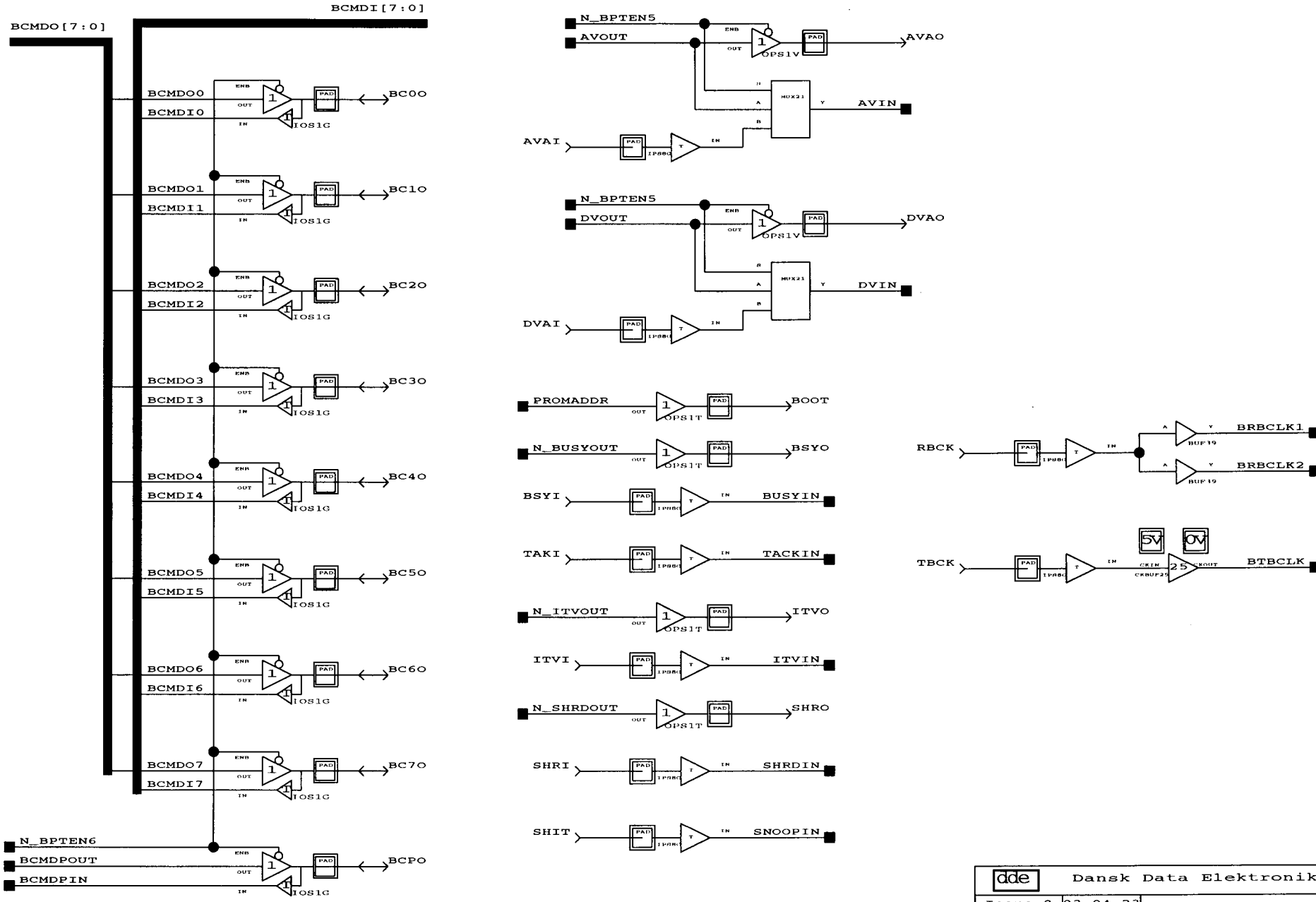
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-02	Host Port I/O Buffers
Issue 2		
Issue 3		File: cpa.4 Page:4 of 42



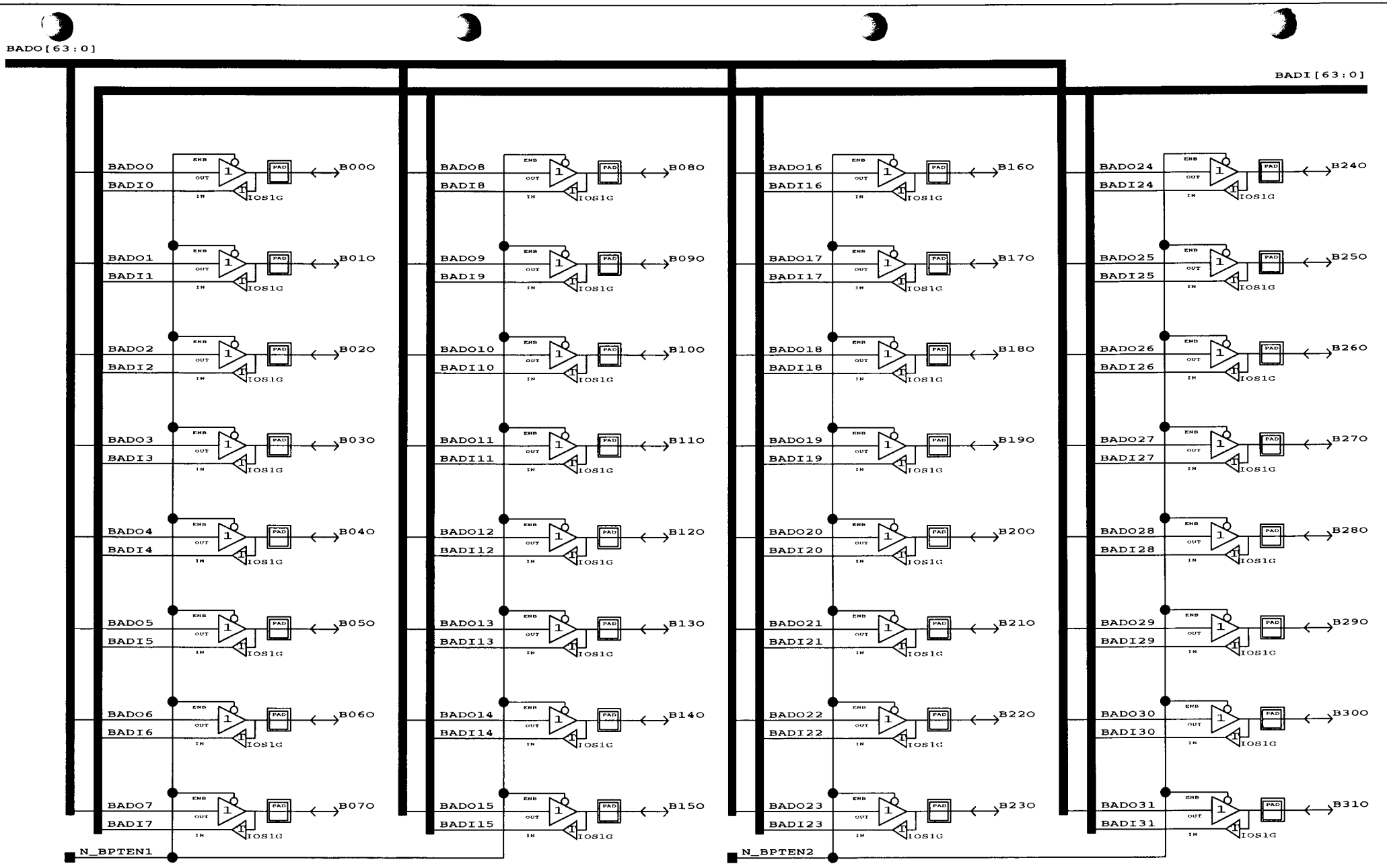




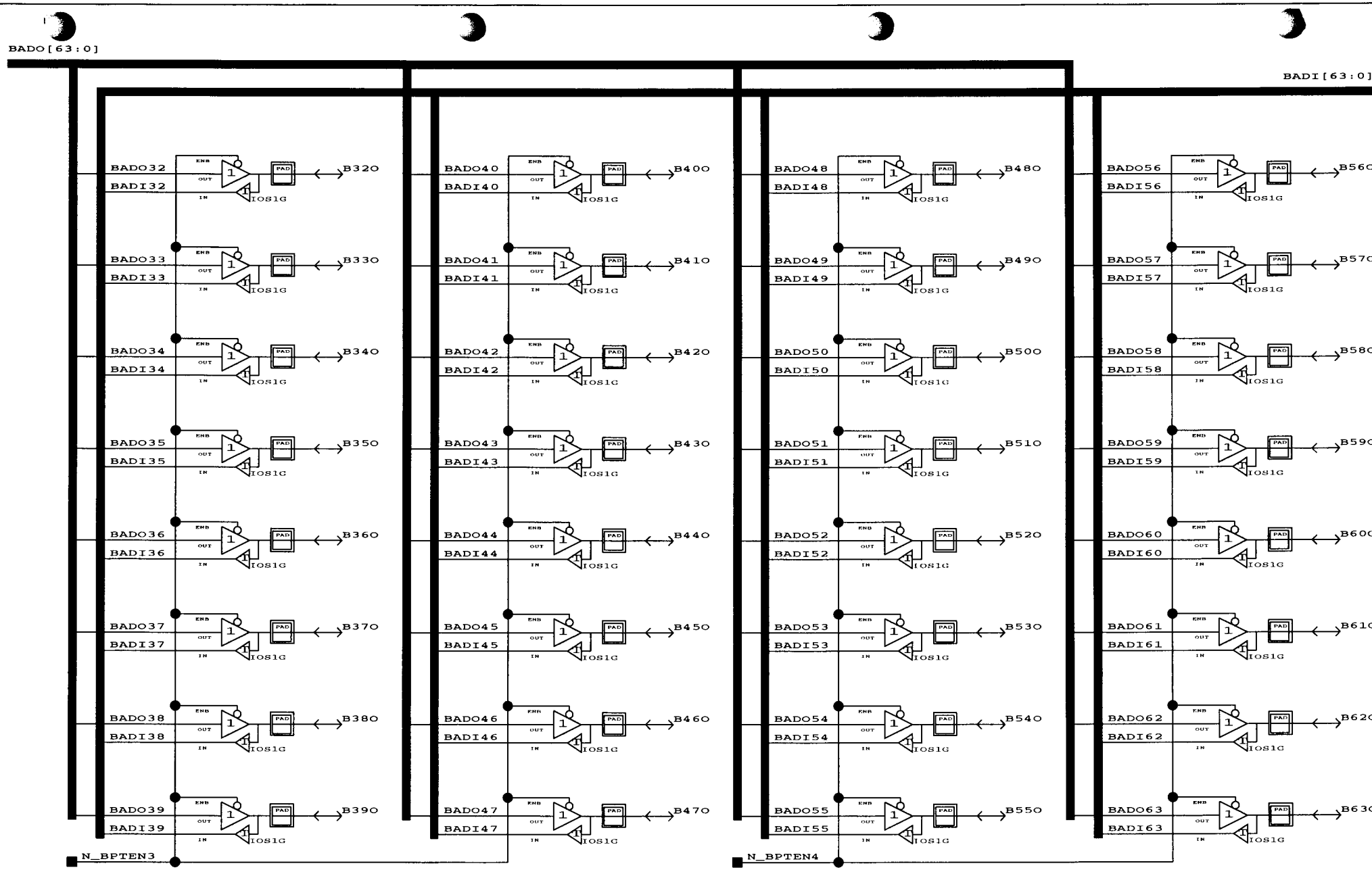
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-02	Host Port I/O Buffers
Issue 2		
Issue 3		File: cpa.5 Page:5 of 42



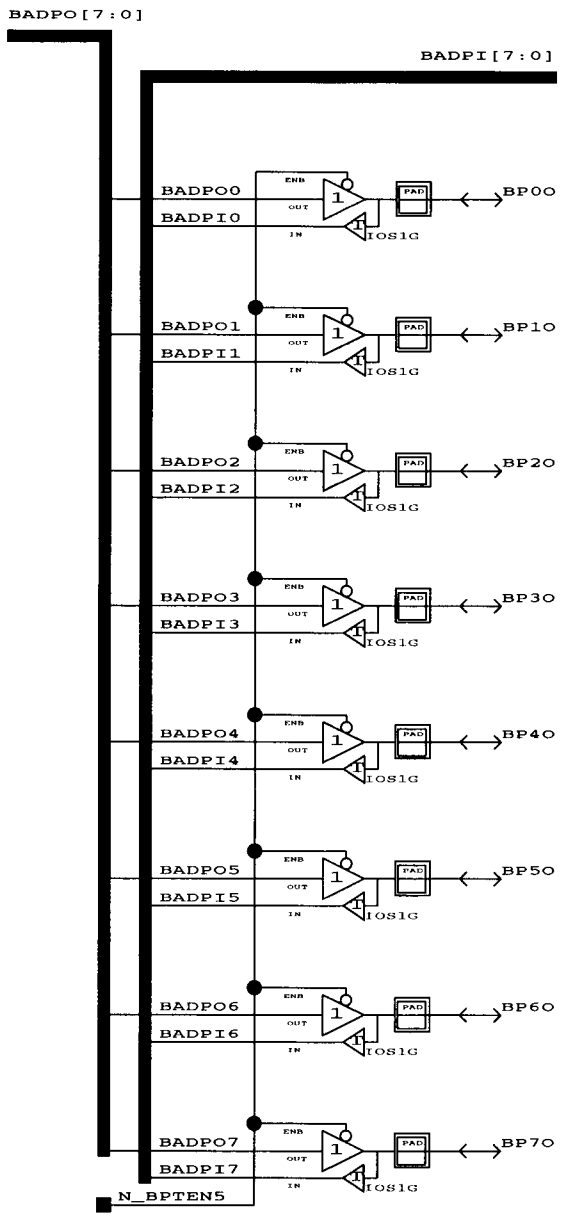
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-02	Bus Port I/O Buffers
Issue 2		
Issue 3		File: cpa.6 Page:6 of 42

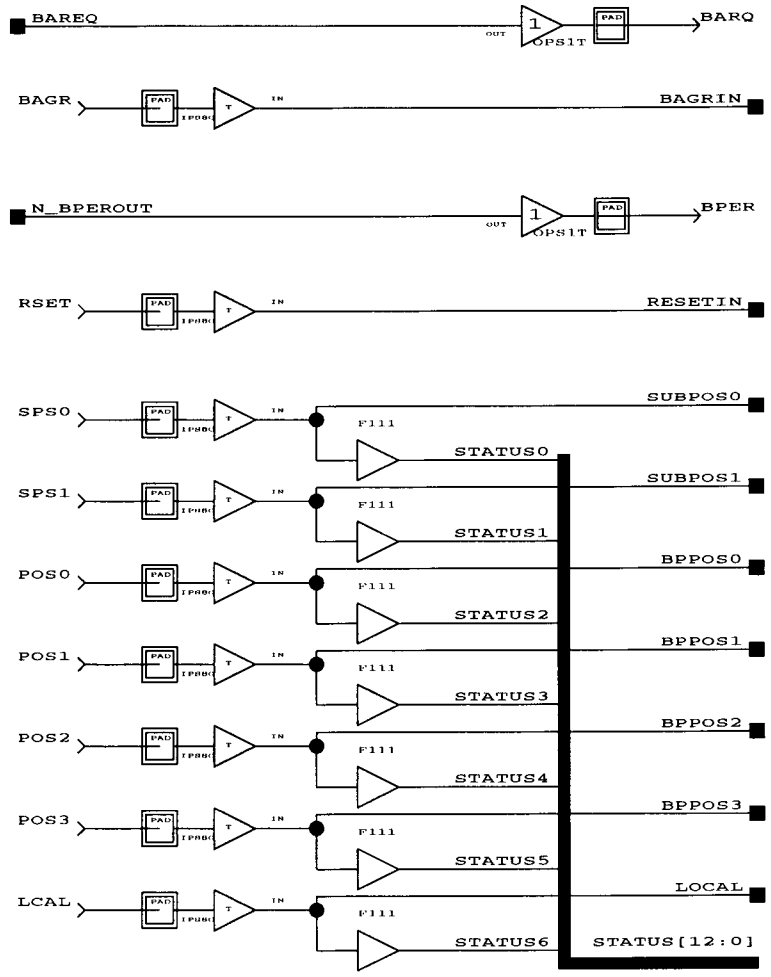


dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-02	Bus Port I/O Buffers
Issue 2		
Issue 3		File: cpa.7 Page:7 of 42

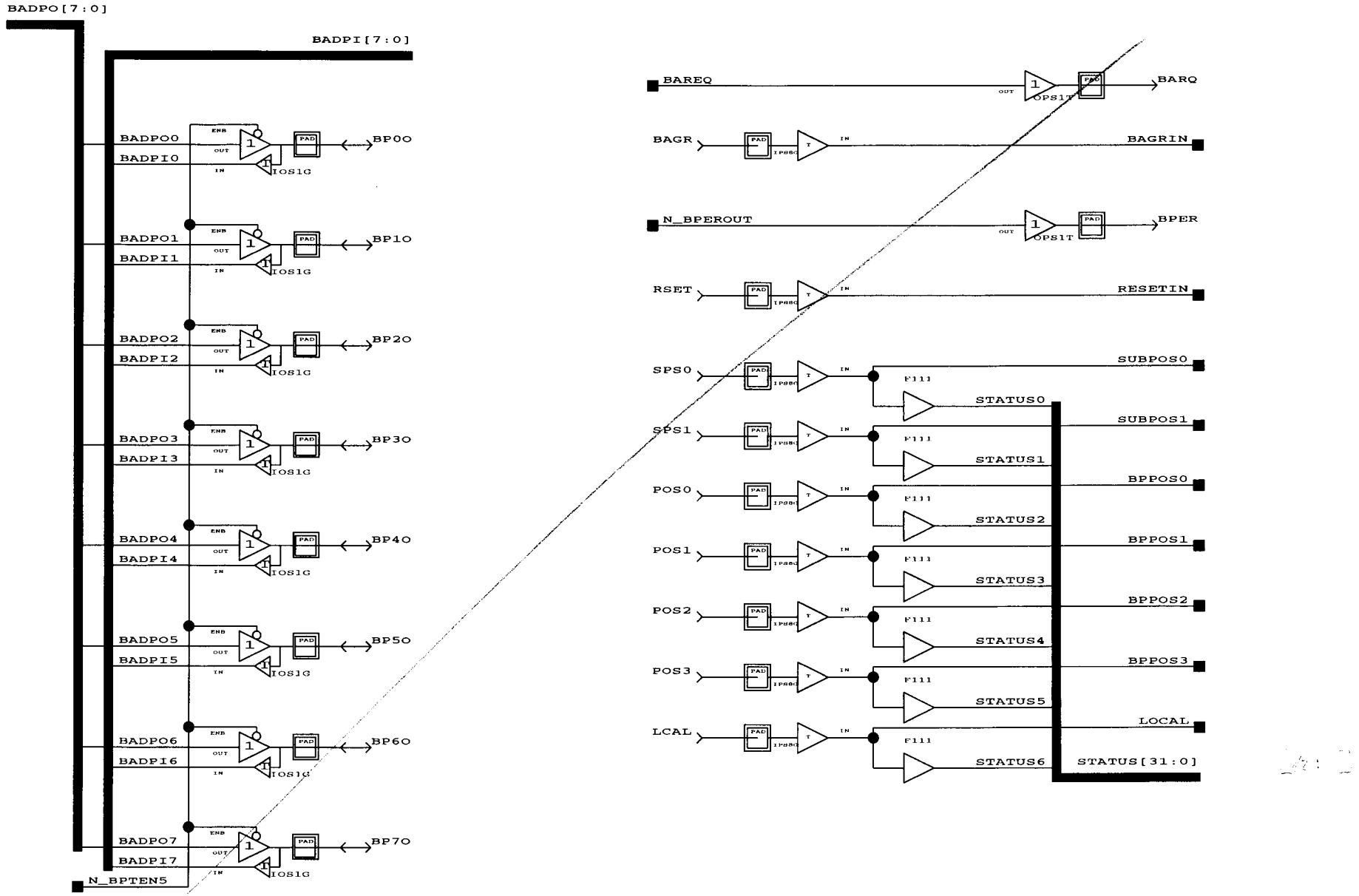


dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-02	Bus Port I/O Buffers
Issue 2		
Issue 3		File: cpa.8 Page:8 of 42

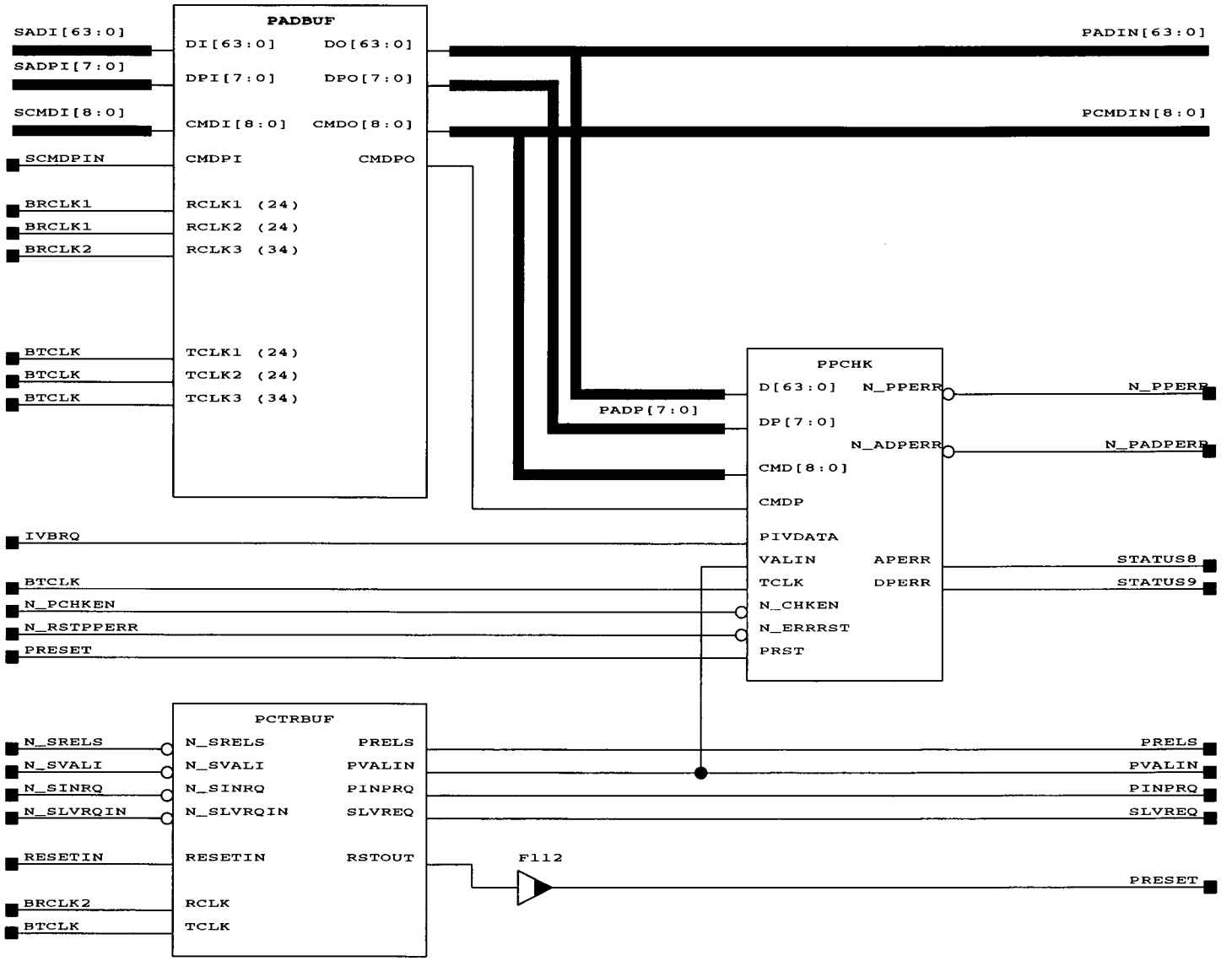




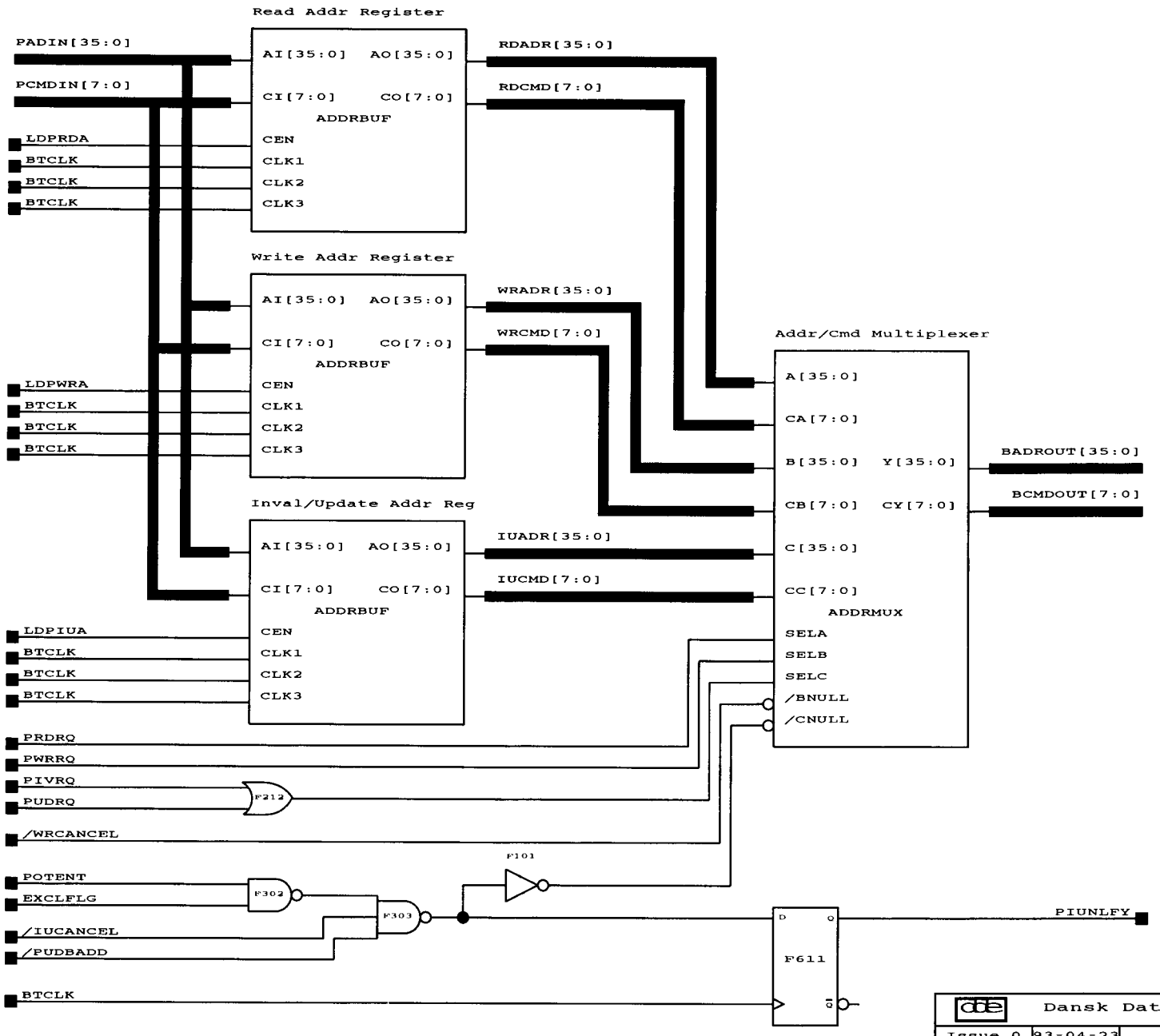
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-16	Bus Port I/O Buffers
Issue 2		
Issue 3		File: cpa.9 Page:9 of 42



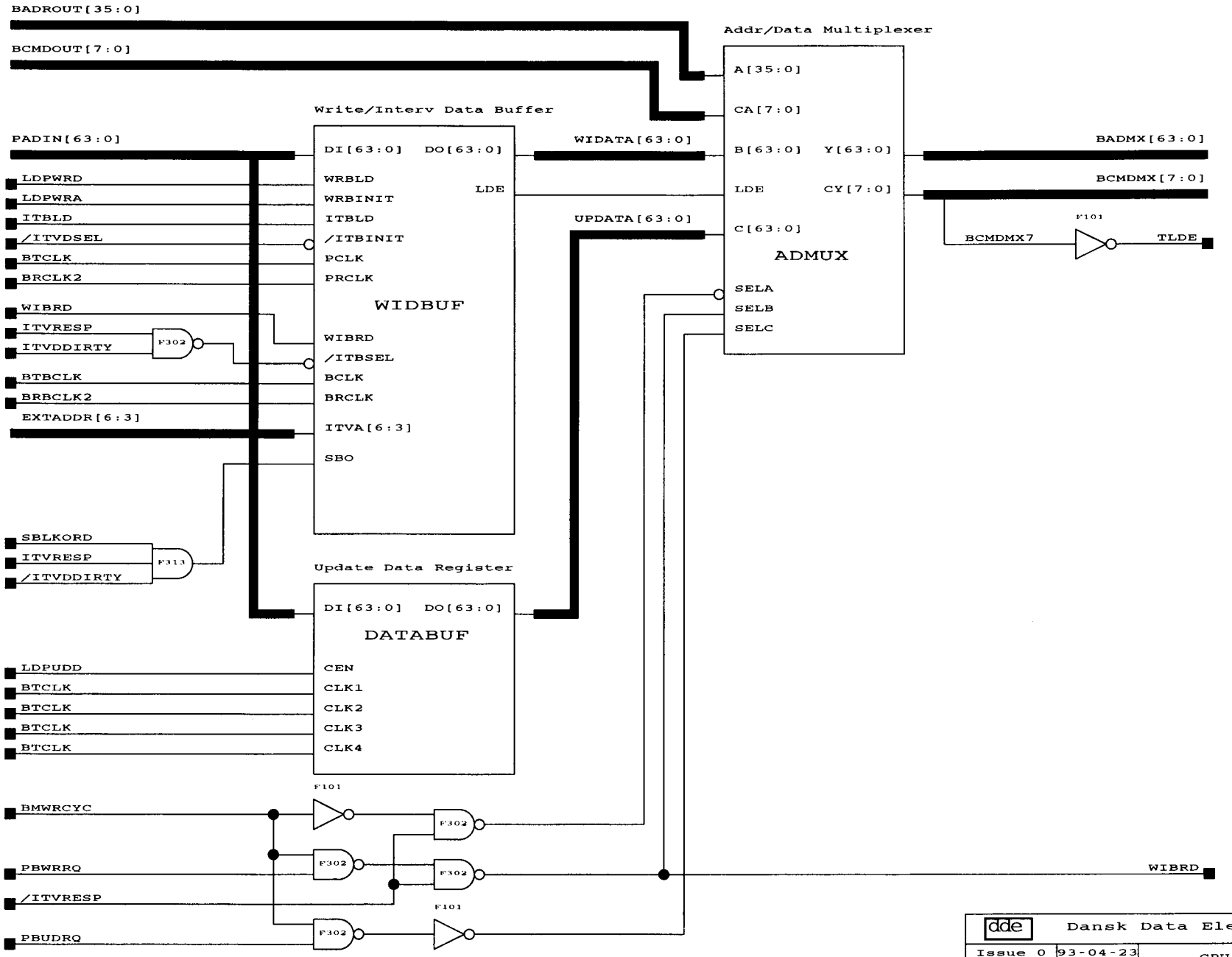
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-02	Bus Port I/O Buffers
Issue 2		
Issue 3		File: cpa.9 Page:9 of 42



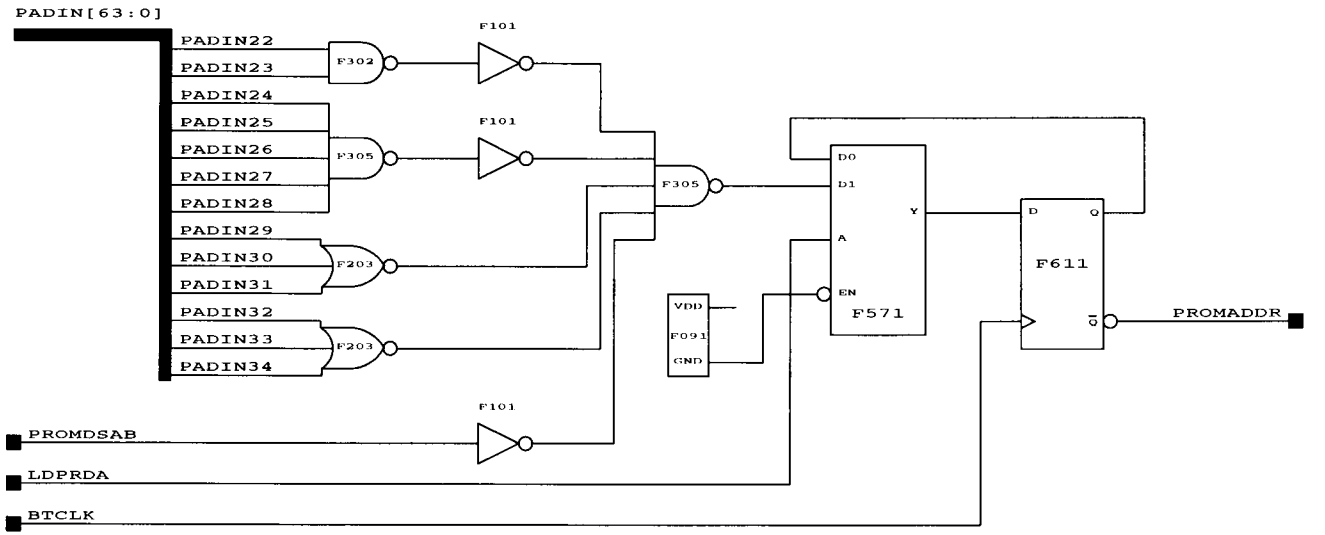
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-18	Host Port Input Registers
Issue 2		
Issue 3		File: cpa.10 Page:10 of 42

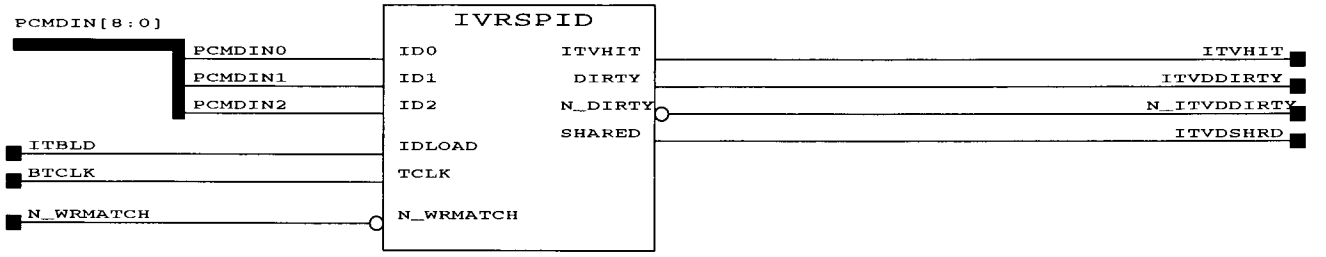


Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Output Address Registers and Address Multiplexer	
Issue 1			
Issue 2			
Issue 3		File: cpa.11	Page:11 of 42

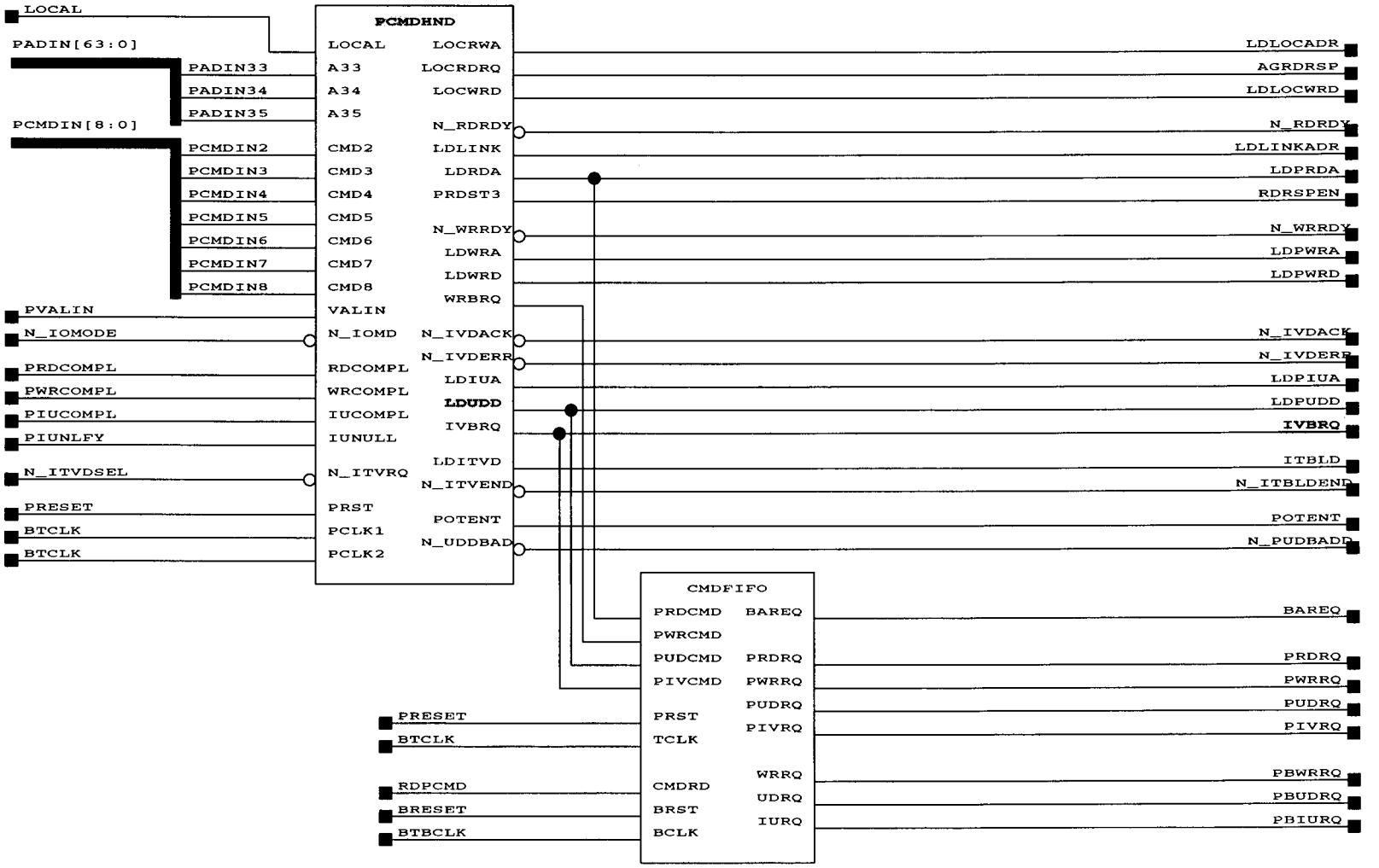


dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-02	Bus Addr/Data Multiplexer
Issue 2		
Issue 3		File: cpa.12 Page:12 of 42

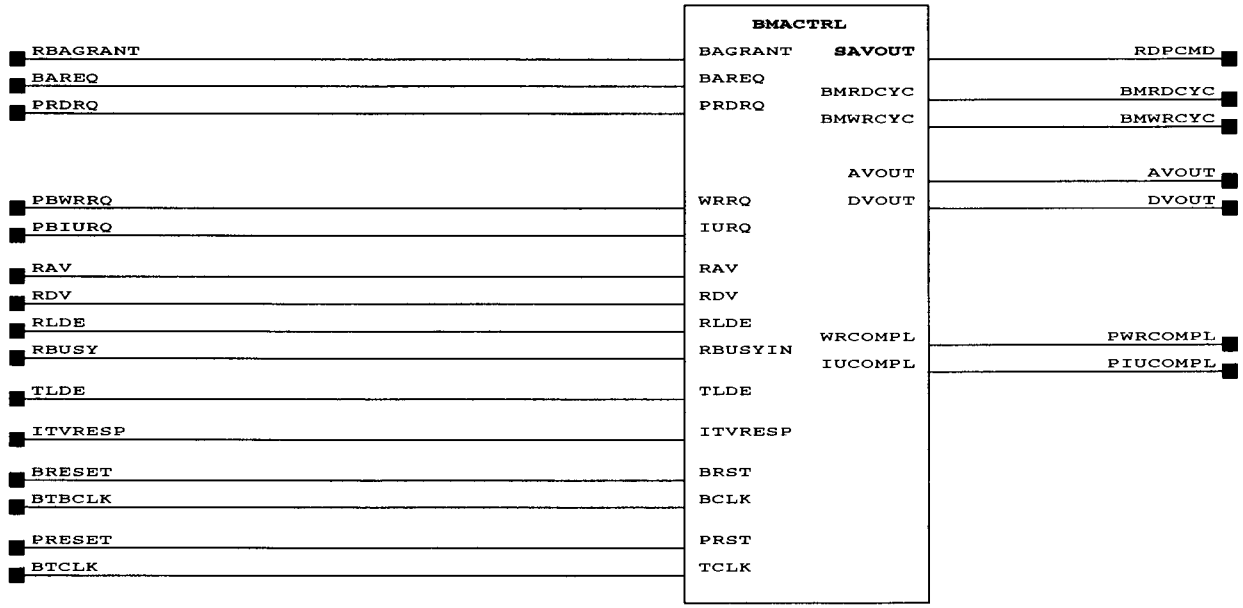




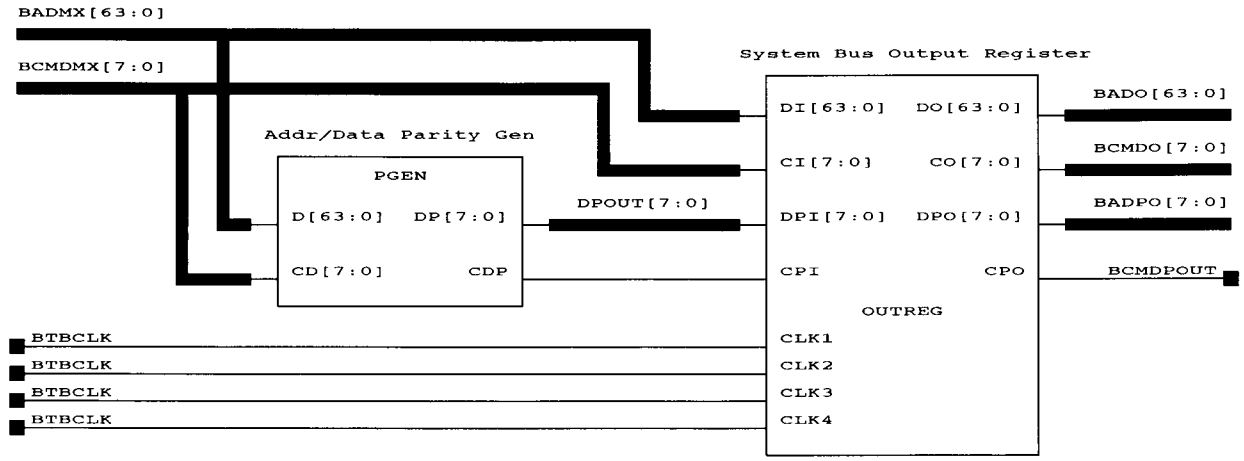
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		PROM Addr Decoding
Issue 2		Intervention Data ID
Issue 3		File: cpa.13 / Page:13 of NN



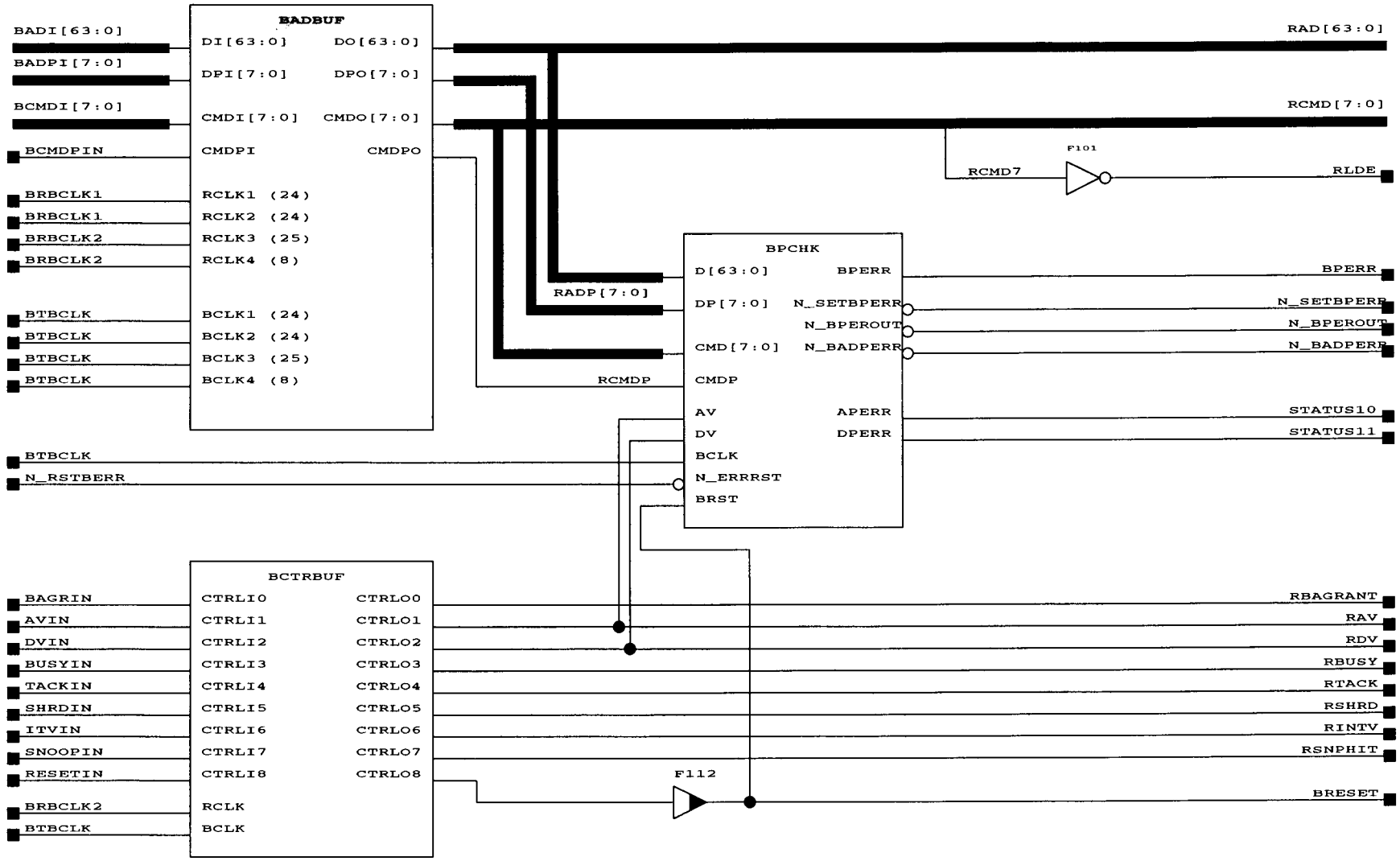
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-08	Processor Command Control
Issue 2		
Issue 3		File: cpa.14 Page:14 of NN



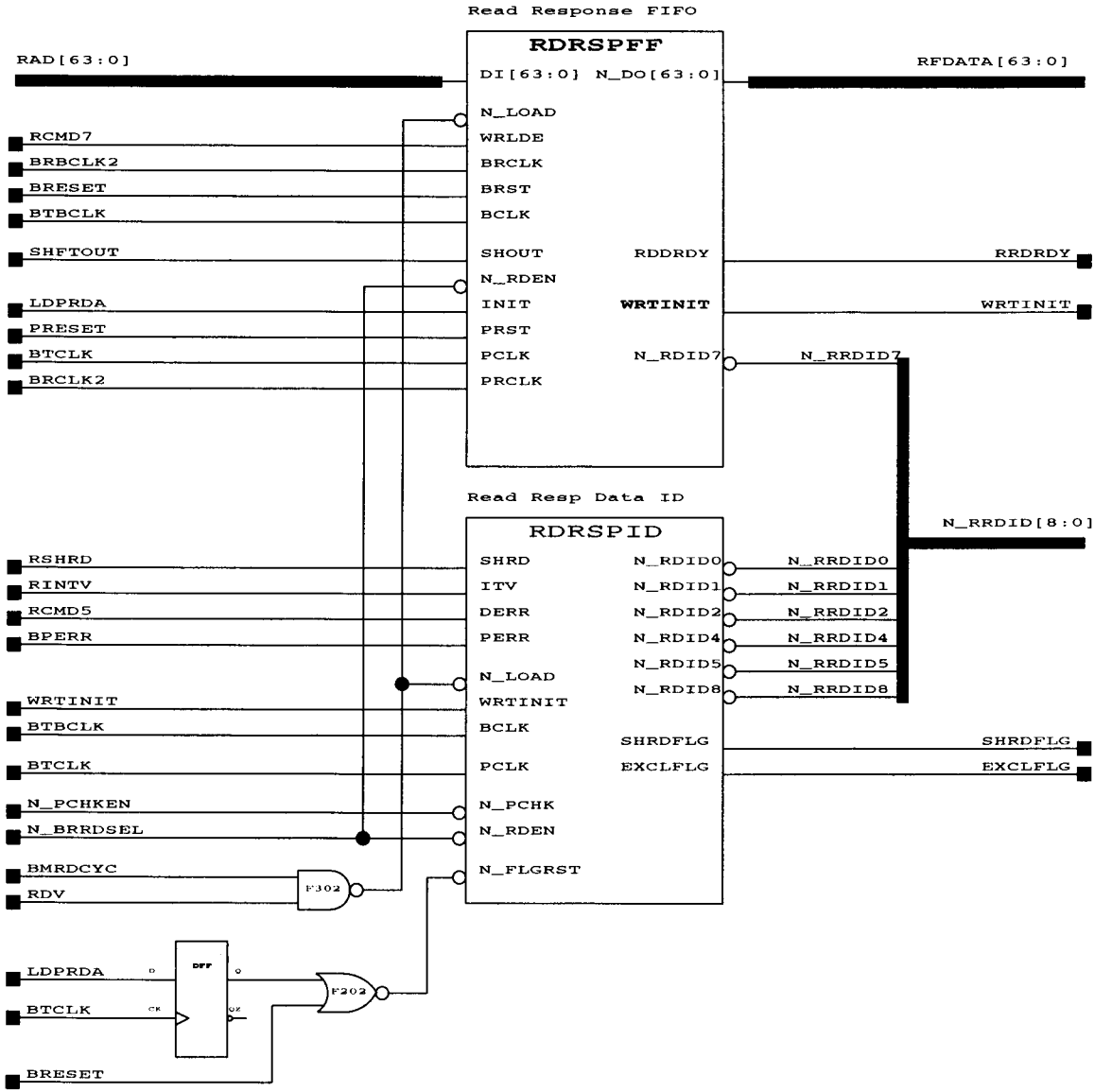
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-08	Bus Master Access Control
Issue 2		
Issue 3		File: cpa.15 Page:15 of NN



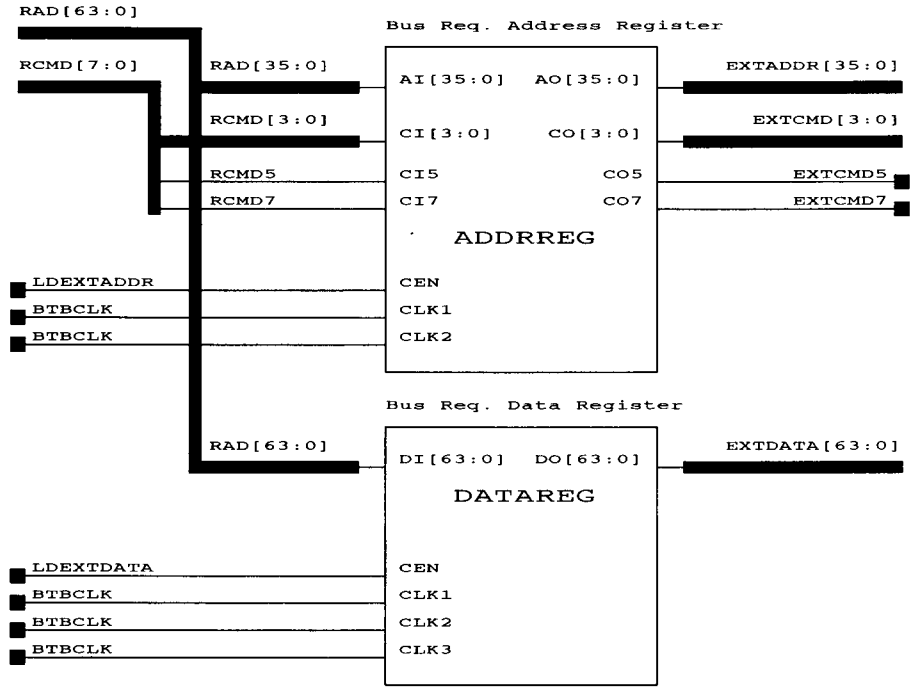
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Bus Output Register
Issue 2		
Issue 3		File: cpa.16 Page:16 of NN



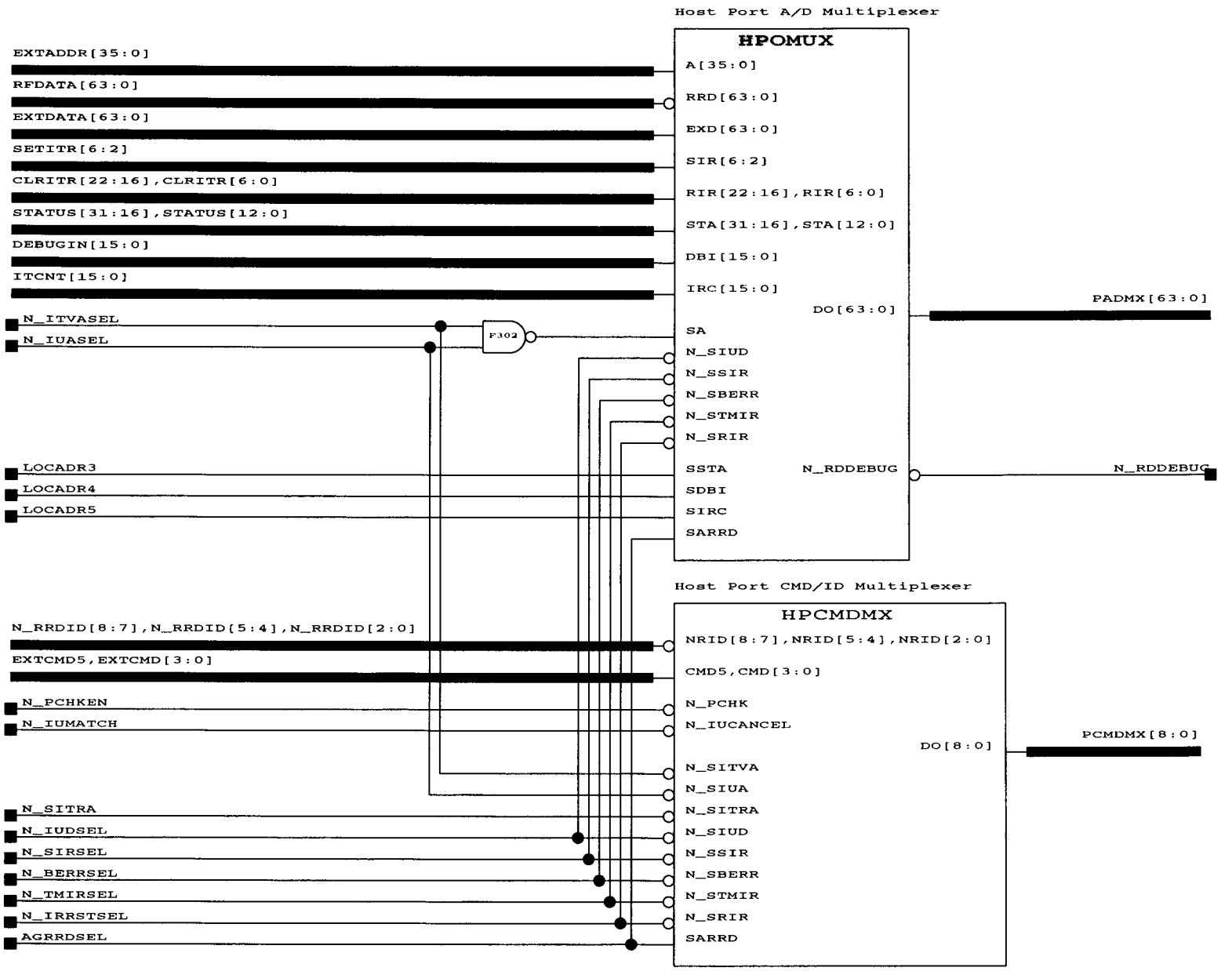
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-18	Bus Port Input Registers
Issue 2		
Issue 3		File: cpa.17 Page:17 of NN



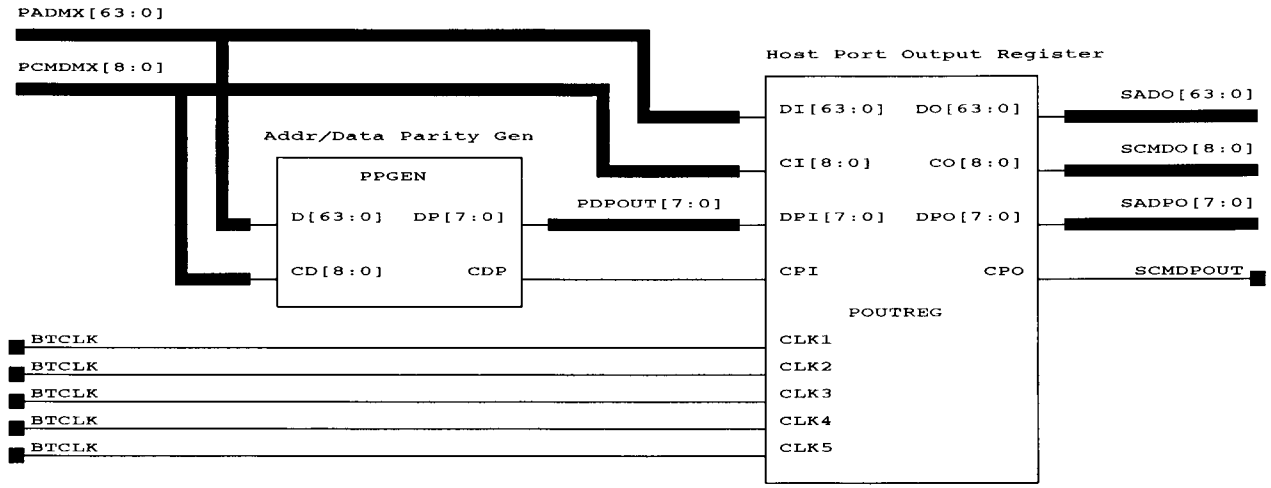
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-08	Read Response FIFO
Issue 2		
Issue 3		File: cpa.18 Page:18 of NN



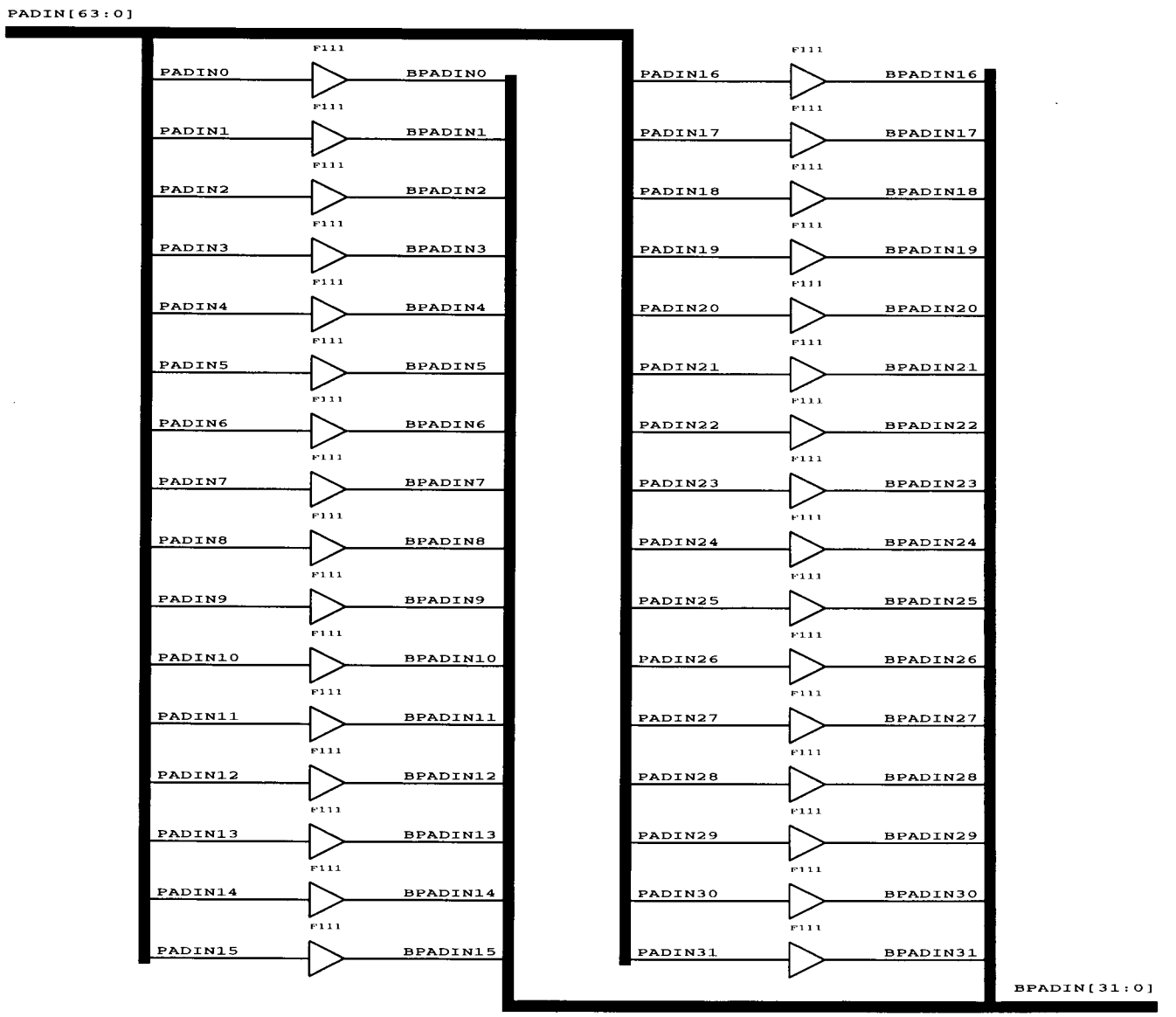
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-16	External Addr/Data Registers
Issue 2		
Issue 3		File: cpa.19 Page:19 of NN



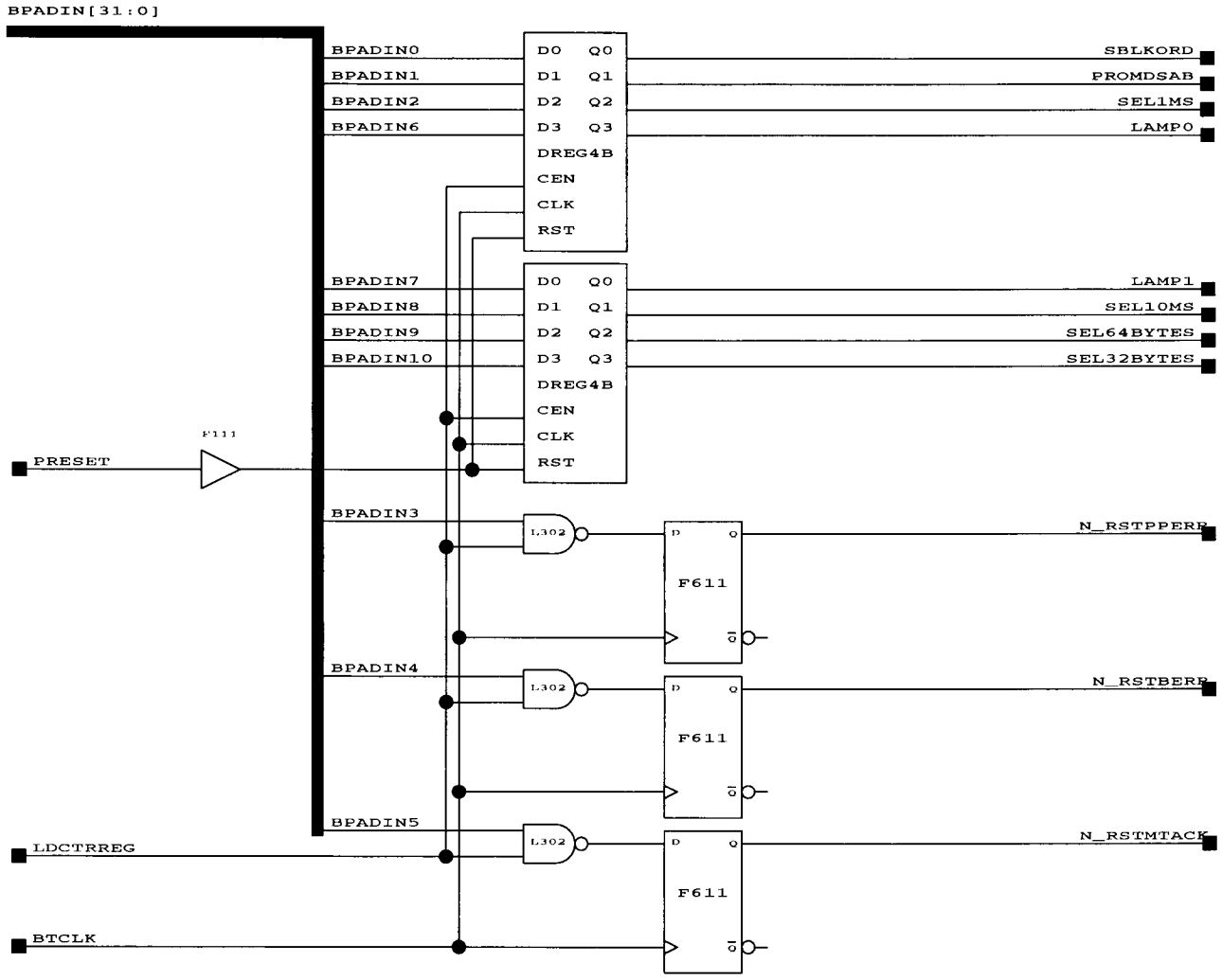
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1	94-09-18	Host Port Multiplexer	
Issue 2			
Issue 3		File: cpa.20	Page:20 of NN



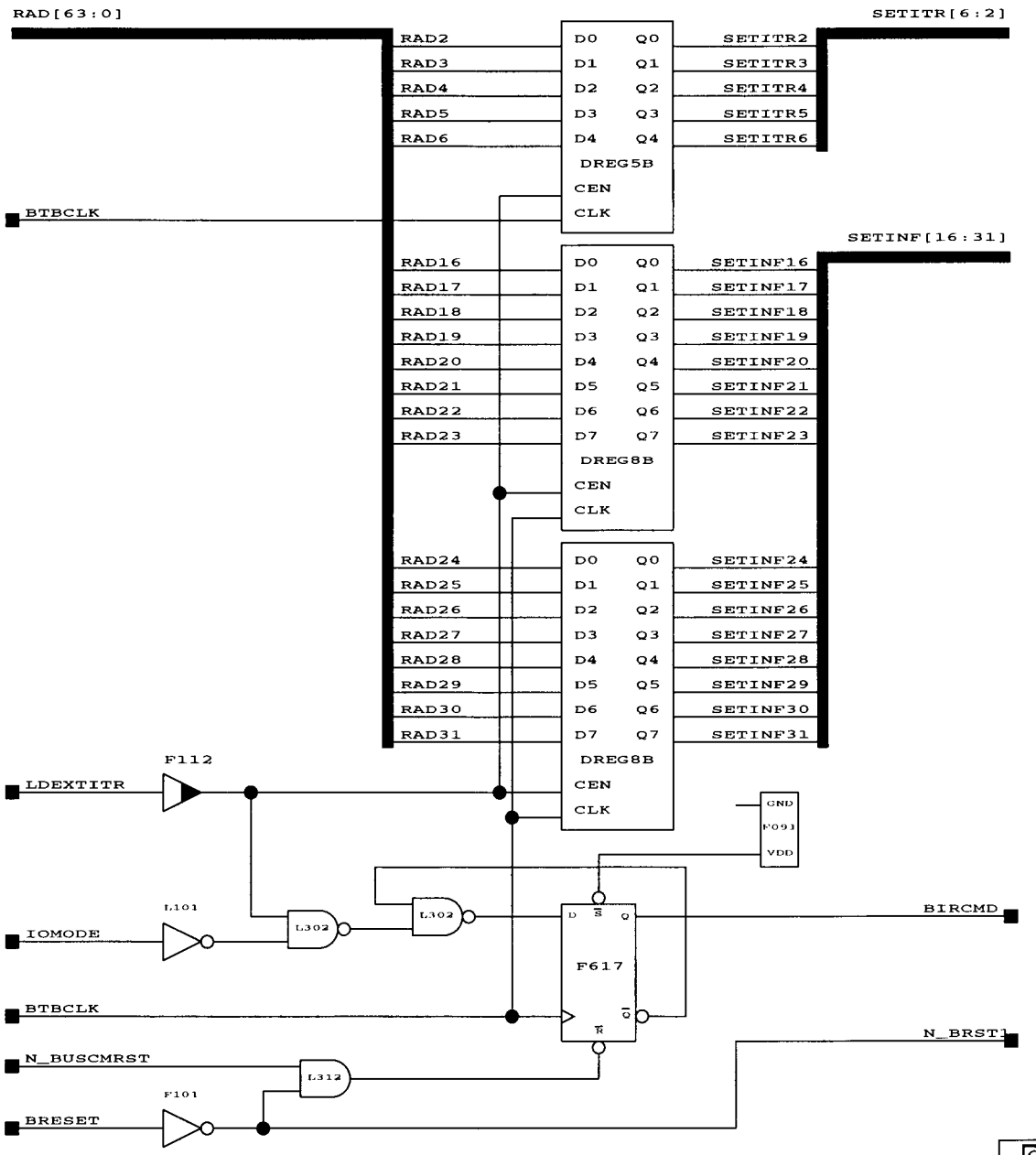
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Host Port Output Register	
Issue 1			
Issue 2			
Issue 3		File: cpa.21	Page:21 of NN



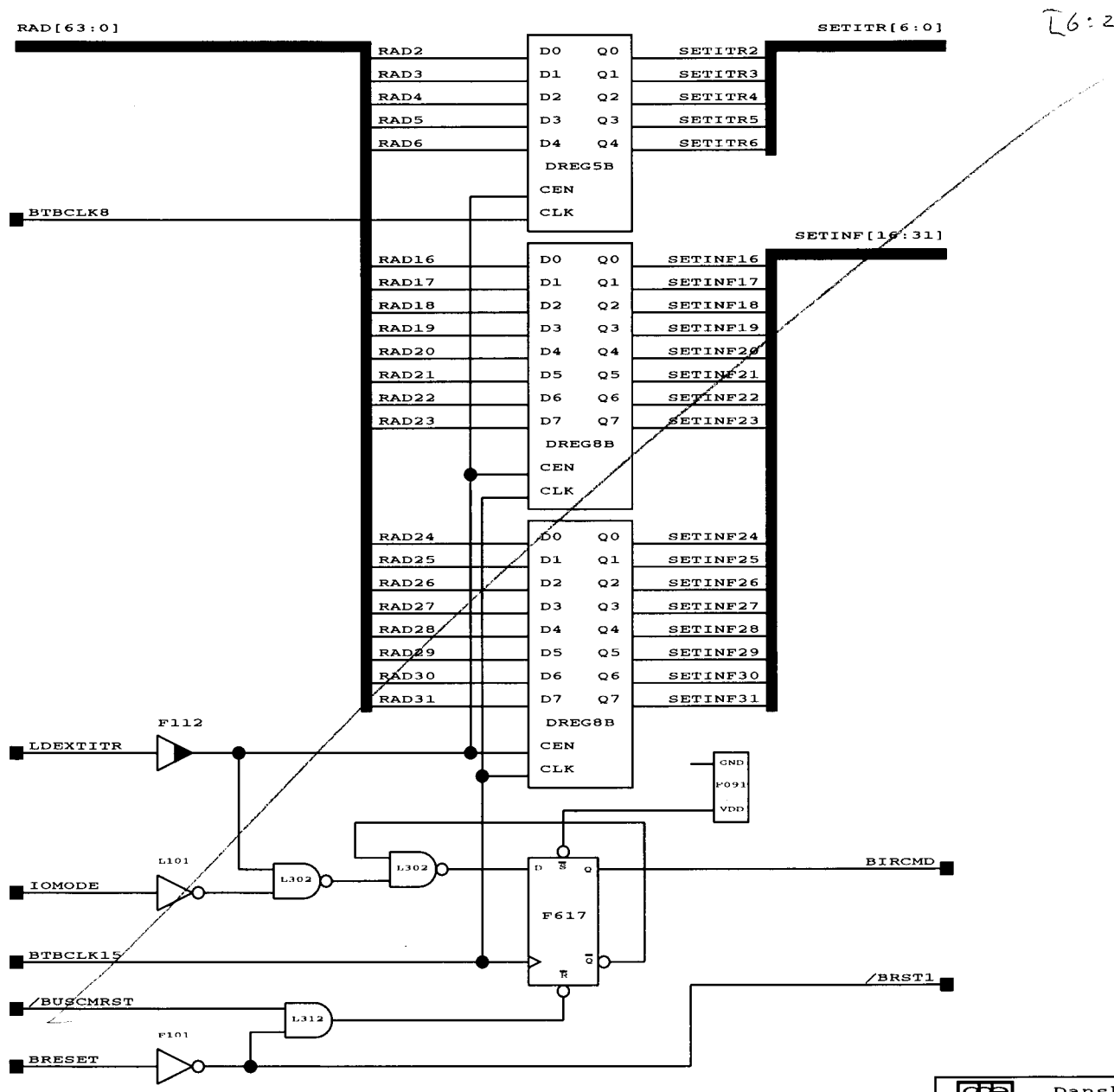
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Processor A/D Buffers	
Issue 1			
Issue 2			
Issue 3		File: cpa.22	Page:22 of NN



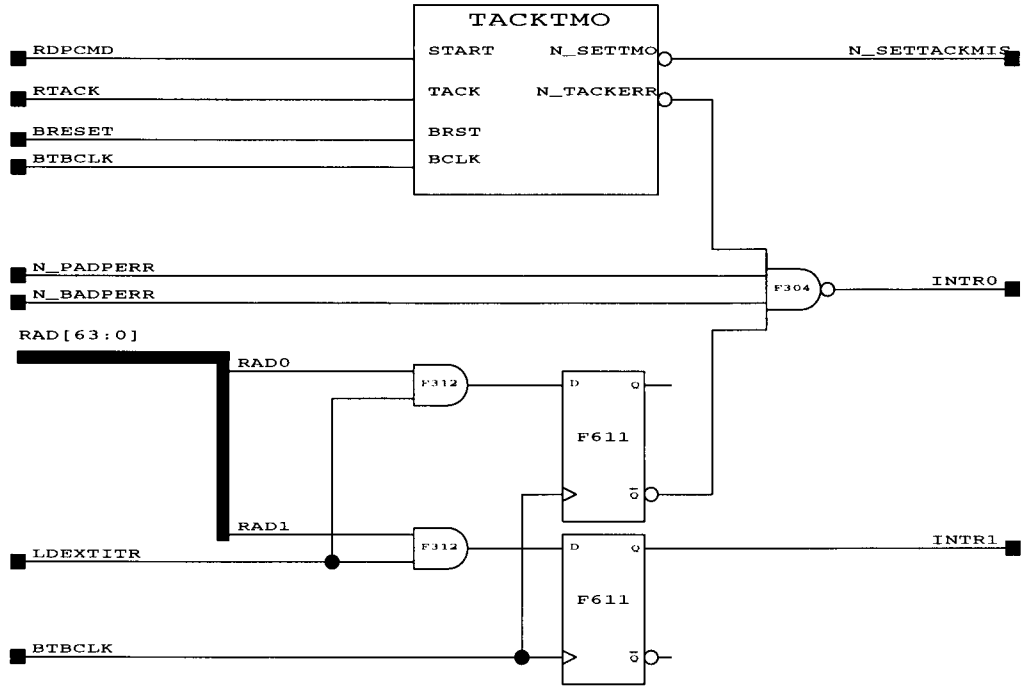
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Control Register	
Issue 1	94-07-11		
Issue 2			
Issue 3		File: cpa.23	Page:23 of NN



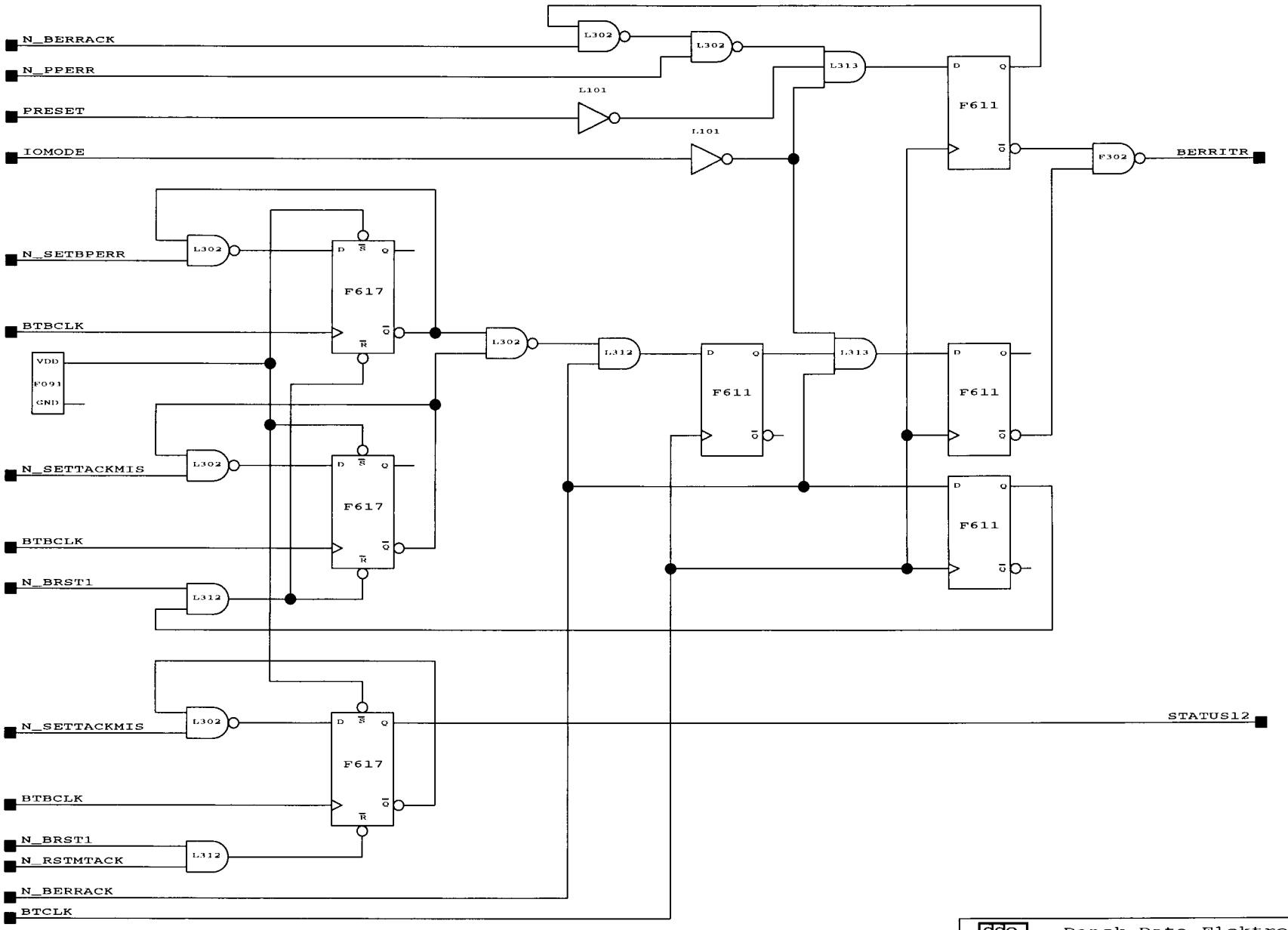
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-16	External Interrupt
Issue 2		
Issue 3		File: cpa.24 Page:24 of NN



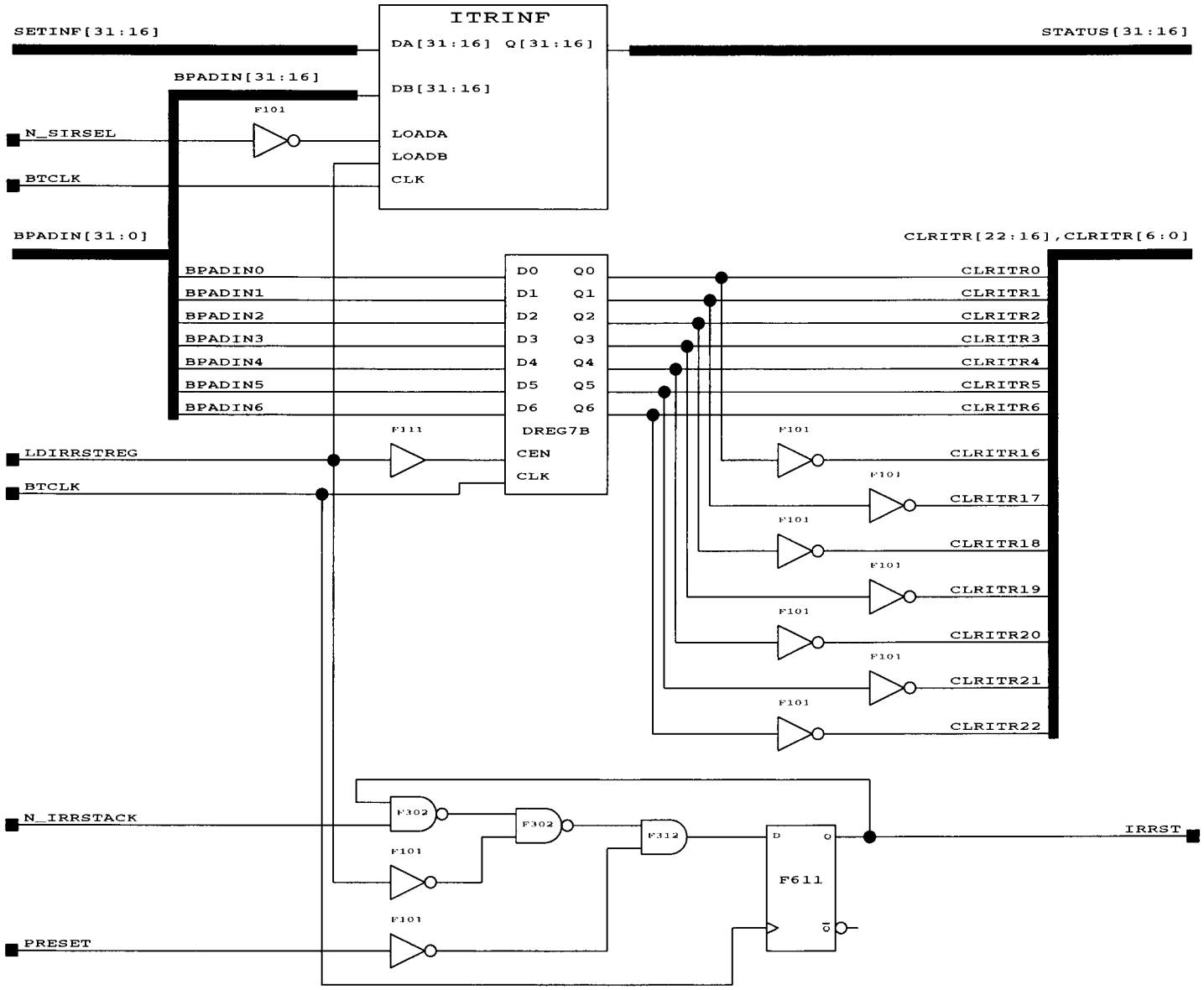
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 External Interrupt	
Issue 1			
Issue 2			
Issue 3		File: cpa.24	Page:24 of NN



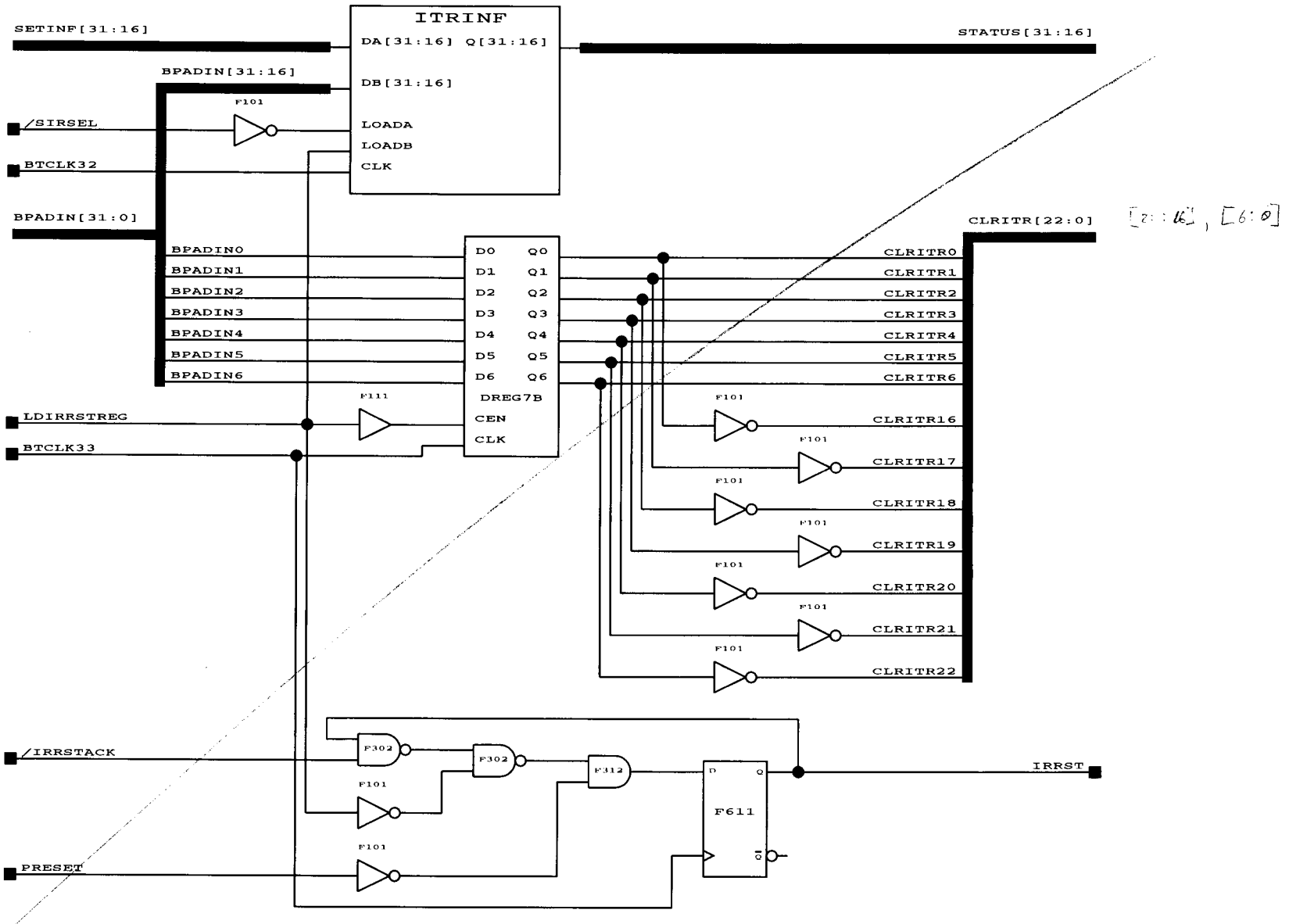
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1		Interrupt Pins INTR0 & INTR1	
Issue 2			
Issue 3		File: cpa.25	Page:25 of NN



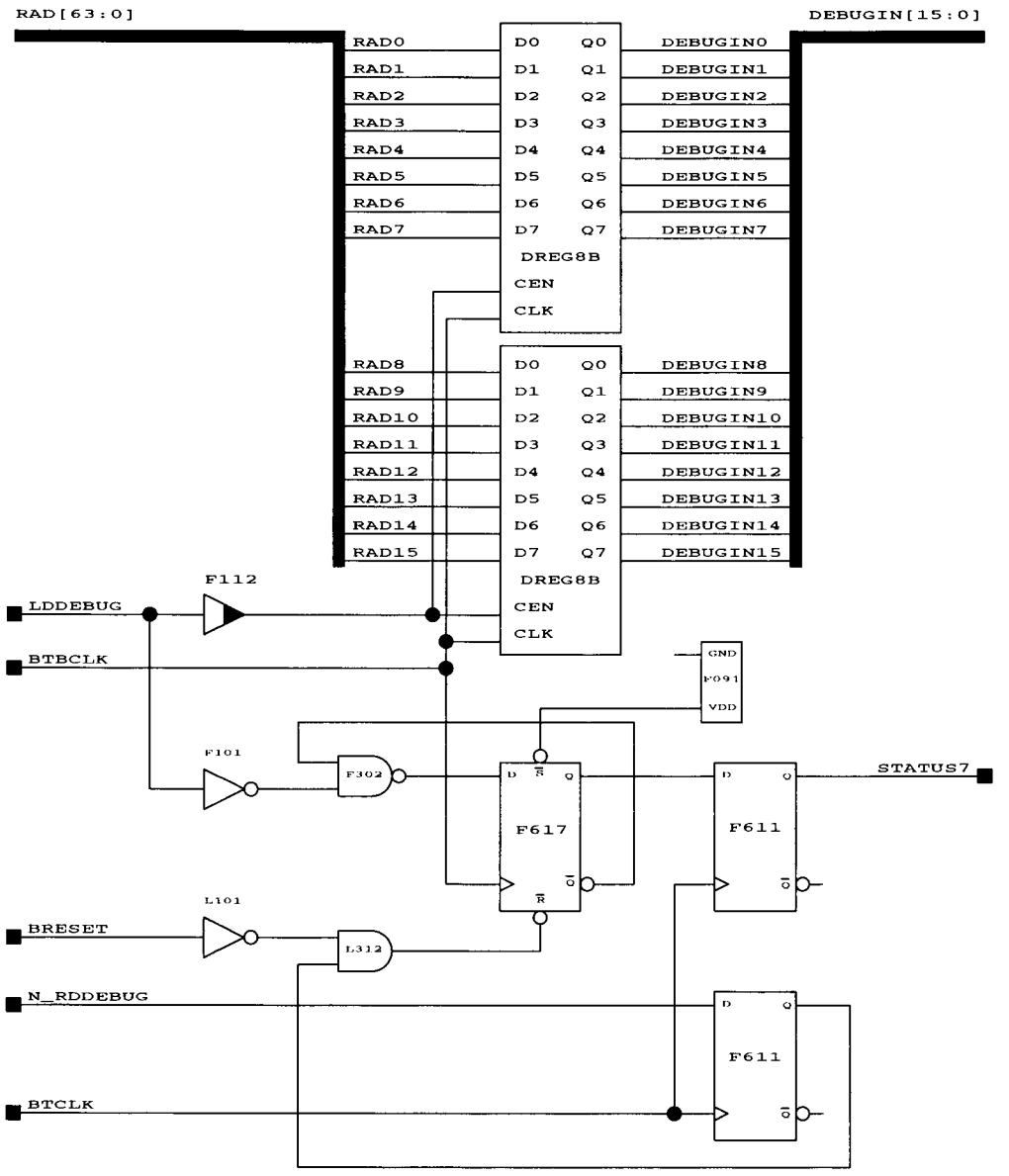
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Bus Error Interrupt	
Issue 1			
Issue 2			
Issue 3		File: cpa.26	Page:26 of NN



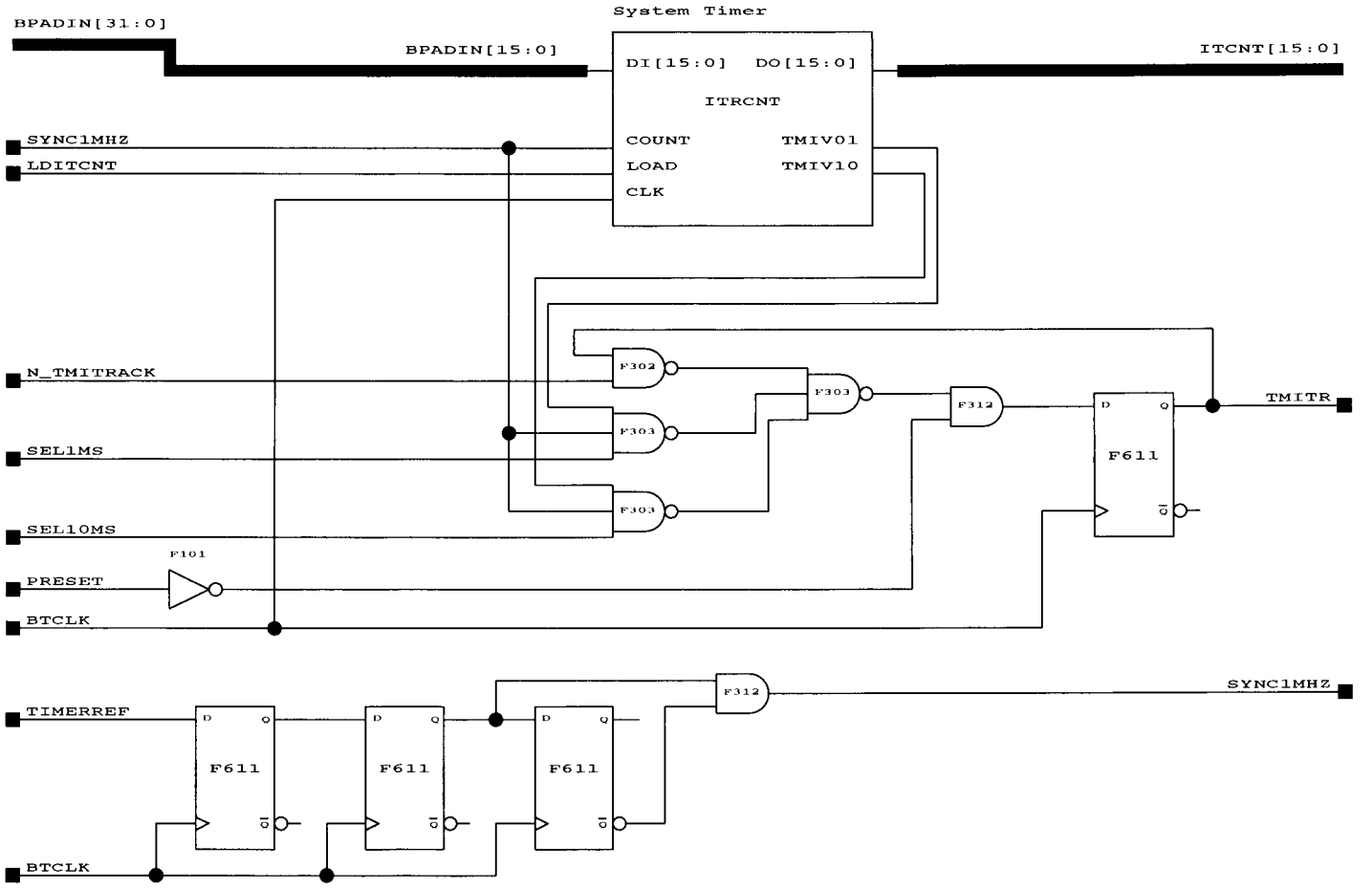
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-16	Interrupt Reset & PE Register
Issue 2		
Issue 3		File: cpa.27 Page:27 of NN



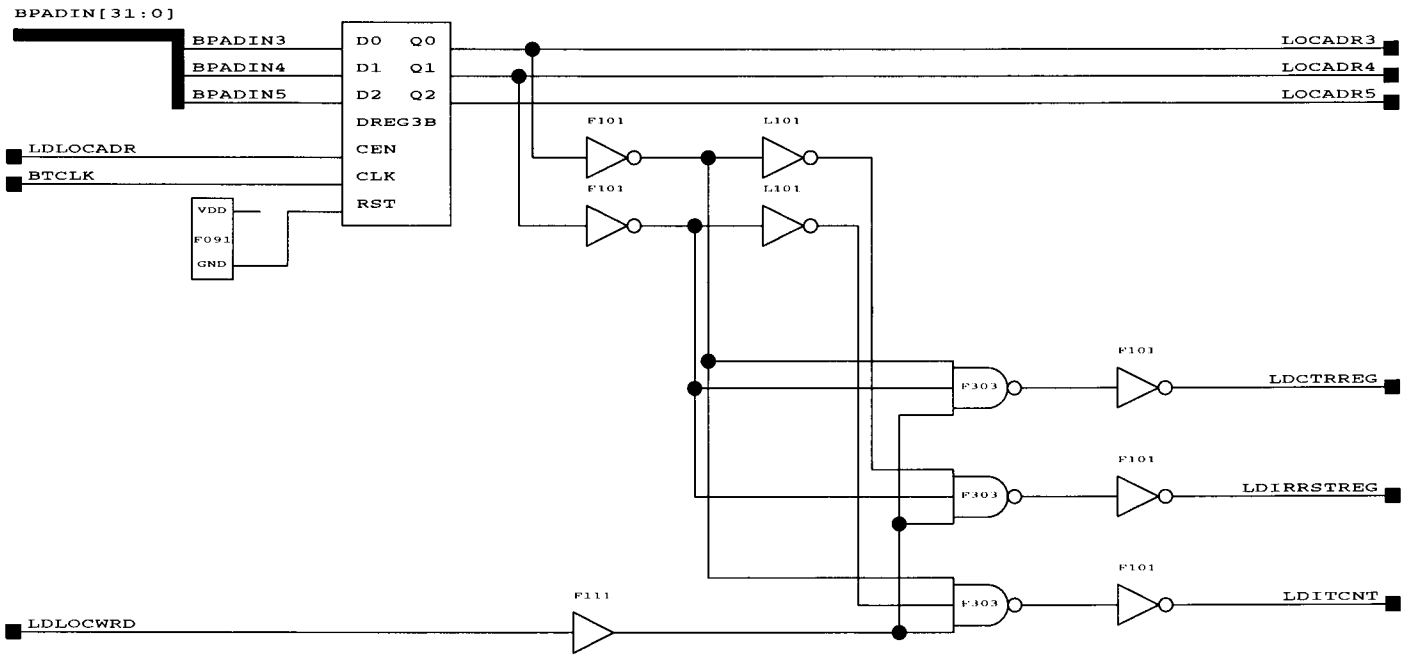
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1		Interrupt Reset & PE Register	
Issue 2			
Issue 3		File: cpa.27	Page:27 of NN



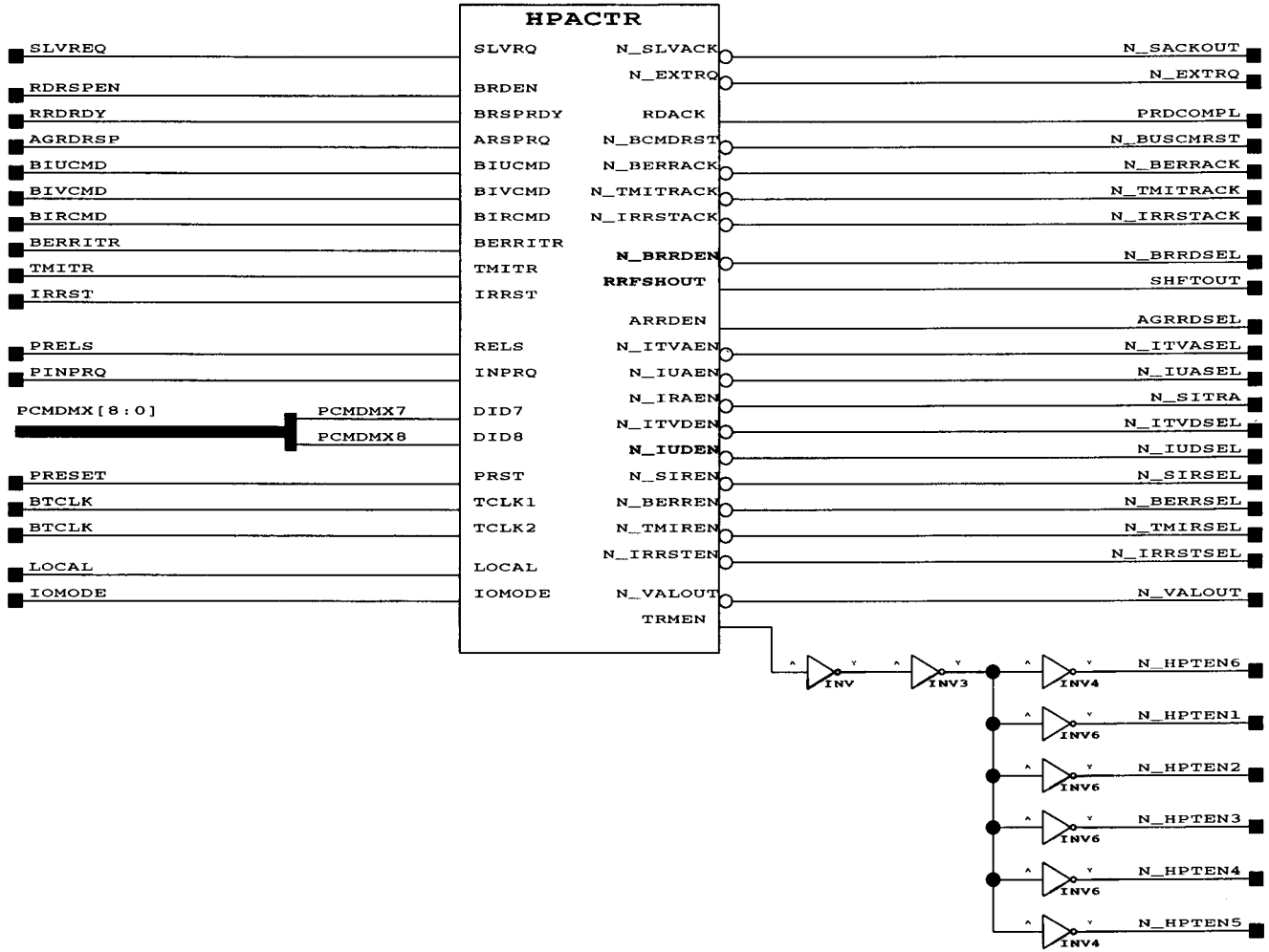
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Debug Input Register
Issue 2		
Issue 3		File: cpa.28 Page:28 of NN



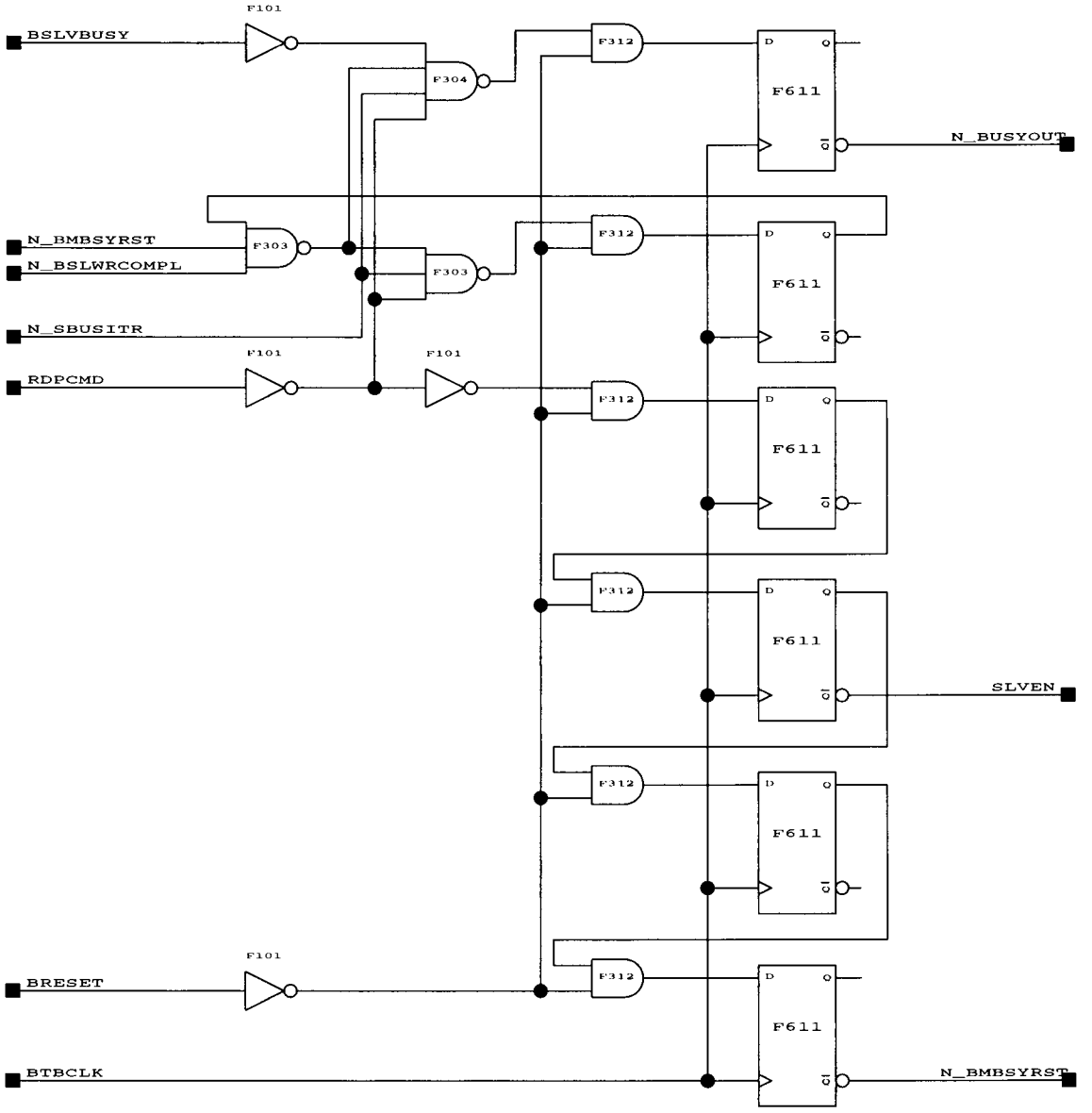
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-05-31	1/10 MS Interval Timer
Issue 2		
Issue 3		File: cpa.29 Page:29 of NN



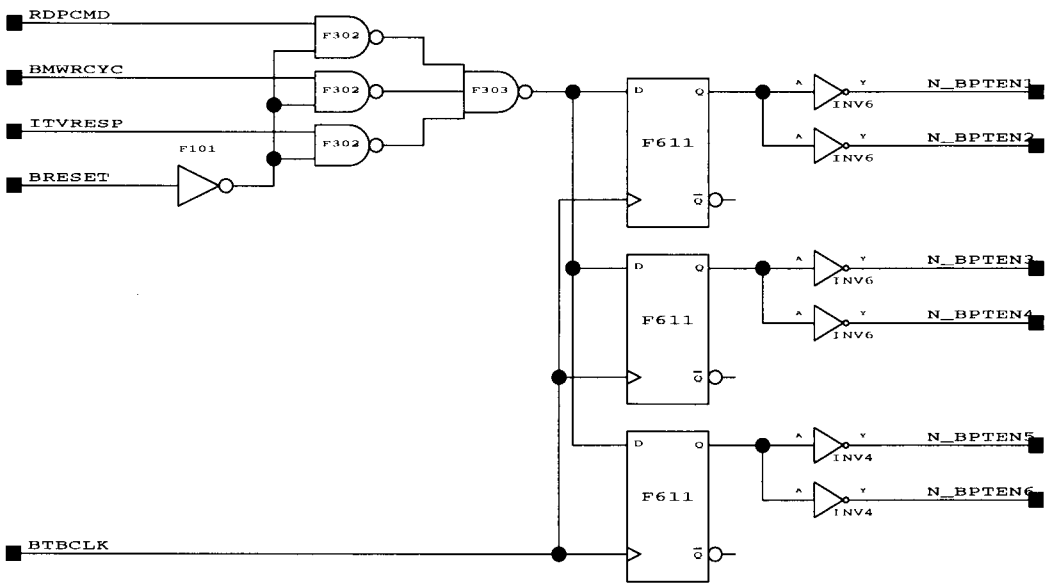
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302 Local Write Addr Decoding
Issue 1		
Issue 2		
Issue 3		File: cpa.30 Page:30 of NN



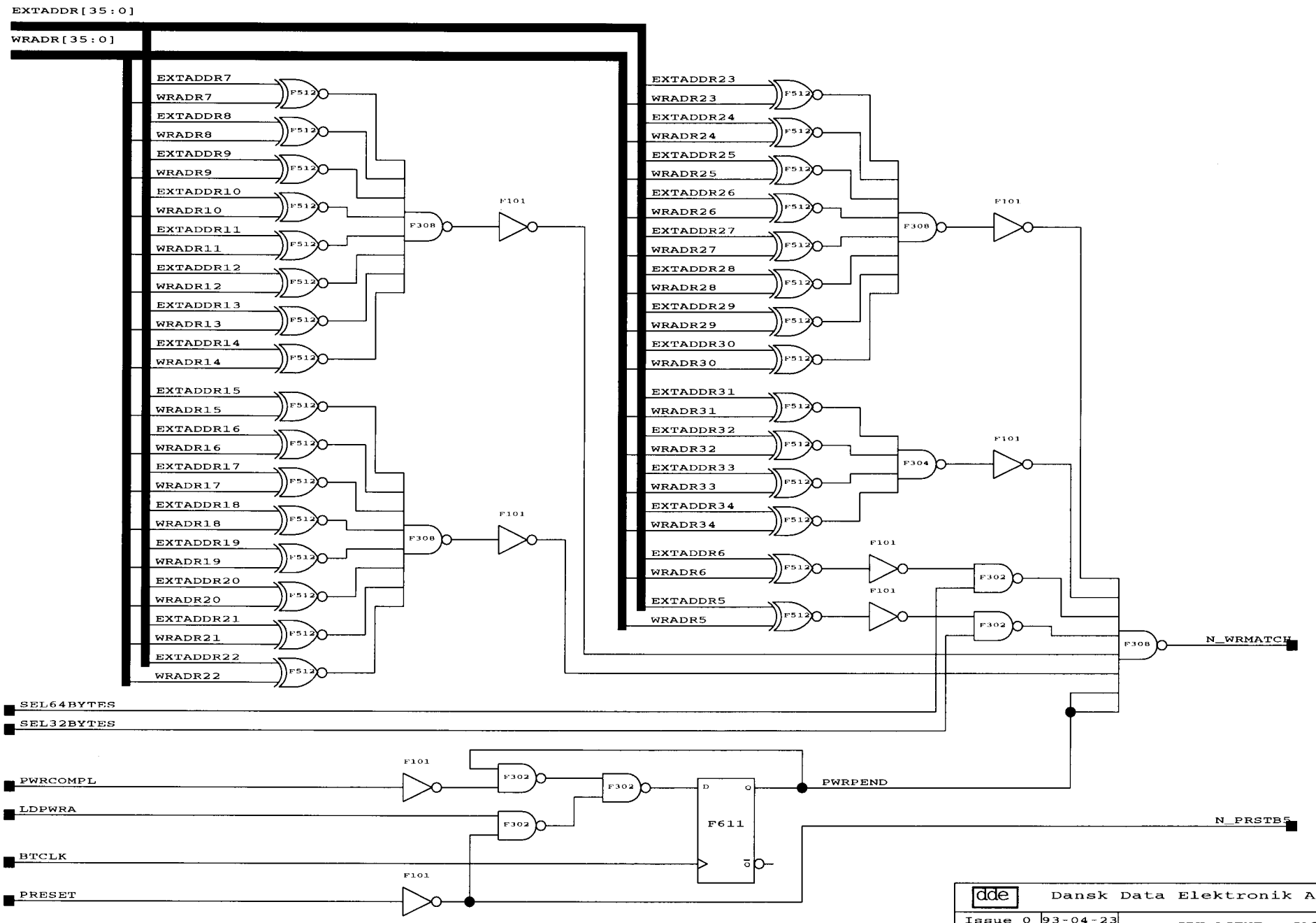
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-08	Host Port Access Control
Issue 2		
Issue 3		File: cpa.31 Page:31 of NN



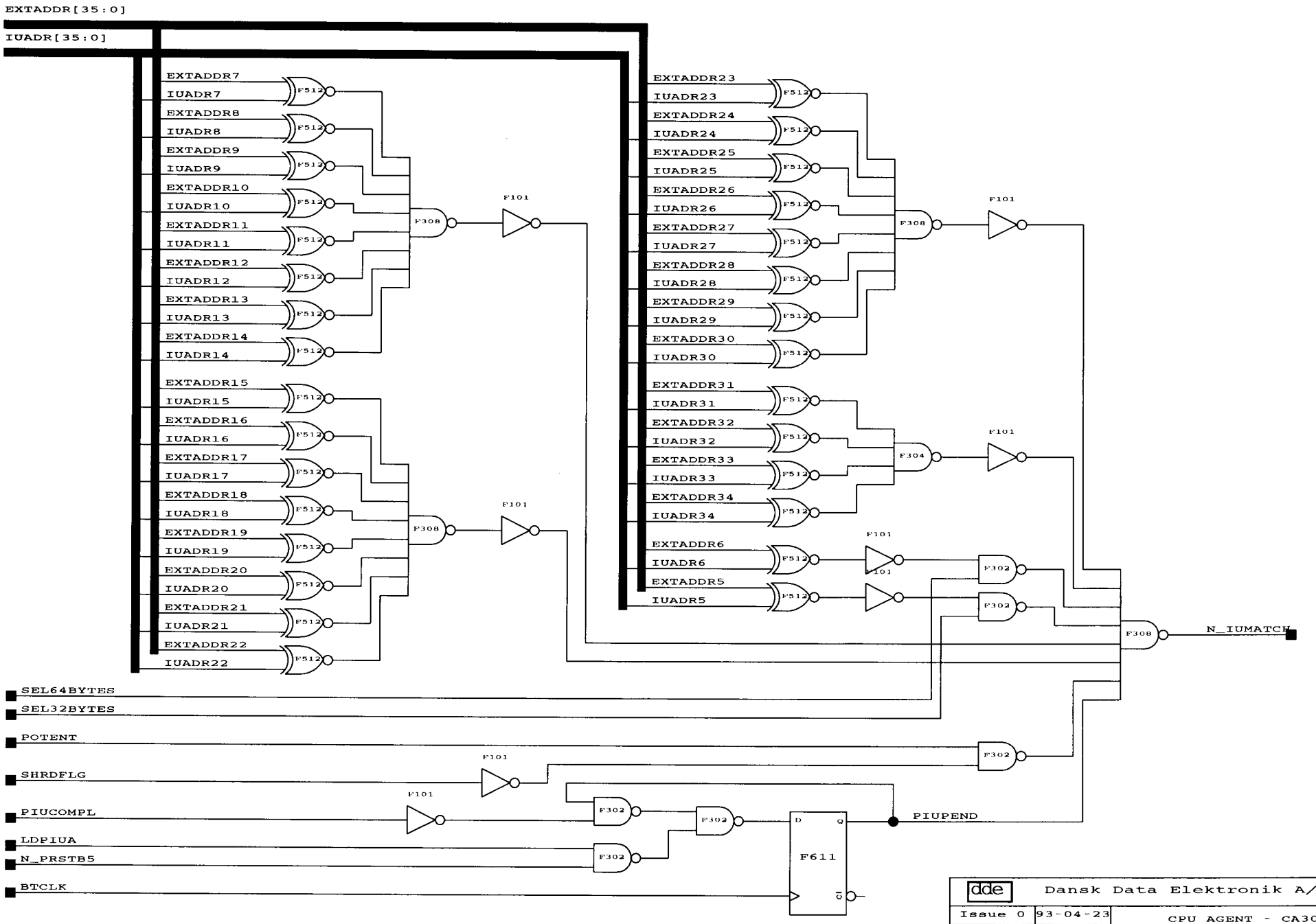
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Busy Out Control - BSYCTRL
Issue 2		
Issue 3		File: cpa.32 Page:32 of NN



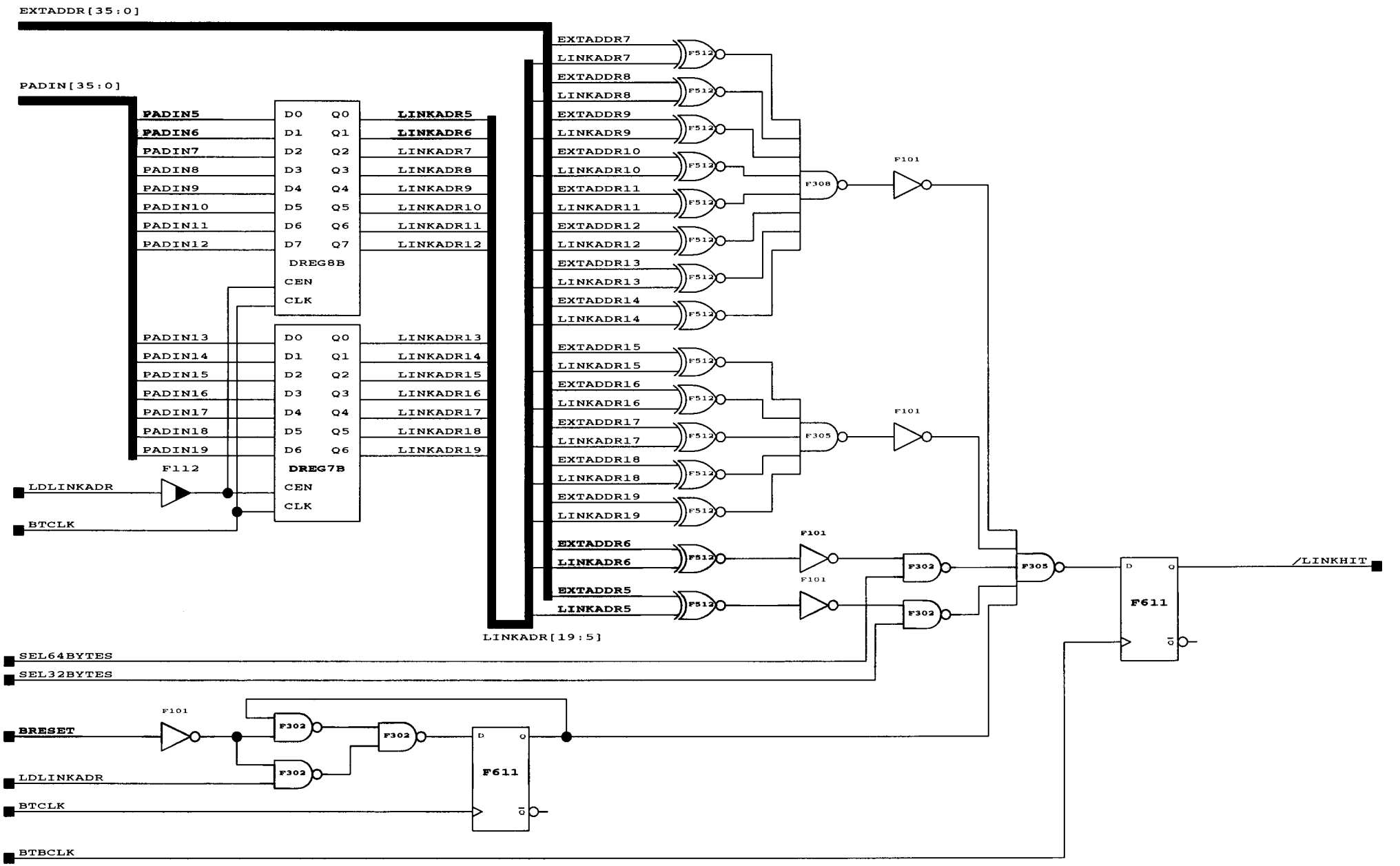
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-15	System Bus Transcv. Control
Issue 2		
Issue 3		File: cpa.33 Page:33 of NN



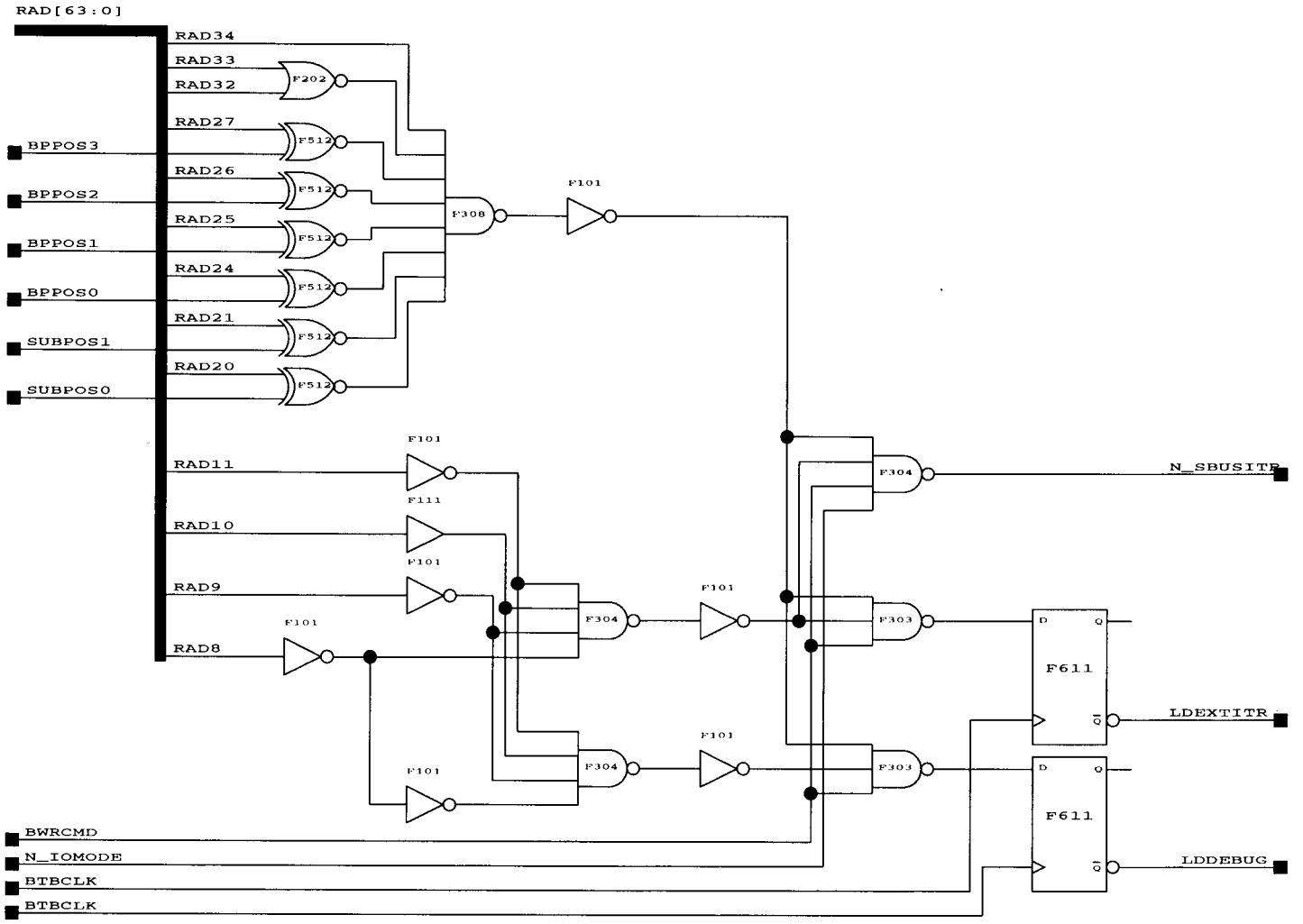
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-11	Write Address Comperator
Issue 2		
Issue 3		File: cpa.34 Page: 34 of NN



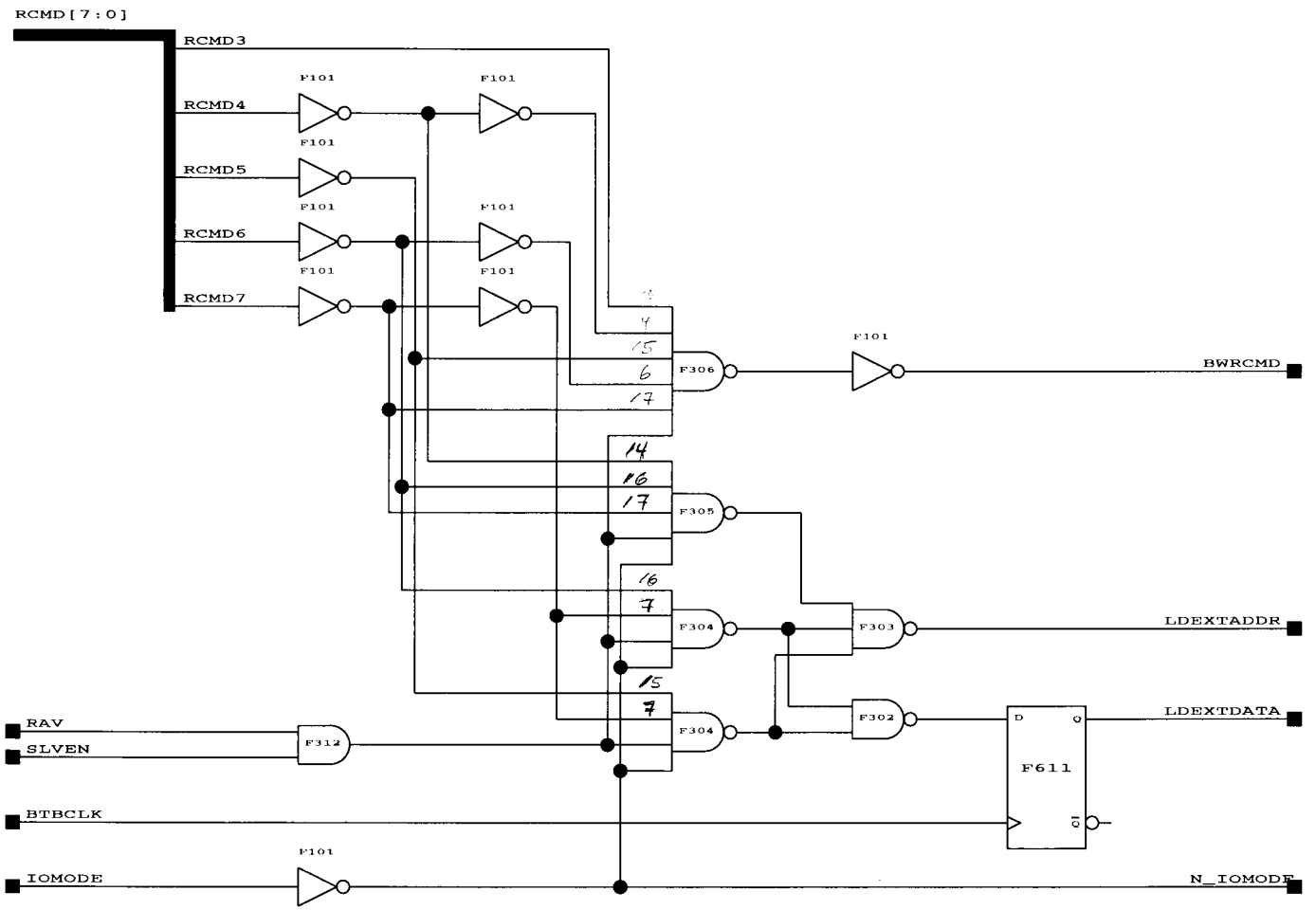
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1	94-07-11	I/U Address Comperator	
Issue 2			
Issue 3		File: cpa.35	Page:35 of NN



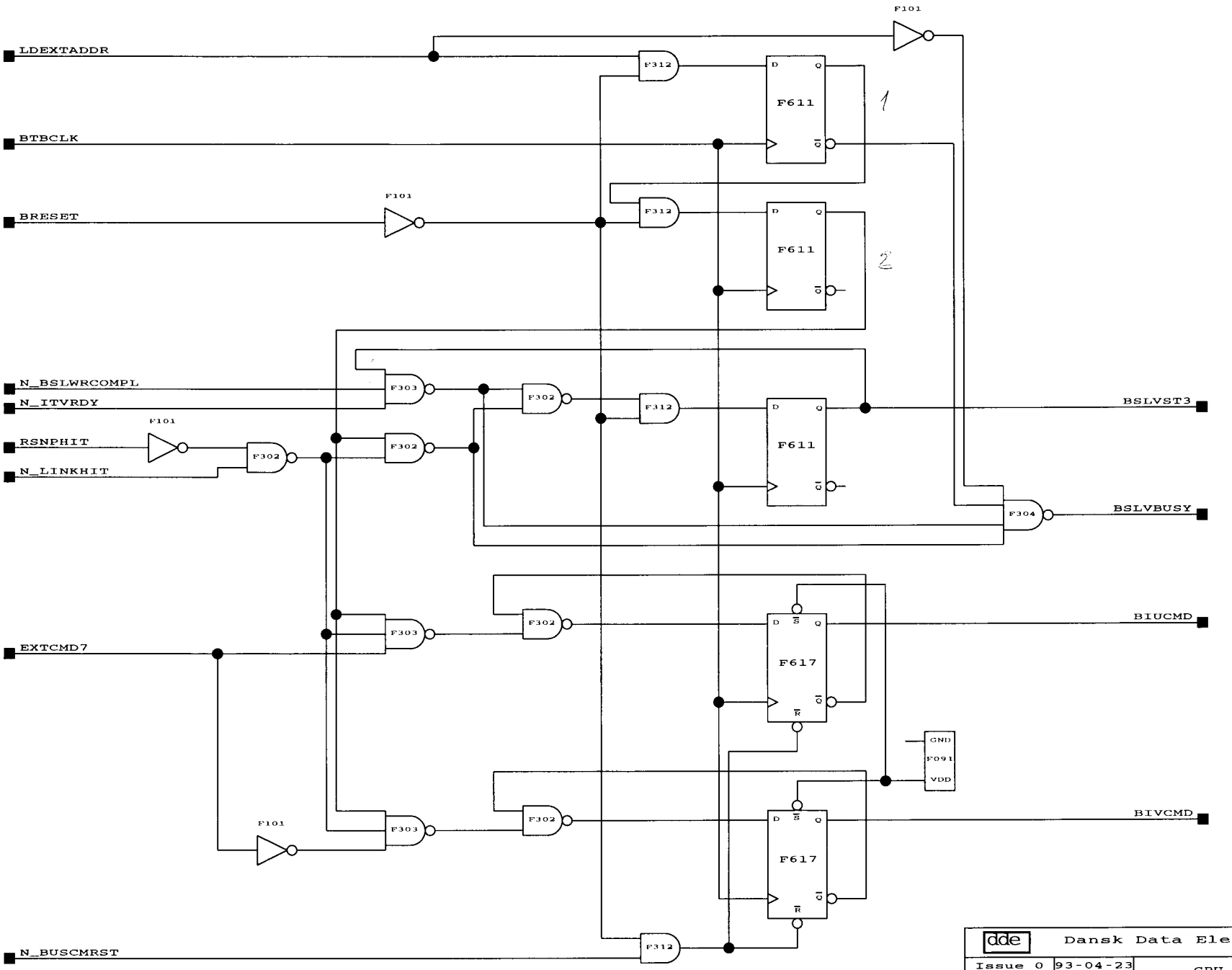
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-27	Link Address Snooper
Issue 2		
Issue 3		File: cpa.36 Page:36 of NN



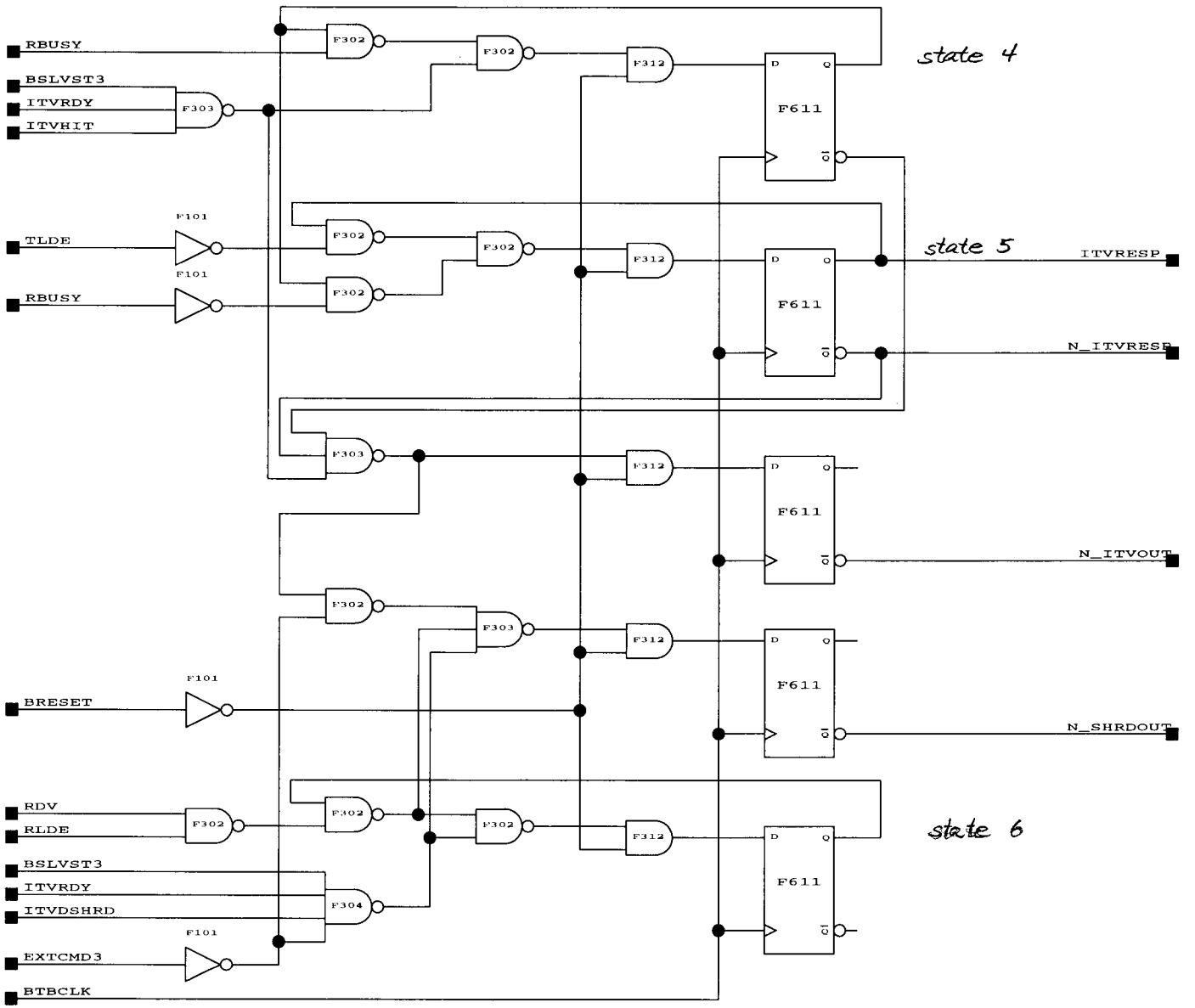
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1		Slave Address Decoding	
Issue 2			
Issue 3		File: cpa.37	Page:37 of NN



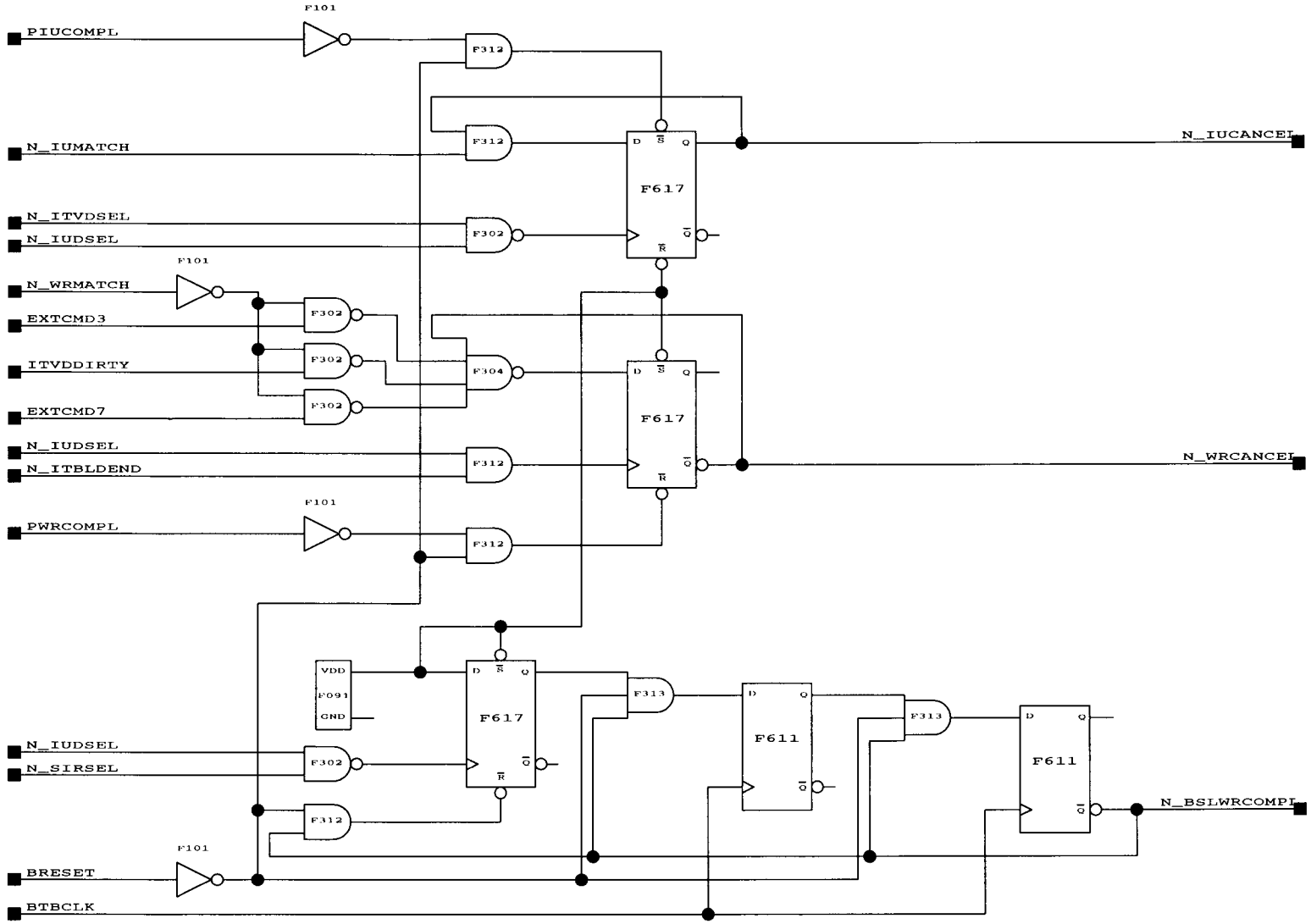
dde Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		System Bus Command Decoding
Issue 2		
Issue 3		File: cpa.38 Page:38 of NN



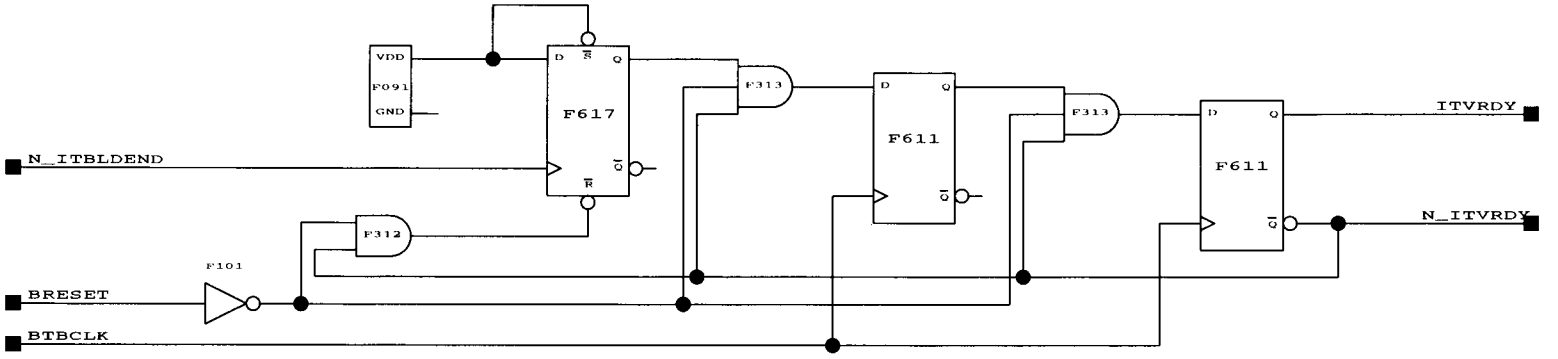
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-11	Bus Implicit Slave Control
Issue 2		
Issue 3		File: cpa.39 Page: 39 of NN



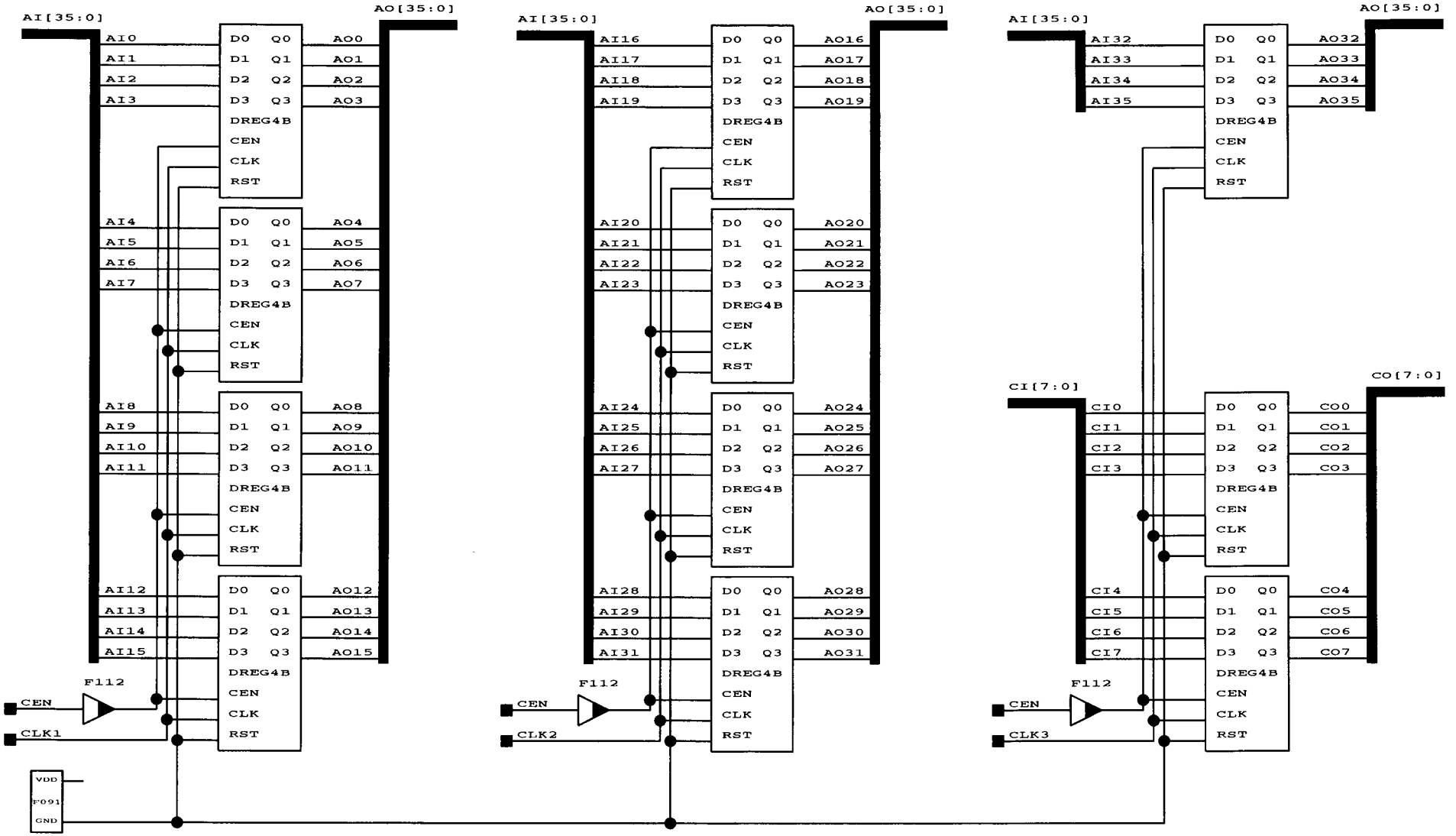
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1		Bus Implicit Slave Control	
Issue 2			
Issue 3		File: cpa.40	Page:40 of NN



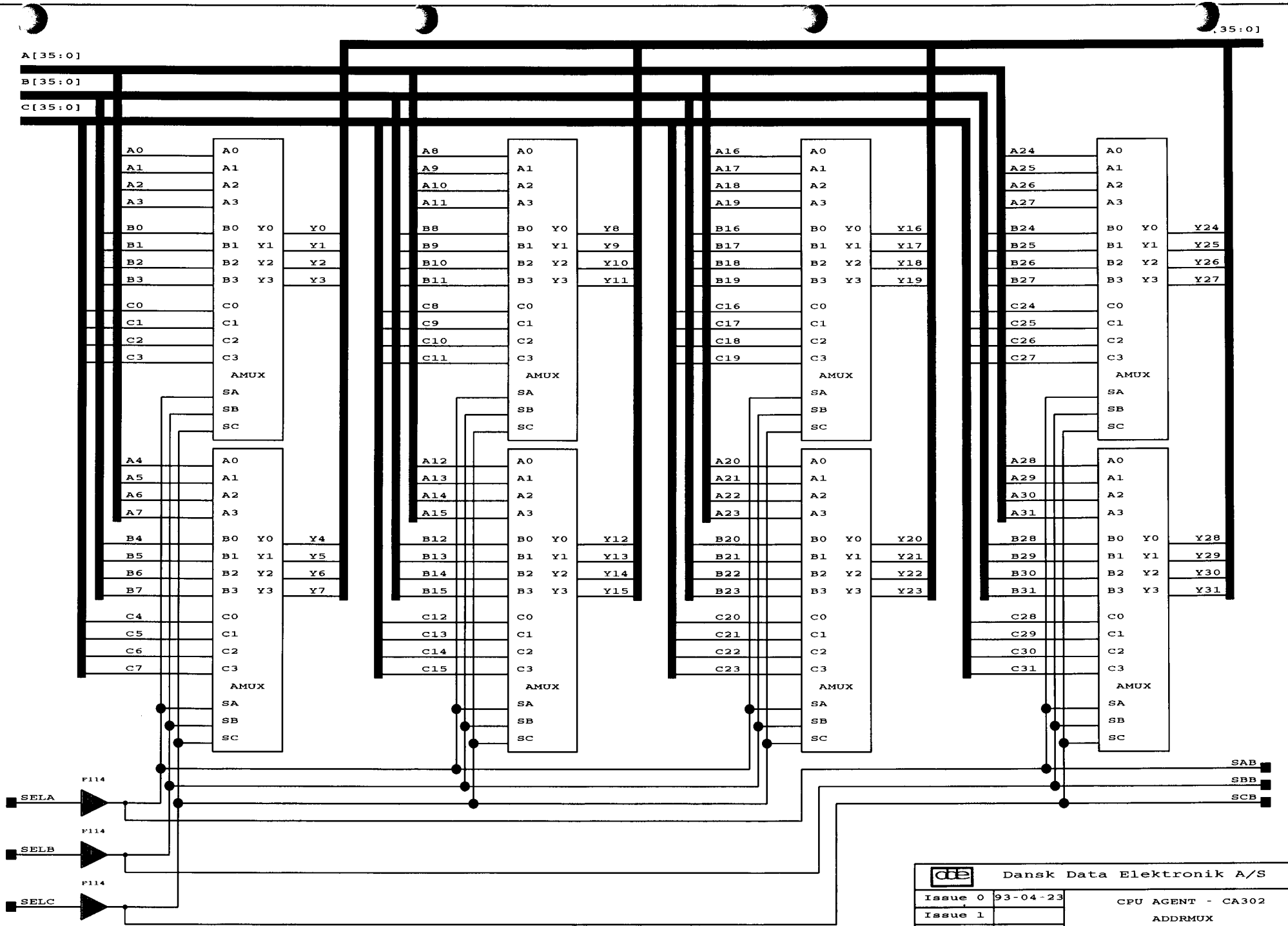
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1	94-05-10	Bus I/U Command Termination	
Issue 2			
Issue 3		File: cpa.41	Page:41 of NN



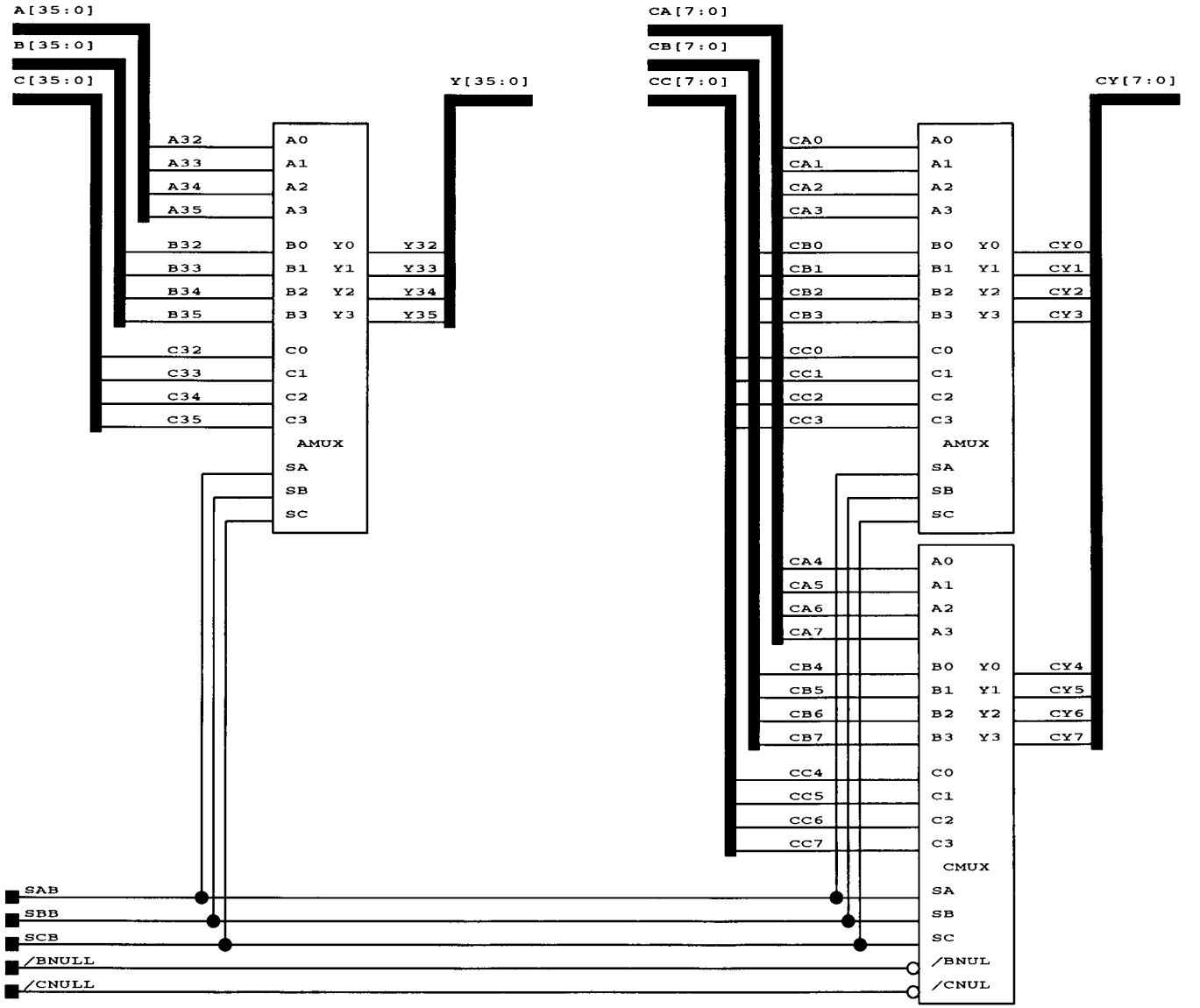
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Bus Intervention Termination
Issue 2		
Issue 3		File: cpa.42 Page:42 of NN



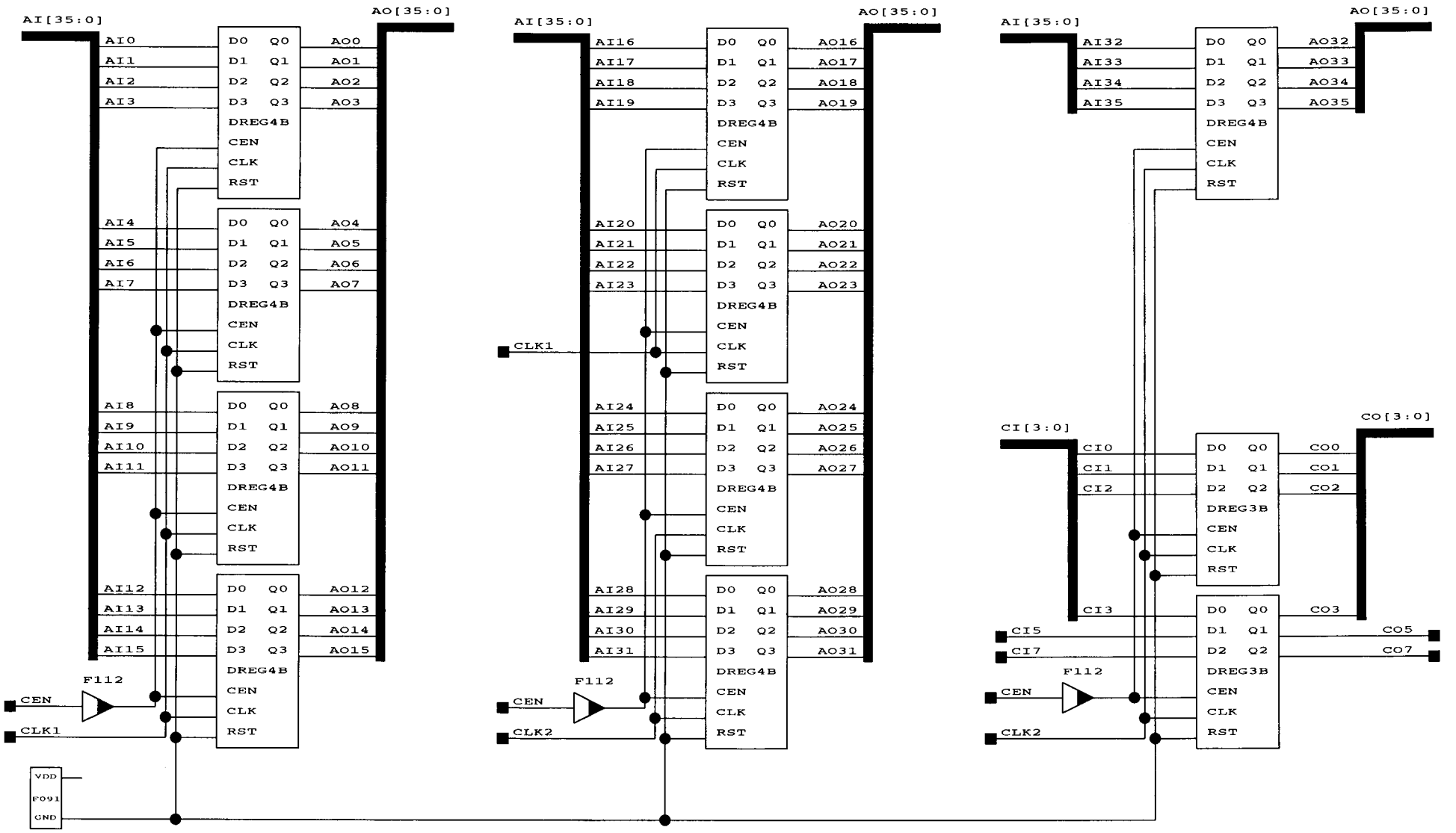
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		ADDRBUF
Issue 2		
Issue 3		File: addrbuf.1 Page: 1 of 1



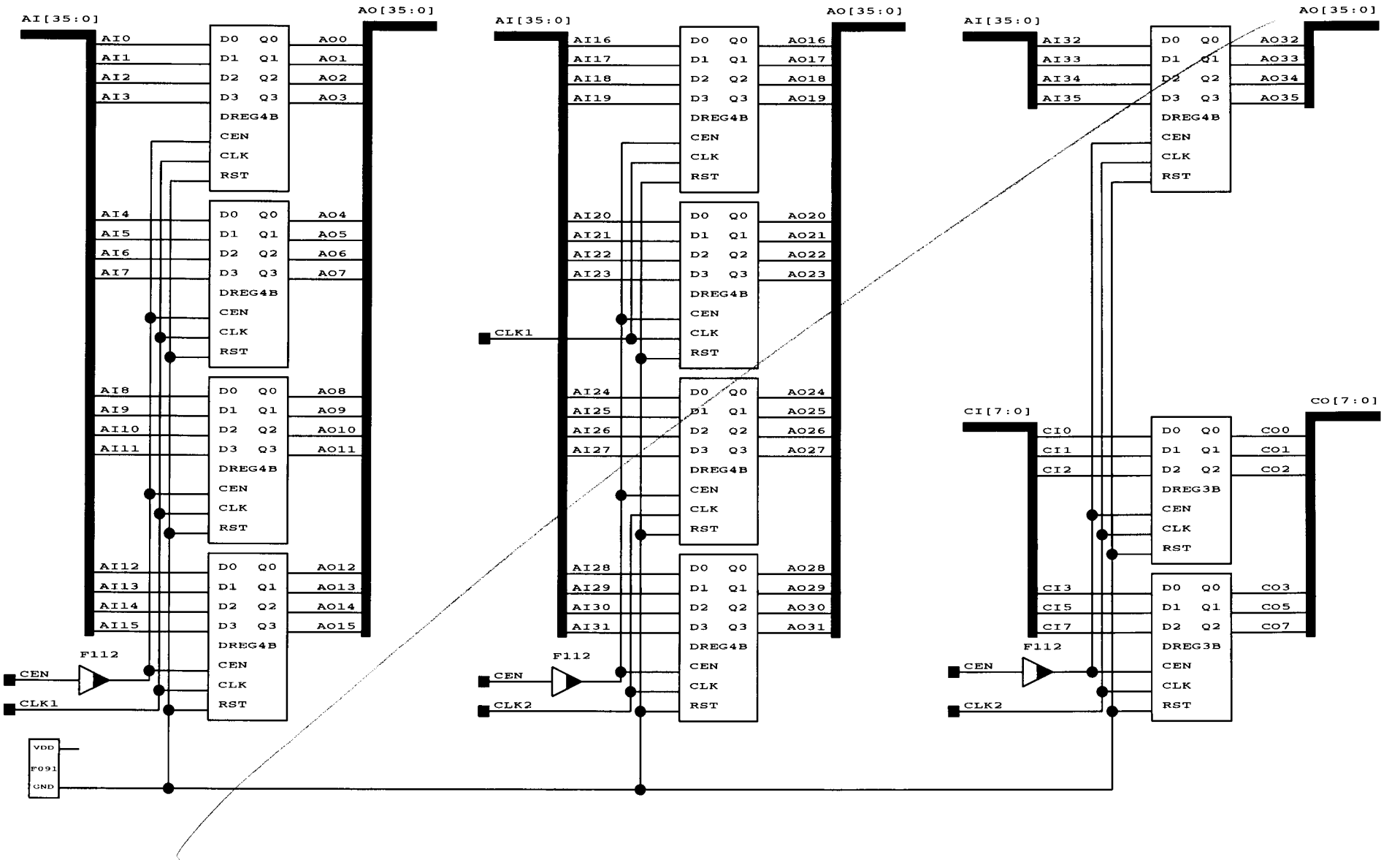
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		ADDRMUX
Issue 2		
Issue 3		File: addrmux.1 Page: 1 of 2



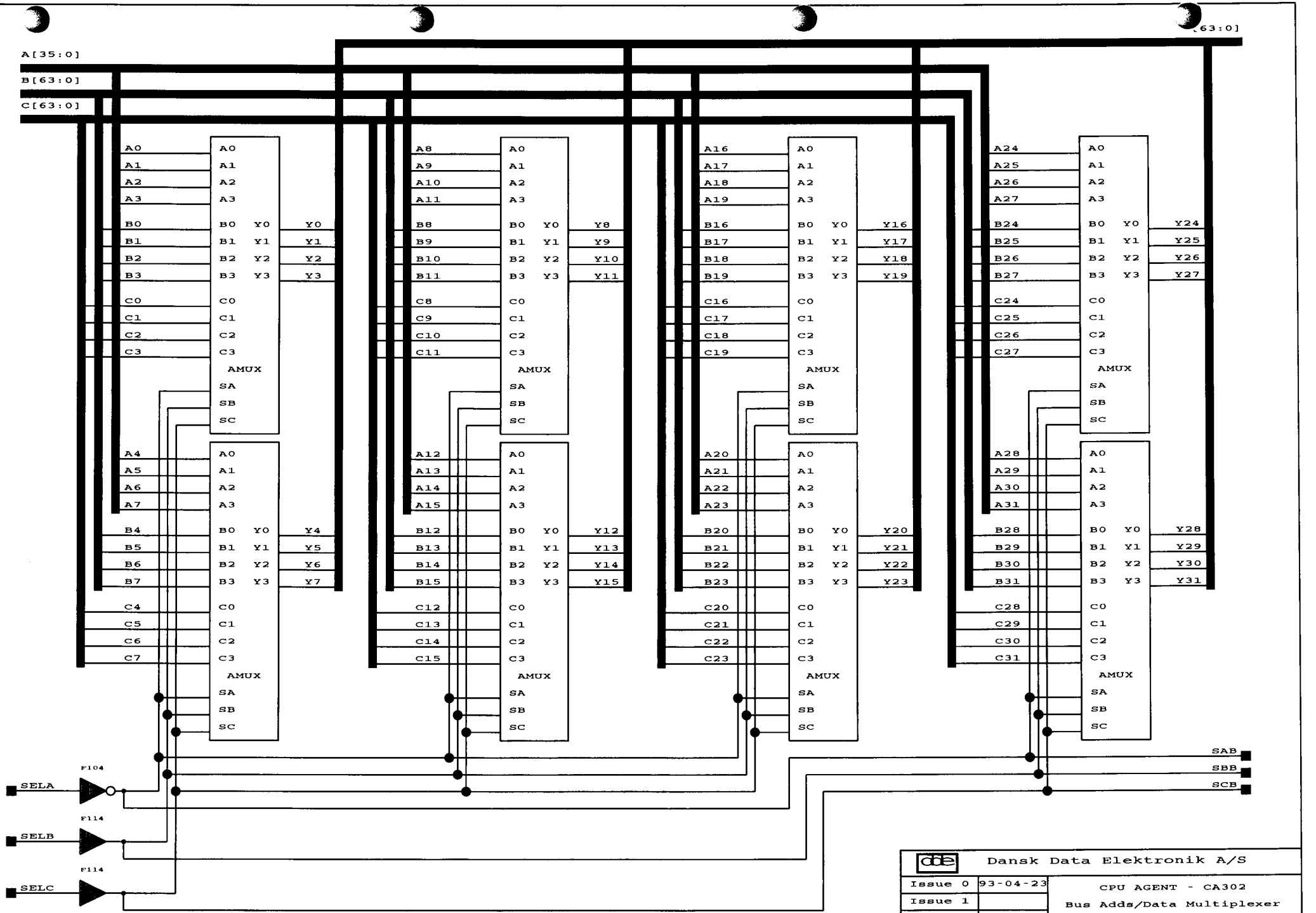
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 ADDRMUX	
Issue 1			
Issue 2			
Issue 3		File: addrmux.2	Page: 2 of 2

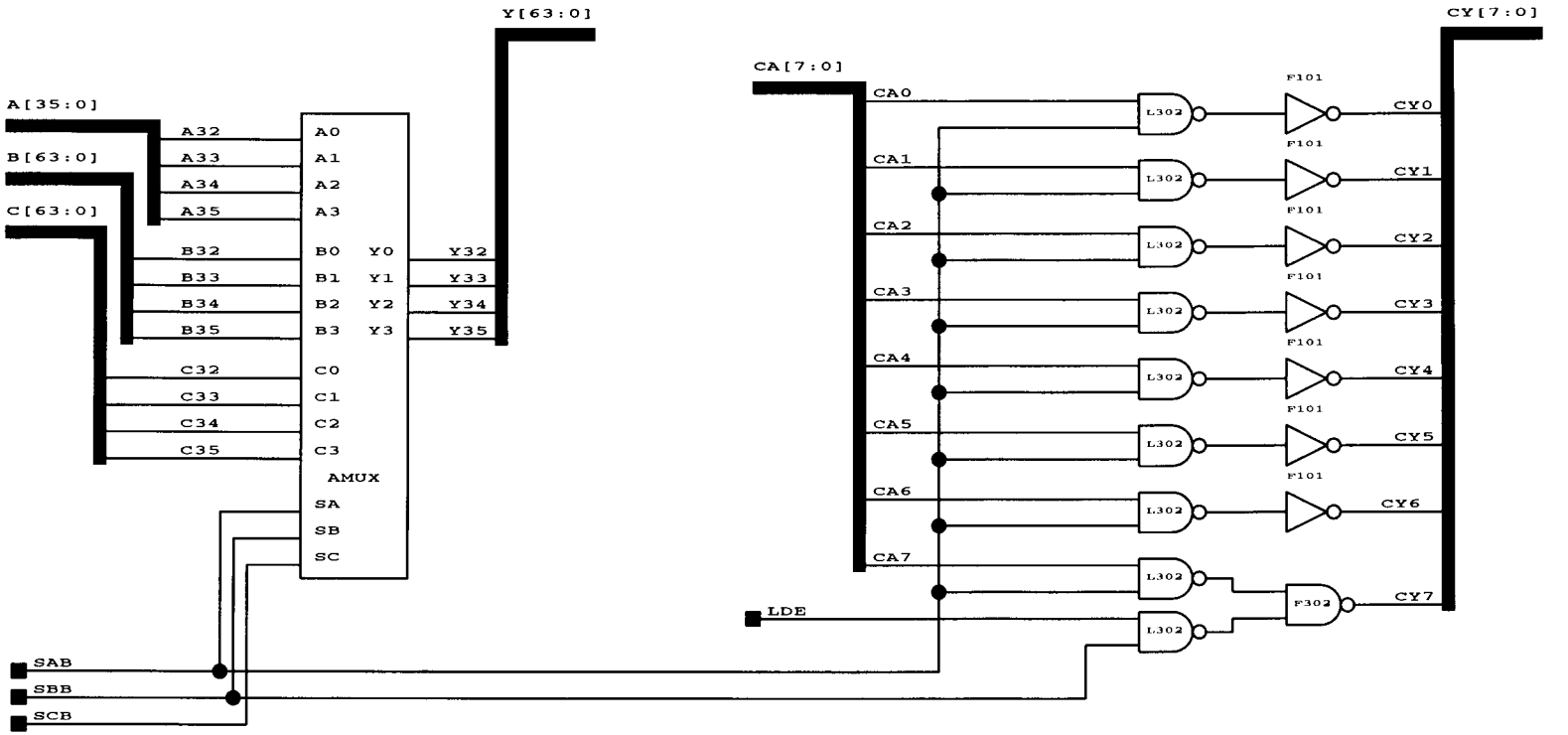


dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-16	ADDRREG
Issue 2		
Issue 3		File: addrreg.1 Page: 1 of 1

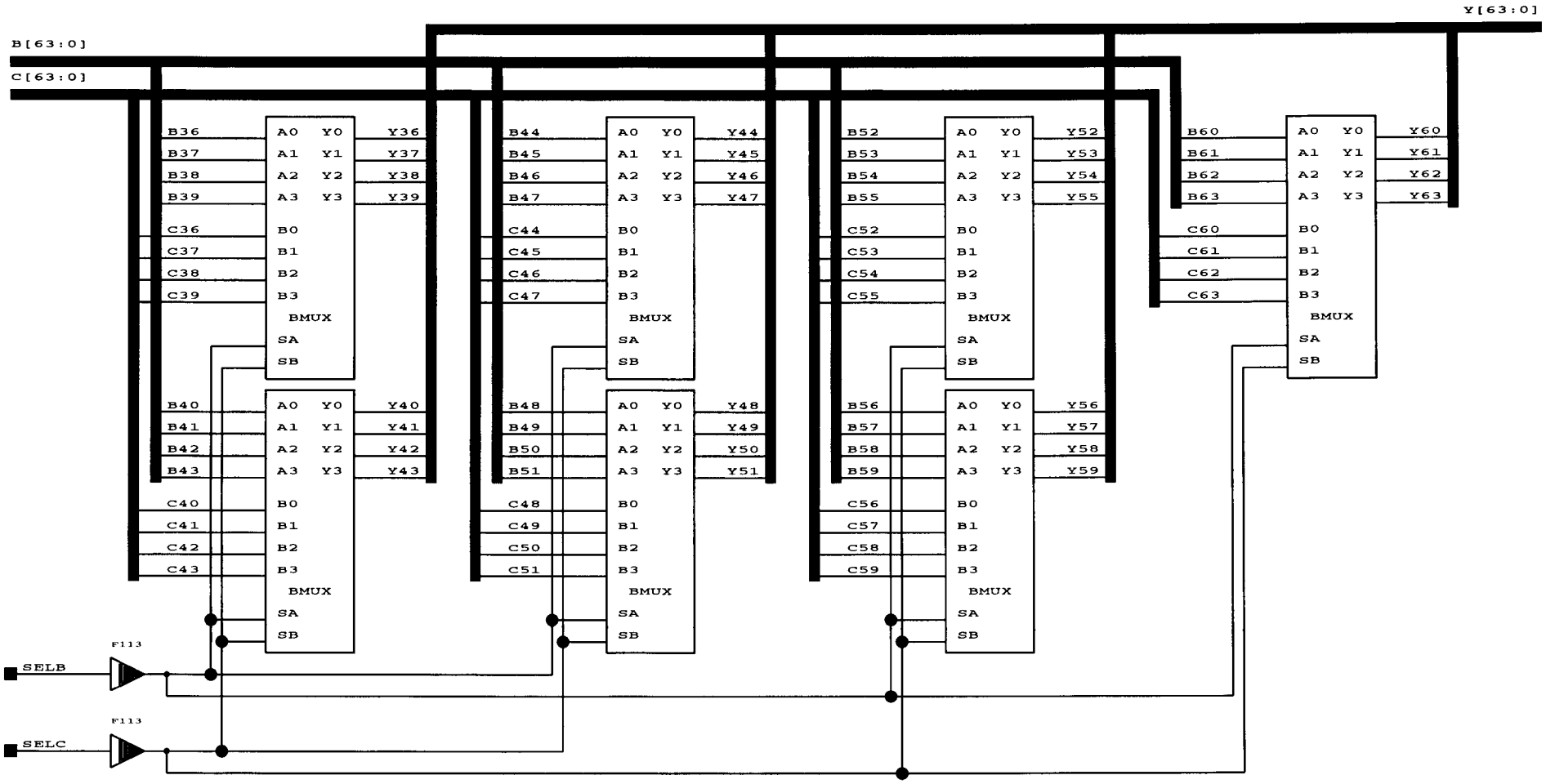


Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 ADDRREG	
Issue 1			
Issue 2			
Issue 3		File: addrreg.1	Page: 1 of 1

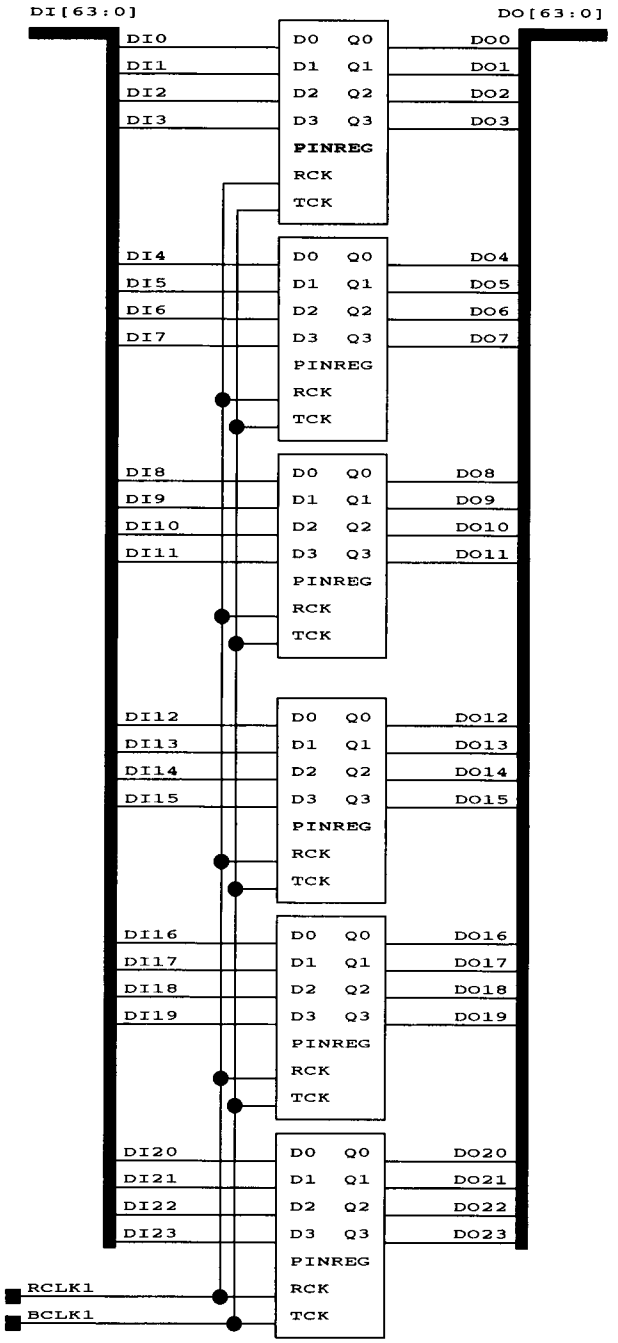

A[35:0]
B[63:0]
C[63:0]
AMUX
SELA
SELB
SELC
F104
F114
F114
SAB
SBB
SCB
Dansk Data Elektronik A/S
Issue 0 93-04-23
Issue 1
Issue 2
Issue 3
CPU AGENT - CA302
Bus Adds/Data Multiplexer
File: admux.1
Page: 1 of 3

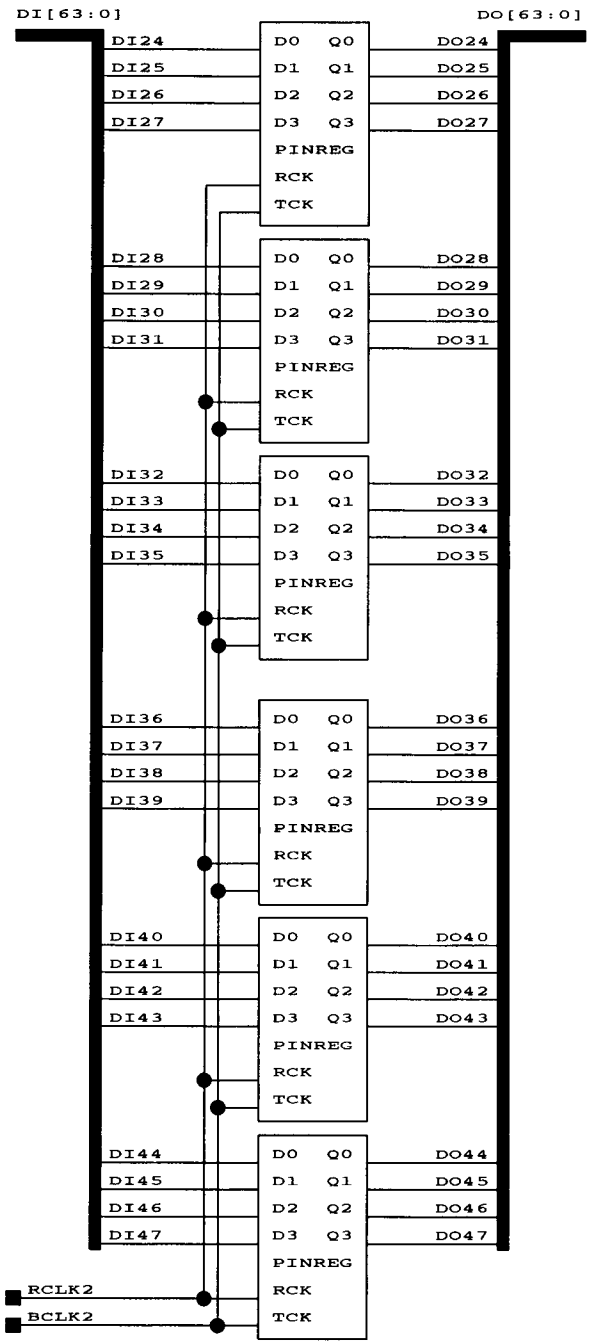


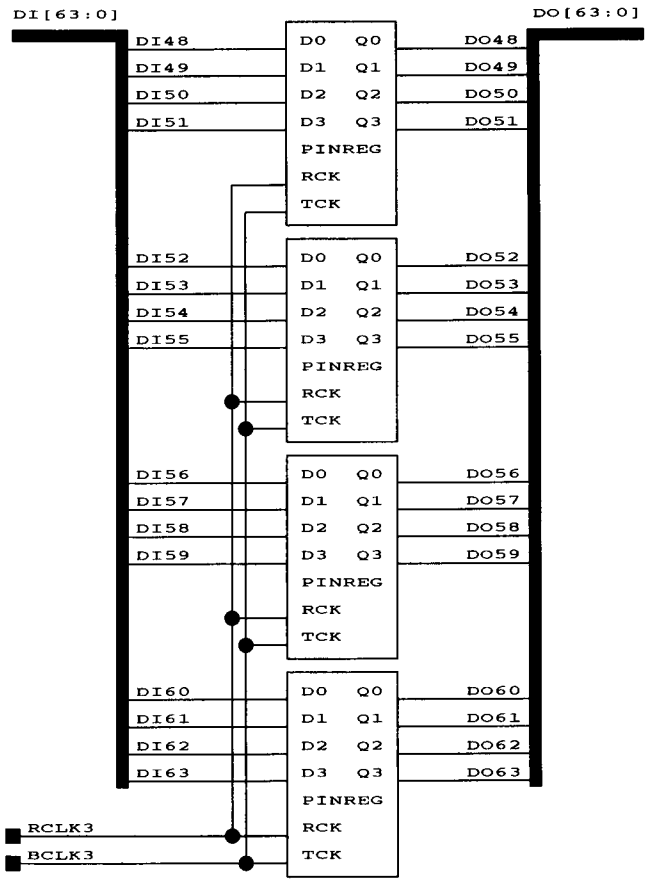
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Bus Addr/Data Multiplexer	
Issue 1			
Issue 2			
Issue 3		File: admux.2	Page: 2 of 3



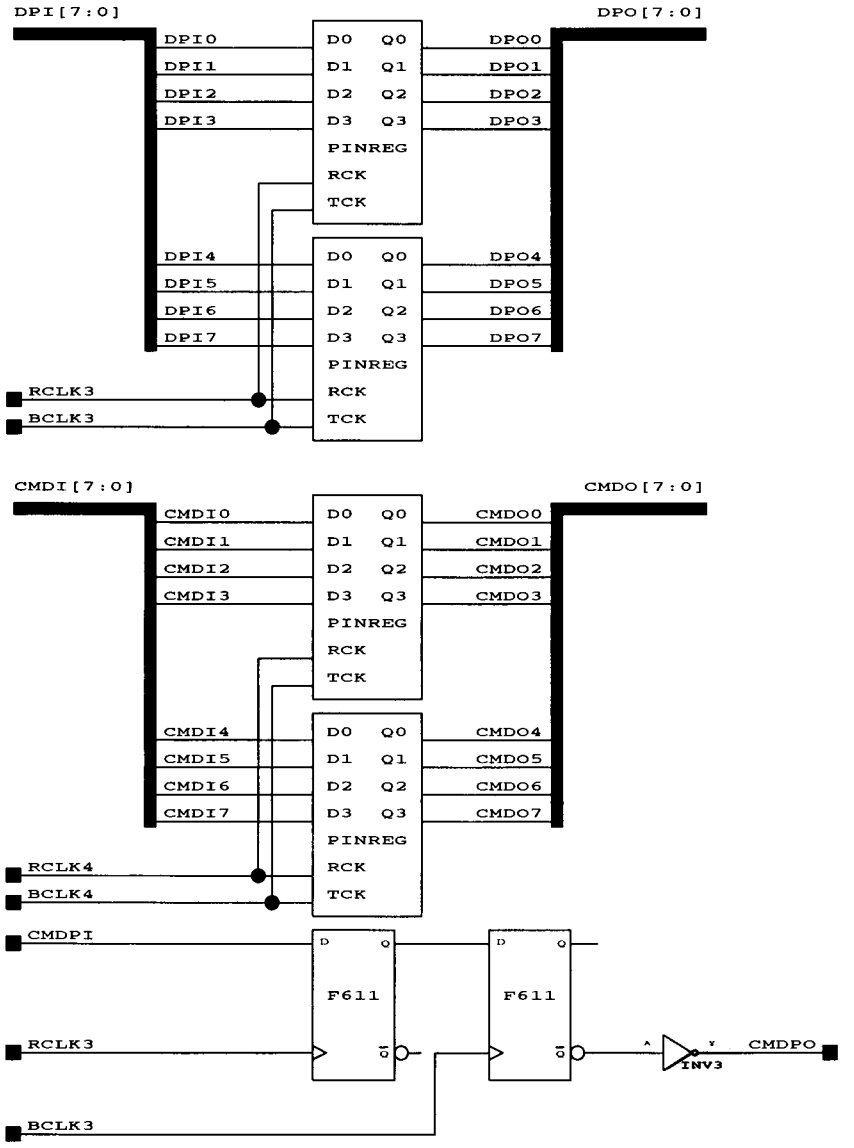
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Bus Addr/Data Multiplexer
Issue 2		
Issue 3		File: admux.3 Page: 3 of 3



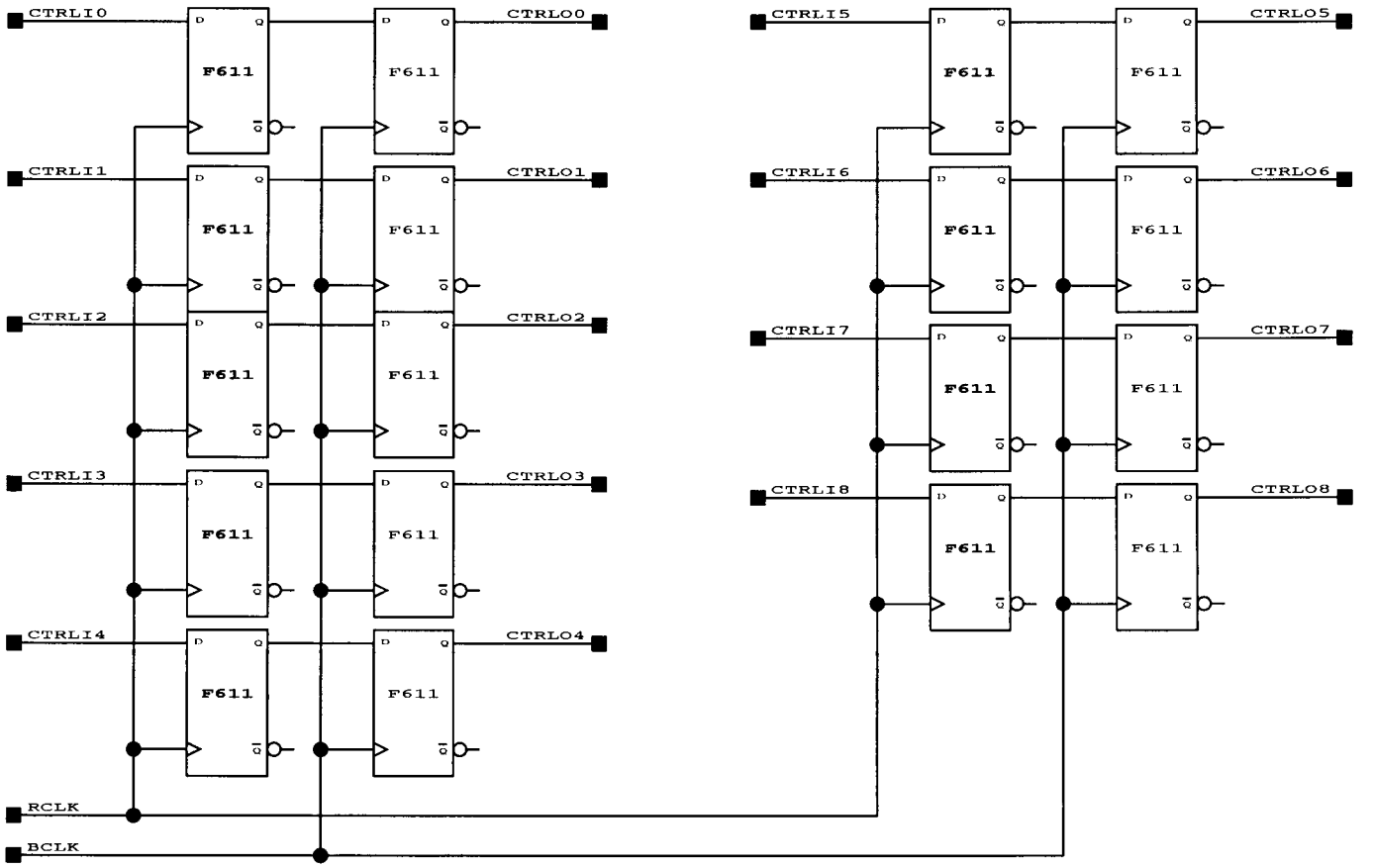




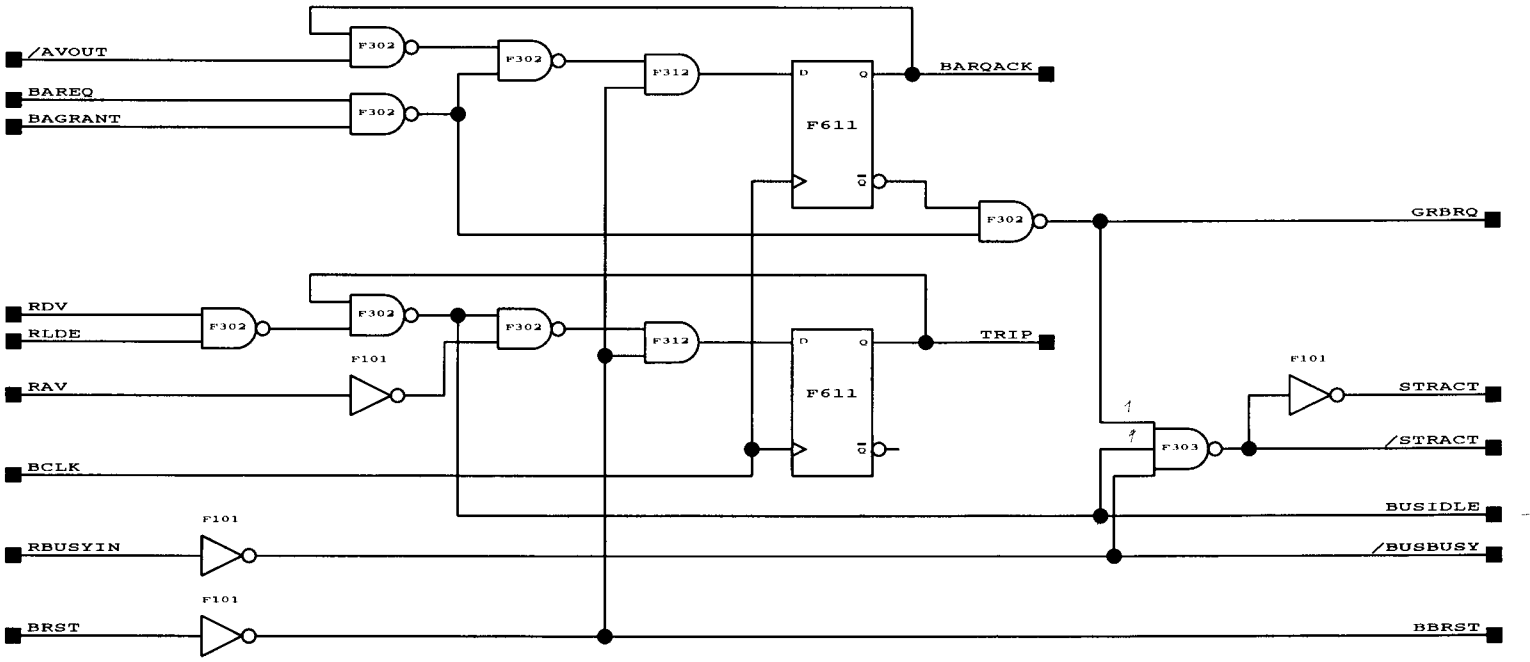
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-18	Bus Interface Buffer
Issue 2		
Issue 3		File: badbuf.1 Page: 1 of 2



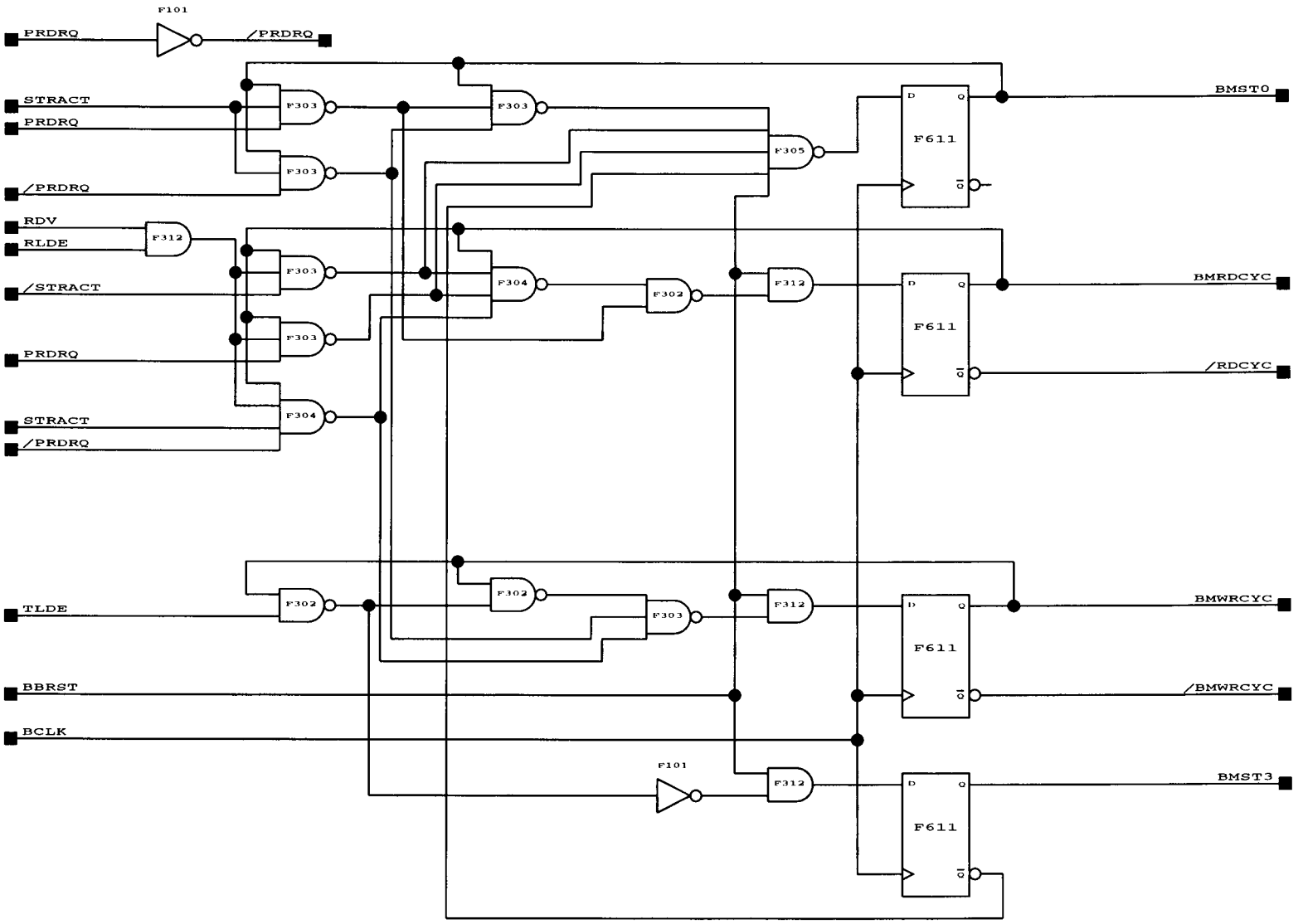
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Bus Interface Buffer	
Issue 1	94-09-18		
Issue 2			
Issue 3		File: badbuf.2	Page: 2 of 2



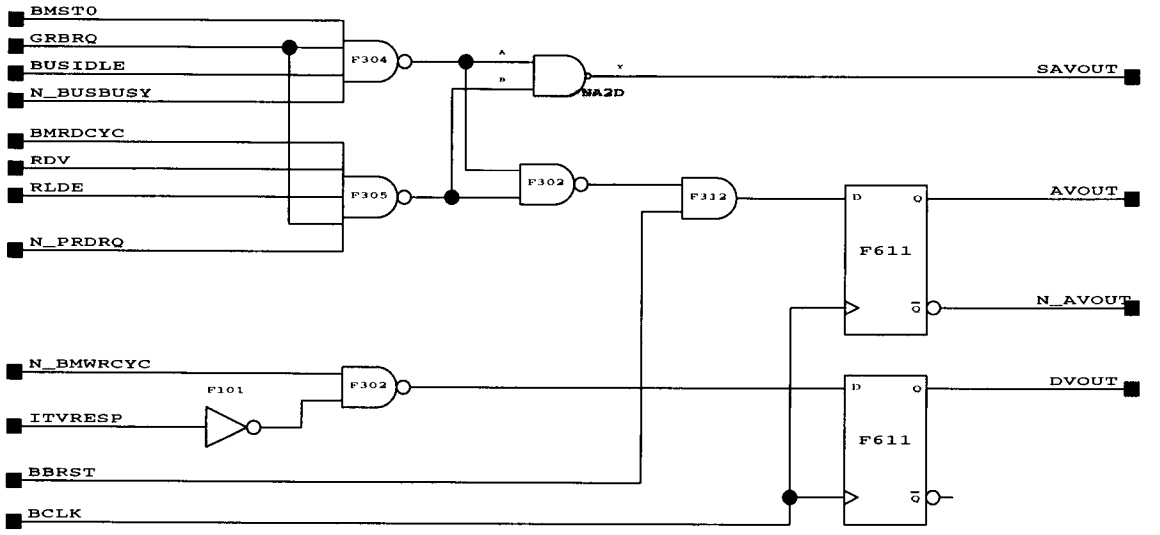
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Bus Interface Buffer
Issue 1	94-06-02	
Issue 2		
Issue 3		File: bctrbuf.1 | Page: 1 of 1



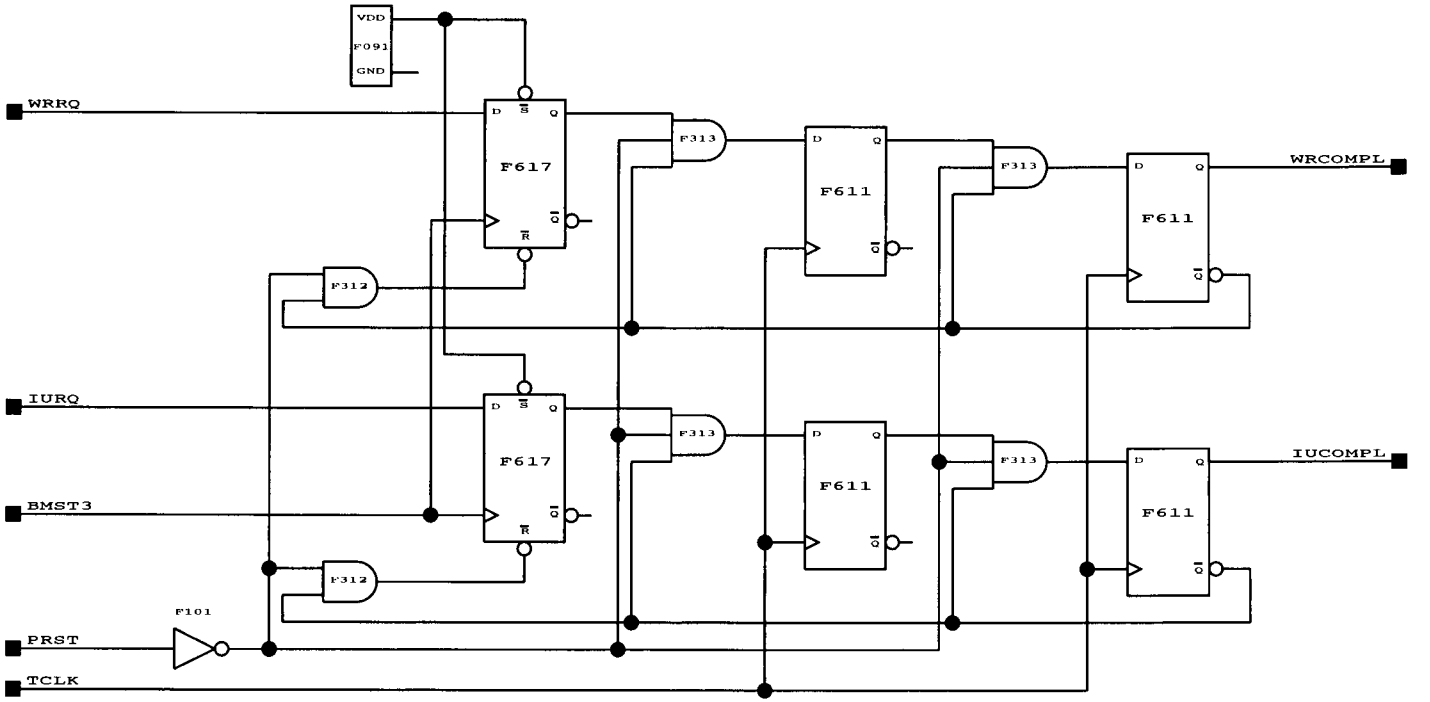
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Bus Master Control - BMACTRL
Issue 2		
Issue 3		File: bmactrl.1 Page:1 of 4



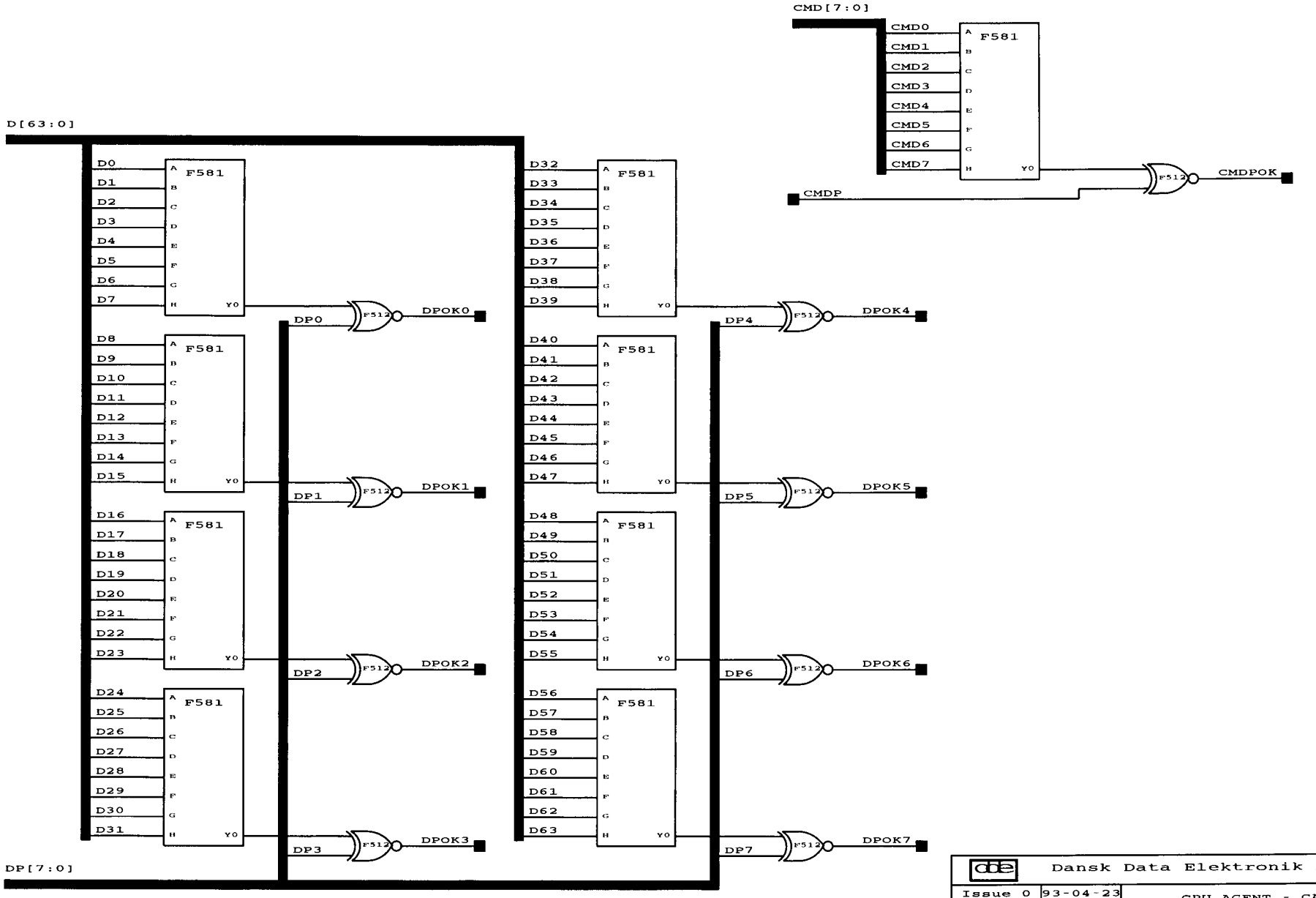
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Bus Master Control - BMACTRL	
Issue 1			
Issue 2			
Issue 3		File: bmactrl.2	Page:2 of 4



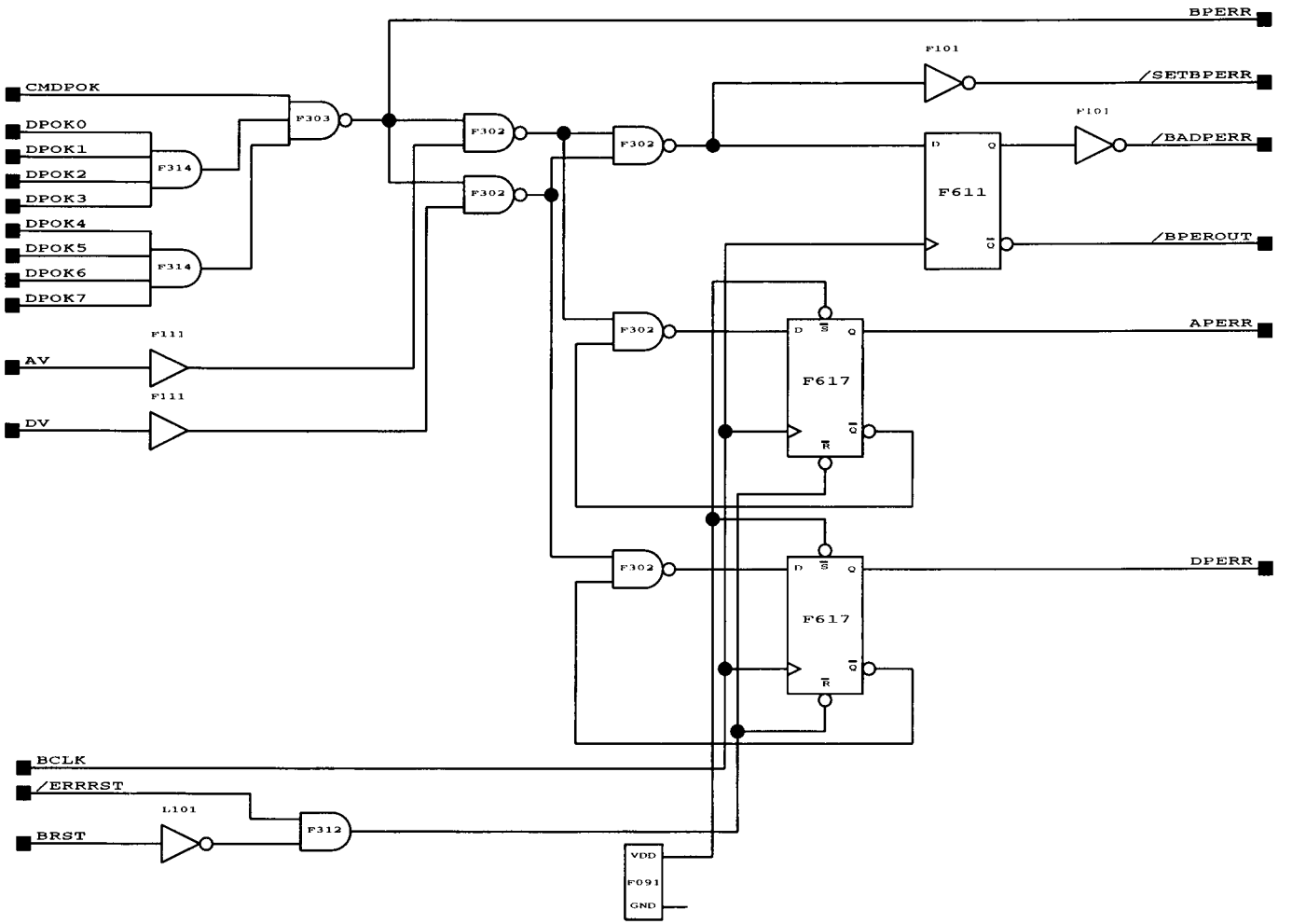
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-08	Bus Master Control - BMACTRL
Issue 2		
Issue 3		File: bmactrl.3 Page:3 of 4



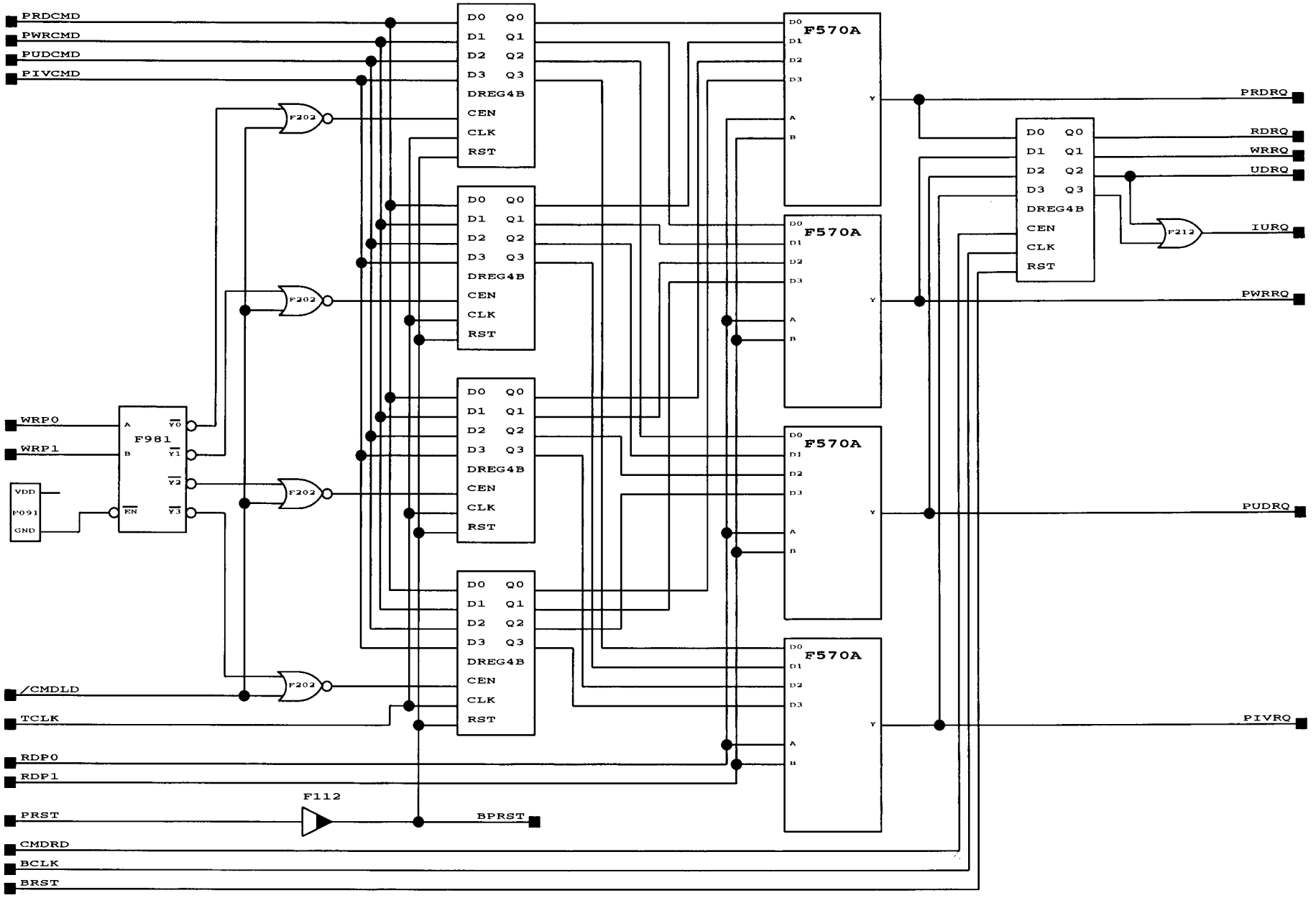
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Bus Master Control - BMACTRL
Issue 2		
Issue 3		File: bmactrl.4 Page:4 of 4



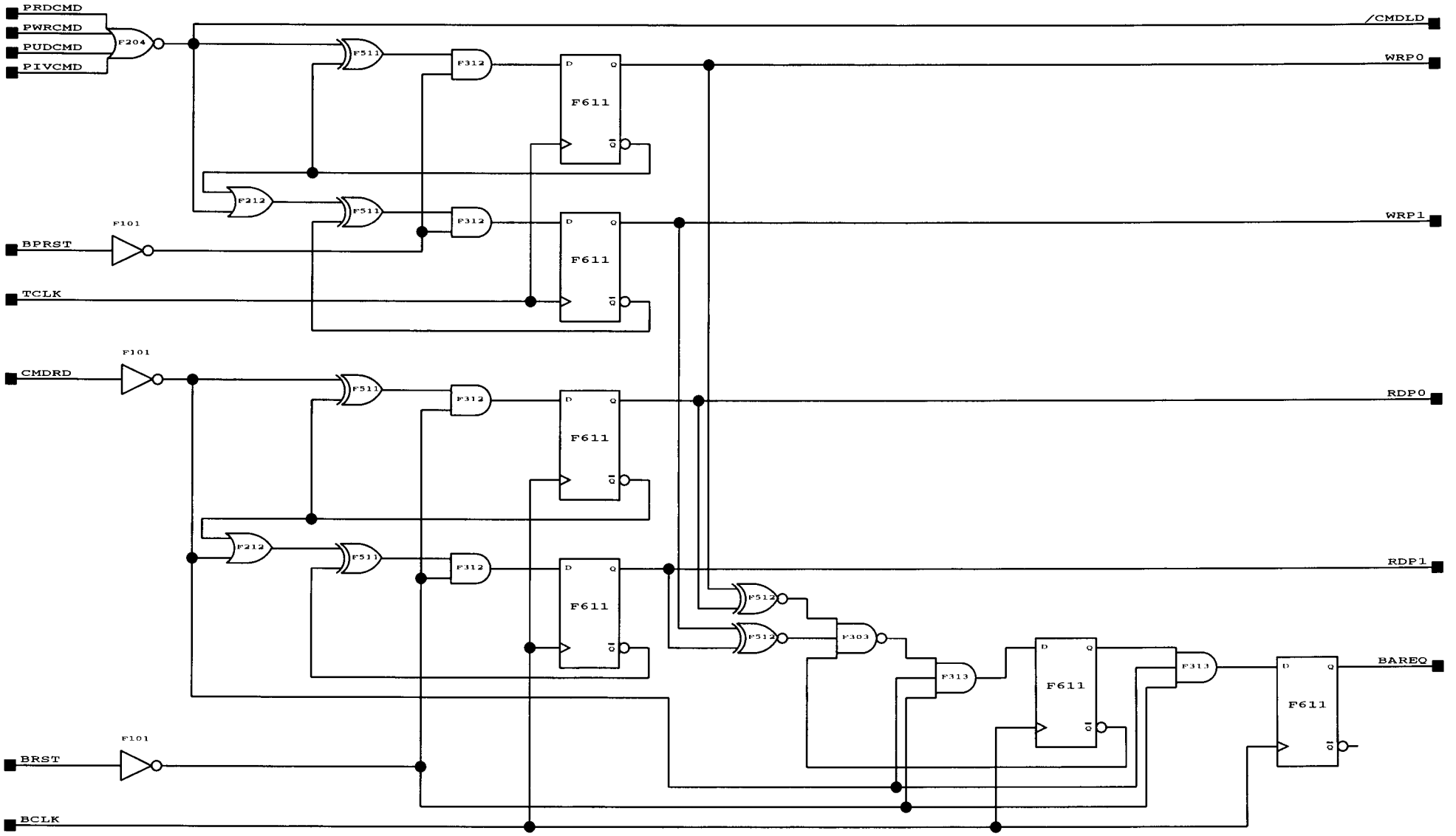
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Bus Parity Checker
Issue 1		
Issue 2		
Issue 3		File: bpchk.1 Page: 1 of 2



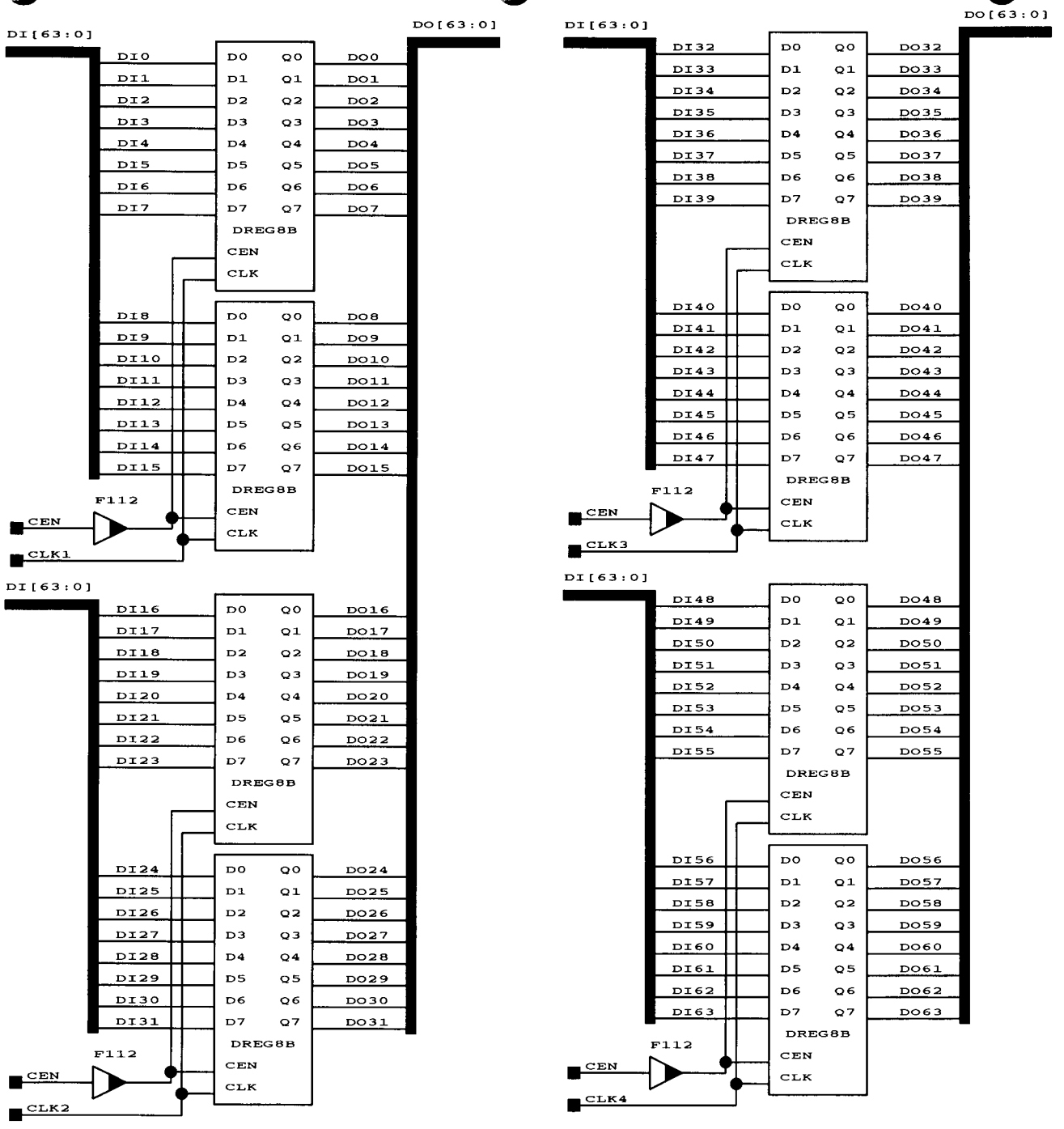
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Bus Parity Checker	
Issue 1			
Issue 2			
Issue 3		File: bpchk.2	Page: 2 of 2



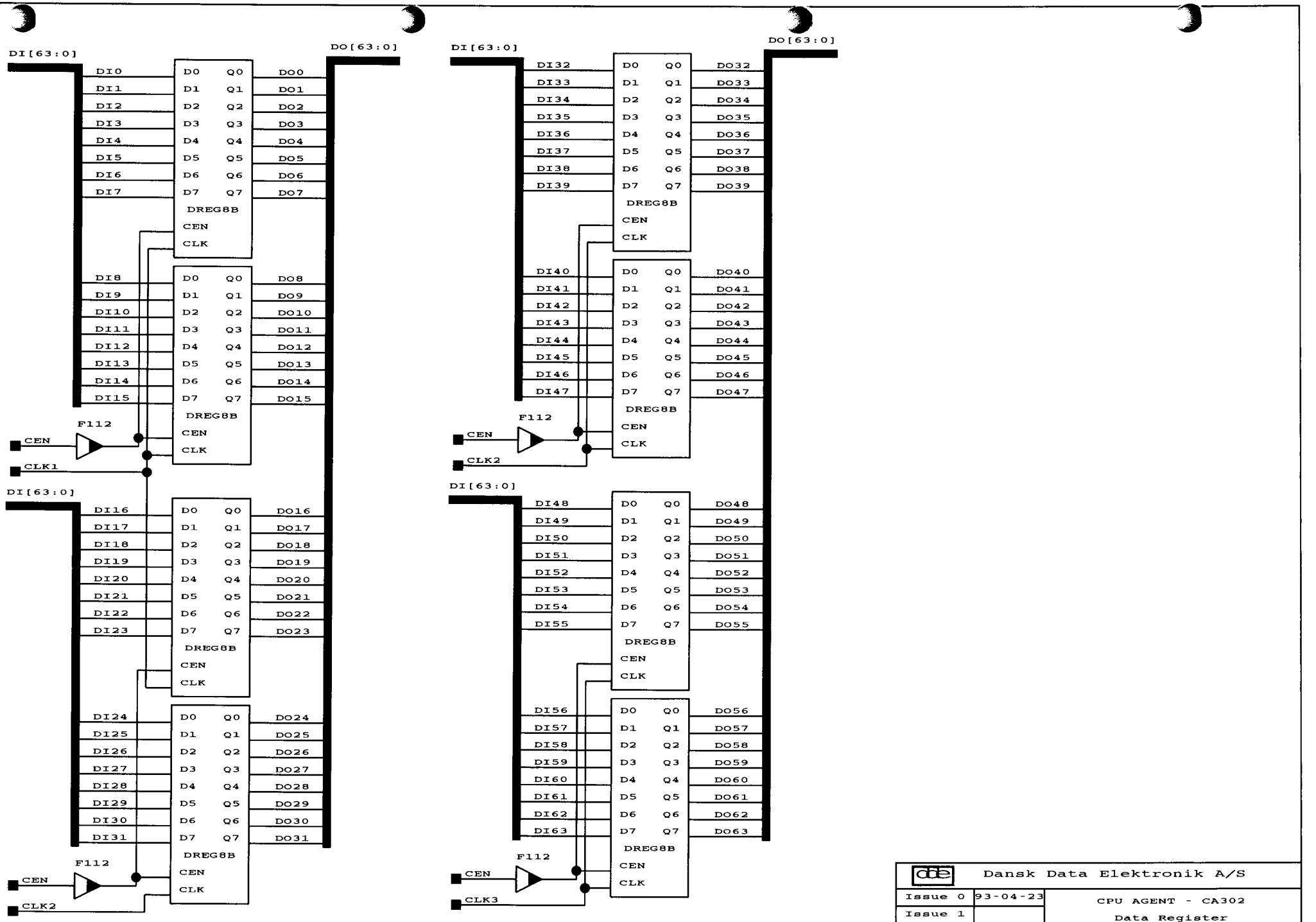
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-18	Command FIFO - CMDFIFO
Issue 2		
Issue 3		File: cmdfifo.1 Page:1 of 2



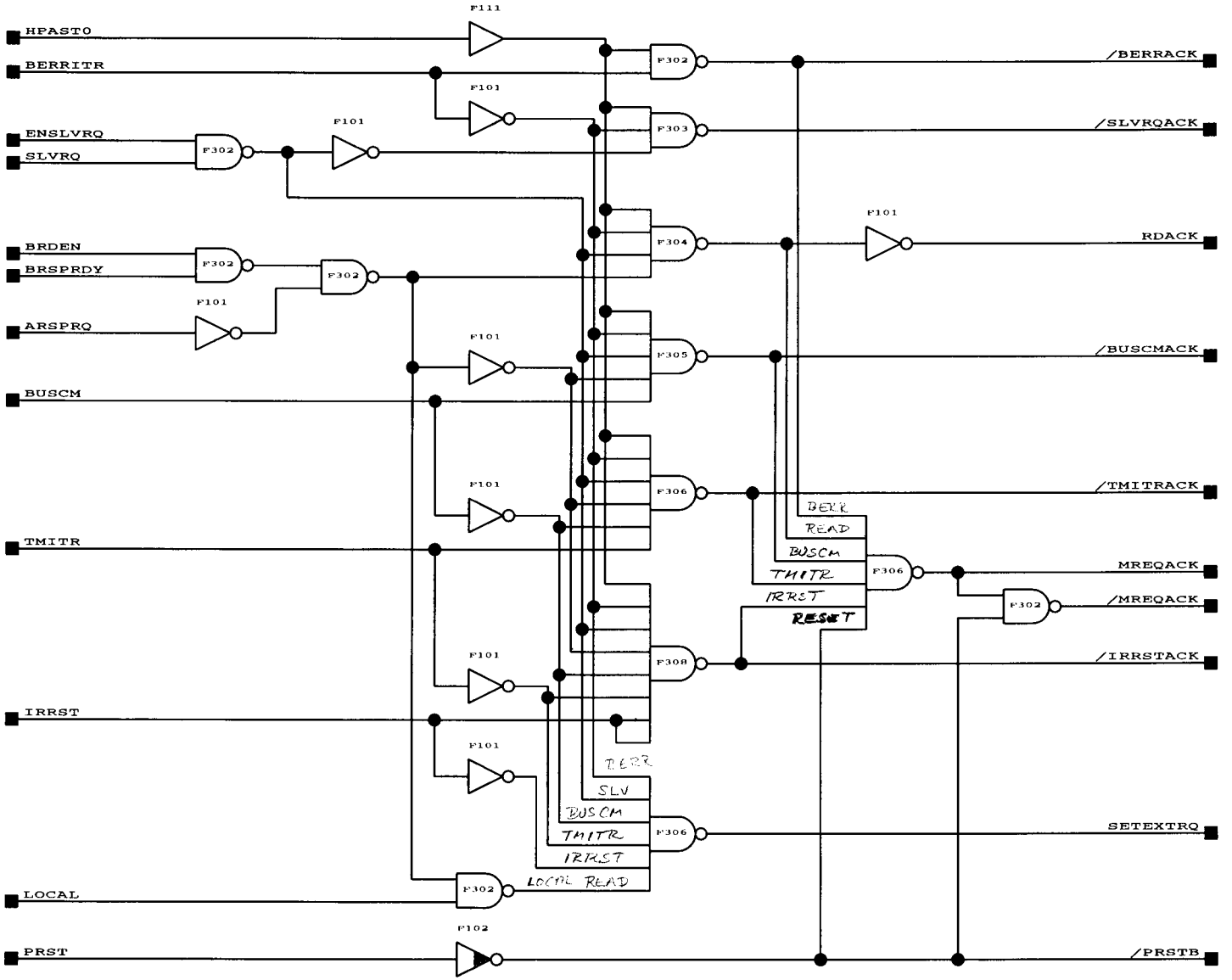
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Command FIFO - CMDFIFO	
Issue 1			
Issue 2			
Issue 3		File: cmdfifo.2	Page:2 of 2



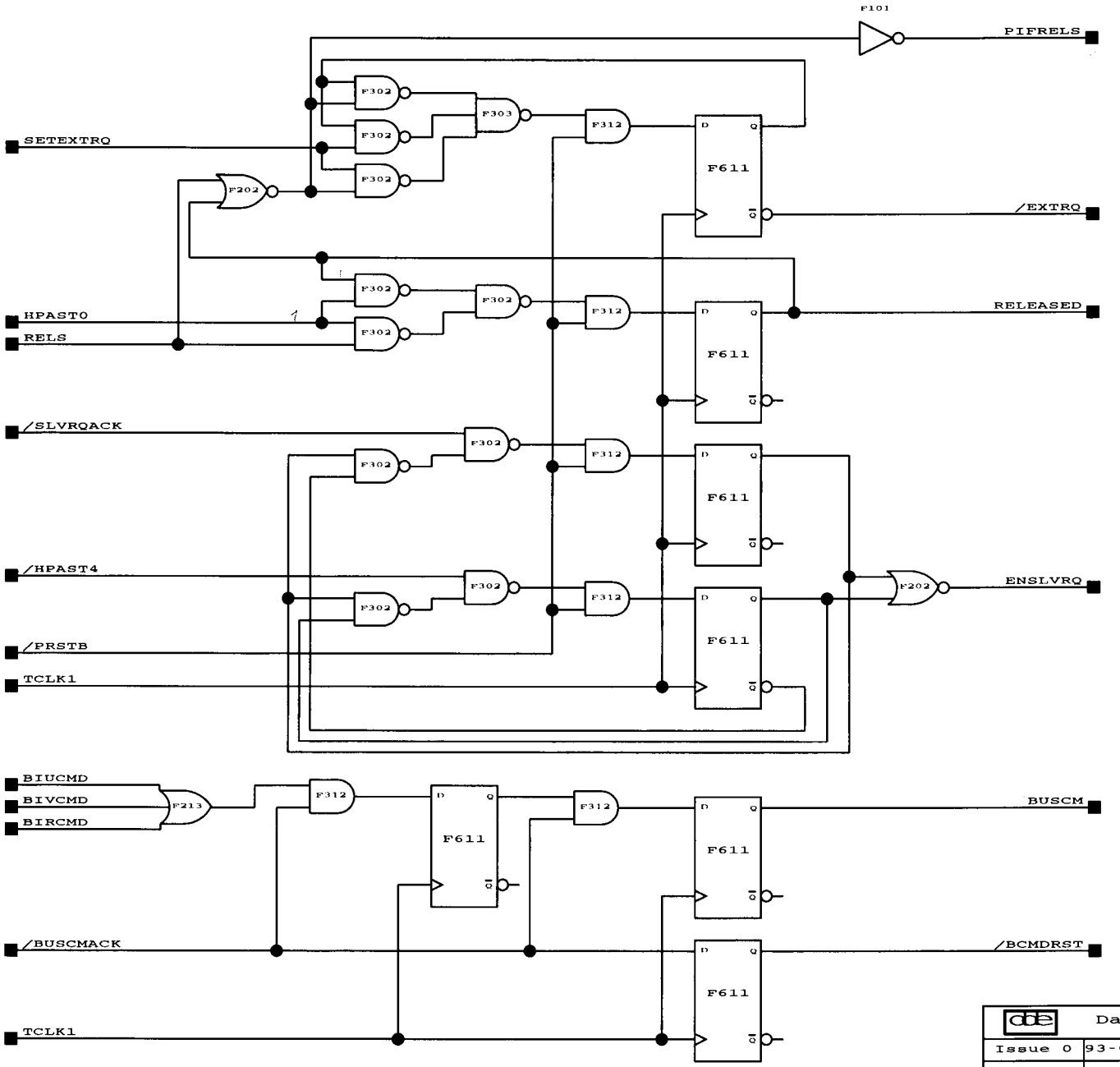
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Data Buffer
Issue 2		
Issue 3		File: databuf.1 | Page:1 of 1



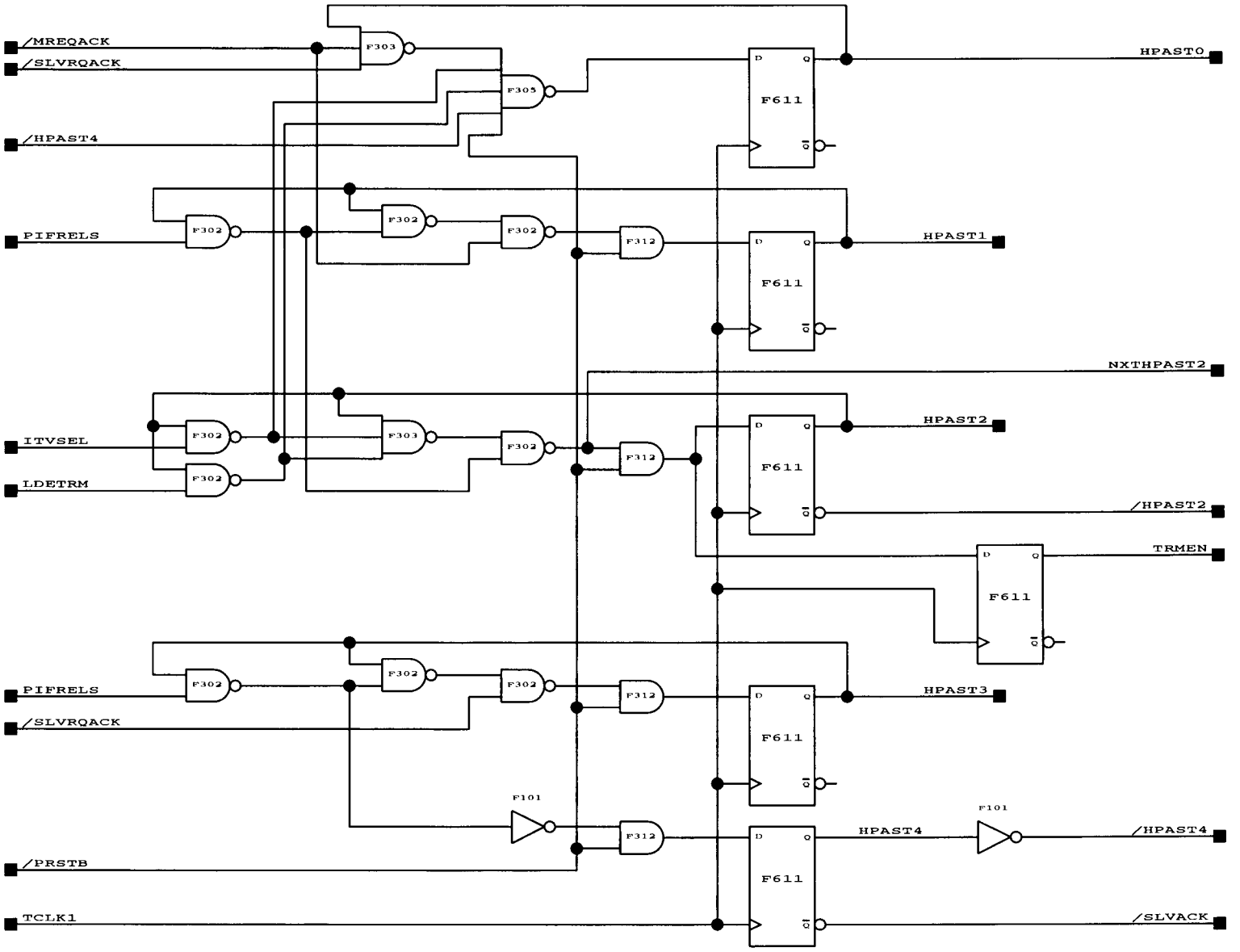
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Data Register
Issue 2		
Issue 3		File: datareg.1 | Page:1 of 1



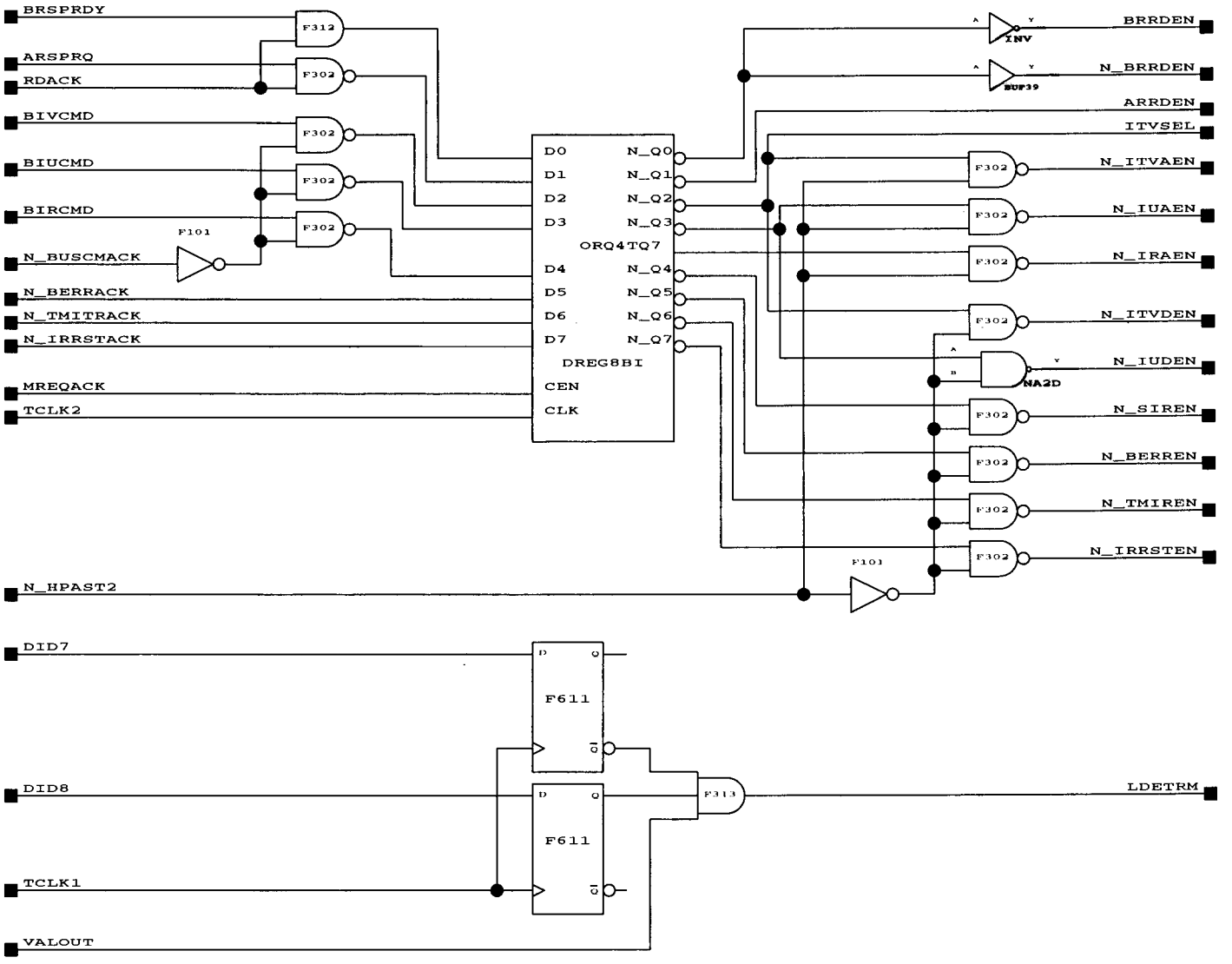
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Host Port Access Priority
Issue 2		
Issue 3		File: hpactr.1 Page:1 of 5



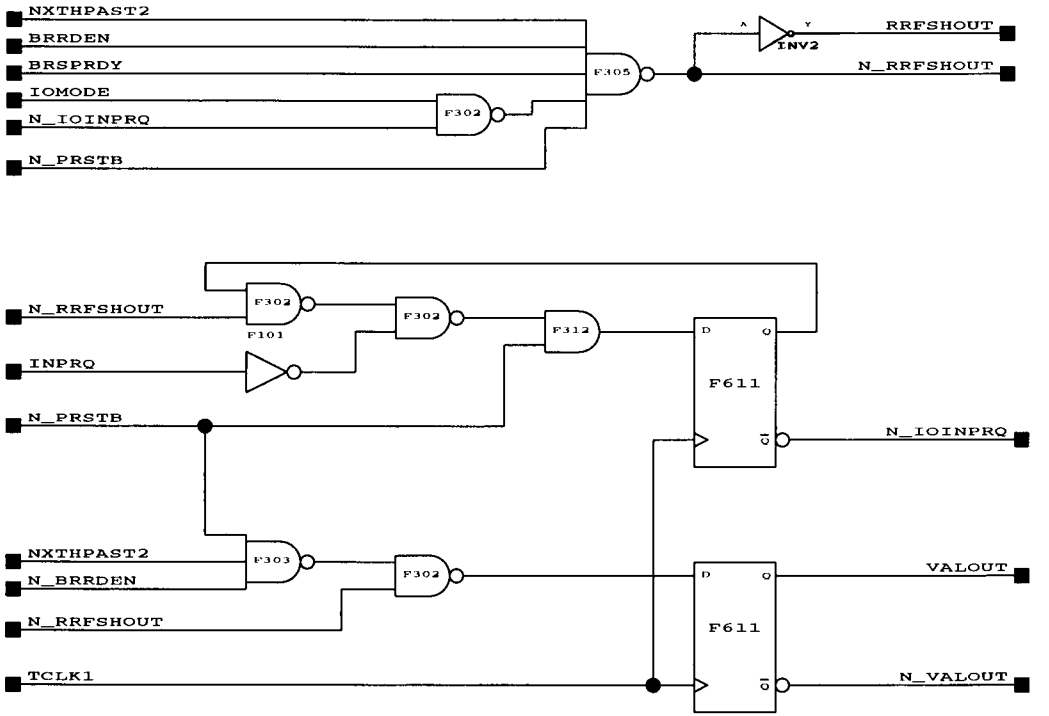
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Host Port Access Control
Issue 2		
Issue 3		File: hpactr.2 Page:2 of 5



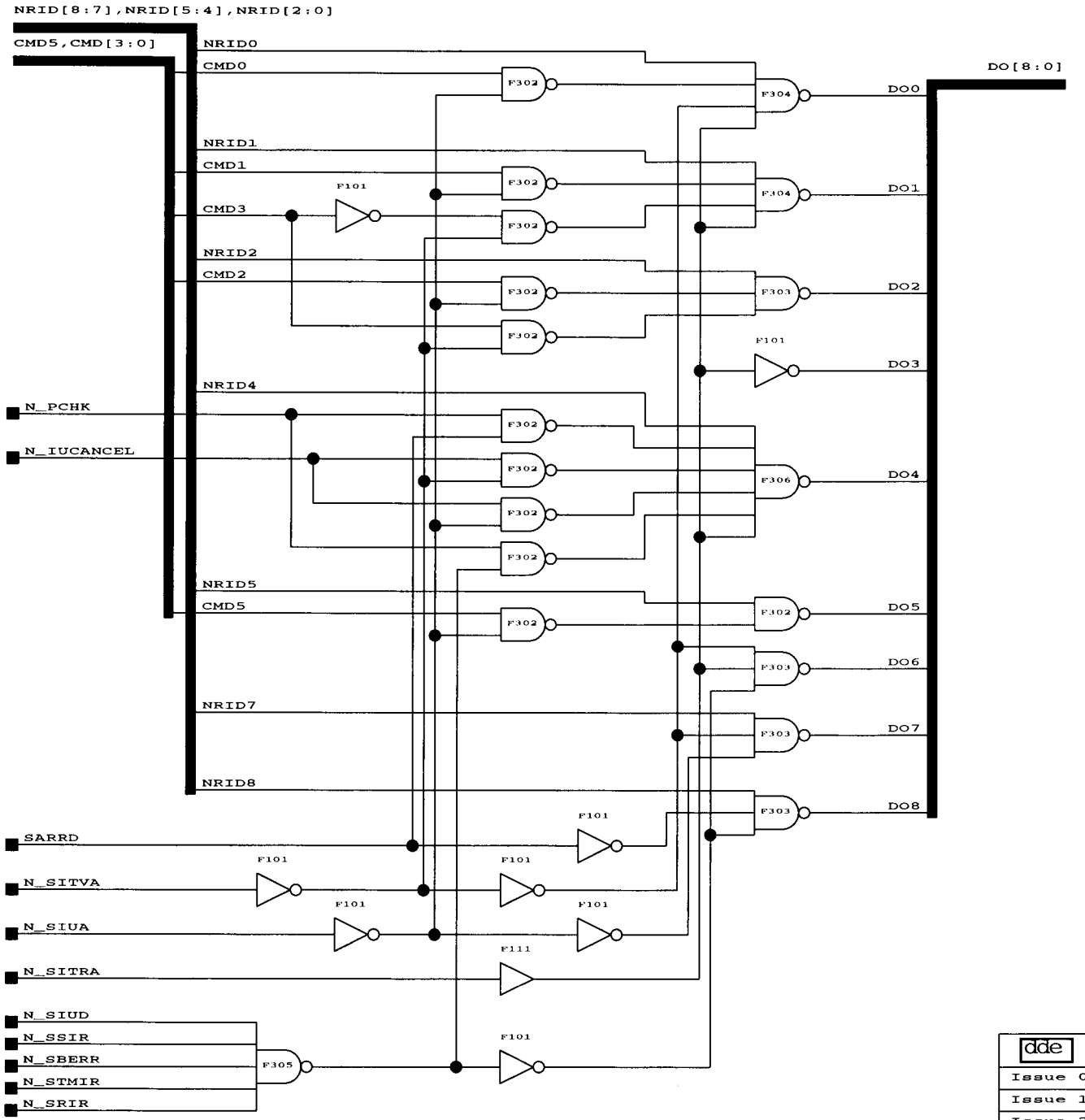
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Host Port Access State Ctrl
Issue 1		
Issue 2		
Issue 3		File: hpactr.3 Page:3 of 5



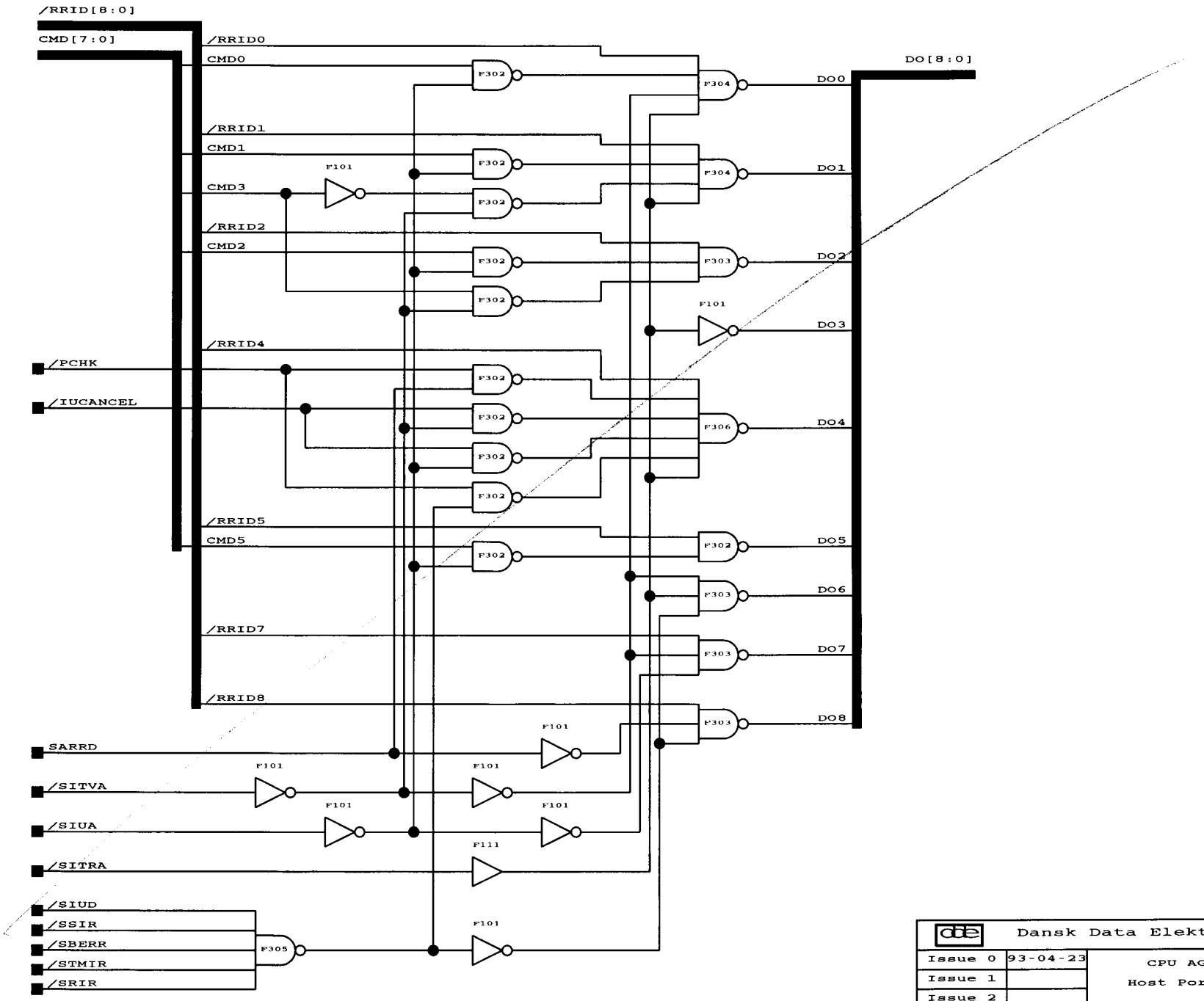
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-08	Host Port Source Selection
Issue 2		
Issue 3		File: hpactr.4 | Page:4 of 5



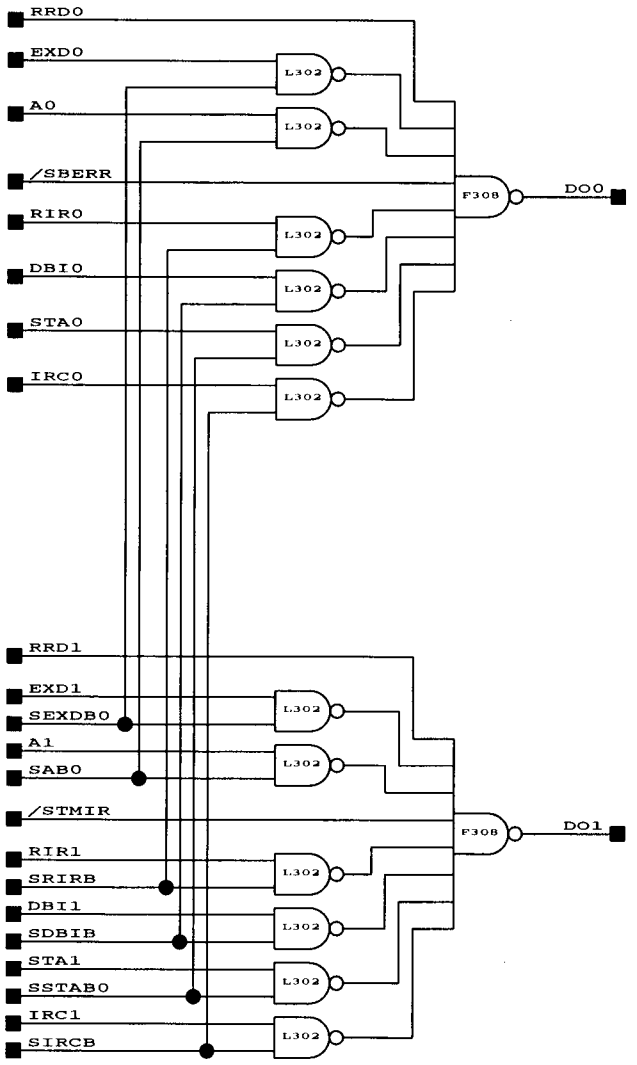
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1	94-09-08	Rd Resp FIFO Shift Out Ctr	
Issue 2			
Issue 3		File: hpactr.5	Page:5 of 5

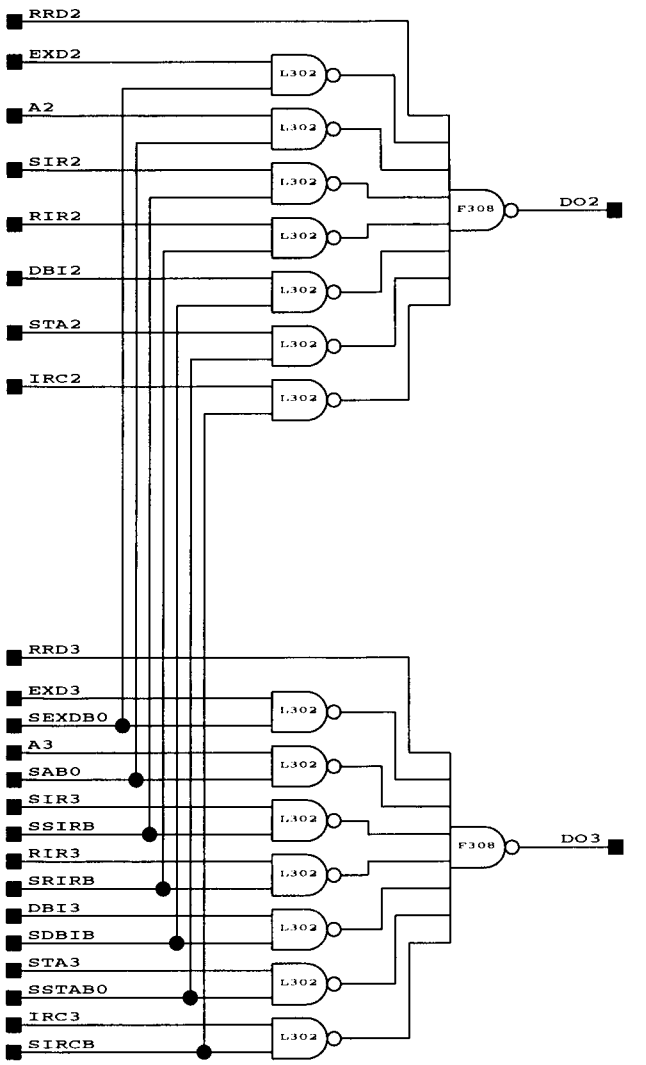


dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-16	Host Port Command Mux
Issue 2		
Issue 3		File: hpcmdmx.1 Page:1 of 1

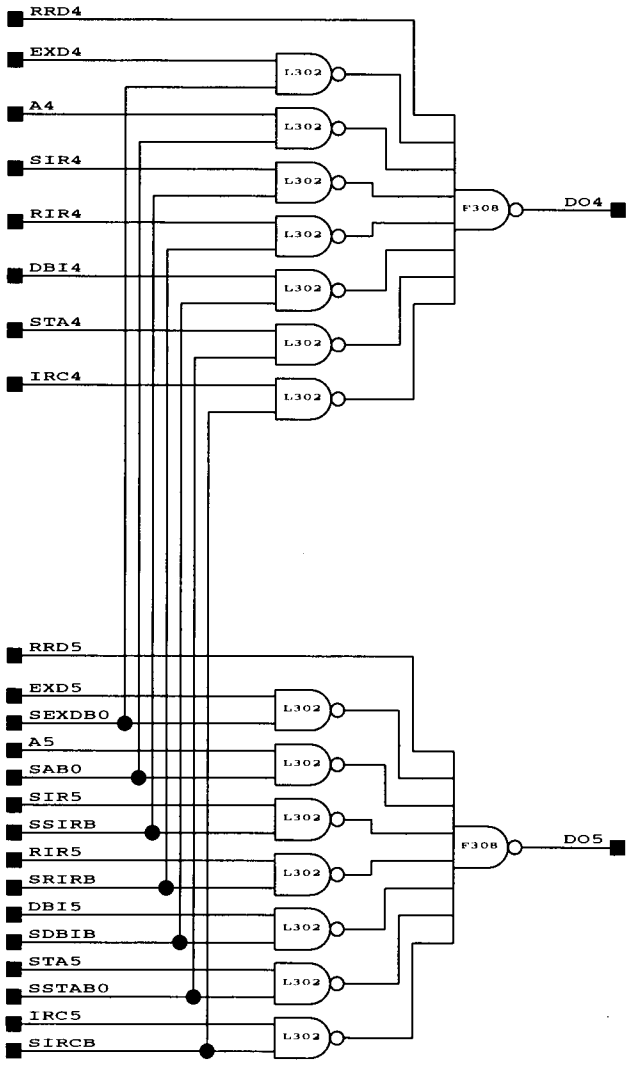


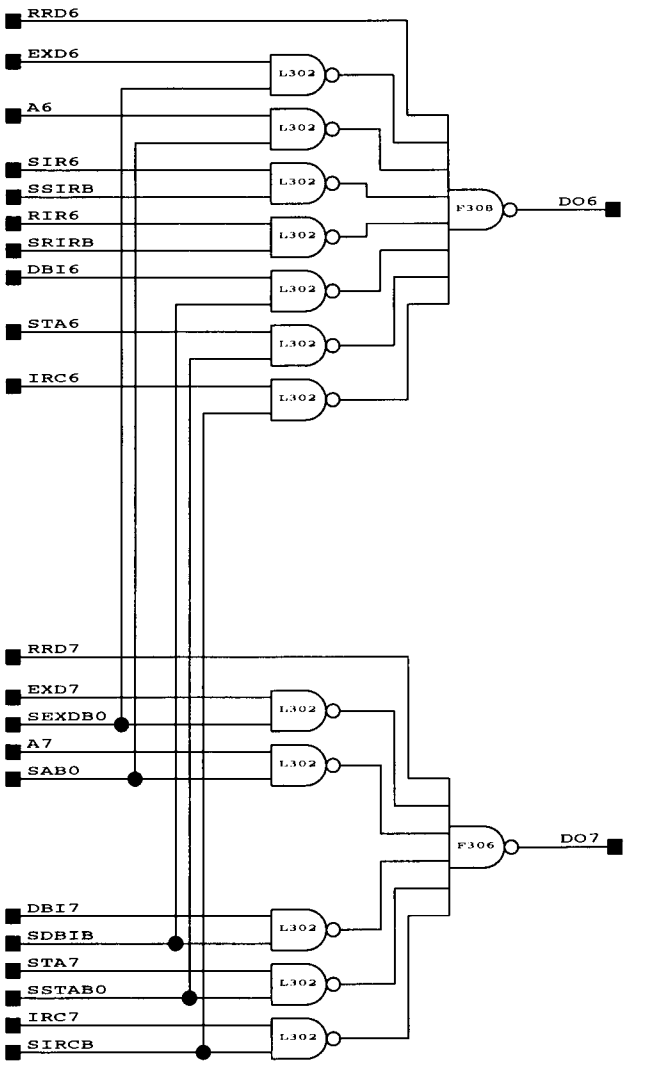
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Host Port Command Mux
Issue 1		
Issue 2		
Issue 3		File: hpcmdmx.1 Page:1 of 1



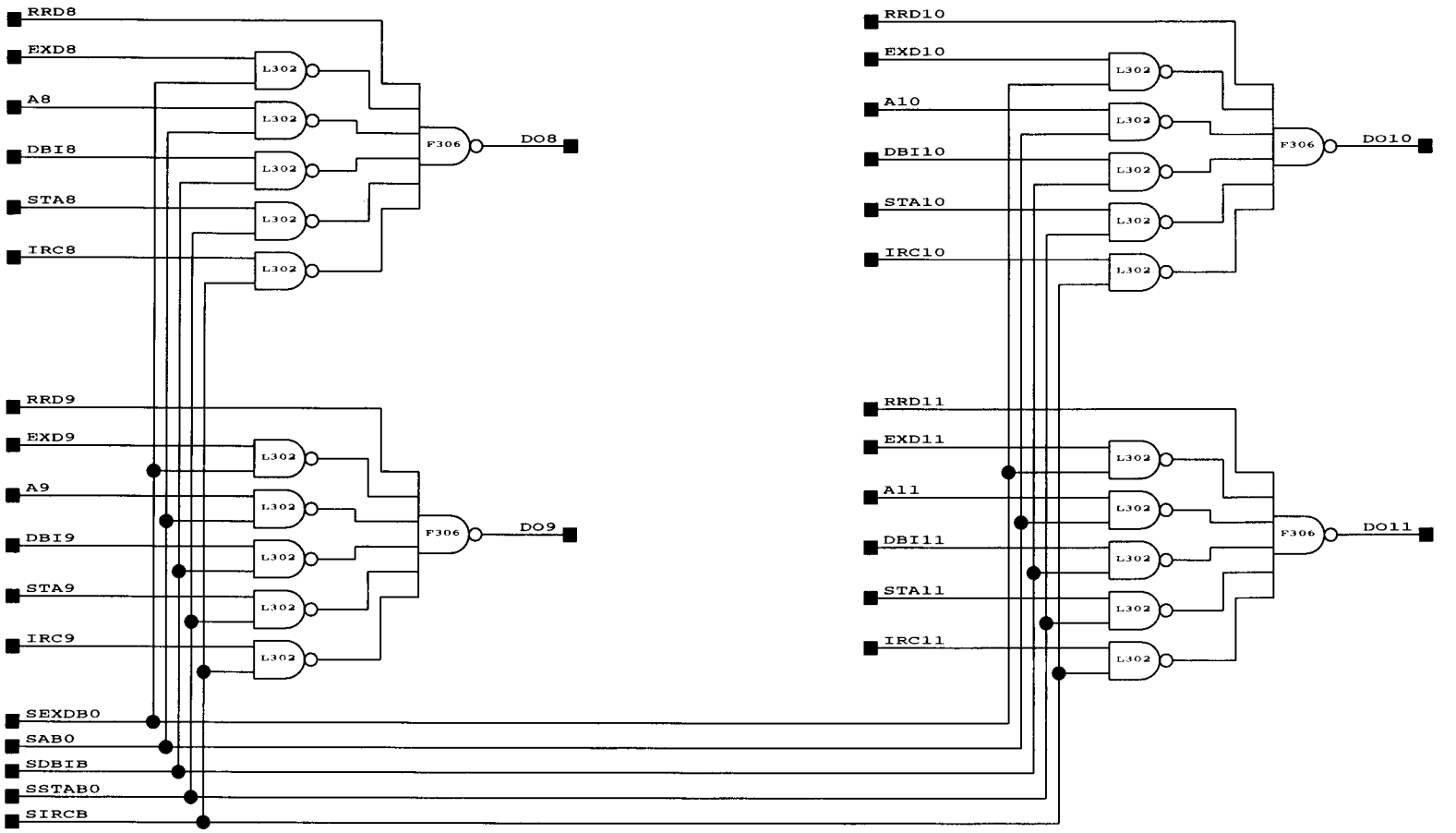


dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-25	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.1 | Page:1 of 11

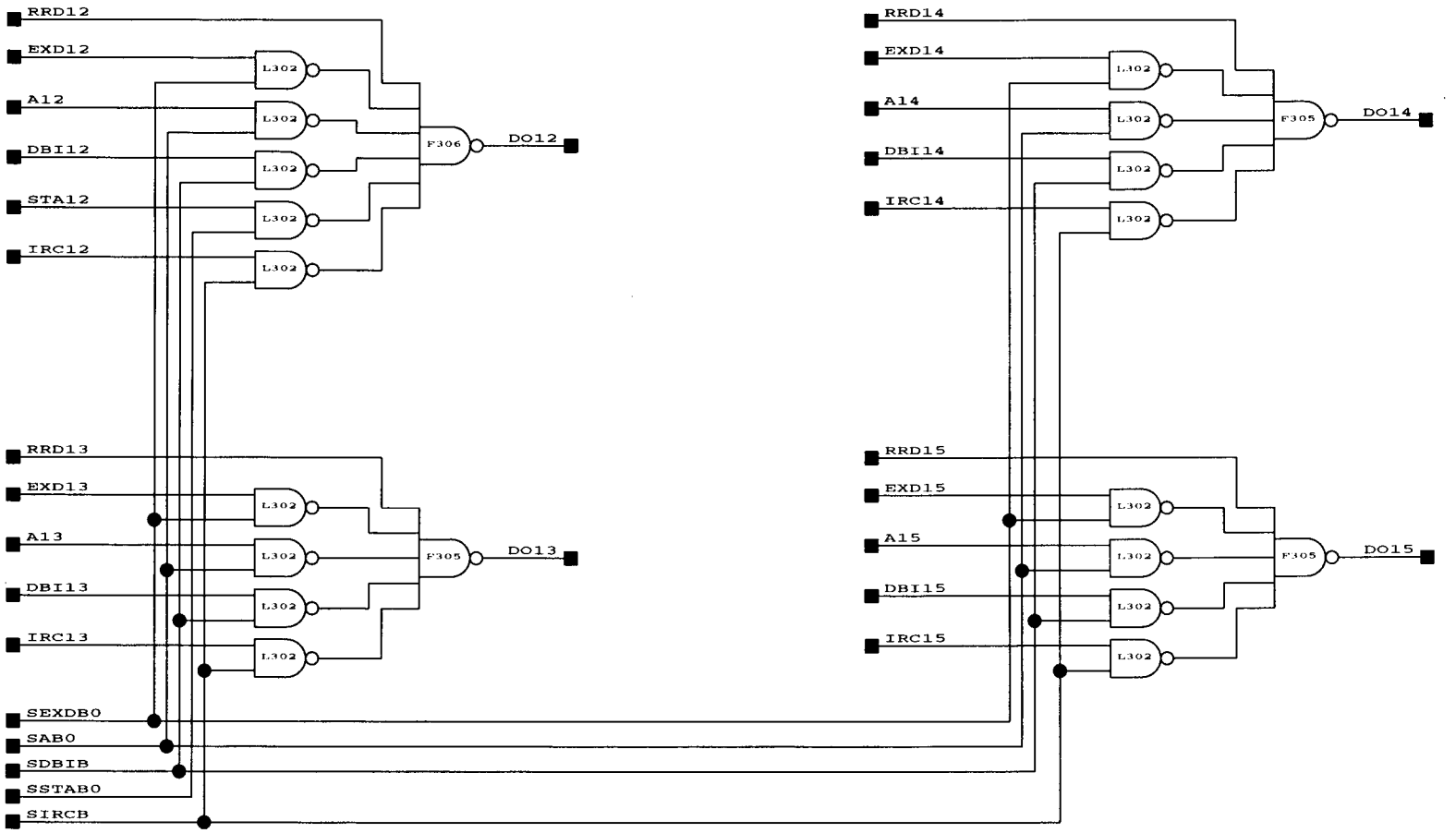




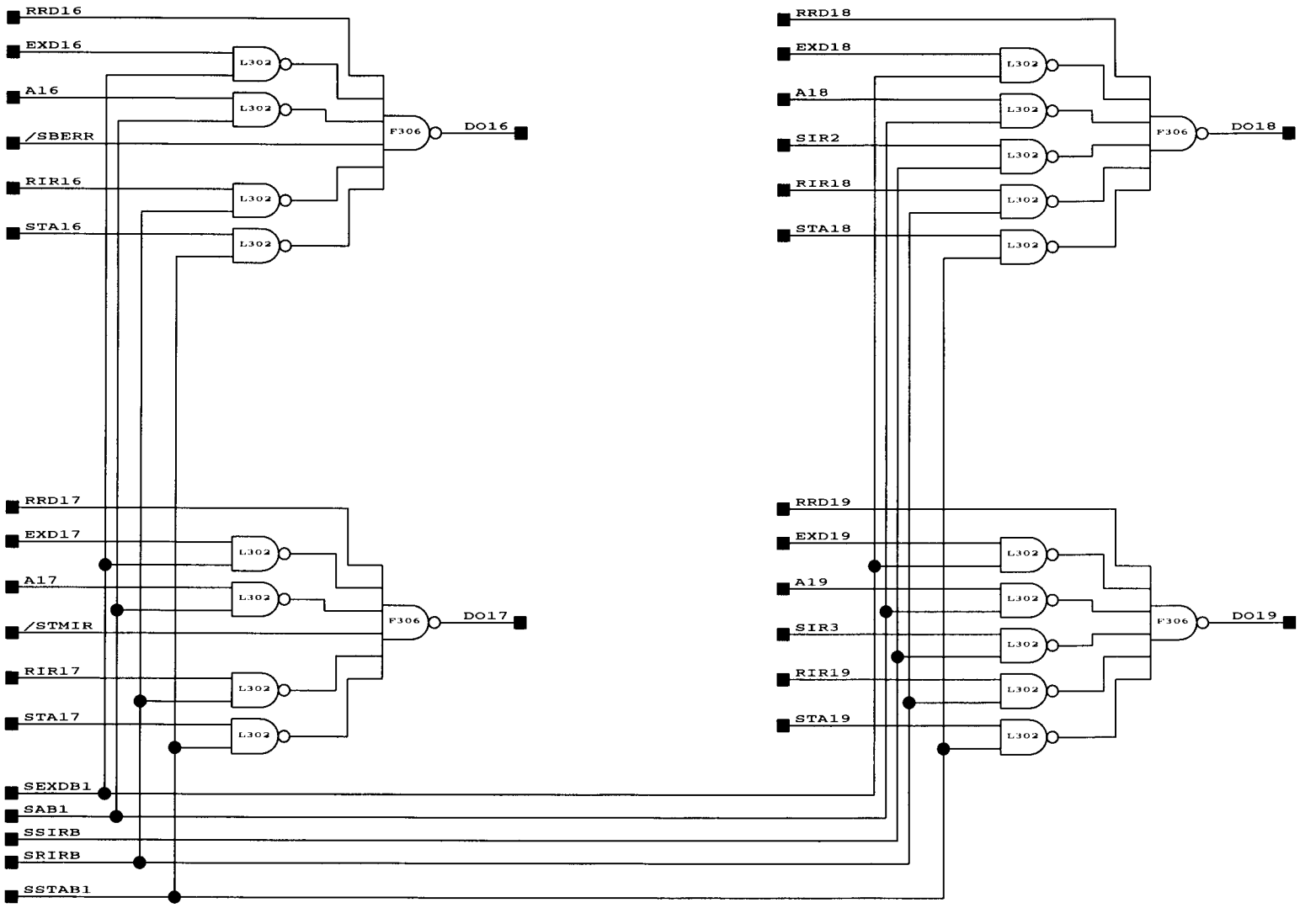
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-25	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.2 Page:2 of 11



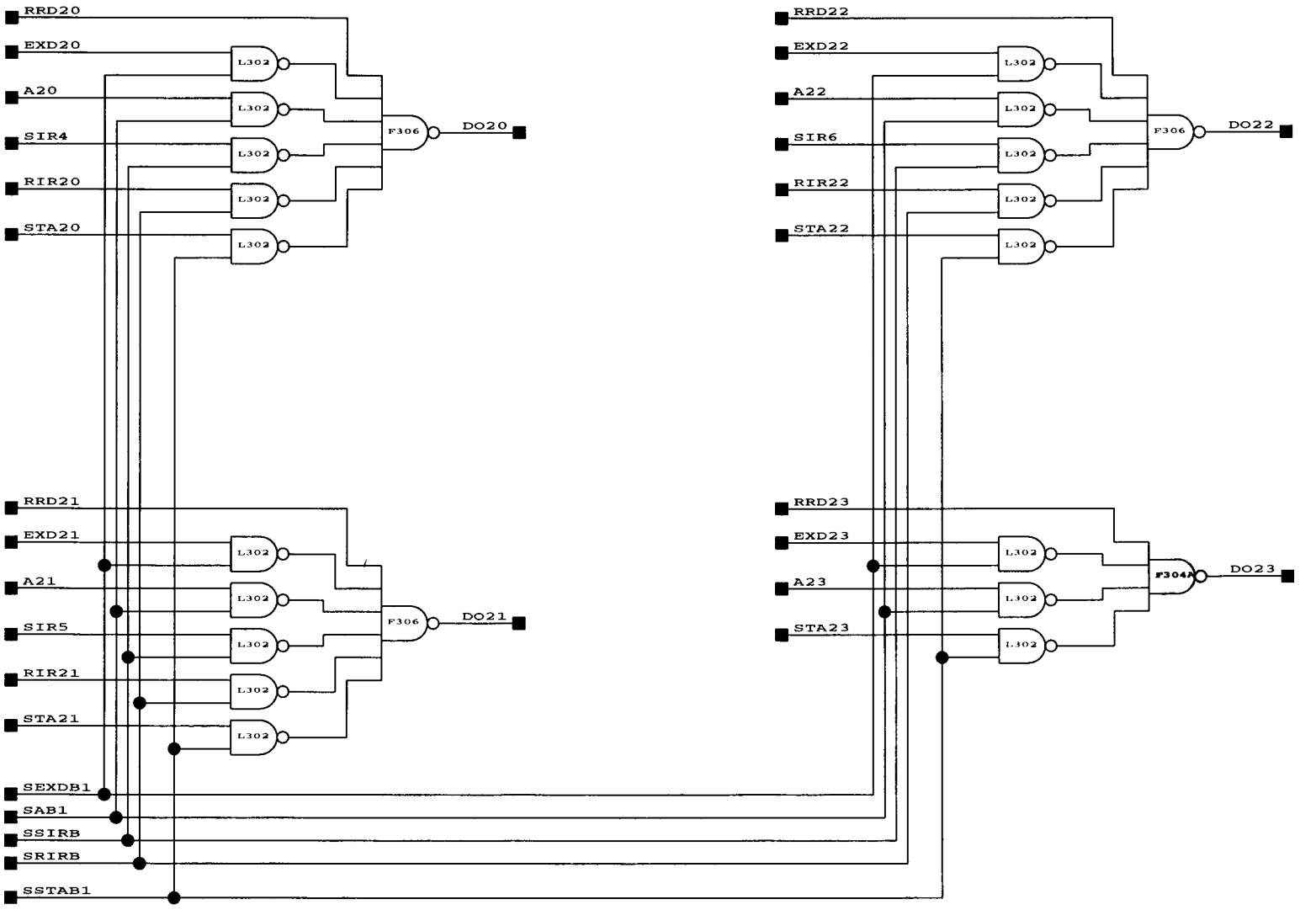
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-25	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.3 Page:3 of 11



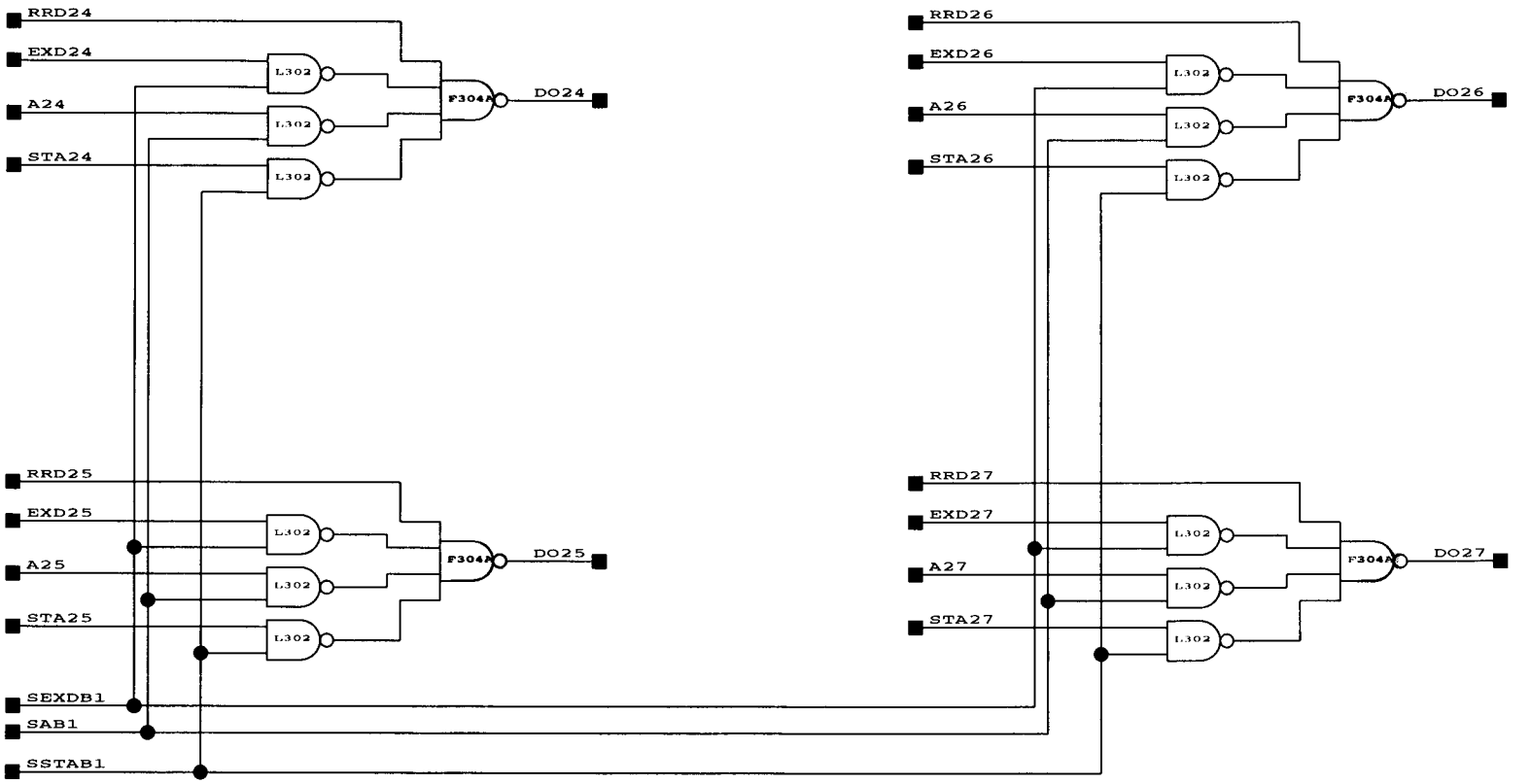
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-15	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.4 Page:4 of 11



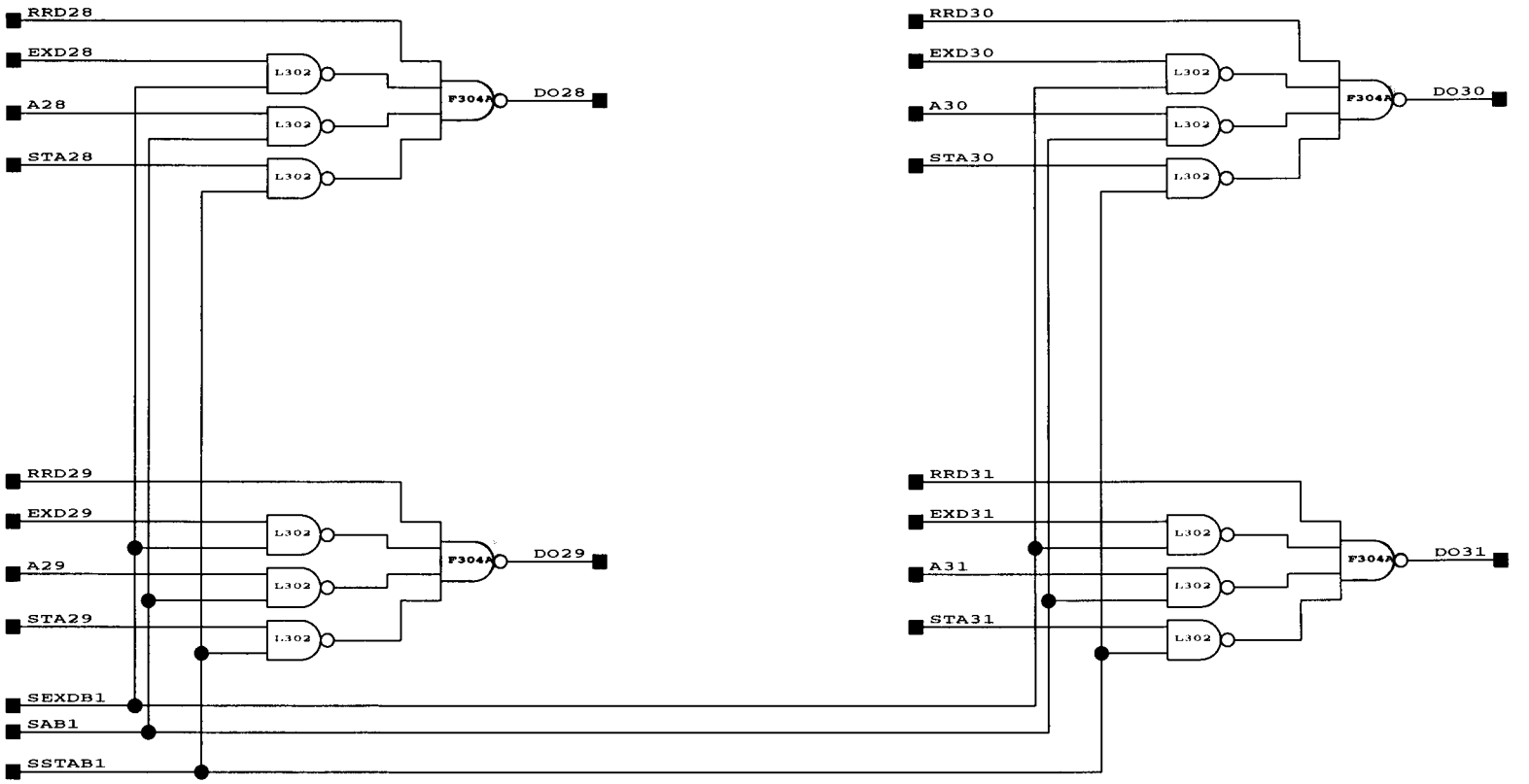
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-25	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.5 Page:5 of 11



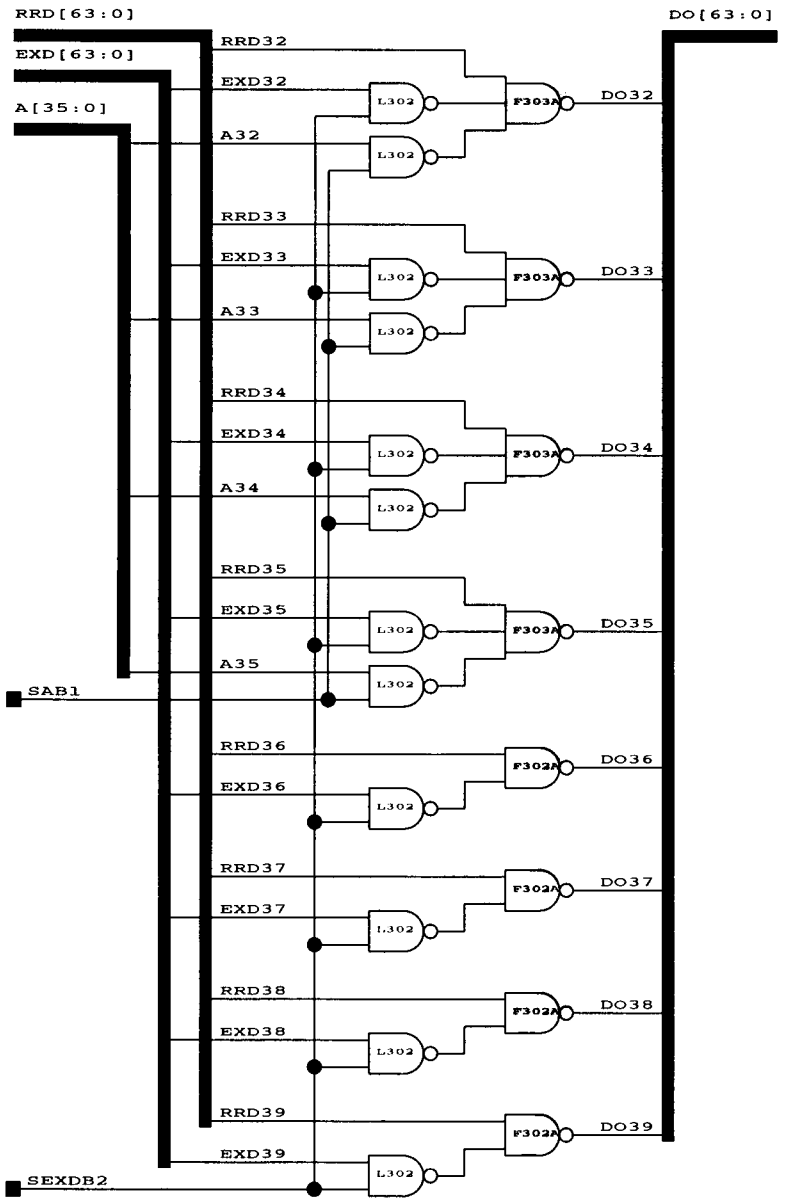
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-18	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.6 Page:6 of 11



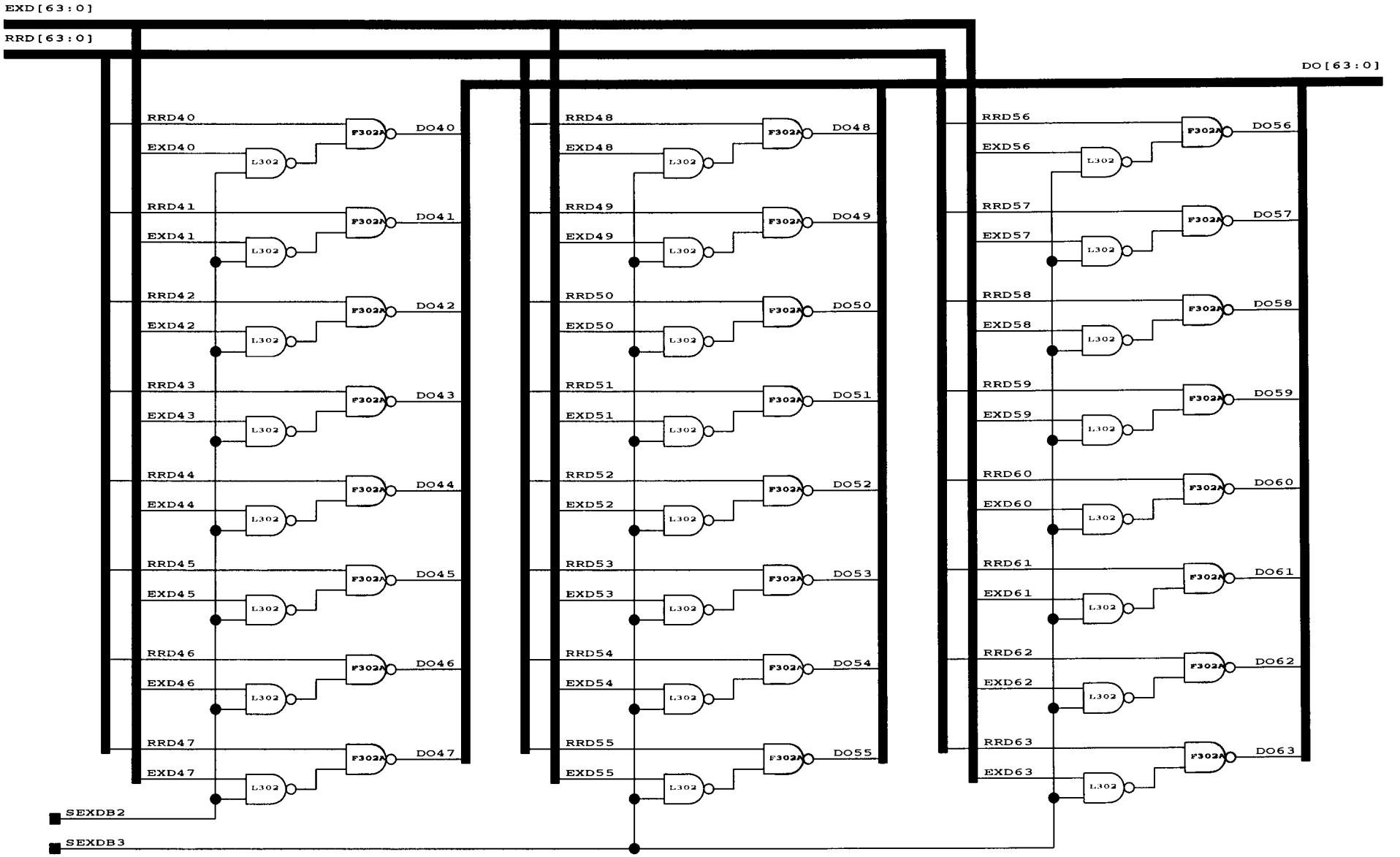
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-18	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.7 Page:7 of 11



dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-18	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.8 Page:8 of 11



dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-18	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.9 Page:9 of 11



dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-18	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.10 Page:10 of 11

A[35:0]

RRD[63:0]

EXD[63:0]

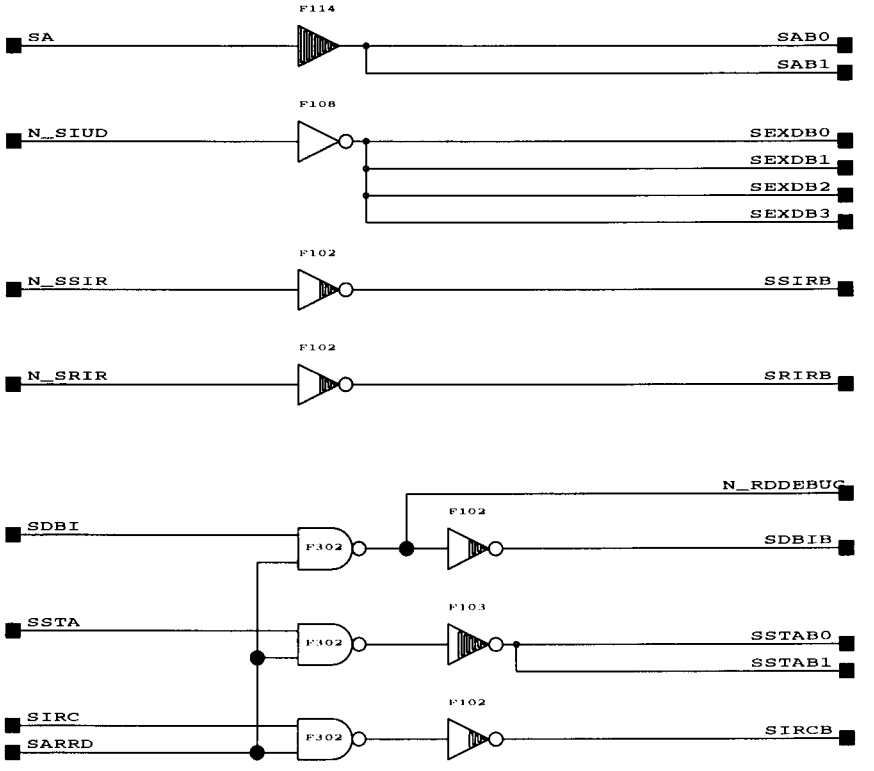
SIR[6:2]

RIR[22:16],RIR[6:0]

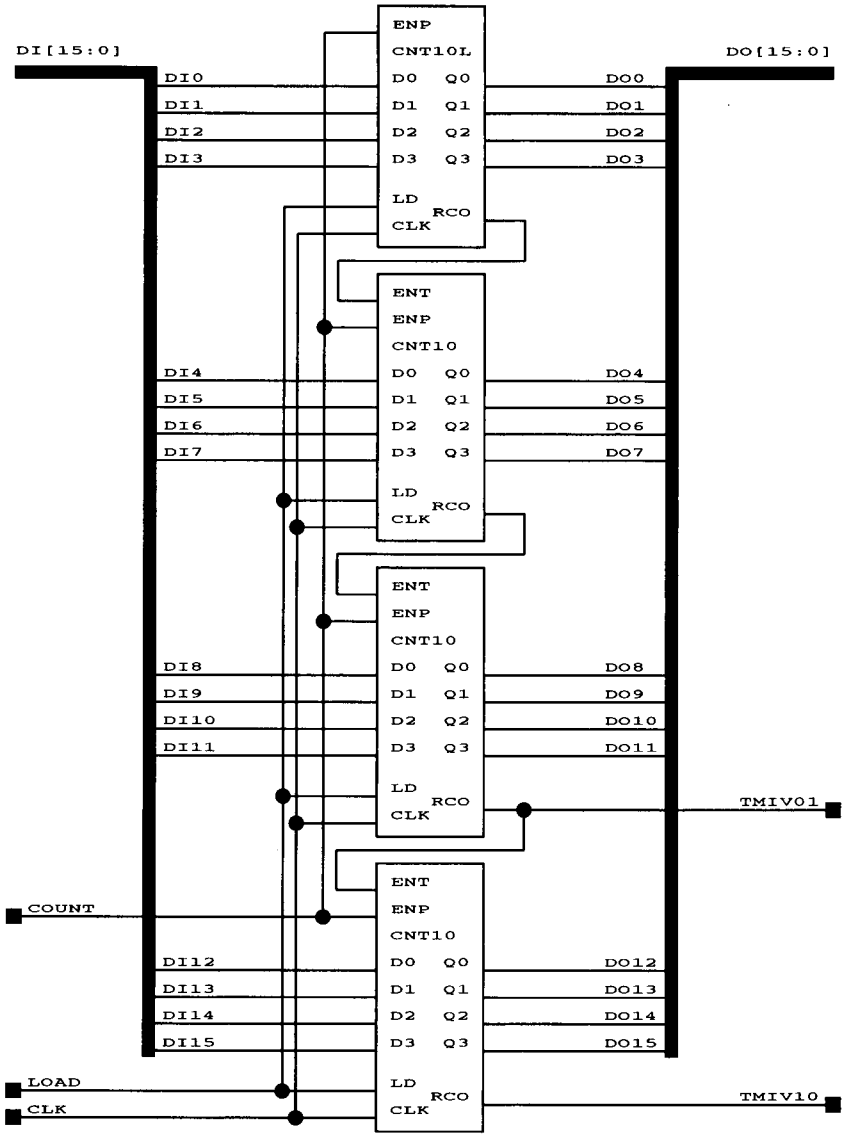
DBI[15:0]

STA[31:16],STA[12:0]

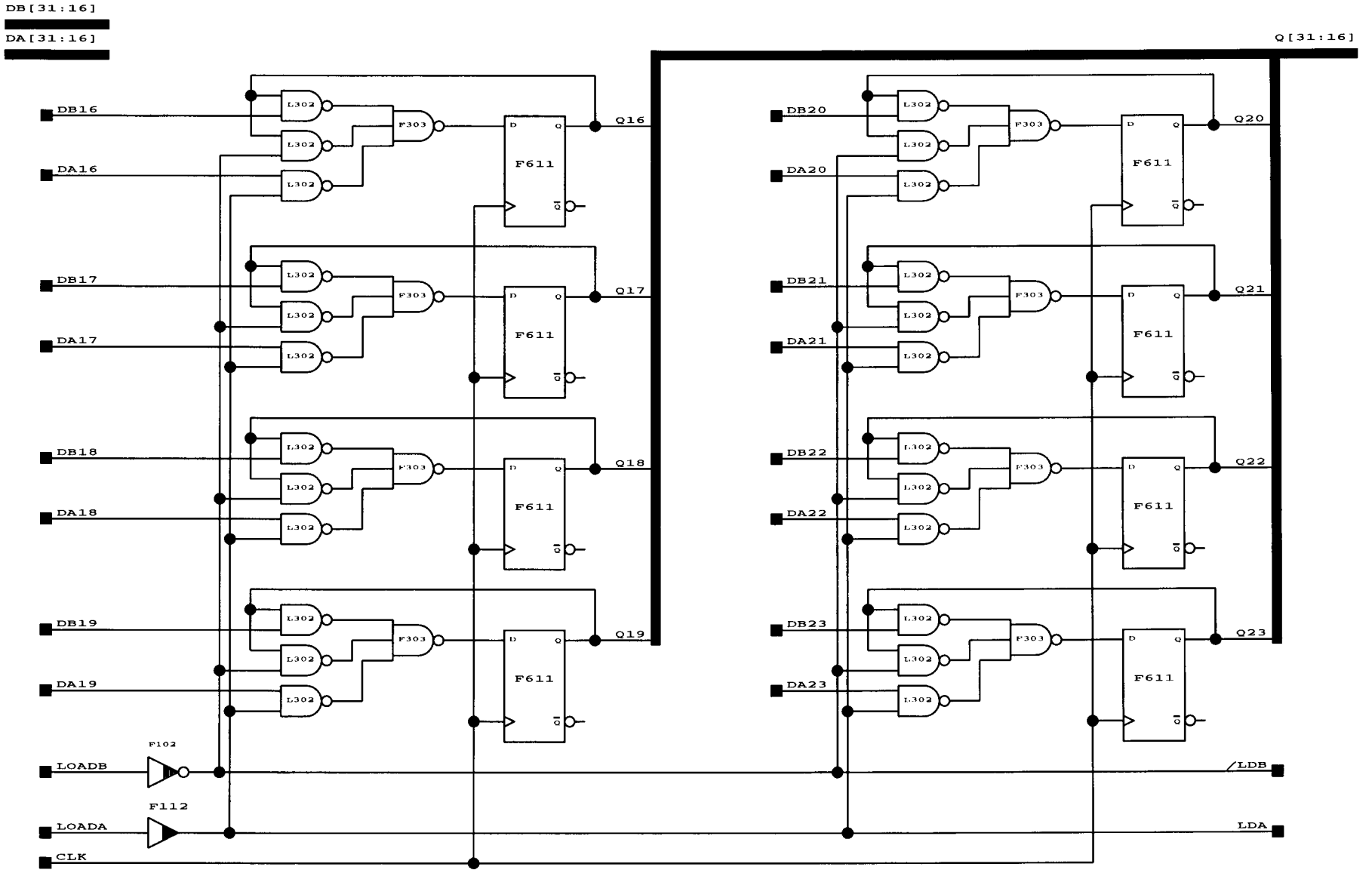
IRC[15:0]



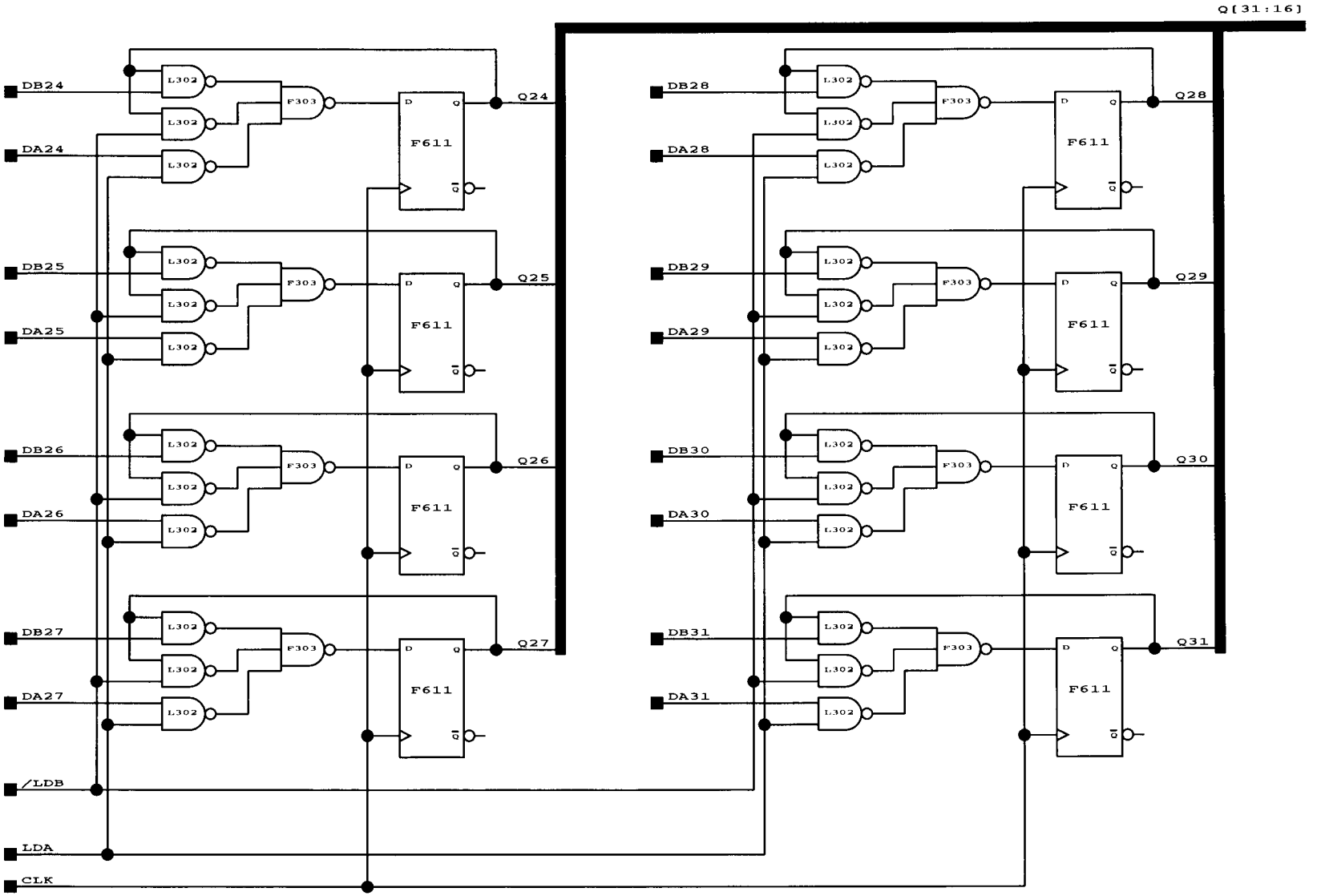
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-08-16	Host Port A/D Multiplexer
Issue 2		
Issue 3		File: hpomux.11 Page:11 of 11



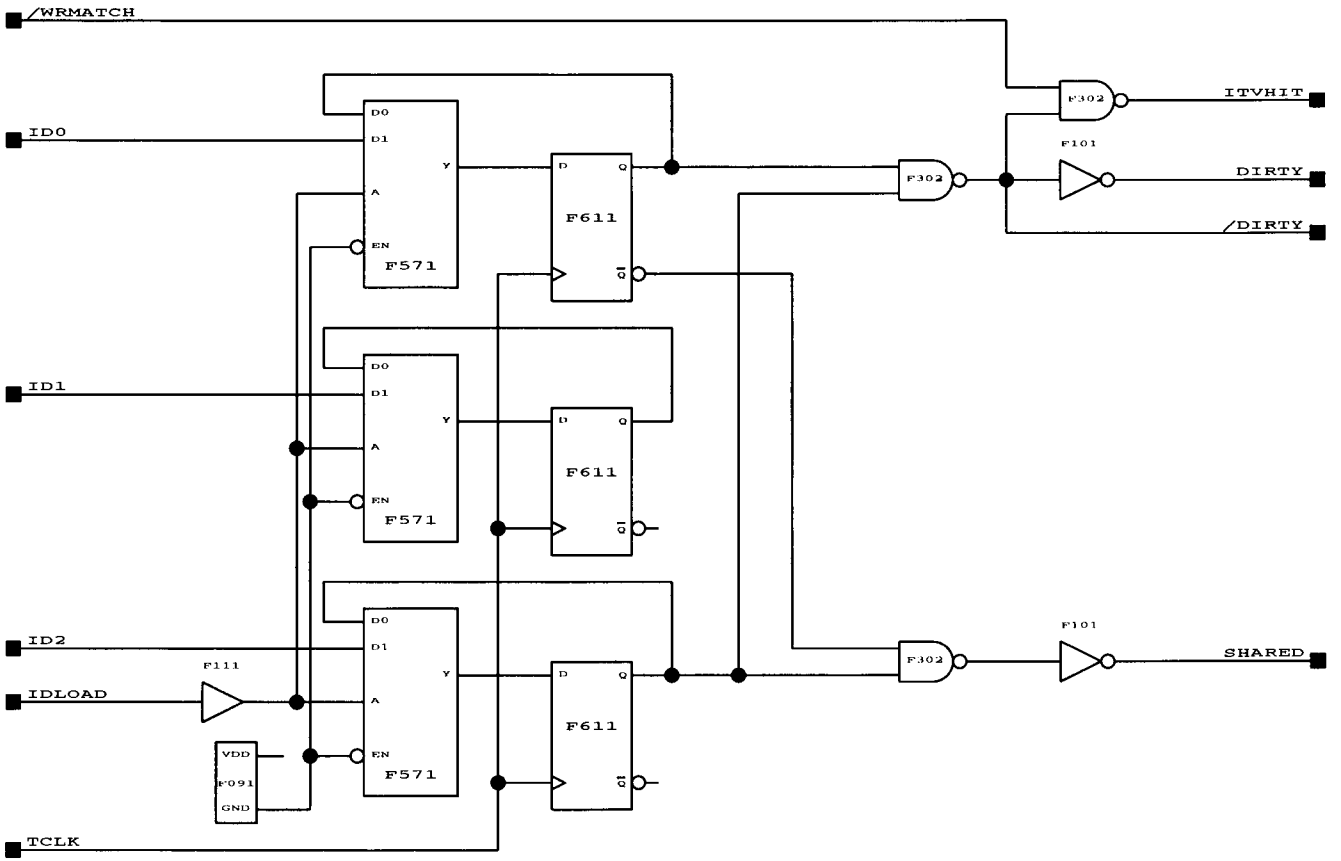
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 ITRCNT Interrupt Counter	
Issue 1			
Issue 2			
Issue 3		File: itrcnt.1	Page: 1 of 1



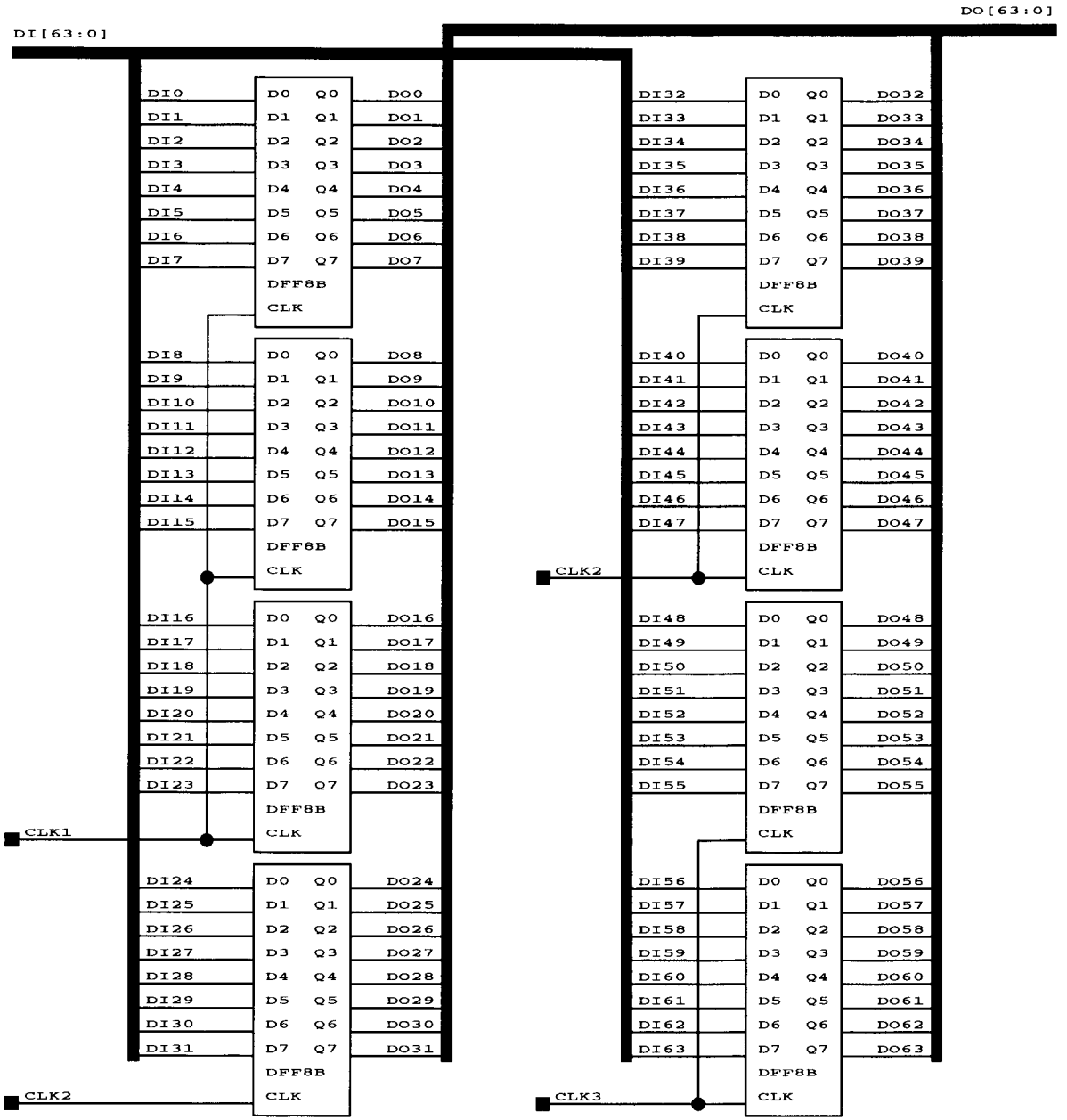
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 ITRINF Register	
Issue 1			
Issue 2			
Issue 3		File: itrinf.1	Page:1 of 2



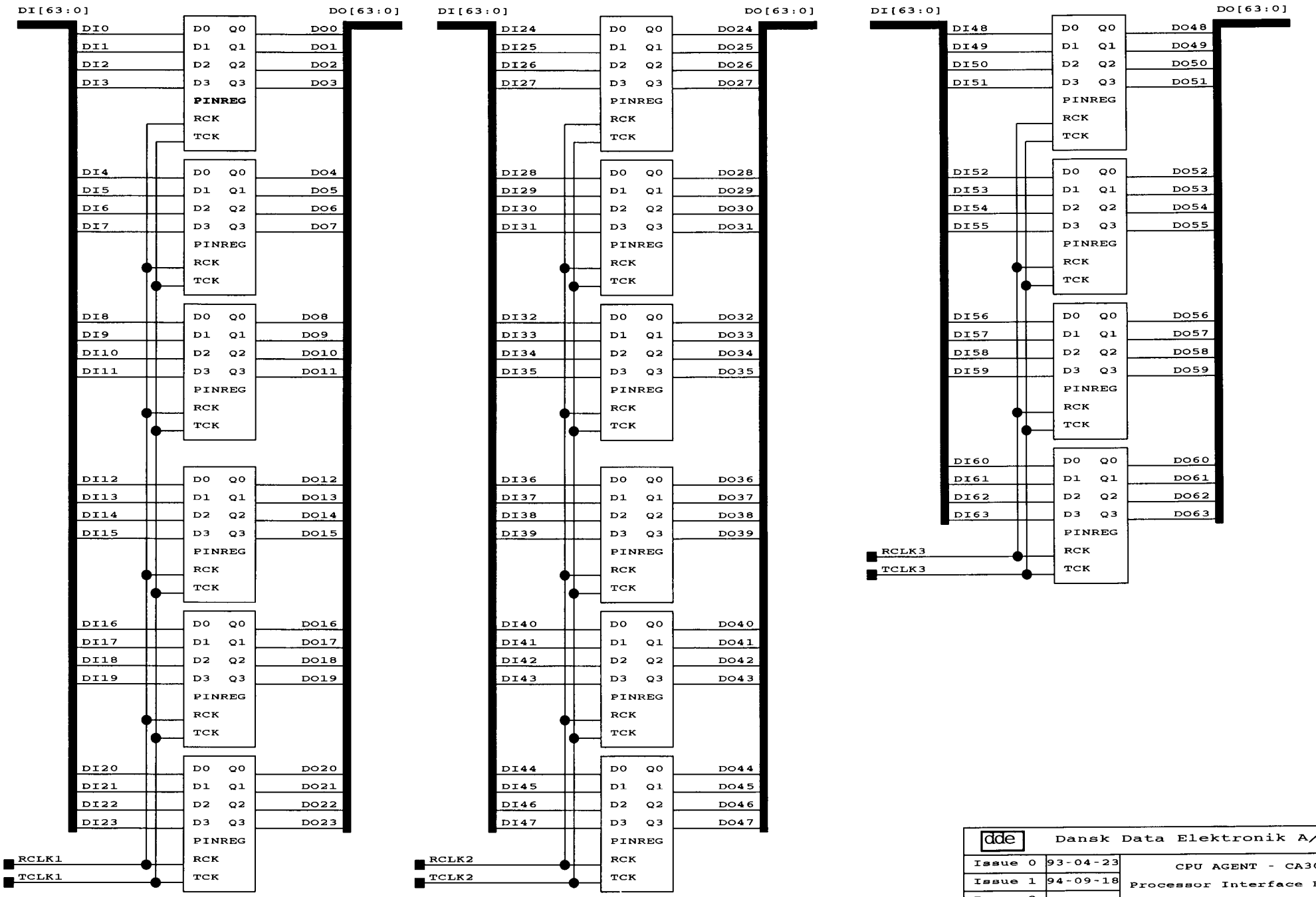
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		ITRINF Register
Issue 2		
Issue 3		File: itrinf.2 Page:2 of 2



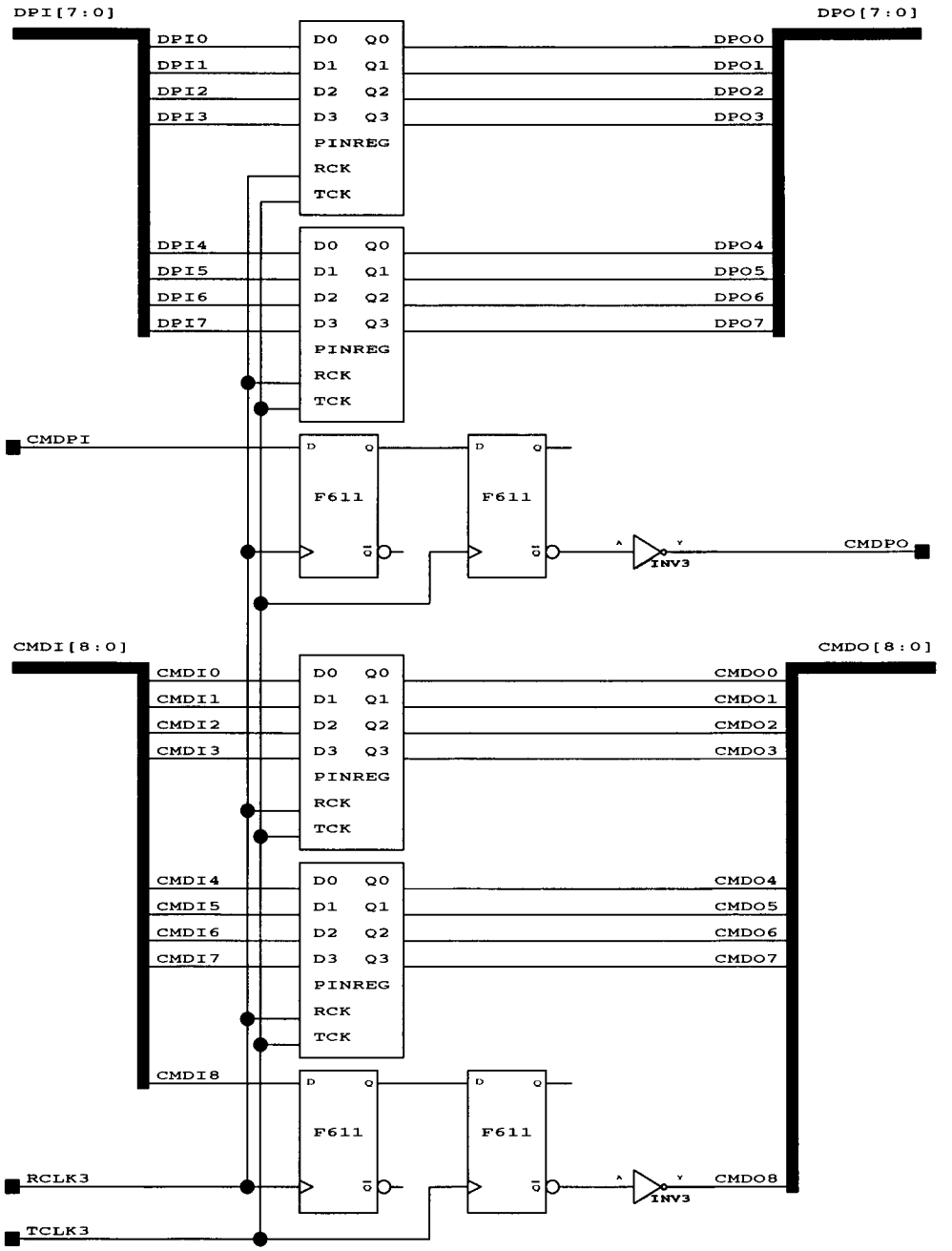
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 INTV Response ID Decoder	
Issue 1			
Issue 2			
Issue 3		File: ivrspid.1	Page: 1 of 1



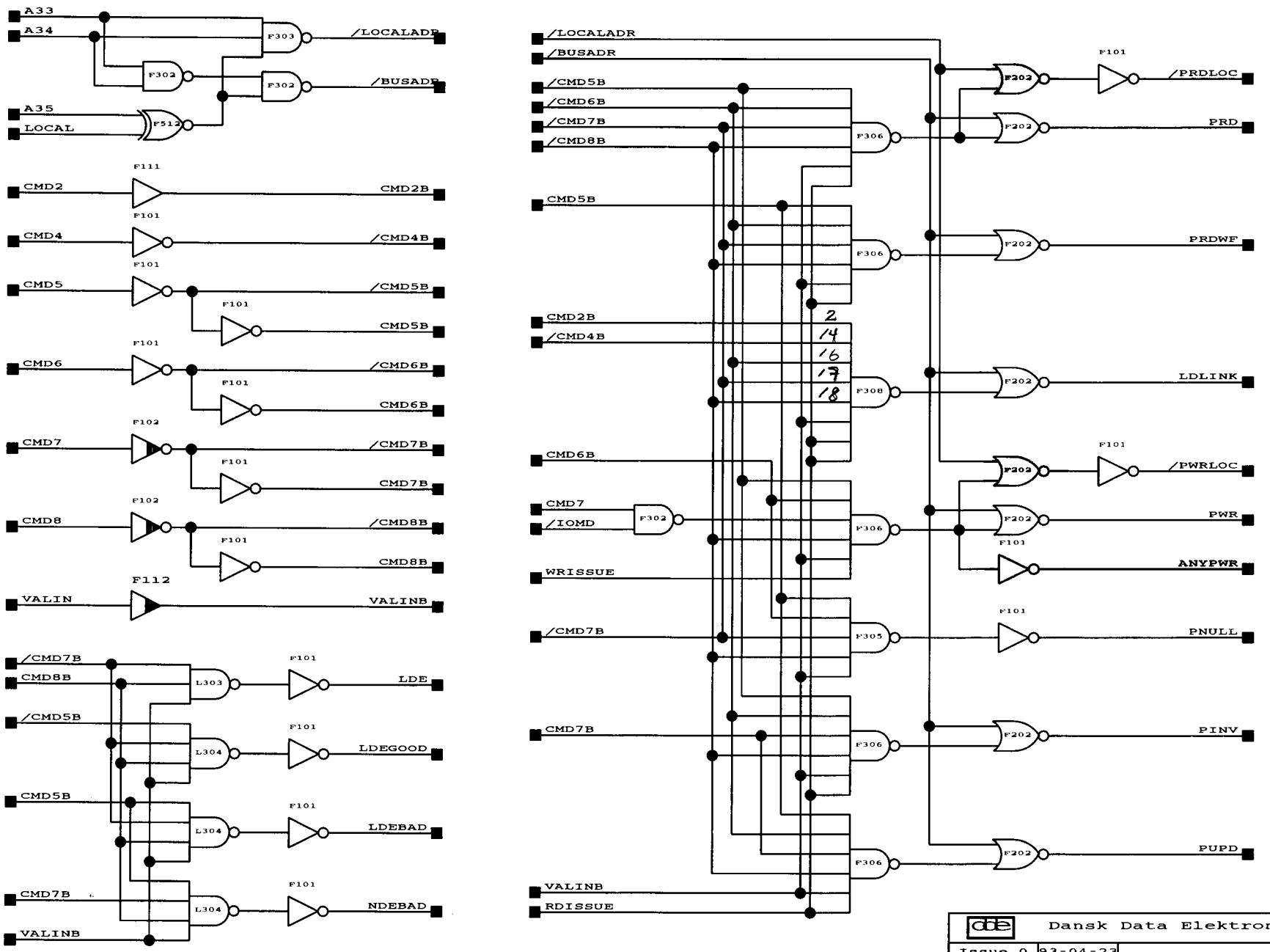
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Bus Output Register
Issue 1		
Issue 2		
Issue 3		File: outreg.1 Page:1 of 1



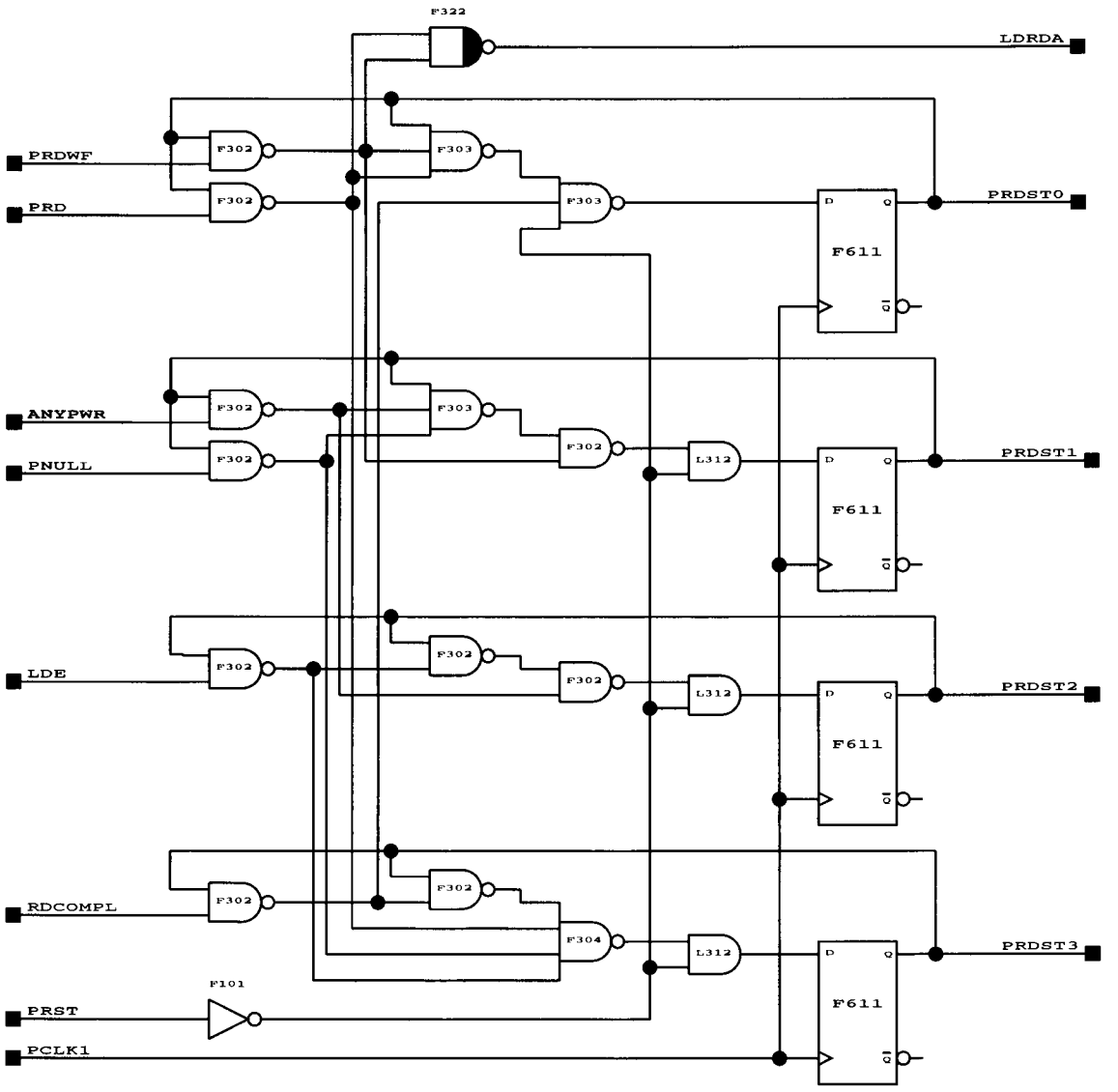
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-18	Processor Interface Buffer
Issue 2		
Issue 3		File: padbuf.1 — Page: 1 of 2



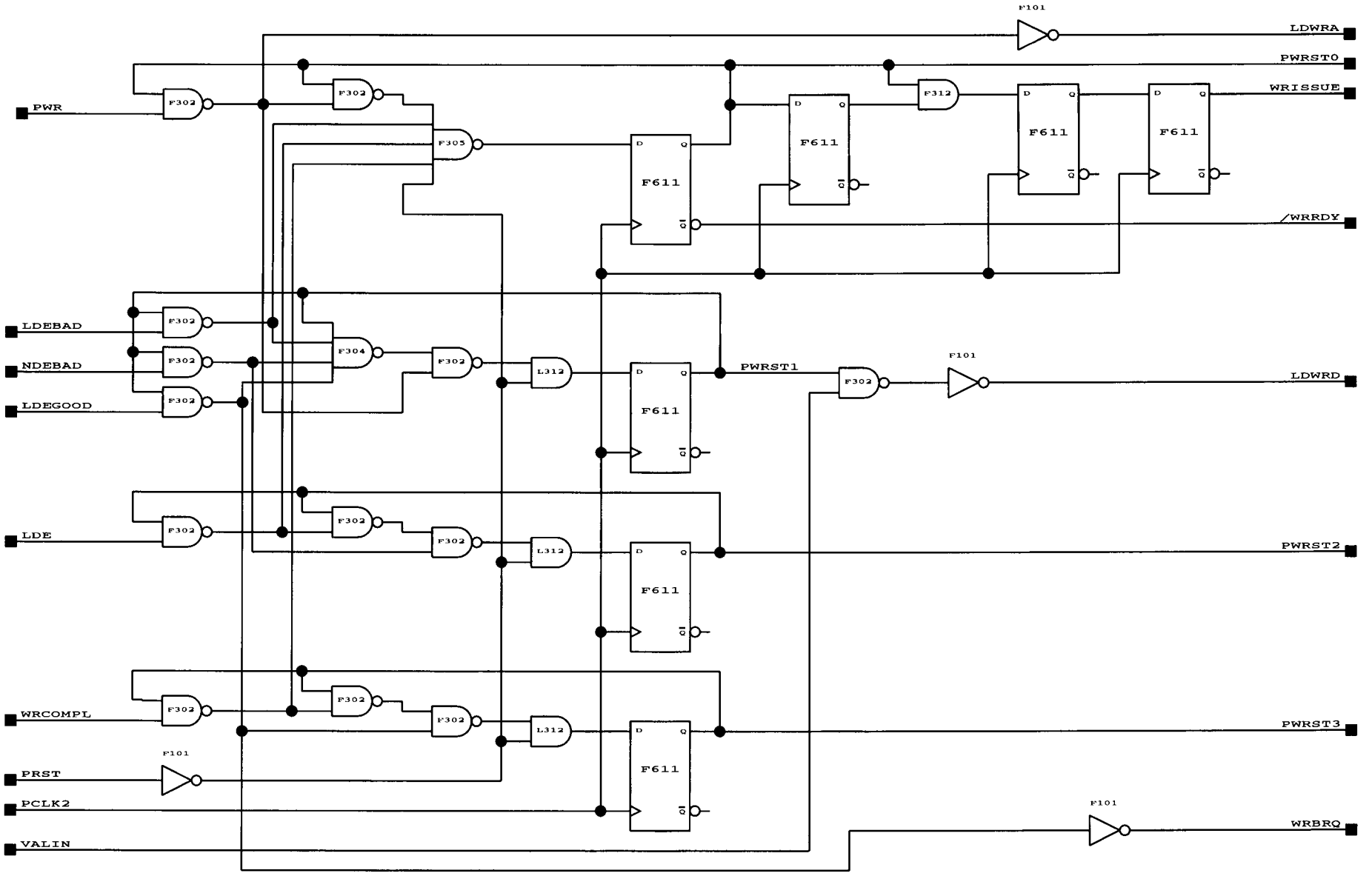
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Processor Interface Buffer	
Issue 1	94-09-18		
Issue 2			
Issue 3		File: padbuf.2	Page: 2 of 2



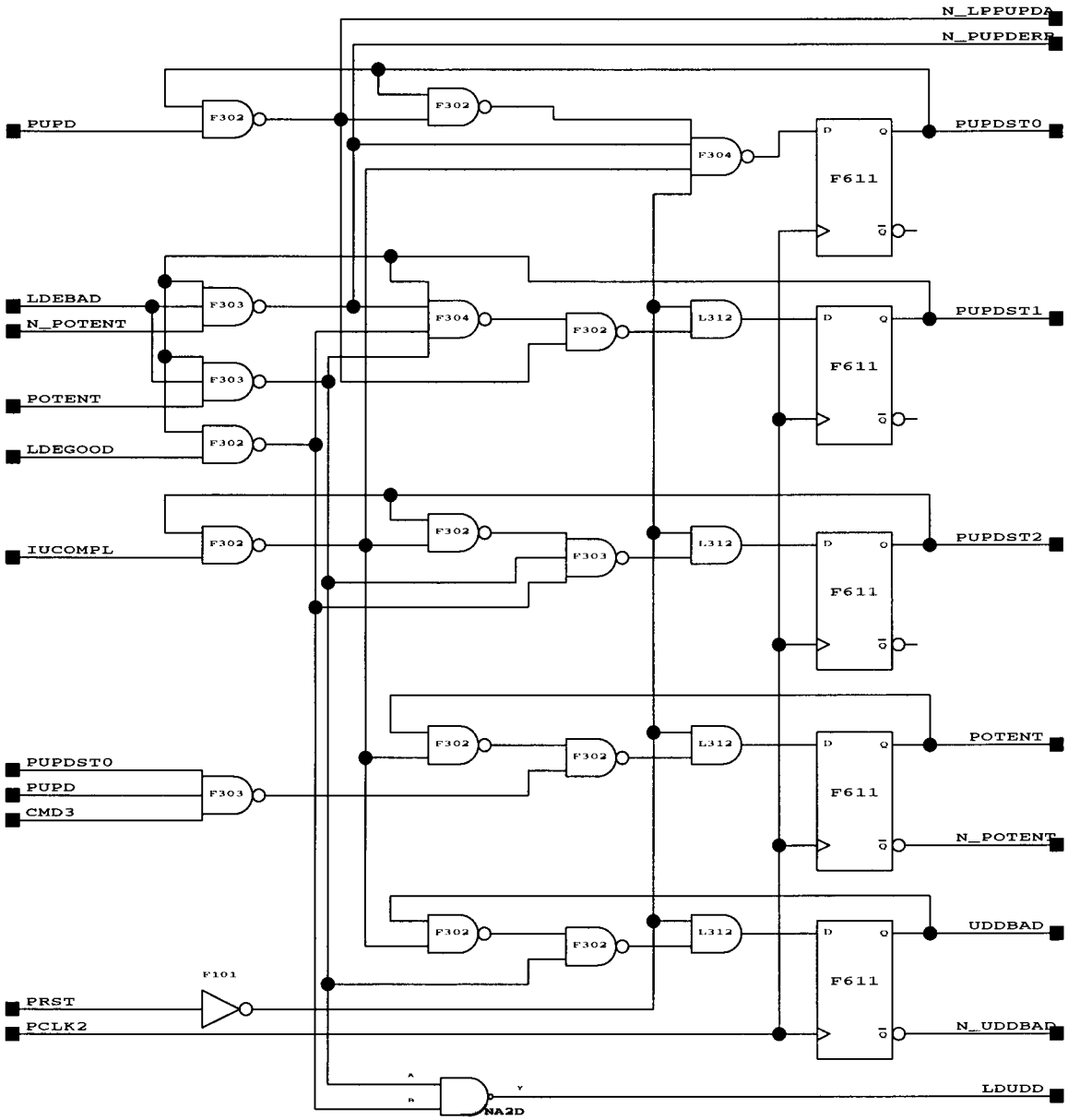
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CPA Command Decoding
Issue 1	94-05-10	
Issue 2		
Issue 3		File: pcmdhnd.1 | Page: 1 of 6



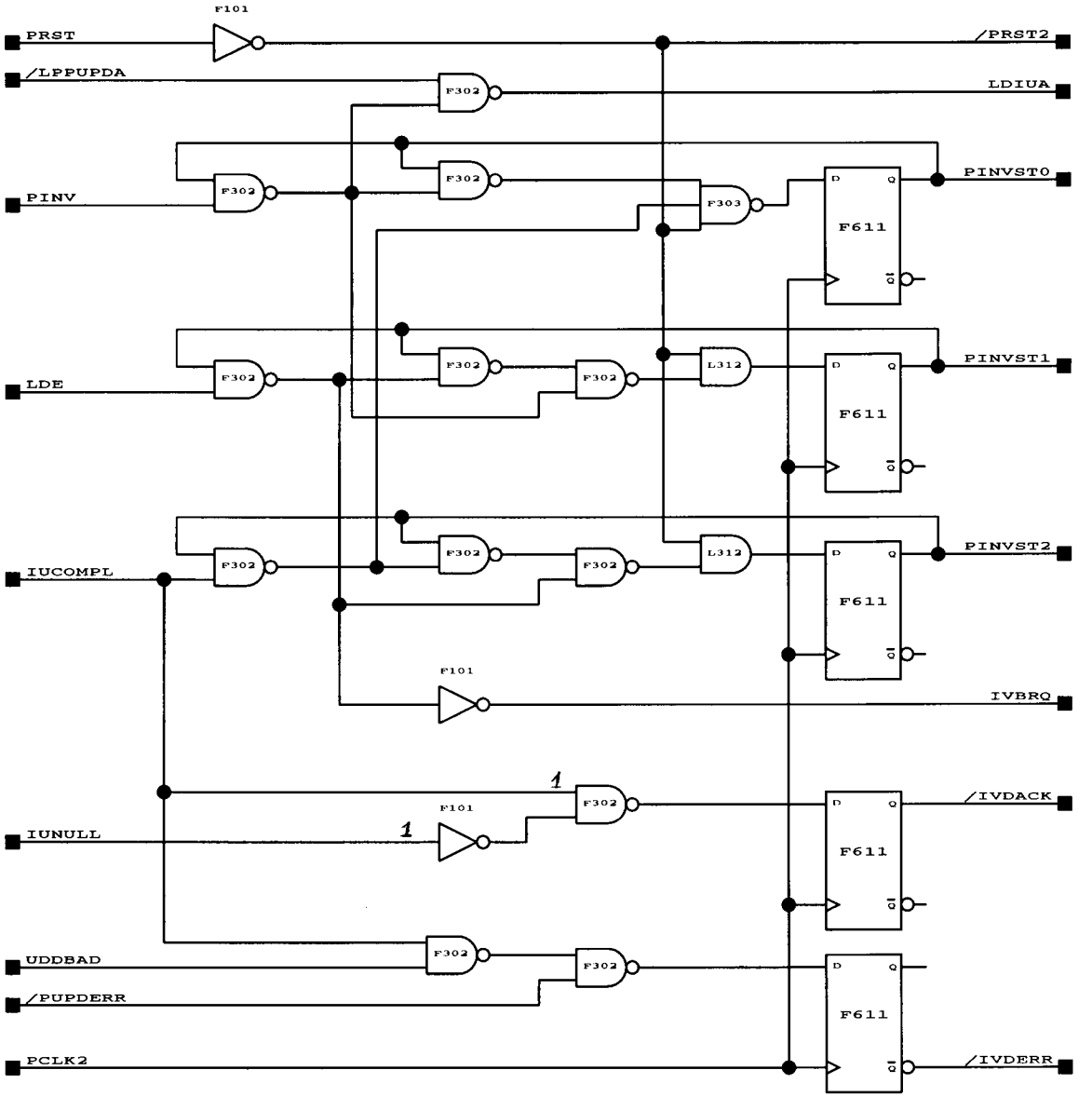
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CPA Proc. Read Req. State Mach.	
Issue 1	94-05-10		
Issue 2			
Issue 3		File: pcmdhnd.2	Page:2 of 6



Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CPA
Issue 1		Proc Write Req State Mach
Issue 2		
Issue 3		File: pcmdhnd.3 Page: 3 of 6

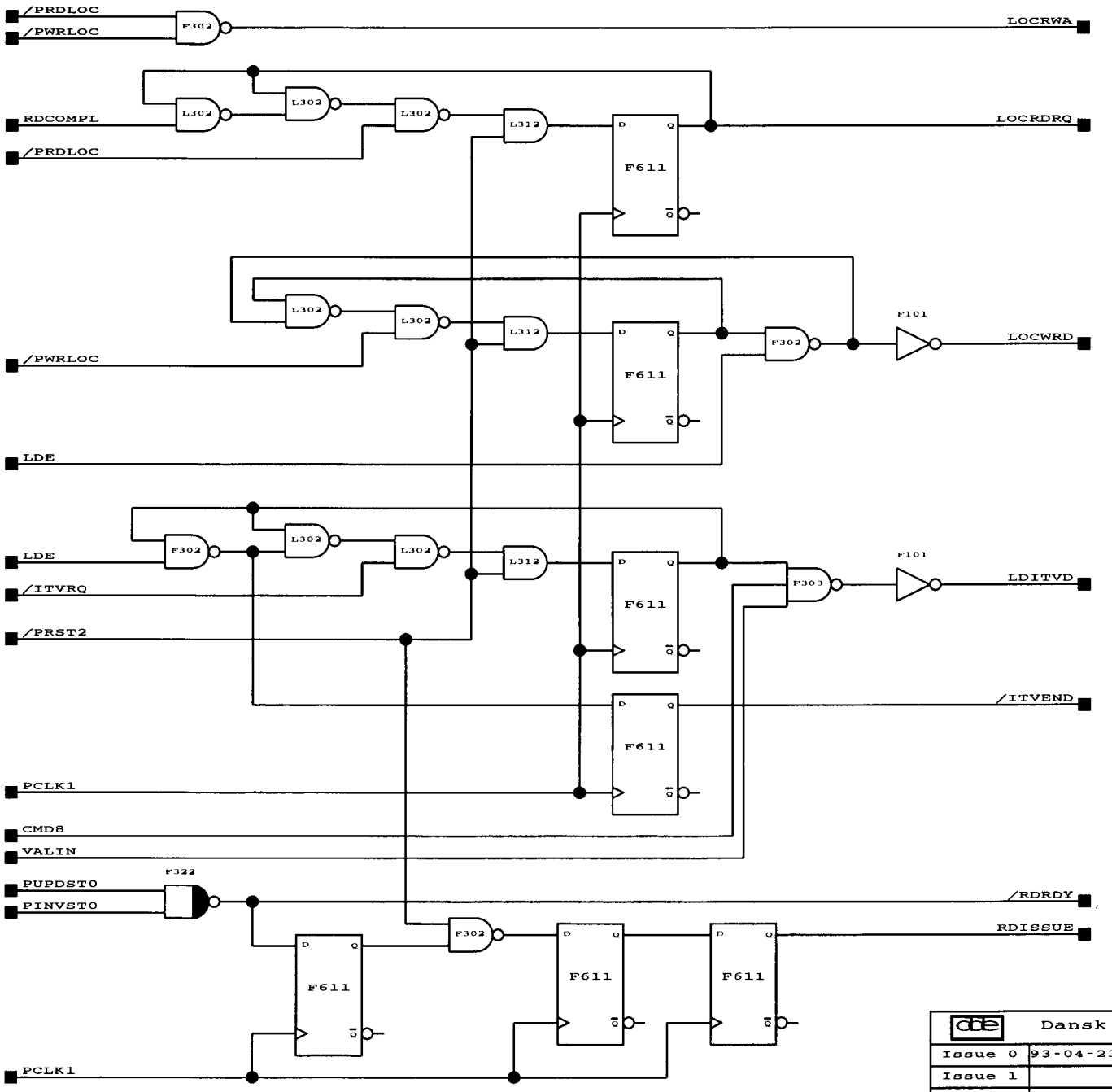


dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CPA
Issue 1	94-09-08	Proc Update Req State Mach
Issue 2		
Issue 3		File: pcmdhnd.4 Page:4 of 6

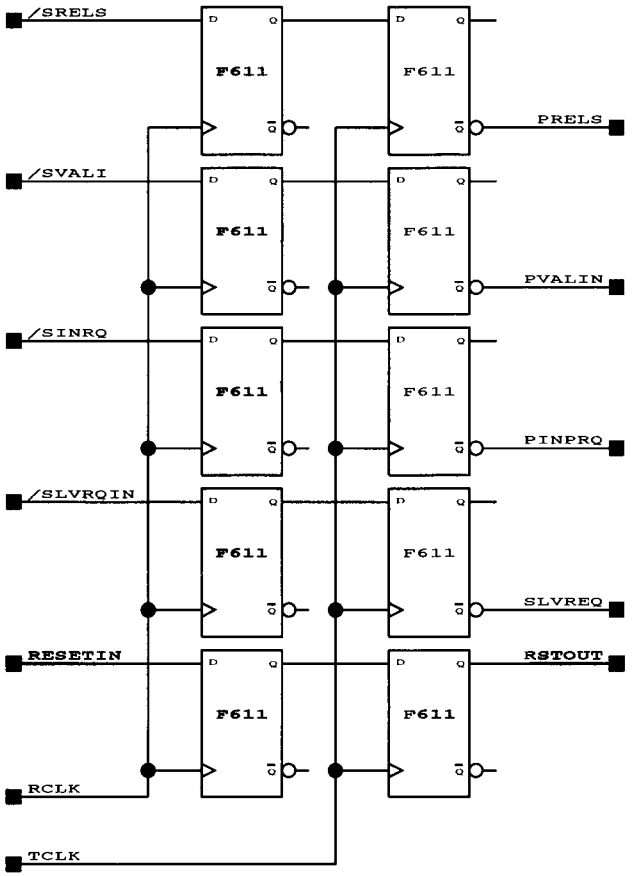


PIUNLFY

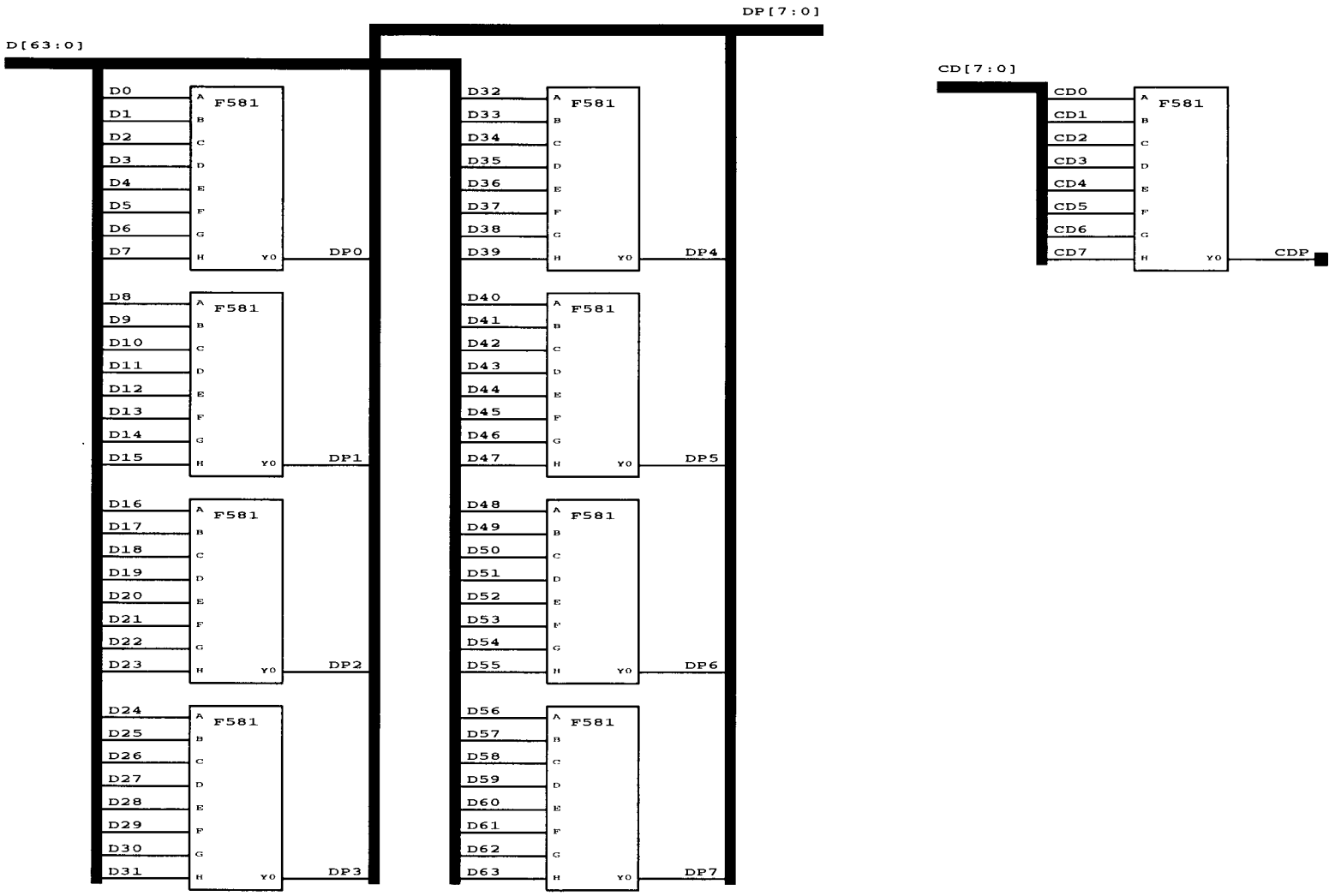
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CPA Proc Invalidate Req St Mach
Issue 1		
Issue 2		
Issue 3		File: pcmdhnd.5 Page:5 of 6



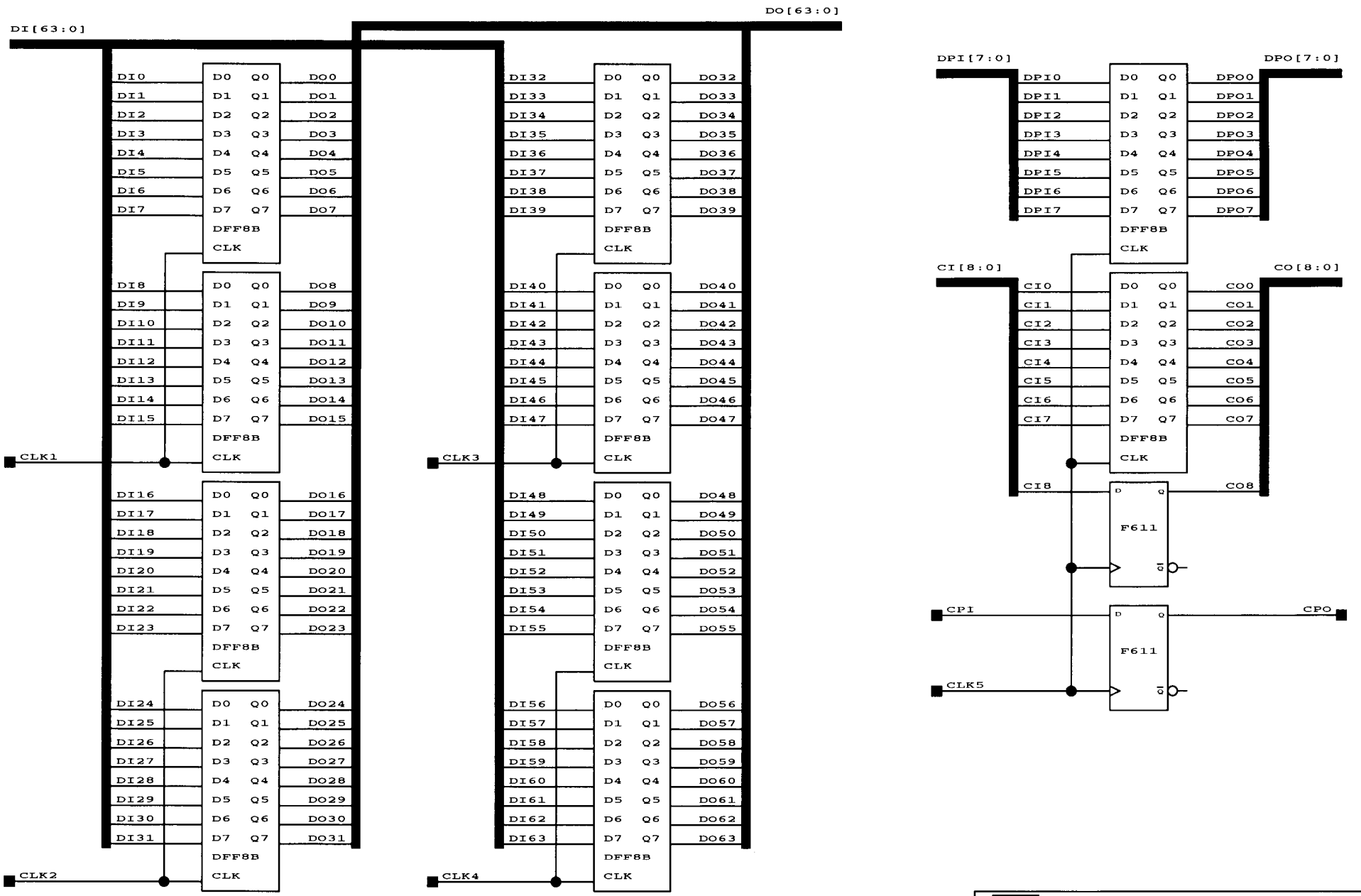
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CPA
Issue 1		Local Read/Write Control
Issue 2		
Issue 3		File: pcmdhnd.6 Page:6 of 6



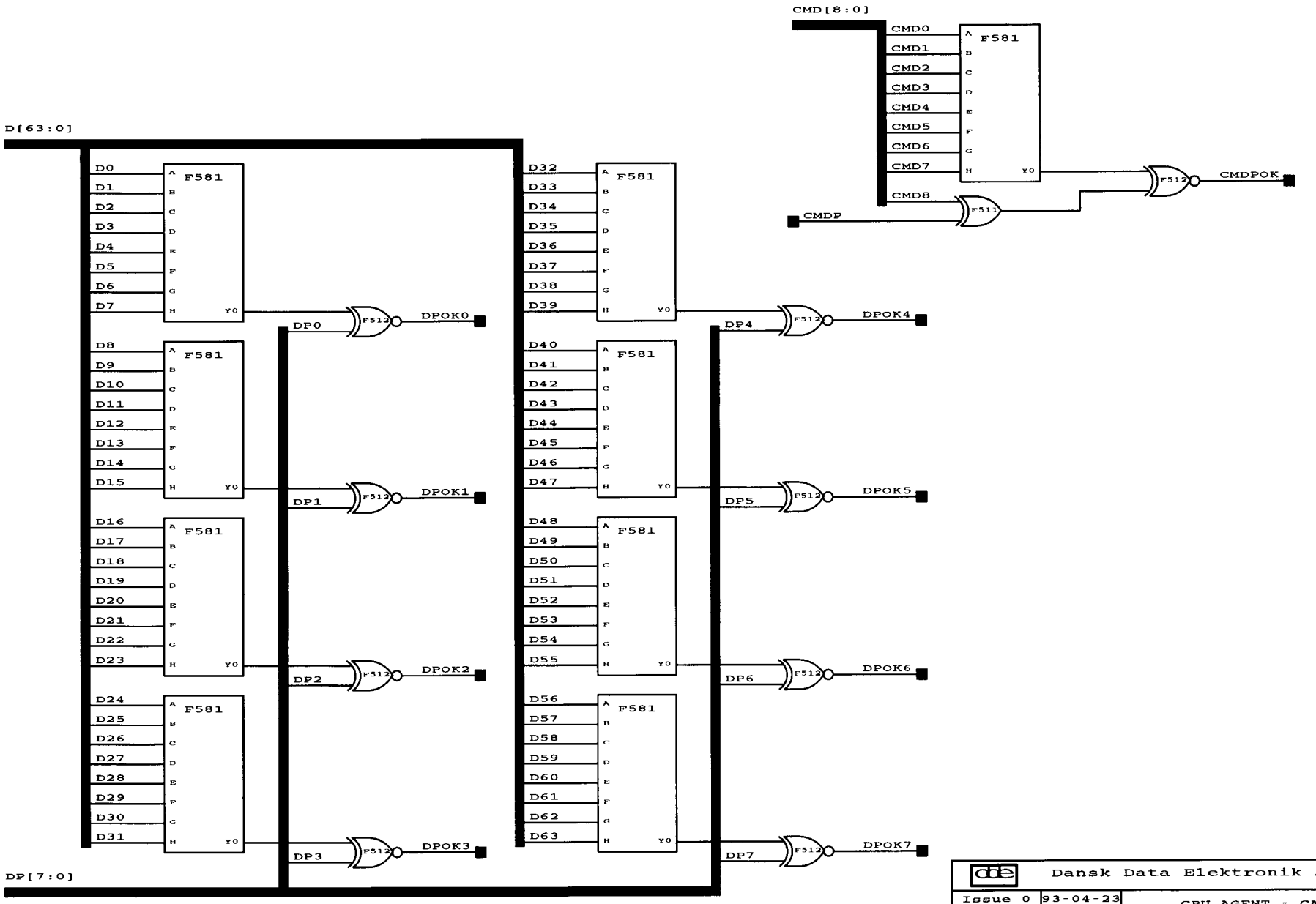
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Bus Interface Buffer
Issue 1	94-07-19	
Issue 2		
Issue 3		File: pctrbuf.1 | Page: 1 of 1



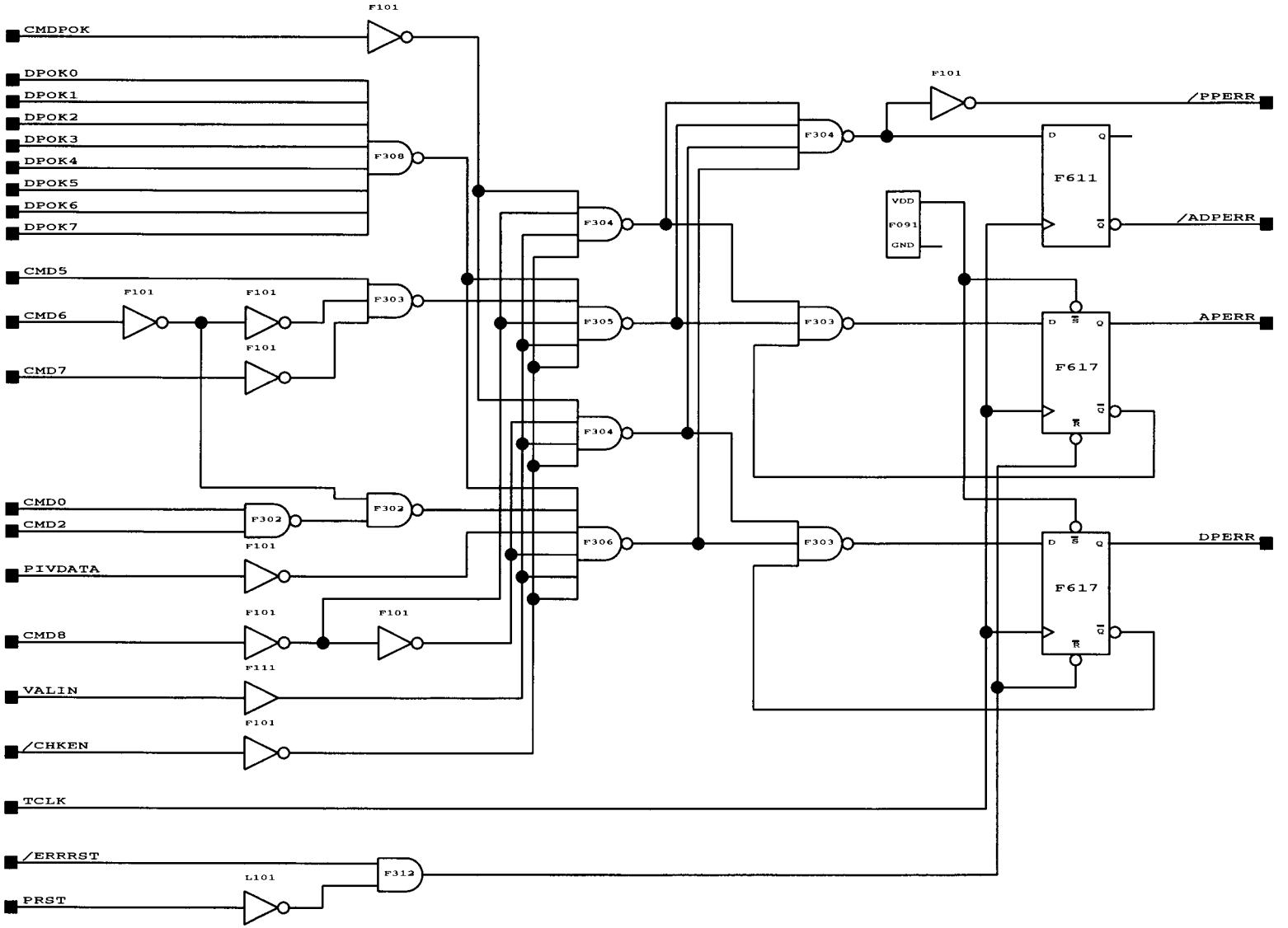
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Even Parity Generator	
Issue 1			
Issue 2			
Issue 3		File: pgen.1	Page: 1 of 1



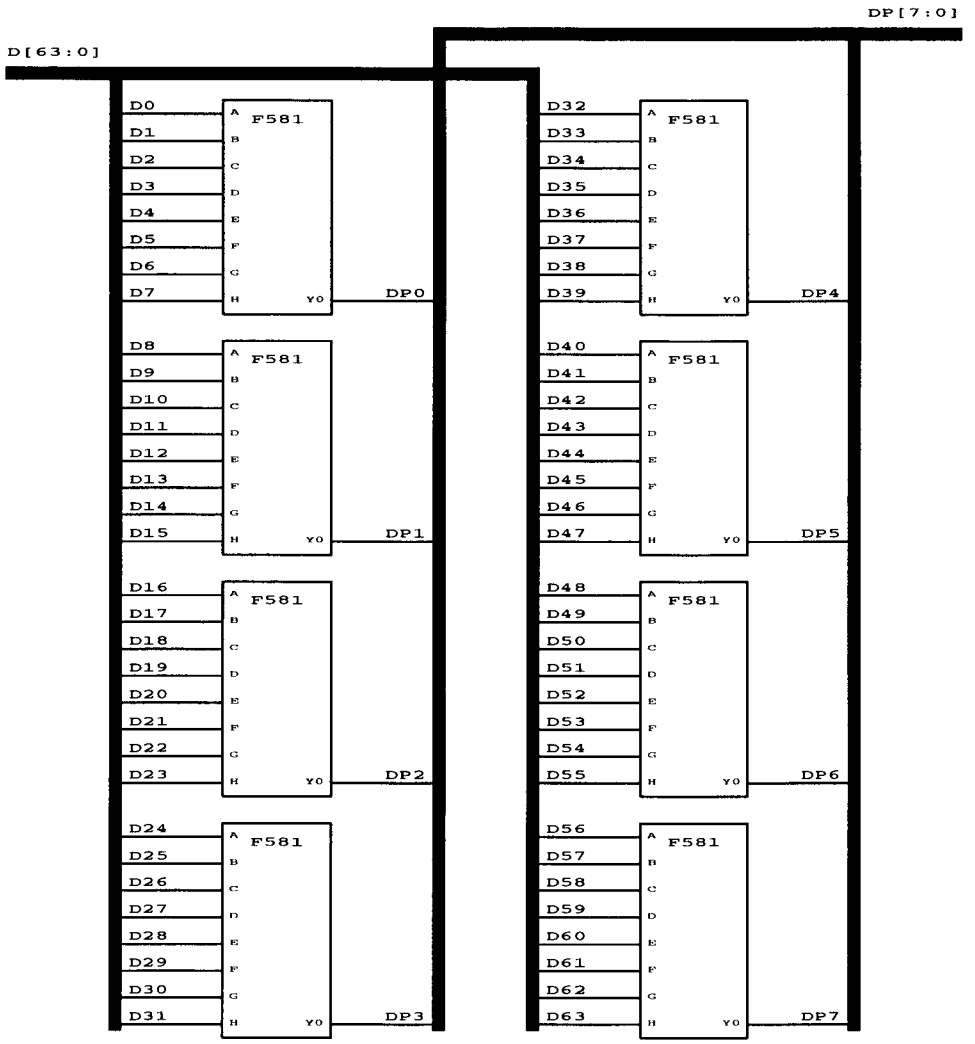
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Processor Output Register
Issue 2		
Issue 3		File: poutreg.1 Page:1 of 1

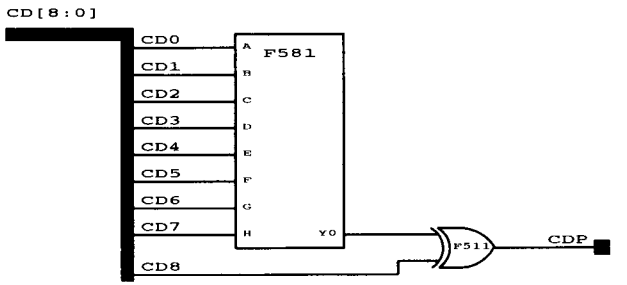


Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Processor Parity Checker
Issue 1		
Issue 2		
Issue 3		File: ppchk.1 | Page: 1 of 2

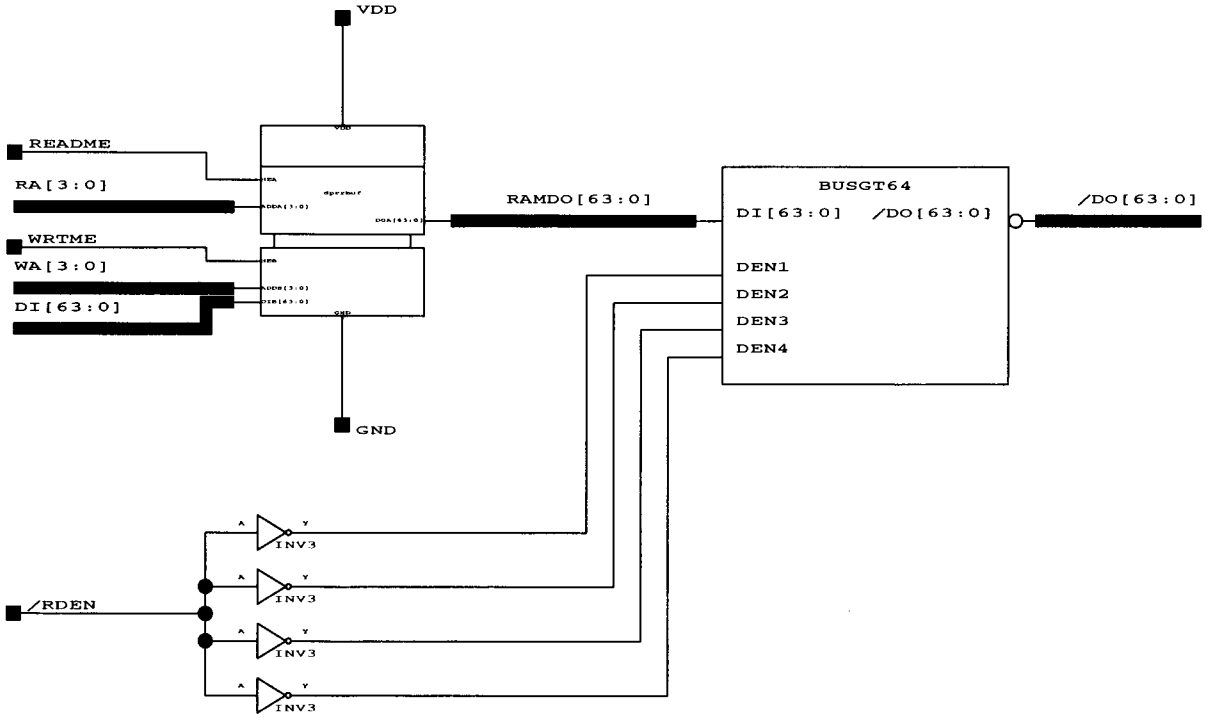


Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Processor Parity Checker	
Issue 1	94-06-27		
Issue 2			
Issue 3		File: ppchk.2	Page: 2 of 2

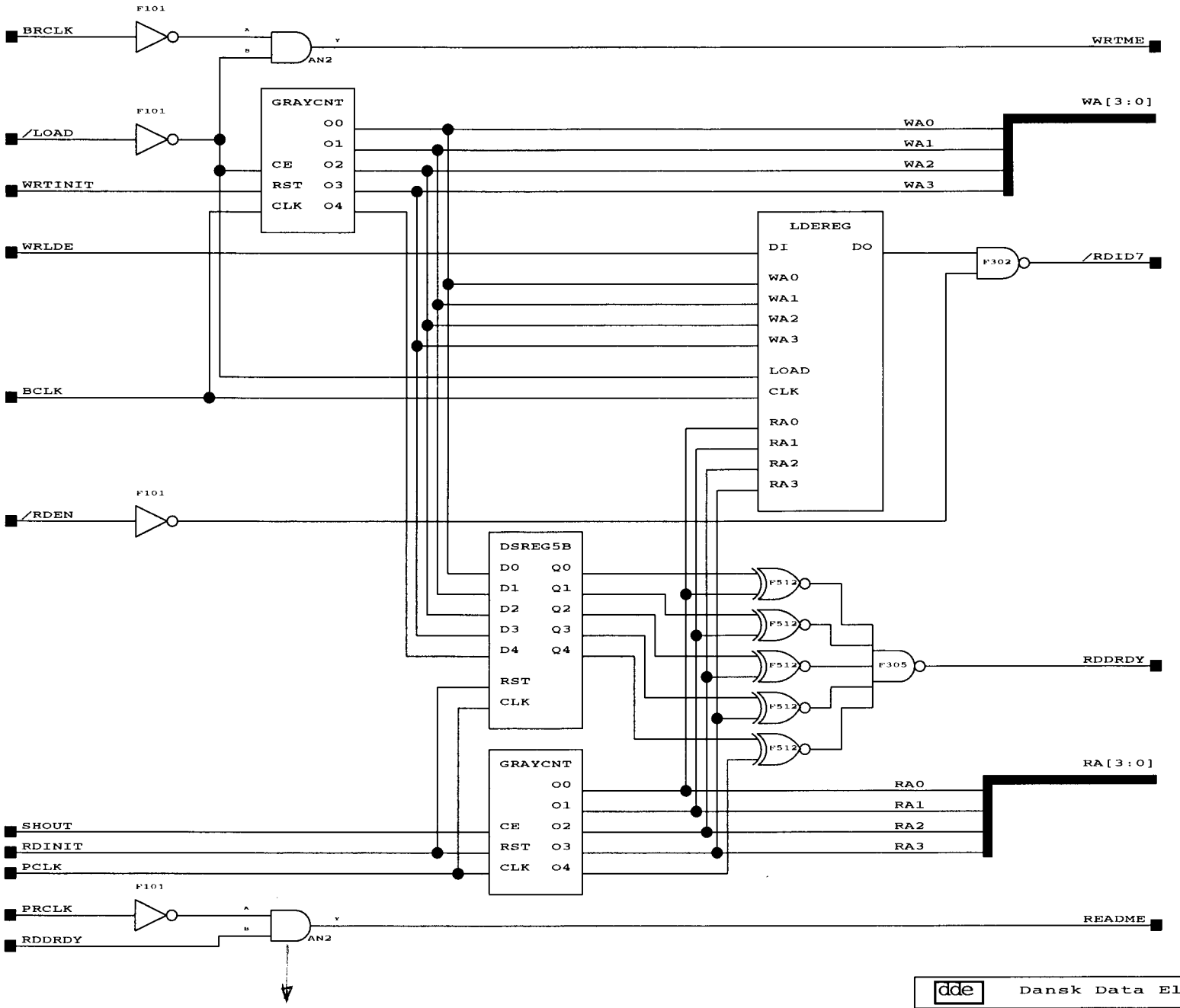




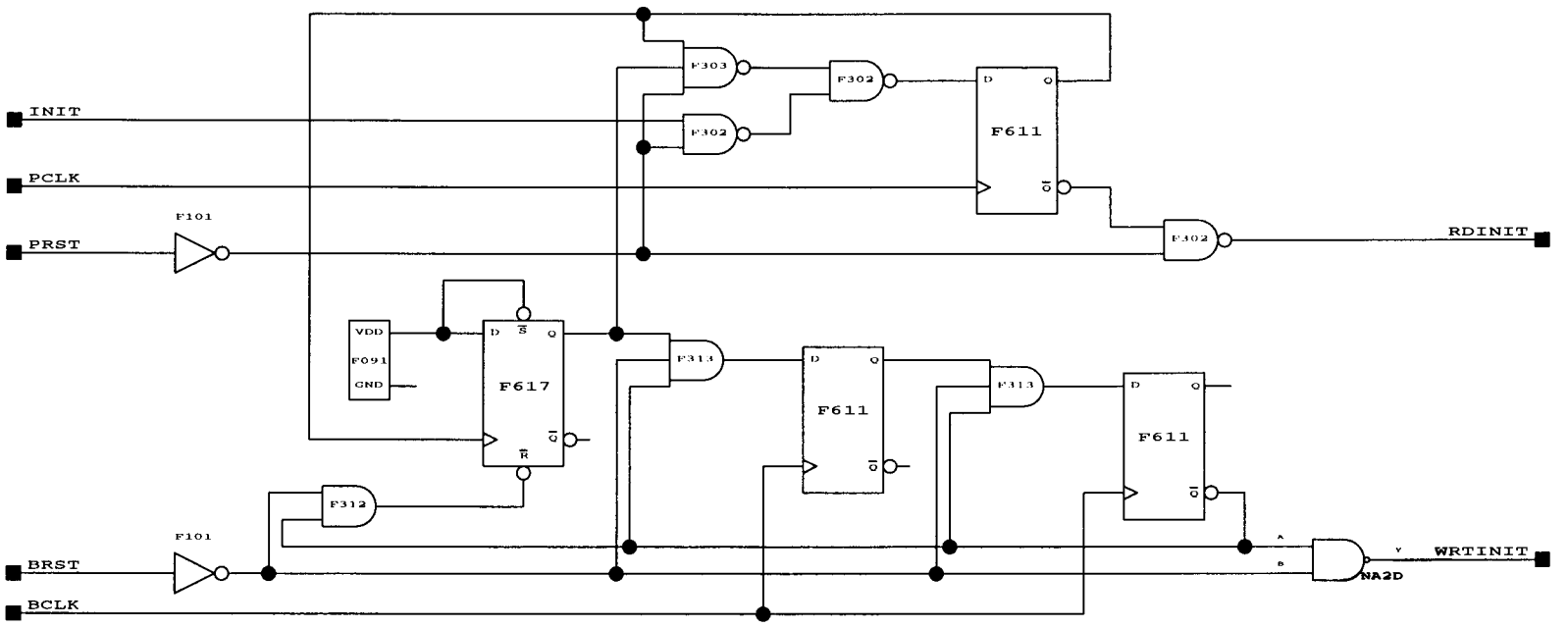
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Even Parity Generator	
Issue 1			
Issue 2			
Issue 3		File: ppgen.1	Page: 1 of 1



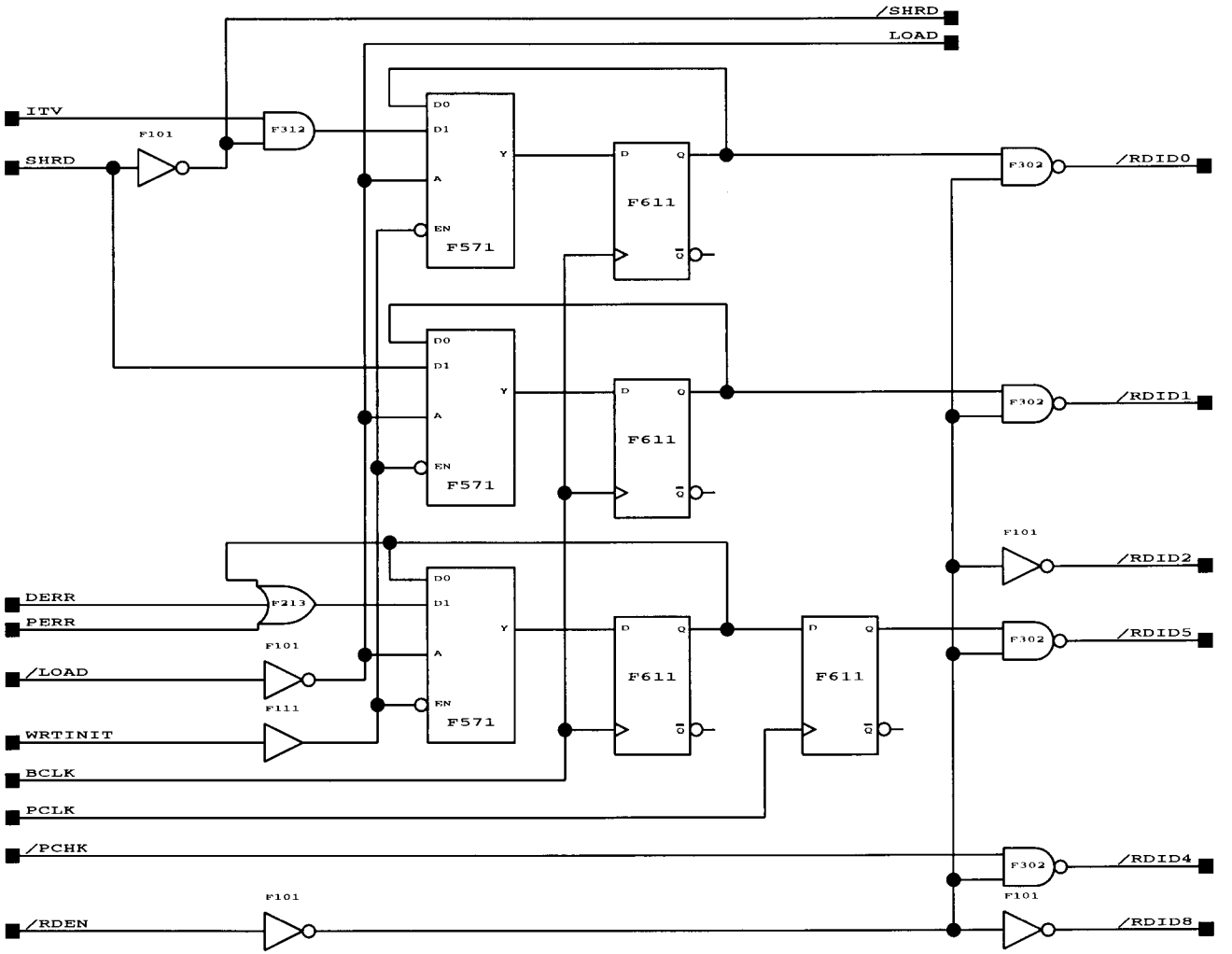
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1	93-07-26	Read Response FIFO	
Issue 2			
Issue 3		File: rdrspff.1	Page: 1 of 3



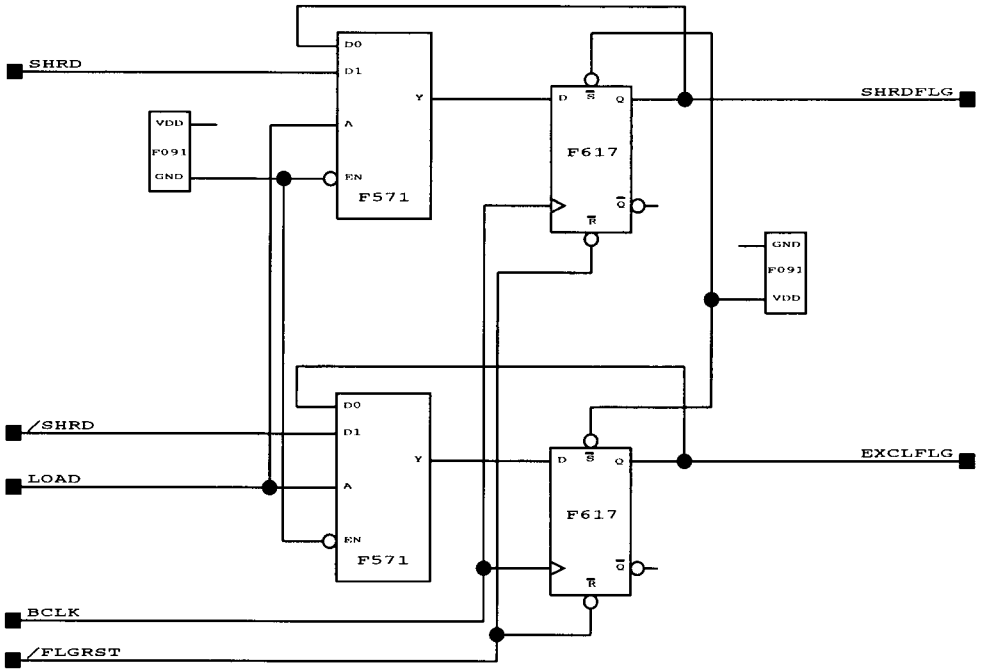
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-26	Address Counters
Issue 2		
Issue 3		File: rdrspff.2 | Page: 2 of 3



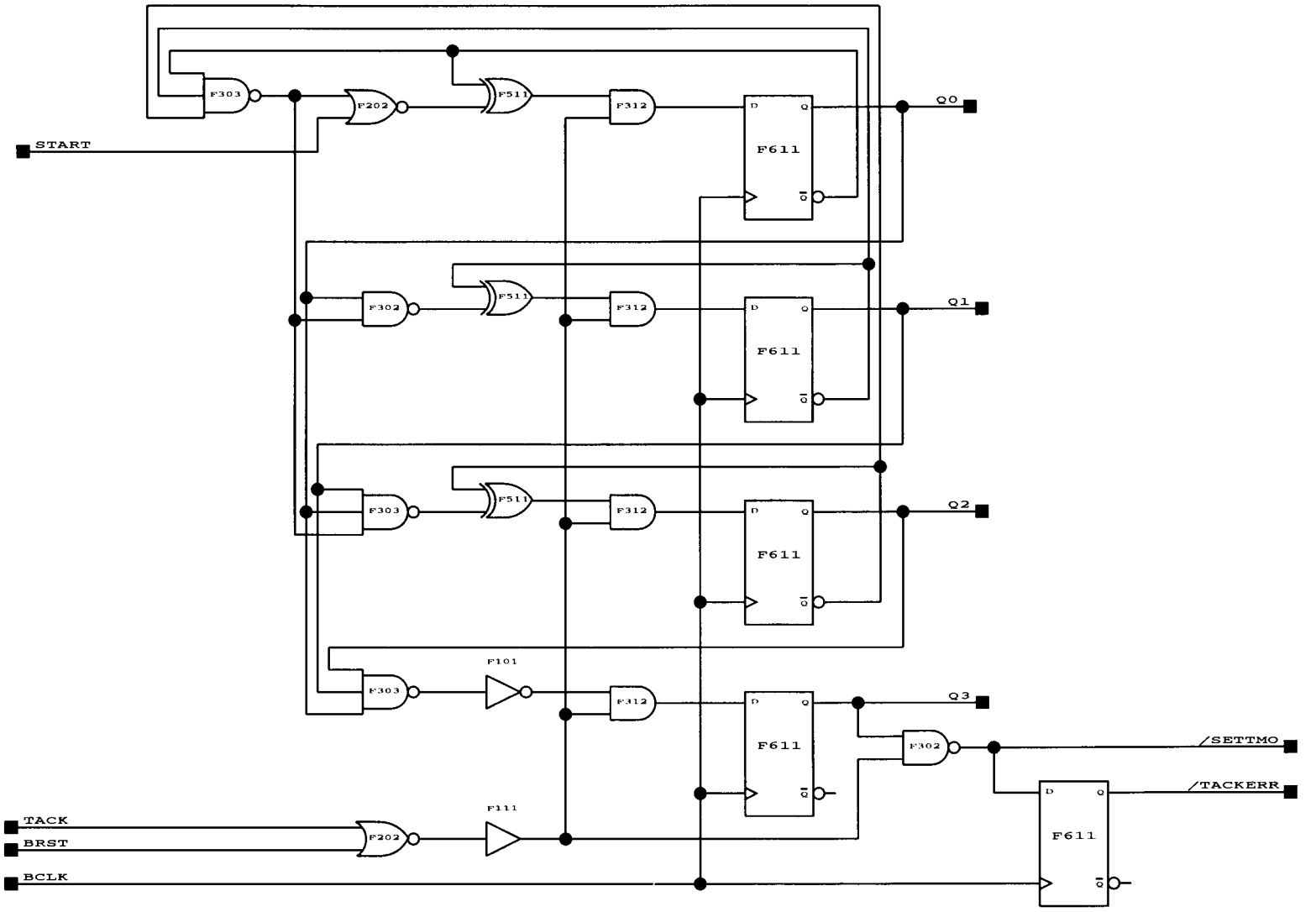
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-08	Initialization Circuit
Issue 2		
Issue 3		File: rdrspff.3 Page: 3 of 3



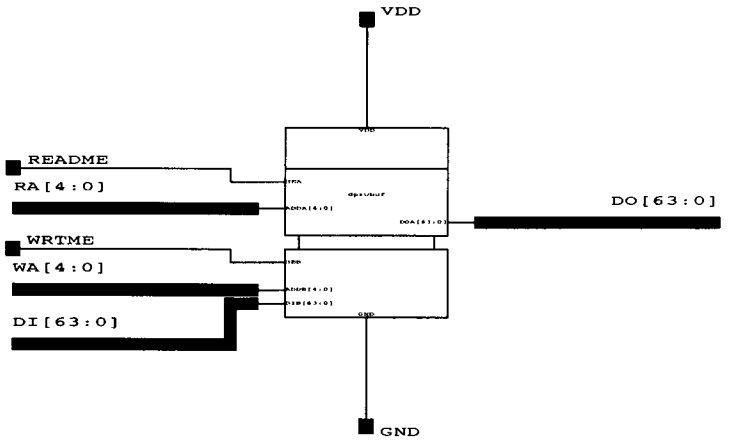
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Read Response Data ID	
Issue 1			
Issue 2			
Issue 3		File: rdrspid.1	Page: 1 of 1



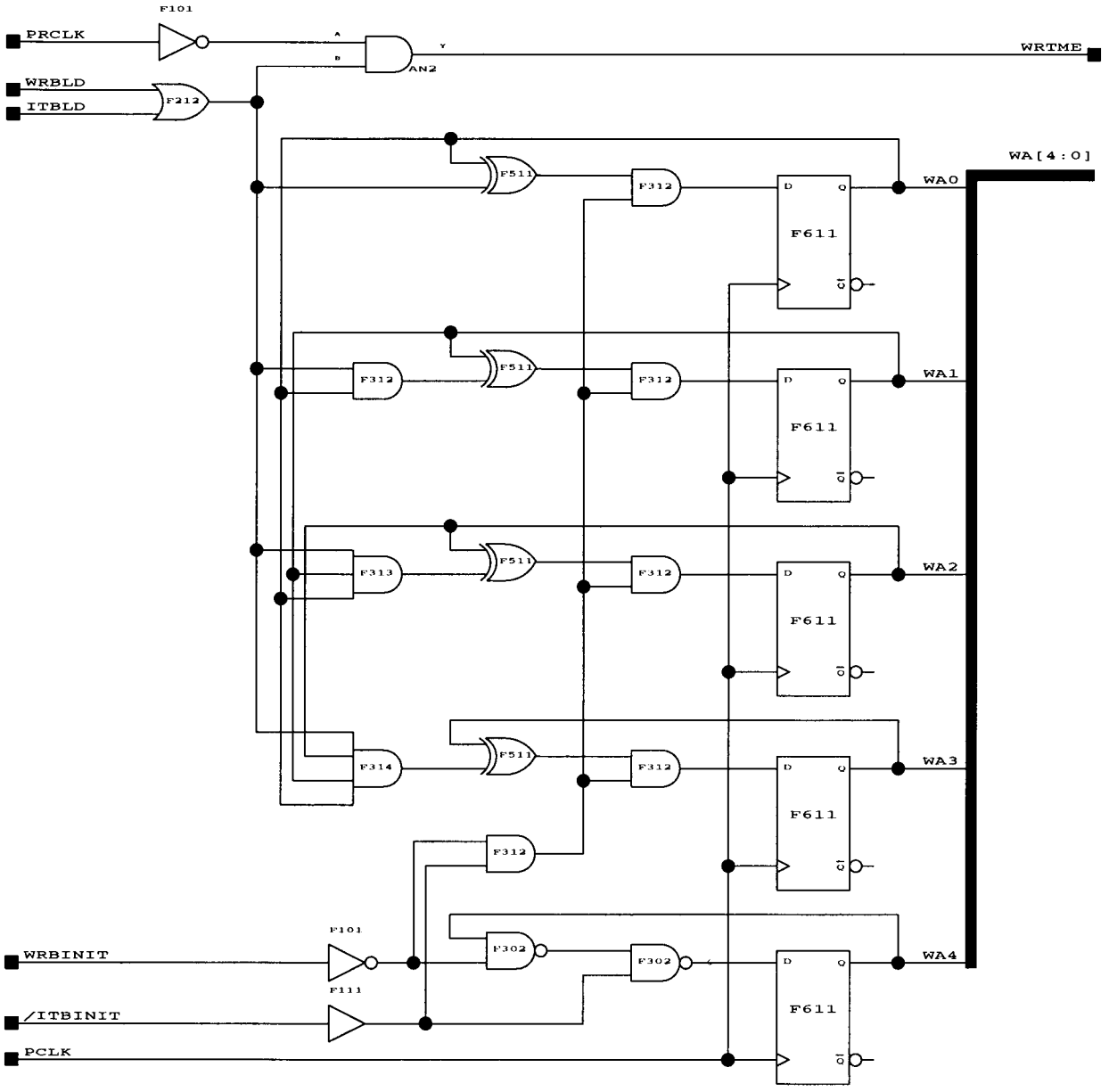
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Read Response Data ID	
Issue 1			
Issue 2			
Issue 3		File: rdrspid.2	Page: 2 of 2



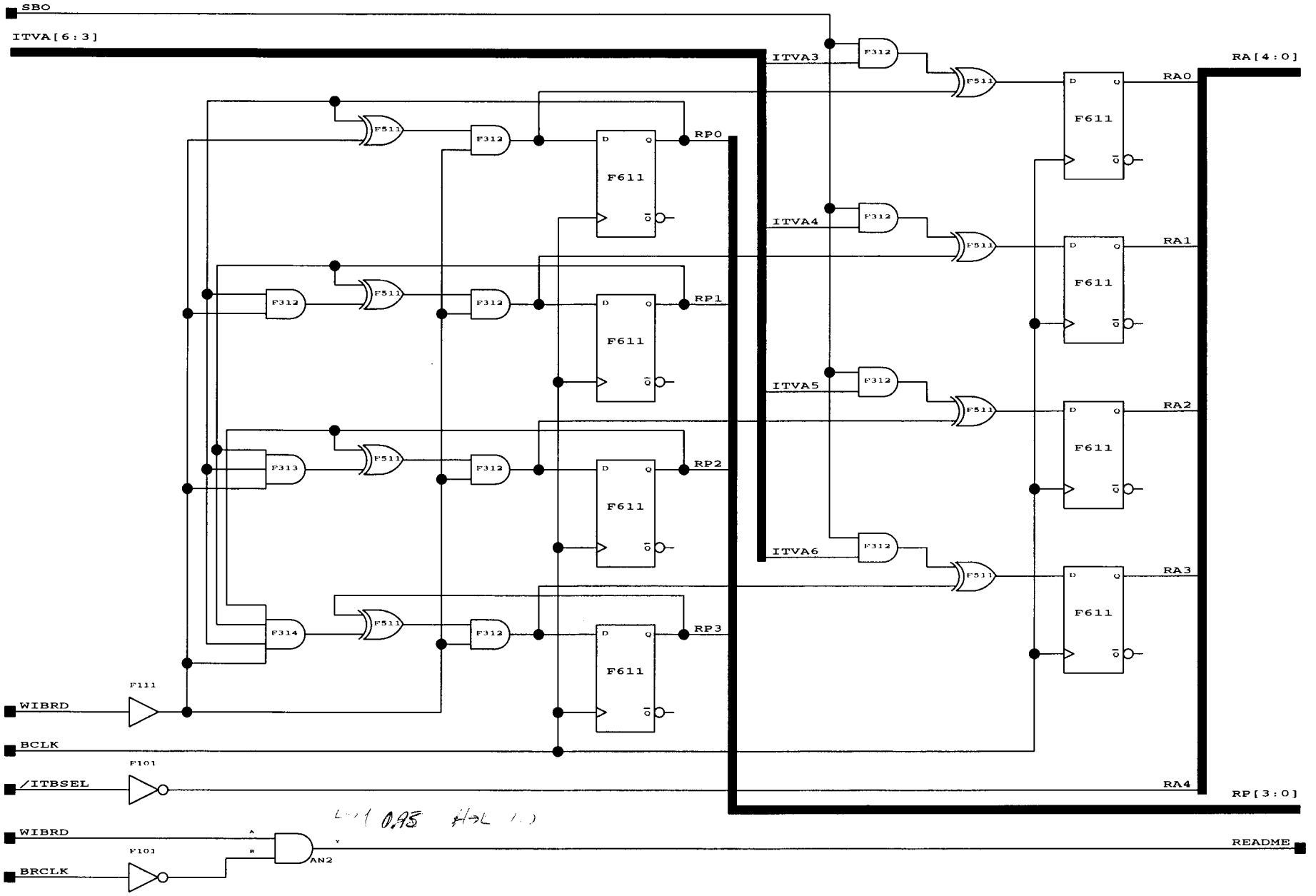
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 TACK Time Out Counter	
Issue 1			
Issue 2			
Issue 3		File: tacktmo.1	Page:1 of 1



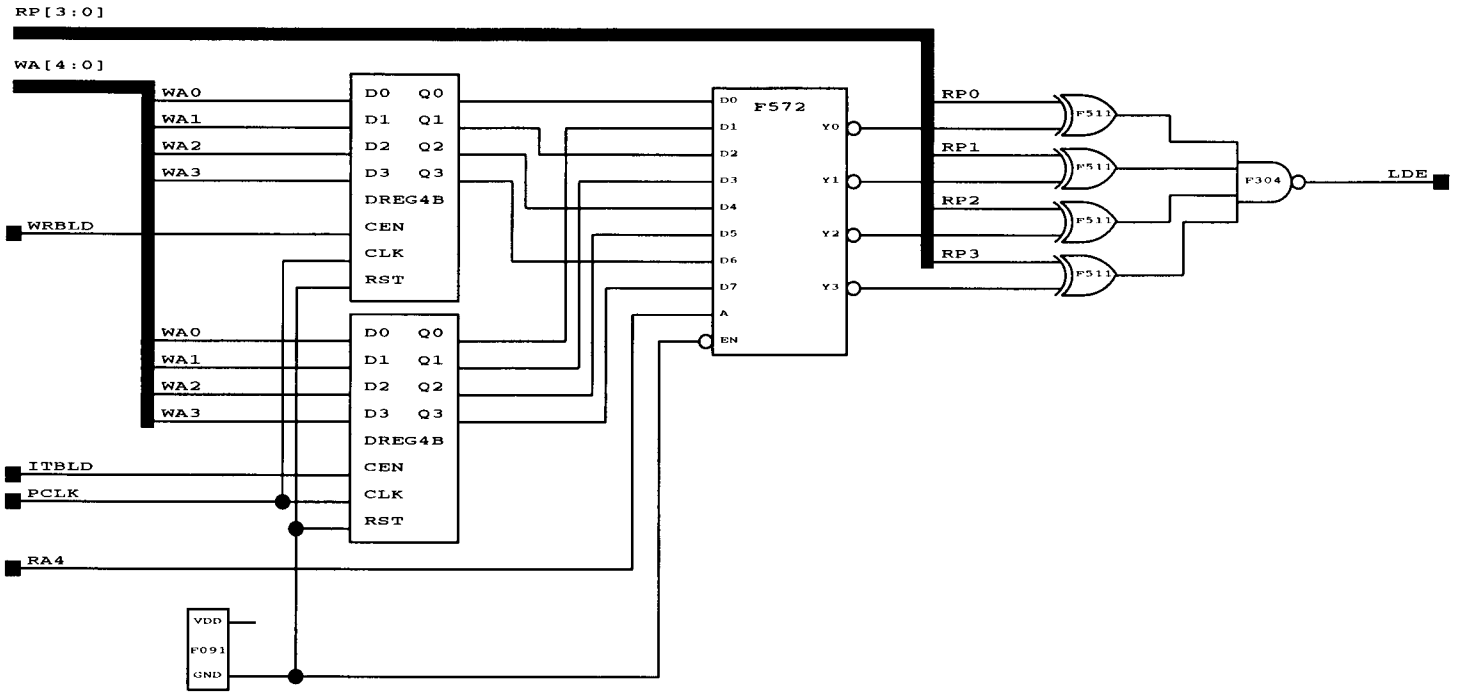
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1	94-07-26	Write/Intervent Data Buffer	
Issue 2			
Issue 3		File: widbuf.1	Page: 1 of 4



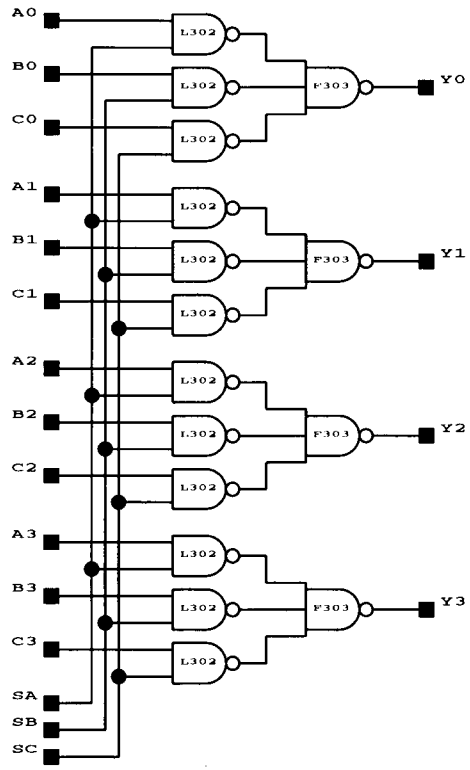
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-26	Write Address Counter
Issue 2		
Issue 3		File: widbuf.2 Page: 2 of 4



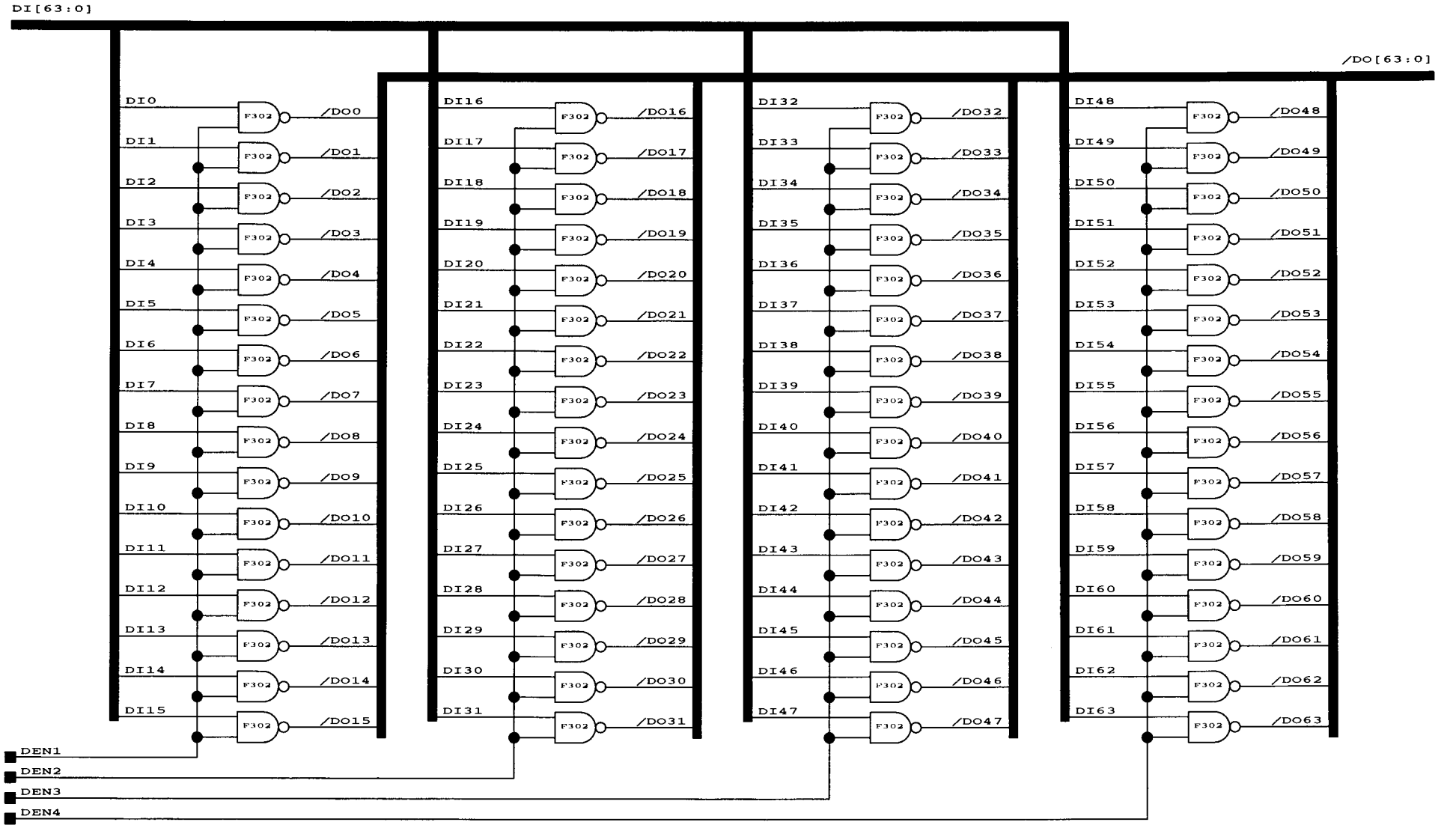
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-26	Read Address Counter
Issue 2		
Issue 3		File: widbuf.3 Page: 3 of 4



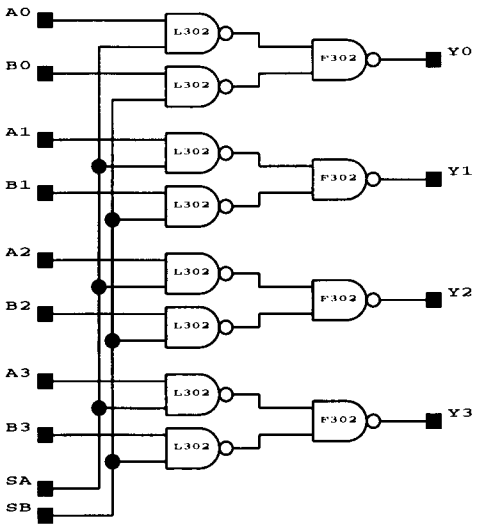
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 LDE Generation	
Issue 1			
Issue 2			
Issue 3		File: widbuf.4	Page: 4 of 4



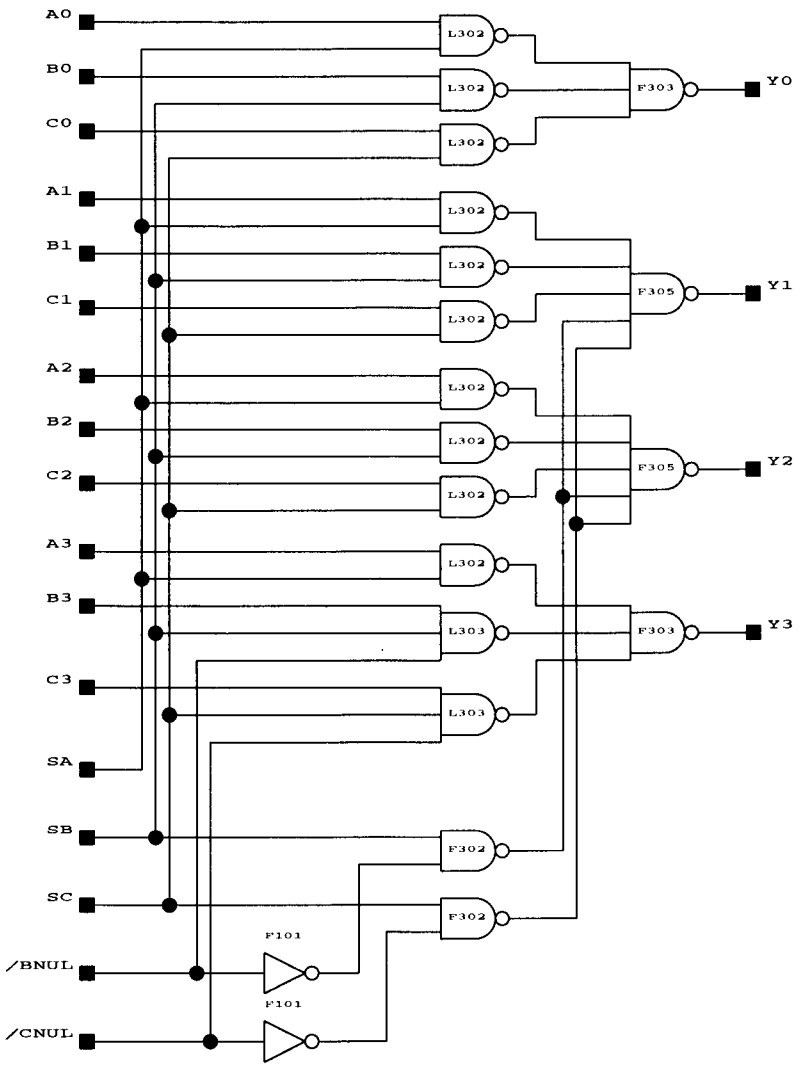
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 AMUX Multiplexer	
Issue 1			
Issue 2			
Issue 3		File: amux.1	Page: 1 of 1



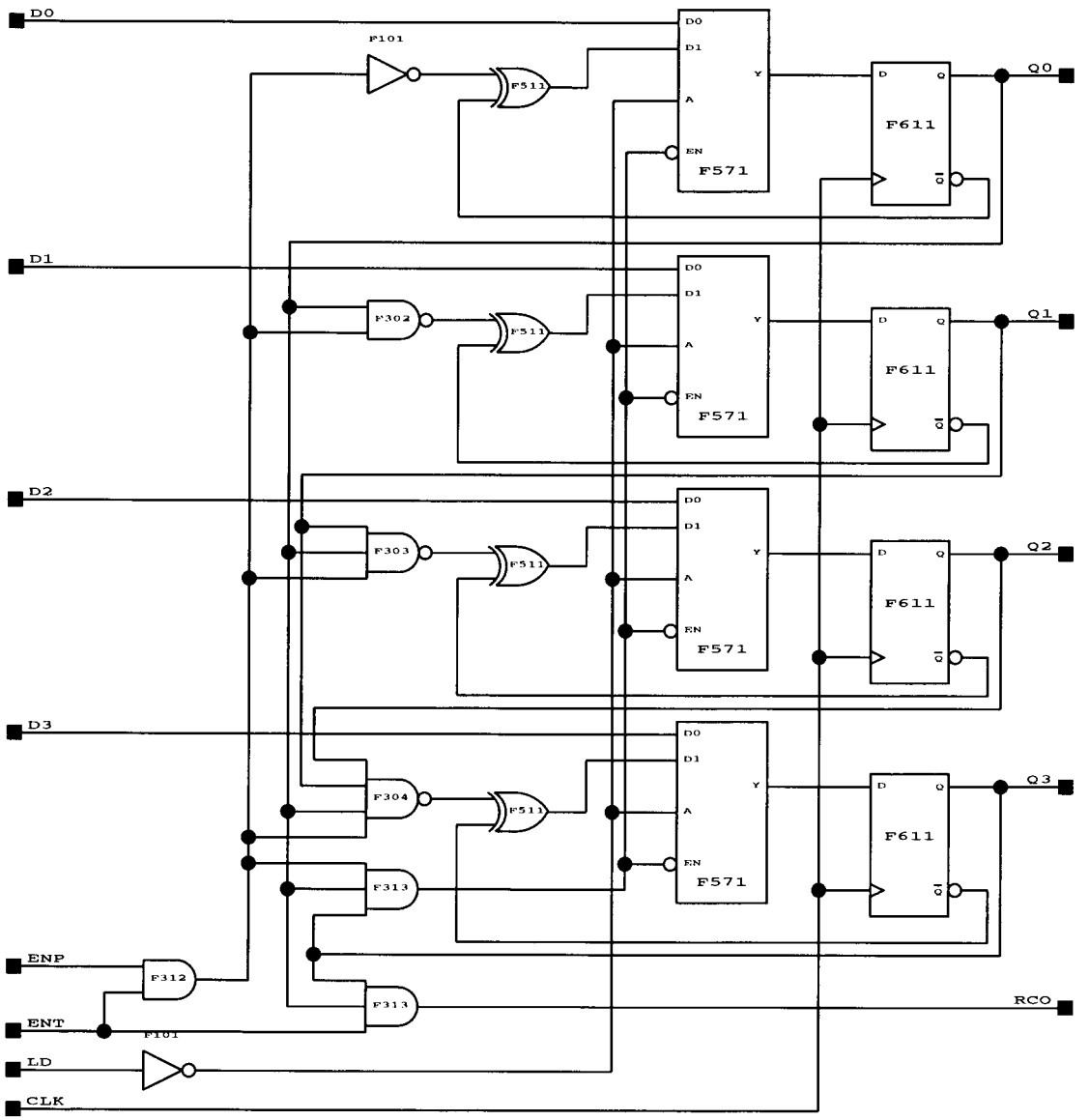
dde	Dansk Data Elektronik A/S	
Issue 0	94-07-26	CPU AGENT - CA302 64-Bit Bus Gate
Issue 1		
Issue 2		
Issue 3		File: busgt64.1 | Page: 1 of 1



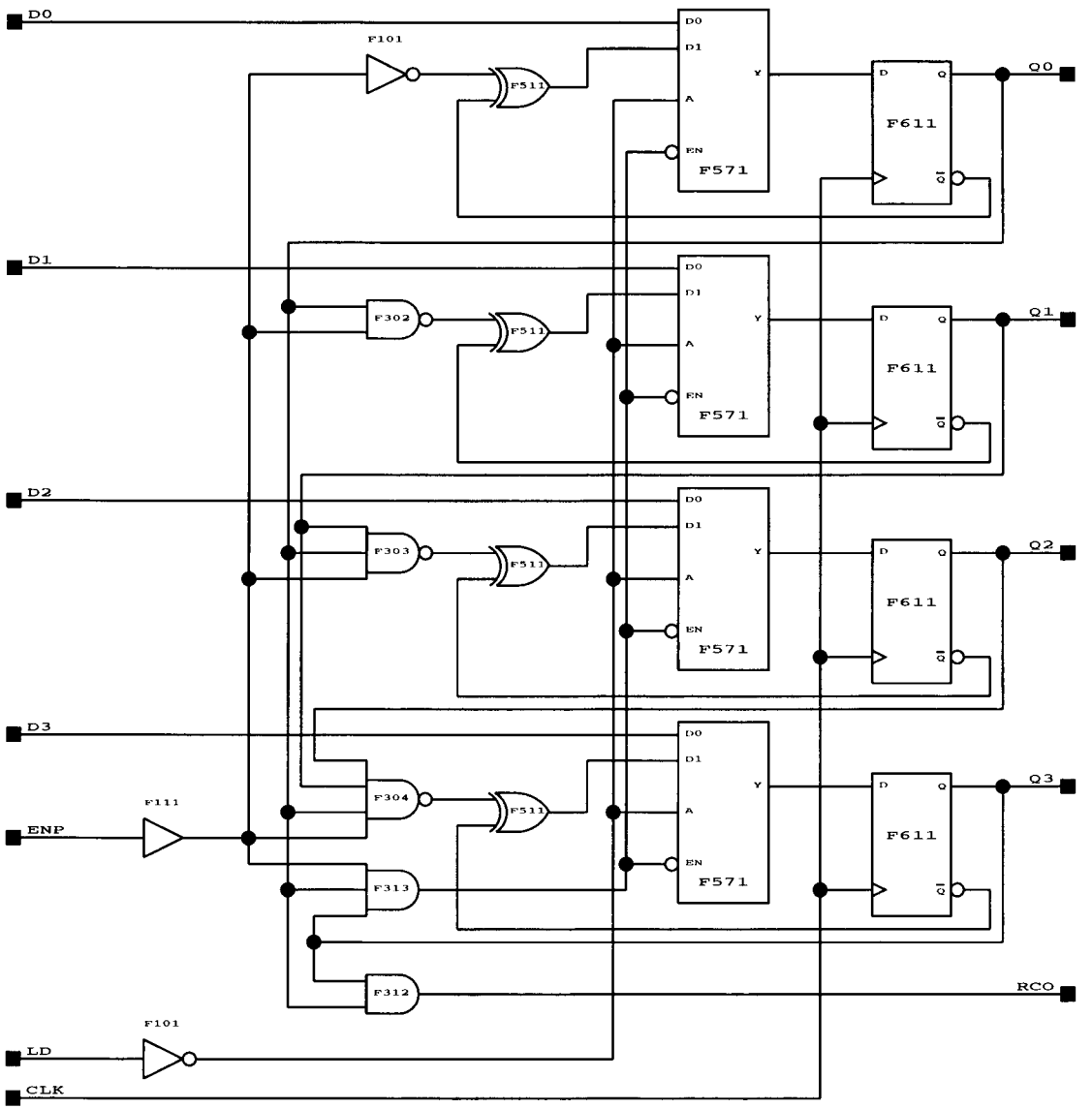
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 BMUX Multiplexer	
Issue 1			
Issue 2			
Issue 3		File: bmux.1	Page: 1 of 1



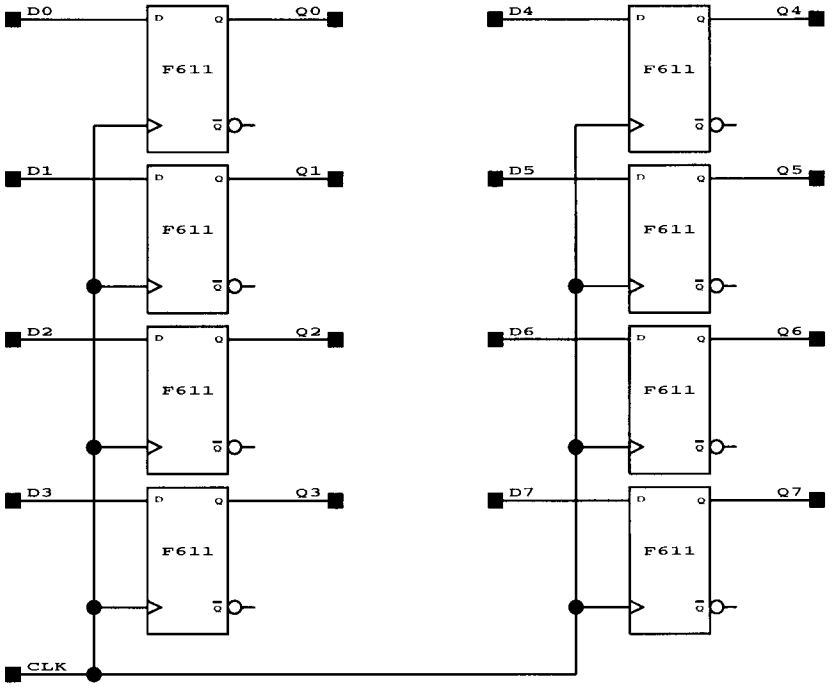
dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 CMUX	
Issue 1			
Issue 2			
Issue 3		File: cmux.1	Page: 1 of 1



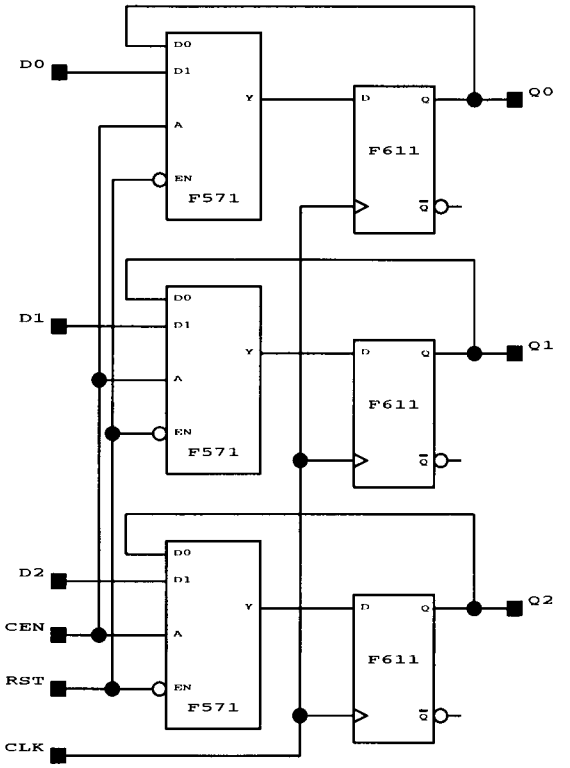
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		CNT10 Decimal Counter
Issue 2		
Issue 3		File: cnt10.1 | Page: 1 of 1



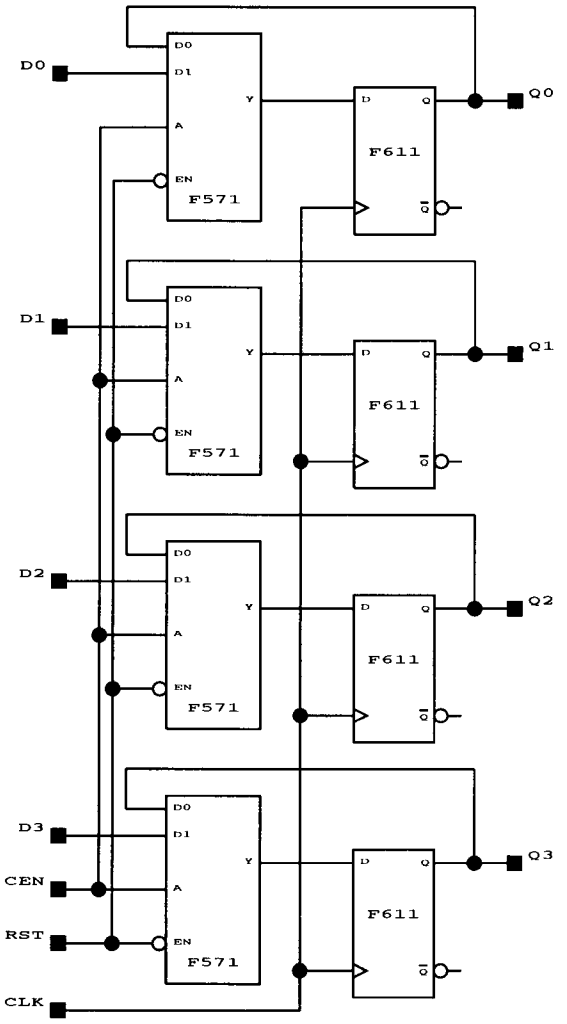
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 CNT10L Decimal Counter LSB	
Issue 1			
Issue 2			
Issue 3		File: cnt101.1	Page: 1 of 1



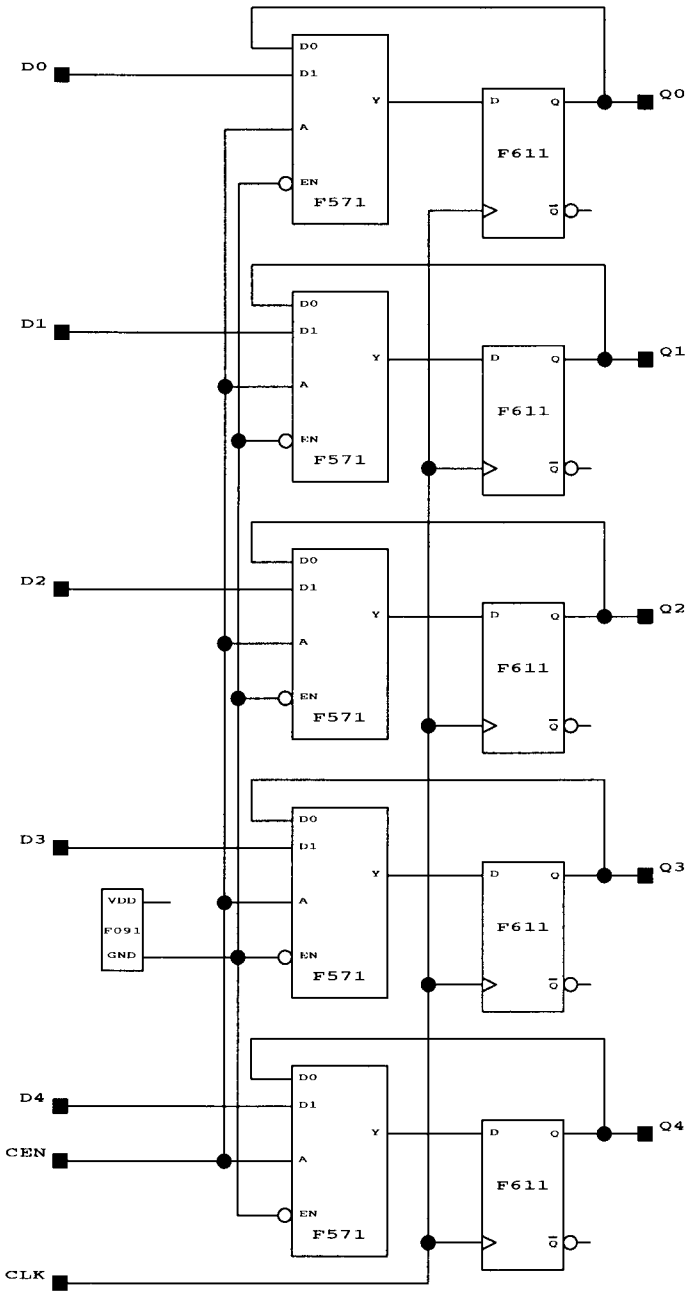
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 8-Bit D-F/F	
Issue 1			
Issue 2			
Issue 3		File: dff8b.1	Page: 1 of 1



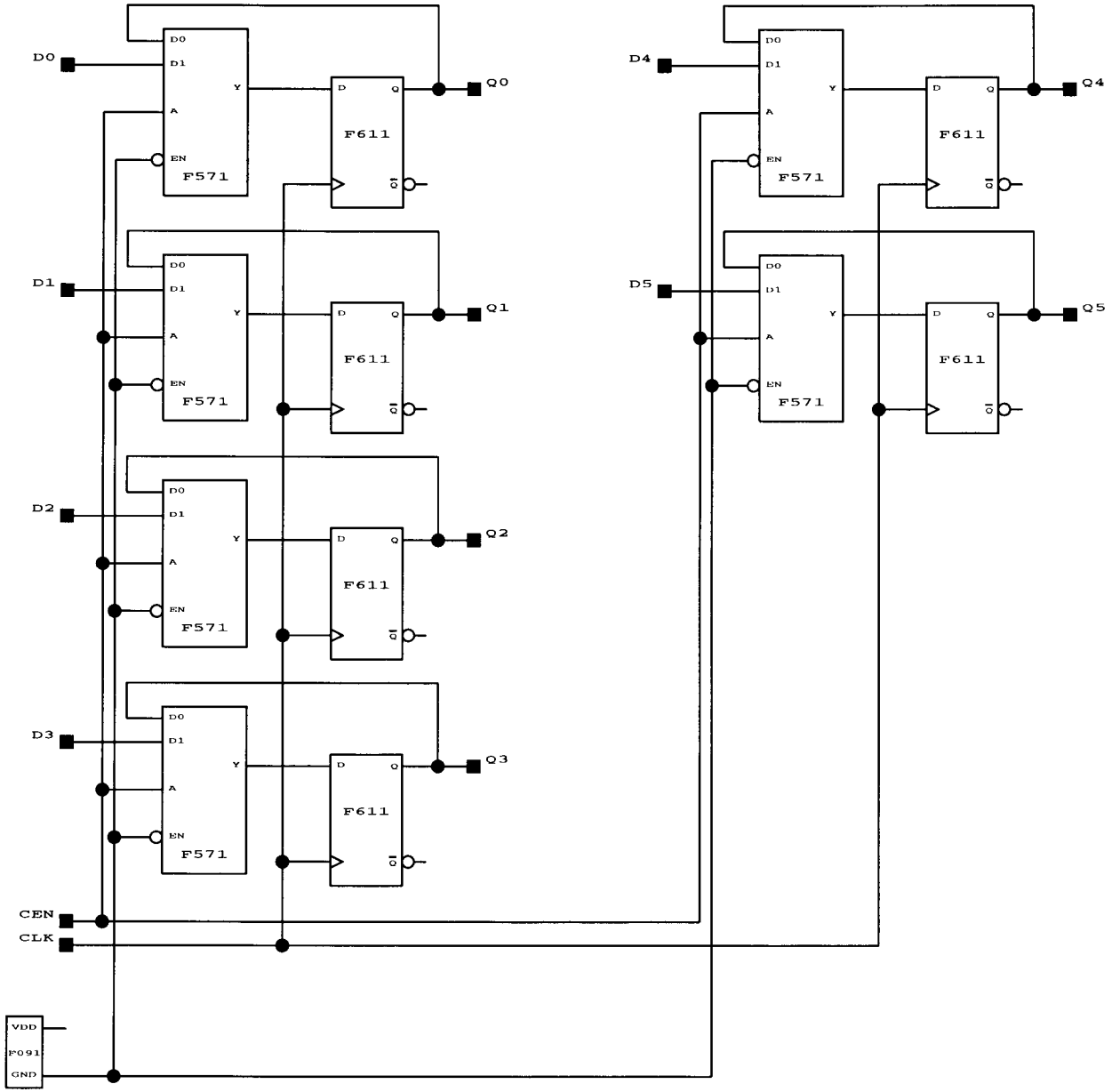
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 3-Bit D-Register	
Issue 1			
Issue 2			
Issue 3		File: dreg3b.1	Page: 1 of 1



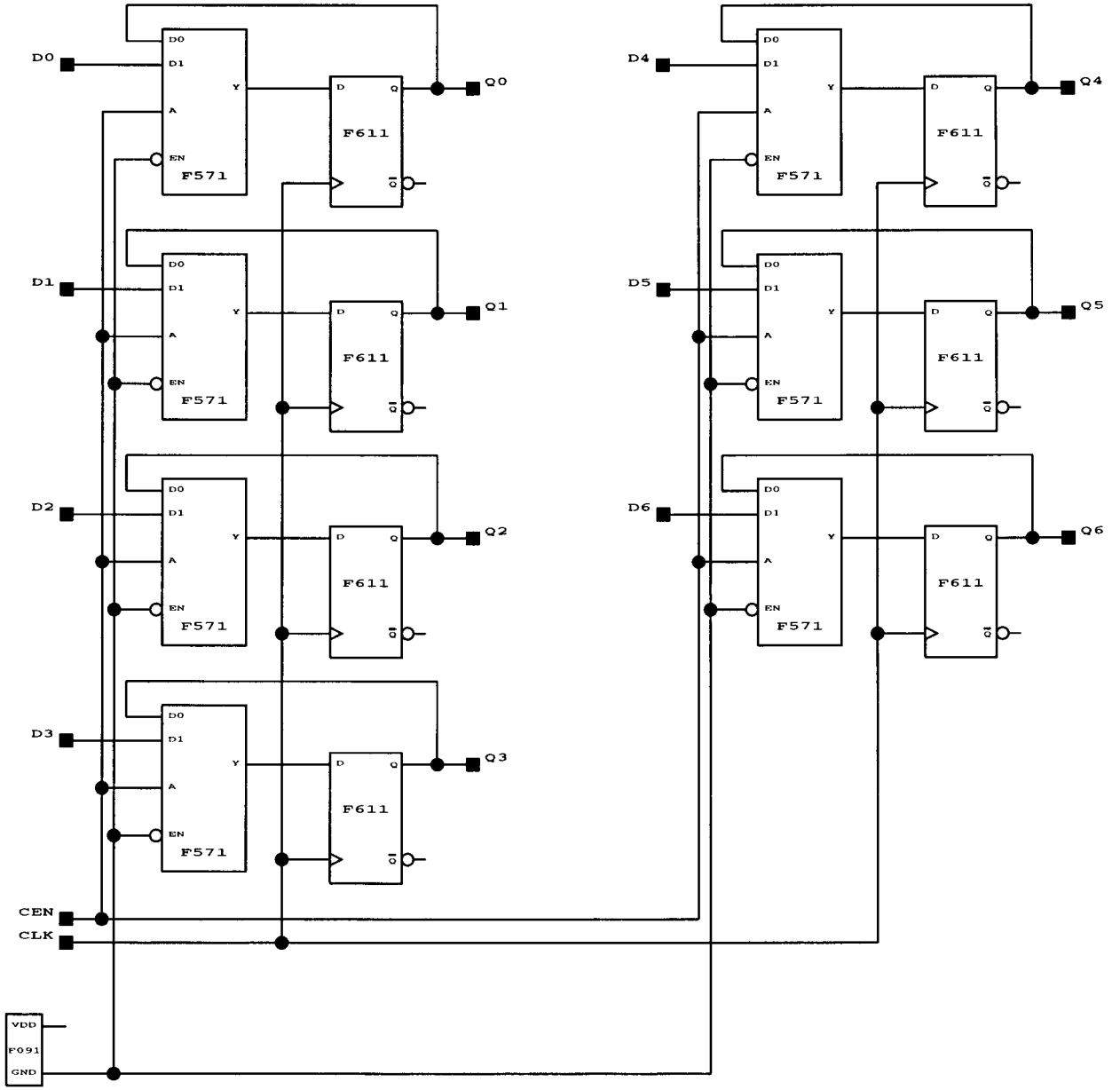
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 4-Bit D-Register
Issue 1		
Issue 2		
Issue 3		File: dreg4b.1 | Page: 1 of 1



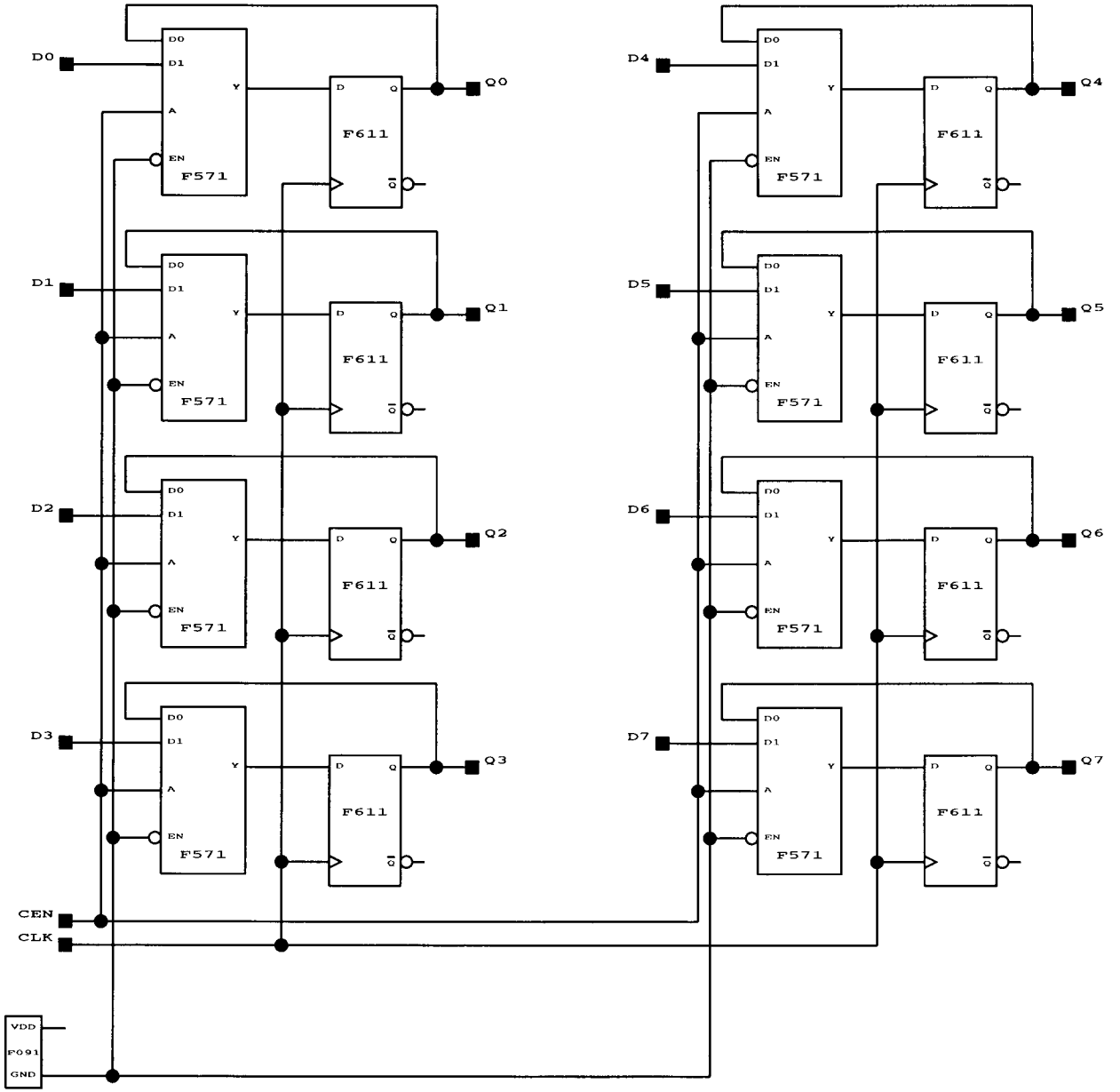
dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		DREG5B 5-Bit D-register
Issue 2		
Issue 3		File: dreg5b.1 — Page: 1 of 1



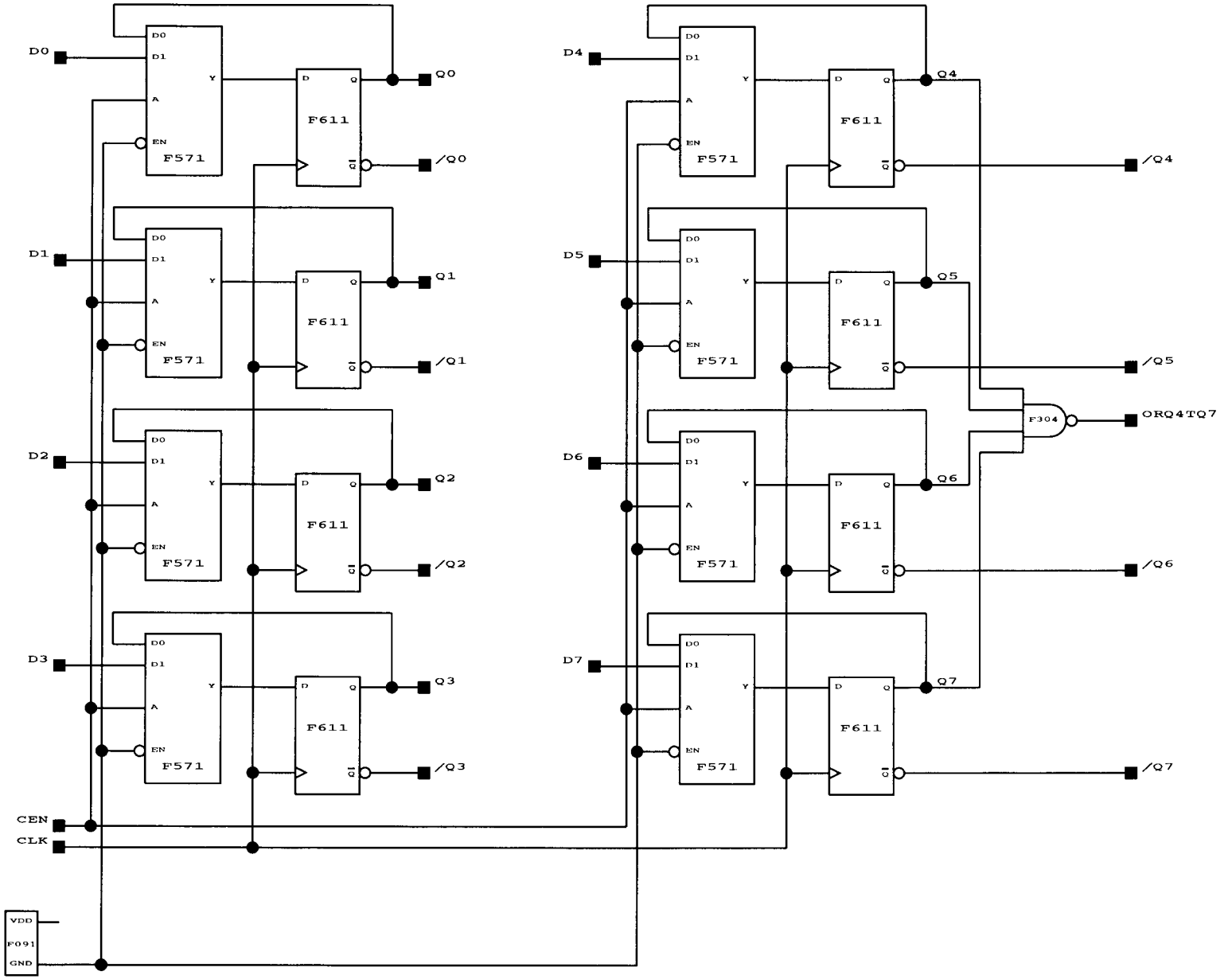
Dansk Data Elektronik A/S			
Issue 0	94-05-29	CPU AGENT - CA302	
Issue 1		DREG6B 6-Bit D-register	
Issue 2			
Issue 3		File: dreg6b.1	Page: 1 of 1



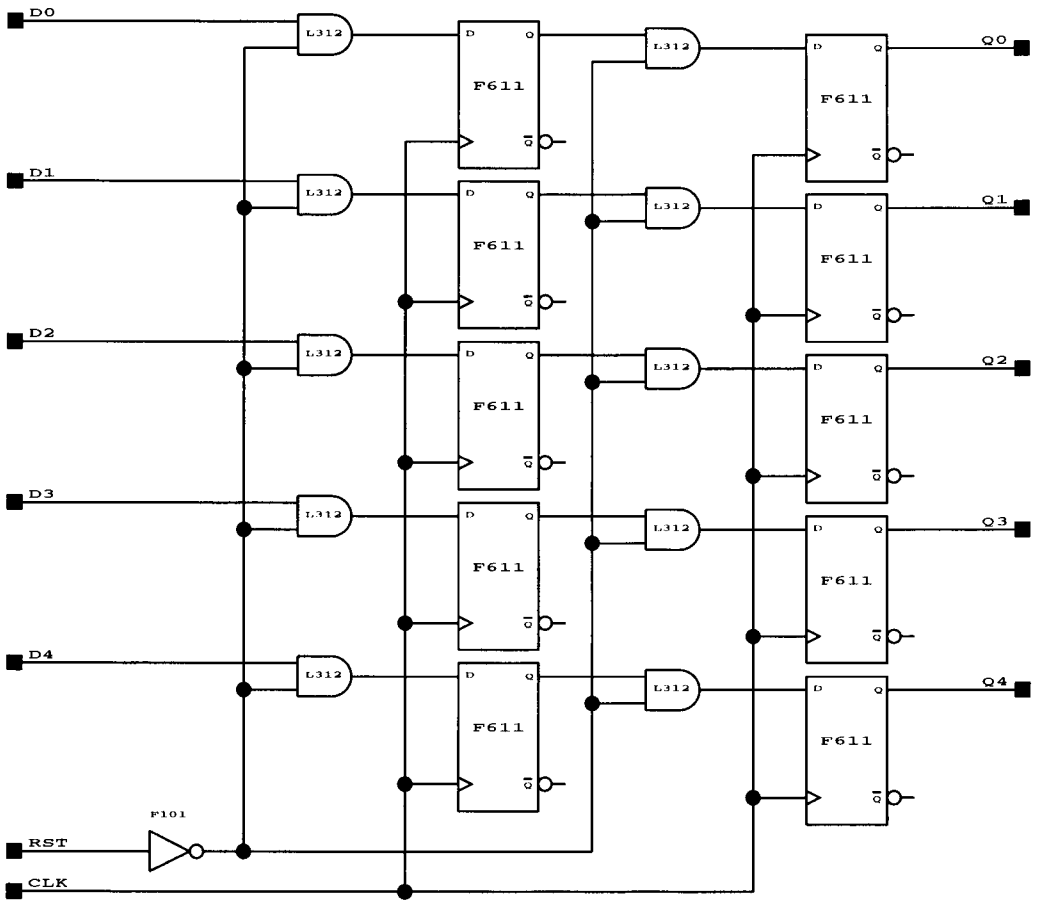
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CPA DREG7B 7-Bit D-Register	
Issue 1			
Issue 2			
Issue 3		File: dreg7b.1	Page:1 of 1



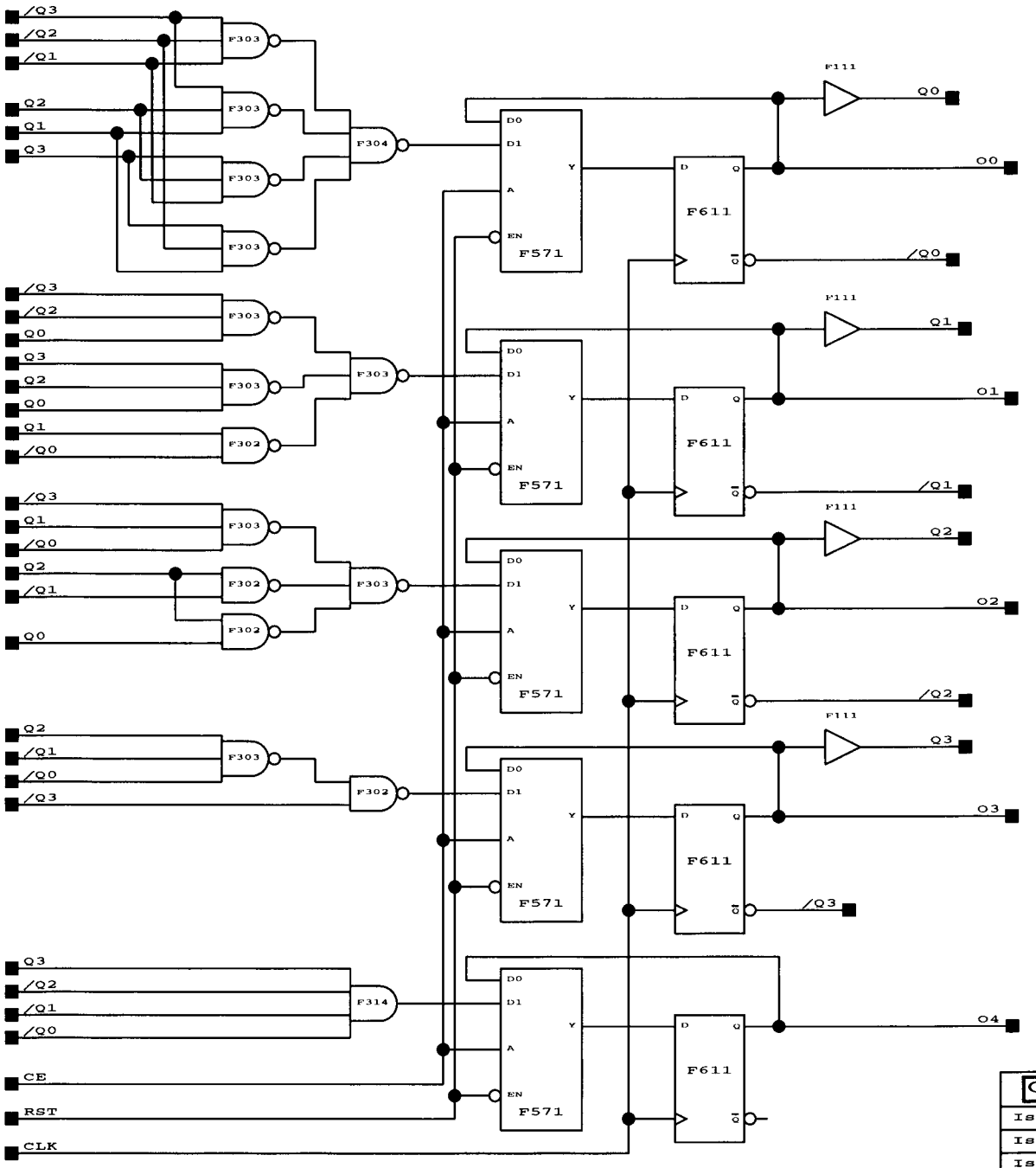
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		DREG8B 8-Bit D-register
Issue 2		
Issue 3		File: dreg8b.1 Page: 1 of 1



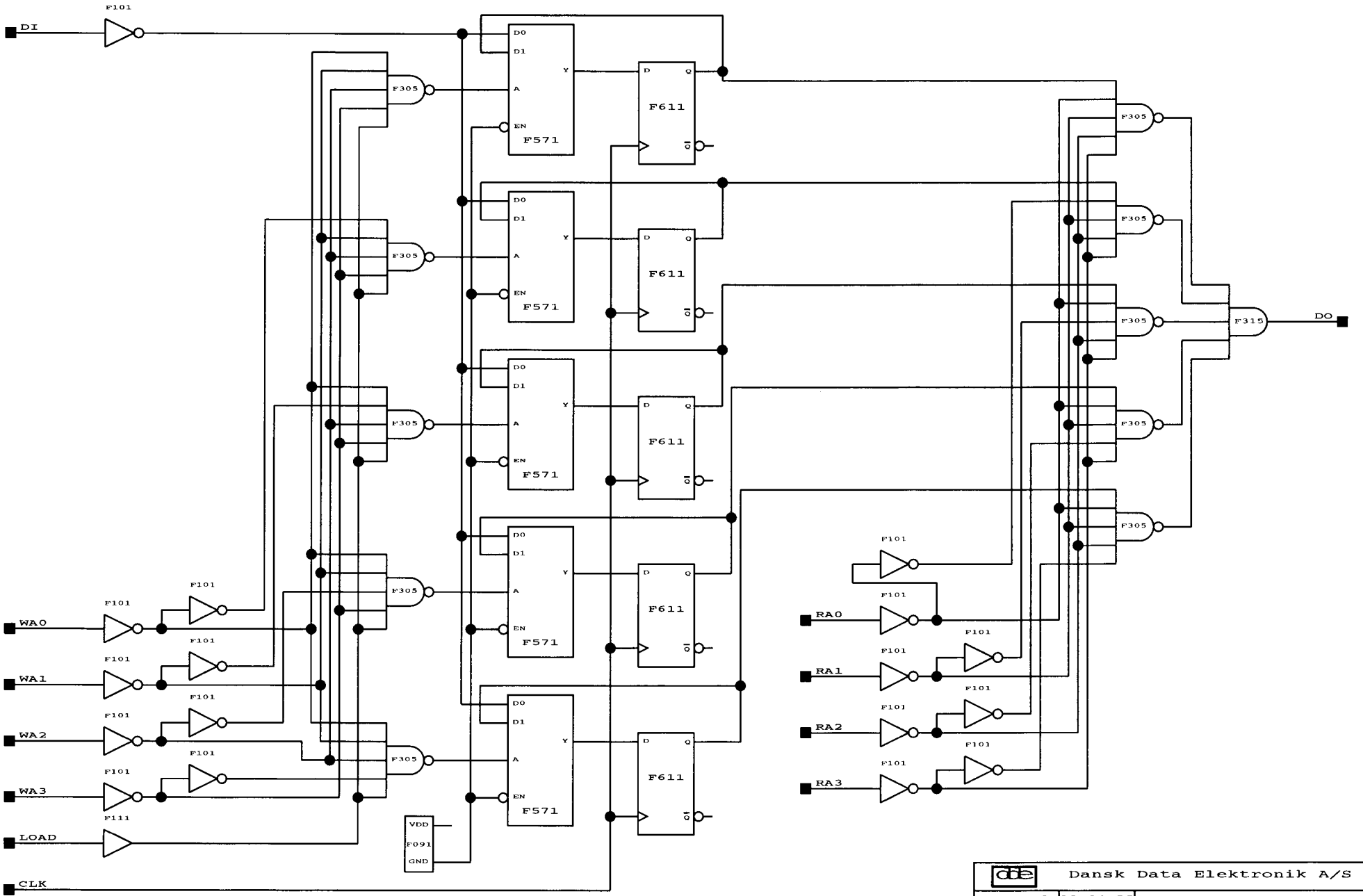
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 8-Bit Invert. D-register
Issue 1		
Issue 2		
Issue 3		File: dreg8bi.1 | Page: 1 of 1



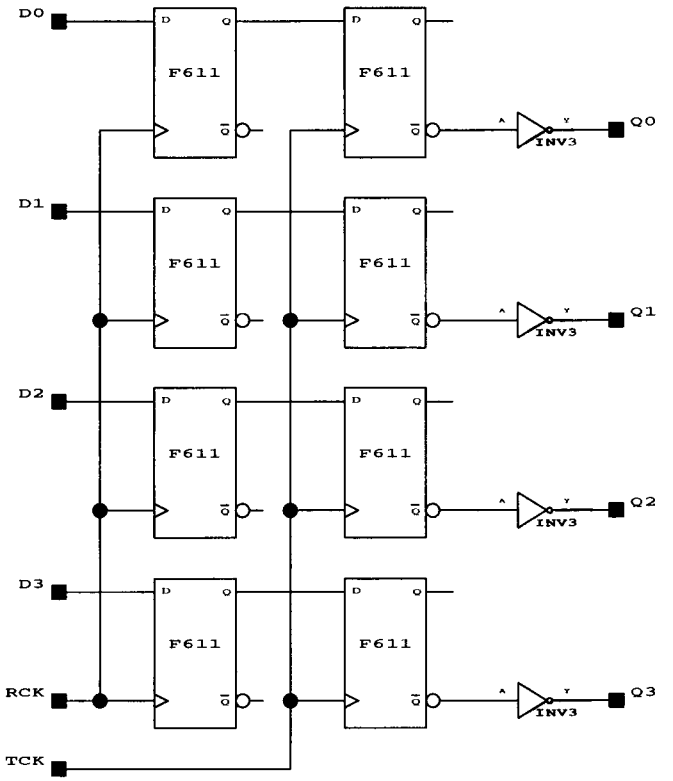
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 DSREG5B Double Sync. Reg.
Issue 1		
Issue 2		
Issue 3		File: dsreg5b.1 | Page: 1 of 1



Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		GRAYCNT Gray-Code Counter
Issue 2		
Issue 3		File: graycnt.1 Page: 1 of 1



Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		LDEREG LDE Register
Issue 2		
Issue 3		File: ldereg.1 Page: 1 of 1



dde	Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-09-18	Sampling & Staging Registers
Issue 2		
Issue 3		File: pinreg.1 | Page:1 of 1

Data Sheet for Block dprwbuf

Generator : generate_1.4_11Jan94
Date/Time : 19 Jul 9:51:20 1994

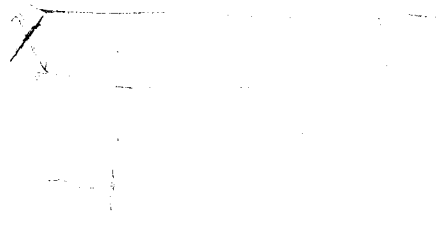
Port A		
	Configuration	: readOnly
	Words	: 32
	Bits per word	: 64
Port B		
	Configuration	: writeOnly
	Words	: 32
	Bits per word	: 64
Aspect Ratio		
	Rows	: 16
	Columns	: 128
Bist		: yes

Technology : ecpd07
Dimensions : 2806.00 x 549.60 (um x um) (without BIST)
Area : 1.54 sq. mm

powerA AC power, portA, VDD=5.0V, unloaded	3.10	mW/MHz
powerB AC power, portB, VDD=5.0V, unloaded	3.31	mW/MHz

ES2 DPRAM GENERATOR Generator : generate_1.4_11Jan94
Block : dprwbuf Date/Time : 19 Jul 9:51:20 1994

Parameter	Description	Min	Typ	Max	Mil	
Port A : Read-Port						
mdlhA	Load dependant rise time	0.24	0.56	1.14	1.34	ns/pF
mdhlA	Load dependant fall time	0.19	0.44	0.90	1.06	ns/pF
taccA	Access time	1.80	4.23	8.61	10.15	ns
tcycA	Cycle time	3.32	7.81	15.89	18.72	ns
tadsA	Address setup time	0.51	1.20	2.44	2.87	ns
tadhA	Address hold time	0.45	1.06	2.15	2.54	ns
tMEhA	MEA pulse width at high	0.49	1.16	2.37	2.79	ns
tMElA	MEA pulse width at low	0.51	1.20	2.44	2.87	ns
twdsA	data setup time	-	-	-	-	ns
twdhA	data hold time	-	-	-	-	ns
tpreA	min precharge (after Write)	-	-	-	-	ns
trdsA	WE_A read pulse setup time	-	-	-	-	ns
trdhA	WE_A read pulse hold time	-	-	-	-	ns
tmpwA	min write (Write Cycle)	-	-	-	-	ns
twpwA	min write (Read Modif Write)	-	-	-	-	ns
twrsA	write setup time	-	-	-	-	ns
Port B :						



Write - Port

mdlhB	Load dependant rise time	-	-	-	-	ns/pF
mdhlB	Load dependant fall time	-	-	-	-	ns/pF
taccB	Access time	-	-	-	-	ns
tcycB	Cycle time	2.23	5.24	10.67	12.57	ns
tadsB	Address setup time	0.51	1.20	2.44	2.87	ns
tadhB	Address hold time	0.45	1.06	2.15	2.54	ns
twdsB	data setup time	0.54	1.28	2.60	3.06	ns
twdhB	data hold time	0.61	1.44	2.93	3.45	ns
tMEhB	MEB pulse width at high	-	-	-	-	ns
tMElB	MEB pulse width at low	-	-	-	-	ns
tpreB	min precharge (after Write)	0.82	1.94	3.95	4.66	ns
trdsB	WE_B read pulse setup time	-	-	-	-	ns
trdhB	WE_B read pulse hold time	-	-	-	-	ns
tmpwB	min write (Write Cycle)	1.05	2.48	5.05	5.96	ns
twpwB	min write (Read Modif Write)	-	-	-	-	ns
twrsB	write setup time	-	-	-	-	ns
	Contentions :					
tmcs	ME (write port) setup time	0.75	1.77	3.60	4.24	ns
tmch	ME (write port) hold time	0.80	1.89	3.84	4.53	ns
twcs	WE_ (write port) setup time	-	-	-	-	ns
twch	WE_ (write port) hold time	-	-	-	-	ns
tdcs	data (write port) setup time	0.12	0.27	0.55	0.65	ns
tdch	data (write port) hold time	1.20	2.83	5.76	6.79	ns
	BIST or FIFO related :					
mclh	Addr. counter load dep. rise	0.40	0.95	1.93	2.28	ns/pF
mchl	Addr. counter load dep. fall	0.31	0.72	1.47	1.73	ns/pF
tctr	Addr. counter output time	0.91	2.14	4.35	5.13	ns
tcsu	Addr. counter setup time	1.00	2.35	4.78	5.64	ns
tmlh	ME hold time to CLRZ end	0.88	2.08	4.23	4.99	ns
trecA	CLRZ minimum low time	1.50	3.53	7.18	8.46	ns
trecB	CLRZ minimum low time	1.50	3.53	7.18	8.46	ns

Data Sheet for Block dprread
Used as core cell in Block fiforead_bst

Generator : generate_1.4_11Jan94
Date/Time : 19 Jul 10: 7:32 1994

Port A
Configuration : readOnly
Words : 16
Bits per word : 64

Port B
Configuration : writeOnly
Words : 16
Bits per word : 64

Aspect Ratio
Rows : 8
Columns : 128

Bist : yes

Technology : ecpd07
Dimensions : 2793.20 x 402.40 (um x um) (without BIST)
Area : 1.12 sq. mm

pconA	Power consumption, port A, typ case	2.54	mW/MHz
pconB	Power consumption, port B, typ case	2.75	mW/MHz

ES2 FIFO GENERATOR Generator : generate_1.4_11Jan94
Block : dprread Date/Time : 19 Jul 10: 7:32 1994

Parameter	Description	Min	Typ	Max	Mil
Port A :					
mdlhA	Load dependant rise time	0.24	0.56	1.14	1.34 ns/pF
mdhlA	Load dependant fall time	0.19	0.44	0.90	1.06 ns/pF
taccA	Access time	1.76	4.13	8.41	9.91 ns
tcycA	Cycle time	3.27	7.69	15.65	18.45 ns
tadsA	Address setup time	0.51	1.20	2.45	2.88 ns
tadhA	Address hold time	0.44	1.04	2.12	2.50 ns
tMEhA	MEA pulse width at high	0.48	1.13	2.30	2.71 ns
tMElA	MEA pulse width at low	0.51	1.20	2.44	2.87 ns
Port B :					
tcycB	Cycle time	2.00	4.70	9.57	11.27 ns
tadsB	Address setup time	0.51	1.20	2.45	2.88 ns
tadhB	Address hold time	0.44	1.04	2.12	2.50 ns
twdsB	data setup time	0.47	1.11	2.26	2.67 ns
twdhB	data hold time	0.61	1.43	2.91	3.43 ns
tpreB	min precharge (after Write)	0.69	1.62	3.30	3.89 ns
tmpwB	min write (Write Cycle)	1.00	2.36	4.81	5.66 ns

Contentions :

tmcs	ME (write port) setup time	0.73	1.73	3.52	4.15 ns
tmch	ME (write port) hold time	0.77	1.82	3.71	4.37 ns
tdcs	data (write port) setup time	0.12	0.27	0.55	0.65 ns
tdch	data (write port) hold time	1.17	2.76	5.61	6.61 ns

FIFO related :

mclh	Addr. counter load dep. rise /pF	0.40	0.95	1.93	2.28 ns
mchl	Addr. counter load dep. fall /pF	0.31	0.72	1.47	1.73 ns
tctr	Addr. counter output time	0.90	2.11	4.29	5.06 ns
tcsu	Addr. counter setup time	1.00	2.35	4.78	5.64 ns
tmlh	ME hold time to CLRZ end	0.88	2.08	4.23	4.99 ns
trecA	CLRZ minimum low time	1.27	2.98	6.07	7.15 ns
trecB	CLRZ minimum low time	1.27	2.98	6.07	7.15 ns

AAJ / 94-10-05

CA302 POST-LAYOUT DELAYS

RCLK to BRCLK1 : ↑ 3.2 ns, ↓ 3.6 ns

to BRCLK2 : ↑ 3.3 ns, ↓ 3.7 ns

TCLK to BTCLK : ↑ 3.0 ns, ↓ 3.6 ns

TCLK to VALO : ↑ 7.3 ns, ↓ 7.3 ns

TCLK to P000 :
Z→H = 10.1 ns
H→L = 8.2 ns
L→Z = 9.1 ns

P010 :
Z→L = 9.8 ns
L→H = 8.0 –, H→L = 8.2 ns
L→Z = 9.1 –

P150 :
Z→L = 9.8 ns
L→H = 8.6 –
H→Z = 9.7 –

P310 :
Z→L = 9.8 ns
L→H = 8.0 –
H→L = 8.2 –
L→Z = 9.1 –

P470 :
Z→L = 9.8 ns
L→H = 8.9 –
H→L = 8.9 –
L→Z = 9.1 –

P630 :
Z→L = 9.8 ns
L→H = 8.2 –
H→Z = 9.7 –

B000 to BAD10 : ↑ 0.6 ns, ↓ 1.2 ns

AAJ / 94-10-05
CA302 POST LAYOUT DELAYS

RBCK to BRBCLK 1 : ↑ 3.5 ns, ↓ 3.8 ns

to BRBCLK2 : ↑ 3.0 ns, ↓ 3.4 ns

TBCK to BTBCLK : ↑ 2.9 ns, ↓ 3.6 ns

TBCK to AVAO : Z→H = 9.3 ns
H→L = 8.5 –
L→Z = 8.5 –

DVAO : Z→L = 9.0 ns
L→H = 8.5 –
H→L =
H→Z = 8.5 –

B000 : Z→H = 9.3 ns
H→L = 8.0 –
Z→L = 8.7 –
L→H = 7.9 –, L→Z = 8.0 ns

B010 : Z→L = 8.7 ns
L→H = 7.8 –
H→L = 8.0 –
L→Z = 8.0 –
Z→H = 9.0 –

B150 : Z→L = 8.7 ns
L→H = 7.8 –
H→Z = 8.0 –

B630 : Z→L = 8.7 ns
L→H = 8.5 –
H→L = 8.5 –
L→Z = 7.9 –

P000 to SADI0 : ↑ 0.6 ns, ↓ 1.3 ns

CA302 DELAYS - MAX. - 25 NS SIM

RCLK to BRCLK1 :	↑ 1.8 ns ,	↓ 2.5 ns	(1.2/1.6)
to BRCLK2 :	↑ 1.7 ns ,	↓ 2.4 ns	(1.2/1.5)
TCLK to BTCLK :	↑ 2.8 ns ,	↓ 3.5 ns	(1.5/1.7)
P000 to SADI0 :	↑ 0.4 ns ,	↓ 1.1 ns	

WRITE / INTV BUFFER - WRITE

BRCLK2 to WRTME :	↑ 1.2 ns ,	↓ 1.5 ns	
BTCLK to WA0 :	↑ 2.7 ns ,	↓ 2.6 ns	
BTCLK to DI0 (RAM) :	↑ 2.7 ns ,	↓ 2.6 ns	
RAM addr set-up :	↑ 4.3 ns ,	↓ 4.4 ns	(2.44 ns)
RAM addr hold :	↑ 20.7 ns	↓ 20.6 ns	(2.15 ns)
RAM data set-up :		↓ 16.5 ns	(2.6 ns)
RAM data hold :		↓ 8.5 ns	(2.93 ns)

SYSTEM BUS CLOCKS

RBCLK to BRBCLK1 :	↑ 1.8 ns ,	↓ 2.5 ns	(1.3 / 1.5)
BRBCLK2 :	↑ 1.8 ns ,	↓ 2.4 ns	(1.2 / 1.4)
TBCK to BTBCLK :	↑ 2.7 ns ,	↓ 3.3 ns	(1.5 / 1.8)

WRITE / INTV BUFFER - READ

BRBCLK2 to README :	↑ 1.2 ns ,	↓ 1.3 ns	
BTBCLK to RA0 :	↑ 2.1 ns ,	↓ 2.1 ns	
RAM addr set-up :	↑ 5.0 ns ,	↓ 5.0 ns	(2.44 ns)
RAM addr hold :	↑ 20.0 ns ,	↓ 20.0 ns	(2.15 ns)
README to DO0 :	↑ 8.7 ns ,	↓ 8.7 ns	(8.61 ns)

SYSTEM BUS

BTBCLK to N_BPTEN1 :	↓ 3.9 ns ,	↑ 3.8 ns	
BTBCLK to (BPTEN1) :	↑ 3.2 ns ,	↓ 3.0 ns	
BTBCLK to B00 0 :	↑ 6.1 ns (EN) ,	↓ 5.0 ns	
TBCK to AVA0 :	↑ 8.5 ns ,	↓ 7.7 ns ,	↑ 7.4 ns
DVA0 :	↓ 8.2 ns ,	↑ 7.5 ns ,	↓ 7.4 ns

AAJ / 94-08-08
CA302 DELAYS - MAX SIM

READ RESPONSE BUFFER - WRITE

BRBCLK2 to WRTME :	↑ 1.2 ns	;	↓ 1.5 ns	
BTBCLK to WA0 :	↑ 2.6 ns	;	↓ 2.5 ns	
BTBCLK to DI0 (RAM) :	↑ 2.6 ns	;	↓ 2.5 ns	
RAM addr set-up :	↑ 4.5 ns	;	↓ 4.6 ns	
RAM addr hold :	↑ 20.5 ns	;	↓ 20.4 ns	
RAM data set-up :	↑ 16.7 ns	;	↓ 16.8 ns	
RAM data hold :			↓ 8.2 ns	

READ RESPONSE BUFFER - READ

BRCLK2 to READ ME :	↑ 1.1 ns	;	↓ 1.4 ns	
BTCLK to RA0 :	↑ 2.6 ns	;	↓ 2.5 ns	
RAM addr. set-up :	↑ 4.4 ns	;	↓ 4.4 ns	
RAM addr hold :	↑ 20.5 ns	;	↓ 20.6 ns	
READ ME to DO0 :	↑ 8.5 ns	;	↓ 8.5 ns	
BTCLK to (HPTEN1) :	↑ 2.2 ns	;	↓ 2.1 ns	
BTCLK to N-HPTEN1 :	↓ 4.8 ns	;	↑ 4.9 ns	
BTCLK to P0O0 :	↑ 7.0 ns (E)	;	↓ 4.9 ns ,	↑ 6.1 ns (D)

DESIGN NOTE

Name:	CA302 Pin Assignment
Date:	94-08-02
Author:	aaj
Version:	4.0
Document:	design note 6

Contents **page**

1 CA302 PIN ASSIGNMENTS

PIN	SIGNAL	BUFFER	LOAD pF
1	BC60	IOS1G	80
2	BC50	IOS1G	80
3	BC40	IOS1G	80
4	BC30	IOS1G	80
5	VDD	PWRPY	
6	BC20	IOS1G	80
7	BC10	IOS1G	80
8	BC00	IOS1G	80
9	BP70	IOS1G	80
10	B630	IOS1G	80
11	B620	IOS1G	80
12	B610	IOS1G	80
13	B600	IOS1G	80
14	B590	IOS1G	80
15	B580	IOS1G	80
16	GND	GNDPY	
17	B570	IOS1G	80
18	B560	IOS1G	80
19	BP60	IOS1G	80
20	B550	IOS1G	80
21	B540	IOS1G	80
22	B530	IOS1G	80
23	B520	IOS1G	80
24	B510	IOS1G	80
25	B500	IOS1G	80
26	B490	IOS1G	80
27	VDD	PWRPY	
28	B480	IOS1G	80
29	BP50	IOS1G	80
30	GND	GNDCO	
31	VDD	PWRCO	
32	B470	IOS1G	80
33	B460	IOS1G	80
34	B450	IOS1G	80
35	B440	IOS1G	80
36	B430	IOS1G	80
37	B420	IOS1G	80
38	B410	IOS1G	80
39	B400	IOS1G	80
40	GND	GNDPY	
41	BP40	IOS1G	80
42	B390	IOS1G	80
43	B380	IOS1G	80
44	B370	IOS1G	80
45	B360	IOS1G	80
46	B350	IOS1G	80
47	B340	IOS1G	80
48	B330	IOS1G	80
49	B320	IOS1G	80
50	BP30	IOS1G	80
51	VDD	PWRPY	
52	B310	IOS1G	80
53	B300	IOS1G	80
54	B290	IOS1G	80
55	B280	IOS1G	80
56	B270	IOS1G	80
57	B260	IOS1G	80
58	B250	IOS1G	80
59	B240	IOS1G	80
60	BP20	IOS1G	80

PIN	SIGNAL	BUFFER	LOAD pF
61	B23O	IOS1G	80
62	GND	GNDPY	
63	B22O	IOS1G	80
64	B21O	IOS1G	80
65	B20O	IOS1G	80
66	B19O	IOS1G	80
67	B18O	IOS1G	80
68	B17O	IOS1G	80
69	B16O	IOS1G	80
70	BP1O	IOS1G	80
71	B15O	IOS1G	80
72	B14O	IOS1G	80
73	VDD	PWRPY	
74	B13O	IOS1G	80
75	B12O	IOS1G	80
76	B11O	IOS1G	80
77	B10O	IOS1G	80
78	B09O	IOS1G	80
79	B08O	IOS1G	80
80	BP0O	IOS1G	80
81	B07O	IOS1G	80
82	B06O	IOS1G	80
83	B05O	IOS1G	80
84	GND	GNDPY	
85	B04O	IOS1G	80
86	B03O	IOS1G	80
87	B02O	IOS1G	80
88	B01O	IOS1G	80
89	B00O	IOS1G	80
90	GND	GNDCO	
91	VDD	PWRCO	
92	P00O	IOS1G	50
93	P01O	IOS1G	50
94	P02O	IOS1G	50
95	P03O	IOS1G	50
96	P04O	IOS1G	50
97	VDD	PWRPY	
98	P05O	IOS1G	50
99	P06O	IOS1G	50
100	P07O	IOS1G	50
101	PP0O	IOS1G	50
102	P08O	IOS1G	50
103	P09O	IOS1G	50
104	P10O	IOS1G	50
105	P11O	IOS1G	50
106	P12O	IOS1G	50
107	P13O	IOS1G	50
108	GND	GNDPY	
109	P14O	IOS1G	50
110	P15O	IOS1G	50
111	PP1O	IOS1G	50
112	P16O	IOS1G	50
113	P17O	IOS1G	50
114	P18O	IOS1G	50
115	P19O	IOS1G	50
116	P20O	IOS1G	50
117	P21O	IOS1G	50
118	P22O	IOS1G	50
119	VDD	PWRPY	
120	P23O	IOS1G	50

PIN	SIGNAL	BUFFER	LOAD pF
121	PP20	IOS1G	50
122	P240	IOS1G	50
123	P250	IOS1G	50
124	P260	IOS1G	50
125	P270	IOS1G	50
126	P280	IOS1G	50
127	P290	IOS1G	50
128	P300	IOS1G	50
129	P310	IOS1G	50
130	GND	GNDPY	
131	PP30	IOS1G	50
132	P320	IOS1G	50
133	P330	IOS1G	50
134	P340	IOS1G	50
135	P350	IOS1G	50
136	P360	IOS1G	50
137	P370	IOS1G	50
138	P380	IOS1G	50
139	P390	IOS1G	50
140	PP40	IOS1G	50
141	VDD	PWRPY	
142	P400	IOS1G	50
143	P410	IOS1G	50
144	P420	IOS1G	50
145	P430	IOS1G	50
146	P440	IOS1G	50
147	P450	IOS1G	50
148	P460	IOS1G	50
149	P470	IOS1G	50
150	GND	GNDCO	
151	VDD	PWRCO	
152	PP50	IOS1G	50
153	P480	IOS1G	50
154	GND	GNDPY	
155	P490	IOS1G	50
156	P500	IOS1G	50
157	P510	IOS1G	50
158	P520	IOS1G	50
159	P530	IOS1G	50
160	P540	IOS1G	50
161	P550	IOS1G	50
162	PP60	IOS1G	50
163	P560	IOS1G	50
164	P570	IOS1G	50
165	VDD	PWRPY	
166	P580	IOS1G	50
167	P590	IOS1G	50
168	P600	IOS1G	50
169	P610	IOS1G	50
170	P620	IOS1G	50
171	P630	IOS1G	50
172	PP70	IOS1G	50
173	PC00	IOS1G	50
174	PC10	IOS1G	50
175	PC20	IOS1G	50
176	GND	GNDPY	
177	PC30	IOS1G	50
178	PC40	IOS1G	50
179	PC50	IOS1G	50
180	PC60	IOS1G	50

PIN	SIGNAL	BUFFER	LOAD pF
181	PC7O	IOS1G	50
182	PC8O	IOS1G	50
183	PCPO	IOS1G	50
184	VALO	OPS1T	25
185	EXRQ	OPS1T	25
186	RRDY	OPS1T	25
187	VDD	PWRPY	
188	WRDY	OPS1T	25
189	IACK	OPS1T	25
190	IERR	OPS1T	25
191	SACK	OPS1T	25
192	ITRO	OPSOT	25
193	ITR1	OPSOT	25
194	LMPO	OPSOT	25
195	LMP1	OPSOT	25
196	GND	GNDPY	
197	VALI	IPS8I	
198	RELS	IPS8I	
199	INRQ	IPS8I	
200	SREQ	IPS8G	
201	TREF	IPS8G	
202	PCEN	IPS8G	
203	RCLK	IPS8G	
204	TCLK	IPS8G	
205	GND	CKBUF25	
206	VDD	CKBUF25	
207	IOMD	IPS8G	
208	SPS1	IPS8G	
209	SPSO	IPS8G	
210	GND	GNDCO	

PIN	SIGNAL	BUFFER	LOAD pF
211	VDD	PWRCO	
212	POS3	IPS8G	
213	POS2	IPS8G	
214	POS1	IPS8G	
215	POSO	IPS8G	
216	LCAL	IPS8G	
217	RBCK	IPS8G	
218	TBCK	IPS8G	
219	GND	CKBUF25	
220	VDD	CKBUF25	
221	SHIT	IPS8G	
222	RSET	IPS8G	
223	TAKI	IPS8G	
224	ITVI	IPS8G	
225	SHRI	IPS8G	
226	BSYI	IPS8G	
227	BAGR	IPS8G	
228	BARQ	OPS1T	25
229	BOOT	OPS1T	25
230	BPER	OPS1T	25
231	ITVO	OPS1T	25
232	GND	GNDPY	
233	SHRO	OPS1T	25
234	BSYO	OPS1T	25
235	DVAI	IPS8G	
236	DVAO	OPS1V	80
237	AVAI	IPS8G	
238	AVAO	OPS1V	80
239	BCPO	IOS1G	80
240	BC7O	IOS1G	80

2 GND and VDD CALCULATIONS

Input buffer pads:	IPS8G:	24
	IPS8T:	3
Output buffer pads:	OPS0T:	4
	OPS1T:	13
	OPS1V:	2
Bidirectional buffer pads:	IOS1G:	163
Core power pads:	PWRCO:	4
	GNDCO:	4
I/O power pads:	PWRPY:	9
	GNDPY:	10
Clock buffer pads (CKBUF25):	VDD:	2
	GND:	2
Total no. of pads		240

Core Power:

Required no. of PWRCO/GNDCO pad pairs: 240/64= 3.75

I/O Power:

I/O current:	OPS0T:	4 x 2.75 =	11.0	mA
	OPS1T:	13 x 5.5 =	71.5	-
	OPS1V:	2 x 5.5 =	11.0	-
	IOS1G:	163 x 5.5 =	896.5	-
Total I/O current			990.0	mA

Required no. of PWRPY/GNDPY pairs: 990/110= 9

10R 2G 1344.8

1.438.25

10 13

```
PlacePad : BOTTOM , Pad : $5I529
PlacePad : BOTTOM , Pad : $5I530
PlacePad : BOTTOM , Pad : $5I531
PlacePad : BOTTOM , Pad : $5I532
PlacePad : BOTTOM , Pad : $1I96
PlacePad : BOTTOM , Pad : $2I381
PlacePad : BOTTOM , Pad : $2I378
PlacePad : BOTTOM , Pad : $2I384
PlacePad : BOTTOM , Pad : $5I576
PlacePad : BOTTOM , Pad : $5I567
PlacePad : BOTTOM , Pad : $2I445
PlacePad : BOTTOM , Pad : $2I441
PlacePad : BOTTOM , Pad : $2I442
PlacePad : BOTTOM , Pad : $2I355
PlacePad : BOTTOM , Pad : $5I572
PlacePad : BOTTOM , Pad : $9I625
PlacePad : BOTTOM , Pad : $9I624
PlacePad : BOTTOM , Pad : $1I107
PlacePad : BOTTOM , Pad : $1I105
PlacePad : BOTTOM , Pad : $9I629
PlacePad : BOTTOM , Pad : $9I628
PlacePad : BOTTOM , Pad : $9I627
PlacePad : BOTTOM , Pad : $9I626
PlacePad : BOTTOM , Pad : $9I630
PlacePad : BOTTOM , Pad : $6I421
PlacePad : BOTTOM , Pad : $6I423
PlacePad : BOTTOM , Pad : $6I353
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PlacePad : BOTTOM , Pad : $6I358
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PlacePad : RIGHT , Pad : $6I408
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PlacePad : RIGHT , Pad : $8I529
PlacePad : RIGHT , Pad : $9I592
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PlacePad : RIGHT , Pad : $7I530
PlacePad : RIGHT , Pad : $7I529
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PlacePad : TOP , Pad : $1I86
PlacePad : TOP , Pad : $7I519
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PlacePad : TOP , Pad : $7I483
PlacePad : TOP , Pad : $7I482
PlacePad : TOP , Pad : $7I481
PlacePad : TOP , Pad : $9I578
PlacePad : TOP , Pad : $7I472

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PlacePad : TOP , Pad : $7I471
PlacePad : TOP , Pad : $7I470
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PlacePad : TOP , Pad : $3I466
PlacePad : TOP , Pad : $1I89
PlacePad : TOP , Pad : $3I468
PlacePad : TOP , Pad : $3I470
PlacePad : TOP , Pad : $3I472
PlacePad : TOP , Pad : $5I543
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PlacePad : TOP , Pad : $3I476
PlacePad : TOP , Pad : $3I478
PlacePad : TOP , Pad : $3I480
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PlacePad : TOP , Pad : $3I486
PlacePad : TOP , Pad : $3I488
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PlacePad : TOP , Pad : $3I491
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PlacePad : TOP , Pad : $3I497
PlacePad : TOP , Pad : $3I499
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PlacePad : TOP , Pad : $1I90
PlacePad : TOP , Pad : $3I503
PlacePad : LEFT , Pad : $5I545
PlacePad : LEFT , Pad : $3I506
PlacePad : LEFT , Pad : $3I508
PlacePad : LEFT , Pad : $3I510
PlacePad : LEFT , Pad : $3I512
PlacePad : LEFT , Pad : $3I514
PlacePad : LEFT , Pad : $3I516
PlacePad : LEFT , Pad : $3I518
PlacePad : LEFT , Pad : $3I520
PlacePad : LEFT , Pad : $1I93
PlacePad : LEFT , Pad : $5I546
PlacePad : LEFT , Pad : $4I457
PlacePad : LEFT , Pad : $4I460
PlacePad : LEFT , Pad : $4I462
PlacePad : LEFT , Pad : $4I464
PlacePad : LEFT , Pad : $4I466
PlacePad : LEFT , Pad : $4I468
PlacePad : LEFT , Pad : $4I470
PlacePad : LEFT , Pad : $4I472
PlacePad : LEFT , Pad : $5I555
PlacePad : LEFT , Pad : $1I91
PlacePad : LEFT , Pad : $4I486
PlacePad : LEFT , Pad : $4I484
PlacePad : LEFT , Pad : $4I482
PlacePad : LEFT , Pad : $4I480
```

```
PlacePad : LEFT , Pad : $4I478
PlacePad : LEFT , Pad : $4I476
PlacePad : LEFT , Pad : $4I474
PlacePad : LEFT , Pad : $4I518
PlacePad : LEFT , Pad : $1I106
PlacePad : LEFT , Pad : $1I104
PlacePad : LEFT , Pad : $5I556
PlacePad : LEFT , Pad : $4I487
PlacePad : LEFT , Pad : $1I94
PlacePad : LEFT , Pad : $4I489
PlacePad : LEFT , Pad : $4I491
PlacePad : LEFT , Pad : $4I493
PlacePad : LEFT , Pad : $4I495
PlacePad : LEFT , Pad : $4I497
PlacePad : LEFT , Pad : $4I499
PlacePad : LEFT , Pad : $4I501
PlacePad : LEFT , Pad : $5I557
PlacePad : LEFT , Pad : $4I503
PlacePad : LEFT , Pad : $4I505
PlacePad : LEFT , Pad : $1I92
PlacePad : LEFT , Pad : $4I507
PlacePad : LEFT , Pad : $4I509
PlacePad : LEFT , Pad : $4I511
PlacePad : LEFT , Pad : $4I513
PlacePad : LEFT , Pad : $4I515
PlacePad : LEFT , Pad : $4I521
PlacePad : LEFT , Pad : $5I558
PlacePad : LEFT , Pad : $2I388
PlacePad : LEFT , Pad : $2I392
PlacePad : LEFT , Pad : $2I393
PlacePad : LEFT , Pad : $1I95
PlacePad : LEFT , Pad : $2I394
PlacePad : LEFT , Pad : $2I395
PlacePad : LEFT , Pad : $2I396
PlacePad : LEFT , Pad : $2I397
DieSize : 1212596 1212596
```

Total transistor equivalent ~~90195~~ 91506

No. of gates : 90195 / 4 = 22549 ~ 22550 gates
91506 / 4 = 22877 ~ 22880

WRITE / INTERVENTION BUFFER

Absolut worst-case er 10 MHz input (Port B) og 10 MHz output (port A), da A og B aldrig er aktive samtidig.

Port A:	3.10 mW/MHz	× 10 MHz =	31 mW
B:	3.31 – –	× 10 –	33.1 –
			64.1 mW

READ RESPONSE BUFFER

Middel data rate : 16/32 = 0.5

Port A:	2.54 mW/MHz	× 10 MHz	25.4 mW
Port B:	2.75 mW/MHz	× 10 MHz	27.5 –
			52.9 mW

INTR0 - INTR1

INTR0		0.6 mA
— 1		0.6 mA
LAMP0	(ALS 240)	0.1 —
— 1	(—)	0.1 —
BOOT	(MACH)	0
BSY0	(MACH + AS)	0.5
ITV0	(AS)	0.5
SHR0	(AS)	
BARQ	(PAL)	0.5
BPER	(AS)	0.5
EXRQ	(R4000)	0
VALO	(FAST)	0.1
RRDY	—	
WRDY	—	
IACK	—	
IERR	—	
SACK	(CA302)	0

17 3.5 mA

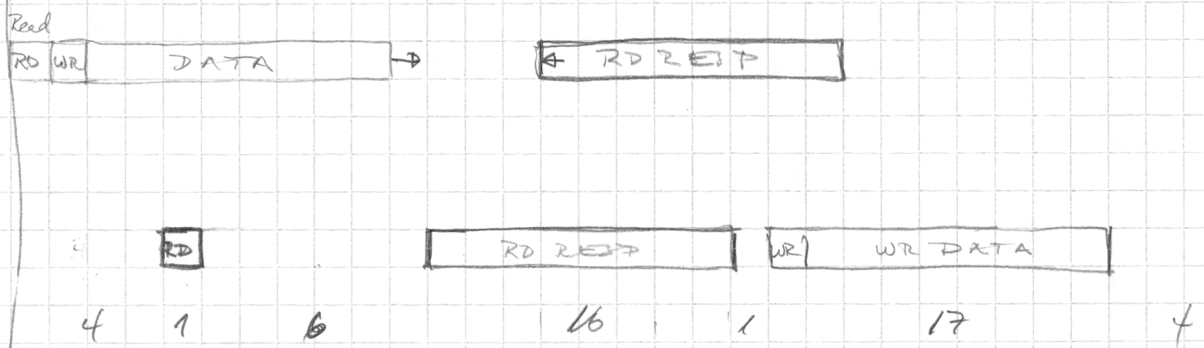
Average 0.21 mA

V_{OL} = 0.5 V @ 5 mA = 0.1 k.

PSOUT = 0.21 × 0.21 × 100 = 4.41 µW

PROCESSOR

BUS



49 clock cycles ~ 50

Sysbus : 34/49 = 0.68

Procbus : 16/49 = 0.32

1.00

Avg. 0.50

40 MHz ~ 20 MHz data rate

Control Register

Write addr= 6 00 00 00 00

Bit	Function
0	Enable subblock ordering
1	Disable PROM address decoding
2	Select 1 ms timer interrupt
3	Reset processor parity error flag
4	Reset bus parity errror flag
5	Reset missing TACK flag
6	Lamp 0
7	Lamp 1
8	Select 10 ms timer interrupt
9	Select 64 bytes cache line length (bit 6)
10	Select 32 bytes cache line length (bit 5)

Interrupt Reset Register

Write addr= 6 00 00 00 08

Bit	Function
0	Reset R4000 interrupt 0, 0 = reset
1	- - - 1, 0 = reset
.	
.	
6	Reset R4000 interrupt 6, 0 = reset
7:15	Not used
16	Reset PE-bit 16, 0 = reset
17	- - 17, 0 = reset
.	
.	
31	Reset PE-bit 31, 0 = reset

Status Register

Read addr= 6 00 00 00 08

Bit	Function
0	Subposition 0
1	- 1
2	Backplaneposition ID 0
3	- - 1
4	- - 2
5	- - 3
6	Local
7	Debug input flag
8	Processor addr parity error
9	- data - -
10	Bus addr parity error
11	- data - -
12	Missing TACK
13	Not used
14	- -
15	- -
16:31	PE-Register

Debug Input Register

Read addr= 6 00 00 00 10

Bit(15:0) = debug input data

Interrupt Counter

Write addr= 6 00 00 00 10
Read addr = 6 00 00 00 20

Bit(15:0) = 4 decade counters

Control Register

Write addr= 6 00 00 00 00

Bit	Function
0	Enable subblock ordering
1	Disable PROM address decoding
2	Select 1 ms timer interrupt
3	Reset processor parity error flag
4	Reset bus parity errror flag
5	Reset missing TACK flag
6	Lamp 0
7	Lamp 1
8	Select 10 ms timer interrupt
9	Select 64 bytes cache line length (bit 6)
10	Select 32 bytes cache line length (bit 5)

Interrupt Reset Register

Write addr= 6 00 00 00 08

Bit	Function
0	Reset R4000 interrupt 0, 0 = reset
1	- - - 1, 0 = reset
.	
.	
6	Reset R4000 interrupt 6, 0 = reset
7:15	Not used
16	Reset PE-bit 16, 0 = reset
17	- - 17, 0 = reset
.	
.	
31	Reset PE-bit 31, 0 = reset

Status Register

Read addr= 6 00 00 00 08

Bit	Function
0	Subposition 0
1	- 1
2	Backplaneposition ID 0
3	- - 1
4	- - 2
5	- - 3
6	Local
7	Debug input flag
8	Processor addr parity error
9	- data - -
10	Bus addr parity error
11	- data - -
12	Missing TACK
13	Not used
14	- -
15	- -
16:31	PE-Register

Debug Input Register

Read addr= 6 00 00 00 10

Bit(15:0) = debug input data

Interrupt Counter

Write addr= 6 00 00 00 10
Read addr = 6 00 00 00 20

Bit(15:0) = 4 decade counters

Status Register

Read addr= 6 00 00 00 08

Bit	Function
0	Subposition 0
1	- 1
2	Backplaneposition ID 0
3	- - 1
4	- - 2
5	- - 3
6	Local
7	Debug input flag
8	Processor addr parity error
9	- data - -
10	Bus addr parity error
11	- data - -
12	Missing TACK
13	Not used
14	- -
15	- -
16:31	PE-Register

Debug Input Register

Read addr= 6 00 00 00 10

Bit(15:0) = debug input data

Interrupt Counter

Write addr= 6 00 00 00 10
Read addr = 6 00 00 00 20

Bit(15:0) = 4 decade counters

AAJ/930322
CPU AGENT

CONTROL REGISTER

Addr = 6 00 00 00 00 (write only)

BIT	FUNCTION
0	Subblock ordering
1	PROM disable
2	Select 1 ms timer interrupt
3	Reset Proc. Par. Error flags
4	Reset Bus Par. Error flags
5	Reset Missing TACK flag
6	Lamp 0
7	Lamp 1
8	Select 1 ms
9	- 10 ms

INTERRUPT RESET REGISTER

Addr = 6 00 00 00 08 (write only)

BIT	FUNCTION
0	RESET R4000 INTR 0 (0 = RESET)
1	- - - 1
-	
-	
6	RESET R4000 INTR 6
7:15	NOT USED
16	RESET PE-BIT 16 (0 = RESET)
17	- - 17
-	
-	
31	RESET PE-BIT 31

AAJ / 930323
CPU AGENT

STATUS REGISTER

Addr = 6 00 00 00 08 (read only)

BIT	FUNCTION
0	SUBPOS 0
1	— 1
2	BPPOS 0
3	— 1
4	— 2
5	— 3
6	LOCAL
7	DEBUG INP FLAG
8	PROC ADDR PAR ERROR
9	— DATA — —
10	BUS ADDR — —
11	— DATA — —
12	MISSING TACK
13	NOT USED
14	— —
15	— —

16:31 PE REGISTER

DEBUG INP REGISTER

Addr = 6 00 00 00 10 (read only)

BIT (15:0) = DEBUG INP. DATA

INTERRUPT COUNTER

Write addr = 6 00 00 00 10

Read addr = 6 00 00 00 20

BIT (15:0) = 4 DECADE COUNTER

Parity Check

Addr Parity Error = /CMD8 & VALIN & /CMDPOK^ERI

+ /CMD8 & VALIN & DTERR & (CMD7 + /CMD6 + /CMD5)

Command / Address Cycle.

Sys Cmd (8:0) is always checked

Sys AD (63:0) check is disabled for Null Req.

Data Cycle

Sys Cmd (8:0) is always checked

Sys AD (63:0) check disabled for

response data and ID = 0, 2, 4, 6

{Clean Exclusive

{Shared

and Invalidate data

/CMD6 & /CMD0 + /CMD4 + /CMD2

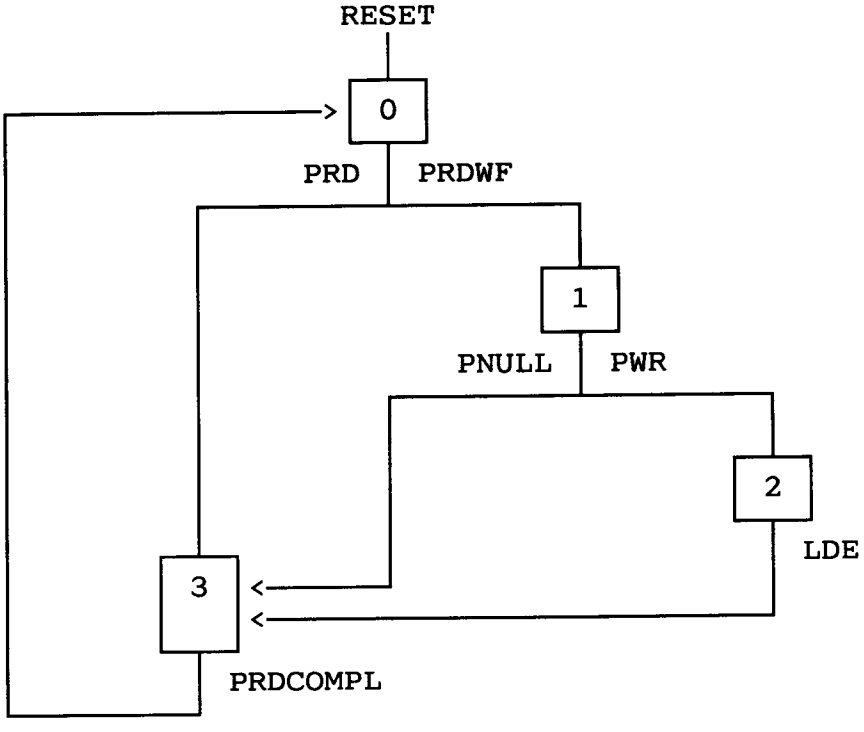
DESIGN NOTE

Name:	CPU Agent
Date:	921112
Author:	aaj
Version:	0.01
Document:	design note 2

Contents page

1 PROCESSOR REQUEST STATE MACHINES

1.1 Processor Read Request



State Equations:

State 0: Idle, waiting for read request.

goto 1 if: PRDWF
goto 3 if: PRD

State 1: Read request with write forthcoming.

goto 2 if: PWR
goto 3 if: PNULL

State 2: Write, waiting for Last Data Element (LDE).

goto 3 if: LDE

State 3: Read response data may be returned to processor.
Waiting for Read Complete (PRDCOMPL).

goto 0 if: PRDCOMPL

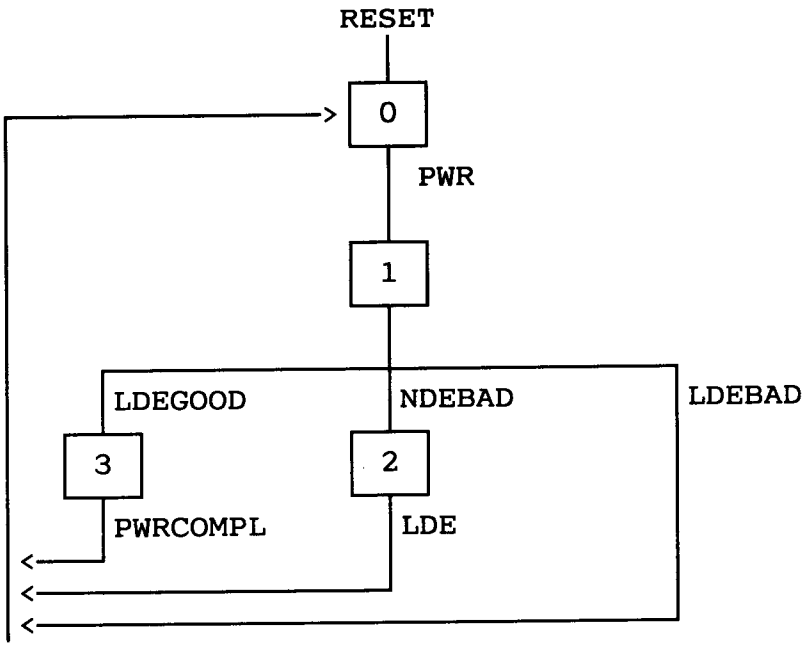
Equations:

Load Processor Read Address/Command Register: LDPRDA

```
LDPRDA=    PRDST0 & PRD
         # PRDST1 & PRDWF
```

Bus Access Request = LDPRDA

1.2 Processor Write Request



State Equations:

State 0: Idle, waiting for write request.

goto 1 if: PWR

State 1: Load write buffer.

goto 0 if: LDEBAD
goto 2 if: NDEBAD
goto 3 if: LDEGOOD

State 2: Bad data received, wait for LDE.

goto 0 if: LDE

State 3: Data loaded, wait for write complete (PWRCOMPL)

goto 0 if: PWRCOMPL

Equations:

Load Processor Write Address and Command Register: LDPWRA

LDPWRA= PWRST0 & PWR

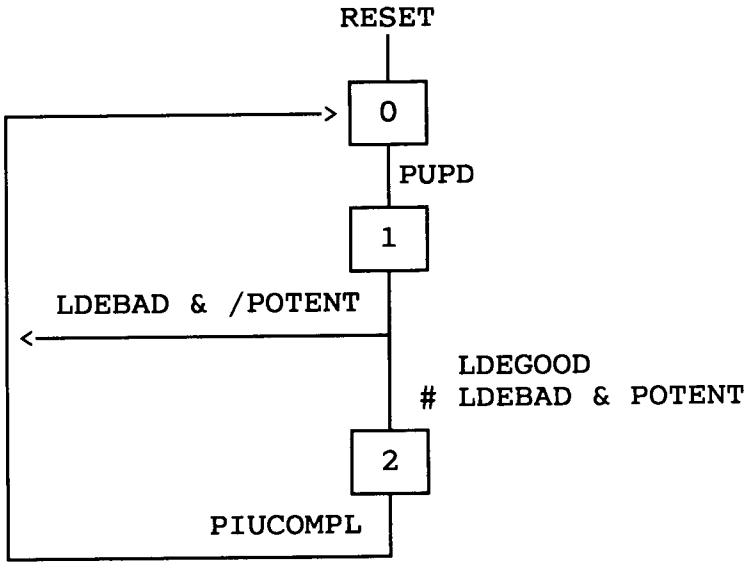
Load Processor Write Data Buffer: LDPWRD

LDPWRD= PWRST1 & SVALO

Bus Access Request: PWRBAR

PWRBAR = PWRST1 & LDEGOOD; (= state 1 & goto 3)

1.3 Processor Update Request



State Equations:

State 0: Idle, waiting for update command.

goto 1 if: PUPD

State 1: Waiting for update data.

goto 2 if: LDEGOOD # LDEBAD & POTENT
goto 0 if: LDEBAD & /POTENT;

State 2: Data loaded, waiting for update termination.

goto 0 if: PIUCOMPL; (invalidate or update cmd completed)

Flags:

POTENT, potential update command.

set POTENT= PUPDST0 & PUPD & PCMDIN3

clear POTENT= PUPDST2 & PIUCOMPL
RESET

PUPDBAD, update data register contains bad data

set PUPDBAD= PUPDST1 & LDEBAD & POTENT

clear PUPDBAD= PUPDST2 & PIUCOMPL
RESET

Equations:

Load processor invalidate/update addr/cmd register:

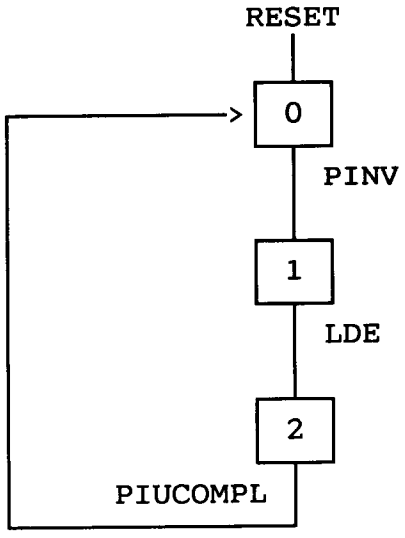
```
LDPIUA=    PUPDST0 & PUPD
         # PINVST0 & PINV
```

Load processor update data register:

```
LDPUPDD=    PUPDST1 & LDEGOOD
          # PUPDST1 & LDEBAD & POTENT
```

Set bus access request = LDPUPDD

1.4 Processor Invalidate Request



State Equations:

State 0: Idle, waiting for invalidate command.

goto 1 if: PINV

State 1: Waiting for dummy data cycle.

goto 2 if: LDE

State 2: Waiting for bus access termination.

goto 0 if: PIUCOMPL; (invalidate or update complete)

Equations:

Load processor invalidate/update addr/cmd register:

```
LDPIUA=   PUPDST0 & PUPD
        # PINVST0 & PINV
```

Set bus access request:

```
PINVBAR= PINVST1 & LDE
```

1.5 Ready and IvdAck/IvdErr Control

Write Ready

```
WRRDY= PWRST0
```

Invalidation/Update Acknowledge

```
IVDACK:=   PUPDST2 & IUCOMPL & /UDDBAD & /UDNULL
         # PINVST2 & IUCOMPL
```

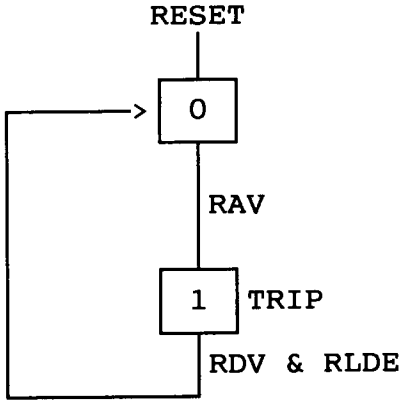
Invalidation/Update Error

```
IVDERR:=   PUPDST2 & IUCOMPL & UDDBAD & /UDNULL
         # PUPDST1 & LDEBAD & /POTENT
```

2 SYSTEM BUS MASTER STATE MACHINES

2.1 BUSIDLE Control

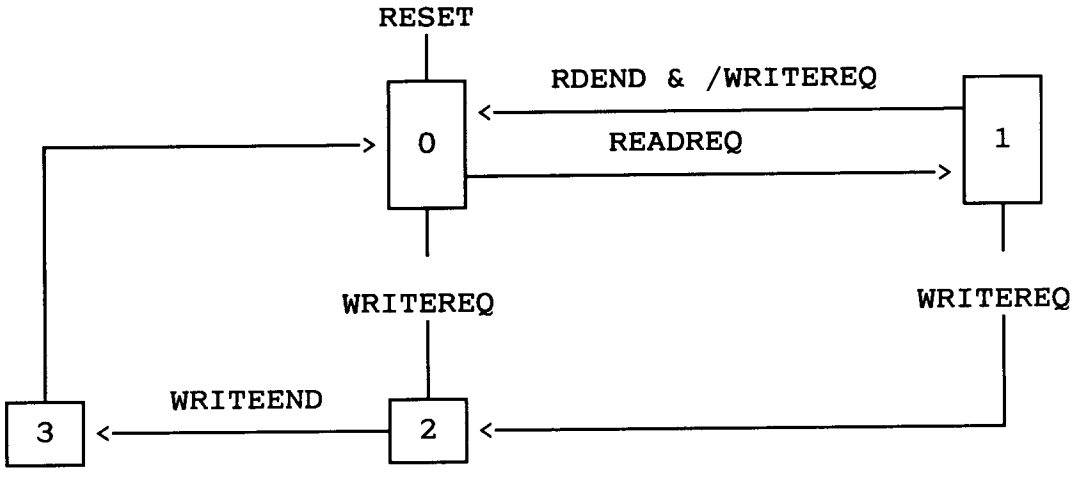
Bus master selection occurs simultaneously with the current bus transaction. Start of a new transaction must therefore wait for termination of the current transaction.



TRIP (Transaction I Progress)

```
TRIP:=  RAV & /RESET
      # TRIP & /(RDV & RLDE) & /RESET

BUSIDLE=  /(RAV # TRIP & /(RDV & RLDE)) & /RBUSYIN
```

2.2 Bus Master Main State Machine



State Equations:

```
STRACT= (BAREQ & BAGRANT # BARQACK) & BUSIDLE & /BUSBUSY
```

State 0: Idle
```
goto 1 if:   STRACT & PRDRQ
goto 2 if:   STRACT & /PRDRQ
```

State 1: BMRDCYC, Bus master read cycle
```
goto 0 if:   RDV & RLDE & /STRACT # RDV & RLDE & PRDRQ
goto 2 if:   RDV & RLDE & STRACT & /PRDRQ
```

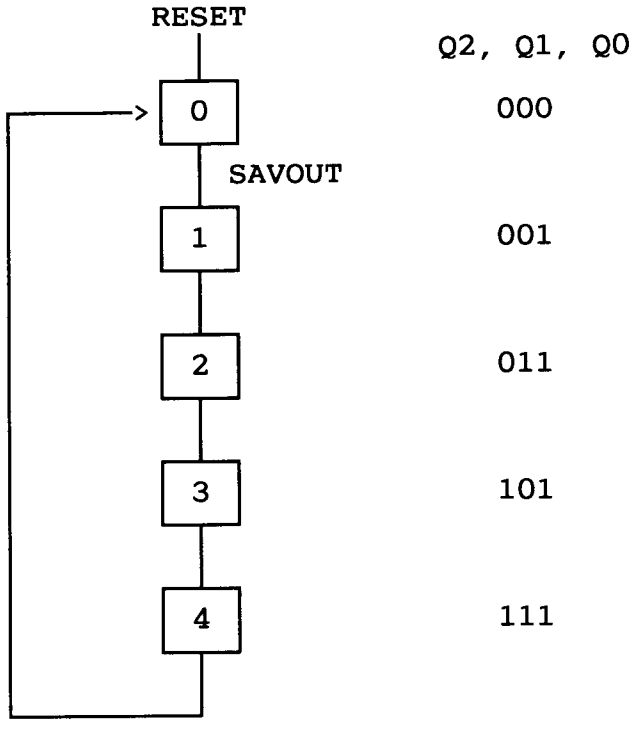
State 2: BMWRCYC, Bus master write cycle
```
goto 3 if:   TLDE
```

State 3:
```
goto 0
```

Equations:

```
AVOUT:=   BMST0 & STRACT
        # BMRDCYC & RDV & RLDE & GRBRQ & /PRDRQ

DVOUT:= BMST2
```

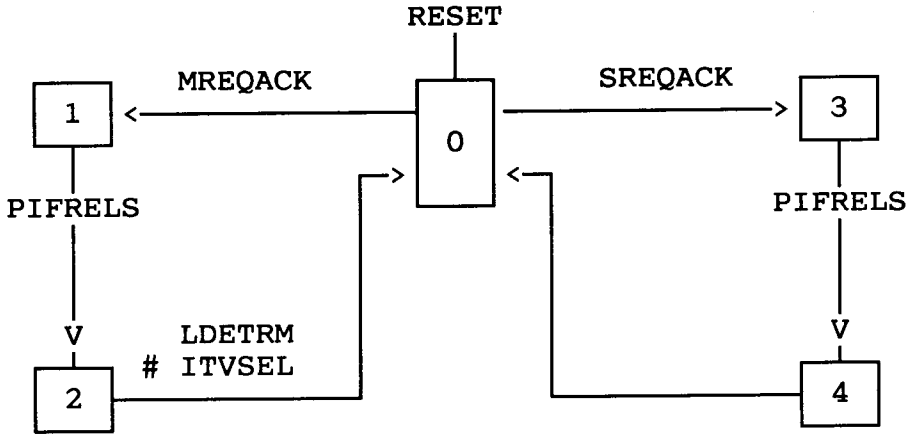
2.3 BUSYOUT State Machine




```
Q0:=  SAVOUT & /RESET
    # Q0 & /Q1 & /RESET
    # Q0 & /Q0 & /RESET

Q1:=  BUSYOUT & Q0 & /RESET

Q2:=  /Q1 & Q0 & /RESET
    # Q1 & /Q0 & /RESET

BUSYOUT:=  SAVOUT & /RESET
         # Q0 & /Q1 & /RESET
         # Q0 & /Q0 & /RESET
```

3 HOST PORT TO PROCESSOR REQUESTS

3.1 Host Port Access Control



State Equations:

State0: Idle
goto 1 if: MRQACK
goto 3 if: SLVRQACK

State 1: Wait for processor release
goto 3 if: PIFRELS

State 2: Enable host port transceivers
goto 0 if: LDETRM # ITVSEL

State 3: Wait for processor release
goto 4 if: PIFRELS

State 4: Send release to slave CA
goto 0

Equations:

```
Released:=  State0 & PRELS
          # Released & State0

PIFRELS=    Released # PRELS

SETEXTRQ=  BERRITR # SLVRQ # BUSCM # TMITR # IRRST
         # (BRDEN & BRSPRDY # ARSPRQ) & LOCAL
```

AFLEVERING TIL ES2

1. FASTsims

2. runFAST

   - Netlist Tools

   Vector tools : to_swif (min og max) ✓

   to_swf (min og max)

   ~~pad_check~~:

   Checkers : pad check ✓

   wave check - max ✓

   default_wave_comp ✓

   :

   skew-check :

   ~~param-check~~

3. skipdes :

   sdot fil - måske ikke gluds på disk.

2

CONVERTEREDE TESTVEKTORER

/wd/mudv4/VVproj/ca302/

es_2pat.~~pat~~ er totalfilen til simulering

es_2pat.ref er reference (200 ns simulering)

/wd/mudv2/bbp/util

Converterings programmer

patconv: konverterer .pat filer → nyt format

savconv: konverterer simuleringsoutput → nyt format

chkconv: som savconv - men konverterer tider. - mangler de sidste rettelser.

```
|
|Viewsim command file for simulation of CA302, CPU AGENT
|
echo
echo CA302 simulation - print-on-strobe
echo 4000 ns simulation cycle
echo
|
|
wfm RCLK 0=0 1000ns=1 (2000ns=0 2000ns=1)*100000
wfm TCLK 0=0 2000ns=1 (2000ns=0 2000ns=1)*100000
wfm RBCK 0=0 2000ns=1 (2000ns=0 2000ns=1)*100000
wfm TBCK 0=0 3000ns=1 (2000ns=0 2000ns=1)*100000
|
|Input vectors
vector PCPIN       PCPO PC8O
vector PCADIN      PC[7:0]O PP[7:0]O P[63:00]O
vector PCTRIN      VALI RELS INRQ SREQ
vector PAUXIN      PCEN IOMD TREF
vector BCTRIN      AVAI DVAI BSYI TAKI ITVI SHRI SHIT BAGR RSET
vector BAUXIN      LCAL POS[3:0] SPS[1:0]
vector BCADIN      BC[7:0]O BP[7:0]O B[63:00]O
|
|Output vectors
vector PCMDOUT     PCPO PC[8:0]O
vector PADOUT      PP[7:0]O P[63:00]O
vector PAUXOUT     ITR1 ITR0 LMP1 LMP0
vector BCMDOUT     BCPO BC[7:0]O
vector BADOUT      BP[7:0]O B[63:00]O
|
|
every 4000ns do (a PCPIN   < es2_pat.pat; +
                 a PCADIN  < es2_pat.pat; +
                 a PCTRIN  < es2_pat.pat; +
                 a PAUXIN  < es2_pat.pat; +
                 a BCPO    < es2_pat.pat; +
                 a BCADIN  < es2_pat.pat; +
                 a BCTRIN  < es2_pat.pat; +
                 a BAUXIN  < es2_pat.pat)
|
sim 58035990ns
```

/CLOCK
RCLK
/SIGNALS
P000 +
P010 +
P020 +
P030 +
P040 +
P050 +
P060 +
P070 +
P080 +
P090 +
P100 +
P110 +
P120 +
P130 +
P140 +
P150 +
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P620 +
P630 +
PP00 +
PP10 +
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PP30 +
PP40 +
PP50 +
PP60 +
PP70 +
PC00 +
PC10 +
PC20 +
PC30 +
PC40 +
PC50 +
PC60 +
PC70 +
PC80 +
PCP0 +
RELS +
VALI +
INRQ +
SREQ +
/CLOCK
RBCK
/SIGNALS
B000 +
B010 +
B020 +
B030 +
B040 +
B050 +
B060 +
B070 +
B080 +
B090 +
B100 +
B110 +
B120 +
B130 +
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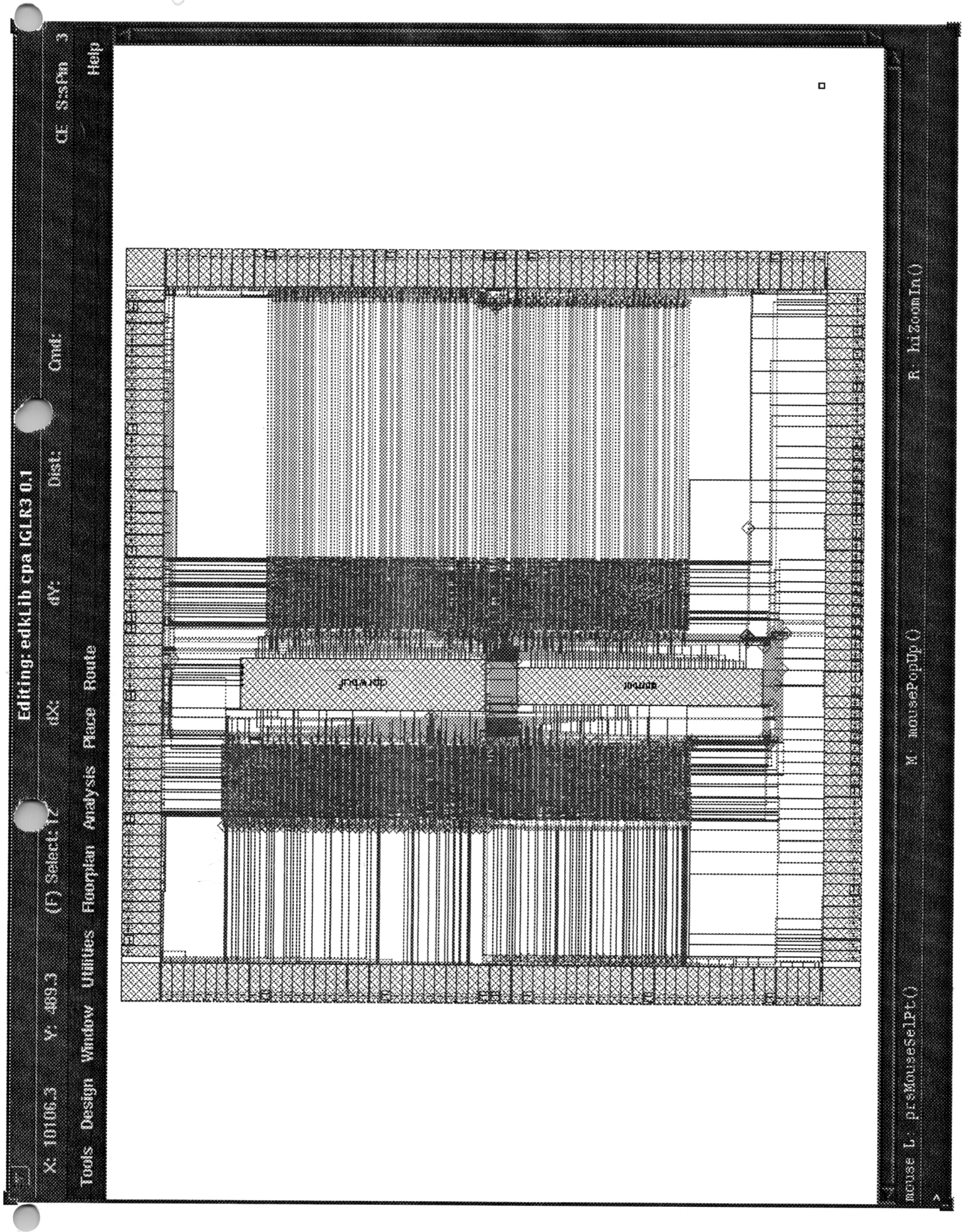
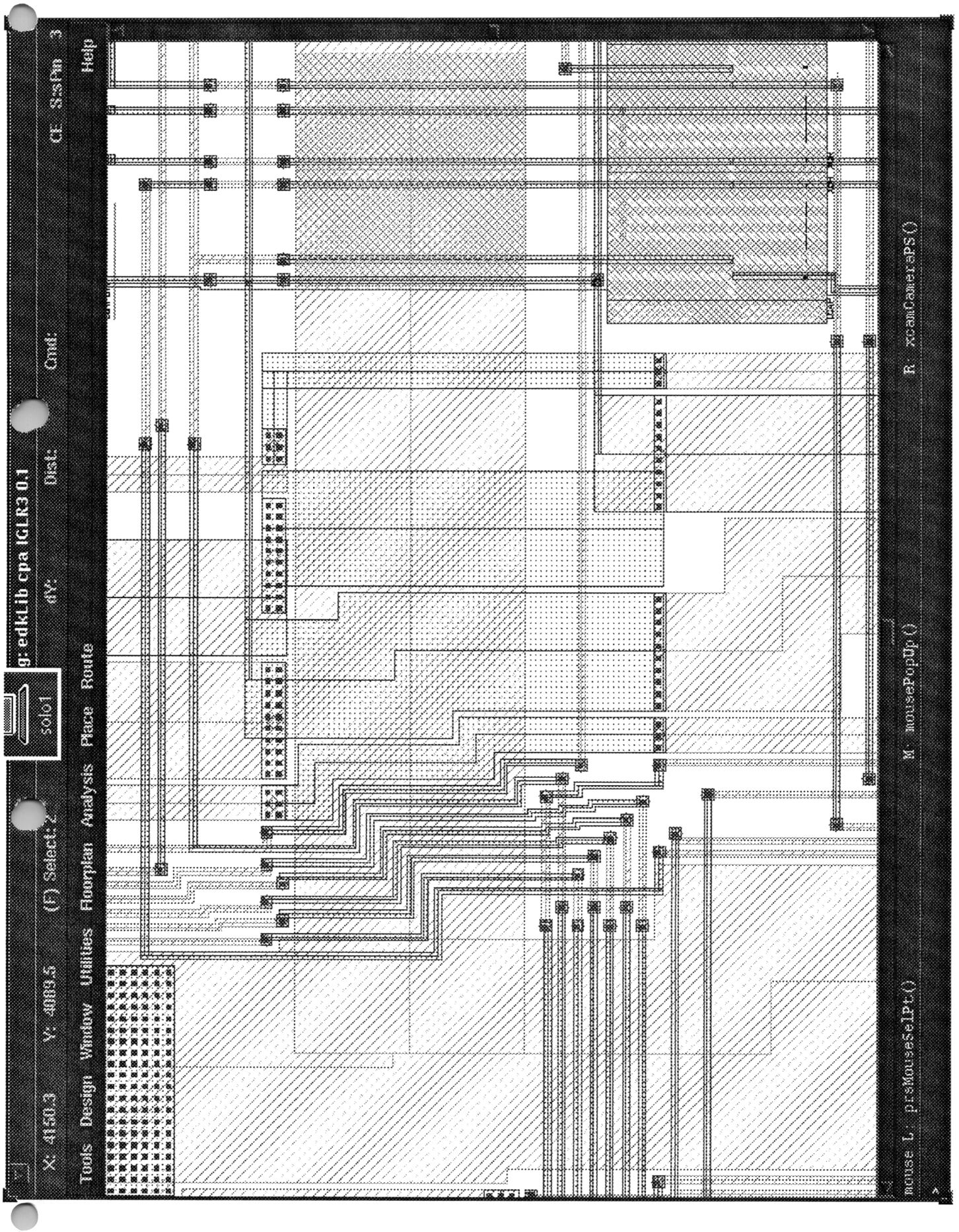
B540 +
B550 +
B560 +
B570 +
B580 +
B590 +
B600 +
B610 +
B620 +
B630 +
BP00 +
BP10 +
BP20 +
BP30 +
BP40 +
BP50 +
BP60 +
BP70 +
BC00 +
BC10 +
BC20 +
BC30 +

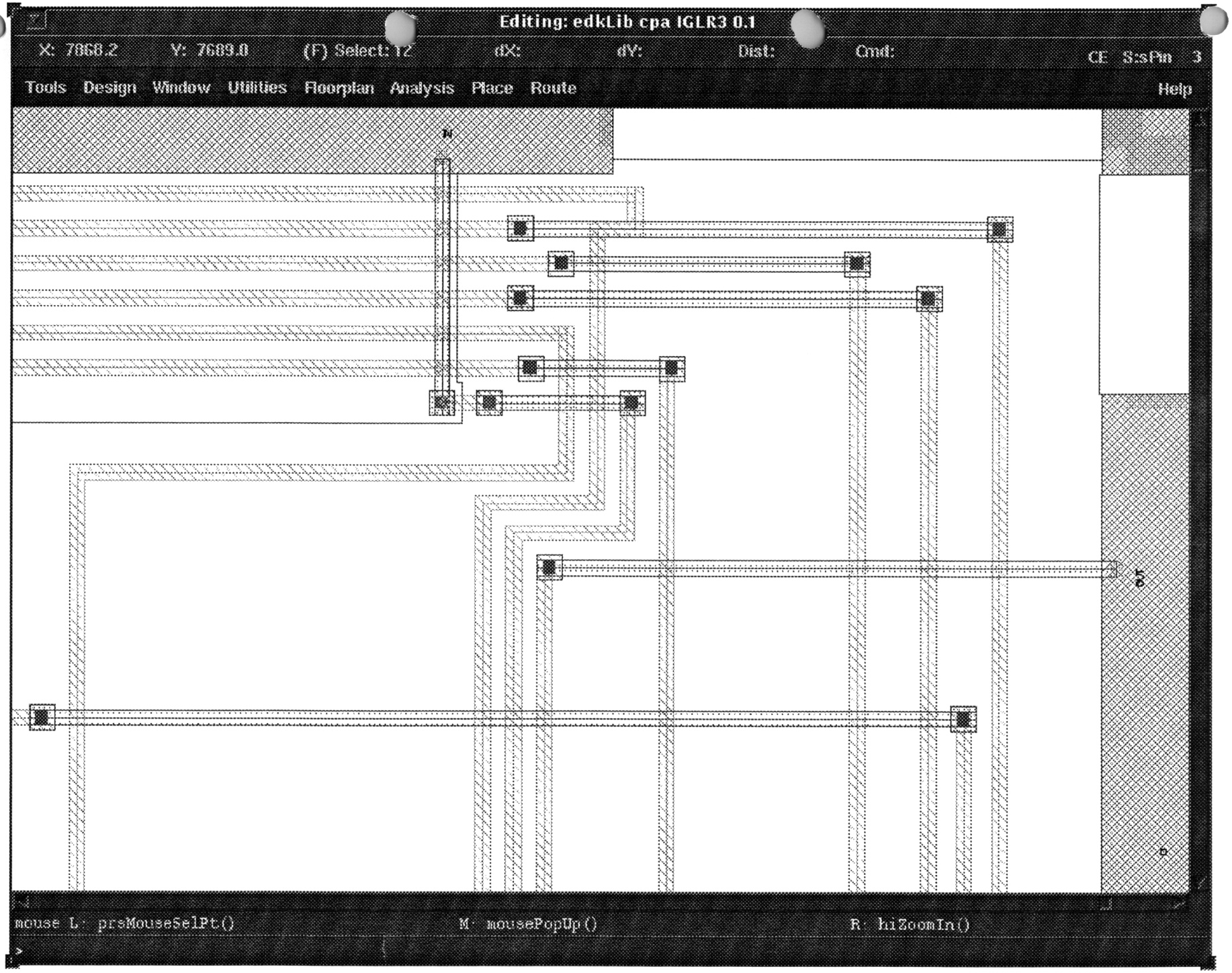
BC4O +
[illegible]O +
BC6O +
BC7O +
BCPO +
BAGR +
AVAI +
DVAI +
BSYI +
TAKI +
SHRI +
ITVI +
SHIT +
RSET +
/CLOCK
TCLK
/SIGNALS
TREF +

Typical PAD bound chip
with corners pushed out -

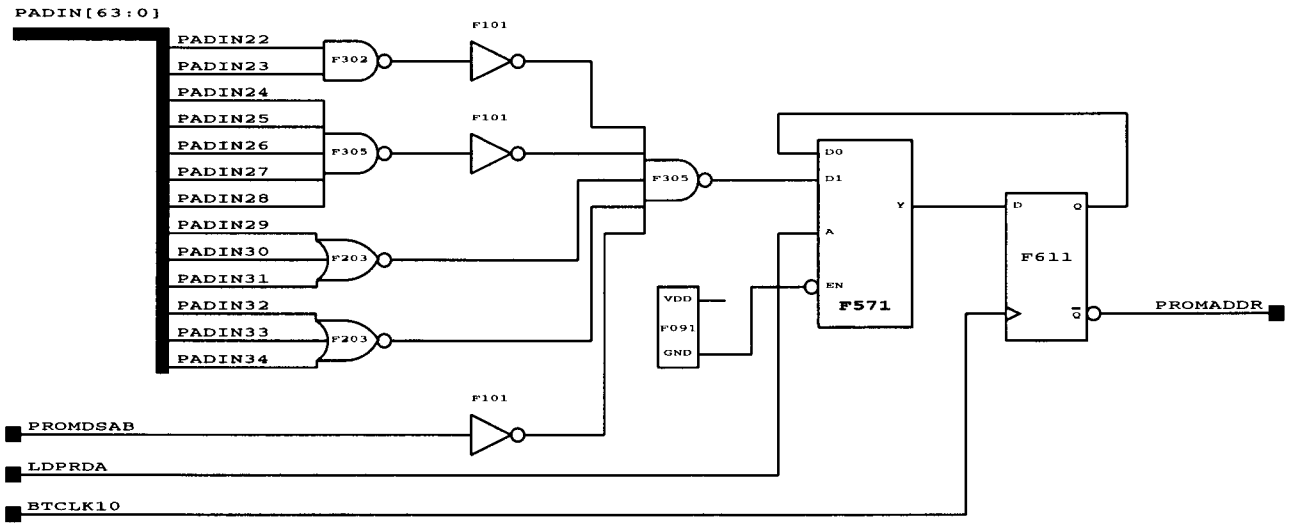


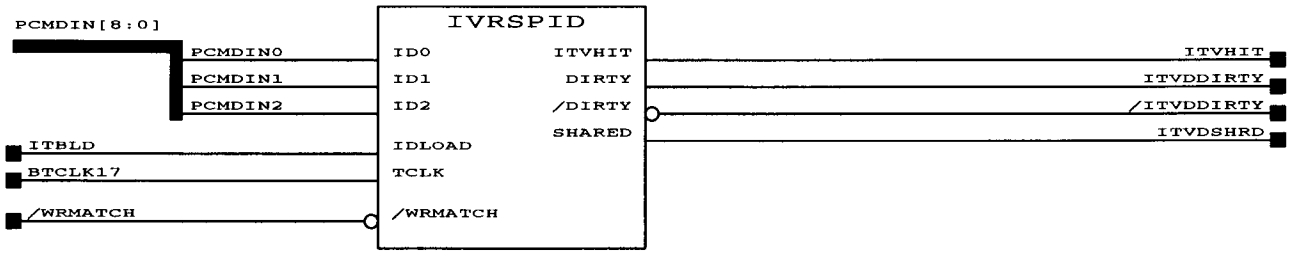
Bad routing of wide global + signal nets.



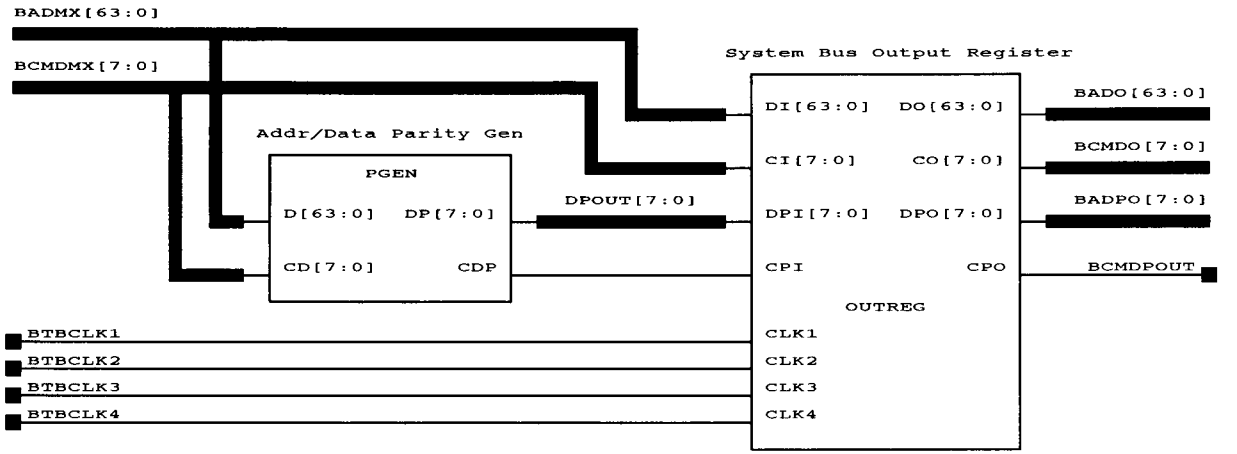


Corner pushed out (due to poor channel compaction algo.)

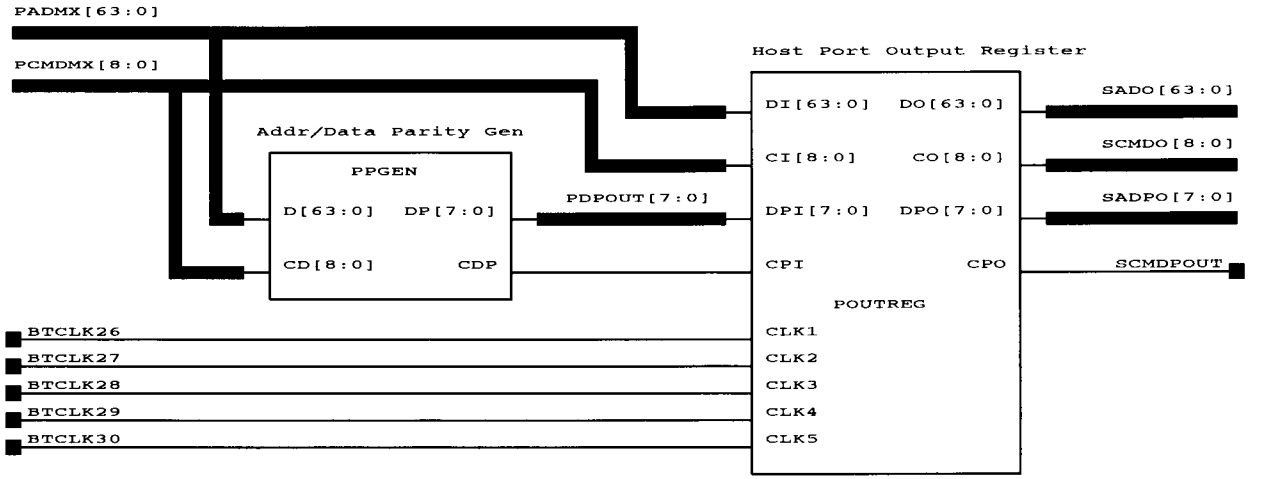




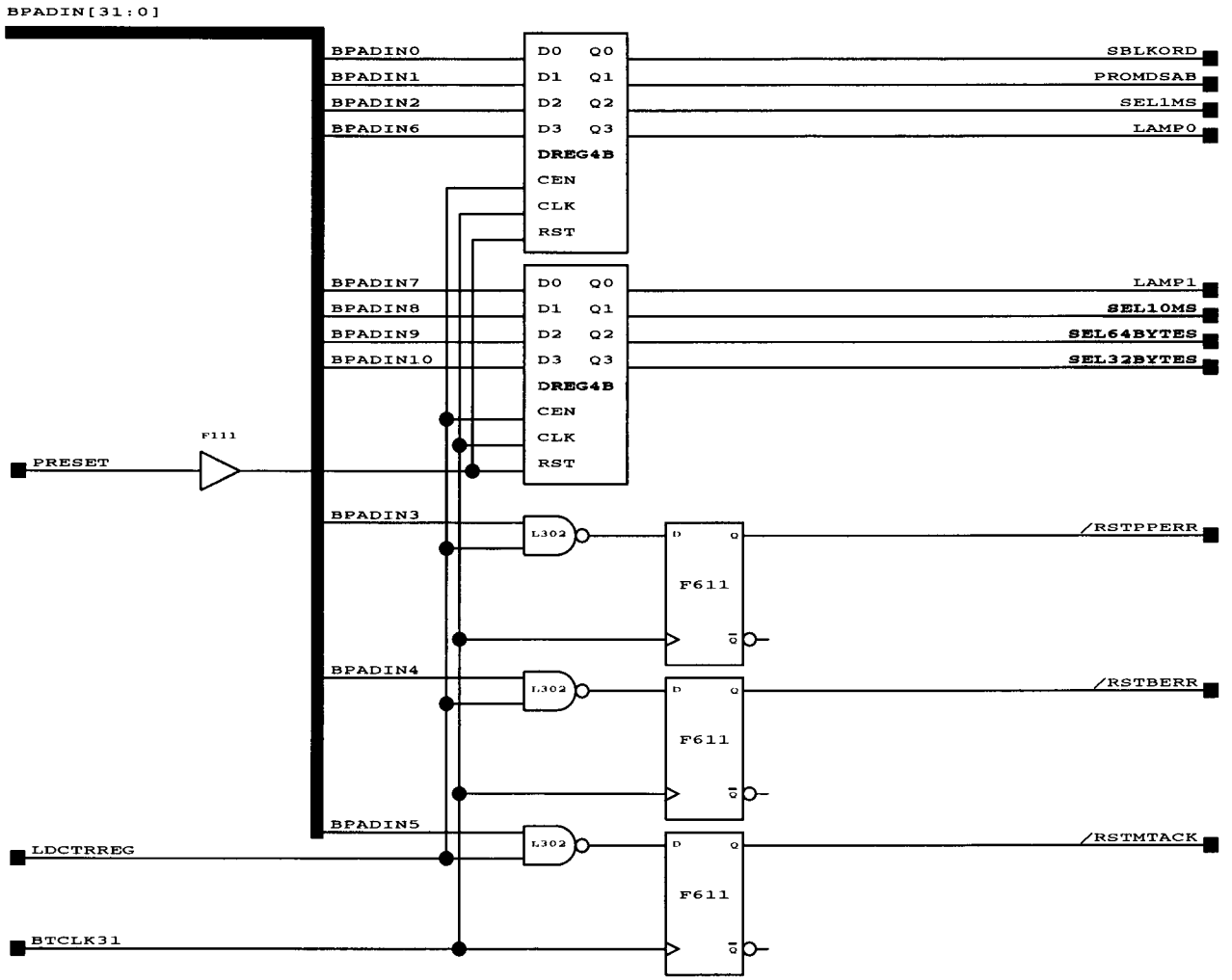
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		PROM Addr Decoding
Issue 2		Intervention Data ID
Issue 3		File: cpa.13 / Page:13 of NN



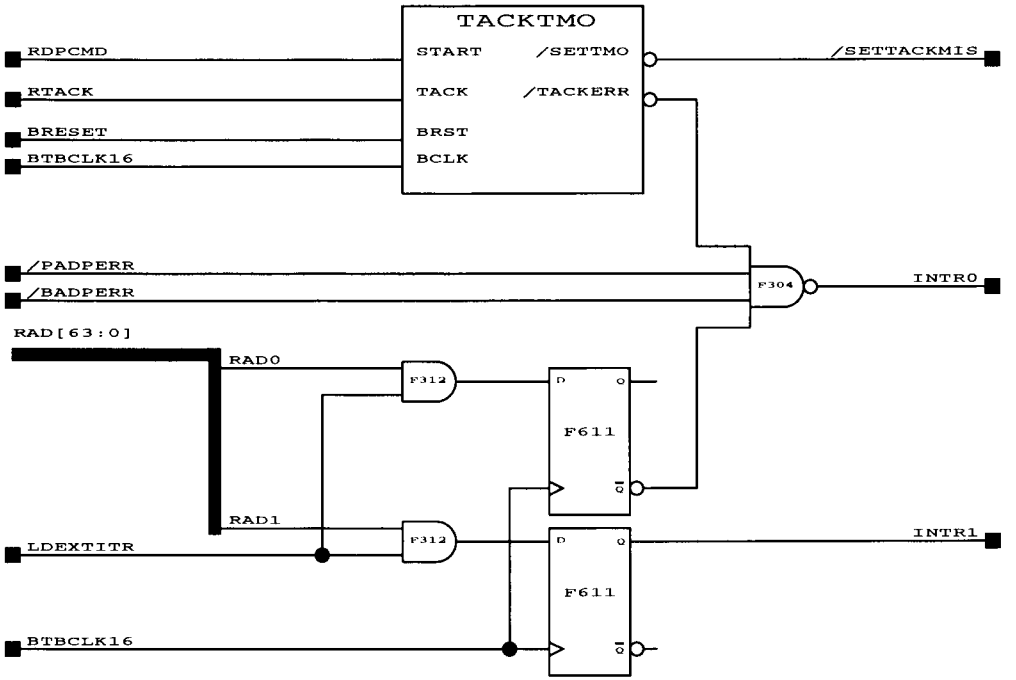
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Bus Output Register	
Issue 1			
Issue 2			
Issue 3		File: cpa.16	Page:16 of NN



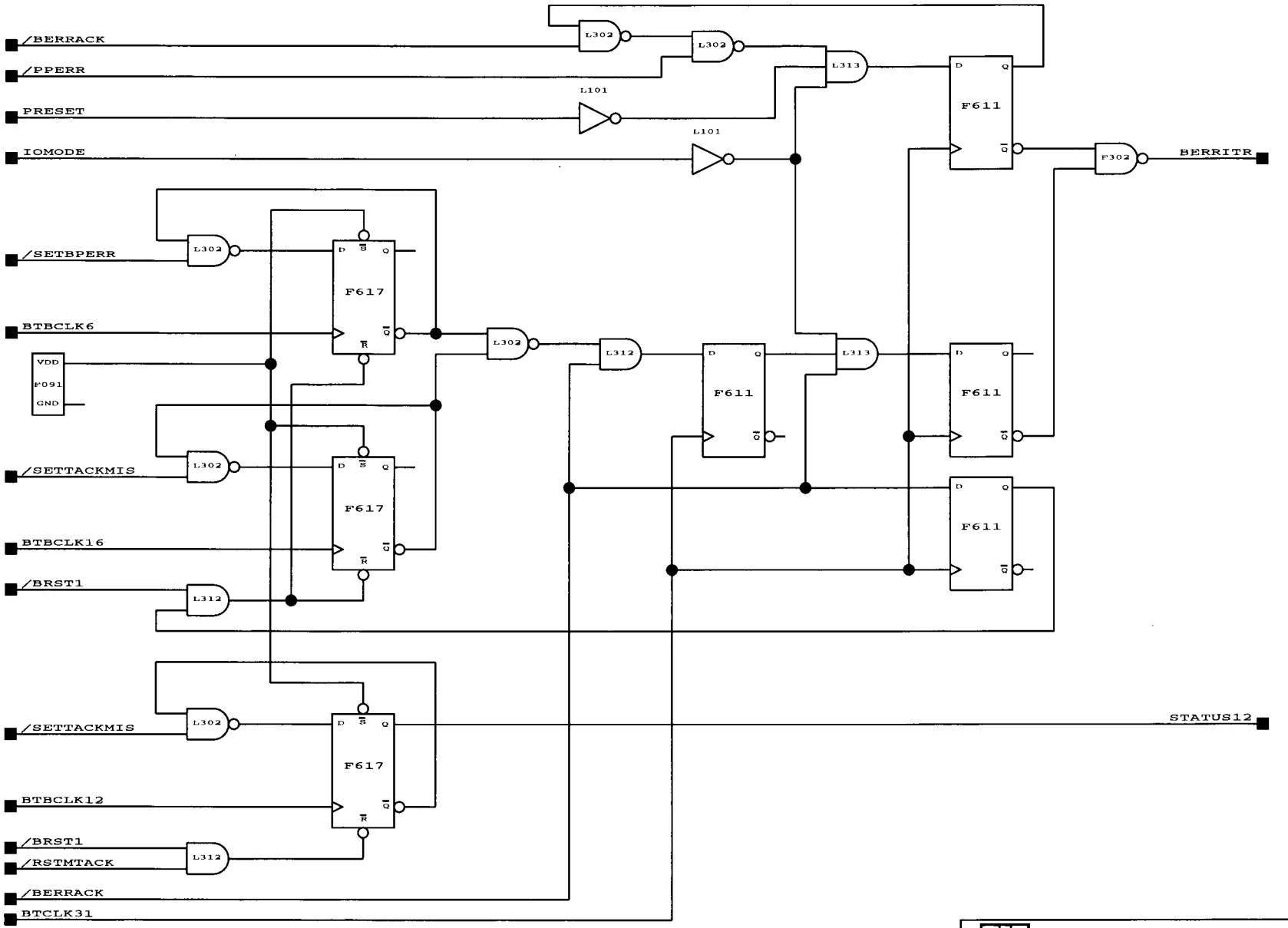
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Host Port Output Register	
Issue 1			
Issue 2			
Issue 3		File: cpa.21	Page:21 of NN



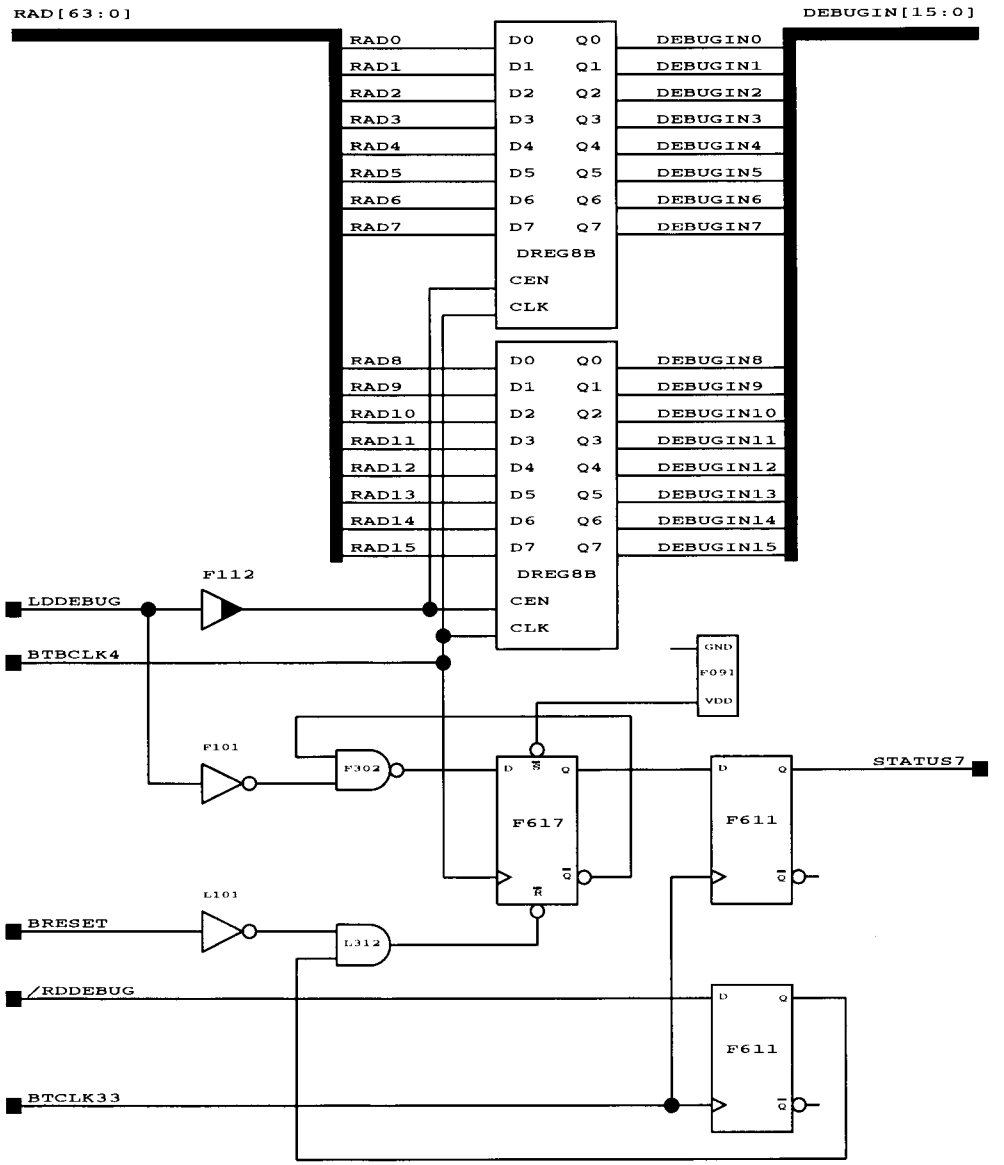
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Control Register	
Issue 1	94-07-11		
Issue 2			
Issue 3		File: cpa.23	Page:23 of NN



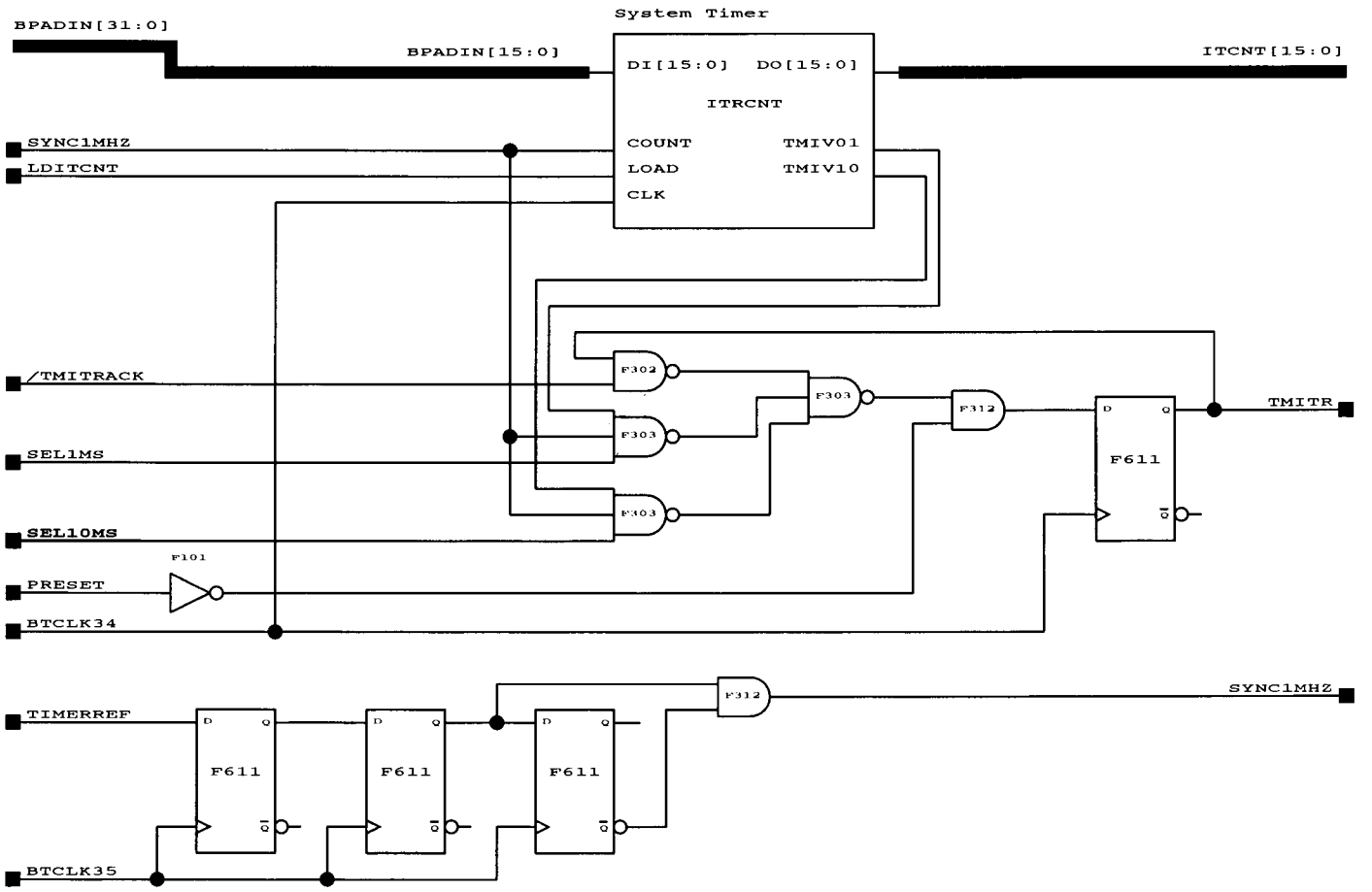
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Interrupt Pins INTR0 & INTR1	
Issue 1			
Issue 2			
Issue 3		File: cpa.25	Page:25 of NN



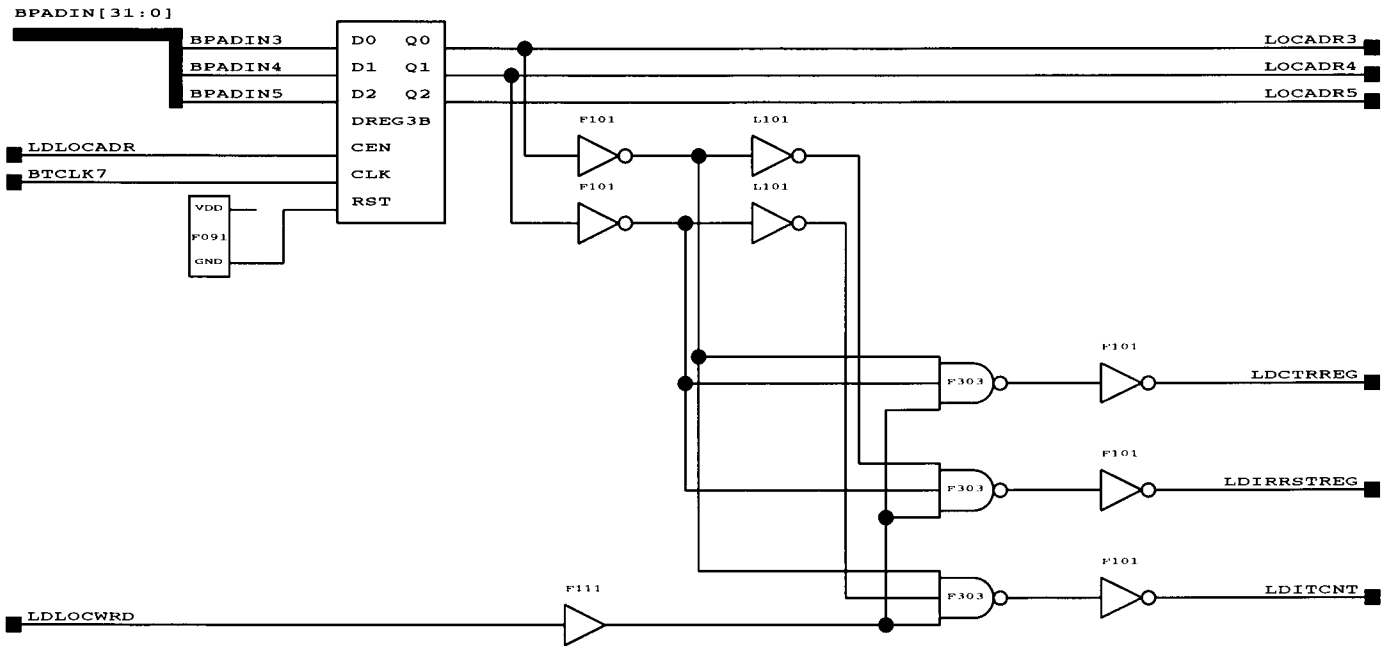
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1		Bus Error Interrupt
Issue 2		
Issue 3		File: cpa.26 Page:26 of NN



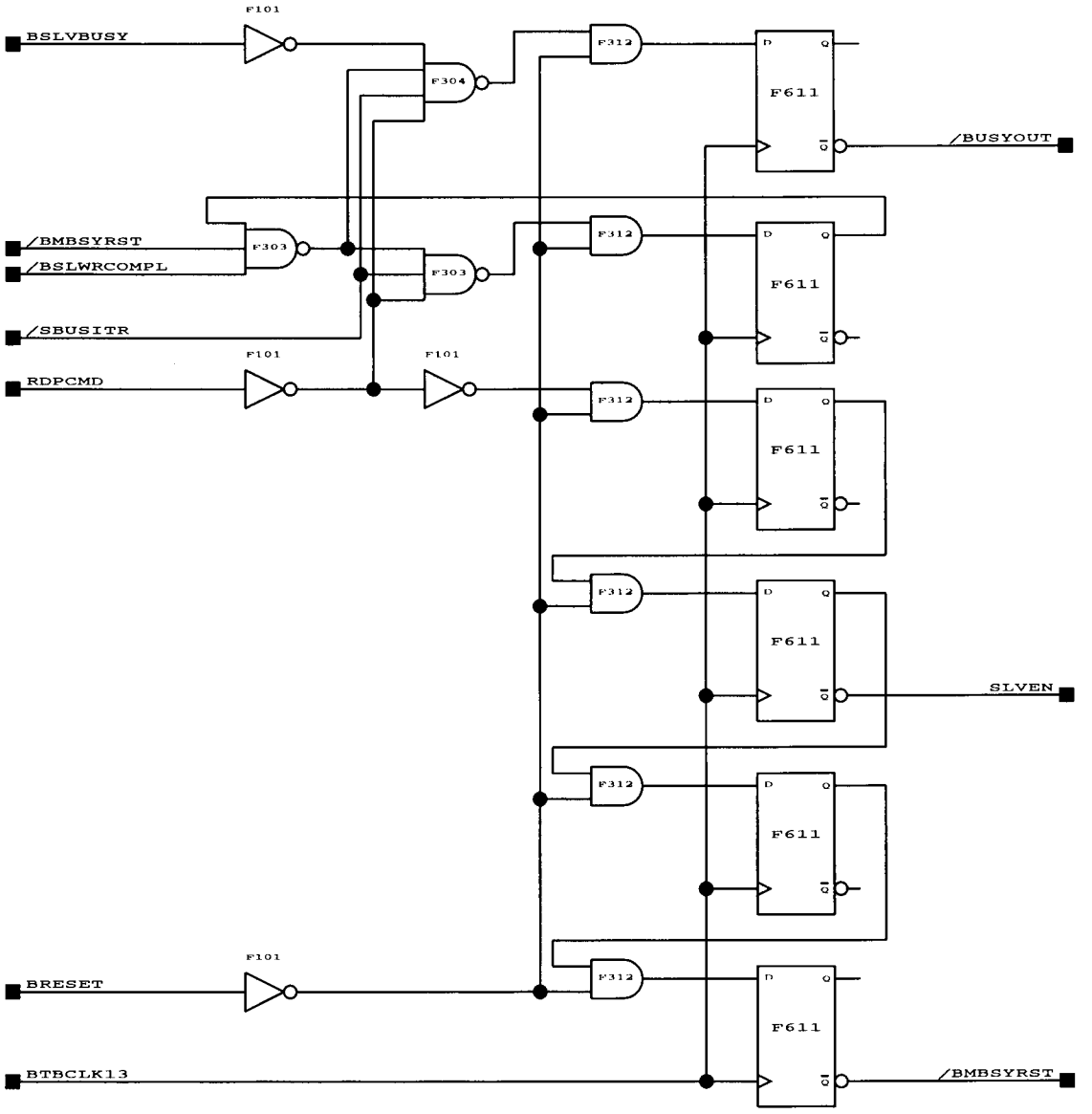
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 Debug Input Register	
Issue 1			
Issue 2			
Issue 3		File: cpa.28	Page:28 of NN



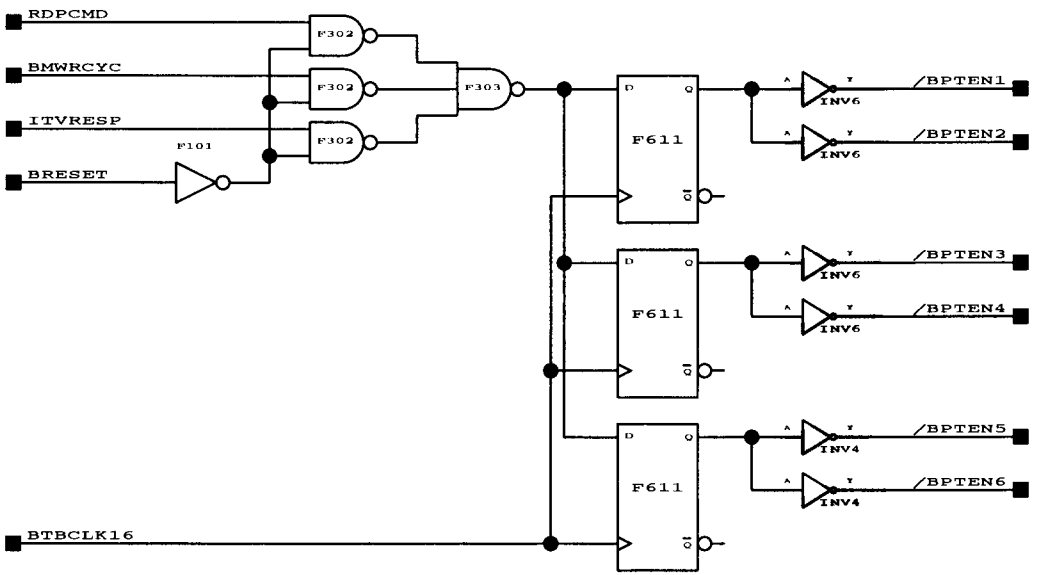
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-05-31	1/10 MS Interval Timer
Issue 2		
Issue 3		File: cpa.29 Page:29 of NN



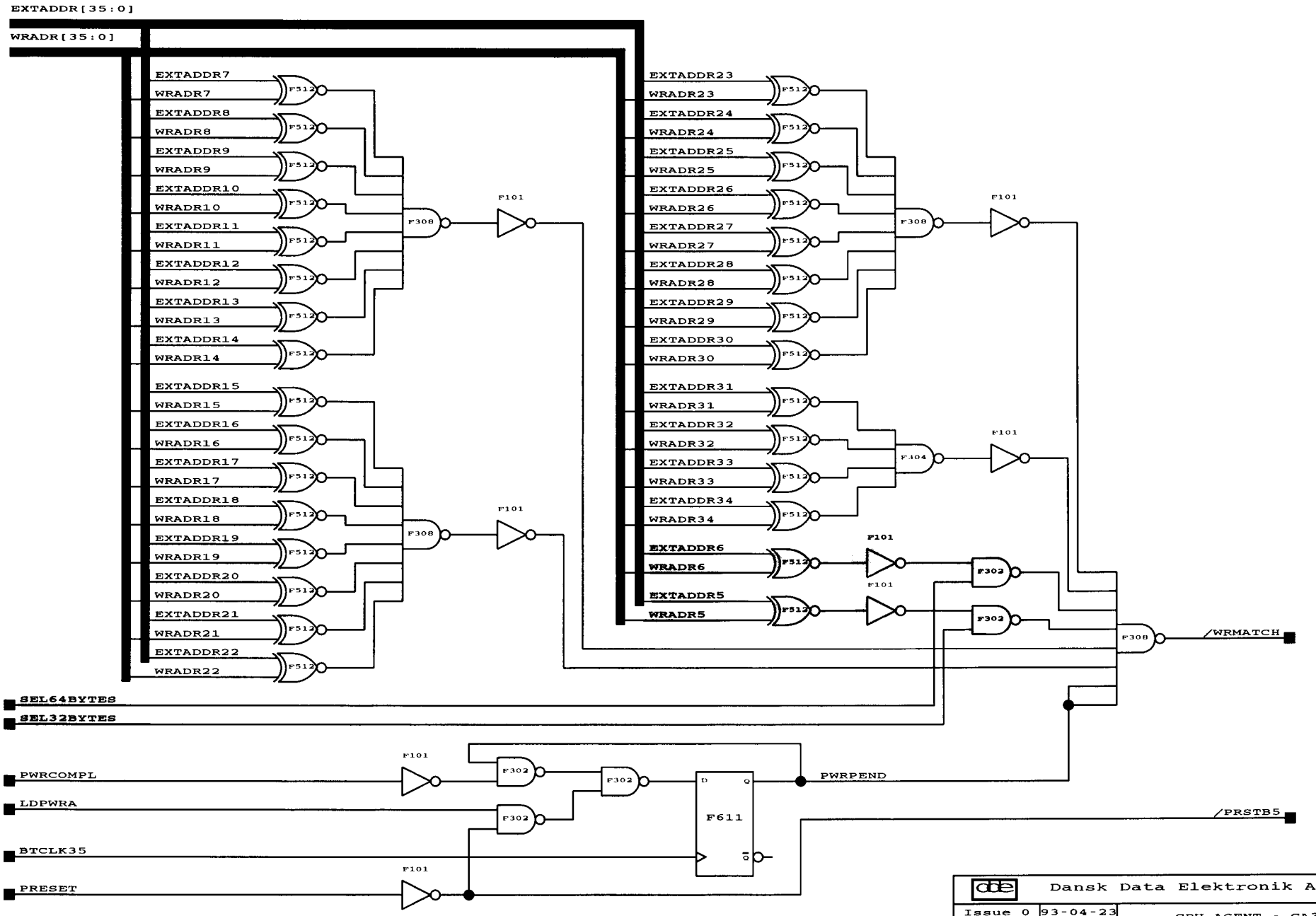
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Local Write Addr Decoding
Issue 1		
Issue 2		
Issue 3		File: cpa.30 Page:30 of NN



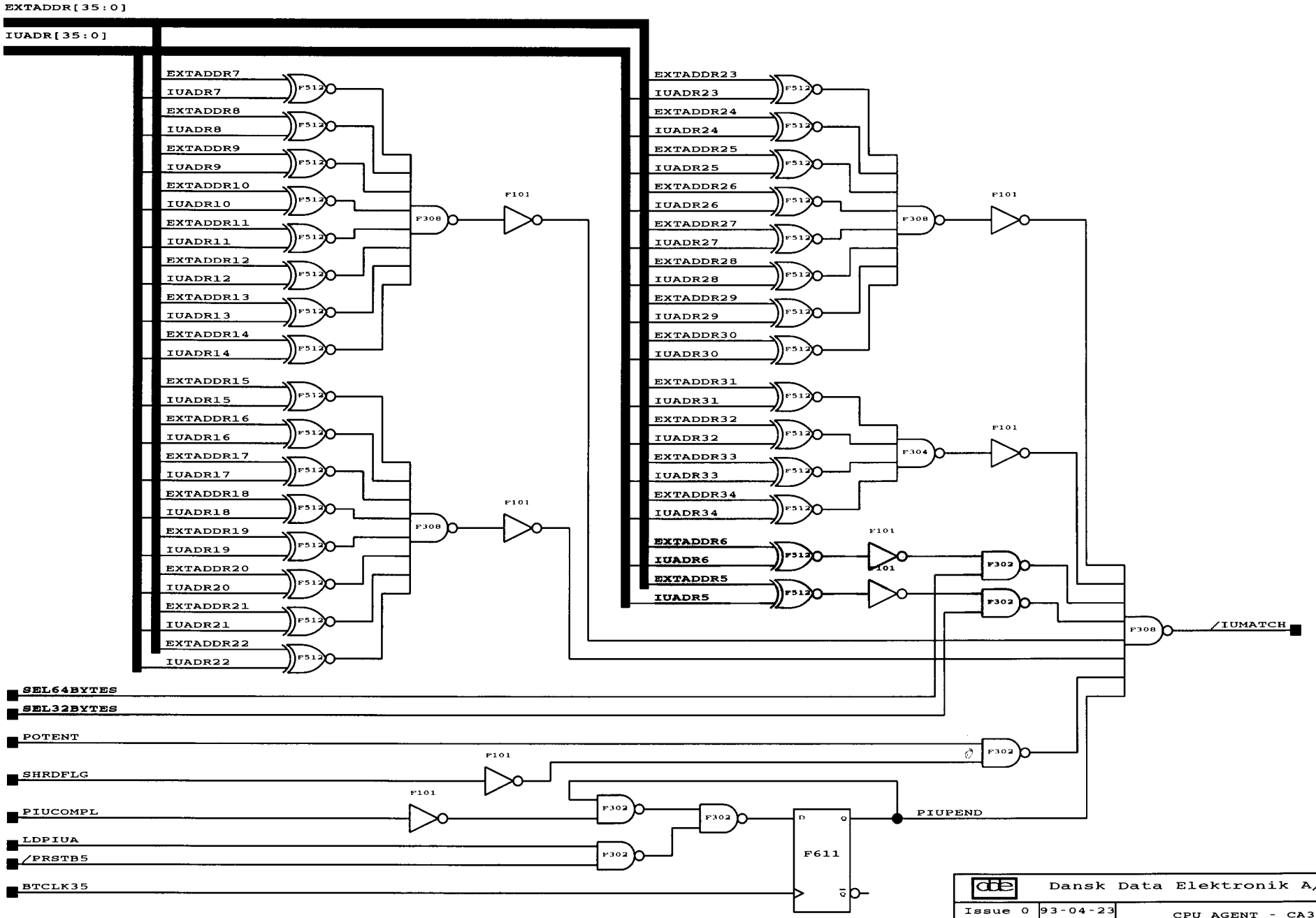
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Busy Out Control - BSYCTRL
Issue 1		
Issue 2		
Issue 3		File: cpa.32 Page:32 of NN



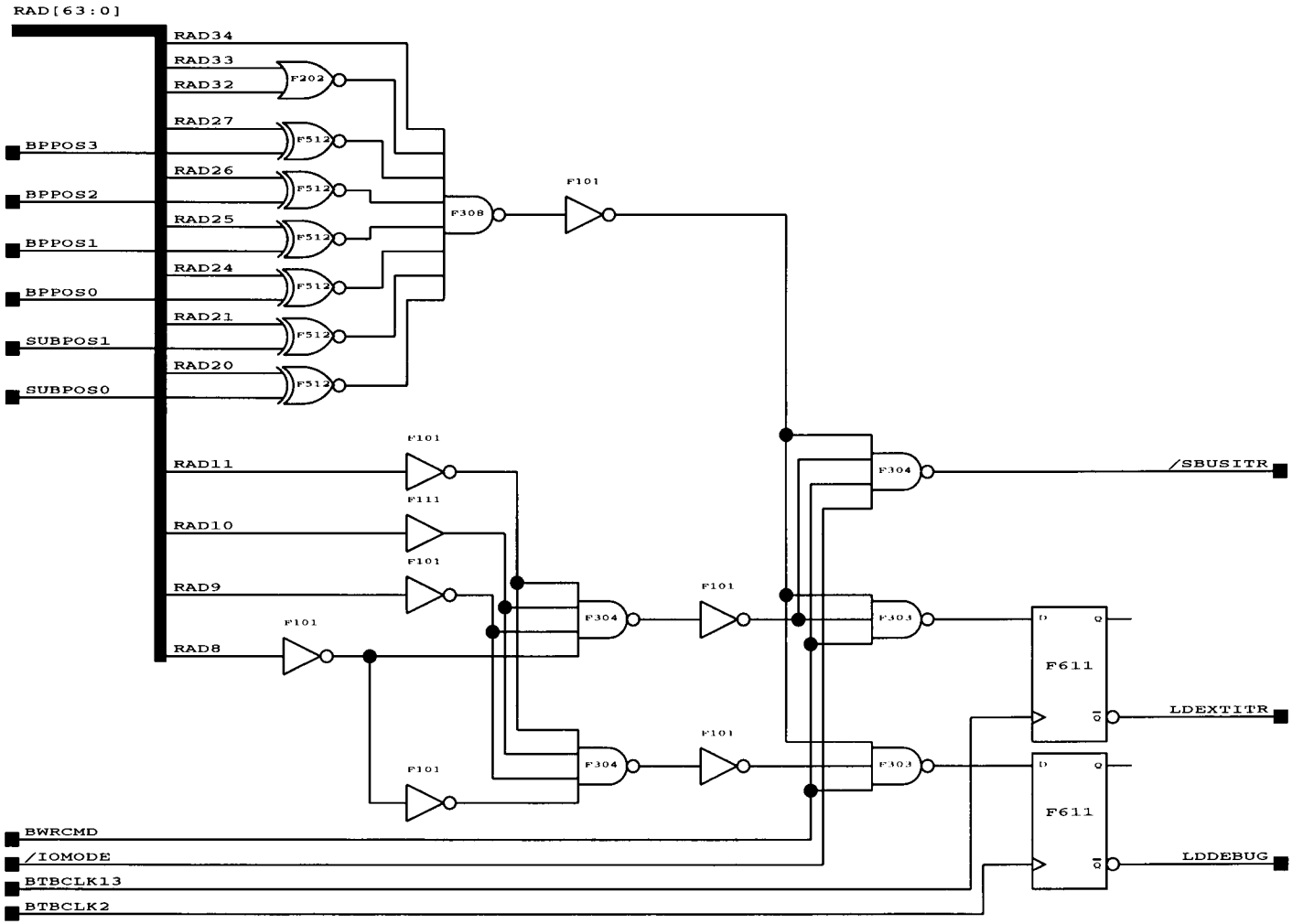
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 System Bus Transcv. Control	
Issue 1	94-07-15		
Issue 2			
Issue 3		File: cpa.33	Page:33 of NN



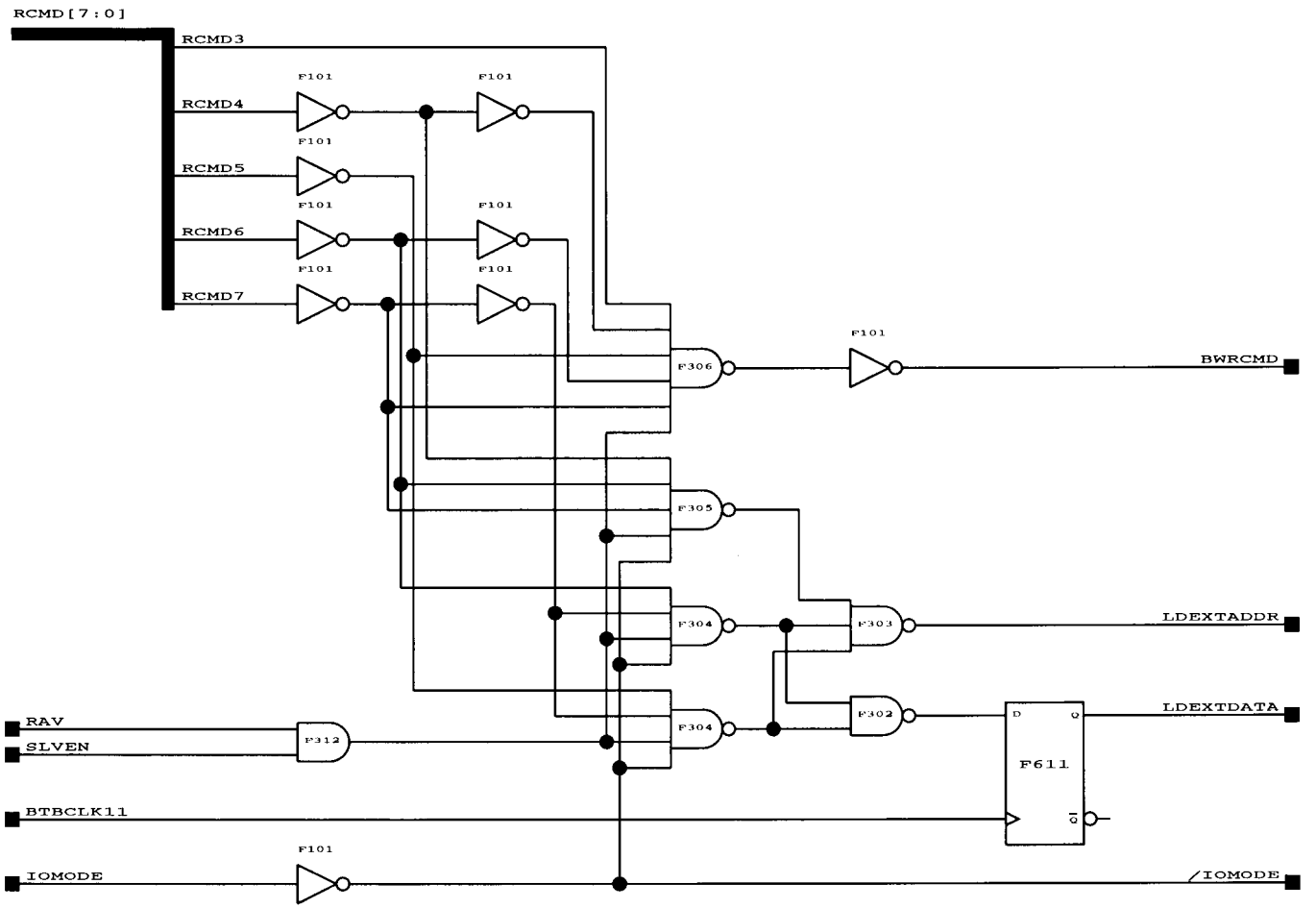
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-11	Write Address Comperator
Issue 2		
Issue 3		File: cpa.34 Page:34 of NN



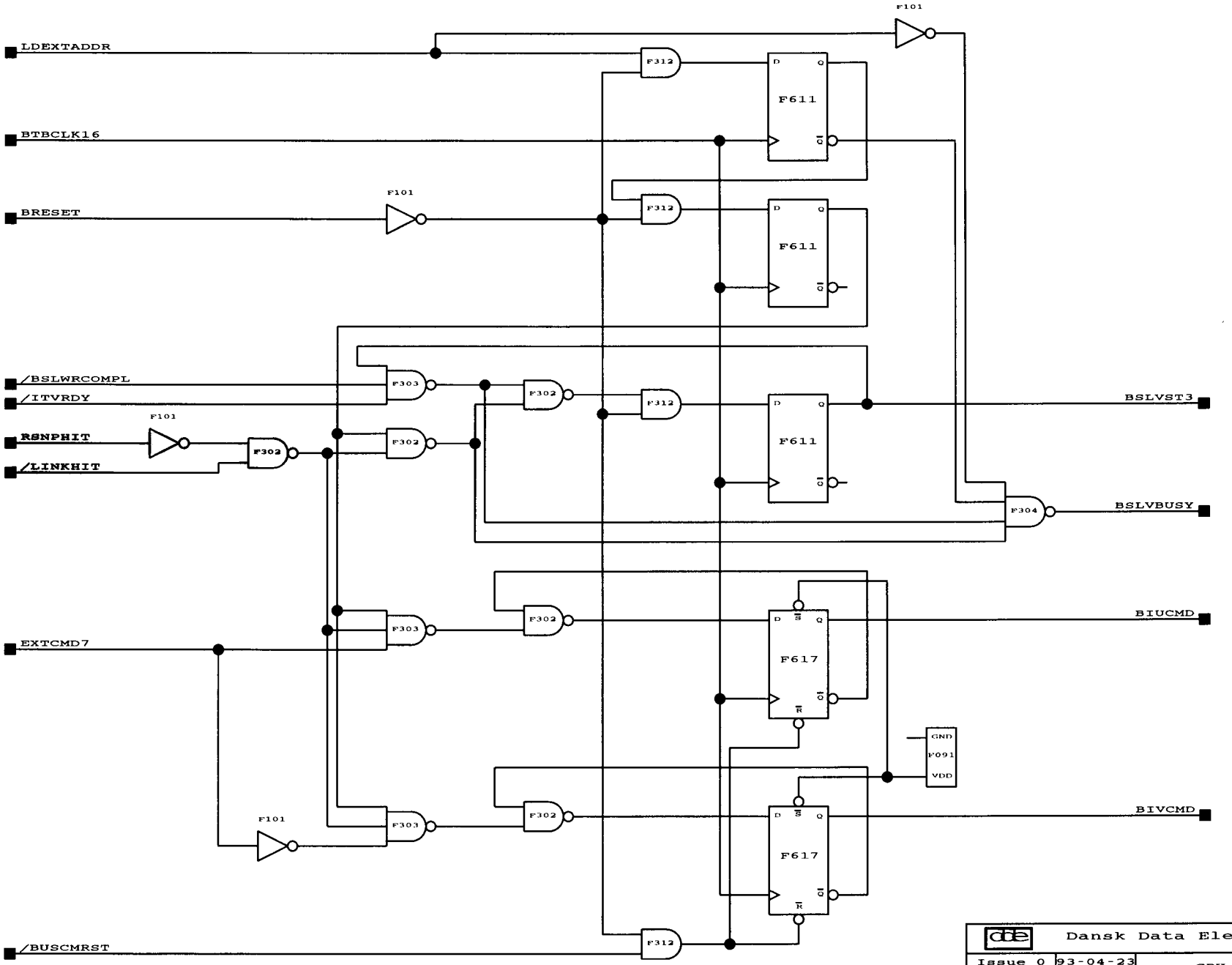
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302
Issue 1	94-07-11	I/U Address Comperator
Issue 2		
Issue 3		File: cpa.35 Page:35 of NN



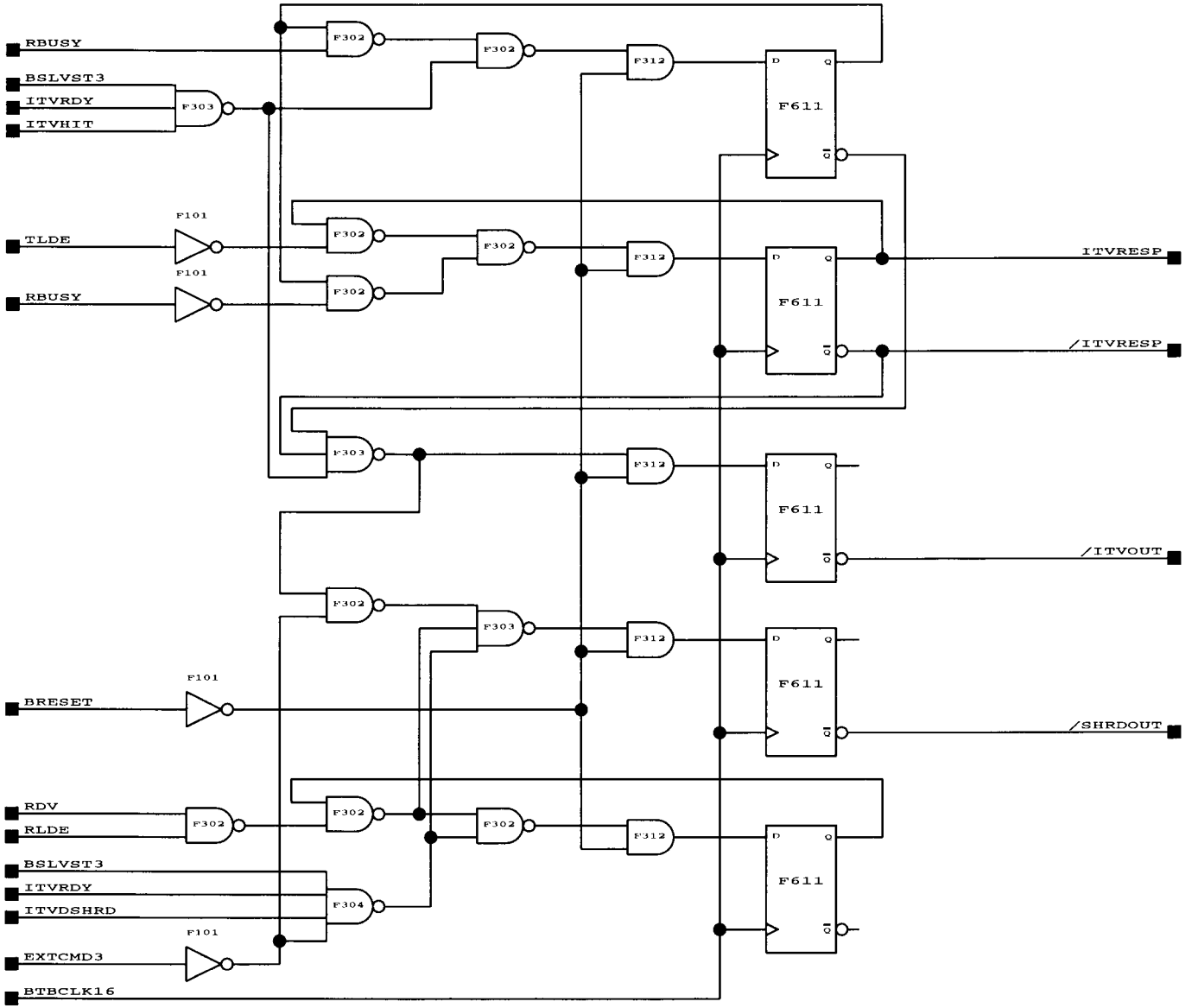
Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Slave Address Decoding
Issue 1		
Issue 2		
Issue 3		File: cpa.37 Page:37 of NN



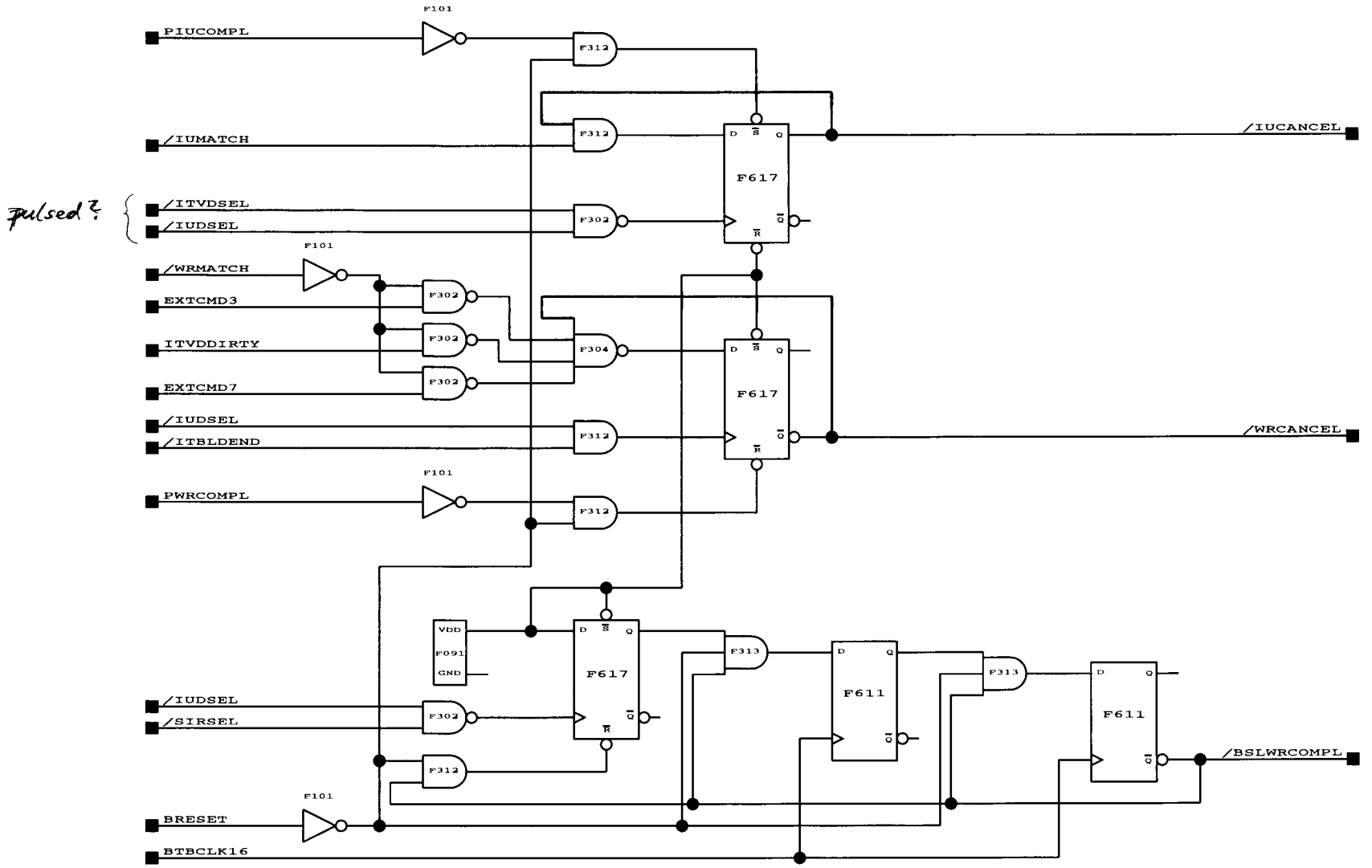
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302 System Bus Command Decoding	
Issue 1			
Issue 2			
Issue 3		File: cpa.38	Page:38 of NN



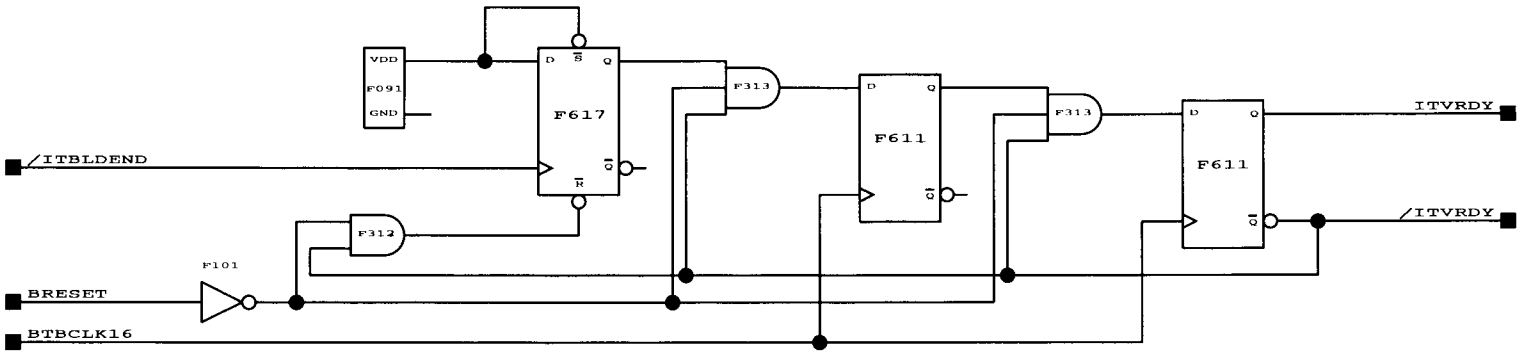
Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1	94-07-11	Bus Implicit Slave Control	
Issue 2			
Issue 3		File: cpa.39	Page:39 of NN



Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Bus Implicit Slave Control
Issue 1		
Issue 2		
Issue 3		File: cpa.40 — Page: 40 of NN



Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CPA Bus I/U Command Termination	
Issue 1	94-05-10		
Issue 2			
Issue 3		File: cpa.41	Page:41 of NN



dde	Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CA302 Bus Intervention Termination	
Issue 1			
Issue 2			
Issue 3		File: cpa.42	Page:42 of NN

AA3/94-05-11

CPU AGENT - CA301

PARITY CHECK AF CPU ADDR/DATA

Parity Check er disabled i flg. situationer, hvor der forekommer 'tomme' dataelementer.

1. NULL:
   - Addr check
   - Data —

2. INVALIDATE
   - Data check

3. INTERVENTION RESPONSE
   - Data check hvis cache state er:

*	0	Invalid	No check
*	1	Reserved	— —
*	2	—	— —
*	3	—	— —
*	4	Clean Exclusive	— —
	5	Dirty Exclusive	Check
*	6	Shared	No check
	7	Dirty Shared	Check

Parity check enabled:

Read	addr
Write block	addr + data
Invalidate	addr
Update	addr

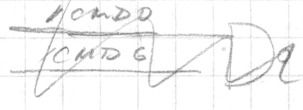
Intervention Response - data with dirty status.

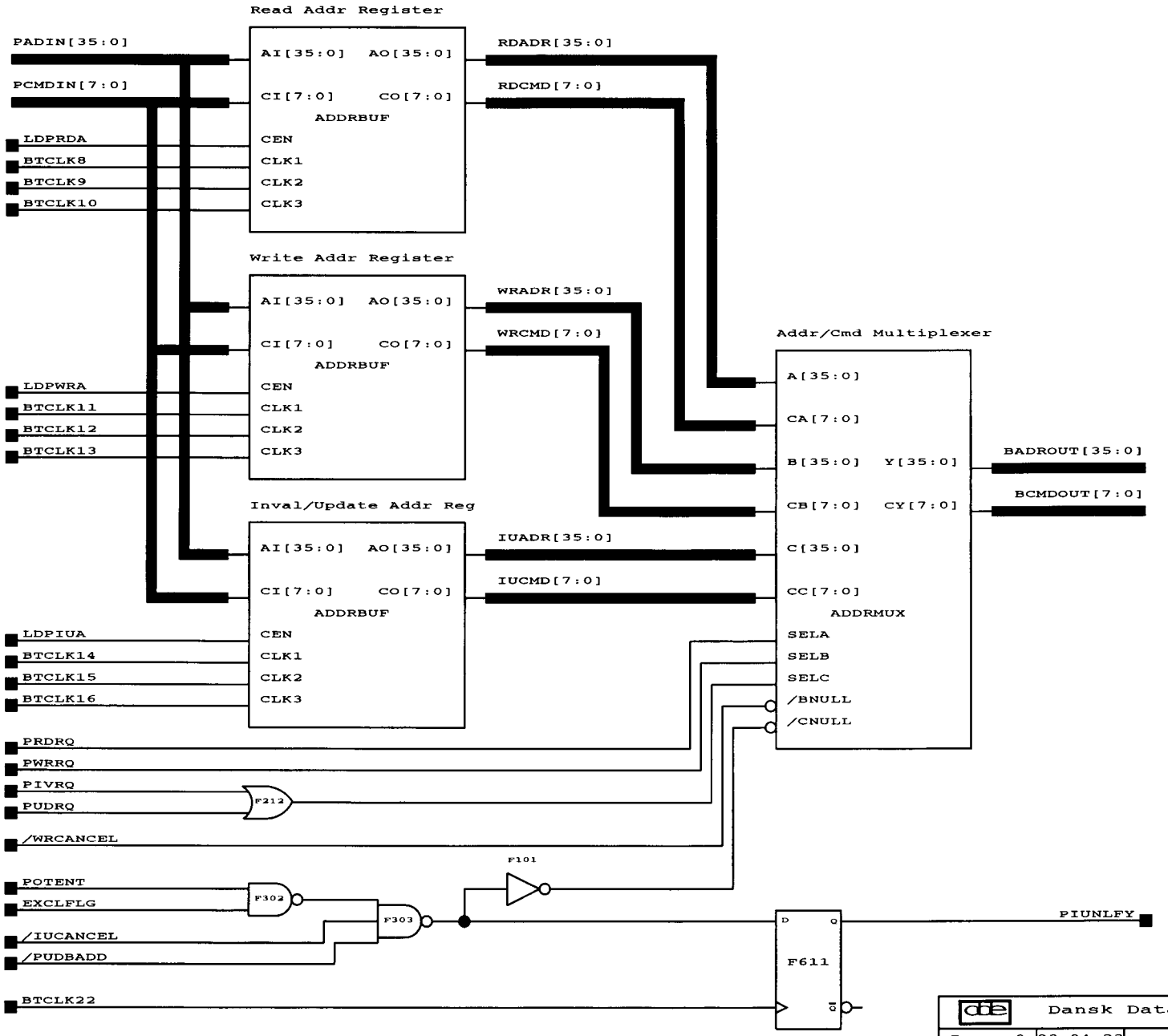
PROCESSOR PARITY CHECK

8	7	6	5	4	3	2	1	0	
0	0	0	x	x	x	x	x		Read
0	0	1	x	x	x	x	x		Read
0	0	1	0	1	0	x	x		Write block
1	x	1							

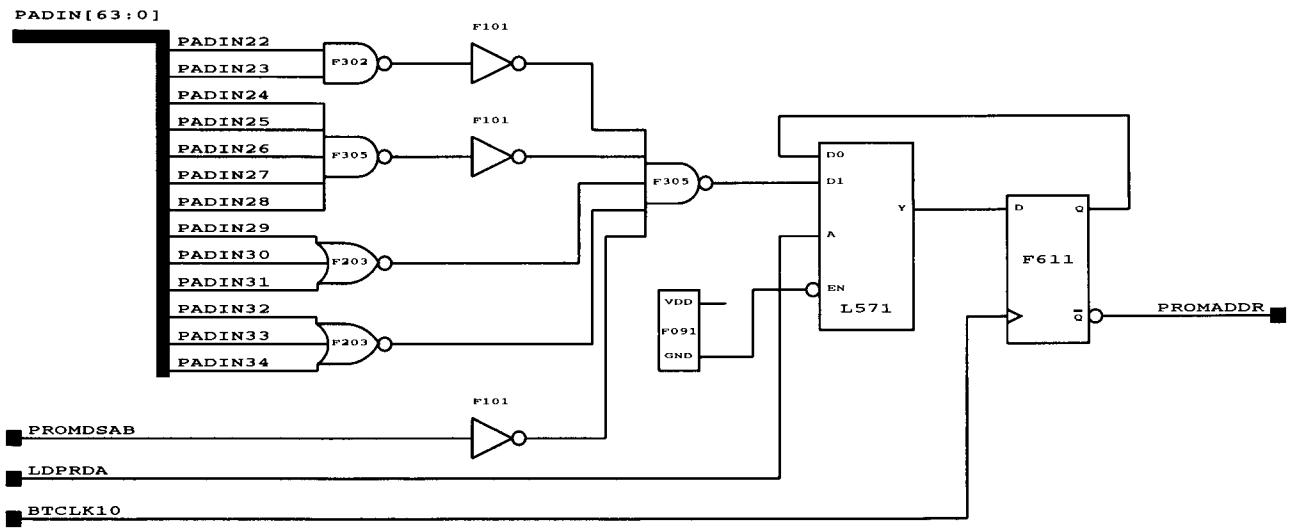
Disable Parity Check

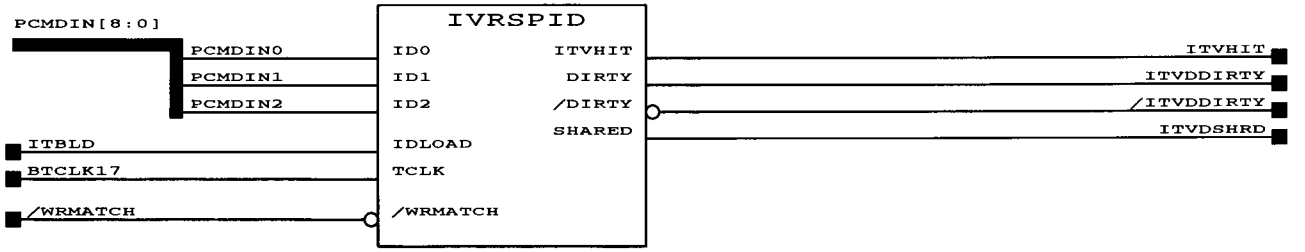
8	7	6	5	4	3	2	1	0	
0	0	1	1	x	x	x	x	x	Null - disable addr check
0	1	0	0	x	x	x	x	x	Inv. - disable data check
(1	x	0	x	x	x	1	x	1	Resp. data - enable data check)
1	x	0	x	x	x	0	x	x	Resp data - disable check.
1	x	0	x	x	x	x	x	0	Resp. data. - - —



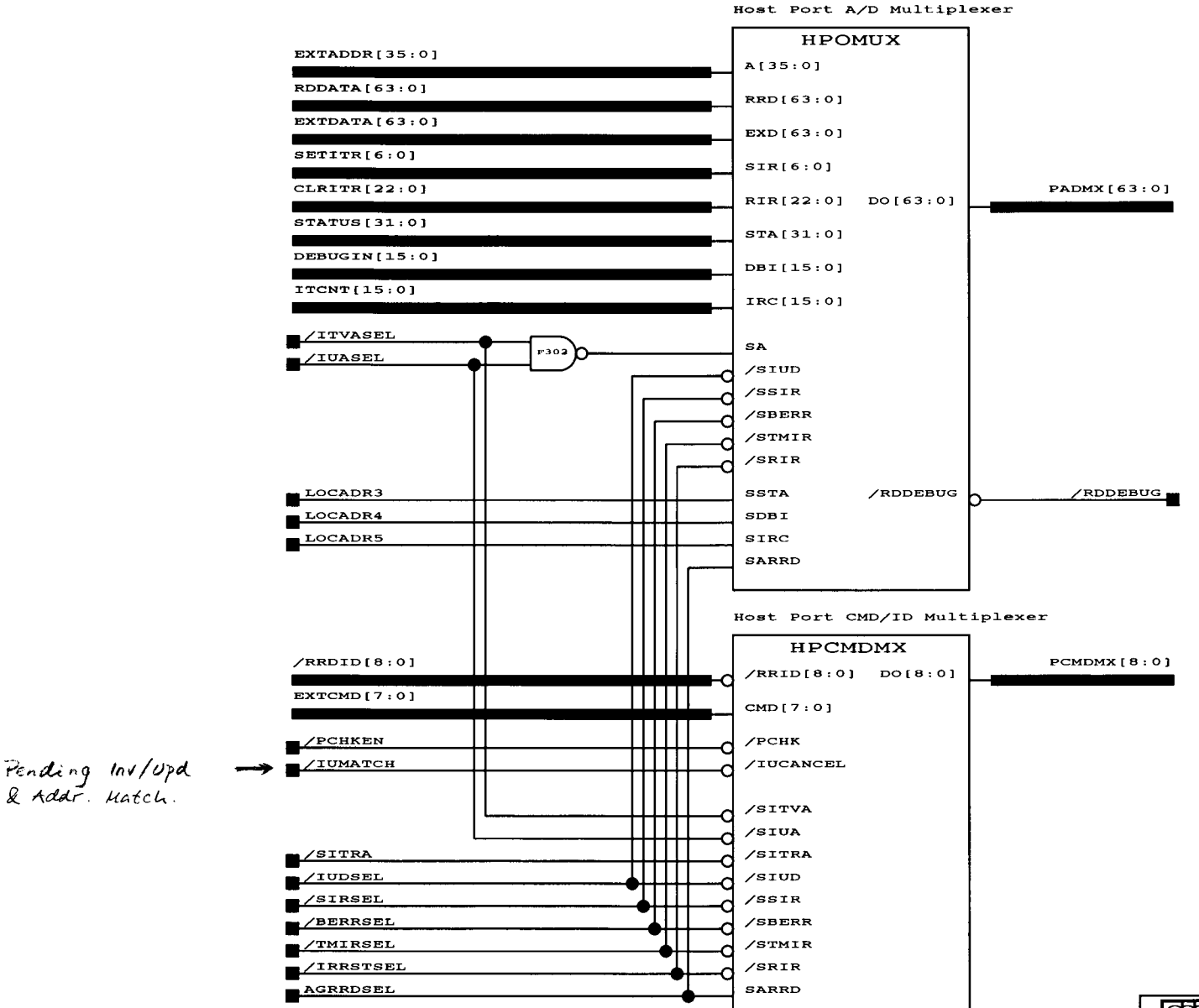


Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CPA Output Address Registers and Address Multiplexer
Issue 1		
Issue 2		
Issue 3		File: cpa.11 Page:11 of

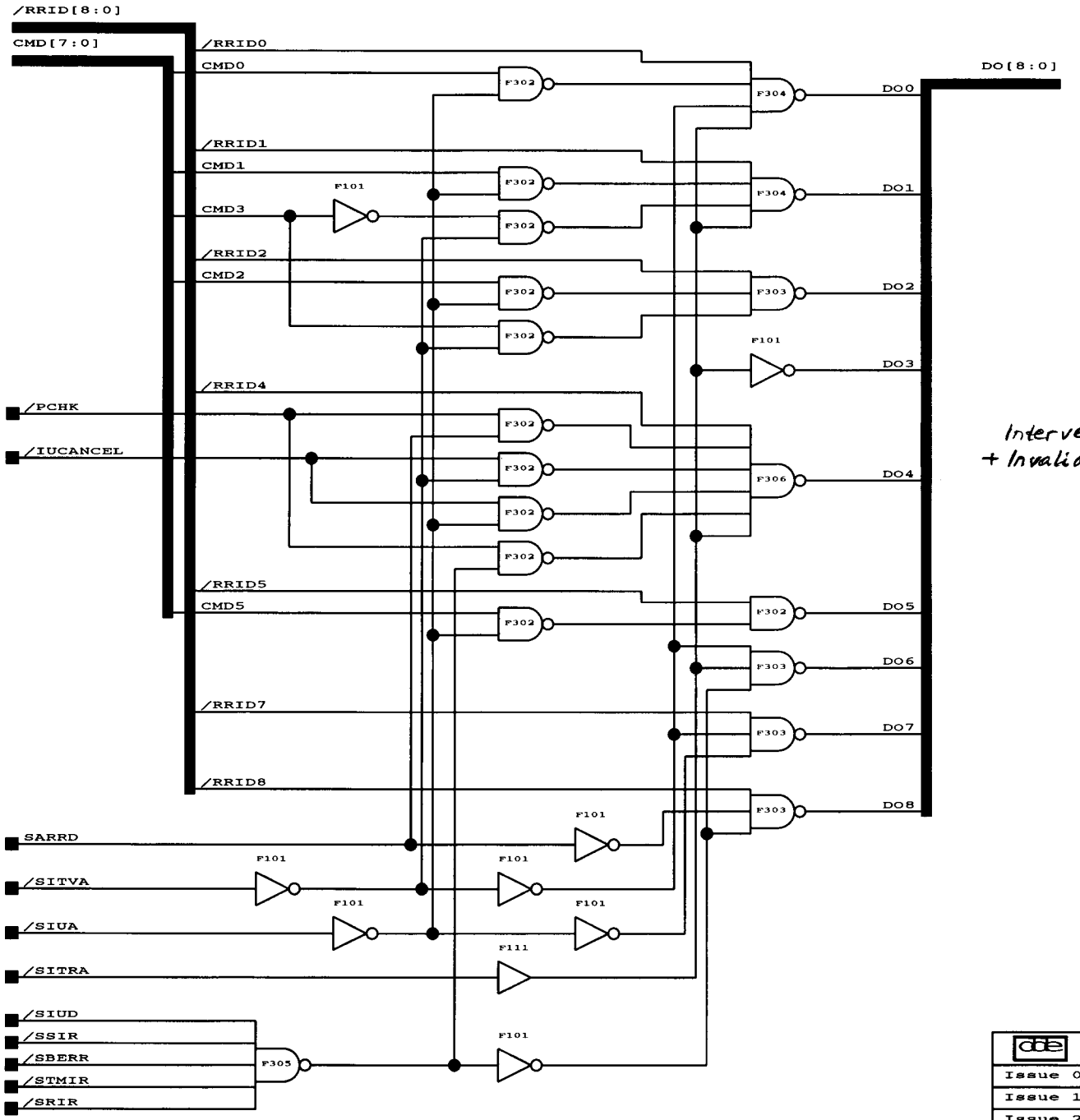




Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CPA PROM Addr Decoding Intervention Data ID
Issue 1		
Issue 2		
Issue 3		File: cpa.13 Page:13 of NN

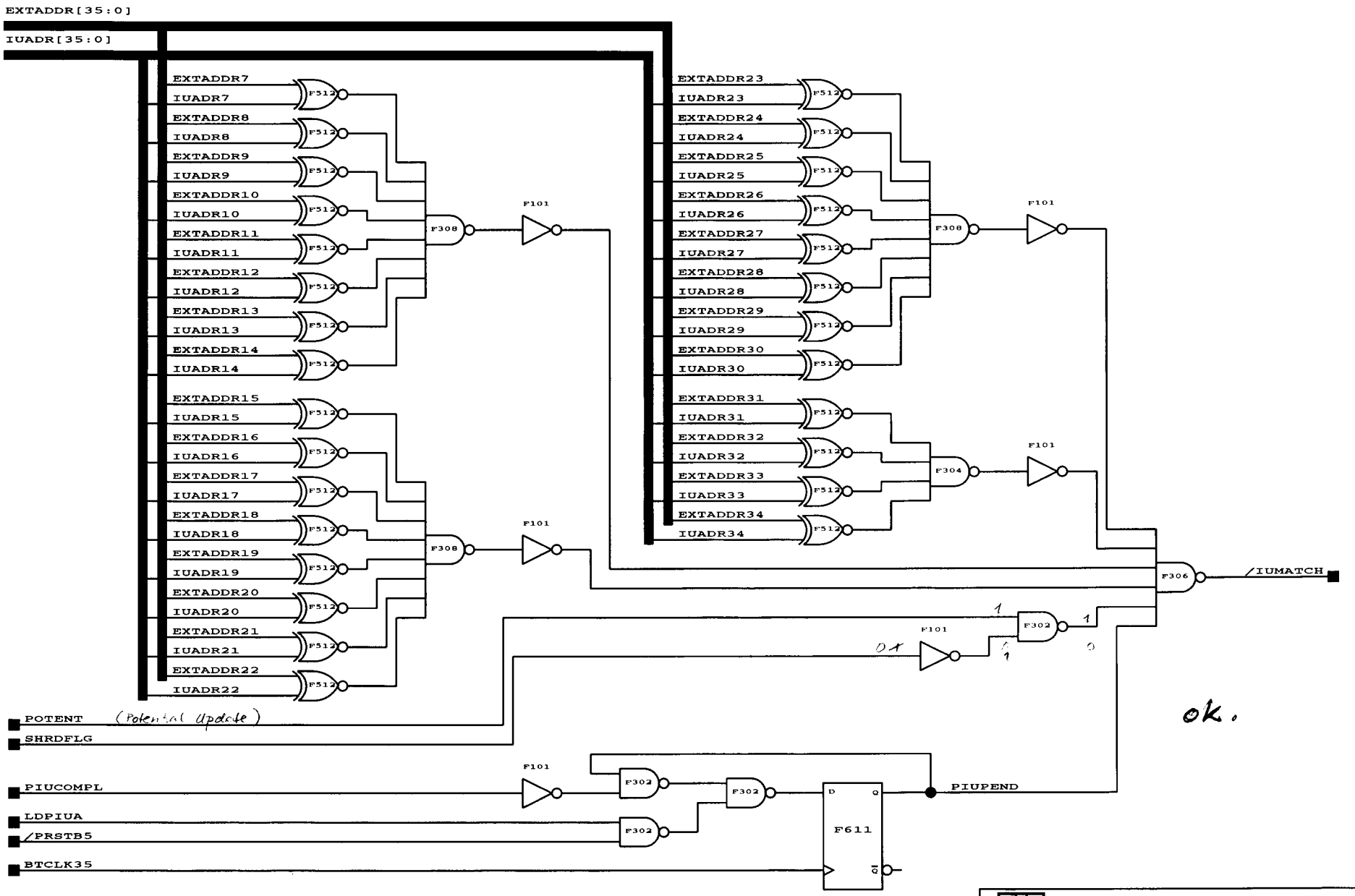


Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CPA Host Port Multiplexer
Issue 1		
Issue 2		
Issue 3		File: cpa.20 Page:20 of NN



Intervention & /IUCANCEL
+ Invalidate/Update & /IUCANCEL

Dansk Data Elektronik A/S		
Issue 0	93-04-23	CPU AGENT - CPA Host Port Command Mux
Issue 1		
Issue 2		
Issue 3		File: HPCMOMX.1 Page:1 of 1



ok.

POTENT clearas, når Update Cmd termineres.

SHRDFLG angiver at den forudgående Read har fået data retur med SHARED status.

Dansk Data Elektronik A/S			
Issue 0	93-04-23	CPU AGENT - CPA Address Comperators	
Issue 1			
Issue 2			
Issue 3		File: cpa.35	Page:35 of NN