

CPU300-303 Design document

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1 REVISION HISTORY

Changes from version 1.1 to 1.2:

The document now defines CPU300-303 as follows:

CPU300: 1 MB snoop. Global bus only.
CPU301: 1 MB snoop.
CPU302: 4 MB snoop. Global bus only.
CPU303: 4 MB snoop.

An old reference to the local TTL interface has been removed.

Changes from version 1.0 to 1.1:

The reference list has been updated.

The LED labels have been changed.

Version 1.0:

Although this is the initial version of the document it is based on the MCU301 Design document from which it differs in the following respects:

The local bus has been changed to all BTL, thus the global and local bus are symmetrical.

All processor modules on a base module must have the same secondary cache size, thus reducing the number of sets of snoop address jumpers from two to one.

The CPU301 and CPU302 support 1-MB and 4-MB secondary cache, respectively, thus the above set of jumpers is fixed for each module.

The boot PROM is a flash EEPROM for re-use.

2 REFERENCES

1. MCU301/302/304 Kravspecifikation
1-0101
2. SPC/3 System bus specification
1-0201
3. MIPS R4000 Microprocessor User's Manual
Integrated Device Technology, Inc.
Part number M8-00040
4. MIPS R4000 Microprocessor User's Manual Errata
Revision 2.0
March 13, 1992
MIPS Technology Products Group
5. CPU Agent Design document
1-0203

3 INTRODUCTION

The CPU module for the SPC/3 computer series consists of a base module CPU300-303 and one to four detachable processor modules, e.g. PMD301 with a 75-MHz R4400MC and 1-MB secondary cache. The base modules, which each take up one backplane position, are defined as follows:

CPU300: 1 MB snooper. Global bus only.
CPU301: 1 MB snooper.
CPU302: 4 MB snooper. Global bus only.
CPU303: 4 MB snooper.

Each of the up to four processors modules connects to a global and a local bus interface through two agents. These identical agents, which are implemented with highly complex gate arrays, provide data buffers, address registers, and control for the commands that originate in the associated processor and for those commands on the associated bus that require cache coherency.

Both the global and local bus interface are BTL.

There is a global control space, which contains the following special registers intended for identification, control, error logging, interrupt, and debugging.

- Status register
- Control register
- Module ID
- Module FCN
- Interrupt register
- Debug register
- Processor module identification register
- Bus error register

There is a control, interrupt, and debug register for each subposition corresponding to each possible processor module. The global control space may be accessed both via the global bus and by the four processors although a processor must not write to the interrupt register of its own subposition.

The local control space, although structured in the same way, only contains interrupt registers.

In addition to the control spaces there are separate address spaces for the internal registers of each agent, these may only be accessed by the associated processor.

The module is equipped with a 1/2-MB detachable boot flash EEPROM, which is common to all processors.

Finally, the choice of little or big endians is made by a fixed signal on the bus.

4 SPECIFICATIONS

4.1 Performance

Bus frequency	33.3 MHz
Bus burst rate	267 MB/s
Bus read rate (32 words)	178 MB/s
Bus write rate (32 words)	213 MB/s

4.2 Secondary cache requirements

Block size	32 words
Cache size, CPU300-301	1 MB
Cache size, CPU302-303	4 MB

4.3 Interfaces

System bus interface:

SPC/3 system bus [2], both global and local bus.

Indicators on front panel:

PARITY ERROR	Red LED that indicates a parity error on the global or local bus.
ERROR(0-3)	One red programmable LED per processor.
BUSY(0-3)	One green programmable LED per processor.
A(0-3)	One green programmable LED per processor.
B(0-3)	One green programmable LED per processor.

Internal processor/base module interface:

SAD(63:0)	System interface address/data
SADP(7:0)	System interface address/data parity
SCMD(8:0)	System interface command
SCMDP	System interface command parity
/VALIN	System interface valid to processor
/VALOUT	System interface valid from processor
/EXTRQ	System interface request from agents
/RELEASE	System interface release from processor
/RDRDY	Read ready
/WRRDY	Write ready
/IVDACK	Invalidate acknowledge
/IVDERR	Invalidate error
RCLK(1:0)	Receive clocks (identical)
TCLK(1:0)	Transmit clocks (identical)
/INT	Error interrupt
/NMI	Non-maskable interrupt

SRE	Selective reset
C2MS	2-ms period clock
C262MS	262-ms period clock
PM_ID(3:0)	Processor module identification
/PRESENT	Processor module present
BIG	Big endian

4.4 Dimensions

Board height	415.0 mm
Board depth	335.0 mm
Module pitch	30.0 mm

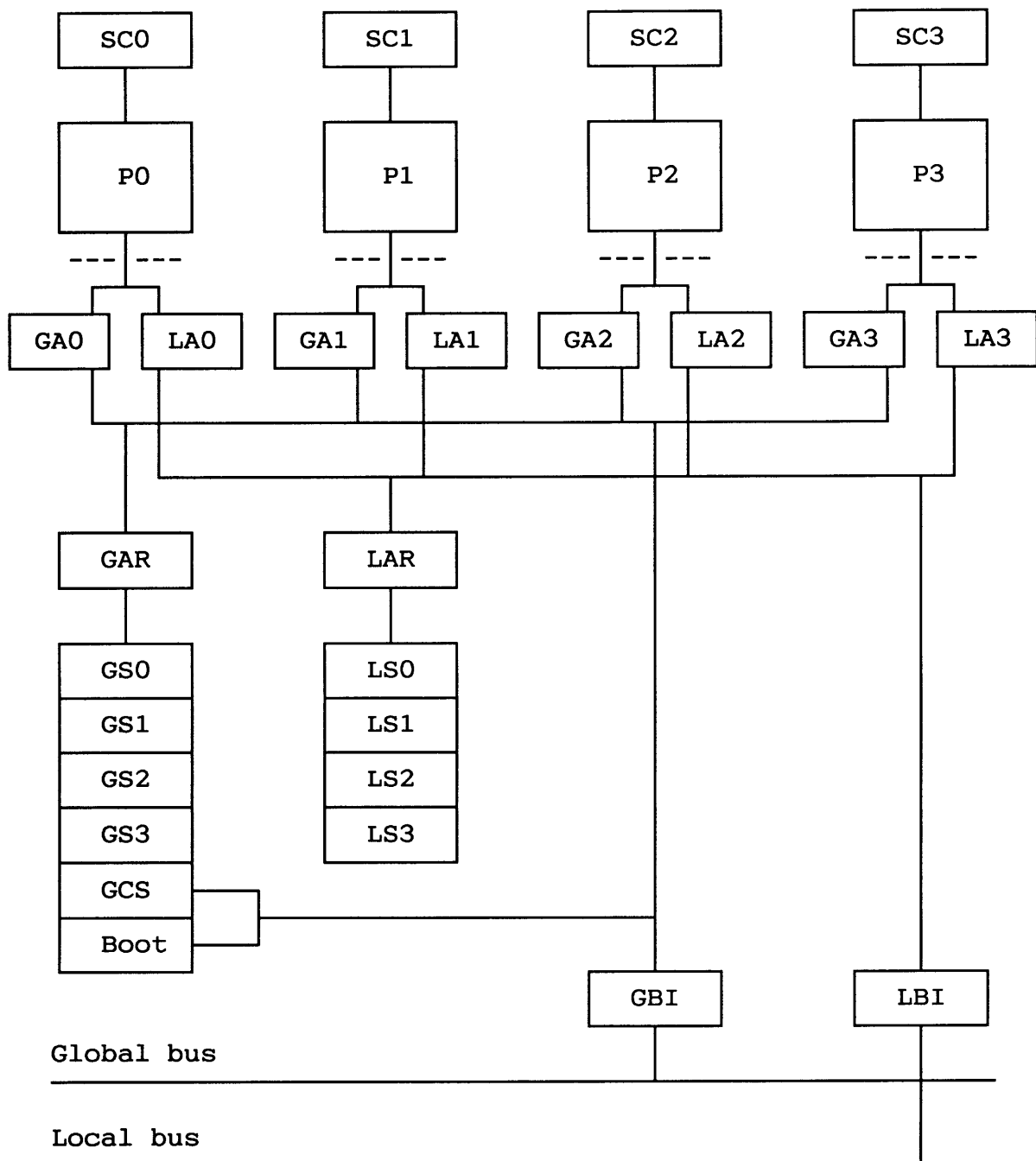
4.5 Power

Voltage	5 V \pm 5 %
Current (CPU300/302)	5 A max.
Current (CPU301/303)	9 A max.

5 Functional description

The block diagram below shows the base module CPU300-303 below the connector interface (---) and four processor modules above.

Each processor module consists of a processor (P) with a secondary cache (SC) and a connector. Associated with each possible processing module, but placed on the base module are a global and a local agent (GA and LA), and a global and a local snooper (GS and LS). In addition, the base module provides a global and a local bus interface (GBI and LBI) with associated address registers (GAR and LAR), a global control spaces (GCS), and finally a boot PROM. A part of the global control space and all of the local control space are inside the respective agents.



5.1 Base module

The main components of the base module are eight agents, two bus interfaces, two address registers, eight snoopers, a global control space, and a boot PROM.

The agent is described in [5] and contains all data buffers, data and address registers, and control required to link a processor to a bus interface. An agent also contains an agent space, which is only accessible from the associated processor, and an interrupt register and a debug register, which are a part of the respective control spaces.

One of the important tasks of the agent is to sequence transactions from the processor and system bus correctly when they pertain the same cache line. Another is to ensure continued snooping on a retained link address, when the link is evicted from the secondary cache and retained by the processor, whereby the link address is evicted from the snooper and therefore must be retained in the agent.

Each bus interface contains a number of registered BTL transceivers and a bus master control including arbitration control.

The task of a snooper is to keep a copy of the physical address tags of the secondary cache tags such that bus snooping can take place without disturbing the respective processor excessively. The format of the snooper depends on the size and block size of the secondary cache:

1-MB: 35 20 19
4-MB: 35 22 21

Tag	Index	Offset
-----	-------	--------

8-word: 5 4 0
16-word: 6 5 0
32-word: 7 6 0

The index gives the entry in the snooper, and, in order for a snoop hit to occur, the tag must match the corresponding bits of the bus address. The offset does not participate in the comparison, and there is no valid bit. The contents of the snoopers are undefined upon reset.

The format of the snoopers, which must correspond to the associated secondary caches, is selected with fixed jumpers given a limit of 15 index bits corresponding to a maximum set size of 32768 entries. Surplus tag bits need not be excluded as they merely become redundant. The CPU300-301 modules are set for 1-MB / 32-word, while the CPU302-303 modules are set for 4-MB / 32-word.

When a cache line is replaced the read and the write are normally bundled together in a command called read with write forthcoming. In this case the write address tag will disappear from the snooper before disappearing from the secondary cache as it is overwritten in the snooper by that of the read, thus creating the possibility of non-coherency. Rather than try do juggle with both tags, the snooper must force hit until the start of the next command from the agent, which is a late but safe indication that the write address tag no longer is present in the secondary cache.

In addition to each snooper, which already does a good job of filtering coherency requests to the processor, there is an extension dubbed the supersnooper, which to the extent possible tracks the state changes in the secondary cache and prevents non-exclusive coherent read requests from reaching the processor if the state is shared or invalid. The contents of the supersnoopers are undefined upon reset.

The global control space contains a number of special registers as mentioned in the introduction. The control for the control space includes an address comparator that can detect a control space access to this module and a simple state machine that can perform the required access. The module FCN PROM is mounted in a socket to allow easy replacement.

There is a 1/2-MB boot PROM providing reset, diagnostic, and debugging code. The boot PROM is located at the beginning of the address range 0x01FC0000 through 0x01FFFFFF, where the former is the physical reset address of the processor. This address range is, alas, right in the memory space. Thus, when a read address falls in this range and the boot PROM is not mapped out, as controlled by a bit in the control register of the global agent, the boot PROM must intervene and supply the data as a cache slave thus pre-empting the memory slave. The boot PROM, which is implemented with a 512 K by 8-bit flash EEPROM, is mounted in a socket.

When a master issues an access with an address for which there is no matching slave a missing target acknowledge will result. This works fine for a write, but for a read the responsible processor would wait forever on the missing 'last data element' because the agent does not provide it instead. Therefore, a dummy block generator is implemented in each bus interface to take care of this case.

6 PROGRAMMING INFORMATION

6.1 Processor

Programming information for the processor can be found in [3, 4].

The physical address space as seen from a processor consists of a global and local space, each subdivided into a memory, agent, and control space. A processor can only access its own agent spaces, while the memory and control spaces are accessible by all processors on the bus in question. The global and local control address spaces are described below. All address formats are shown in [2].

The interrupt register of the processor, whose format is shown below, contains a non-maskable interrupt (NMI), four general interrupts (I5-I2), a timer interrupt (TIM), and an error interrupt (ERR).

NMI	I5	I4	I3	I2	TIM	ERR
6	5	4	3	2	1	0

These bits result from the OR'ing of the respective bits in the two agents, and, in case of bit 0, also from the OR'ing of the bits in the Bus error register, more specifically the global and local bus parity error interrupts, and the debug interrupt. Only the timer in the global agent is active.

All interrupts are level-sensitive, thus the processor must remove an interrupt when it is accepted, but in order to do so the source of the interrupt must be known. This is a problem for the general interrupts unless each in software is assigned to only one agent, thus the use of local interrupts is discouraged.

Accesses to the address space 0x01FC0000 through 0x01FFFFFF may, under control of a bit in the control register of the appropriate global agent, be directed at either memory or the 1/2-MB boot PROM, which is located at the start of the address space and contains reset, diagnostic, and debugging code.

The selection of little or big endians is determined by a fixed signal on the system bus.

The states of the snoopers and supersnoopers are, like those of the secondary caches, undefined upon reset.

6.2 Agent space

For a description of the agent address space, please, refer to [5].

There are four programmable LEDs labelled ERROR(0-3), BUSY(0-3), A(0-3), and B(0-3) on the front panel for each of the four possible processor modules. They are controlled by the associated global agent control register bit 6 and 7, and local agent control register bit 6 and 7, respectively.

6.3 Control space

The CPU module has a global and a local control space, which are both divided into subpositions and contain a number of special registers intended for identification, configuration, error logging, interrupt, and debug. These registers have varying bit widths, but are all right justified within double words (64 bits), and any access less than a double word must take into account the subtle differences between little and big endians.

The global control space comprises all of the following special registers, while the local control space only comprises the interrupt register. Below is for every register or group of registers listed whether it can be read, written, or cleared along with its hexadecimal byte offset relative to the start of the control address space of the module.

Register	Access	Offset
Status register	Read/clear	0
Control register	Write	100
Module ID	Read	200
Module FCN	Read	300
Interrupt register	Write	400
Debug register	Write	500
Processor module register	Read	600
Bus error register	Read/clear	700

The function and format of the individual registers are described in the following. Reserved bits (r) must be 0 when written, and are undefined when read. Bits 16 through 63 are reserved, unless otherwise noted.

6.4 Status register

The Status register indicates bus parity errors found by this module. Individual bits may be cleared by writing ones in the respective positions, and the bits are all cleared by bus reset.

r	r	r	r	r	r	r	r	r	r	r	r	r	r	LPE	GPE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

GPE: Global parity error.

LPE: Local parity error.

6.5 Control register

There is a Control register for every subposition, and each contains a bit for selective reset of the corresponding processor. The bits are all set by bus reset.

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	SRE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SRE: Selective reset.

6.6 Module ID

The Module ID consists of a 32-byte string stored in 32 consecutive double words. The byte offset given earlier applies to the first double word.

r	r	r	r	r	r	r	r	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ID(7:0): Single byte of module
 Identification string.

The format of the string is given in [2].

6.7 Module FCN

The Module FCN consists of a 32-byte string stored in 32 consecutive double words. The byte offset given earlier applies to the first double word.

r	r	r	r	r	r	r	r	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FCN(7:0): Single byte of module
 Field Change Notice string.

The format of the string is given in [2].

6.8 Interrupt register

The Interrupt register, which is 32 bits wide, is used to write interrupts. There is an Interrupt register for every subposition in both the global and the local control space, and it is not possible for a master to write to its own register.

P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
r	r	r	r	r	r	r	r	r	r	NMI	I5	I4	I3	I2	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

I(5:2): Interrupts.
 Provides a direct path to the
 corresponding bits of the
 Interrupt register of the

processor.

NMI: Non-maskable interrupt.
 Provides a direct path to the NMI bit of the Interrupt register of the processor.

P(15:0): Peripheral interrupts.
 New bits are OR'ed to old ones, and the bits may be cleared by the processor.

6.9 Debug register

The Debug register is used to write a double byte to a processor during debug. There is a Debug register for every subposition, and it is not possible for a master to write to its own register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

D(15:0): Debug data.

6.10 Processor module register

The Processor module register indicates the presence and identity of each processor module.

M33	M32	M31	M30	M23	M22	M21	M20	M13	M12	M11	M10	M03	M02	M01	M00
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Mi(3:0): Identity of module i.

No module is present in position i if Mi=15.

6.11 Bus error register

There is a Bus error register for every subposition, and each indicates interrupts caused by a bus parity error or a debug request. Individual bits may be cleared by writing ones in the respective positions, and the bits are all cleared by bus reset.

r	r	r	r	r	r	r	r	r	r	r	r	r	DBI	LPI	GPI
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

GPI: Global parity error interrupt.

LPI: Local parity error interrupt.

DBI: Debug interrupt.

CPU300-303 Diagrams

CPU300: 1 MB snooper. Only global bus components mounted.
CPU301: 1 MB snooper.
CPU302: 4 MB snooper. Only global bus components mounted.
CPU303: 4 MB snooper.

Processor/agent interface

- 1 Connectors 0
- 2 Global agent 0
- 3 Local agent 0
- 4 Connectors 1
- 5 Global agent 1
- 6 Local agent 1
- 7 Connectors 2
- 8 Global agent 2
- 9 Local agent 2
- 10 Connectors 3
- 11 Global agent 3
- 12 Local agent 3
- 13 Programmable LEDs
- 14 Reset counters
- 15 Gating towards processors
- 16 Gating towards system bus

Bus control

- 17 Global and local output enable control
- 18 Pull-down for address and data valid
- 19 Global and local bus request decoder
- 20 Global bus arbitration
- 21 Local bus arbitration

Snooper control

- 22 Global snooper control
- 23 Global super snooper 0-1
- 24 Global super snooper 2-3
- 25 Local snooper control
- 26 Local super snooper 0-1
- 27 Local super snooper 2-3

Address and command registers and snoopers

- 28 Global and local command register
- 29 Global address register
- 30 Global snooper 0
- 31 Global snooper 1
- 32 Global snooper 2
- 33 Global snooper 3
- 34 Local address register
- 35 Local snooper 0
- 36 Local snooper 1
- 37 Local snooper 2
- 38 Local snooper 3

Global control space, boot, and dummy block generator

- 39 Global control space decode
- 40 Global control space control
- 41 Module ID and FCN PROMs
- 42 Processor module ID register
- 43 Global control space transceiver
- 44 Boot control

- 45 Boot PROM
- 46 Boot register
- 47 Global dummy block generator
- 48 Global data identifier output register

Local control space and dummy block generator

- 49 Local control space decode and target acknowledge
- 50 Local dummy block generator
- 51 Local dummy data
- 52 Local data identifier output register

Clock

- 53 Clock distribution

Bus interface

- 54 Global address/data transceiver
- 55 Global address/data transceiver
- 56 Global command and valid transceiver
- 57 Global bus request transceiver
- 58 Global control transceiver
- 59 Local address/data transceiver
- 60 Local address/data transceiver
- 61 Local command and valid transceiver
- 62 Local bus request transceiver
- 63 Local control transceiver
- 64 Connector (row 1-25)
- 65 Connector (row 26-50)
- 66 Connector (row 51-75)
- 67 Connector (row 76-100)

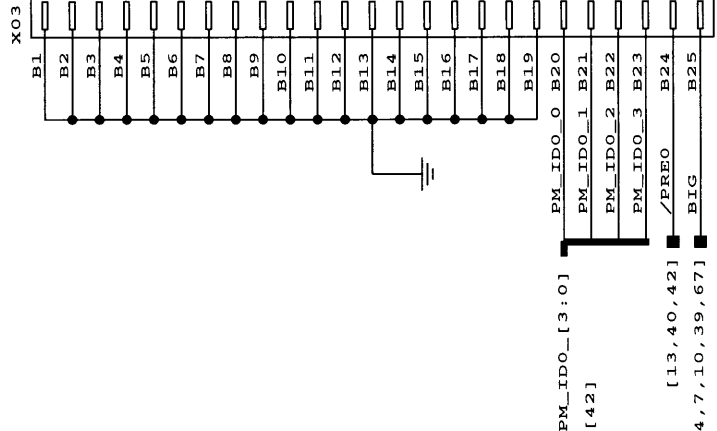
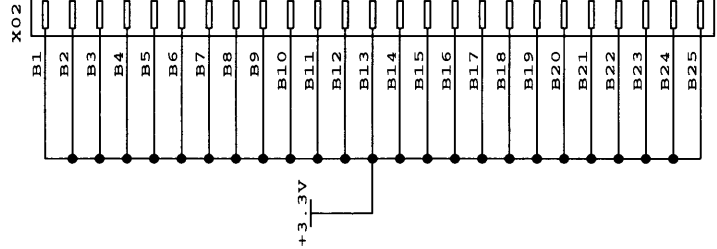
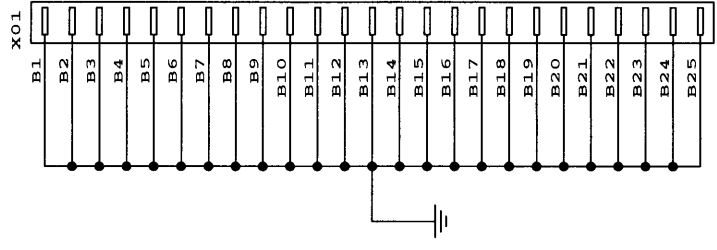
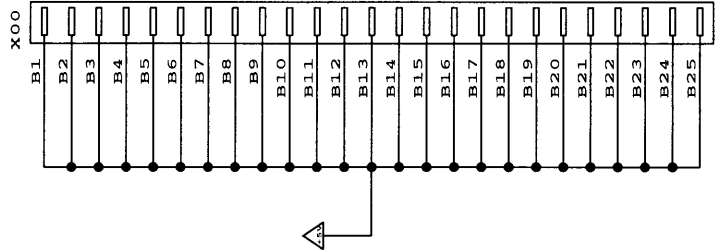
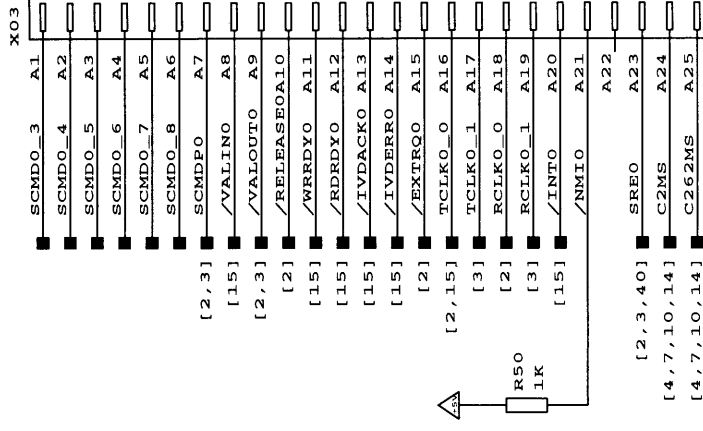
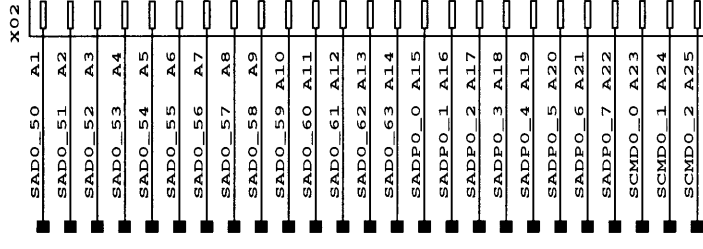
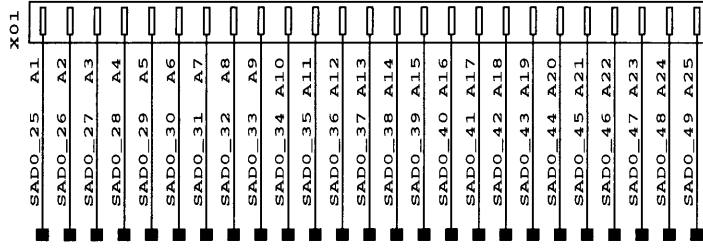
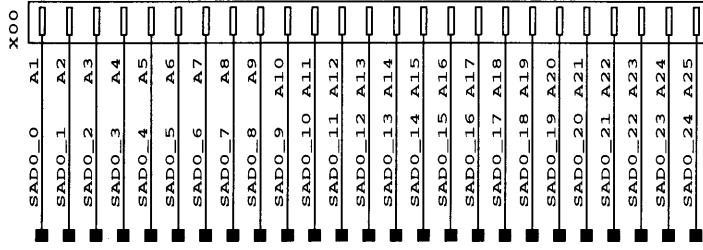
Termination and decoupling

- 68 Internal global bus termination
- 69 Internal local bus termination
- 70 Decoupling capacitors
- 71 Decoupling capacitors
- 72 Decoupling capacitors

Fix of bad agent

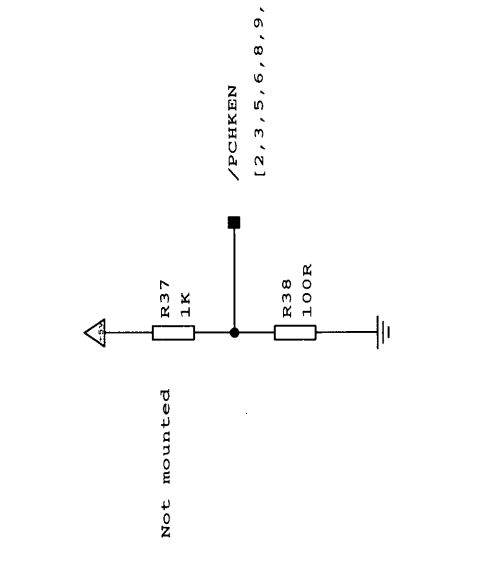
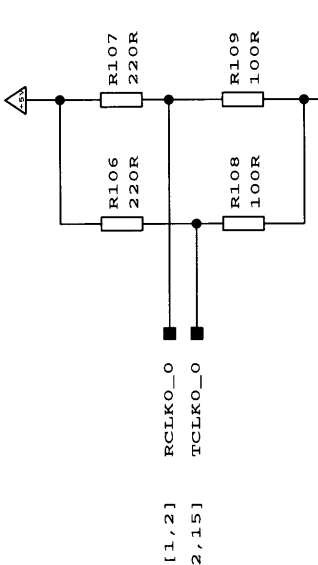
- 73 Controlled intervention for bad CA302

(Page 73 only present for CPU30x-1)



SADO_0	52	BAD0	89	AD_R0
SADO_1	53	BAD1	90	AD_R1
SADO_2	54	BAD2	91	AD_R2
SADO_3	55	BAD3	92	AD_R3
SADO_4	56	BAD4	93	AD_R4
SADO_5	57	BAD5	94	AD_R5
SADO_6	58	BAD6	95	AD_R6
SADO_7	59	BAD7	96	AD_R7
SADO_8	60	BAD8	97	AD_R8
SADO_9	61	BAD9	98	AD_R9
SADO_10	62	BAD10	99	AD_R10
SADO_11	63	BAD11		AD_R11
SADO_12	64	BAD12		AD_R12
SADO_13	65	BAD13		AD_R13
SADO_14	66	BAD14		AD_R14
SADO_15	67	BAD15		AD_R15
SADO_16	68	BAD16		AD_R16
SADO_17	69	BAD17		AD_R17
SADO_18	70	BAD18		AD_R18
SADO_19	71	BAD19		AD_R19
SADO_20	72	BAD20		AD_R20
SADO_21	73	BAD21		AD_R21
SADO_22	74	BAD22		AD_R22
SADO_23	75	BAD23		AD_R23
SADO_24	76	BAD24		AD_R24
SADO_25	77	BAD25		AD_R25
SADO_26	78	BAD26		AD_R26
SADO_27	79	BAD27		AD_R27
SADO_28	80	BAD28		AD_R28
SADO_29	81	BAD29		AD_R29
SADO_30	82	BAD30		AD_R30
SADO_31	83	BAD31		AD_R31
SADO_32	84	BAD32		AD_R32
SADO_33	85	BAD33		AD_R33
SADO_34	86	BAD34		AD_R34
SADO_35	87	BAD35		AD_R35
SADO_36	88	BAD36		AD_R36
SADO_37	89	BAD37		AD_R37
SADO_38	90	BAD38		AD_R38
SADO_39	91	BAD39		AD_R39
SADO_40	92	BAD40		AD_R40
SADO_41	93	BAD41		AD_R41
SADO_42	94	BAD42		AD_R42
SADO_43	95	BAD43		AD_R43
SADO_44	96	BAD44		AD_R44
SADO_45	97	BAD45		AD_R45
SADO_46	98	BAD46		AD_R46
SADO_47	99	BAD47		AD_R47
SADO_48		BAD48		AD_R48
SADO_49		BAD49		AD_R49
SADO_50		BAD50		AD_R50
SADO_51		BAD51		AD_R51
SADO_52		BAD52		AD_R52
SADO_53		BAD53		AD_R53
SADO_54		BAD54		AD_R54
SADO_55		BAD55		AD_R55
SADO_56		BAD56		AD_R56
SADO_57		BAD57		AD_R57
SADO_58		BAD58		AD_R58
SADO_59		BAD59		AD_R59
SADO_60		BAD60		AD_R60
SADO_61		BAD61		AD_R61
SADO_62		BAD62		AD_R62
SADO_63		BAD63		AD_R63

SCMDP0	172	BCMD7	9	ADP_R7
SCMDP0_0	173	BCMD0	8	CMD_R0
SCMDP0_1	174	BCMD1	7	CMD_R1
SCMDP0_2	175	BCMD2	6	CMD_R2
SCMDP0_3	176	BCMD3	5	CMD_R3
SCMDP0_4	177	BCMD4	4	CMD_R4
SCMDP0_5	178	BCMD5	3	CMD_R5
SCMDP0_6	179	BCMD6	2	CMD_R6
SCMDP0_7	180	BCMD7	1	CMD_R7
SCMDP0_8	181	BCMD0	239	CMDP_R
SCMDP0_9	182	BCMD1	238	AVIN
SCMDP0_10	183	BCMD2	237	AVOUT
SCMDP0_11	184	BCMD3	236	DVAVIN
SCMDP0_12	185	BCMD4	235	DVAVOUT
SCMDP0_13	186	BCMD5	234	BUSYIN
SCMDP0_14	187	BCMD6	233	BUSYOUT
SCMDP0_15	188	BCMD7	232	SHRDIIN
SCMDP0_16	189	BCMD0	231	SHRDIOUT
SCMDP0_17	190	BCMD1	230	INTVIN
SCMDP0_18	191	BCMD2	229	INTVOUT
SCMDP0_19	192	BCMD3	228	ERRIN
SCMDP0_20	193	BCMD4	227	ERROUT
SCMDP0_21	194	BCMD5	226	SNPHIT
SCMDP0_22	195	BCMD6	225	BOOT
SCMDP0_23	196	BCMD7	224	BARO
SCMDP0_24	197	BCMD0	223	BAGRANT
SCMDP0_25	198	BCMD1	222	SRST
SCMDP0_26	199	BCMD2	221	SRSTO
SCMDP0_27	200	BCMD3	220	RTCLK
SCMDP0_28	201	BCMD4	219	LOCAL
SCMDP0_29	202	BCMD5	218	POSE1
SCMDP0_30	203	BCMD6	217	POSE2
SCMDP0_31	204	BCMD7	216	POSE3
SCMDP0_32	205	BCMD0	215	ID0
SCMDP0_33	206	BCMD1	214	ID1
SCMDP0_34	207	BCMD2	213	ID2
SCMDP0_35	208	BCMD3	212	ID3
SCMDP0_36	209	BCMD4	211	POSE1
SCMDP0_37	210	BCMD5	210	POSE2
SCMDP0_38	211	BCMD6	209	POSE3
SCMDP0_39	212	BCMD7	208	SUBPOSI
SCMDP0_40	213	BCMD0	207	GND
SCMDP0_41	214	BCMD1	206	GND
SCMDP0_42	215	BCMD2	205	GND
SCMDP0_43	216	BCMD3	204	GND
SCMDP0_44	217	BCMD4	203	GND
SCMDP0_45	218	BCMD5	202	GND
SCMDP0_46	219	BCMD6	201	GND
SCMDP0_47	220	BCMD7	200	GND
SCMDP0_48	221	BCMD0	199	GND
SCMDP0_49	222	BCMD1	198	GND
SCMDP0_50	223	BCMD2	197	GND
SCMDP0_51	224	BCMD3	196	GND
SCMDP0_52	225	BCMD4	195	GND
SCMDP0_53	226	BCMD5	194	GND
SCMDP0_54	227	BCMD6	193	GND
SCMDP0_55	228	BCMD7	192	GND
SCMDP0_56	229	BCMD0	191	GND
SCMDP0_57	230	BCMD1	190	GND
SCMDP0_58	231	BCMD2	189	GND
SCMDP0_59	232	BCMD3	188	GND
SCMDP0_60	233	BCMD4	187	GND
SCMDP0_61	234	BCMD5	186	GND
SCMDP0_62	235	BCMD6	185	GND
SCMDP0_63	236	BCMD7	184	GND
SCMDP0_64	237	BCMD0	183	GND
SCMDP0_65	238	BCMD1	182	GND
SCMDP0_66	239	BCMD2	181	GND
SCMDP0_67	240	BCMD3	180	GND
SCMDP0_68	241	BCMD4	179	GND
SCMDP0_69	242	BCMD5	178	GND
SCMDP0_70	243	BCMD6	177	GND
SCMDP0_71	244	BCMD7	176	GND
SCMDP0_72	245	BCMD0	175	GND
SCMDP0_73	246	BCMD1	174	GND
SCMDP0_74	247	BCMD2	173	GND
SCMDP0_75	248	BCMD3	172	GND
SCMDP0_76	249	BCMD4	171	GND
SCMDP0_77	250	BCMD5	170	GND
SCMDP0_78	251	BCMD6	169	GND
SCMDP0_79	252	BCMD7	168	GND
SCMDP0_80	253	BCMD0	167	GND
SCMDP0_81	254	BCMD1	166	GND
SCMDP0_82	255	BCMD2	165	GND
SCMDP0_83	256	BCMD3	164	GND
SCMDP0_84	257	BCMD4	163	GND
SCMDP0_85	258	BCMD5	162	GND
SCMDP0_86	259	BCMD6	161	GND
SCMDP0_87	260	BCMD7	160	GND
SCMDP0_88	261	BCMD0	159	GND
SCMDP0_89	262	BCMD1	158	GND
SCMDP0_90	263	BCMD2	157	GND
SCMDP0_91	264	BCMD3	156	GND
SCMDP0_92	265	BCMD4	155	GND
SCMDP0_93	266	BCMD5	154	GND
SCMDP0_94	267	BCMD6	153	GND
SCMDP0_95	268	BCMD7	152	GND
SCMDP0_96	269	BCMD0	151	GND
SCMDP0_97	270	BCMD1	150	GND
SCMDP0_98	271	BCMD2	149	GND
SCMDP0_99	272	BCMD3	148	GND



SADO_0	52	BAD0	89	LAD_R0
SADO_1	53	BAD1	90	LAD_R1
SADO_2	54	BAD2	91	LAD_R2
SADO_3	55	BAD3	92	LAD_R3
SADO_4	56	BAD4	93	LAD_R4
SADO_5	57	BAD5	94	LAD_R5
SADO_6	58	BAD6	95	LAD_R6
SADO_7	59	BAD7	96	LAD_R7
SADO_8	60	BAD8	97	LAD_R8
SADO_9	61	BAD9	98	LAD_R9
SADO_10	62	BAD10	99	LAD_R10
SADO_11	63	BAD11	100	LAD_R11
SADO_12	64	BAD12	101	LAD_R12
SADO_13	65	BAD13	102	LAD_R13
SADO_14	66	BAD14	103	LAD_R14
SADO_15	67	BAD15	104	LAD_R15
SADO_16	68	BAD16	105	LAD_R16
SADO_17	69	BAD17	106	LAD_R17
SADO_18	70	BAD18	107	LAD_R18
SADO_19	71	BAD19	108	LAD_R19
SADO_20	72	BAD20	109	LAD_R20
SADO_21	73	BAD21	110	LAD_R21
SADO_22	74	BAD22	111	LAD_R22
SADO_23	75	BAD23	112	LAD_R23
SADO_24	76	BAD24	113	LAD_R24
SADO_25	77	BAD25	114	LAD_R25
SADO_26	78	BAD26	115	LAD_R26
SADO_27	79	BAD27	116	LAD_R27
SADO_28	80	BAD28	117	LAD_R28
SADO_29	81	BAD29	118	LAD_R29
SADO_30	82	BAD30	119	LAD_R30
SADO_31	83	BAD31	120	LAD_R31
SADO_32	84	BAD32	121	LAD_R32
SADO_33	85	BAD33	122	LAD_R33
SADO_34	86	BAD34	123	LAD_R34
SADO_35	87	BAD35	124	LAD_R35
SADO_36	88	BAD36	125	LAD_R36
SADO_37	89	BAD37	126	LAD_R37
SADO_38	90	BAD38	127	LAD_R38
SADO_39	91	BAD39	128	LAD_R39
SADO_40	92	BAD40	129	LAD_R40
SADO_41	93	BAD41	130	LAD_R41
SADO_42	94	BAD42	131	LAD_R42
SADO_43	95	BAD43	132	LAD_R43
SADO_44	96	BAD44	133	LAD_R44
SADO_45	97	BAD45	134	LAD_R45
SADO_46	98	BAD46	135	LAD_R46
SADO_47	99	BAD47	136	LAD_R47
SADO_48	100	BAD48	137	LAD_R48
SADO_49	101	BAD49	138	LAD_R49
SADO_50	102	BAD50	139	LAD_R50
SADO_51	103	BAD51	140	LAD_R51
SADO_52	104	BAD52	141	LAD_R52
SADO_53	105	BAD53	142	LAD_R53
SADO_54	106	BAD54	143	LAD_R54
SADO_55	107	BAD55	144	LAD_R55
SADO_56	108	BAD56	145	LAD_R56
SADO_57	109	BAD57	146	LAD_R57
SADO_58	110	BAD58	147	LAD_R58
SADO_59	111	BAD59	148	LAD_R59
SADO_60	112	BAD60	149	LAD_R60
SADO_61	113	BAD61	150	LAD_R61
SADO_62	114	BAD62	151	LAD_R62
SADO_63	115	BAD63	152	LAD_R63
SADO_64	116	BAD64	153	LAD_R64
SADO_65	117	BAD65	154	LAD_R65
SADO_66	118	BAD66	155	LAD_R66
SADO_67	119	BAD67	156	LAD_R67

SADPO_[7:0]

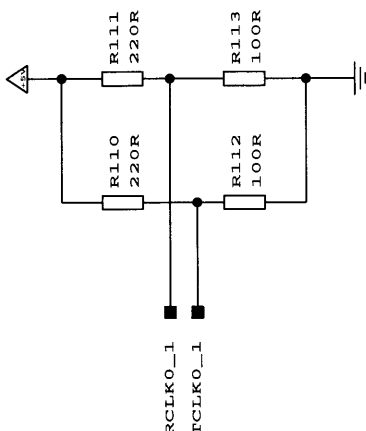
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SADPO_1	102	BAD61	81	LADP_R1
SADPO_2	103	BAD62	82	LADP_R2
SADPO_3	104	BAD63	83	LADP_R3
SADPO_4	105	BAD64	84	LADP_R4
SADPO_5	106	BAD65	85	LADP_R5
SADPO_6	107	BAD66	86	LADP_R6
SADPO_7	108	BAD67	87	LADP_R7

SCMDO_[8:0]

SCMDO_0	173	RCMD0	8	LCMD_R0
SCMDO_1	174	RCMD1	7	LCMD_R1
SCMDO_2	175	RCMD2	6	LCMD_R2
SCMDO_3	176	RCMD3	5	LCMD_R3
SCMDO_4	177	RCMD4	4	LCMD_R4
SCMDO_5	178	RCMD5	3	LCMD_R5
SCMDO_6	179	RCMD6	2	LCMD_R6
SCMDO_7	180	RCMD7	1	LCMD_R7
SCMDO_8	181	RCMD8	0	LCMD_R8
SCMDO_9	182	RCMD9	240	LCMD_R9
SCMDO_10	183	RCMD10	239	LCMD_R10

SCMDPO

[1,2]	SCMDPO	AVIN	237	
[1]	/VALOUT0	AVOUT	237	
[2]	/RELEASE_I0	DVAIN	236	
[15]	/VALIN_LO	DVOUT	235	
[15]	/EXTRO_LO	BUSYOUT	236	
[15]	/WRDRY_LO	SHRDIN	225	
[15]	/VDACK_LO	SHRDOUT	225	
[15]	/VDERR_LO	INTVOUT	233	
[1,3]	TCLKO_1	INTVOUT	231	
[1,3]	VDD	INPER	230	
[1,3]	GND	SNPHIT	221	
[1,3]	GND	BOOT	229	
[2]	/CHKEN	BAGRANT0	228	
[13]	LEDO_2	RESET	222	
[13]	LEDO_3	BTCLK	217	
[13]	GND	LOCAL	216	
[13]	GND	POS0	215	IO0
[13]	GND	POS1	214	IO1
[13]	GND	POS2	213	IO2
[13]	GND	POS3	212	IO3



[1,3] RCLKO_1
[1,3] TCLKO_1

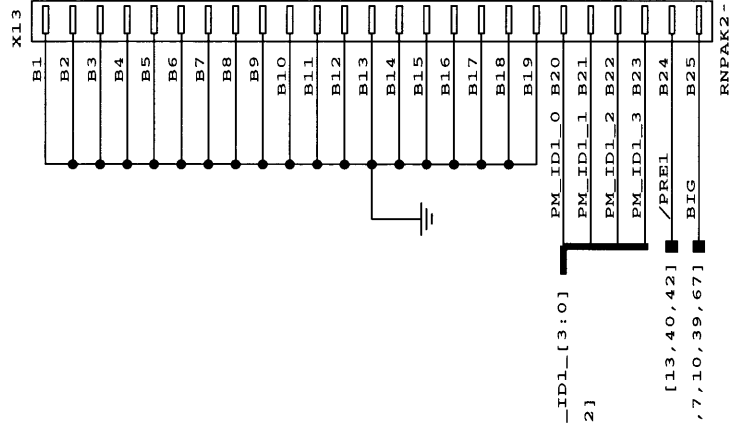
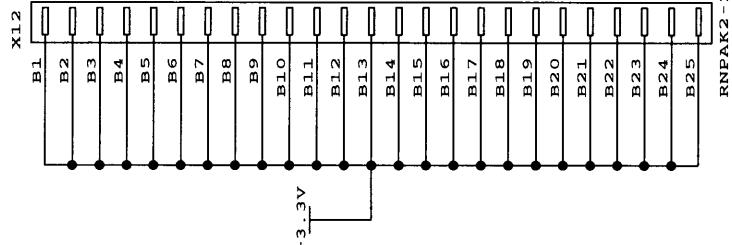
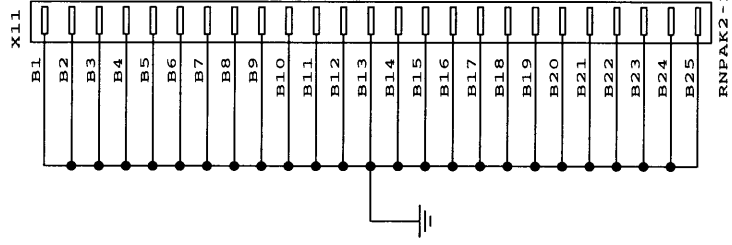
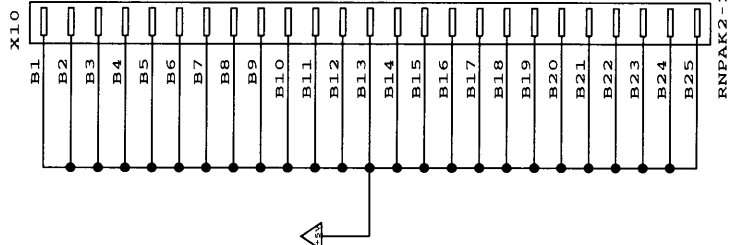
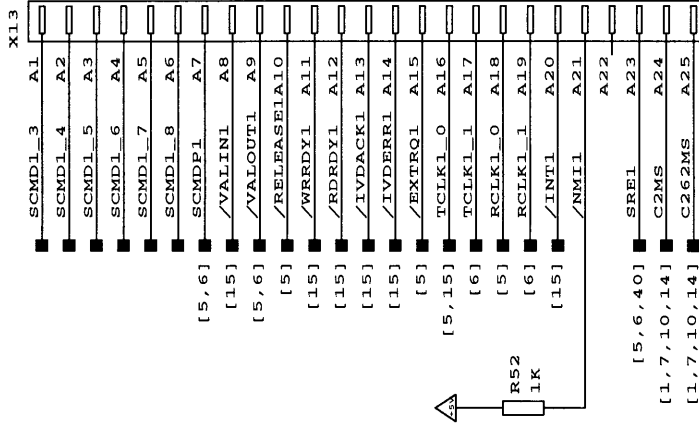
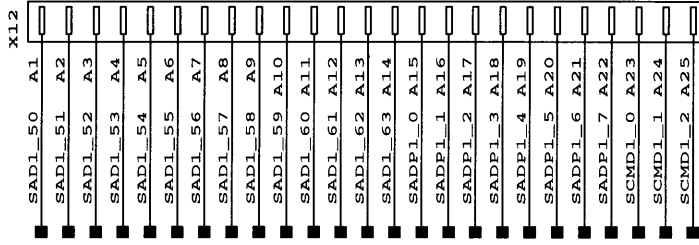
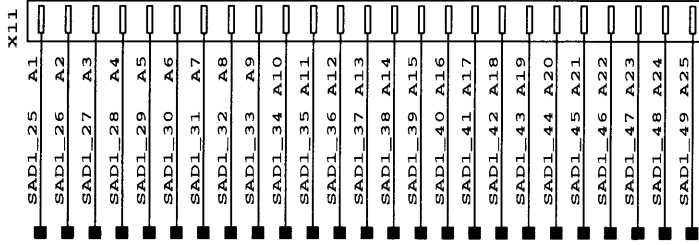
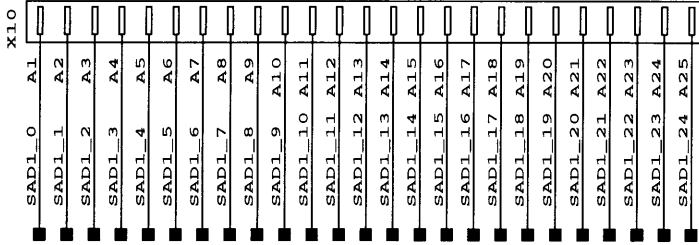
LCMD_R[7:0]

LCMD_R[7:0]	[6,9,12,17,18,28,52,61,69]
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LCMDP_R

LCMDP_R	[6,9,12,52,61]
LAVAL_R	[6,9,12,17,18,25,61,69]
LDVAL_R	[6,9,12,17,18,25,61,69]
LBUSY_INO	[73]
LBUSY_OUTO	[16]
LSHRD_R	[25,63]
LSHRD_OUTO	[116]
LINTV_R	[50,63]
LINTV_OUTO	[16,26,73]
LUPERR_R	[16,63]
LSNPHITO	[126]
LBAREO0	[121]
LBAGRANTO	[121]
SREO	[1,40]
LIBRCLKO	[153]
LIBRCLKI	[153]
VDD	[153]
ID[3:0]	[39,65]

dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local agent 0	
Issue 2			
Issue 3			



SADP1_0	92	PAD0	BAD0	89	AD_R0
SADP1_1	93	PAD1	BAD1	88	AD_R1
SADP1_2	94	PAD2	BAD2	87	AD_R2
SADP1_3	95	PAD3	BAD3	86	AD_R3
SADP1_4	96	PAD4	BAD4	85	AD_R4
SADP1_5	97	PAD5	BAD5	84	AD_R5
SADP1_6	98	PAD6	BAD6	83	AD_R6
SADP1_7	99	PAD7	BAD7	82	AD_R7
SADP1_8	100	PAD8	BAD8	81	AD_R8
SADP1_9	101	PAD9	BAD9	80	AD_R9
SADP1_10	102	PAD10	BAD10	79	AD_R10
SADP1_11	103	PAD11	BAD11	78	AD_R11
SADP1_12	104	PAD12	BAD12	77	AD_R12
SADP1_13	105	PAD13	BAD13	76	AD_R13
SADP1_14	106	PAD14	BAD14	75	AD_R14
SADP1_15	107	PAD15	BAD15	74	AD_R15
SADP1_16	108	PAD16	BAD16	73	AD_R16
SADP1_17	109	PAD17	BAD17	72	AD_R17
SADP1_18	110	PAD18	BAD18	71	AD_R18
SADP1_19	111	PAD19	BAD19	70	AD_R19
SADP1_20	112	PAD20	BAD20	69	AD_R20
SADP1_21	113	PAD21	BAD21	68	AD_R21
SADP1_22	114	PAD22	BAD22	67	AD_R22
SADP1_23	115	PAD23	BAD23	66	AD_R23
SADP1_24	116	PAD24	BAD24	65	AD_R24
SADP1_25	117	PAD25	BAD25	64	AD_R25
SADP1_26	118	PAD26	BAD26	63	AD_R26
SADP1_27	119	PAD27	BAD27	62	AD_R27
SADP1_28	120	PAD28	BAD28	61	AD_R28
SADP1_29	121	PAD29	BAD29	60	AD_R29
SADP1_30	122	PAD30	BAD30	59	AD_R30
SADP1_31	123	PAD31	BAD31	58	AD_R31
SADP1_32	124	PAD32	BAD32	57	AD_R32
SADP1_33	125	PAD33	BAD33	56	AD_R33
SADP1_34	126	PAD34	BAD34	55	AD_R34
SADP1_35	127	PAD35	BAD35	54	AD_R35
SADP1_36	128	PAD36	BAD36	53	AD_R36
SADP1_37	129	PAD37	BAD37	52	AD_R37
SADP1_38	130	PAD38	BAD38	51	AD_R38
SADP1_39	131	PAD39	BAD39	50	AD_R39
SADP1_40	132	PAD40	BAD40	49	AD_R40
SADP1_41	133	PAD41	BAD41	48	AD_R41
SADP1_42	134	PAD42	BAD42	47	AD_R42
SADP1_43	135	PAD43	BAD43	46	AD_R43
SADP1_44	136	PAD44	BAD44	45	AD_R44
SADP1_45	137	PAD45	BAD45	44	AD_R45
SADP1_46	138	PAD46	BAD46	43	AD_R46
SADP1_47	139	PAD47	BAD47	42	AD_R47
SADP1_48	140	PAD48	BAD48	41	AD_R48
SADP1_49	141	PAD49	BAD49	40	AD_R49
SADP1_50	142	PAD50	BAD50	39	AD_R50
SADP1_51	143	PAD51	BAD51	38	AD_R51
SADP1_52	144	PAD52	BAD52	37	AD_R52
SADP1_53	145	PAD53	BAD53	36	AD_R53
SADP1_54	146	PAD54	BAD54	35	AD_R54
SADP1_55	147	PAD55	BAD55	34	AD_R55
SADP1_56	148	PAD56	BAD56	33	AD_R56
SADP1_57	149	PAD57	BAD57	32	AD_R57
SADP1_58	150	PAD58	BAD58	31	AD_R58
SADP1_59	151	PAD59	BAD59	30	AD_R59
SADP1_60	152	PAD60	BAD60	29	AD_R60
SADP1_61	153	PAD61	BAD61	28	AD_R61
SADP1_62	154	PAD62	BAD62	27	AD_R62
SADP1_63	155	PAD63	BAD63	26	AD_R63
SADP1_64	156	PAD64	BAD64	25	AD_R64
SADP1_65	157	PAD65	BAD65	24	AD_R65
SADP1_66	158	PAD66	BAD66	23	AD_R66
SADP1_67	159	PAD67	BAD67	22	AD_R67
SADP1_68	160	PAD68	BAD68	21	AD_R68
SADP1_69	161	PAD69	BAD69	20	AD_R69
SADP1_70	162	PAD70	BAD70	19	AD_R70
SADP1_71	163	PAD71	BAD71	18	AD_R71
SADP1_72	164	PAD72	BAD72	17	AD_R72
SADP1_73	165	PAD73	BAD73	16	AD_R73
SADP1_74	166	PAD74	BAD74	15	AD_R74
SADP1_75	167	PAD75	BAD75	14	AD_R75
SADP1_76	168	PAD76	BAD76	13	AD_R76
SADP1_77	169	PAD77	BAD77	12	AD_R77
SADP1_78	170	PAD78	BAD78	11	AD_R78
SADP1_79	171	PAD79	BAD79	10	AD_R79
SADP1_80	172	PAD80	BAD80	9	AD_R80
SADP1_81	173	PAD81	BAD81	8	AD_R81
SADP1_82	174	PAD82	BAD82	7	AD_R82
SADP1_83	175	PAD83	BAD83	6	AD_R83
SADP1_84	176	PAD84	BAD84	5	AD_R84
SADP1_85	177	PAD85	BAD85	4	AD_R85
SADP1_86	178	PAD86	BAD86	3	AD_R86
SADP1_87	179	PAD87	BAD87	2	AD_R87
SADP1_88	180	PAD88	BAD88	1	AD_R88
SADP1_89	181	PAD89	BAD89	0	AD_R89
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SADP1_92	184	PAD92	BAD92	0	AD_R92
SADP1_93	185	PAD93	BAD93	0	AD_R93
SADP1_94	186	PAD94	BAD94	0	AD_R94
SADP1_95	187	PAD95	BAD95	0	AD_R95
SADP1_96	188	PAD96	BAD96	0	AD_R96
SADP1_97	189	PAD97	BAD97	0	AD_R97
SADP1_98	190	PAD98	BAD98	0	AD_R98
SADP1_99	191	PAD99	BAD99	0	AD_R99
SADP1_100	192	PAD100	BAD100	0	AD_R100
SADP1_101	193	PAD101	BAD101	0	AD_R101
SADP1_102	194	PAD102	BAD102	0	AD_R102
SADP1_103	195	PAD103	BAD103	0	AD_R103
SADP1_104	196	PAD104	BAD104	0	AD_R104
SADP1_105	197	PAD105	BAD105	0	AD_R105
SADP1_106	198	PAD106	BAD106	0	AD_R106
SADP1_107	199	PAD107	BAD107	0	AD_R107
SADP1_108	200	PAD108	BAD108	0	AD_R108
SADP1_109	201	PAD109	BAD109	0	AD_R109
SADP1_110	202	PAD110	BAD110	0	AD_R110
SADP1_111	203	PAD111	BAD111	0	AD_R111
SADP1_112	204	PAD112	BAD112	0	AD_R112
SADP1_113	205	PAD113	BAD113	0	AD_R113
SADP1_114	206	PAD114	BAD114	0	AD_R114
SADP1_115	207	PAD115	BAD115	0	AD_R115
SADP1_116	208	PAD116	BAD116	0	AD_R116
SADP1_117	209	PAD117	BAD117	0	AD_R117
SADP1_118	210	PAD118	BAD118	0	AD_R118
SADP1_119	211	PAD119	BAD119	0	AD_R119
SADP1_120	212	PAD120	BAD120	0	AD_R120
SADP1_121	213	PAD121	BAD121	0	AD_R121
SADP1_122	214	PAD122	BAD122	0	AD_R122
SADP1_123	215	PAD123	BAD123	0	AD_R123
SADP1_124	216	PAD124	BAD124	0	AD_R124
SADP1_125	217	PAD125	BAD125	0	AD_R125
SADP1_126	218	PAD126	BAD126	0	AD_R126
SADP1_127	219	PAD127	BAD127	0	AD_R127
SADP1_128	220	PAD128	BAD128	0	AD_R128
SADP1_129	221	PAD129	BAD129	0	AD_R129
SADP1_130	222	PAD130	BAD130	0	AD_R130
SADP1_131	223	PAD131	BAD131	0	AD_R131
SADP1_132	224	PAD132	BAD132	0	AD_R132
SADP1_133	225	PAD133	BAD133	0	AD_R133
SADP1_134	226	PAD134	BAD134	0	AD_R134
SADP1_135	227	PAD135	BAD135	0	AD_R135
SADP1_136	228	PAD136	BAD136	0	AD_R136
SADP1_137	229	PAD137	BAD137	0	AD_R137
SADP1_138	230	PAD138	BAD138	0	AD_R138
SADP1_139	231	PAD139	BAD139	0	AD_R139
SADP1_140	232	PAD140	BAD140	0	AD_R140
SADP1_141	233	PAD141	BAD141	0	AD_R141
SADP1_142	234	PAD142	BAD142	0	AD_R142
SADP1_143	235	PAD143	BAD143	0	AD_R143
SADP1_144	236	PAD144	BAD144	0	AD_R144
SADP1_145	237	PAD145	BAD145	0	AD_R145
SADP1_146	238	PAD146	BAD146	0	AD_R146
SADP1_147	239	PAD147	BAD147	0	AD_R147
SADP1_148	240	PAD148	BAD148	0	AD_R148
SADP1_149	241	PAD149	BAD149	0	AD_R149
SADP1_150	242	PAD150	BAD150	0	AD_R150
SADP1_151	243	PAD151	BAD151	0	AD_R151
SADP1_152	244	PAD152	BAD152	0	AD_R152
SADP1_153	245	PAD153	BAD153	0	AD_R153
SADP1_154	246	PAD154	BAD154	0	AD_R154
SADP1_155	247	PAD155	BAD155	0	AD_R155
SADP1_156	248	PAD156	BAD156	0	AD_R156
SADP1_157	249	PAD157	BAD157	0	AD_R157
SADP1_158	250	PAD158	BAD158	0	AD_R158
SADP1_159	251	PAD159	BAD159	0	AD_R159
SADP1_160	252	PAD160	BAD160	0	AD_R160
SADP1_161	253	PAD161	BAD161	0	AD_R161
SADP1_162	254	PAD162	BAD162	0	AD_R162
SADP1_163	255	PAD163	BAD163	0	AD_R163
SADP1_164	256	PAD164	BAD164	0	AD_R164
SADP1_165	257	PAD165	BAD165	0	AD_R165
SADP1_166	258	PAD166	BAD166	0	AD_R166
SADP1_167	259	PAD167	BAD167	0	AD_R167
SADP1_168	260	PAD168	BAD168	0	AD_R168
SADP1_169	261	PAD169	BAD169	0	AD_R169
SADP1_170	262	PAD170	BAD170	0	AD_R170
SADP1_171	263	PAD171	BAD171	0	AD_R171
SADP1_172	264	PAD172	BAD172	0	AD_R172
SADP1_173	265	PAD173	BAD173	0	AD_R173
SADP1_174	266	PAD174	BAD174	0	AD_R174
SADP1_175	267	PAD175	BAD175	0	AD_R175
SADP1_176	268	PAD176	BAD176	0	AD_R176
SADP1_177	269	PAD177	BAD177	0	AD_R177
SADP1_178	270	PAD178	BAD178	0	AD_R178
SADP1_179	271	PAD179	BAD179	0	AD_R179
SADP1_180	272	PAD180	BAD180	0	AD_R180
SADP1_181	273	PAD181	BAD181	0	AD_R181
SADP1_182	274	PAD182	BAD182	0	AD_R182
SADP1_183	275	PAD183	BAD183	0	AD_R183
SADP1_184	276	PAD184	BAD184	0	AD_R184
SADP1_185	277	PAD185	BAD185	0	AD_R185
SADP1_186	278	PAD186	BAD186	0	AD_R186
SADP1_187	279	PAD187	BAD187	0	AD_R187
SADP1_188	280	PAD188	BAD188	0	AD_R188
SADP1_189	281	PAD189	BAD189	0	AD_R189
SADP1_190	282	PAD190	BAD190	0	AD_R190
SADP1_191	283	PAD191	BAD191	0	AD_R191
SADP1_192	284	PAD192	BAD192	0	AD_R192
SADP1_193	285	PAD193	BAD193	0	AD_R193
SADP1_194	286	PAD194	BAD194	0	AD_R194
SADP1_195	287	PAD195	BAD195	0	AD_R195
SADP1_196	288	PAD196	BAD196	0	AD_R196
SADP1_197	289	PAD197	BAD197	0	AD_R197
SADP1_198	290	PAD198	BAD198	0	AD_R198
SADP1_199	291	PAD199	BAD199	0	AD_R199
SADP1_200	292	PAD200	BAD200	0	AD_R200
SADP1_201	293	PAD201	BAD201	0	AD_R201
SADP1_202	294	PAD202	BAD202	0	AD_R202
SADP1_203	295	PAD203	BAD203	0	AD_R203
SADP1_204	296	PAD204	BAD204	0	AD_R204
SADP1_205	297	PAD205	BAD205	0	AD_R205
SADP1_206	298	PAD206	BAD206	0	AD_R206
SADP1_207	299	PAD207	BAD207	0	AD_R207
SADP1_208	300	PAD208	BAD208	0	AD_R208
SADP1_209	301	PAD209	BAD209	0	AD_R209
SADP1_210	302	PAD210	BAD210	0	AD_R210
SADP1_211					

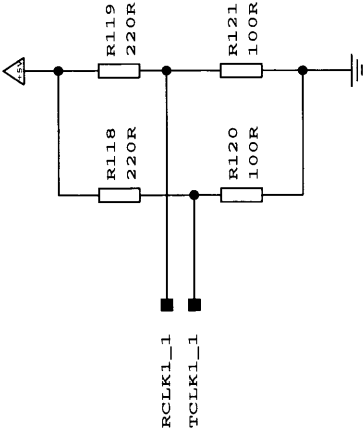
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SAD1_1	93	PAD1
SAD1_2	94	PAD2
SAD1_3	95	PAD3
SAD1_4	96	PAD4
SAD1_5	98	PAD5
SAD1_6	99	PAD6
SAD1_7	100	PAD7
SAD1_8	101	PAD8
SAD1_9	102	PAD9
SAD1_10	104	PAD9
SAD1_11	105	PAD10
SAD1_12	106	PAD12
SAD1_13	107	PAD13
SAD1_14	109	PAD14
SAD1_15	110	PAD15
SAD1_16	111	PAD16
SAD1_17	113	PAD16
SAD1_18	114	PAD17
SAD1_19	115	PAD19
SAD1_20	116	PAD20
SAD1_21	117	PAD21
SAD1_22	118	PAD22
SAD1_23	120	PAD22
SAD1_24	122	PAD23
SAD1_25	123	PAD24
SAD1_26	124	PAD26
SAD1_27	125	PAD27
SAD1_28	126	PAD28
SAD1_29	128	PAD29
SAD1_30	129	PAD30
SAD1_31	129	PAD30
SAD1_32	132	PAD31
SAD1_33	133	PAD33
SAD1_34	134	PAD34
SAD1_35	135	PAD35
SAD1_36	137	PAD36
SAD1_37	137	PAD36
SAD1_38	138	PAD37
SAD1_39	139	PAD39
SAD1_40	142	PAD40
SAD1_41	143	PAD41
SAD1_42	144	PAD42
SAD1_43	144	PAD42
SAD1_44	146	PAD43
SAD1_45	147	PAD44
SAD1_46	148	PAD46
SAD1_47	149	PAD47
SAD1_48	153	PAD48
SAD1_49	153	PAD48
SAD1_50	155	PAD49
SAD1_51	157	PAD50
SAD1_52	158	PAD51
SAD1_53	159	PAD52
SAD1_54	160	PAD54
SAD1_55	161	PAD55
SAD1_56	163	PAD56
SAD1_57	163	PAD56
SAD1_58	166	PAD57
SAD1_59	167	PAD58
SAD1_60	168	PAD60
SAD1_61	169	PAD61
SAD1_62	170	PAD62
SAD1_63	171	PAD63
SAD1_63	171	PAD63

SADP1_0	101	PAD00
SADP1_1	111	PAD01
SADP1_2	121	PAD02
SADP1_3	131	PAD03
SADP1_4	140	PAD04
SADP1_5	152	PAD05
SADP1_6	154	PAD06
SADP1_7	172	PAD07

SCMD1_0	173	PCMD0
SCMD1_1	174	PCMD1
SCMD1_2	175	PCMD2
SCMD1_3	177	PCMD3
SCMD1_4	179	PCMD4
SCMD1_5	180	PCMD5
SCMD1_6	181	PCMD6
SCMD1_7	181	PCMD6
SCMD1_8	182	PCMD8
SCMD1_9	183	PCMDP

[4,5] SCMDP1

[4]	/VALOUT1	197	VALIN
[5]	/RELEASE_L1	198	SELS
[5]	/VALIN_L1	199	VALIN
[5]	/EXTRQ_L1	184	EXTRQ
[15]	/WRDRY_L1	186	WRDRY
[15]	/LDACK_L1	188	LDACK
[15]	/VDERR_L1	190	VDERR
[4,6]	TCLK1_1	203	TCLK
[4,6]	TCLK1_1	204	TCLK
[4,6]	TCLK1_1	200	SLVREQ
[4,6]	TCLK1_1	191	SLVACK
[4,6]	TCLK1_1	201	TRF
[2]	/PCKKEN	202	PCKKEN
[2]	GND	207	GND
[13]	LED1_2	192	LED1
[13]	LED1_3	194	LED1
[13]	VDD	205	VDD
[13]	GND	208	SUBPOSI



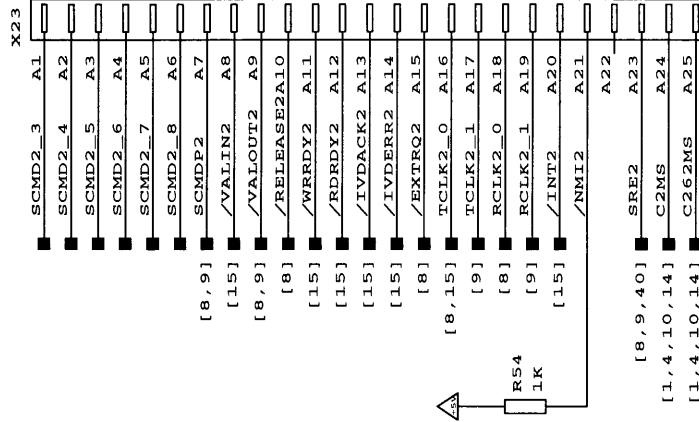
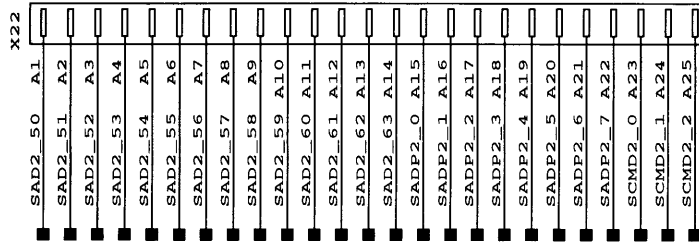
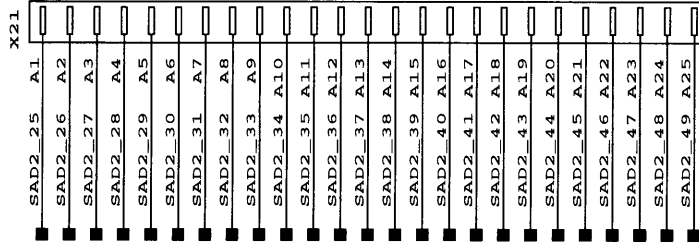
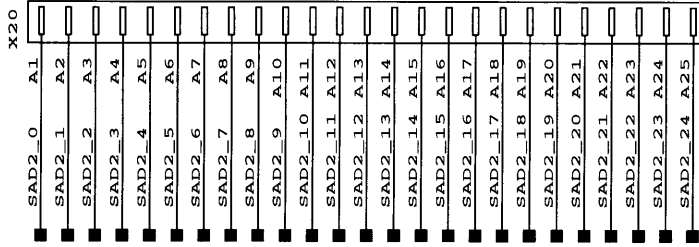
[4,6] RCLK1_1
[4,6] TCLK1_1

LCMD_R0	8	LCMD_R0
LCMD_R1	7	LCMD_R1
LCMD_R2	6	LCMD_R2
LCMD_R3	4	LCMD_R3
LCMD_R4	2	LCMD_R4
LCMD_R5	1	LCMD_R5
LCMD_R6	240	LCMD_R7
LCMD_R7	239	LCMD_R7

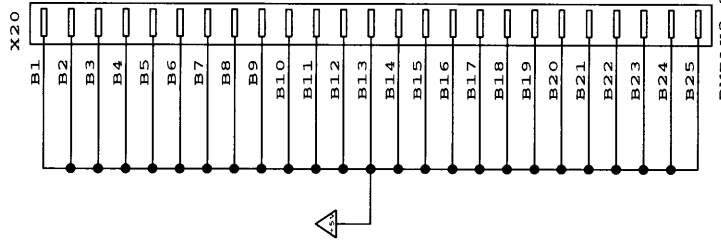
[3,9,12,17,18,20,52,61,69]

LCMDP_R	237	AVIN
LCMDP_R	238	AVOUT
LCMDP_R	236	DVIN
LCMDP_R	236	DVOUT
LCMDP_R	234	BUSYOUT
LCMDP_R	225	SHRDIN
LCMDP_R	233	SHRDOUT
LCMDP_R	231	INTVIN
LCMDP_R	231	INTVOUT
LCMDP_R	230	TRIPR
LCMDP_R	221	SNPHIT
LCMDP_R	229	BOOT
LCMDP_R	229	BARQC
LCMDP_R	222	RESSET
LCMDP_R	217	BLK
LCMDP_R	218	LOCAL
LCMDP_R	216	POS0
LCMDP_R	215	ID0
LCMDP_R	214	POS1
LCMDP_R	214	ID1
LCMDP_R	212	POS2
LCMDP_R	212	ID2
LCMDP_R	212	POS3

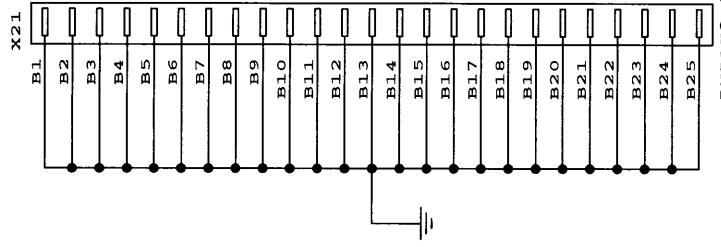
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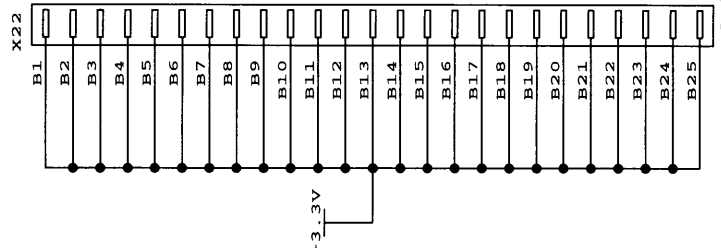
RNPAK2-25P



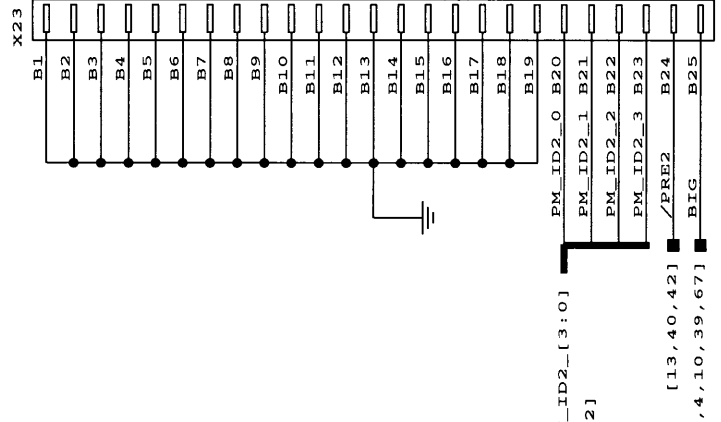
RNPAK2-25P



RNPAK2-25P



RNPAK2-25P



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Issue 3	
CPU301 Module Connectors 2	
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SAD2_[6:0]

U5

AD_R[63:0],ADP_R[7:0]

[2,5,11,17,18,22,43,46,54,55,68]

SAD2_0	92
SAD2_1	93
SAD2_2	94
SAD2_3	95
SAD2_4	96
SAD2_5	98
SAD2_6	99
SAD2_7	100
SAD2_8	103
SAD2_9	104
SAD2_10	104
SAD2_11	105
SAD2_12	106
SAD2_13	107
SAD2_14	109
SAD2_15	110
SAD2_16	112
SAD2_17	113
SAD2_18	114
SAD2_19	115
SAD2_20	116
SAD2_21	117
SAD2_22	120
SAD2_23	120
SAD2_24	122
SAD2_25	123
SAD2_26	124
SAD2_27	125
SAD2_28	126
SAD2_29	128
SAD2_30	128
SAD2_31	129
SAD2_32	132
SAD2_33	133
SAD2_34	134
SAD2_35	135
SAD2_36	137
SAD2_37	137
SAD2_38	138
SAD2_39	139
SAD2_40	142
SAD2_41	143
SAD2_42	144
SAD2_43	144
SAD2_44	146
SAD2_45	147
SAD2_46	148
SAD2_47	149
SAD2_48	153
SAD2_49	155
SAD2_50	155
SAD2_51	157
SAD2_52	158
SAD2_53	159
SAD2_54	160
SAD2_55	161
SAD2_56	163
SAD2_57	163
SAD2_58	166
SAD2_59	167
SAD2_60	168
SAD2_61	169
SAD2_62	170
SAD2_63	171
SAD2_64	171

SADP2_[7:0]

U5

ADP_R[7:0]

[7,8]

SADP2_0	101
SADP2_1	111
SADP2_2	121
SADP2_3	131
SADP2_4	140
SADP2_5	152
SADP2_6	162
SADP2_7	172

SCMD2_[8:0]

U5

CMD_R[7:0]

[2,5,11,17,18,28,48,56,68]

SCMD2_0	173
SCMD2_1	174
SCMD2_2	175
SCMD2_3	177
SCMD2_4	179
SCMD2_5	180
SCMD2_6	181
SCMD2_7	182
SCMD2_8	182
SCMDP	183

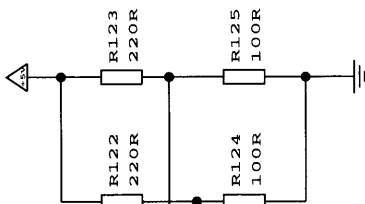
SCMDP2

U5

CMDP_R

[2,5,11,17,18,22,56,68,69]

VALOUT2	197
RELEASE2	198
VD	199
EXTRO2	184
EXTRO2	185
WRDRY_G2	186
WRDRY_G2	188
IVDACK_G2	190
IVDERR_G2	203
RCLK	204
EXTRO_L2	191
RELEASE_L2	201
TREF	207
PCHKEN	202
GND	192
LAMP1	193
LAMP0	194
LAMP1	195
LAMP0	196
GND	208
SUBPOS0	209
VDD	208



RCLK2_0 [7,8]
TCLK2_0 [7,8,15]

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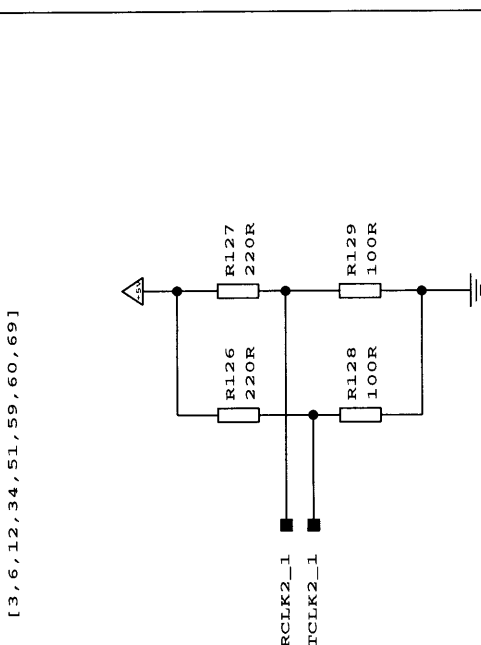
Dansk Data Elektronik A/S
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SAD2_[63:0]

U6

LAD_R[63:0], LADP_R[7:0]

[3,6,12,17,18,25,51,59,60,69]



[7,9] RCLK2_1
[7,9] TCLK2_1

LAD_R[63:0], LADP_R[7:0]

[3,6,12,17,18,25,51,59,60,69]

LAD_R[63:0], LADP_R[7:0]

[3,6,12,17,18,25,51,59,60,69]

LAD_R[63:0], LADP_R[7:0]

[3,6,12,17,18,25,51,59,60,69]

LAD_R[63:0], LADP_R[7:0]

[3,6,12,17,18,25,51,59,60,69]

LAD_R[63:0], LADP_R[7:0]

[3,6,12,17,18,25,51,59,60,69]

LAD_R[63:0], LADP_R[7:0]

[3,6,12,17,18,25,51,59,60,69]

LAD_R[63:0], LADP_R[7:0]

[3,6,12,17,18,25,51,59,60,69]

SADP2_[7:0]

U6

LADP_R[7:0]

[3,6,12,17,18,25,51,59,60,69]

SCMD2_[8:0]

U6

LCMD_R[7:0]

[3,6,12,17,18,25,51,59,60,69]

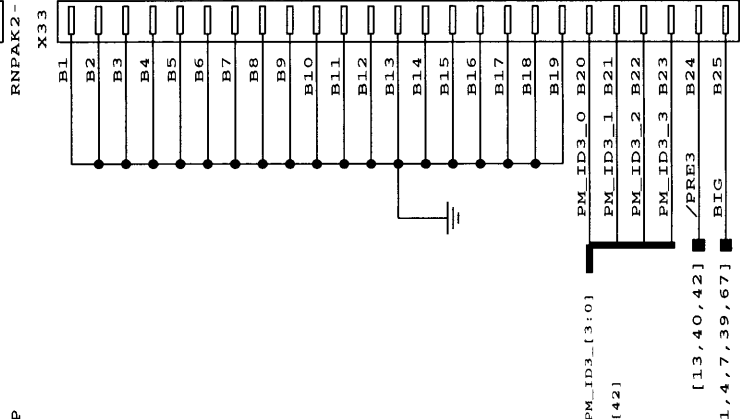
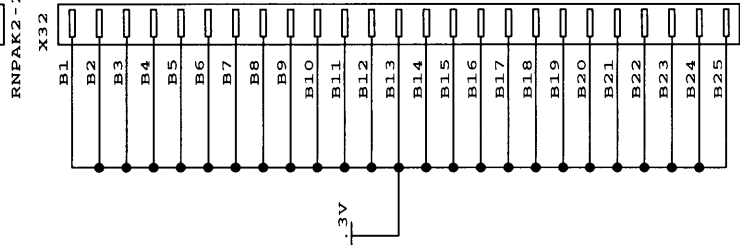
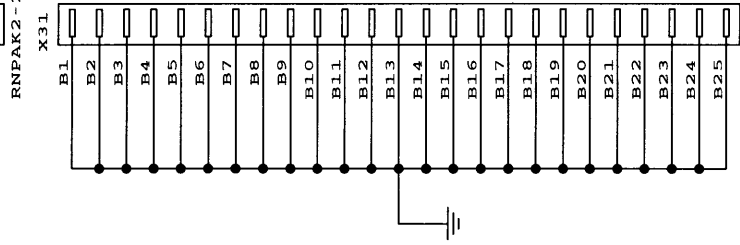
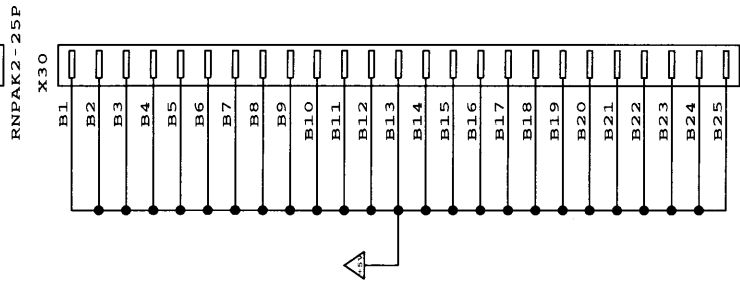
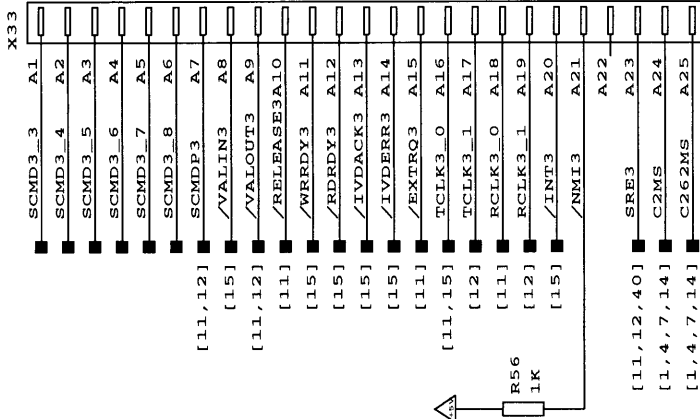
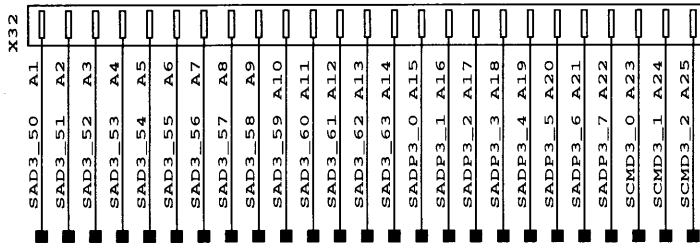
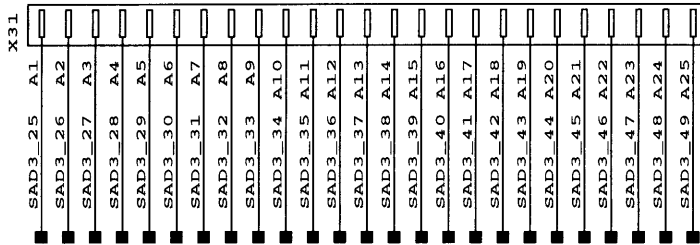
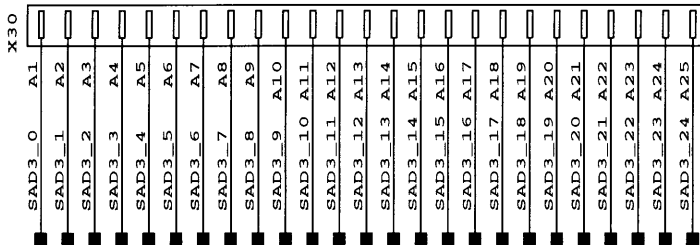
SCMDP2

U6

LCMDP_R

[3,6,12,52,61]

BAD0	89	LAD_R0
BAD1	88	LAD_R1
BAD2	86	LAD_R3
BAD3	85	LAD_R4
BAD4	83	LAD_R5
BAD5	82	LAD_R6
BAD6	81	LAD_R7
BAD7	79	LAD_R8
BAD8	77	LAD_R10
BAD9	76	LAD_R11
BAD10	75	LAD_R12
BAD11	74	LAD_R13
BAD12	72	LAD_R14
BAD13	71	LAD_R15
BAD14	68	LAD_R17
BAD15	67	LAD_R18
BAD16	66	LAD_R19
BAD17	65	LAD_R20
BAD18	64	LAD_R21
BAD19	63	LAD_R22
BAD20	62	LAD_R23
BAD21	59	LAD_R24
BAD22	58	LAD_R25
BAD23	56	LAD_R27
BAD24	55	LAD_R28
BAD25	54	LAD_R29
BAD26	53	LAD_R30
BAD27	52	LAD_R31
BAD28	49	LAD_R32
BAD29	48	LAD_R33
BAD30	47	LAD_R34
BAD31	46	LAD_R35
BAD32	45	LAD_R36
BAD33	44	LAD_R37
BAD34	43	LAD_R38
BAD35	42	LAD_R39
BAD36	41	LAD_R40
BAD37	38	LAD_R41
BAD38	37	LAD_R42
BAD39	35	LAD_R43
BAD40	34	LAD_R44
BAD41	33	LAD_R45
BAD42	32	LAD_R46
BAD43	28	LAD_R48
BAD44	26	LAD_R49
BAD45	25	LAD_R50
BAD46	23	LAD_R52
BAD47	22	LAD_R53
BAD48	21	LAD_R54
BAD49	20	LAD_R55
BAD50	19	LAD_R56
BAD51	18	LAD_R57
BAD52	16	LAD_R59
BAD53	15	LAD_R60
BAD54	14	LAD_R61
BAD55	13	LAD_R62
BAD56	12	LAD_R63
BAD57	11	LAD_R64
BAD58	10	LAD_R65
BAD59	8	LADP_R0
BAD60	7	LADP_R1
BAD61	6	LADP_R2
BAD62	5	LADP_R3
BAD63	4	LADP_R4
BAD64	3	LADP_R5
BAD65	2	LADP_R6
BAD66	1	LADP_R7
BAD67	0	LADP_R8
BCMD0	8	LCMD_R0
BCMD1	7	LCMD_R1
BCMD2	6	LCMD_R2
BCMD3	4	LCMD_R3
BCMD4	2	LCMD_R5
BCMD5	1	LCMD_R6
BCMD6	240	LCMD_R7
BCMD7	239	LCMD_R8
AVIN	237	
AVOUT	236	
DVIN	235	
DVOUT	234	
BUSYOUT	226	
SHRDIN	225	
SHROUT	223	
INTVIN	221	
INTVOUT	223	
INTVCLK	220	
SNPHIT	221	
BOOT	229	
BARQ	228	
RESET	222	
BRCLK	217	
LOCAL	216	
POS0	215	
POS1	214	
POS2	213	
POS3	212	
AVIN	237	
AVOUT	236	
DVIN	235	
DVOUT	234	
BUSYOUT	226	
SHRDIN	225	
SHROUT	223	
INTVIN	221	
INTVOUT	223	
INTVCLK	220	
SNPHIT	221	
BOOT	229	
BARQ	228	
RESET	222	
BRCLK	217	
LOCAL	216	
POS0	215	
POS1	214	
POS2	213	
POS3	212	



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SAD3_0	52	PAD0
SAD3_1	53	PAD1
SAD3_2	54	PAD2
SAD3_3	55	PAD3
SAD3_4	56	PAD4
SAD3_5	57	PAD5
SAD3_6	58	PAD6
SAD3_7	59	PAD7
SAD3_8	60	PAD8
SAD3_9	61	PAD9
SAD3_10	62	PAD10
SAD3_11	63	PAD11
SAD3_12	64	PAD12
SAD3_13	65	PAD13
SAD3_14	66	PAD14
SAD3_15	67	PAD15
SAD3_16	68	PAD16
SAD3_17	69	PAD17
SAD3_18	70	PAD18
SAD3_19	71	PAD19
SAD3_20	72	PAD20
SAD3_21	73	PAD21
SAD3_22	74	PAD22
SAD3_23	75	PAD23
SAD3_24	76	PAD24
SAD3_25	77	PAD25
SAD3_26	78	PAD26
SAD3_27	79	PAD27
SAD3_28	80	PAD28
SAD3_29	81	PAD29
SAD3_30	82	PAD30
SAD3_31	83	PAD31
SAD3_32	84	PAD32
SAD3_33	85	PAD33
SAD3_34	86	PAD34
SAD3_35	87	PAD35
SAD3_36	88	PAD36
SAD3_37	89	PAD37
SAD3_38	90	PAD38
SAD3_39	91	PAD39
SAD3_40	92	PAD40
SAD3_41	93	PAD41
SAD3_42	94	PAD42
SAD3_43	95	PAD43
SAD3_44	96	PAD44
SAD3_45	97	PAD45
SAD3_46	98	PAD46
SAD3_47	99	PAD47
SAD3_48	100	PAD48
SAD3_49	101	PAD49
SAD3_50	102	PAD50
SAD3_51	103	PAD51
SAD3_52	104	PAD52
SAD3_53	105	PAD53
SAD3_54	106	PAD54
SAD3_55	107	PAD55
SAD3_56	108	PAD56
SAD3_57	109	PAD57
SAD3_58	110	PAD58
SAD3_59	111	PAD59
SAD3_60	112	PAD60
SAD3_61	113	PAD61
SAD3_62	114	PAD62
SAD3_63	115	PAD63
SADP3_0	101	PADC0
SADP3_1	102	PADC1
SADP3_2	103	PADC2
SADP3_3	104	PADC3
SADP3_4	105	PADC4
SADP3_5	106	PADC5
SADP3_6	107	PADC6
SADP3_7	108	PADC7
SCMD3_0	173	PCMD0
SCMD3_1	174	PCMD1
SCMD3_2	175	PCMD2
SCMD3_3	176	PCMD3
SCMD3_4	177	PCMD4
SCMD3_5	178	PCMD5
SCMD3_6	179	PCMD6
SCMD3_7	180	PCMD7
SCMD3_8	181	PCMD8
SCMD3_9	182	PCMD9
SCMDP3	183	PCMDP

LADP_R[7:0] [3,6,9,17,18,28,52,61,69]

LCMD_R[7:0] [3,6,9,17,18,28,52,61,69]

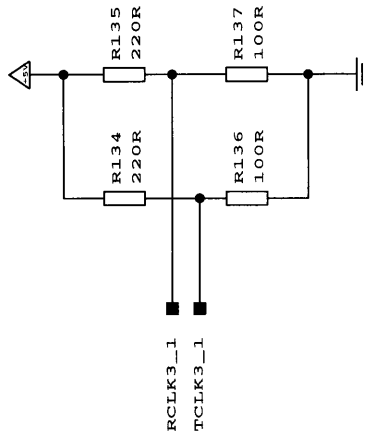
SCMDP3

SCMD3_[8:0]

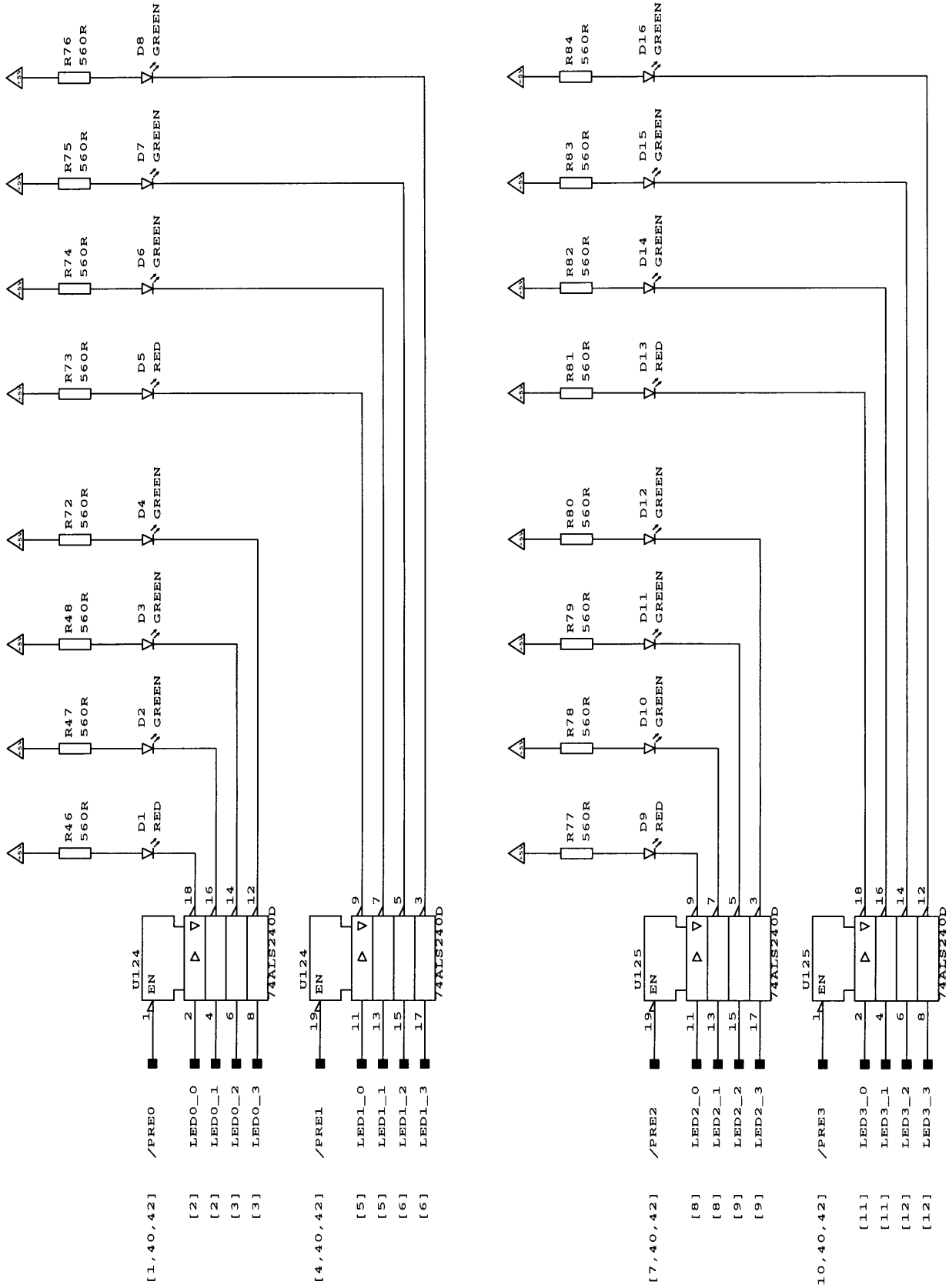
(10,11)

/VALOUT3	101	VALIN
/RELEASE_L3	102	RELS
/VALIN_L3	103	VALOUT
/EXTRO_L3	104	EXTRO
/WRDY_L3	105	WRDY
/VDACK_L3	106	VDACK
/VDERR_L3	107	VDERR
RCLK3_1	108	RCLK3_1
RCLK3_2	109	RCLK3_2
RCLK3_3	110	RCLK3_3
VDD	111	VDD
GND	112	GND
/PCHKEN	202	PCHKEN
GND	203	GND
LED3_2	192	LED3_2
LED3_3	193	LED3_3
VDD	194	VDD
LAMP0	195	LAMP0
LAMP1	196	LAMP1
VDD	197	VDD
SUBPOS0	208	SUBPOS0
SUBPOS1	209	SUBPOS1
SUBPOS2	210	SUBPOS2
SUBPOS3	211	SUBPOS3
AVIN	237	AVIN
AVOUT	238	AVOUT
DVIN	239	DVIN
BUSSIN	240	BUSSIN
BUSSOUT	241	BUSSOUT
RUSYOUT	242	RUSYOUT
SHRDIN	243	SHRDIN
SHRDOUT	244	SHRDOUT
INTVIN	245	INTVIN
INTVOUT	246	INTVOUT
PACK	247	PACK
SNPHT	248	SNPHT
SNPHT2	249	SNPHT2
SNPHT3	250	SNPHT3
BOO1	251	BOO1
BOO2	252	BOO2
BOO3	253	BOO3
BAGRANT	254	BAGRANT
RESET	255	RESET
BRCLK	256	BRCLK
BRCLK2	257	BRCLK2
LOCAL	258	LOCAL
POS0	259	POS0
POS1	260	POS1
POS2	261	POS2
POS3	262	POS3

LADP_R	[3,6,9,17,18,28,52,61,69]
LCMD_R	[3,6,9,17,18,28,52,61,69]
LAVAL_R	[3,6,9,17,18,25,61,69]
LVAL_R	[3,6,9,17,18,25,61,69]
LBUSY_IN3	[16]
LBUSY_OUT3	[16]
LSHRD_R	[25,63]
LSHRD_OUT3	[16]
LINTV_R	[50,63]
LINTV_OUT3	[16,27,73]
LTPACK_R	[50,63]
LTRCK_R	[50,63]
LNSPHT3	[27]
LBAREQ3	[21]
LBAGRANT3	[21]
SRES3	[10,40]
LBRCLK2	[53]
LBRCLK	[53]
VDD	[39,65]
ID[3:0]	[39,65]



dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1	950131	Local agent 3
Issue 2		
Issue 3		



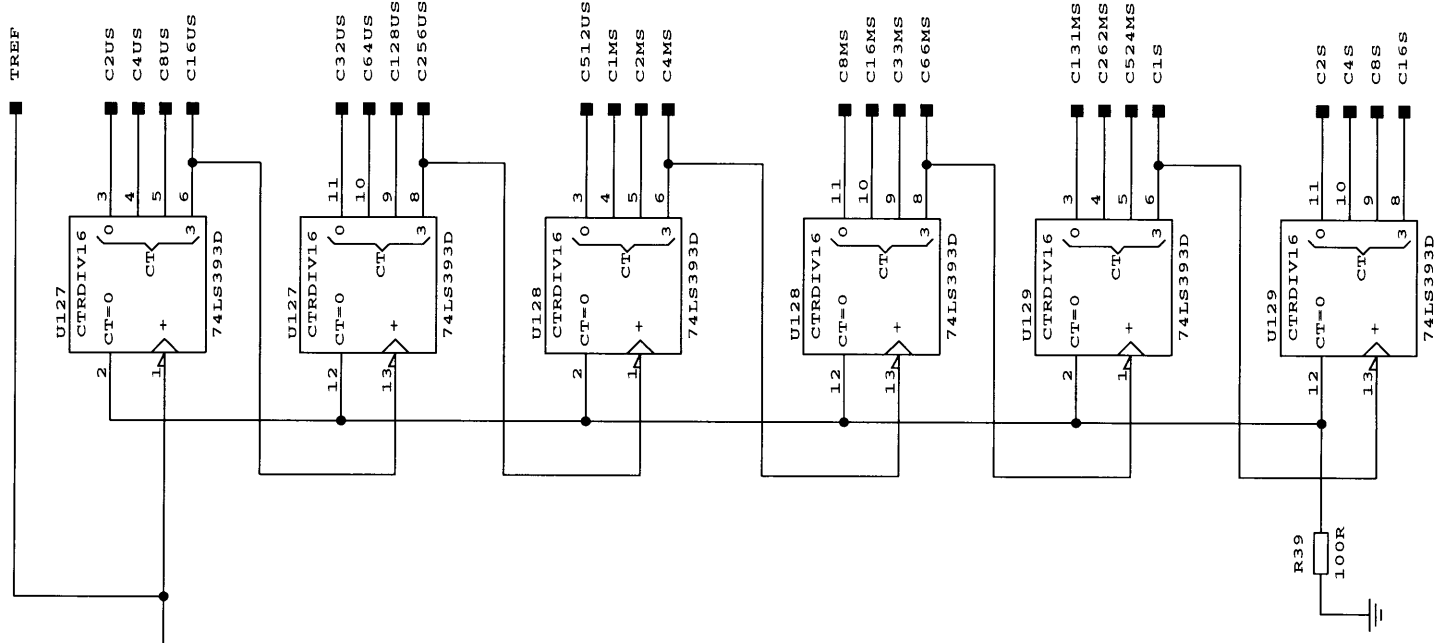
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Programmable LEDs	
Issue 2			
Issue 3			

[2,5,8,11]

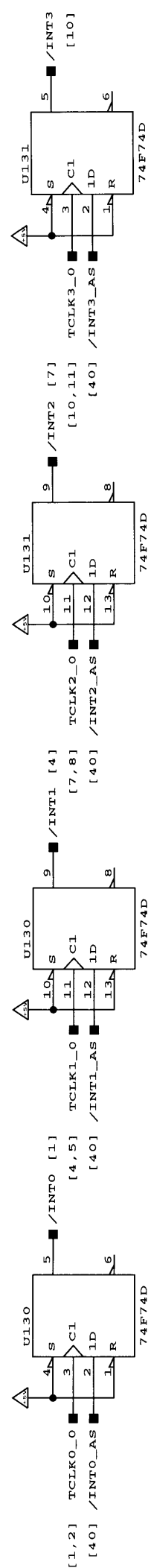
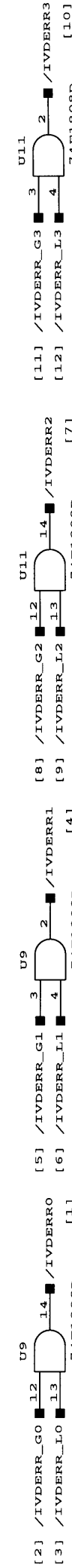
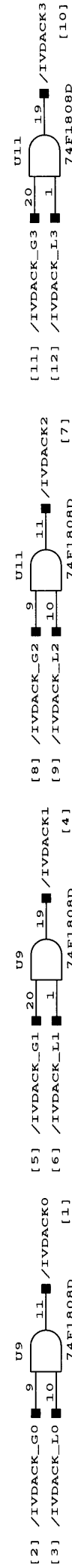
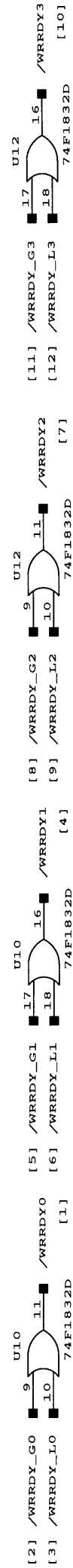
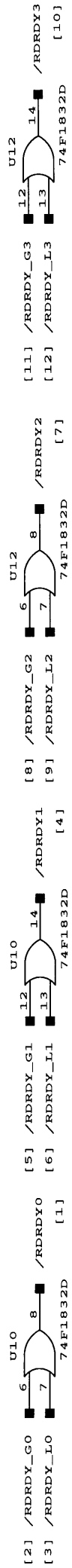
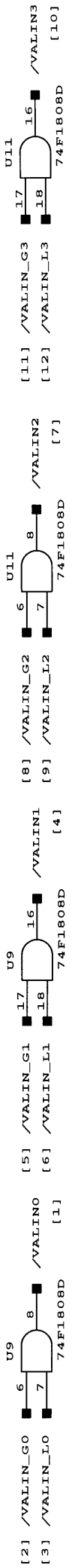
[20,21]

[1,4,7,10]

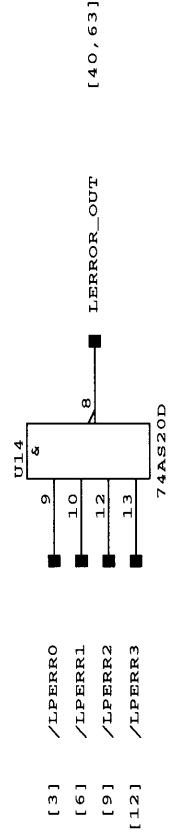
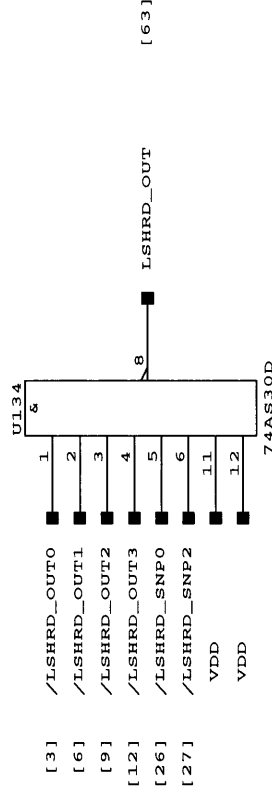
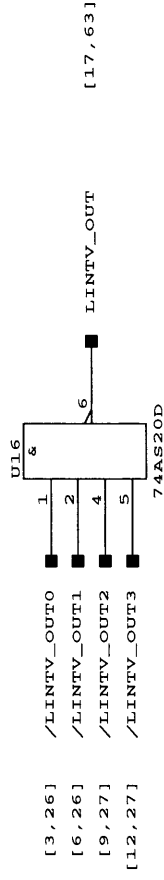
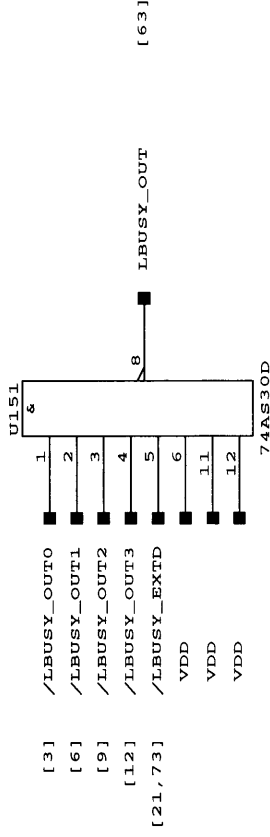
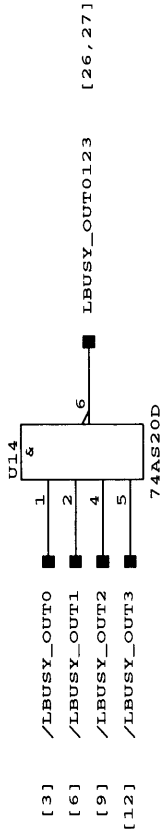
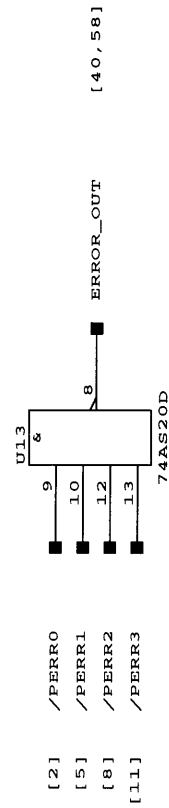
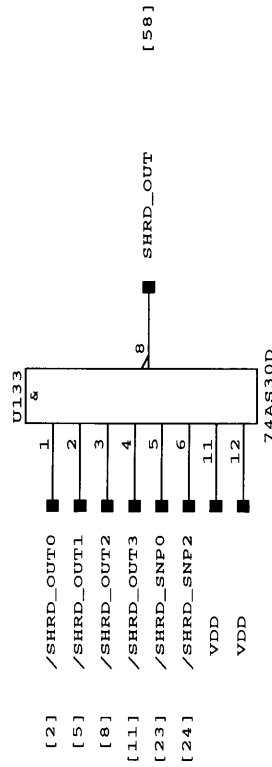
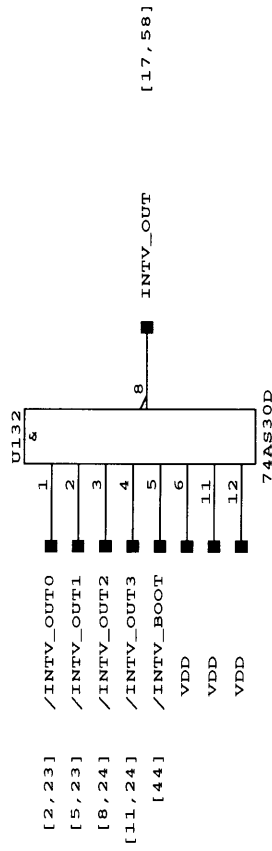
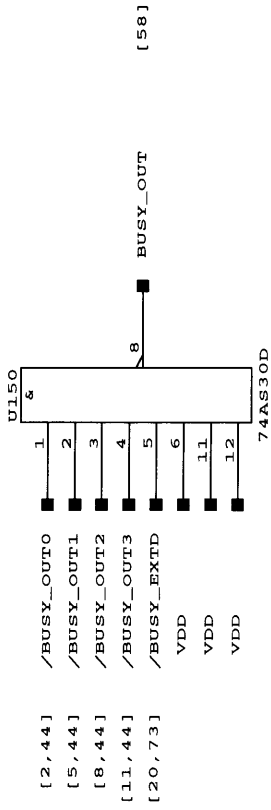
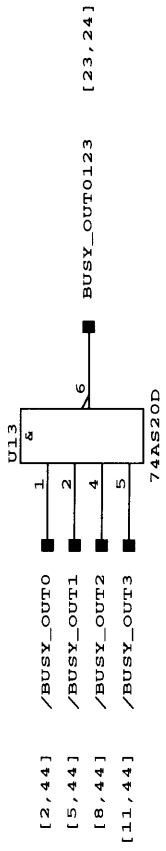
[1,4,7,10]



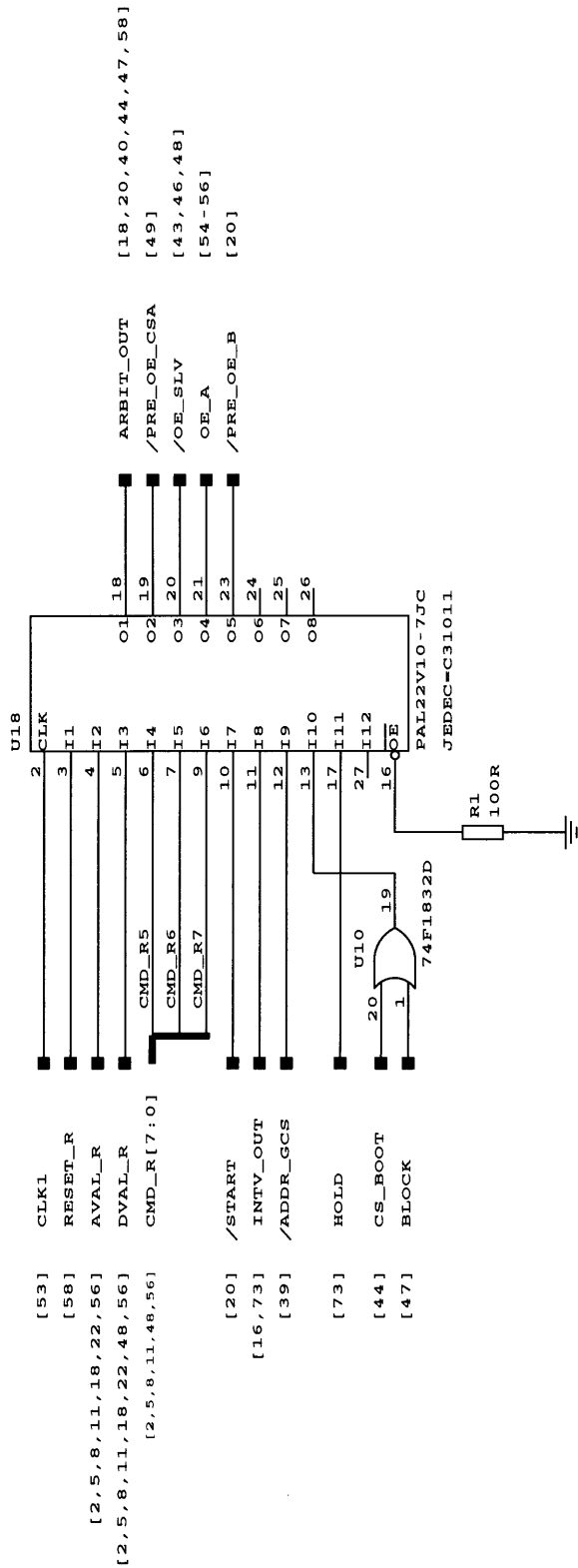
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Reset counters	
Issue 2			
Issue 3			



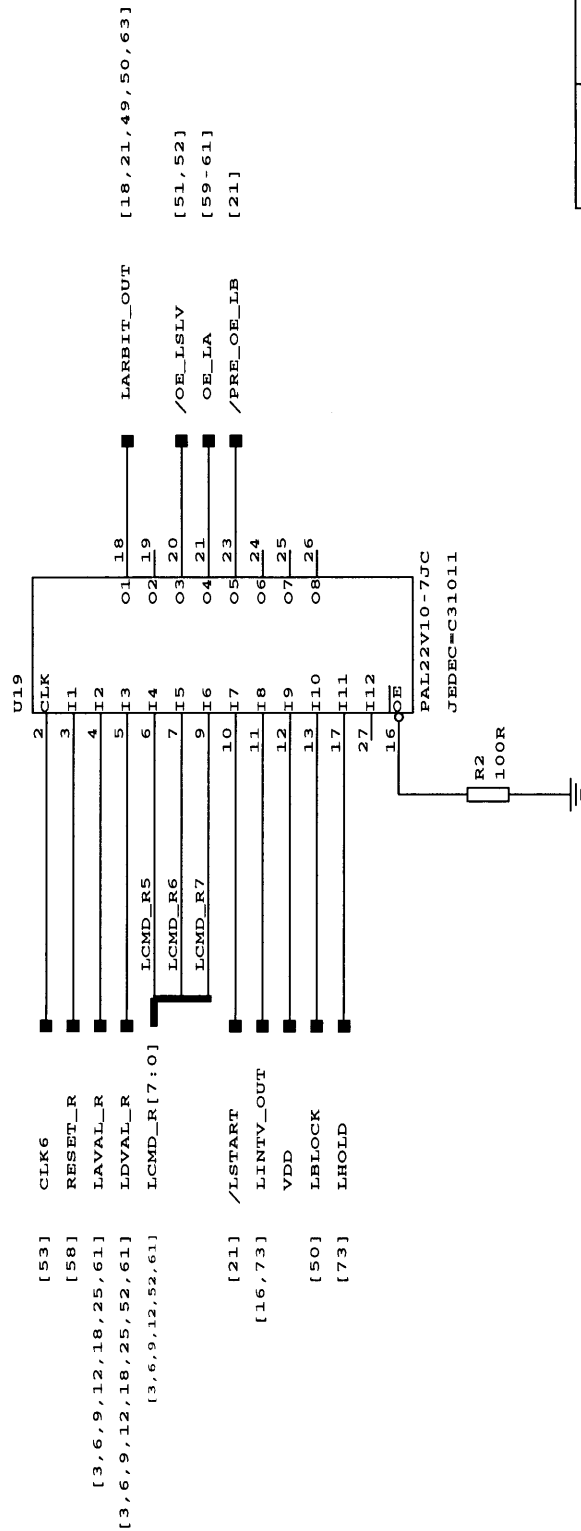
dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Gating towards processors	
Issue 2			
Issue 3			
		File: cpu301	Page: 15 of 73



dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Gating towards system bus	
Issue 2			
Issue 3			
	File: cpu301	Page: 16 of 73	

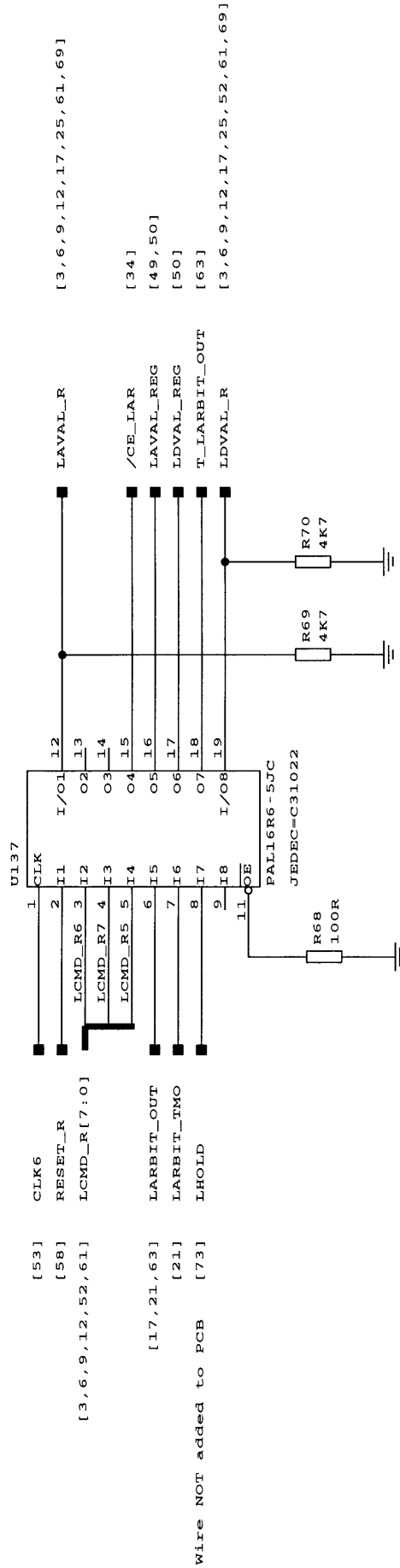
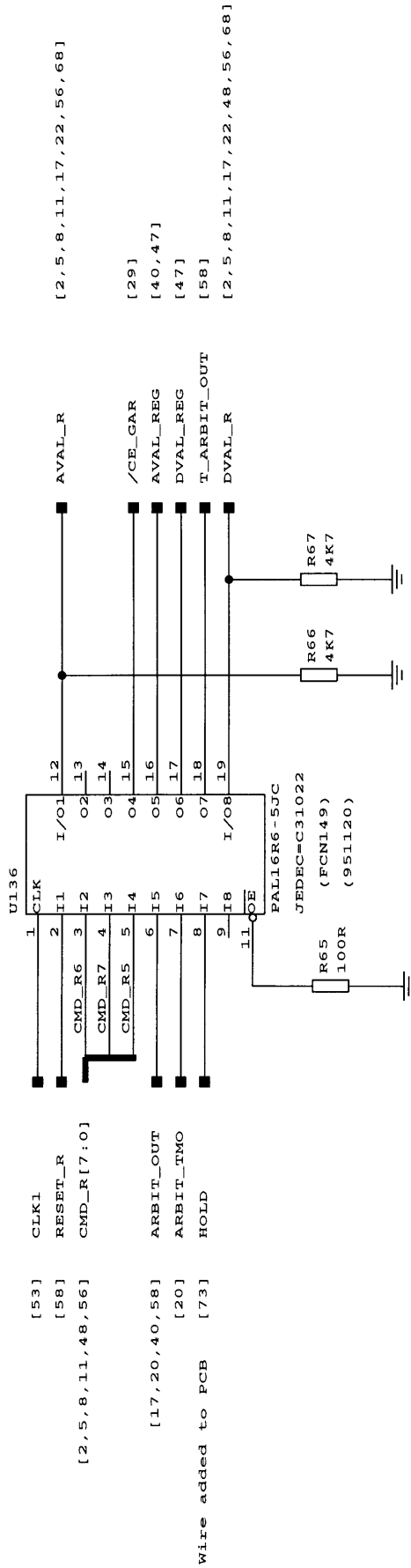


[53] CLK1
 [58] RESET_R
 [2,5,8,11,18,22,56] AVAL_R
 [2,5,8,11,18,22,48,56] DVAL_R
 [2,5,8,11,48,56] CMD_R[7:0]
 [20] /START
 [16,73] INTV_OUT
 [39] /ADDR_GCS
 [73] HOLD
 [44] CS_BOOT
 [47] BLOCK

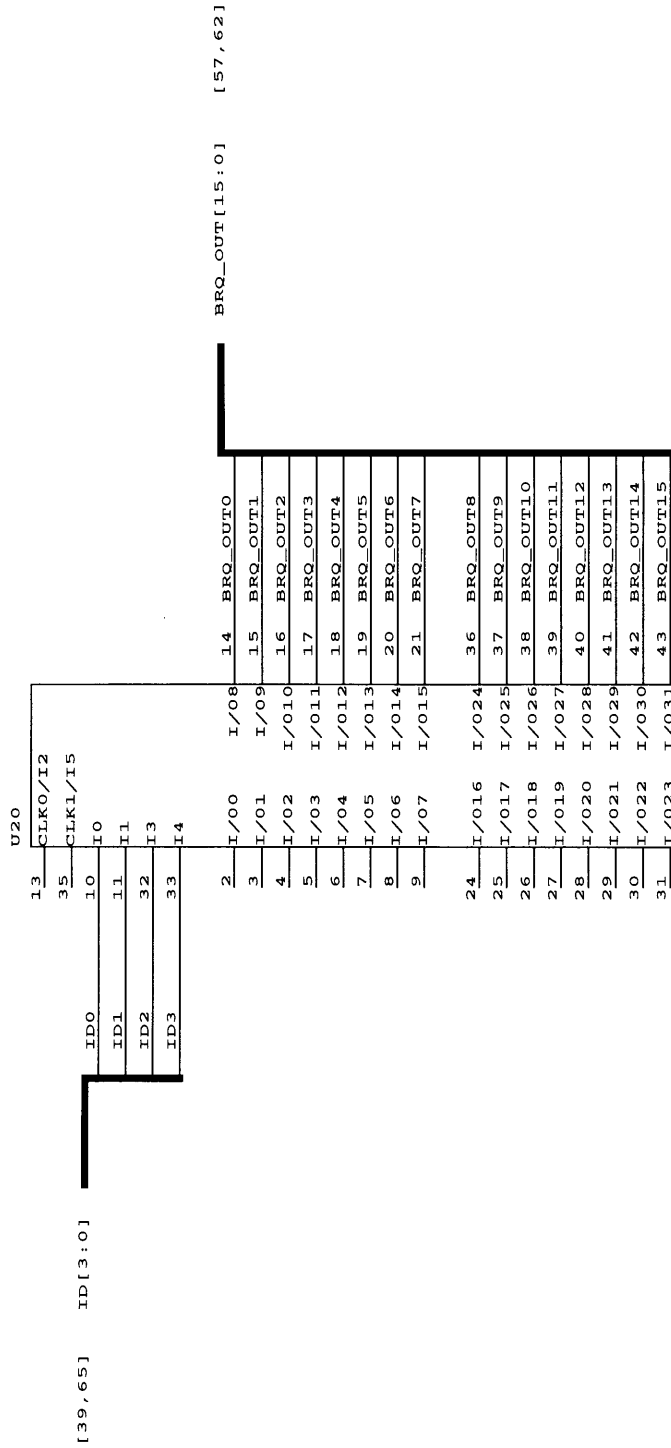


[53] CLK6
 [58] RESET_R
 [3,6,9,12,18,25,61] LAVAL_R
 [3,6,9,12,18,25,52,61] LDVAL_R
 [3,6,9,12,52,61] LCMD_R[7:0]
 [21] /LSTART
 [16,73] LINTV_OUT
 [50] LBLOCK
 [73] LHOLD

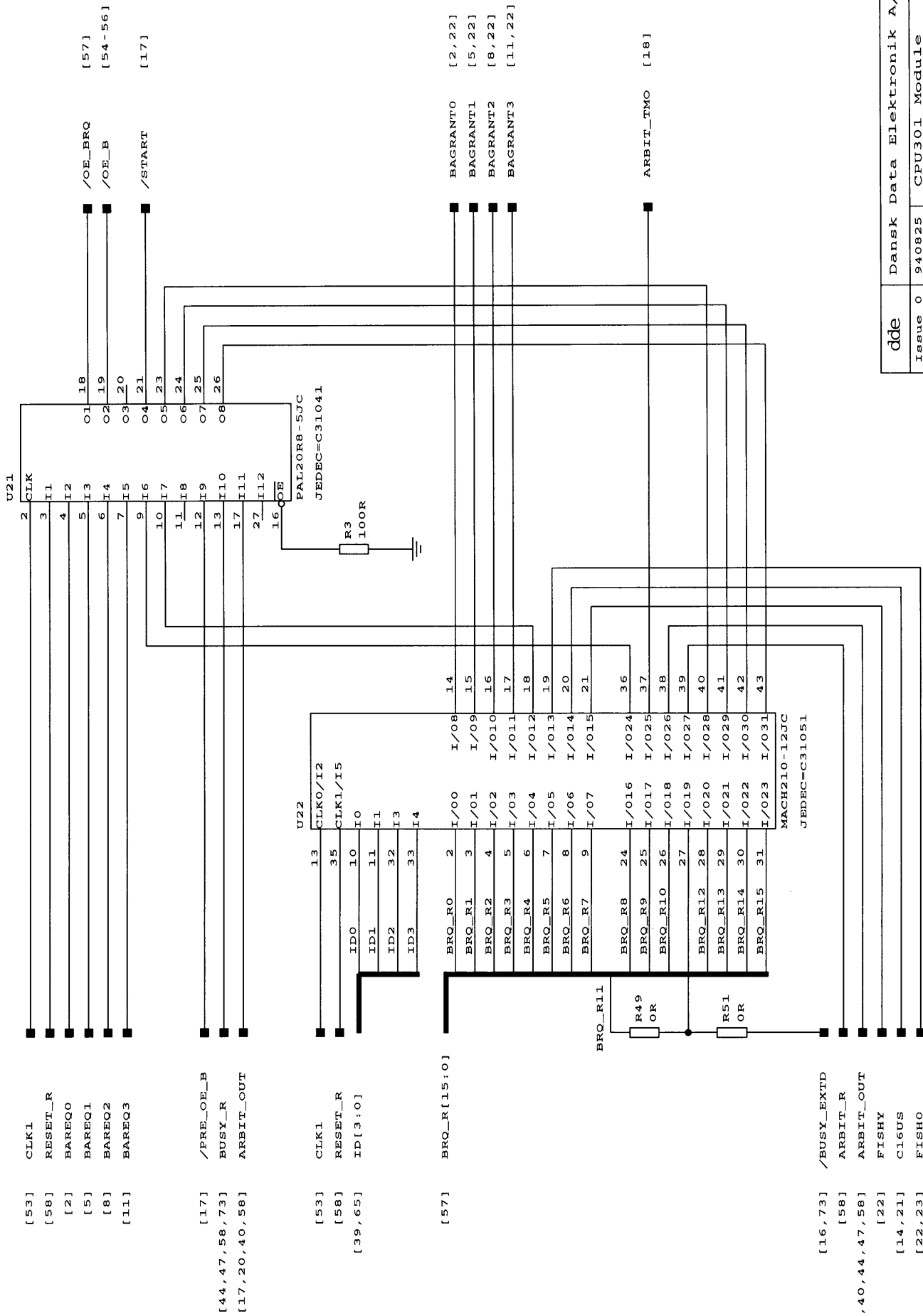
dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global and local	
Issue 2		output enable control	
Issue 3		File:	cpu301 Page:17 of 73



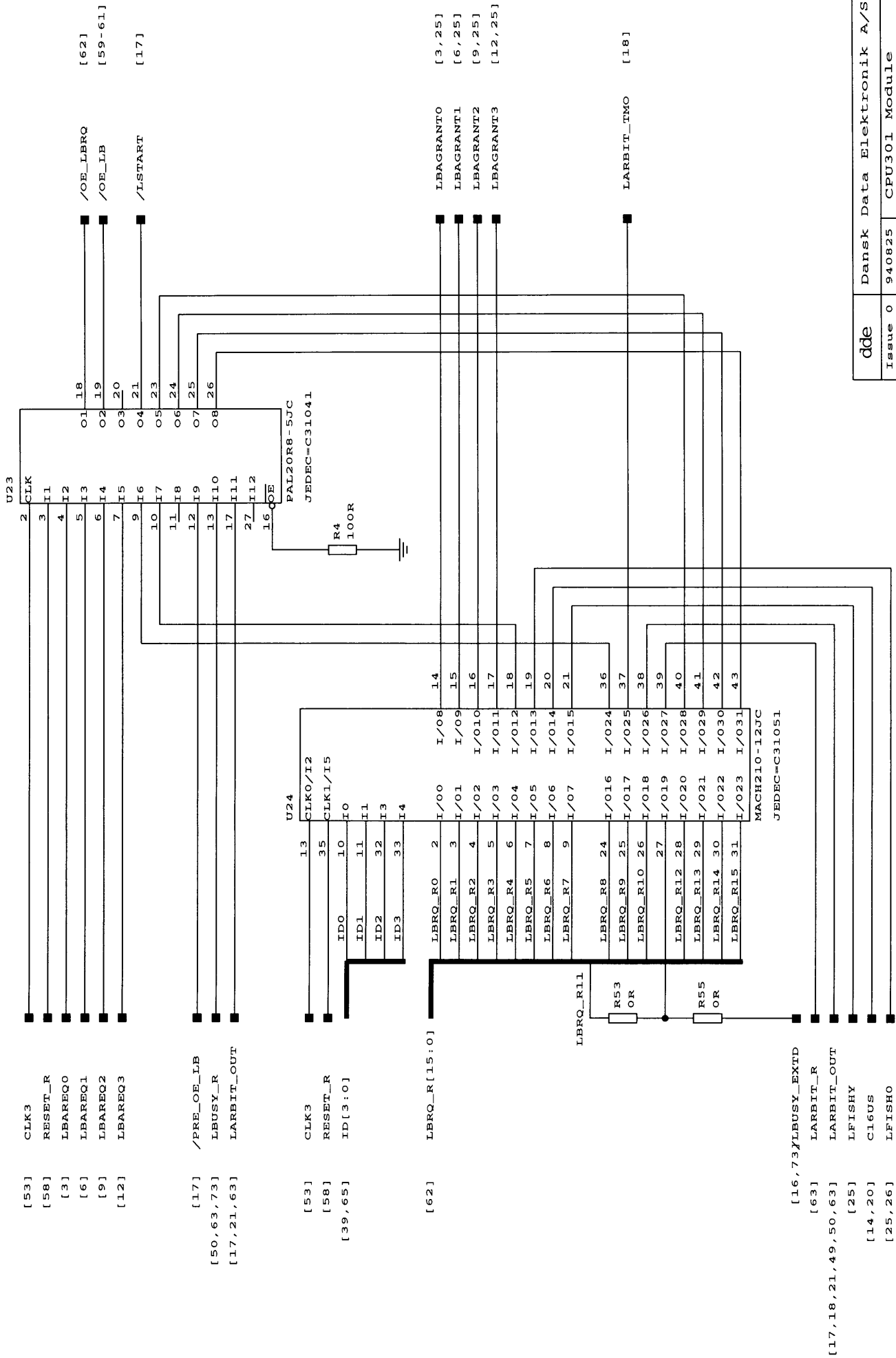
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1	950131	Pull-down for
Issue 2		address and data valid
Issue 3		File: cpu301



dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global and local bus request decoder	
Issue 2			
Issue 3		File: cpu301 Page:19 of 73	



dde	Dansk Data Elektronik A/S
Issue 0	940825
Issue 1	950131
Issue 2	
Issue 3	
CPU301 Module	
Global bus arbitration	
File:	cpu301
Page:	20 of 73



U23

2 CLK

3 I1

4 I2

5 I3

6 I4

7 I5

9 I6

10 I7

11 I8

12 I9

13 I10

17 I11

27 I12

16 OE

PAL20R8-5JC

JEDEC=C31041

R4

100R

01 /OE_LBRQ [62]

02 /OE_LB [59-61]

04 /LSTART [17]

[53] CLK3

[58] RESET_R

[3] LBAREQ0

[6] LBAREQ1

[9] LBAREQ2

[12] LBAREQ3

[17] /PRE_OE_LB

[50,63,73] LBARREQ1

[17,21,63] LBARREQ2

U24

13 CLK0/I2

35 CLK1/I5

10 ID0

11 ID1

32 ID2

33 ID3

14 ID4

2 I/00

3 I/01

4 I/02

5 I/03

6 I/04

7 I/05

8 I/06

9 I/07

24 I/016

25 I/017

26 I/018

27 I/019

28 I/020

29 I/021

30 I/022

31 I/023

MACH210-12JC

JEDEC=C31051

[53] CLK3

[58] RESET_R

ID[3:0]

[62] LBRQ_R[15:0]

LBRO_R0

LBRO_R1

LBRO_R2

LBRO_R3

LBRO_R4

LBRO_R5

LBRO_R6

LBRO_R7

LBRO_R8

LBRO_R9

LBRO_R10

LBRO_R11

LBRO_R12

LBRO_R13

LBRO_R14

LBRO_R15

R53 OR

R55 OR

[16,73] LBRQ_R[15:0]

[63] LARBIT_TMO

[25] LBARREQ1

[14,20] LBARREQ2

[25,26] LBARREQ3

LBAGRANT0 [3,25]

LBAGRANT1 [6,25]

LBAGRANT2 [9,25]

LBAGRANT3 [12,25]

LARBIT_TMO [18]

[16,73] LBRQ_R[15:0]

[63] LARBIT_TMO

[25] LBARREQ1

[14,20] LBARREQ2

[25,26] LBARREQ3

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local bus arbitration	
Issue 2			
Issue 3			
	File: cpu301	Page: 21 of 73	

[28,40,44,47]
 [2,5,8,11,58]
 [28,40,47]
 [28,47]
 [28,47]

GCR6
 SHRD_R
 GCR5
 GCR4
 GCR3

U138

[53]
 [58]
 [20]
 [20]
 [20]
 [20]

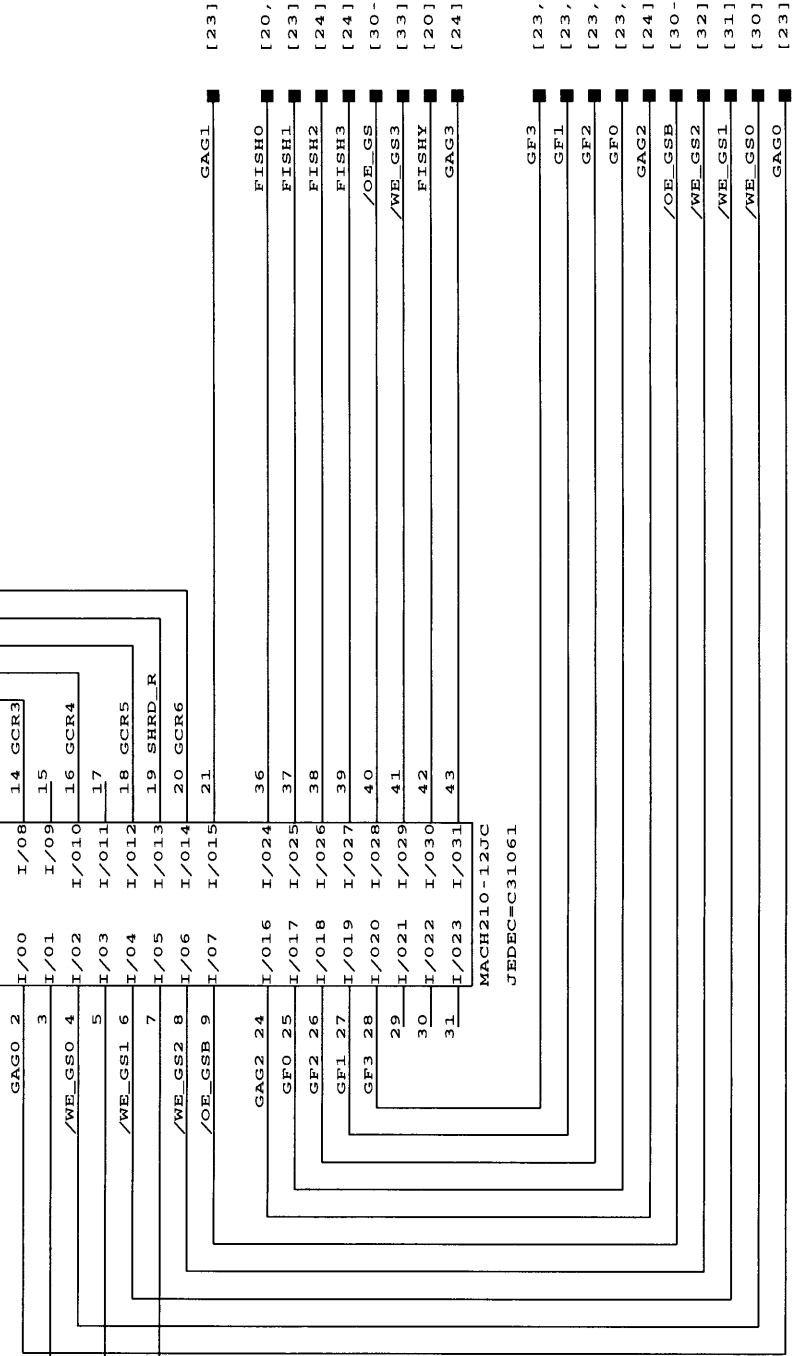
CLK1 13 CLK0/I2
 RESET_R 35 CLK1/I5
 BAGRANT0 I0 I0
 BAGRANT1 I1 I1
 BAGRANT2 I3 I3
 BAGRANT3 I4 I4

[2,5,8,11,17,18,56,68]
 [2,5,8,11,17,18,48,56,68]

AVAL_R
 DVAL_R

[28,40,44,47]

GCR7



[29, 40]
GAR[35:3]
[29]
GAR[21:20]A

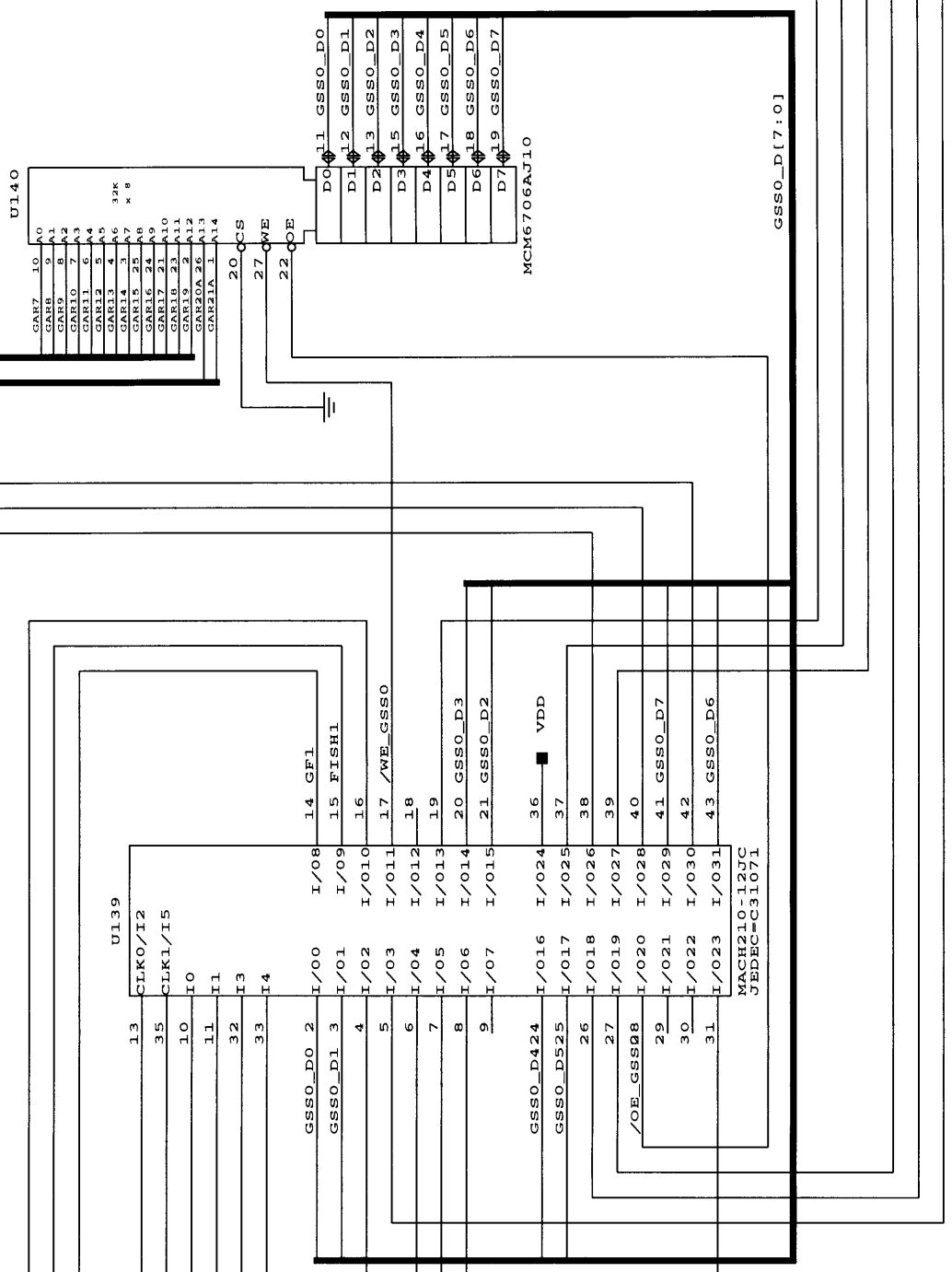
[2, 16, 73]
[5, 16, 73]
[22, 24]
/INTV_OUTO
/INTV_OUT1
GF3

[16, 24]
[22]
[22, 24]
BUSY_OUTO123
FISH1
GFI

[53]
[58]
[30]
[30]
[31]
[31]
CLK1
RESET_R
/HIT_GS01
/HIT_GS00
/HIT_GS11
/HIT_GS10

[22]
[22]
[20, 22]
GFI
GAG1
GAGO
FISHO

[22, 24]
GFI



SNPHIT1 [5]
HOLDO [73]
/SHRD_SNP0 [16]
TURN [24]
HOLD1 [73]
SNPHITO [2]

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global Super Snooper 0-1	
Issue 2			
Issue 3			
		File: cpu301	Page: 23 of 73

GAR[35:3]

GAR[21:20]A

/INTV_OUT2

/INTV_OUT3

GF3

TURN

BUSY_OUT0123

FISH3

GF1

CLK1

RESET_R

/HIT_GS21

/HIT_GS20

/HIT_GS31

/HIT_GS30

[29, 40]

[29]

[8, 16, 73]

[11, 16, 73]

[22, 23]

[23]

[16, 23]

[22]

[22, 23]

[53]

[58]

[32]

[32]

[33]

[33]

[22, 23]

[22]

[22]

[22]

[22, 23]

U142

GAR7 10 A0
 GAR8 9 A1
 GAR9 8 A2
 GAR10 7 A3
 GAR11 6 A4
 GAR12 5 A5
 GAR13 4 A6
 GAR14 3 A7
 GAR15 2 A8
 GAR16 25 A9
 GAR17 21 A10
 GAR18 23 A11
 GAR19 2 A12
 GAR20 2 A13
 GAR21 1 A14

20 CCS

27 OWE

22 OOE

D0 11 GSS1_D0
 D1 12 GSS1_D1
 D2 13 GSS1_D2
 D3 15 GSS1_D3
 D4 16 GSS1_D4
 D5 17 GSS1_D5
 D6 18 GSS1_D6
 D7 19 GSS1_D7

MCM6706AJ10

GSS1_D[7:0]

U141

13 CLK0/I2
 35 CLK1/I5
 10 IO
 11 I1
 32 I3
 33 I4

GSS1_D0 2 I/00

GSS1_D1 3 I/01

4 I/02

5 I/03

6 I/04

7 I/05

8 I/06

9 I/07

GSS1_D4 24 I/016

GSS1_D5 25 I/017

26 I/018

27 I/019

/OE_GSS1 28 I/020

29 I/021

30 I/022

31 I/023

MACH210-12JC
JEDEC-C31071

14 CF1

15 FISH3

16

17 /WE_GSS1

18

19

20 GSS1_D3

21 GSS1_D2

36

37

38

39

40

41 GSS1_D7

42

43 GSS1_D6

SNPHIT3 [11]

HOLD2 [73]

/SHRD_SNP2 [16]

HOLD3 [73]

SNPHIT2 [8]

dde

Dansk Data Elektronik A/S

Issue 0 940825 CPU301 Module

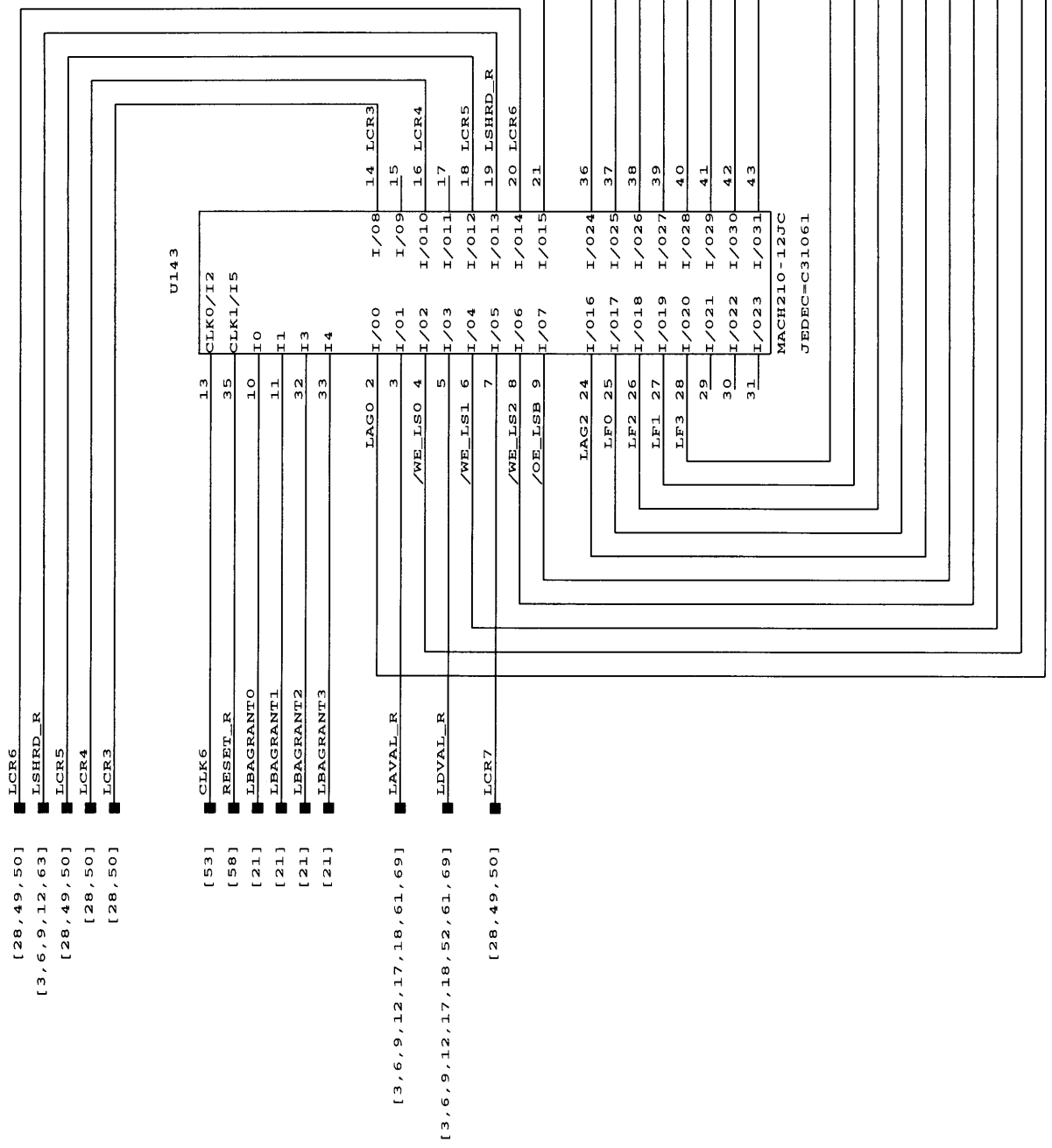
Issue 1 950131 Global Super Snooper 2-3

Issue 2

Issue 3

File: cpu301

Page: 24 of 73



[28,49,50]

[3,6,9,12,63]

[28,49,50]

[28,50]

[28,50]

[53]

[58]

[21]

[21]

[21]

[21]

[3,6,9,12,17,18,61,69]

[3,6,9,12,17,18,52,61,69]

[28,49,50]

[34] LAR[35:3]

[34] LAR[21:20]A

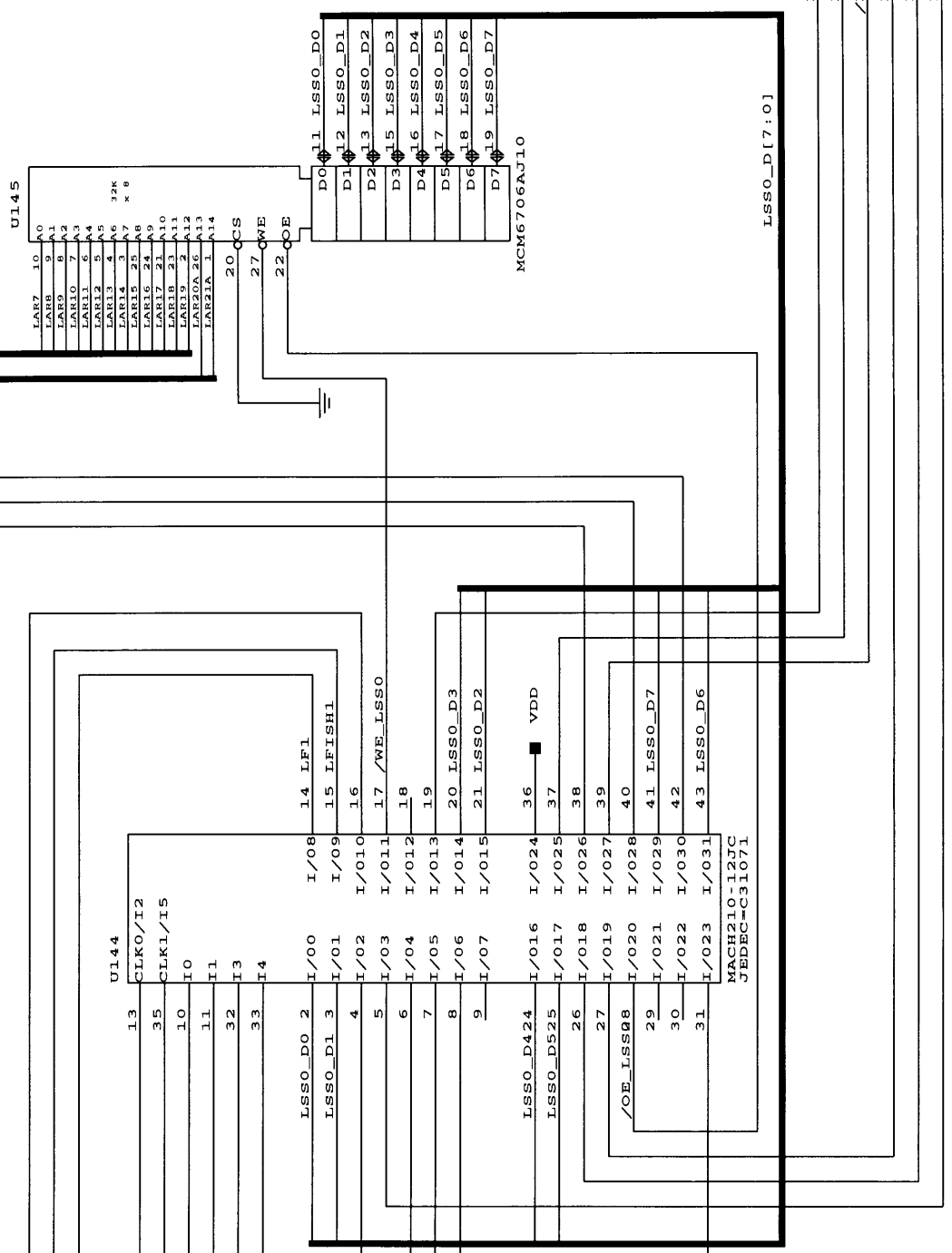
[3,16,73] /LINTV_OUT0
[6,16,73] /LINTV_OUT1
[25,27] LF3

[16,27] LBUSY_OUT0,1,2,3
[25] LFI5H1
[25,27] LFI1

[53] CLK6
[58] RESET_R
[35] /HIT_LS01
[35] /HIT_LS00
[36] /HIT_LS11
[36] /HIT_LS10

[25,27] LFO
[25] LAG1
[25] LAGO
[21,25] LFI5H0

[25,27] LF2



LSNPHIT1 [6]
 LHOLDO [73]
 /LSHRD_SNPO [16]
 LTURN [27]
 LHOLD1 [73]
 LSNPHITO [3]

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local Super Snooper 0-1	
Issue 2			
Issue 3			
	File: cpu301	Page:26 of 73	

LAR[35:3]

[34]

LAR[21:20]A

[34]

/LINTV_OUT2

[9,16,73]

/LINTV_OUT3

[12,16,73]

LF3

[25,26]

LTURN

[26]

LBUSY_OUT0,1,2,3

[16,26]

LFISH3

[25]

LF1

[25,26]

CLK6

U146

[53]

CLKO/I2

RESET_R

35 CLKI/I5

[58]

/HIT_LS21

10 IO

[37]

/HIT_LS20

11 I1

[37]

/HIT_LS31

32 I3

[38]

/HIT_LS30

33 I4

[38]

LFO

LSS1_D0 2 I/00

[25,26]

LSS1_D1 3 I/01

14 LF1

[25,26]

LSS1_D2 4 I/02

15 LFISH3

[25,26]

LSS1_D3 5 I/03

16 I/010

[25,26]

LSS1_D4 6 I/04

17 /WE_LSS1

[25,26]

LSS1_D5 7 I/05

18

[25]

LSS1_D6 8 I/06

19 I/013

[25]

LSS1_D7 9 I/07

20 LSS1_D3

[25]

LSS1_D8 24 I/016

21 LSS1_D2

[25]

LSS1_D9 25 I/017

36

[25]

LSS1_D10 26 I/018

37

[25]

LSS1_D11 27 I/019

38

[25]

LSS1_D12 28 I/020

39

[25]

LSS1_D13 29 I/021

40

[25]

LSS1_D14 30 I/022

41 LSS1_D7

[25]

LSS1_D15 31 I/023

42

[25]

LSS1_D16 31 I/023

43 LSS1_D6

[25,26]

LSS1_D17 31 I/023

43 LSS1_D6

[25,26]

LSS1_D18 31 I/023

43 LSS1_D6

[25,26]

LSS1_D19 31 I/023

43 LSS1_D6

[25,26]

LSS1_D20 31 I/023

43 LSS1_D6

[25,26]

LSS1_D21 31 I/023

43 LSS1_D6

[25,26]

LSS1_D22 31 I/023

43 LSS1_D6

[25,26]

LSS1_D23 31 I/023

43 LSS1_D6

[25,26]

LSS1_D24 31 I/023

43 LSS1_D6

[25,26]

LSS1_D25 31 I/023

43 LSS1_D6

[25,26]

LSS1_D26 31 I/023

43 LSS1_D6

[25,26]

LSS1_D27 31 I/023

43 LSS1_D6

[25,26]

LSS1_D28 31 I/023

43 LSS1_D6

[25,26]

LSS1_D29 31 I/023

43 LSS1_D6

[25,26]

LSS1_D30 31 I/023

43 LSS1_D6

[25,26]

LSS1_D31 31 I/023

43 LSS1_D6

[25,26]

LSS1_D32 31 I/023

43 LSS1_D6

[25,26]

LSS1_D33 31 I/023

43 LSS1_D6

[25,26]

LSS1_D34 31 I/023

43 LSS1_D6

[25,26]

LSS1_D35 31 I/023

43 LSS1_D6

[25,26]

LSS1_D36 31 I/023

43 LSS1_D6

[25,26]

LSS1_D37 31 I/023

43 LSS1_D6

[25,26]

LSS1_D38 31 I/023

43 LSS1_D6

[25,26]

LSS1_D39 31 I/023

43 LSS1_D6

[25,26]

LSS1_D40 31 I/023

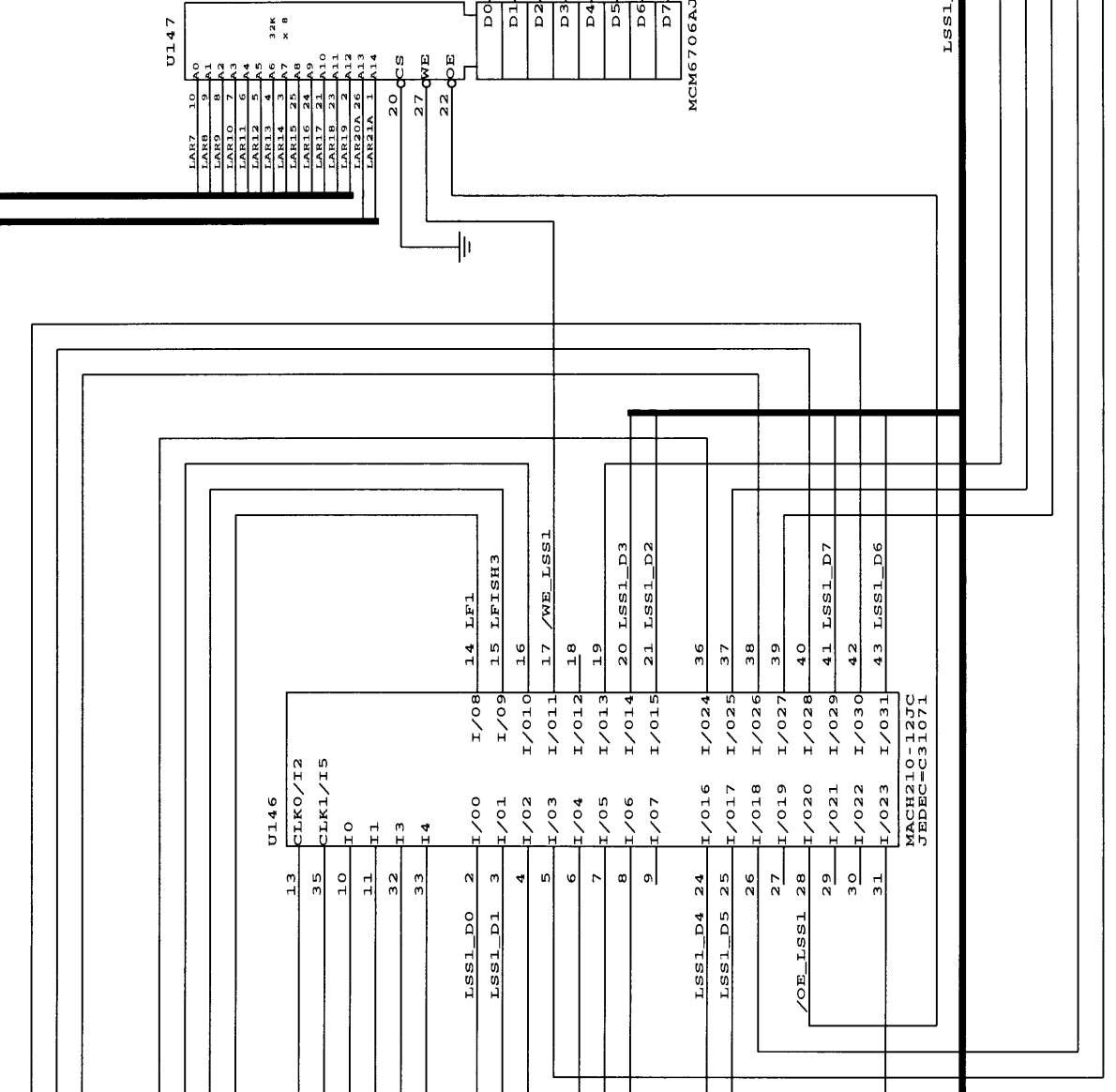
43 LSS1_D6

[25,26]

LSS1_D41 31 I/023

43 LSS1_D6

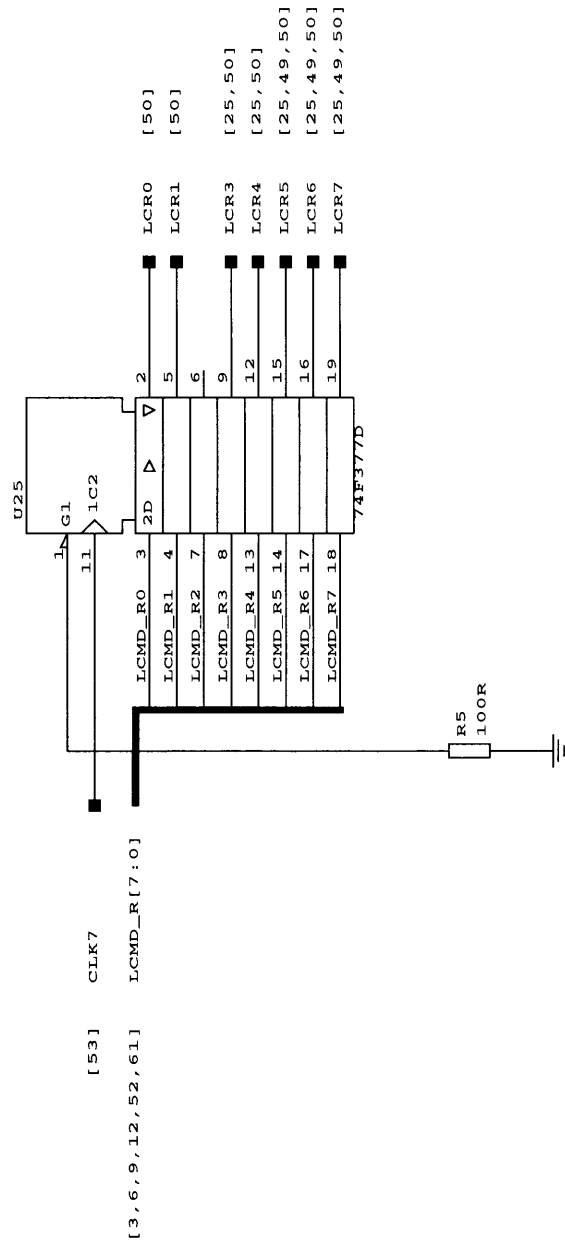
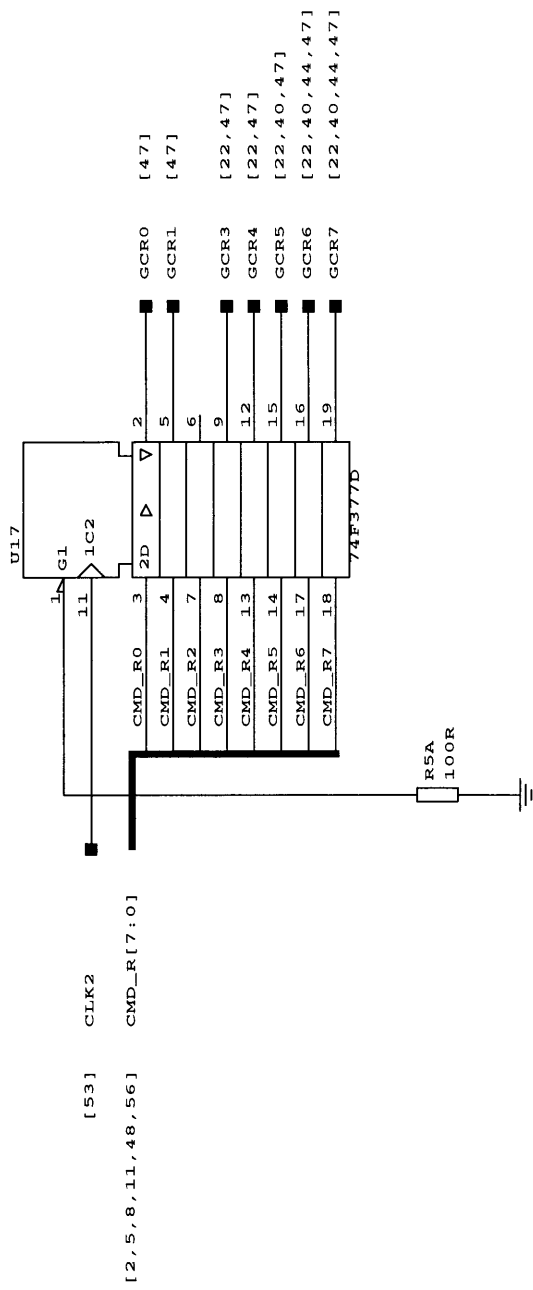
[25,26]



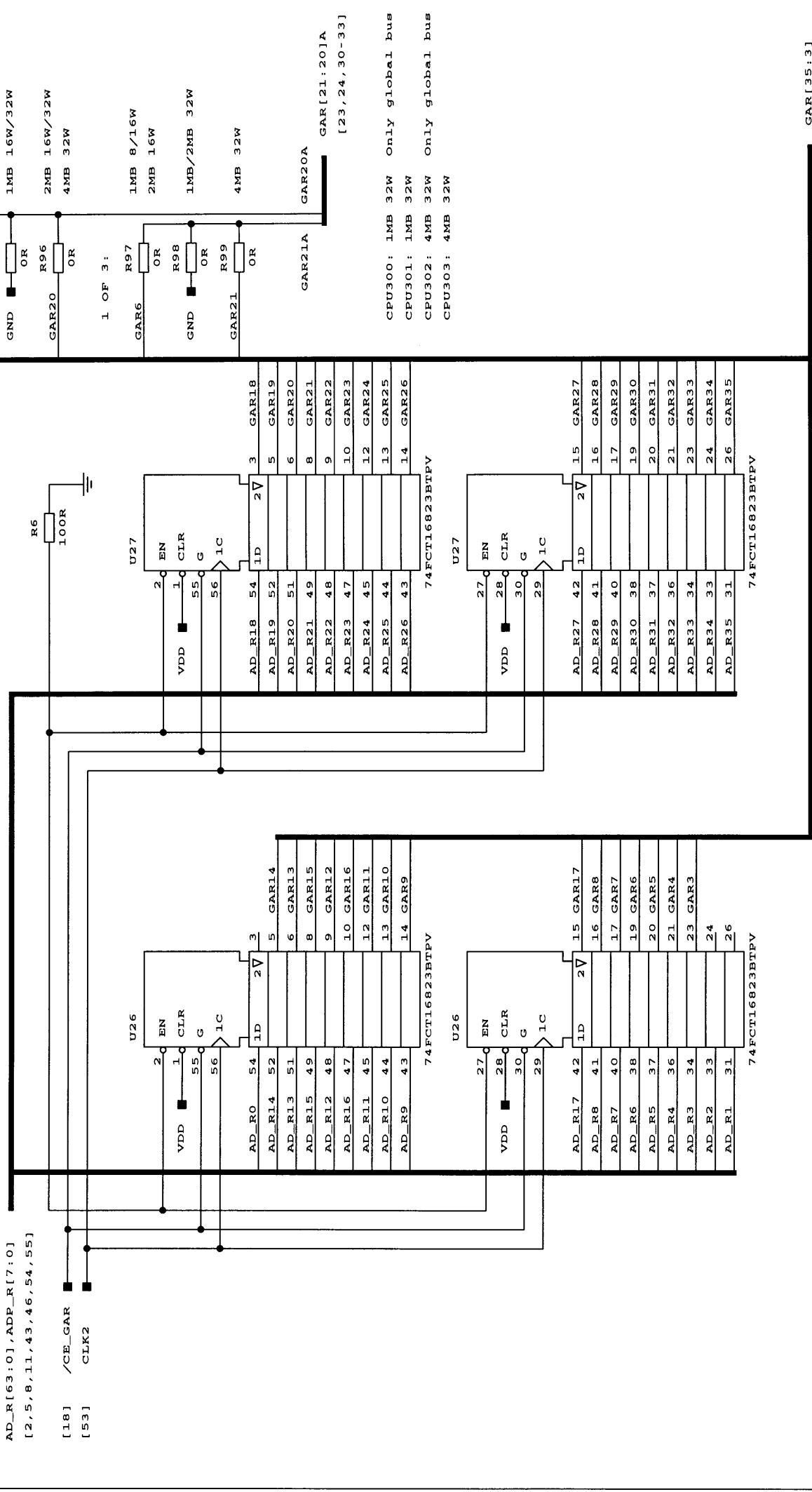
LSS1_D[7:0]

LSNPHIT3 [12]
 LHOLD2 [73]
 /LSHRD_SNP2 [16]
 LHOLD3 [73]
 LSNPHIT2 [9]

dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local Super Snooper 2-3	
Issue 2			
Issue 3			



dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global and local command register	
Issue 2			
Issue 3		File: cpu301	



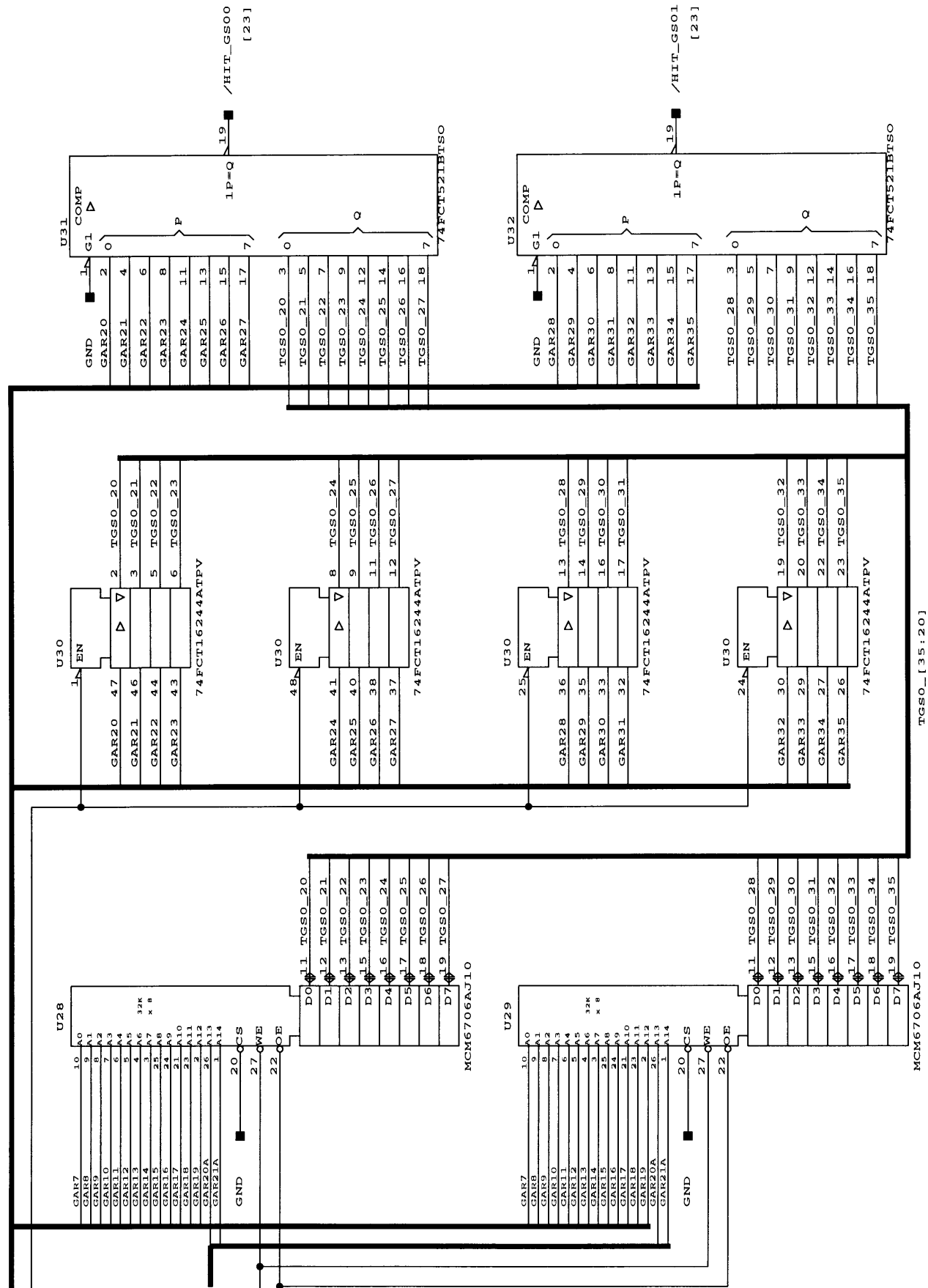
dde	Dansk Dede Elektronik A/S
Issue 0	940825 CPU301 Module
Issue 1	950131 Global address register
Issue 2	
Issue 3	File: cpu301 Page:29 of 73

[29, 40] GAR [35:3]
[22] /OE_GSB

[29] GAR [21:20]A

[22] /WE_GSO

[22] /OE_GS



TGSO_[35:20]

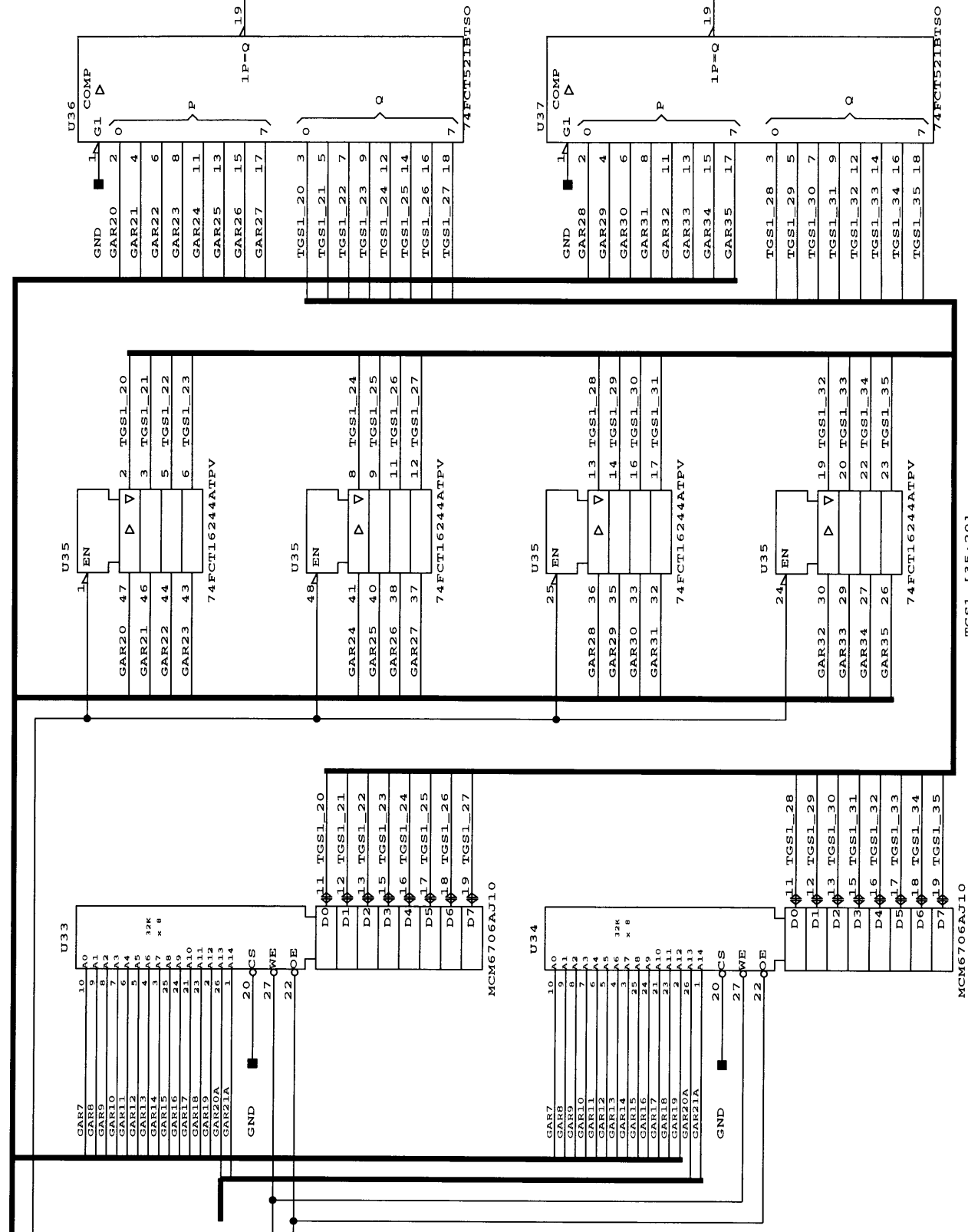
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global snocooper 0	
Issue 2			
Issue 3			
		File: cpu301	Page:30 of 73

[29, 40] GAR [35:3]
[22] /OE_GSB

[29] GAR [21:20]A

[22] /WE_GS1

[22] /OE_GS

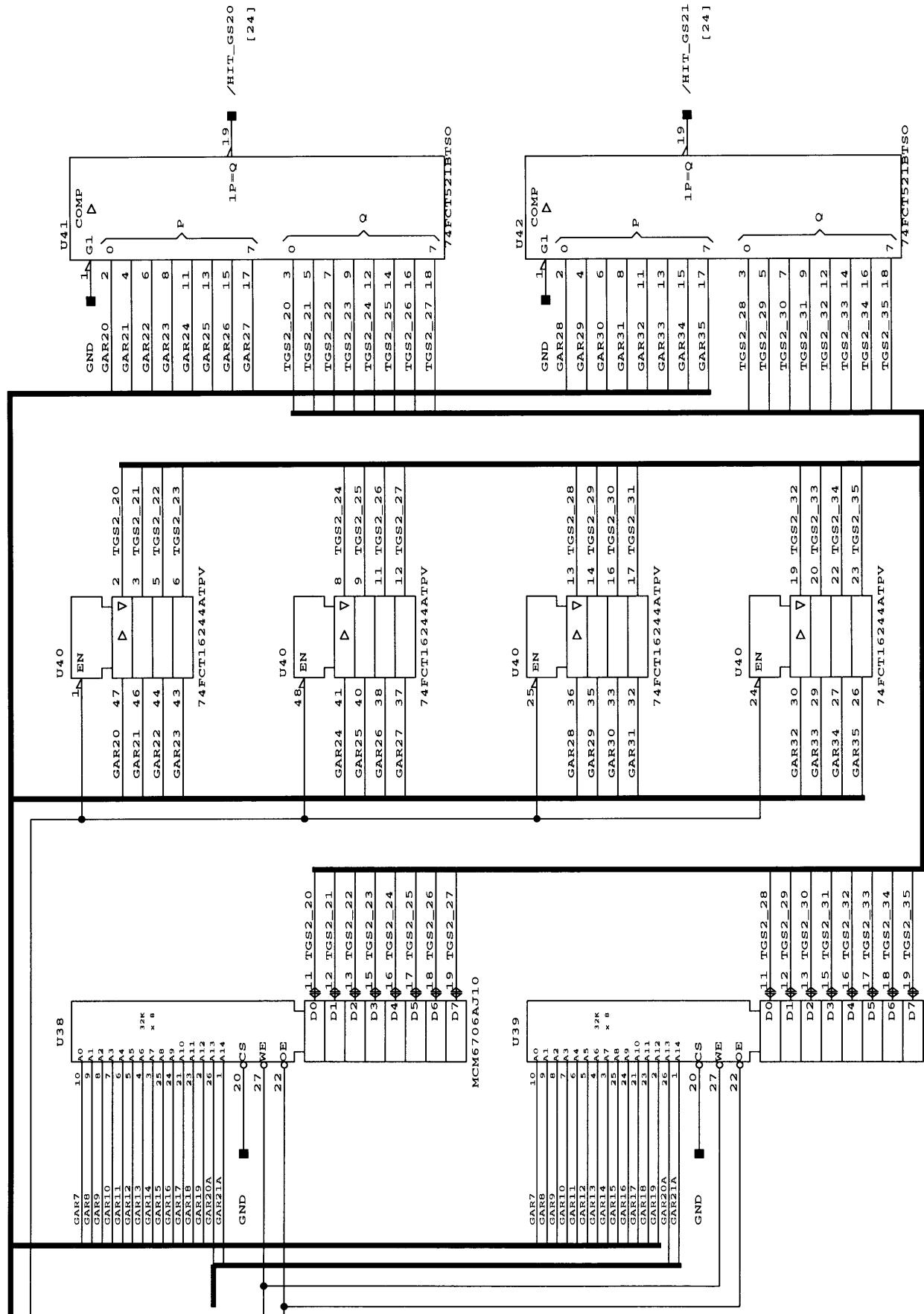


TGS1_[35:20]

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global snocooper 1	
Issue 2			
Issue 3			
	File:	cpu301	Page: 31 of 73

[29, 40] GAR[35:3]
[22] /OE_GSB

[29] GAR[21:20]A
[22] /WE_CS2
[22] /OE_CS



TGS2_[35:20]

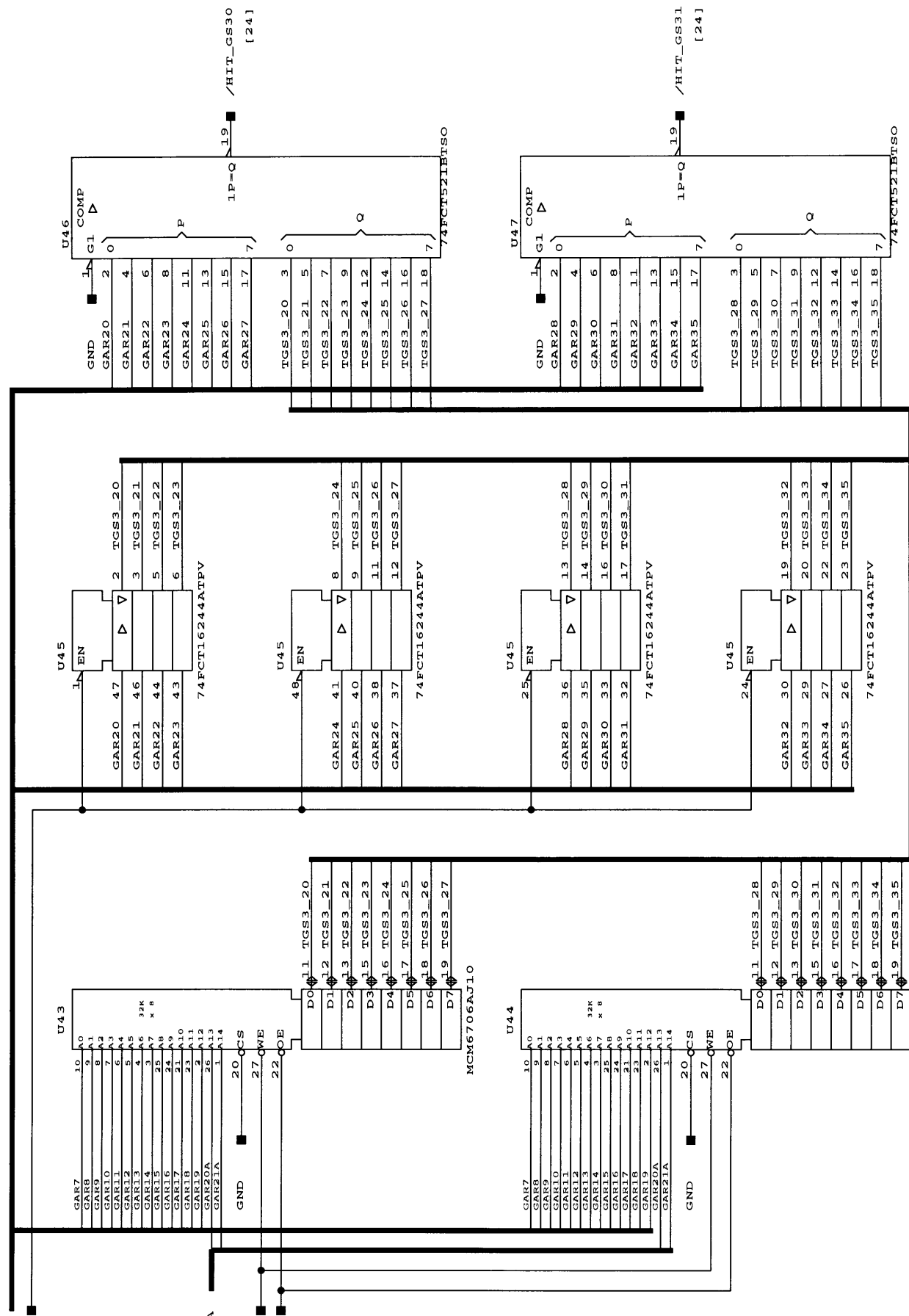
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global snocooper 2	
Issue 2			
Issue 3			
		File: cpu301	Page: 32 of 73

[29, 40] GAR [35:3]
[22] /OE_GSB

[29] GAR [21:20]A

[22] /WE_GS3

[22] /OE_GS

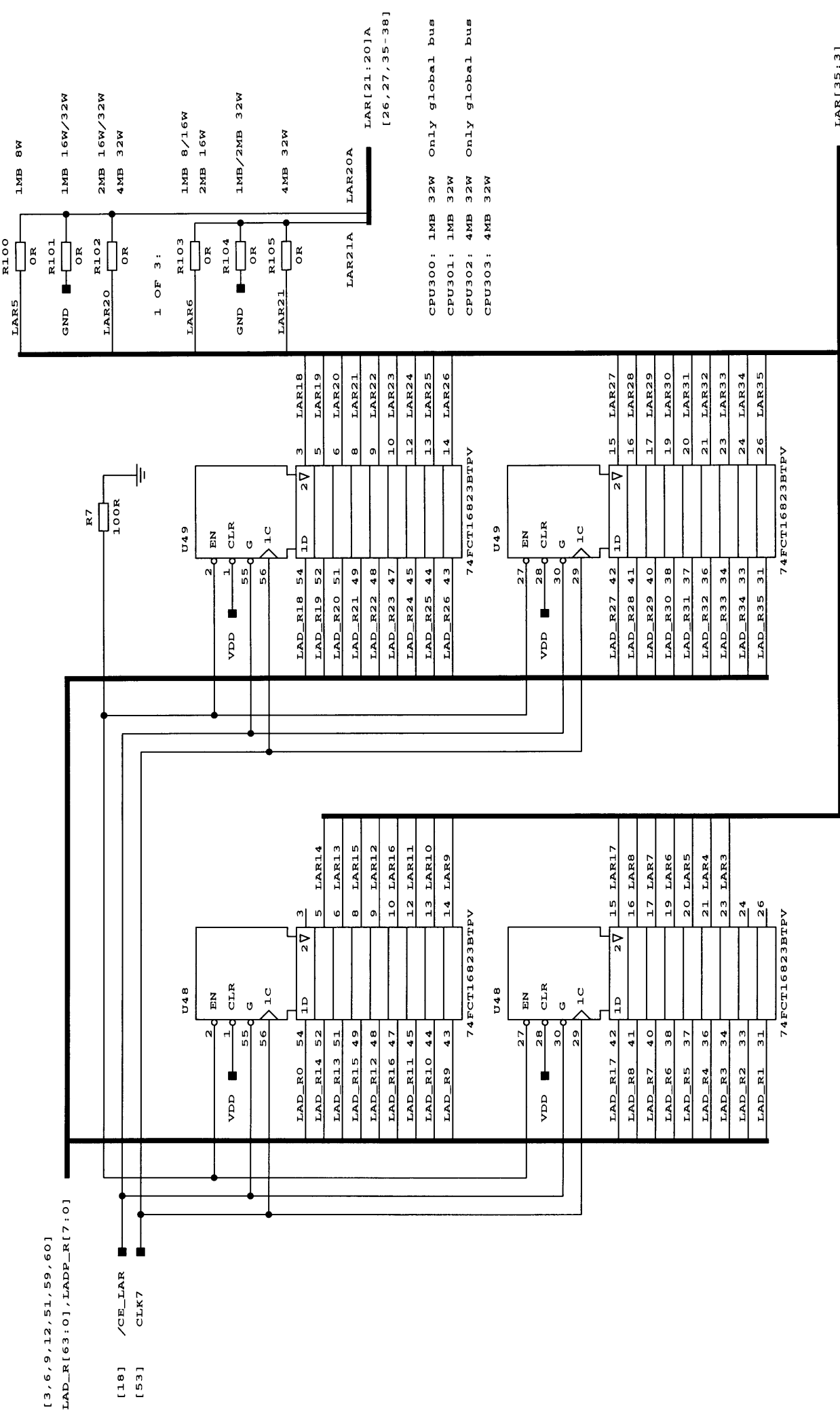


TGS3_ [35:20]

MCM6706AJ10

dde	Dansk Data Elektronik A/S
Issue 0	940825
Issue 1	950131
Issue 2	
Issue 3	
CPU301 Module	
Global sncooper 3	
File:	cpu301
Page:	33 of 73

1 OF 3: CACHE & BLOCK SIZE:



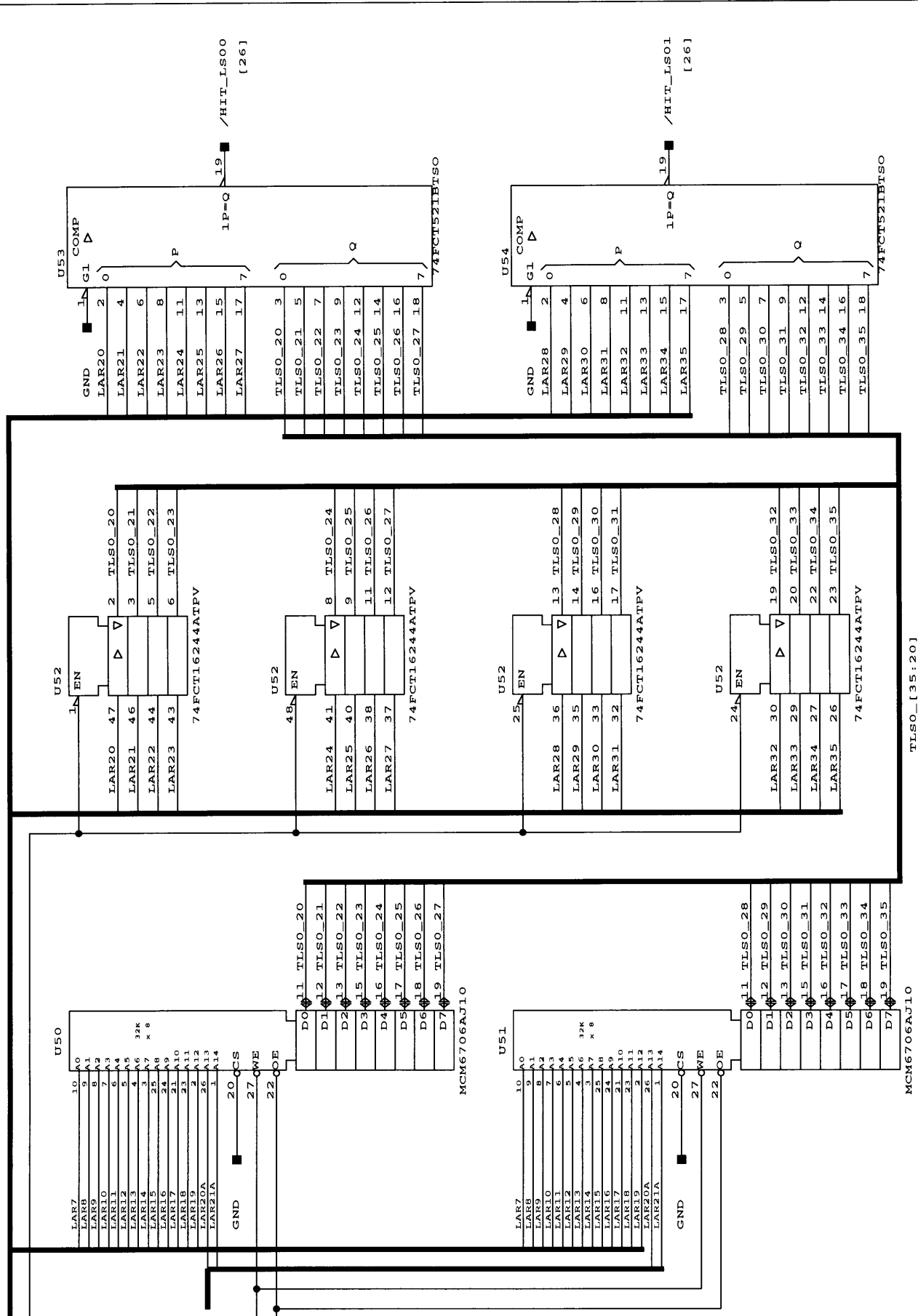
LAR[35:3] [26,27,35-38,49]

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local address register	
Issue 2			
Issue 3		File:	cpu301 page:34 of 73

[34] LAR[35:3]
 [25] /OE_LSB

[34] LAR[21:20]A

[25] /WE_LSO
 [25] /OE_US



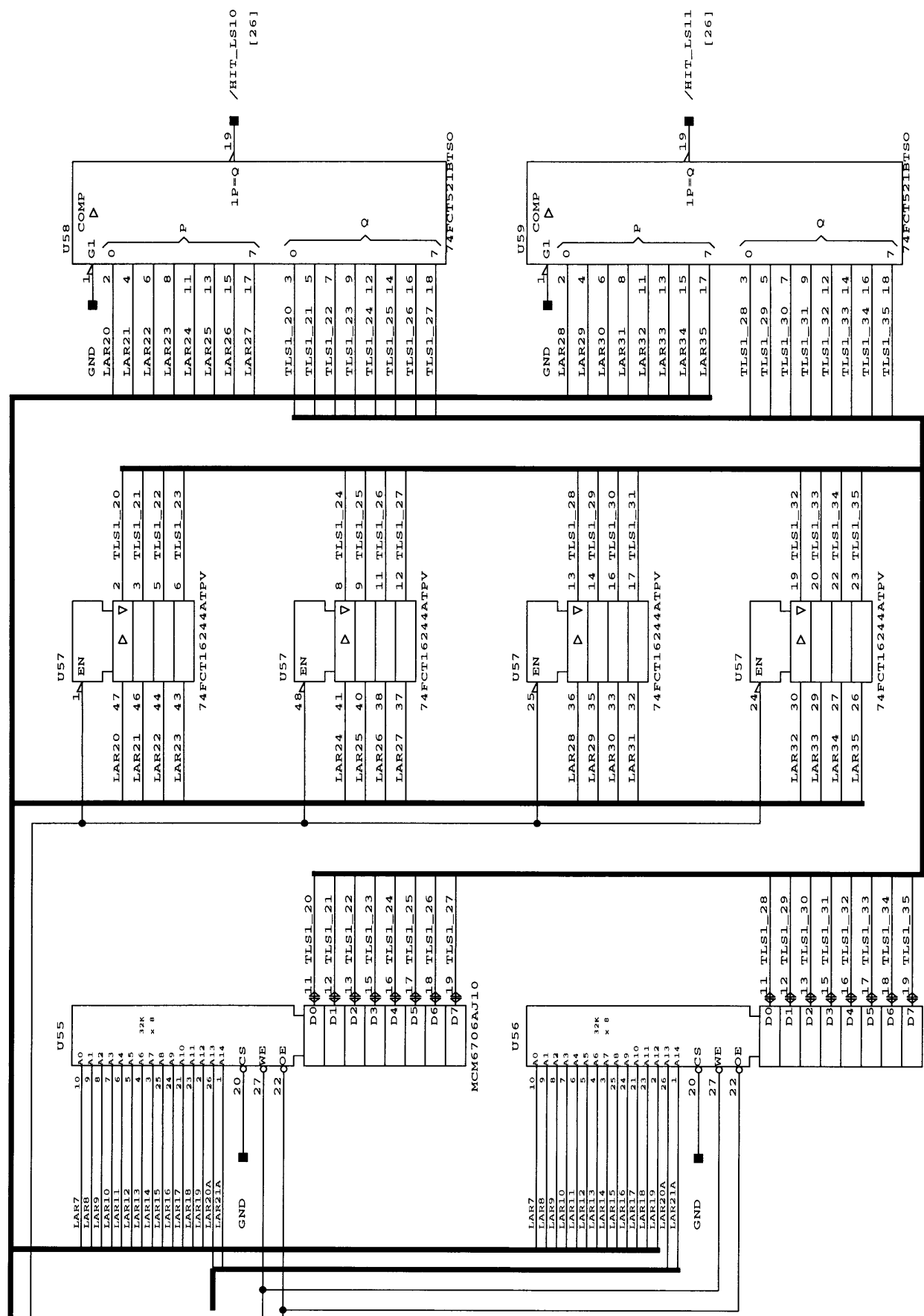
TLDO-[35:20]

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local snoooper 0	
Issue 2			
Issue 3		File: cpu301	Page:35 of 73

[34] LAR[35:3]
 [25] /OE_LSB

[34] LAR[21:20]A

[25] /WE_LSI1
 [25] /OE_LS



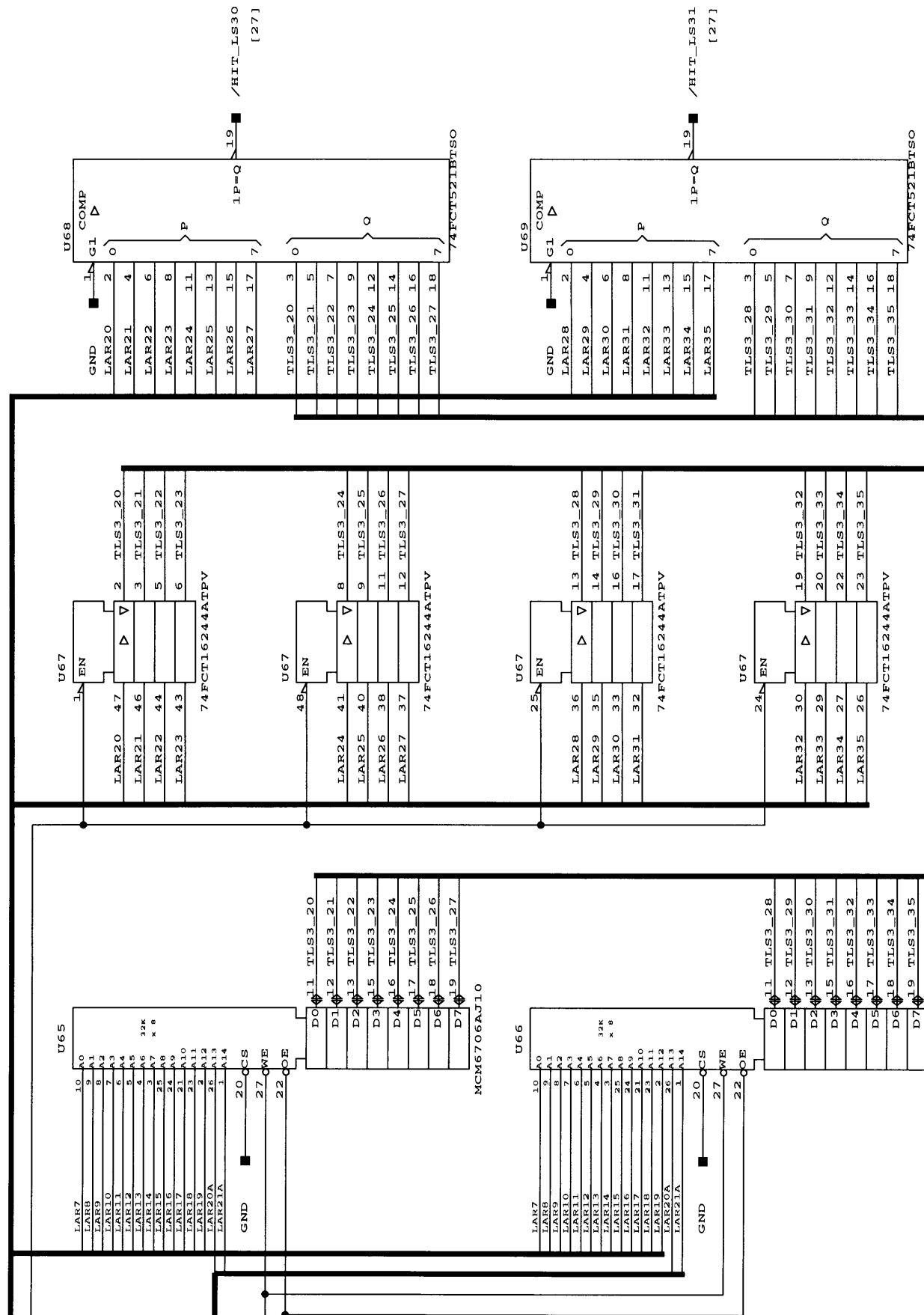
TLSL_[35:20]

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local snooper 1	
Issue 2			
Issue 3		File:	cpu301
			Page:36 of 73

[34] LAR[35:3]
 [25] /OE_LSB

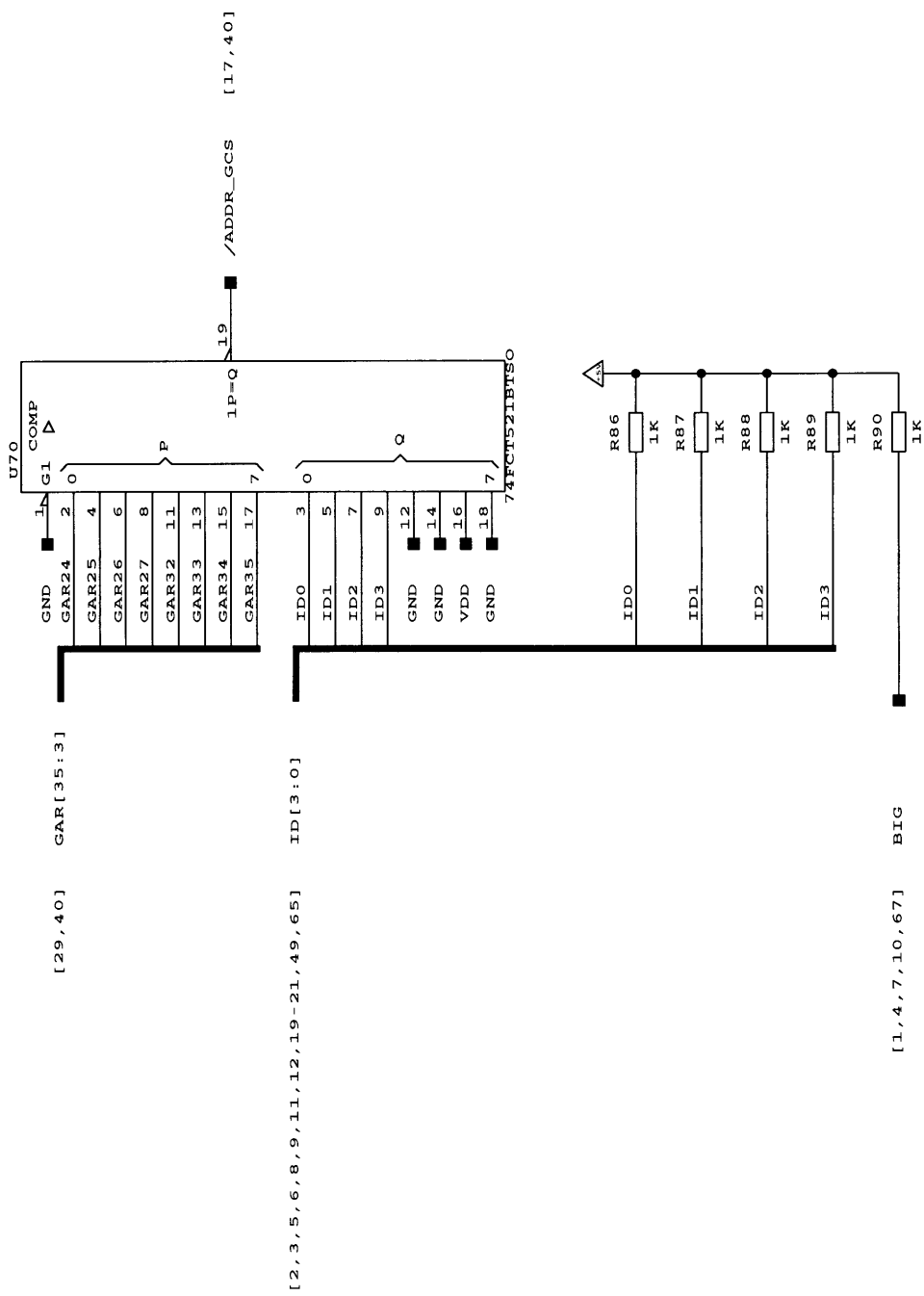
[34] LAR[21:20]A

[25] /WE_LS3
 [25] /OE_LS

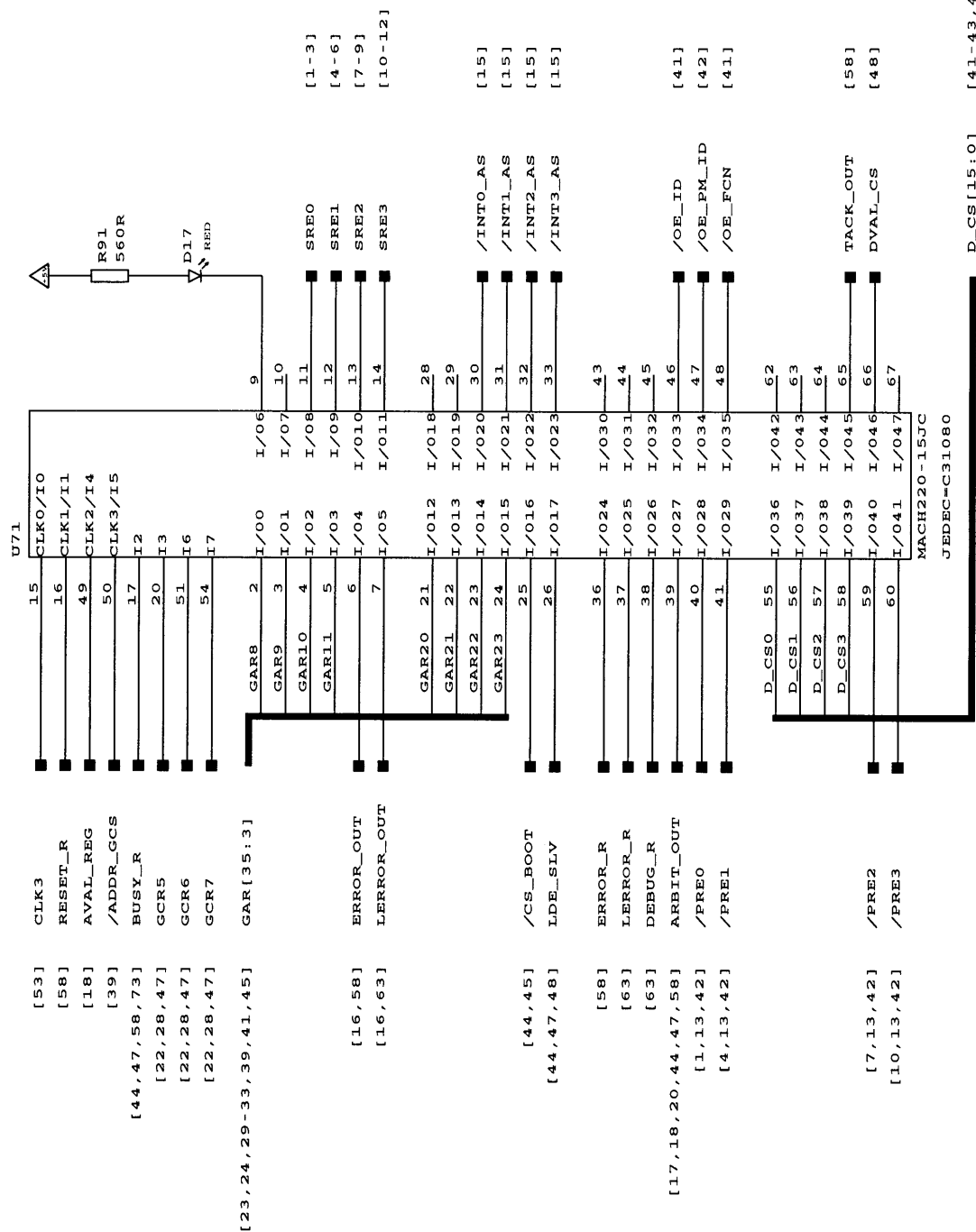


TLS3_[35:20]

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local snooper 3	
Issue 2			
Issue 3		File:	cpu301
			Page: 38 of 73

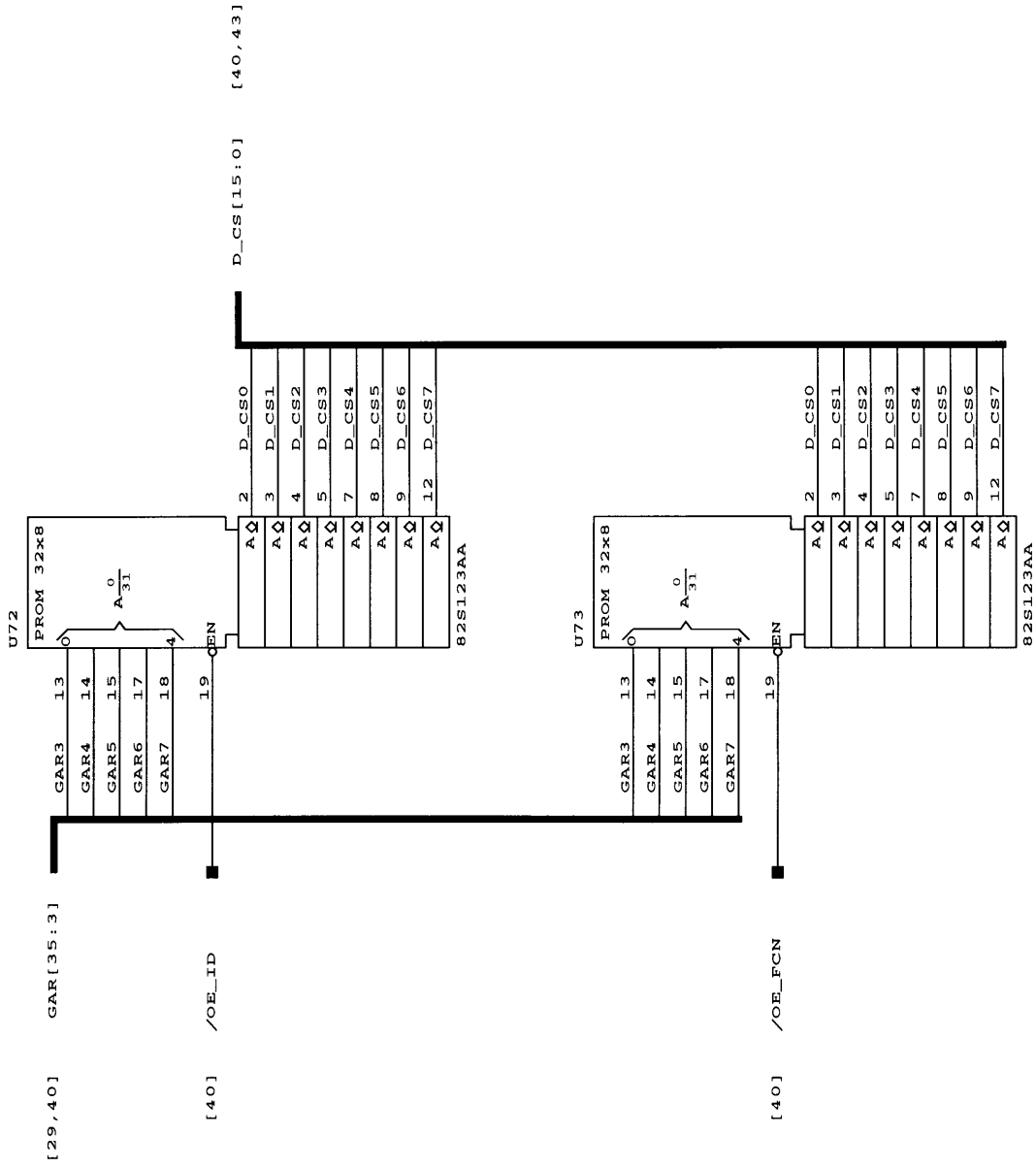


dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global control	
Issue 2		space decode	
Issue 3		File: cpu301	Page:39 of 73



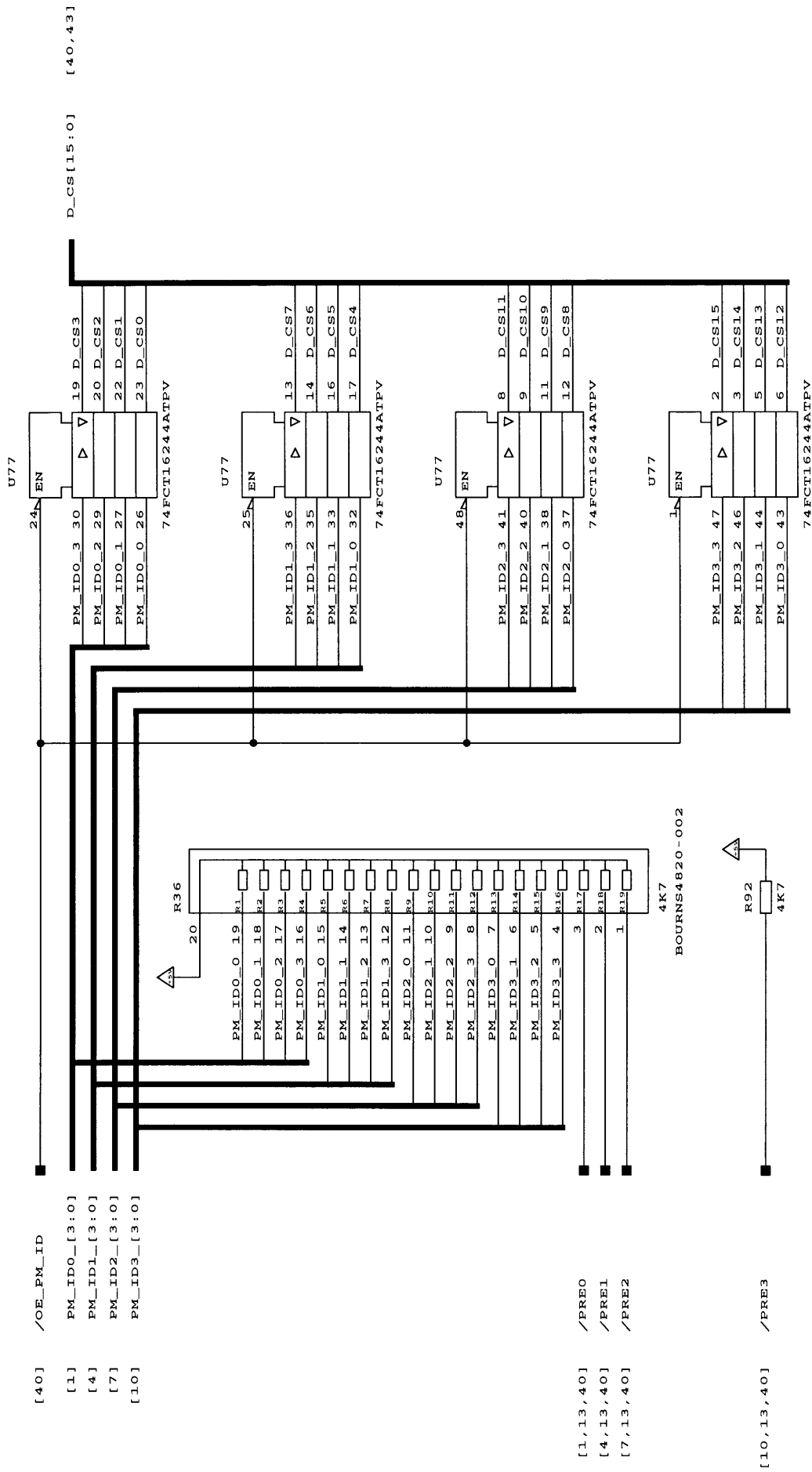
D_CS[15:0] [41-43,46]

dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global control space	
Issue 2		control	
Issue 3		File:	cpu301



FCN PROM mounted in socket.

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Module ID and FCN PROMs.	
Issue 2			
Issue 3			
		File: cpu301	Page: 41 of 73

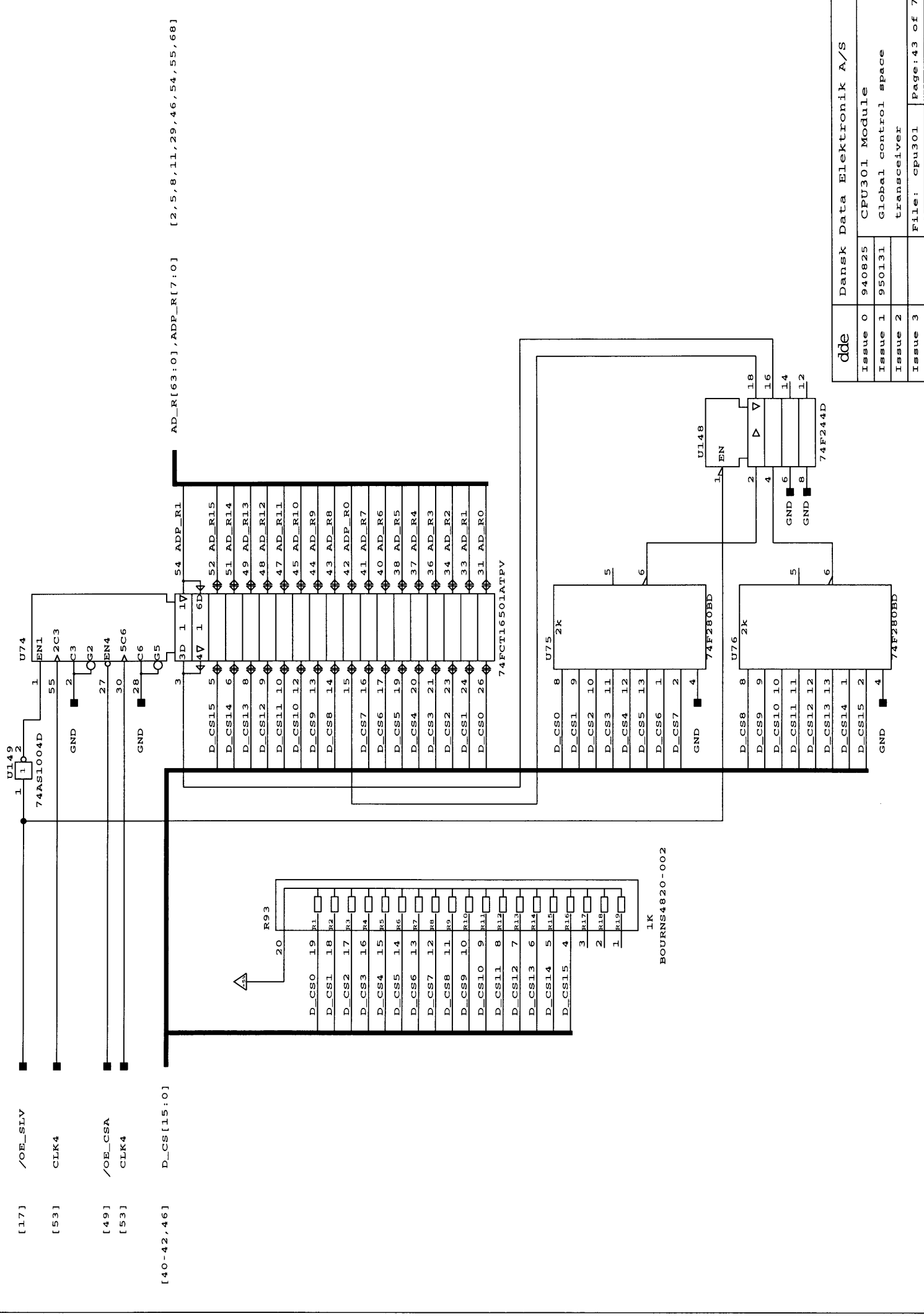


[40] /OE_PM_ID
 [1] PM_ID0_[3:0]
 [4] PM_ID1_[3:0]
 [7] PM_ID2_[3:0]
 [10] PM_ID3_[3:0]

[1,13,40] /PRE0
 [4,13,40] /PRE1
 [7,13,40] /PRE2

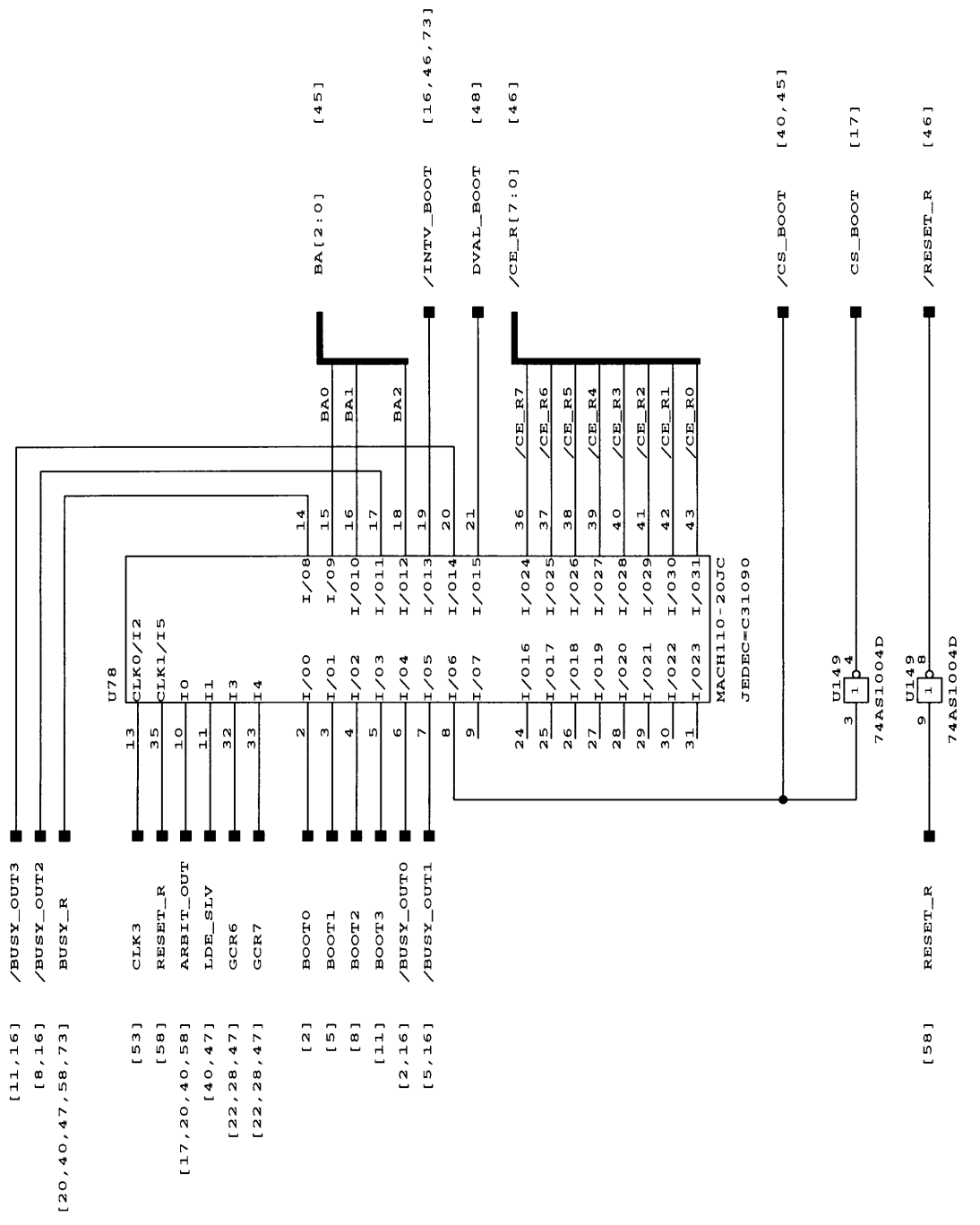
[10,13,40] /PRE3

dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Processor module	
Issue 2		ID register	
Issue 3		File: cpu301	

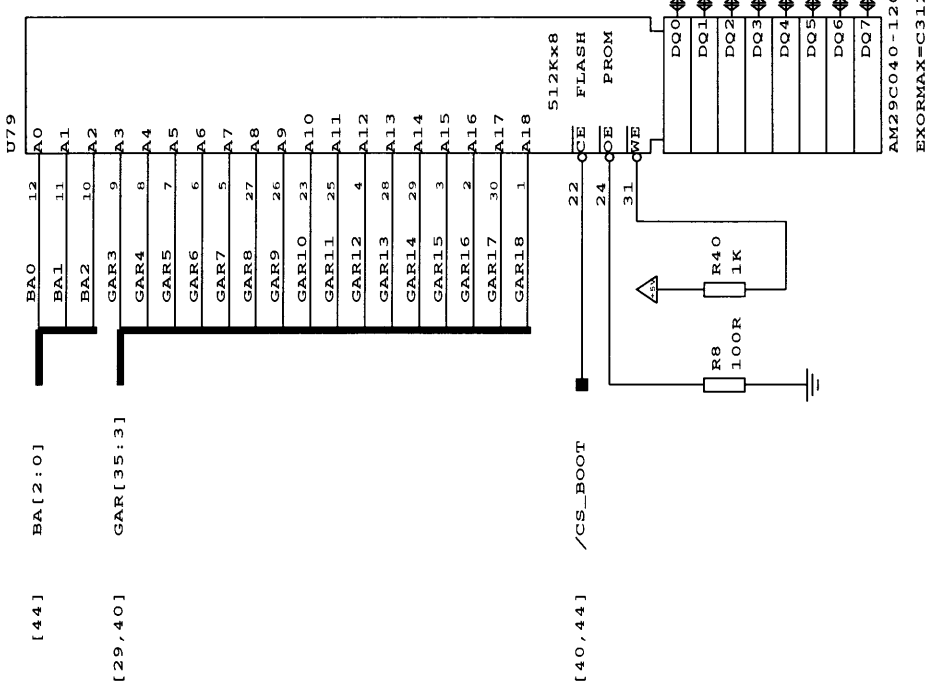


[17] /OE_SLV [53] CLK4 [49] /OE_CSA [53] CLK4 [40-42,46] D_CS[15:0] AD_P_R[63:0],ADP_R[7:0] [2,5,8,11,29,46,54,55,68]

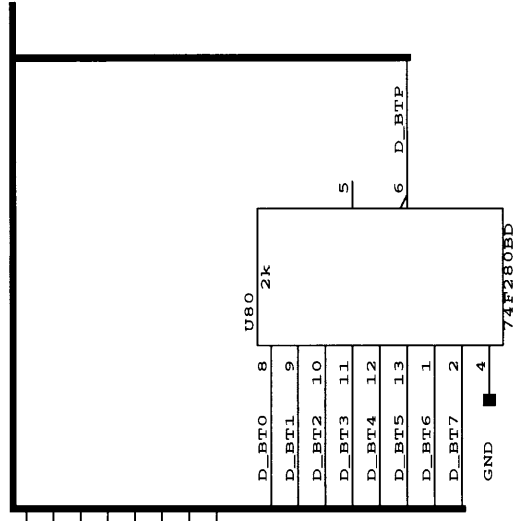
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global control space	
Issue 2		transceiver	
Issue 3		File: cpu301	



dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Boot control	
Issue 2			
Issue 3		File: cpu301	
		Page: 44 of 73	

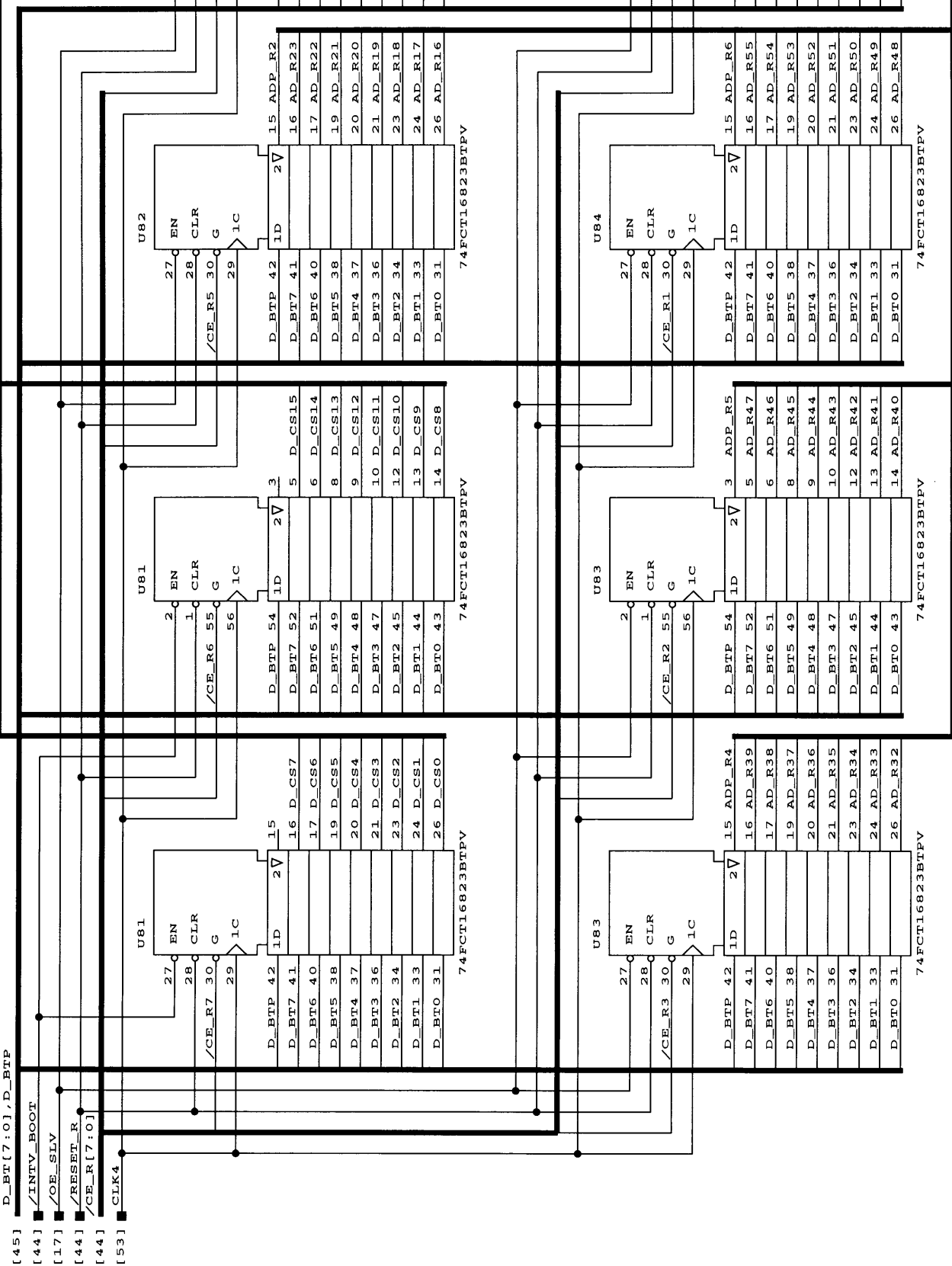


D_BT[7:0], D_BTP [46]



dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Boot PROM	
Issue 2			
Issue 3			
		File: cpu301	Page: 45 of 73

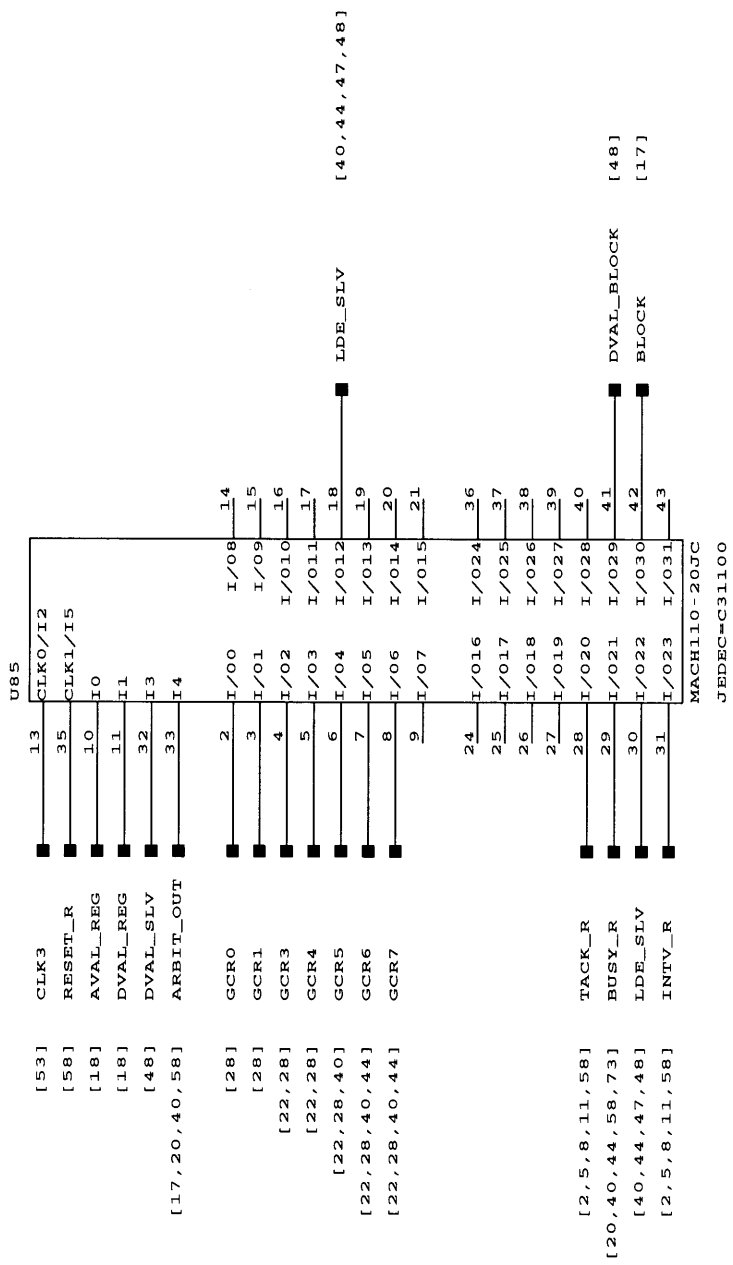
D_CS[15:0] [40,43]



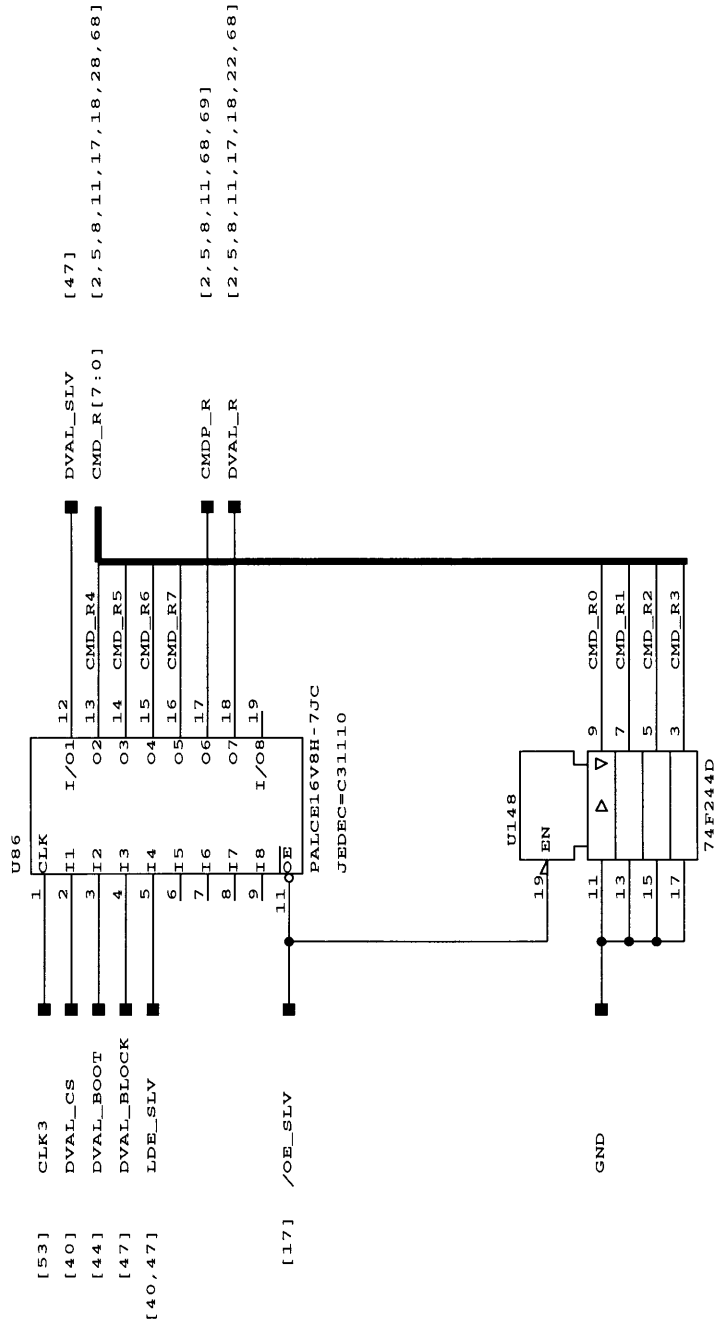
[45] D_BT[7:0], D_BTP
 [44] /INV_BOOT
 [17] /OE_SLV
 [44] /RESET_R
 [44] /CE_R[7:0]
 [53] CLK4

AD_R[63:0], ADP_R[7:0]
 [2,5,8,11,29,43,68]

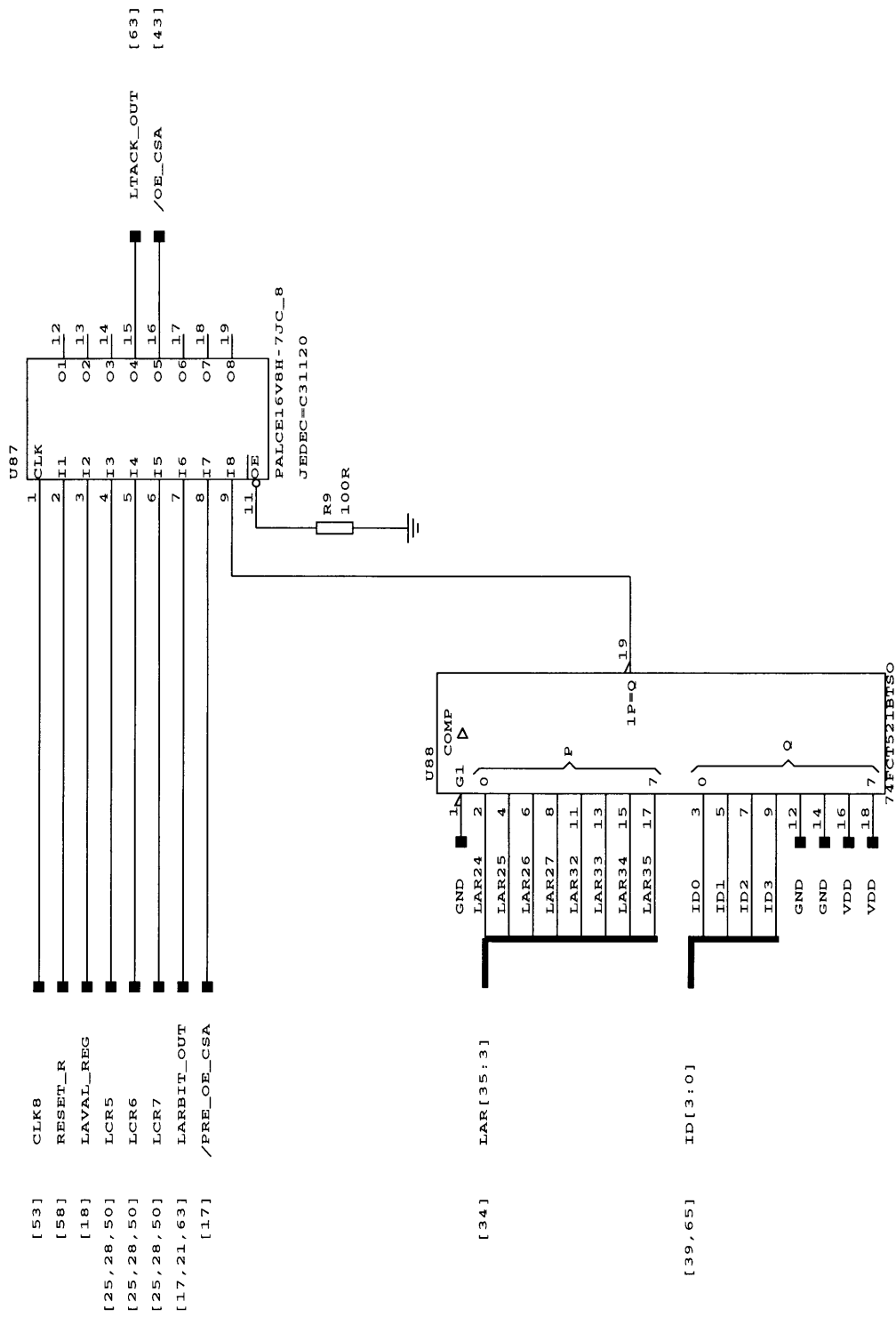
dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Boot register	
Issue 2			
Issue 3			
		File:	cpu301
		Page: 46 of 73	

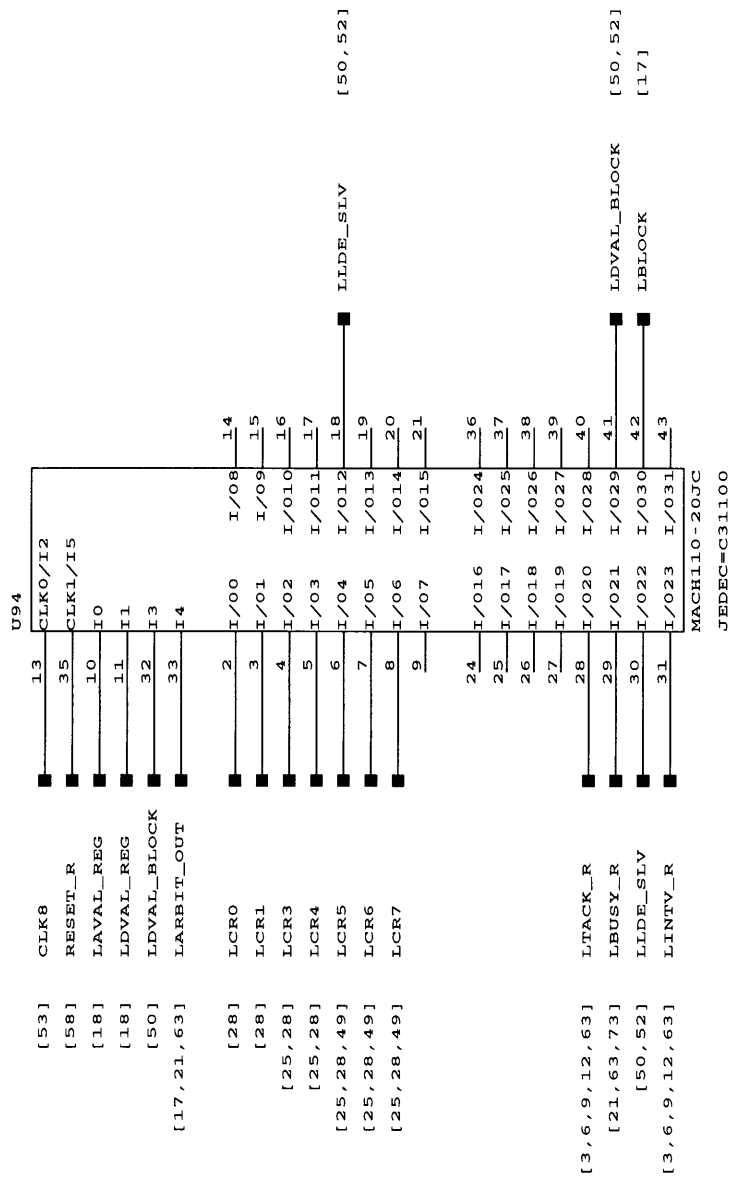


dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global dummy	
Issue 2		block generator	
Issue 3		File: cpu301	Page:47 of 73

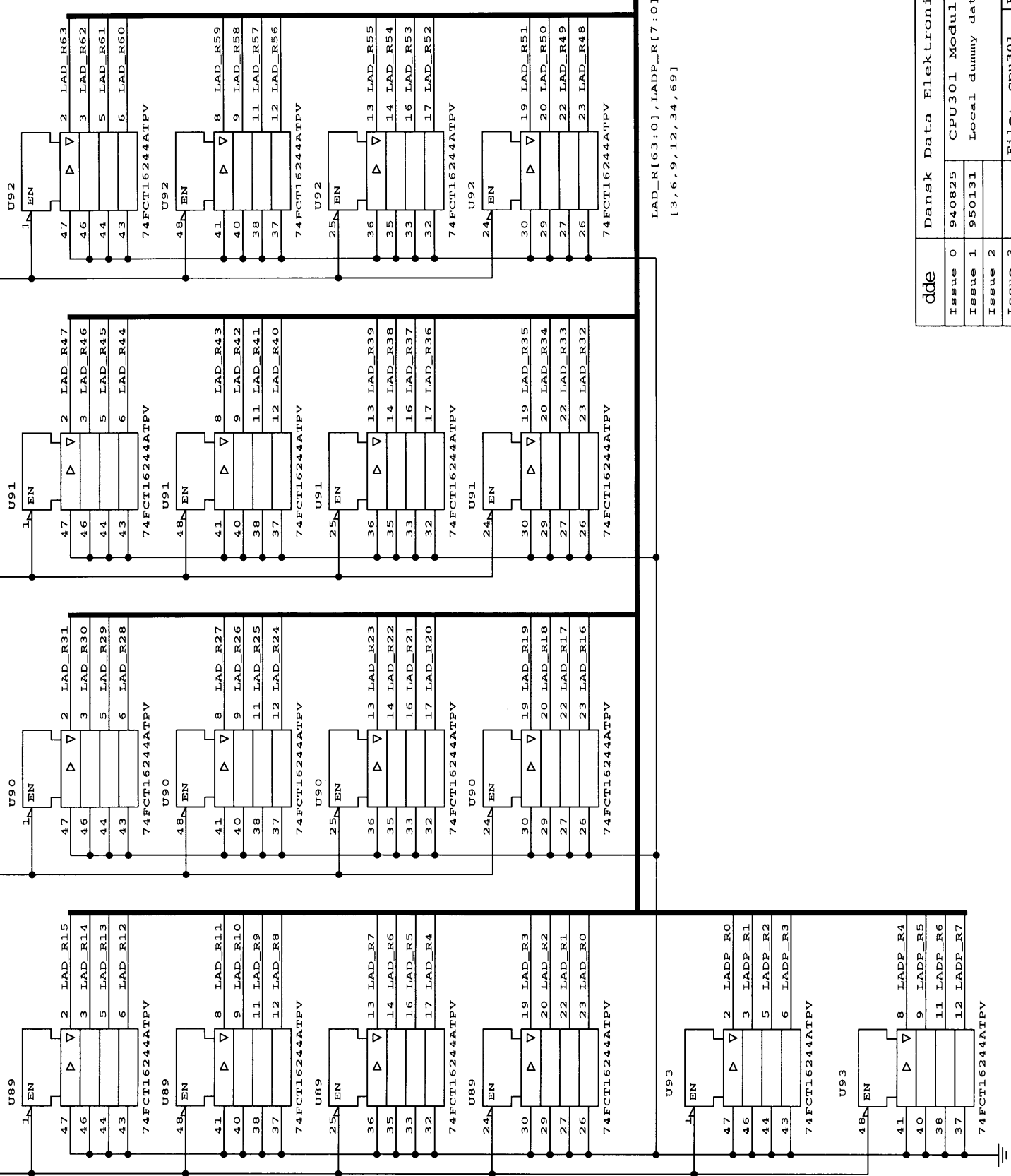


dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global data identifier	
Issue 2		output register	
Issue 3		File: cpu301	
		Page: 48 of 73	

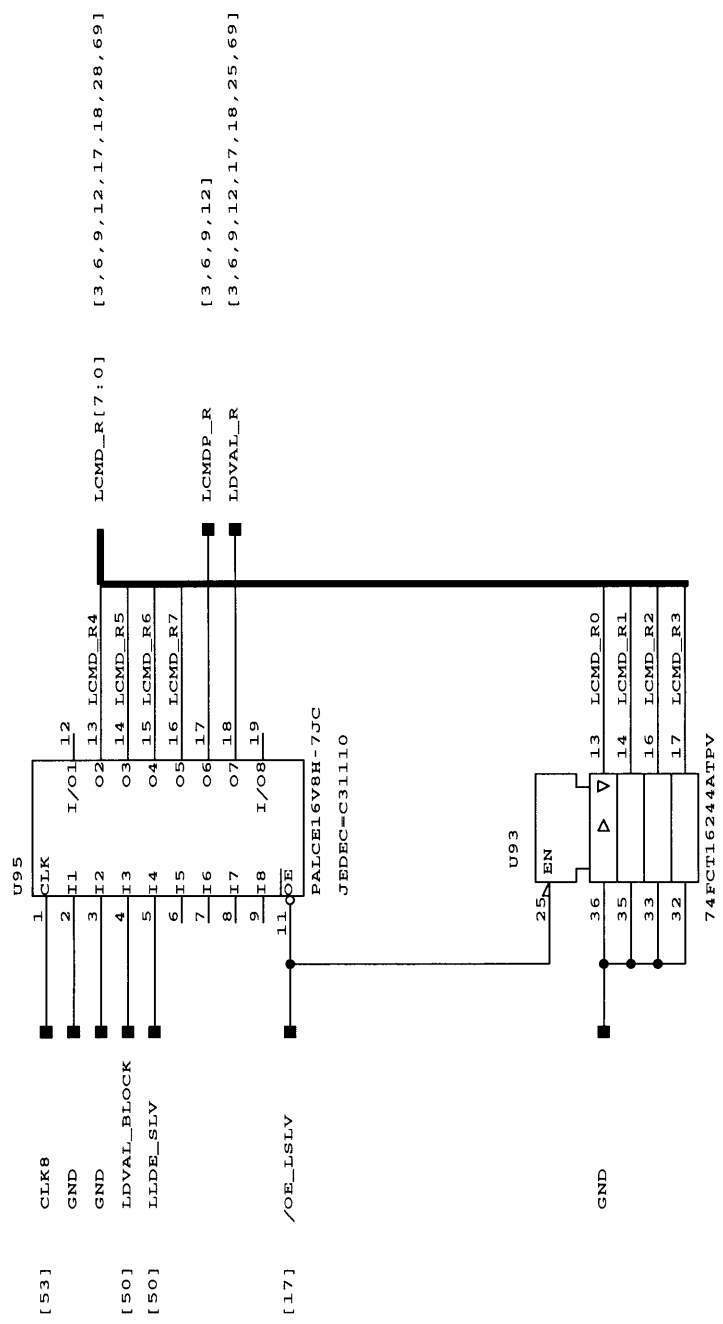




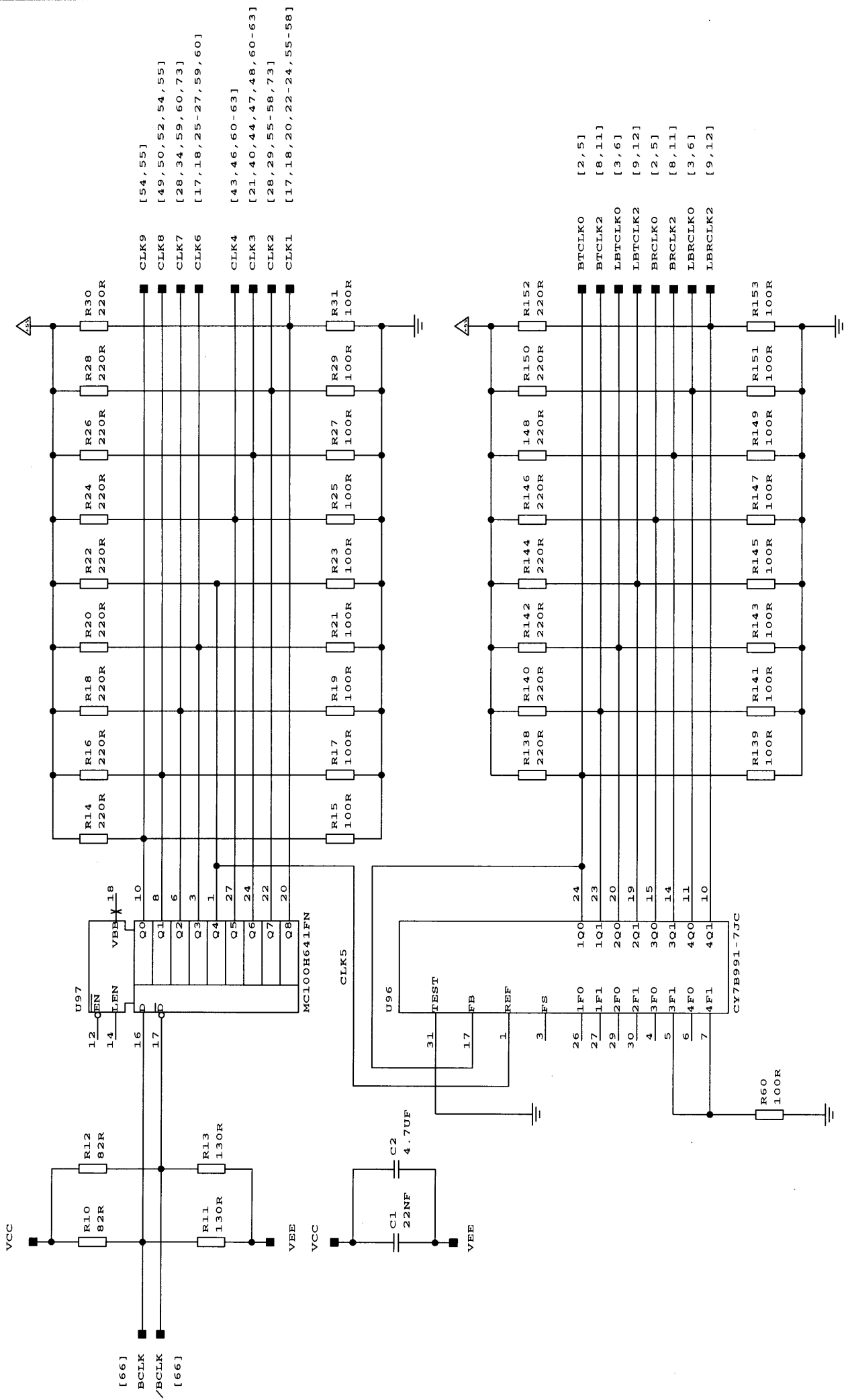
[17] /OE_LSLV



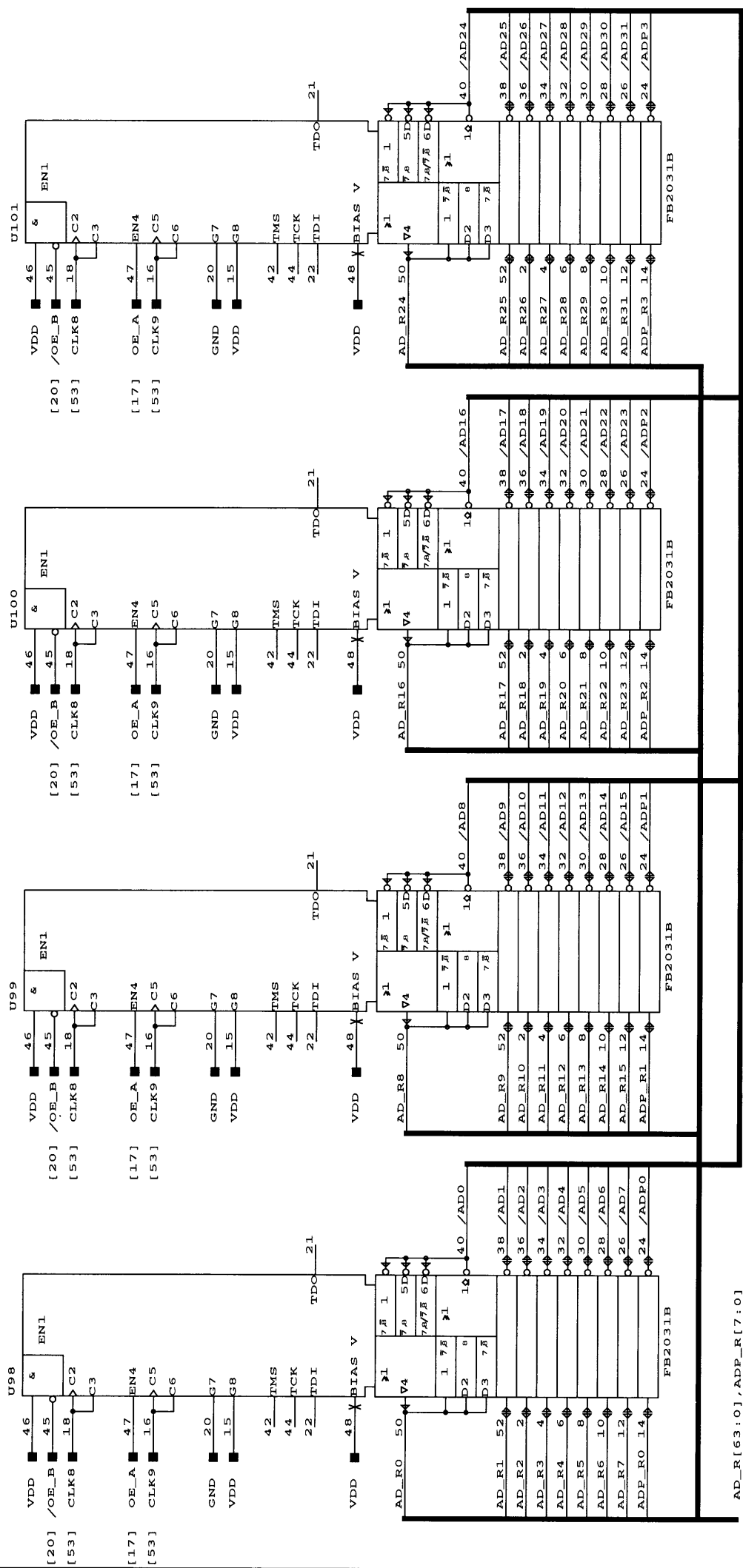
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local dummy data	
Issue 2			
Issue 3			



dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local data identifier	
Issue 2		output register	
Issue 3		File: cpu301	
		Page: 52 of 73	



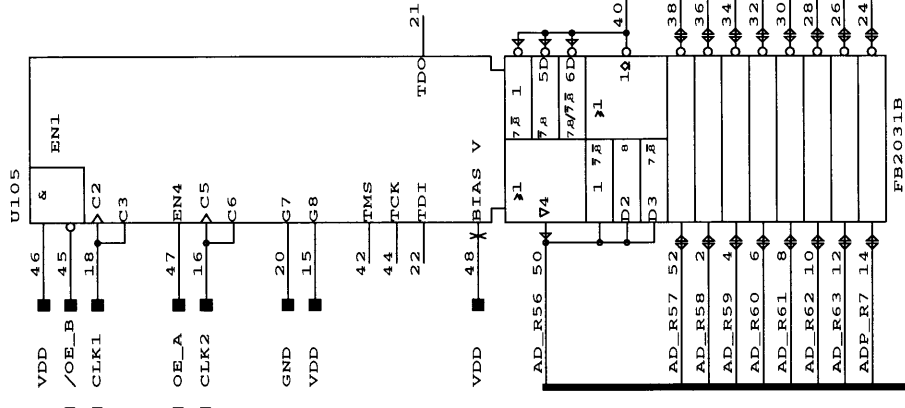
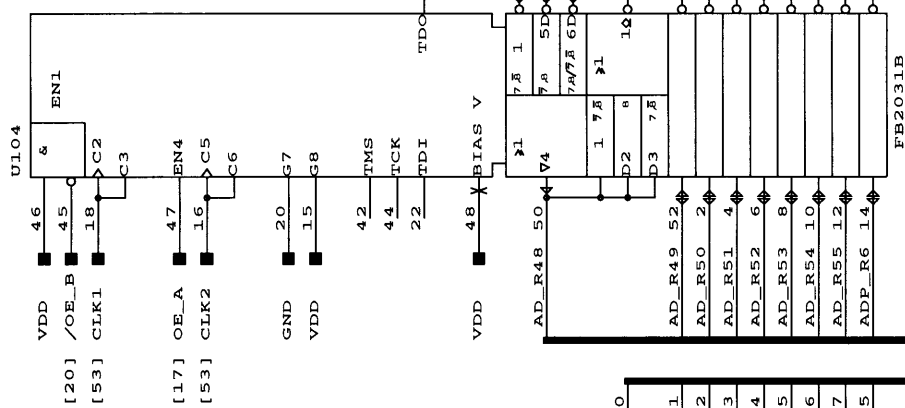
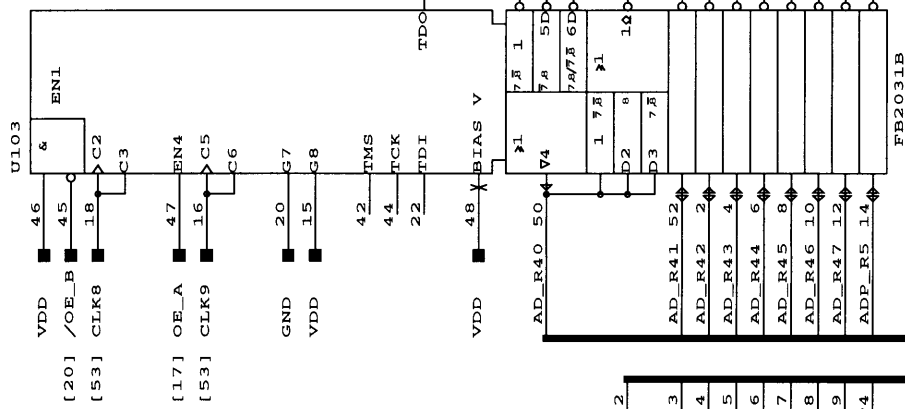
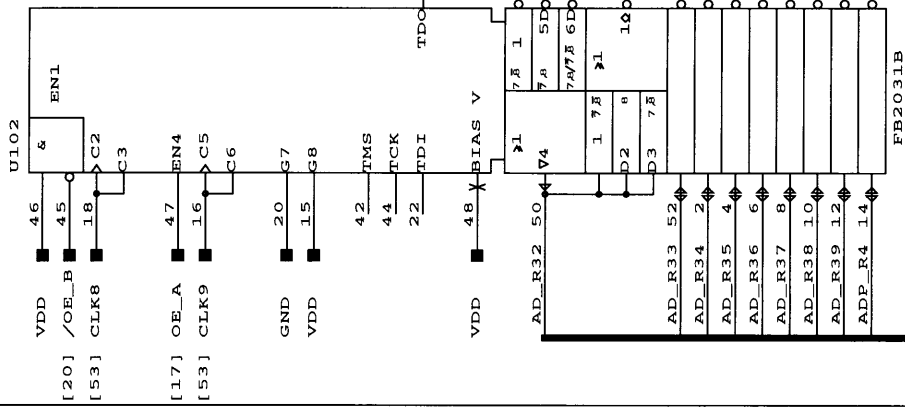
dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Clock distribution	
Issue 2			
Issue 3			
		File:	cpu301
		Page: 53 of 73	



AD_R[63:0],ADP_R[7:0]
[2,5,8,11,29,43,68]

/AD[63:0],/ADP[7:0]

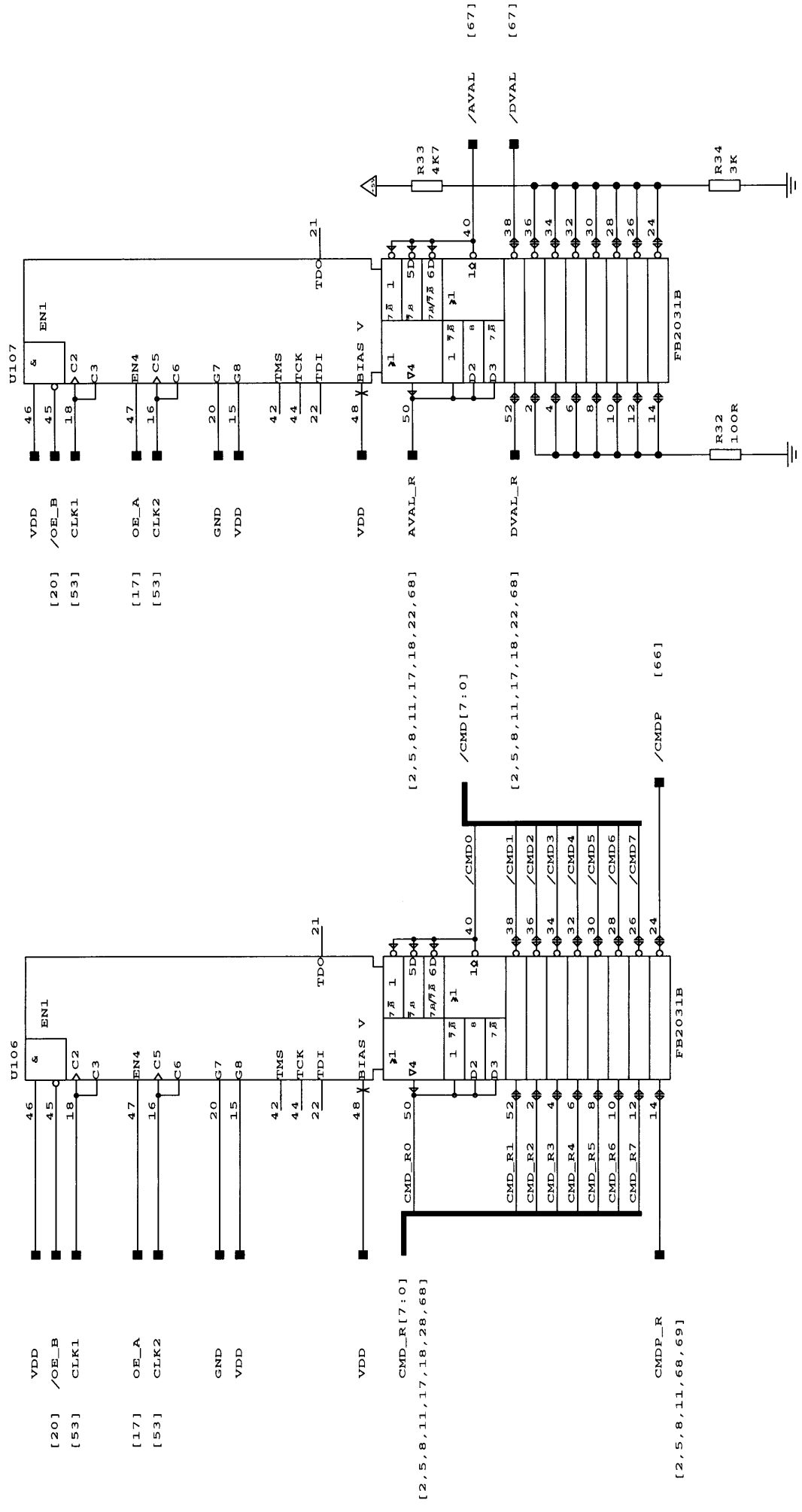
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global address/data	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:54 of 73



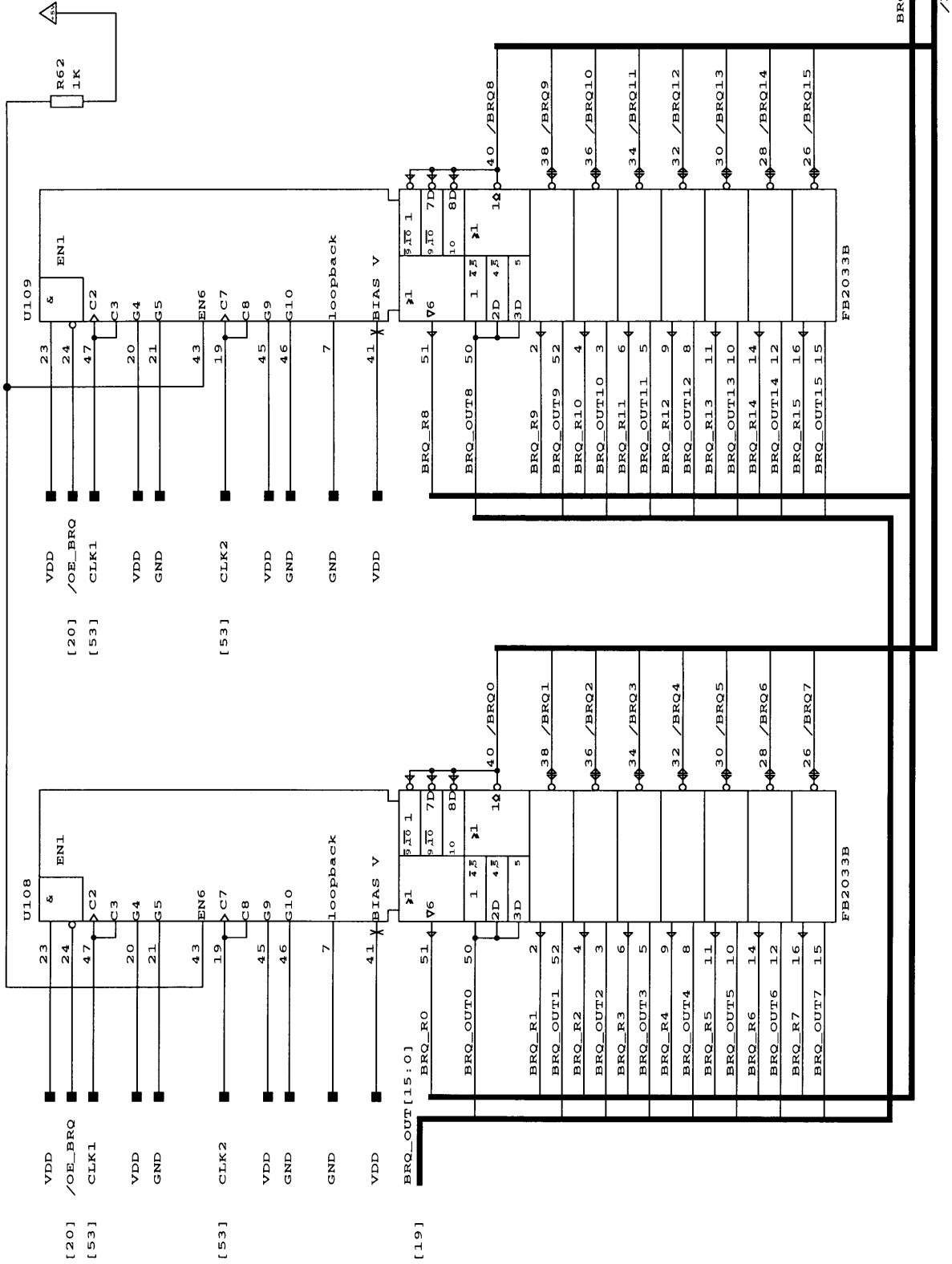
AD_R[63:0],ADP_R[7:0]
[2,5,8,11,29,43,68]

/AD[63:0],/ADP[7:0]

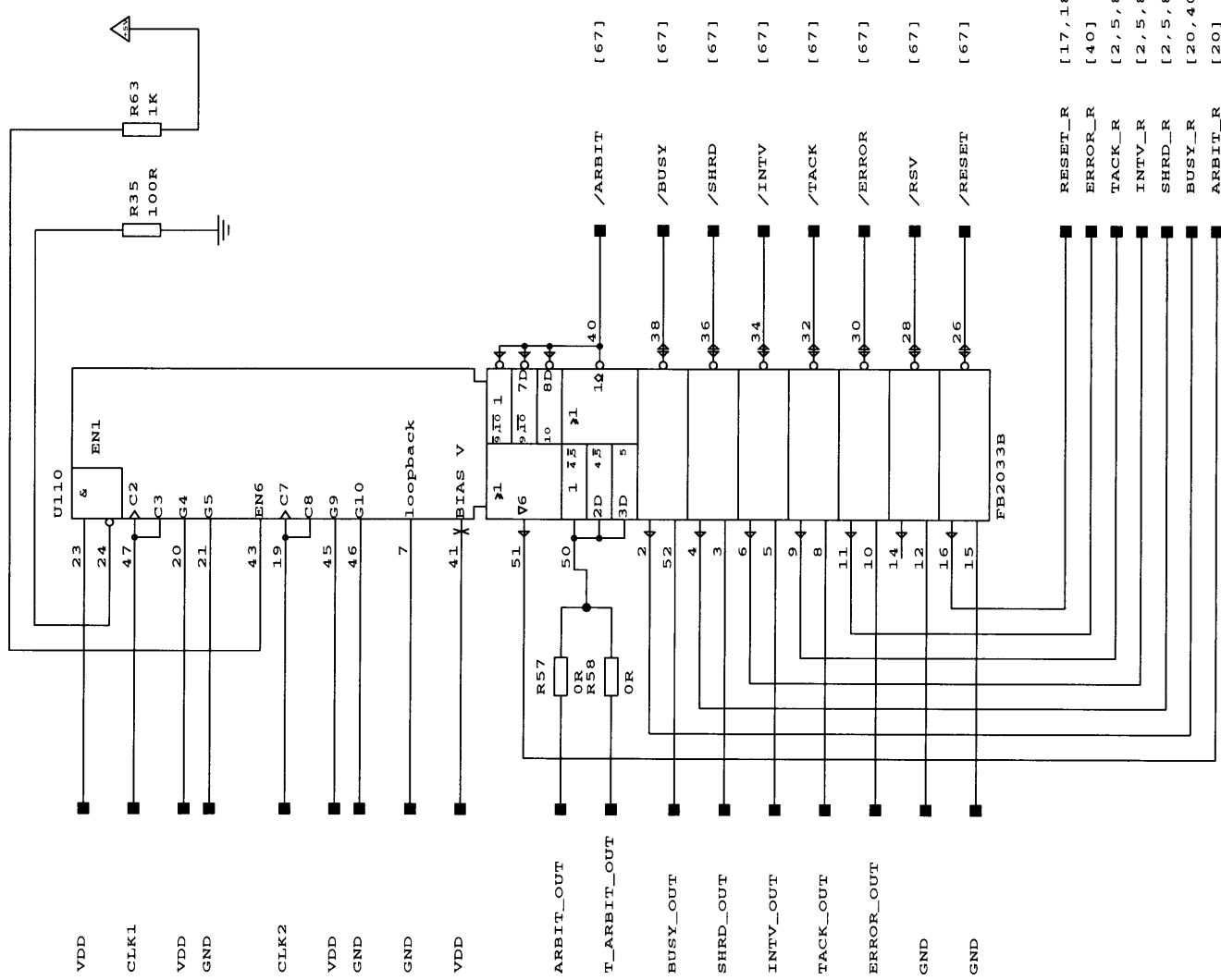
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global address/data	
Issue 2		transceiver	
Issue 3		File: cpu301	
		Page:55 of 73	



dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global command and valid	
Issue 2		transceiver	
Issue 3		File: cpu301	
Page: 56 of 73			



dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global bus request	
Issue 2		transceiver	
Issue 3		File: cpu301	Page: 57 of 73



[53]

[53]

[17, 18, 20, 40, 44, 47]

[18]

[16]

[16]

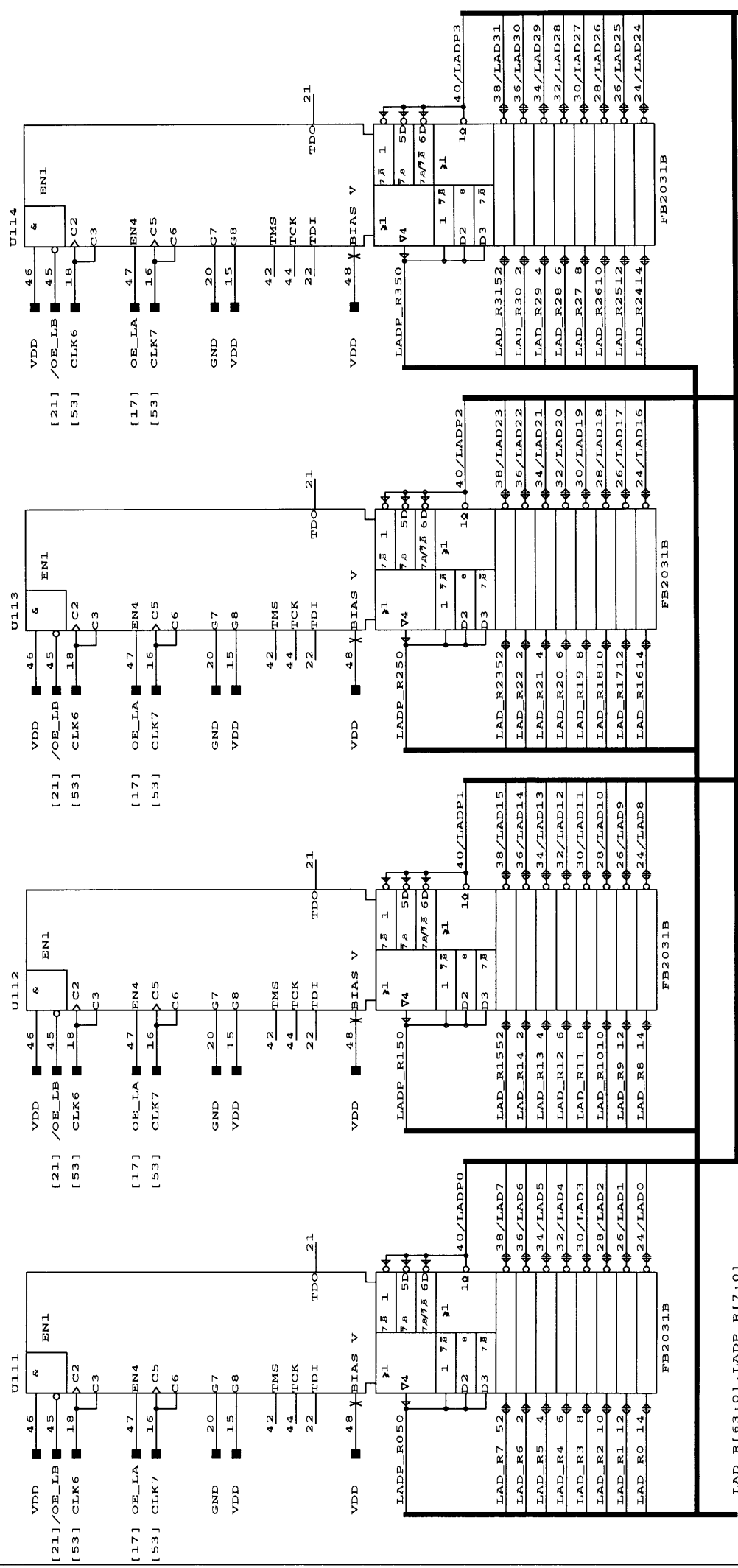
[16, 73]

[40]

[16, 40]

[17, 18, 20-27, 40, 44, 47, 49, 50, 73]
 [40]
 [2, 5, 8, 11, 47]
 [2, 5, 8, 11, 47]
 [2, 5, 8, 11, 22]
 [20, 40, 44, 47, 73]
 [20]

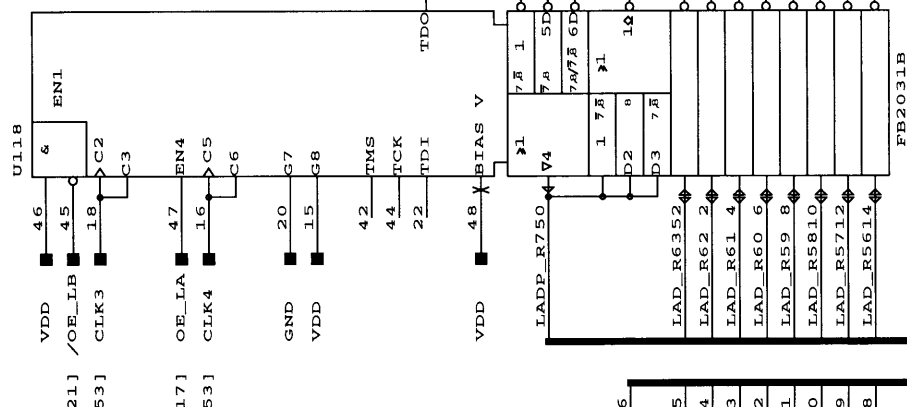
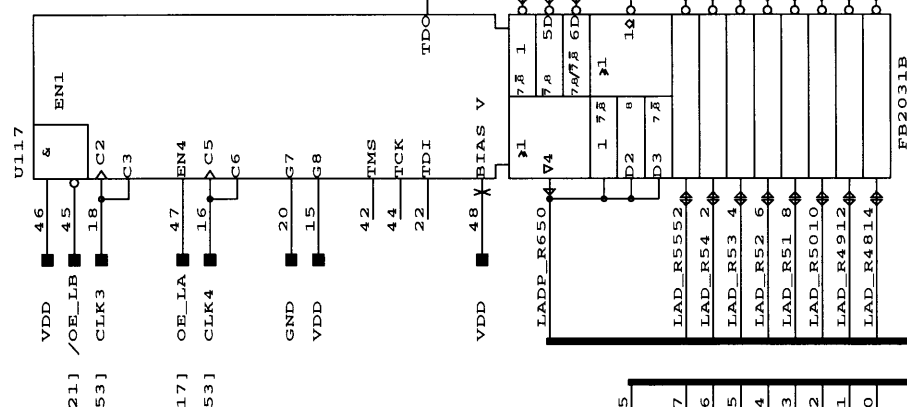
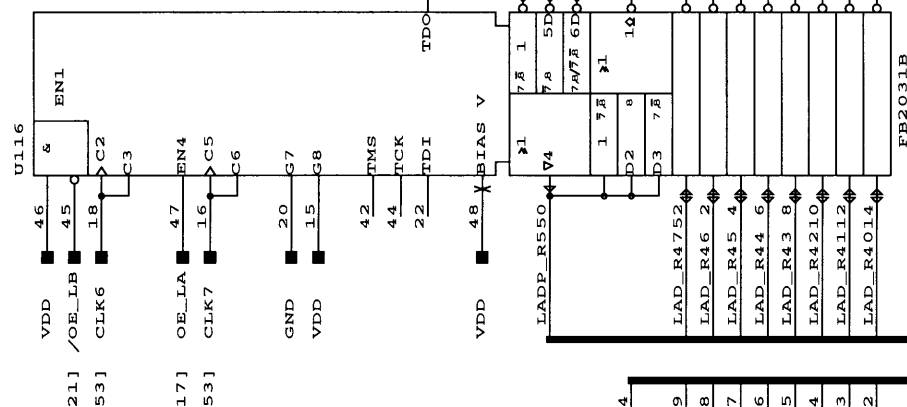
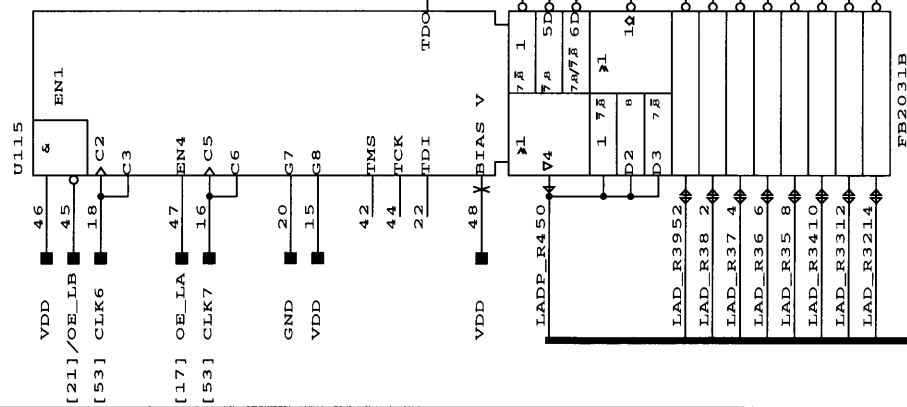
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global control transceiver	
Issue 2			
Issue 3		File:	cpu301 Page: 58 of 73



LAD_R[63:0], LADP_R[7:0]
[3,6,9,12,34,69]

/LAD[63:0], LADP[7:0]

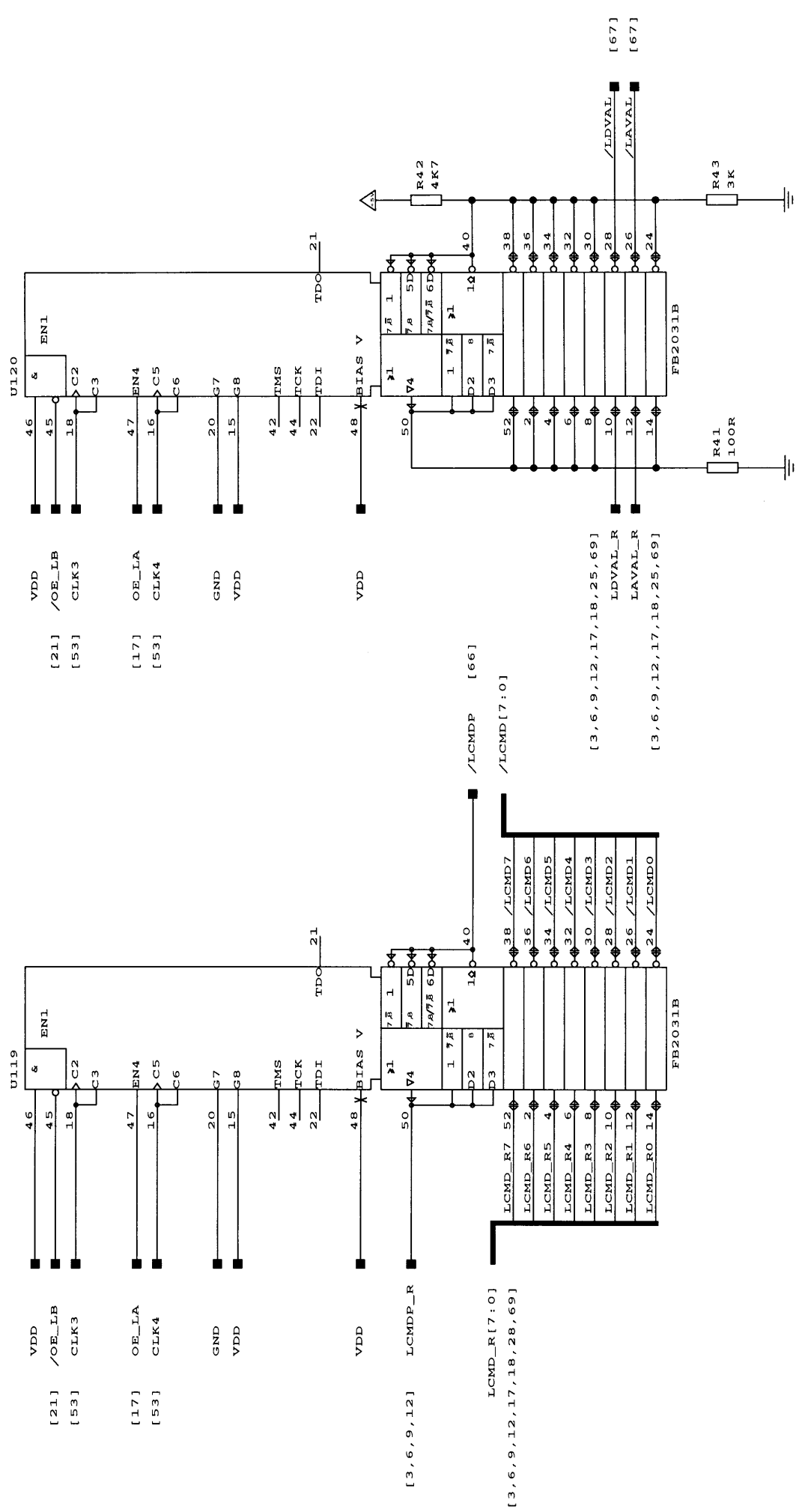
dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local address/data	
Issue 2		transceiver	
Issue 3		File: cpu301	Page: 59 of 73



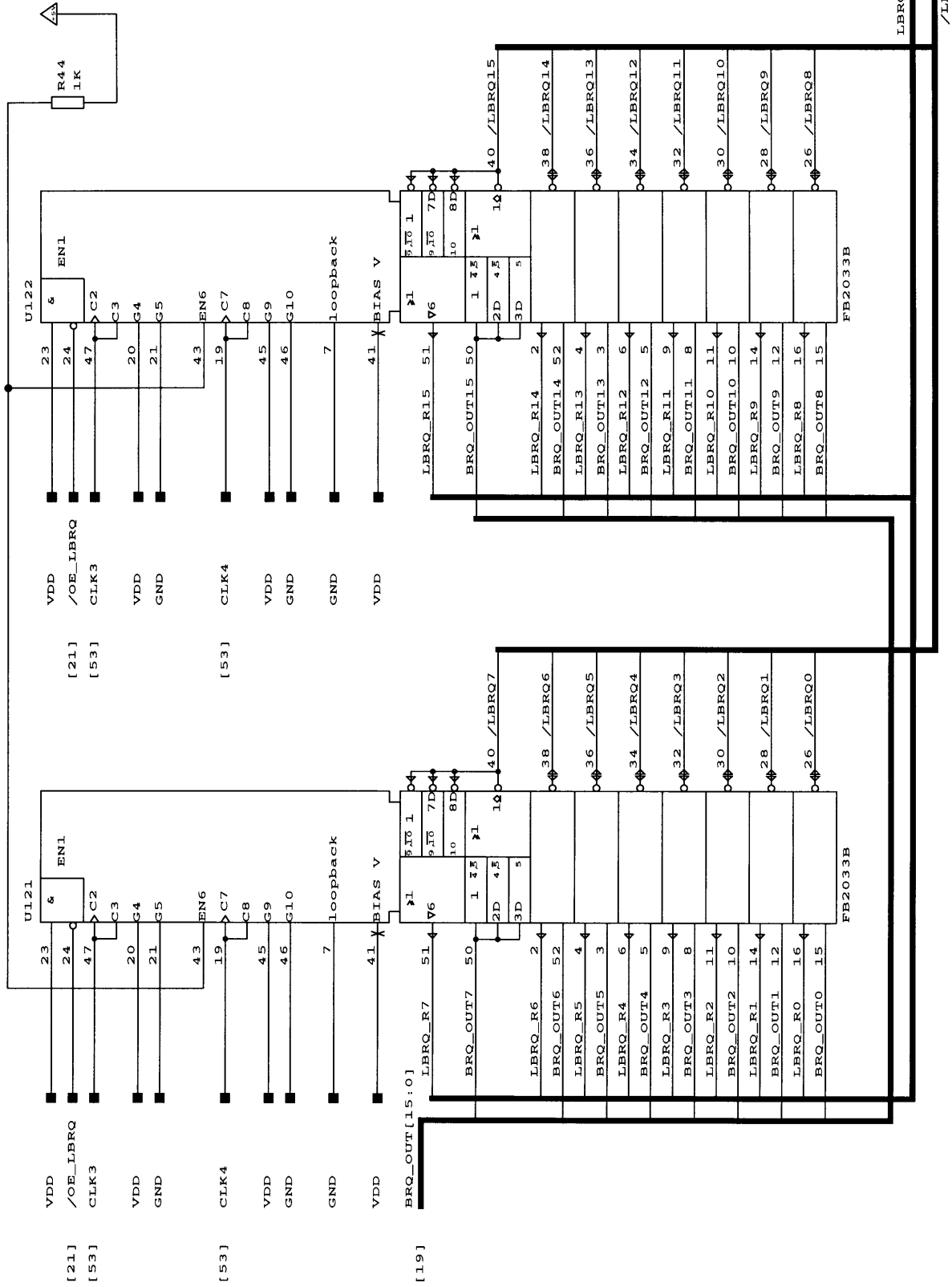
LAD_R[63:0], LADP_R[7:0]
[3,6,9,12,34,69]

/LAD[63:0],/LADP[7:0]

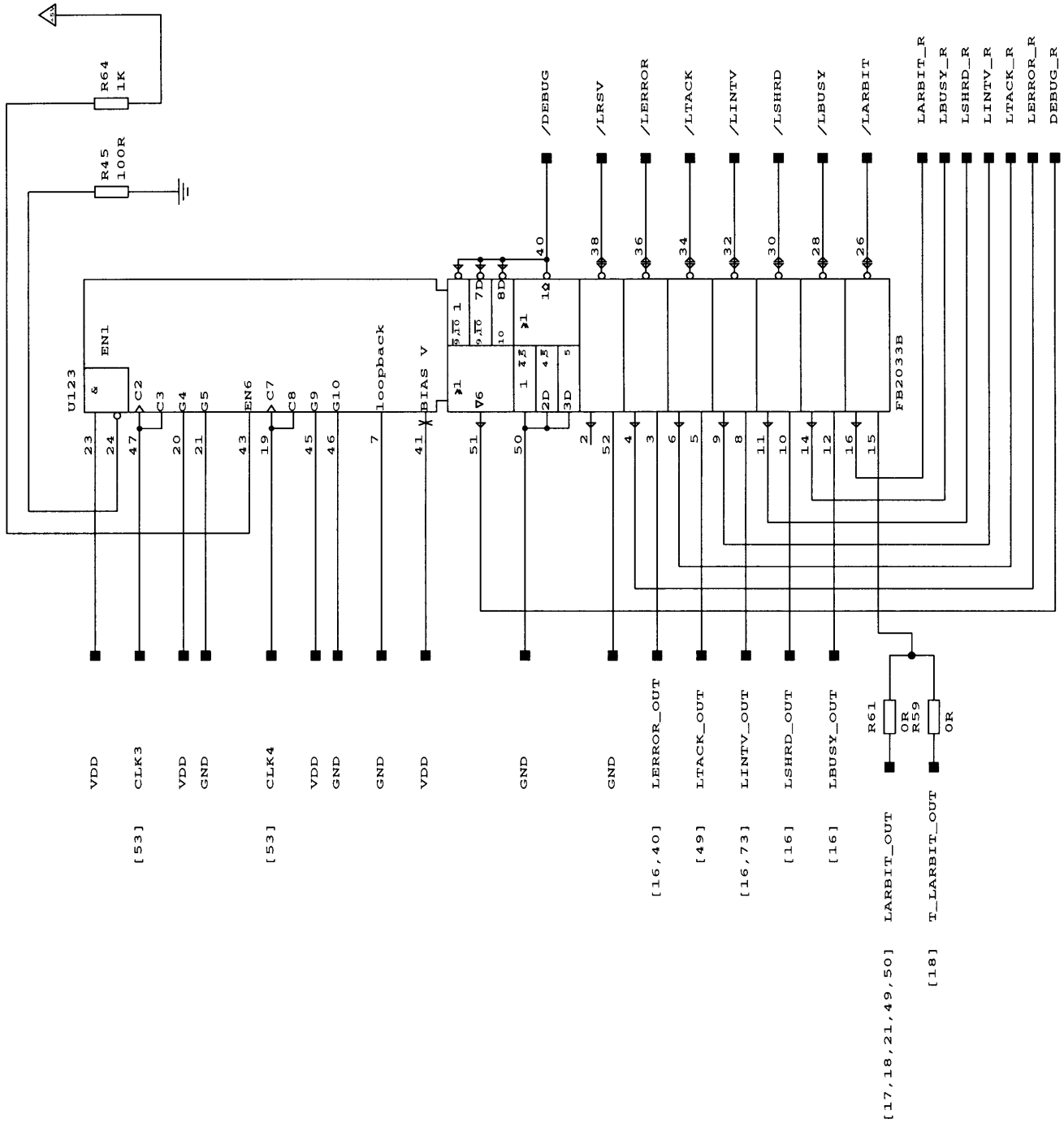
dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local address/data	
Issue 2		transceiver	
Issue 3		File: cpu301	
		Page:60 of 73	



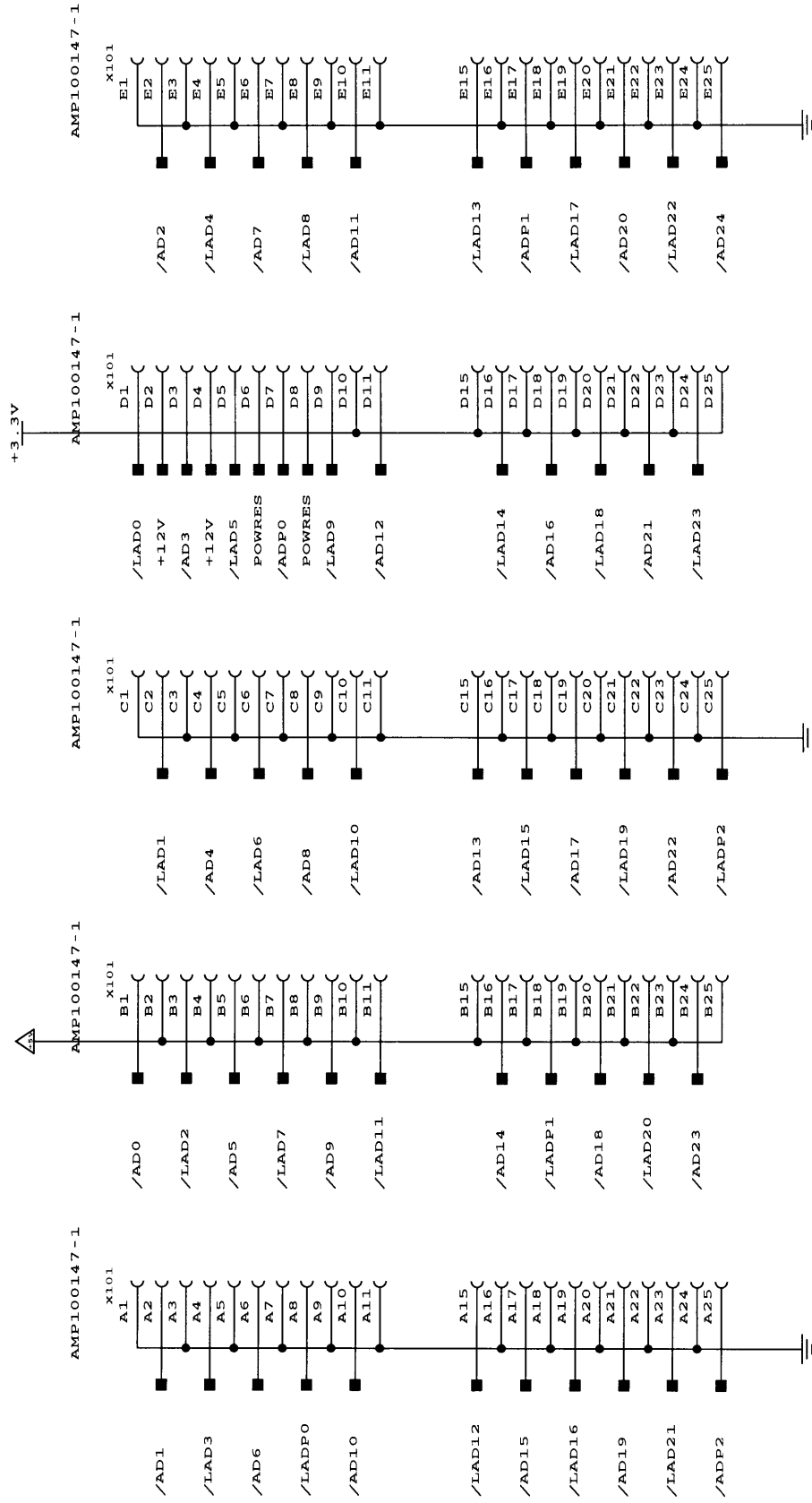
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local command and valid	
Issue 2		transceiver	
Issue 3		File:	cpu301
			Page:61 of 73

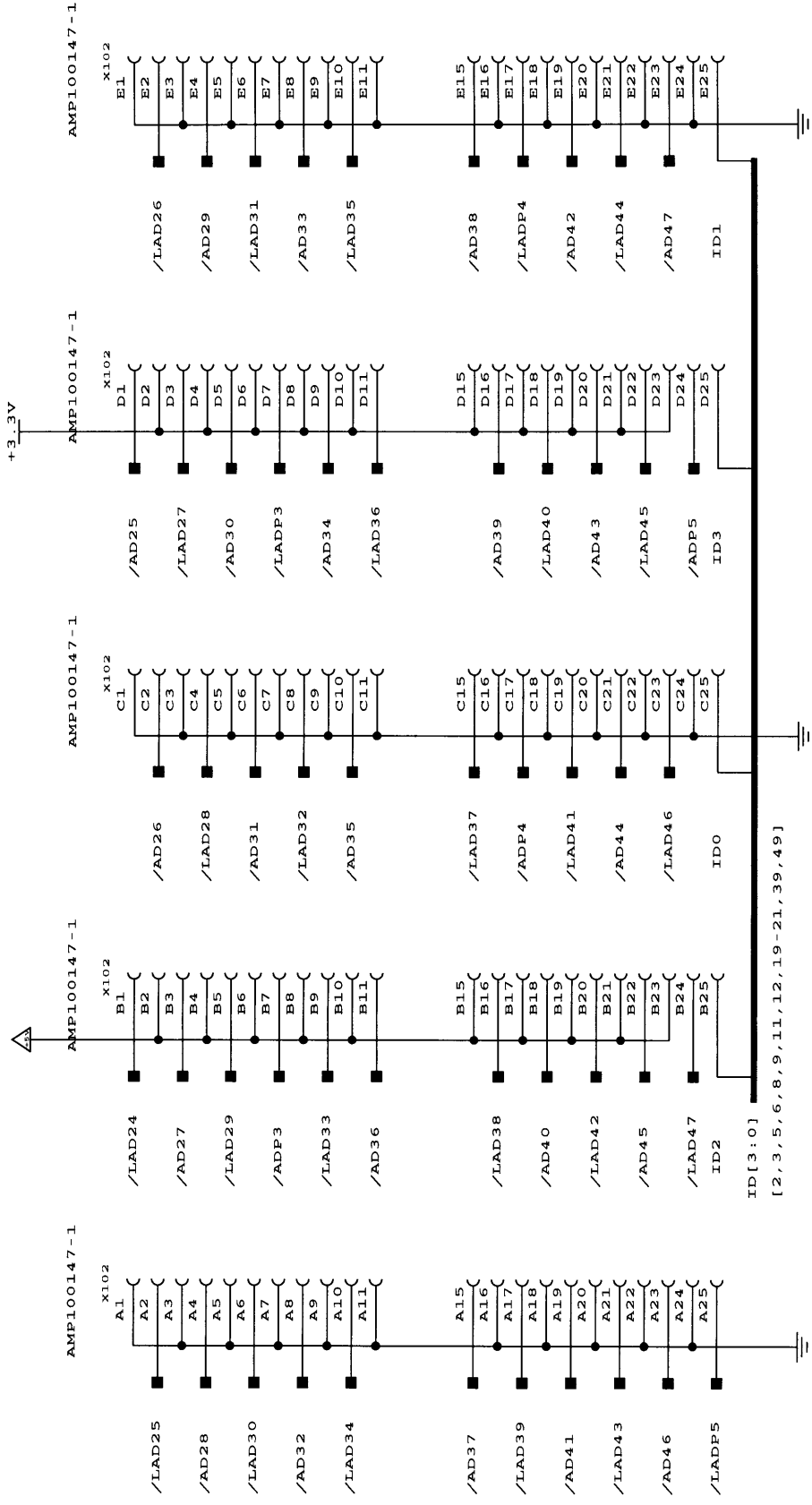


dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local bus request	
Issue 2		transceiver	
Issue 3		File:	cpu301



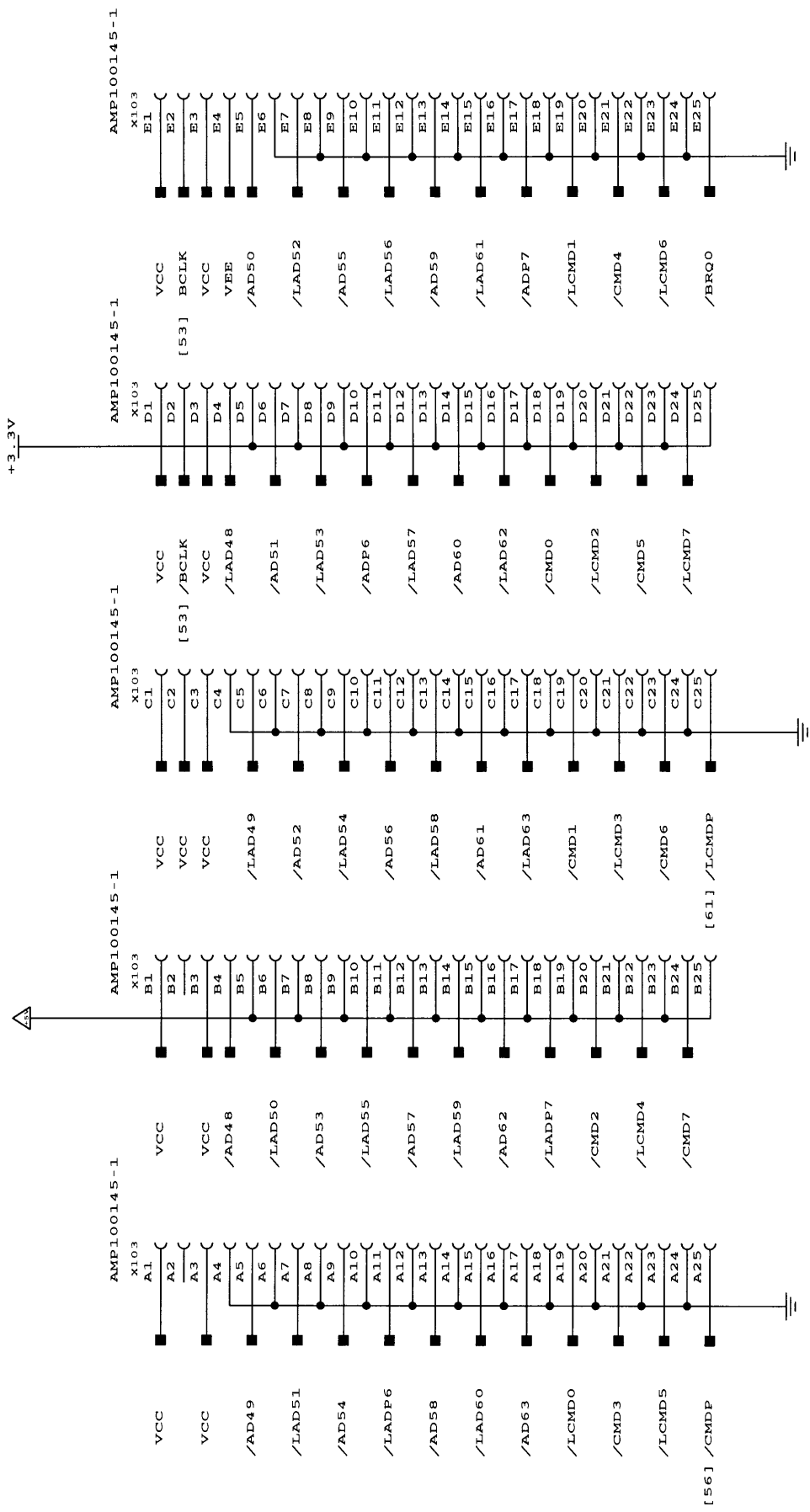
dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local control transceiver	
Issue 2			
Issue 3			



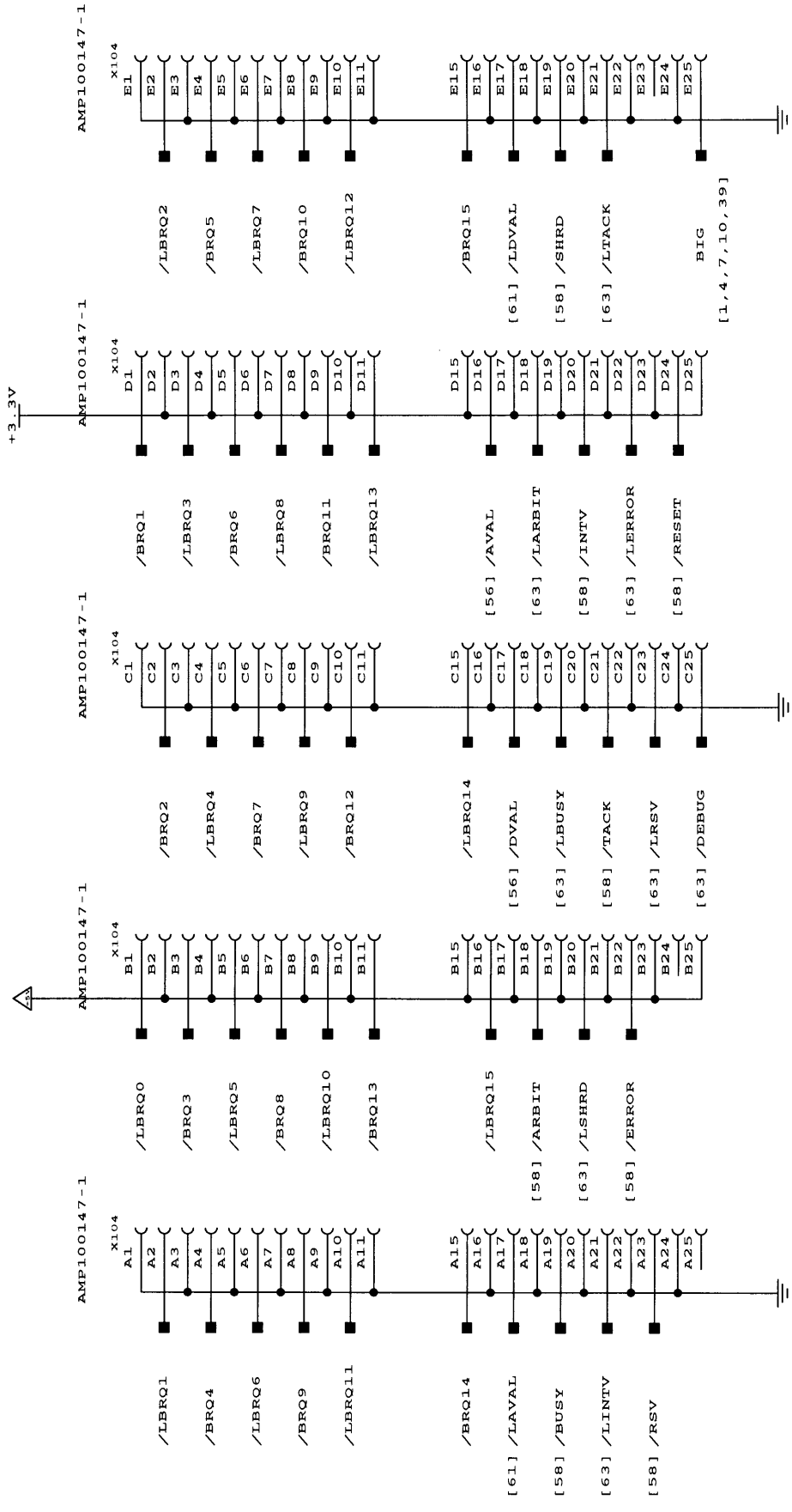


ID[3:0]
[2,3,5,6,8,9,11,12,19-21,39,49]

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connector (row 26-50)	
Issue 2			
Issue 3			
		File:	cpu301 Page:65 of 73

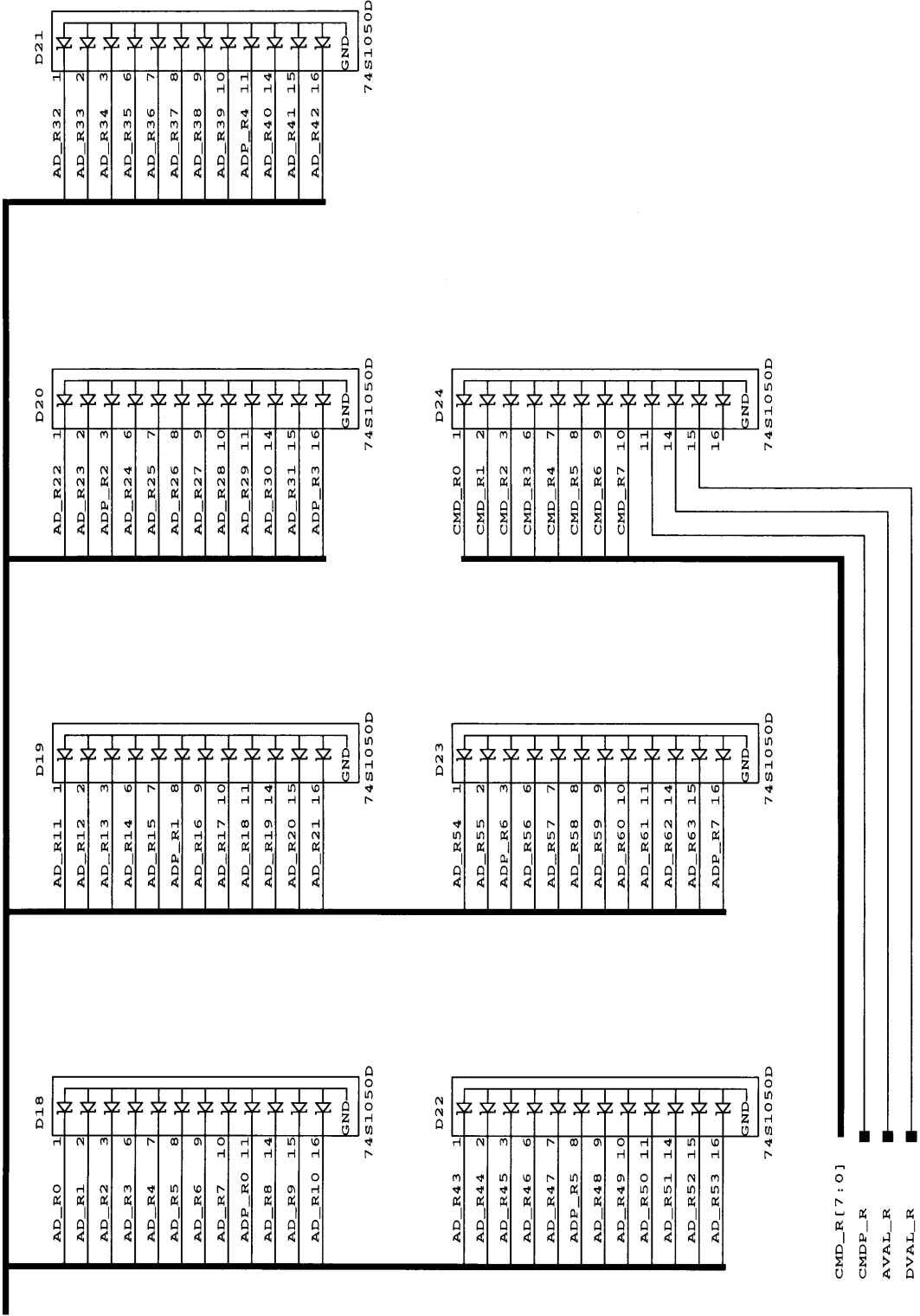


dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connector (row 51-75)	
Issue 2			
Issue 3		File: cpu301 Page:66 of 73	



dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connector (row 76-100)	
Issue 2			
Issue 3		File: cpu301 Page:67 of 73	

[2,5,8,11,43,46,54,55]
 AD_R[63:0].ADP_R[7:0]



[2,5,8,11,48,56] CMD_R[7:0]
 [2,5,8,11,48,56] CMDP_R
 [2,5,8,11,18,22,56] AVAL_R
 [2,5,8,11,18,22,48,56] DVAL_R

D21

AD_R32	1
AD_R33	2
AD_R34	3
AD_R35	6
AD_R36	7
AD_R37	8
AD_R38	9
AD_R39	10
ADP_R4	11
AD_R40	14
AD_R41	15
AD_R42	16
GND	

74S1050D

D20

AD_R22	1
AD_R23	2
ADP_R2	3
AD_R24	6
AD_R25	7
AD_R26	8
AD_R27	9
AD_R28	10
AD_R29	11
AD_R30	14
AD_R31	15
ADP_R3	16
GND	

74S1050D

D19

AD_R11	1
AD_R12	2
AD_R13	3
AD_R14	6
AD_R15	7
ADP_R1	8
AD_R16	9
AD_R17	10
AD_R18	11
AD_R19	14
AD_R20	15
AD_R21	16
GND	

74S1050D

D18

AD_R0	1
AD_R1	2
AD_R2	3
AD_R3	6
AD_R4	7
AD_R5	8
AD_R6	9
AD_R7	10
ADP_R0	11
AD_R8	14
AD_R9	15
AD_R10	16
GND	

74S1050D

D24

CMD_R0	1
CMD_R1	2
CMD_R2	3
CMD_R3	6
CMD_R4	7
CMD_R5	8
CMD_R6	9
CMD_R7	10
	11
	14
	15
	16
GND	

74S1050D

D23

AD_R54	1
AD_R55	2
ADP_R6	3
AD_R56	6
AD_R57	7
AD_R58	8
AD_R59	9
AD_R60	10
AD_R61	11
AD_R62	14
AD_R63	15
ADP_R7	16
GND	

74S1050D

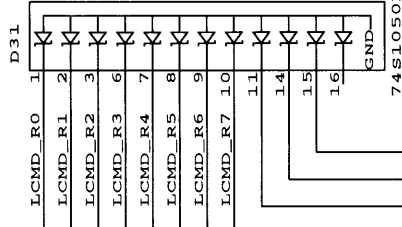
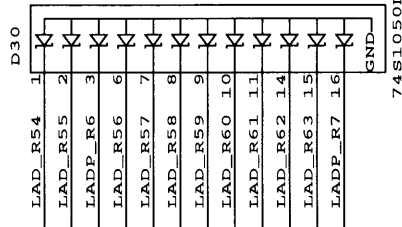
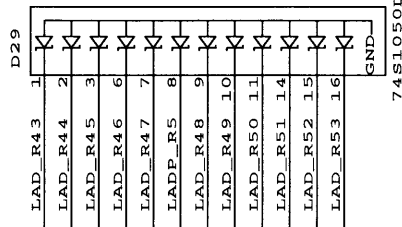
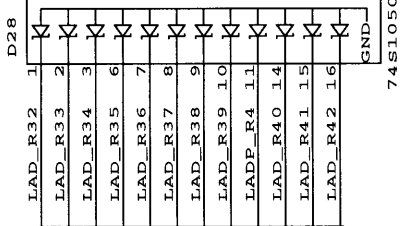
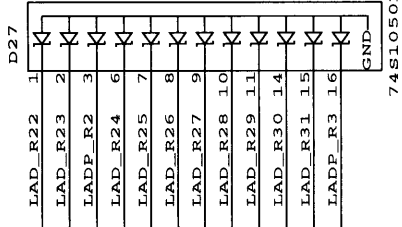
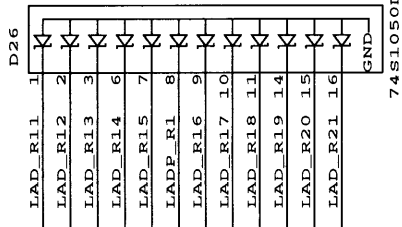
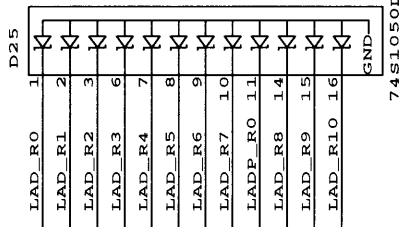
D22

AD_R43	1
AD_R44	2
AD_R45	3
AD_R46	6
AD_R47	7
ADP_R5	8
AD_R48	9
AD_R49	10
AD_R50	11
AD_R51	14
AD_R52	15
AD_R53	16
GND	

74S1050D

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Internal global bus term.	
Issue 2			
Issue 3			
File:	cpu301	Page:68 of 73	

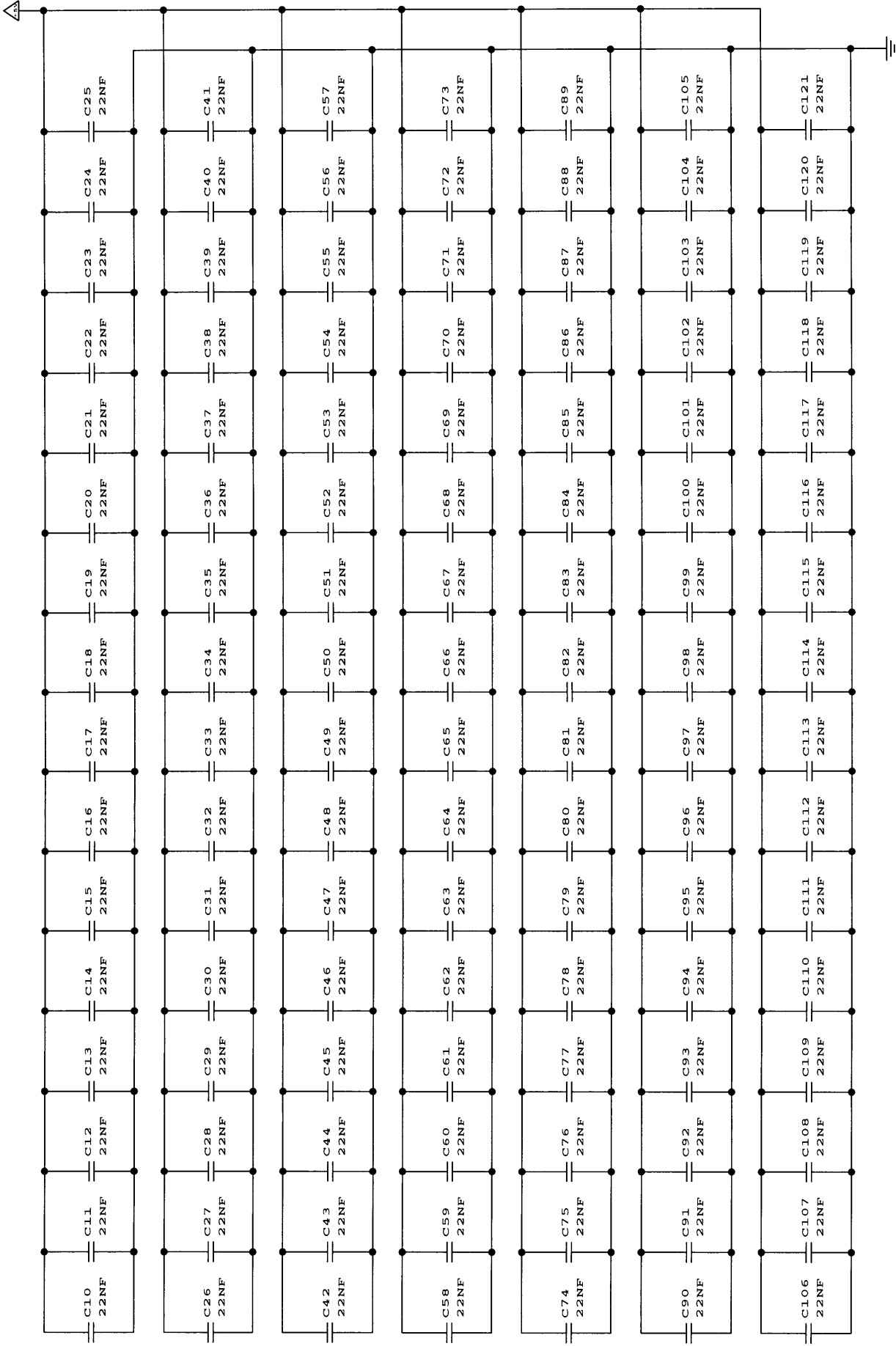
[3, 6, 9, 12, 51, 59, 60]
 LAD_R[63:0], LADP_R[7:0]



[3, 6, 9, 12, 52, 61] LCMD_R[7:0]
 [3, 6, 9, 12, 52, 61] LCMDP_R
 [3, 6, 9, 12, 18, 25, 61] LAVAL_R
 [3, 6, 9, 12, 18, 25, 52, 61] LDVAL_R

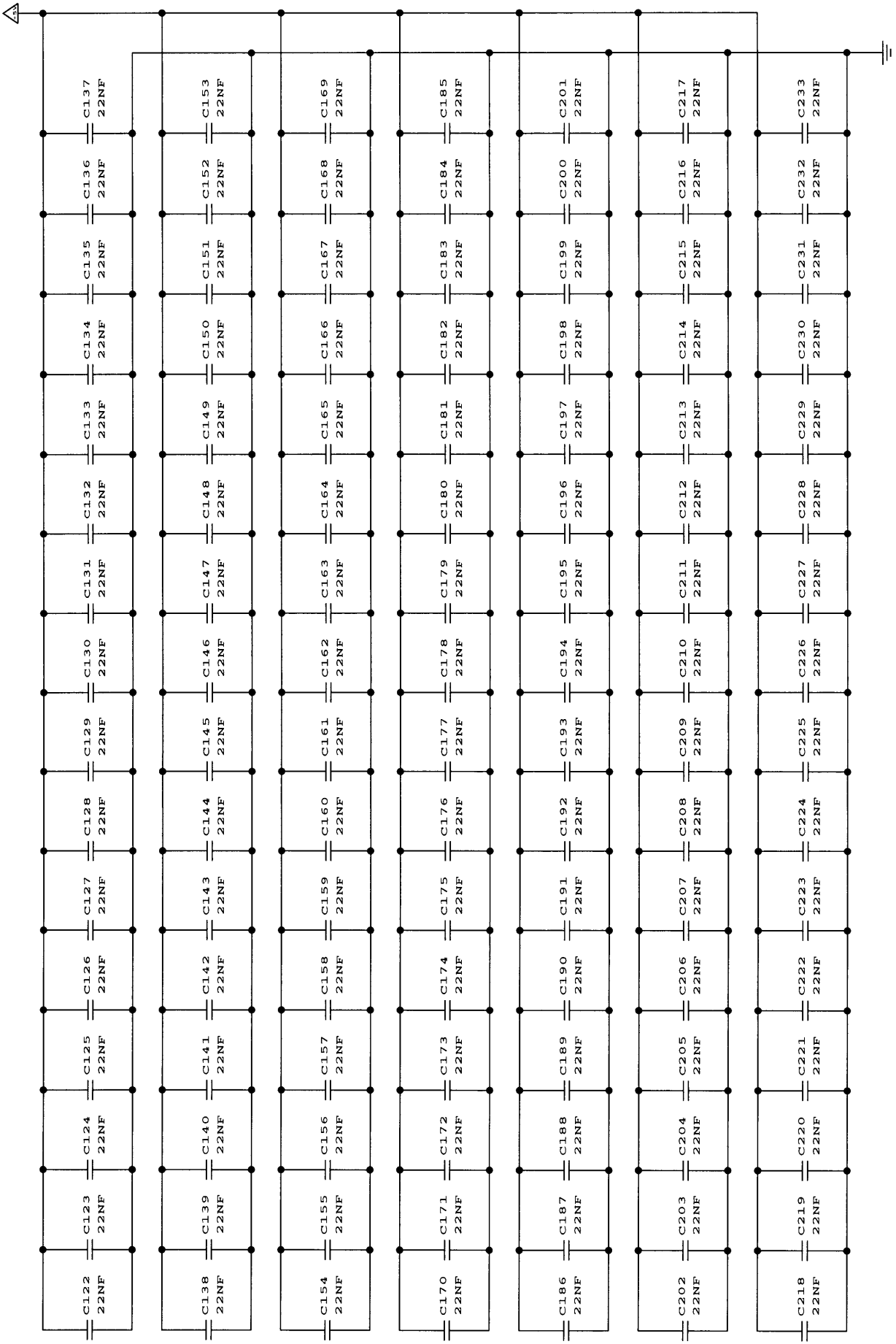
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Internal local bus term.	
Issue 2			
Issue 3			
	File: cpu301	Page: 69 of 73	

Chip level decoupling: 22nF/chip, 2*22nF/MACH chip, and 8*22nF/agent chip.



dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Decoupling capacitors	
Issue 2			
Issue 3		File: cpu301	

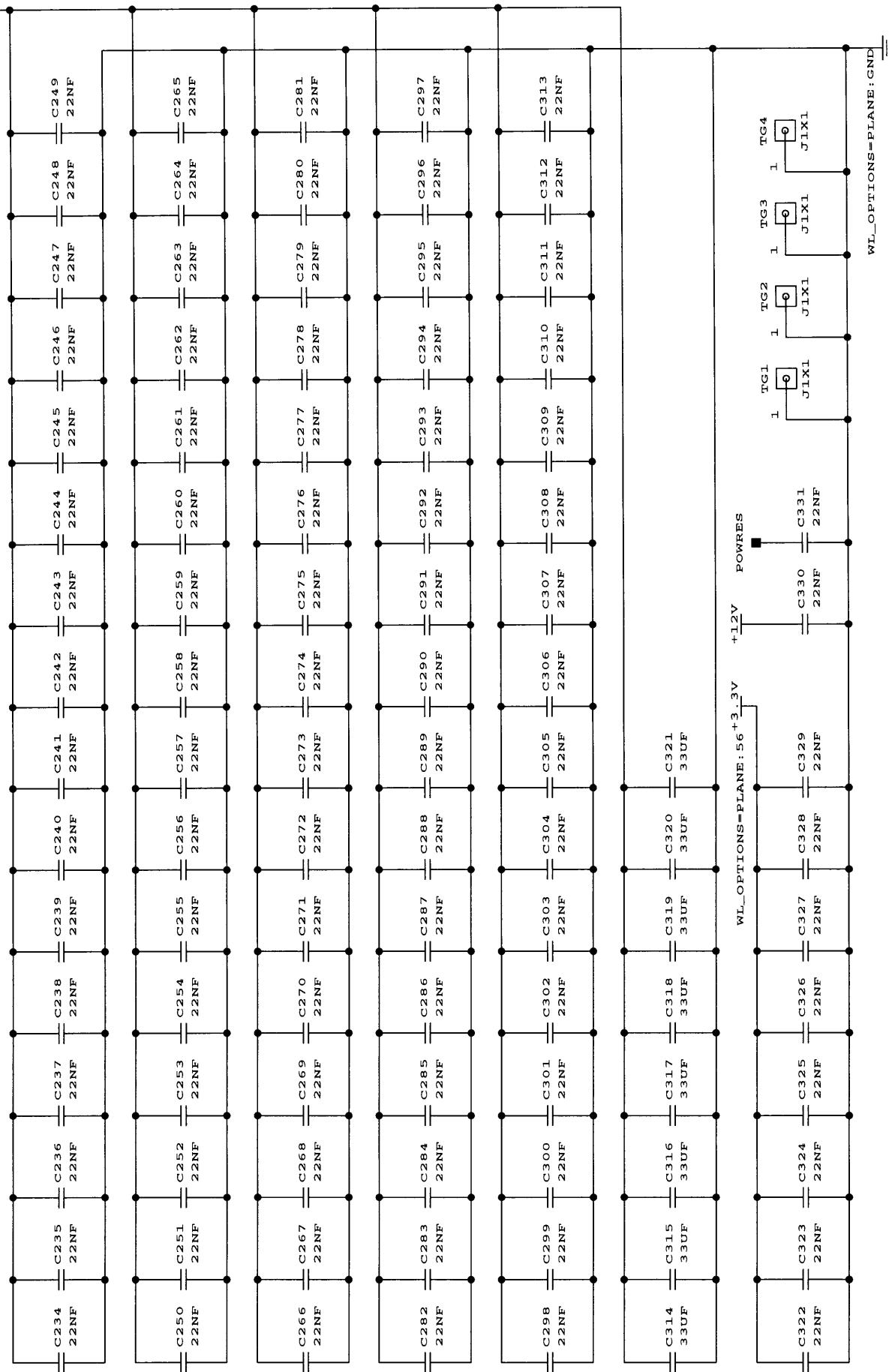
Chip level decoupling: 22nF/chip, 2*22nF/MACH chip, and 8*22nF/agent chip.



dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Decoupling capacitors	
Issue 2			
Issue 3		File: cpu301	
		Page: 71 of 73	

Chip level decoupling: 22nF/chip, 2*22nF/MACH chip, and 8*22nF/agent chip.

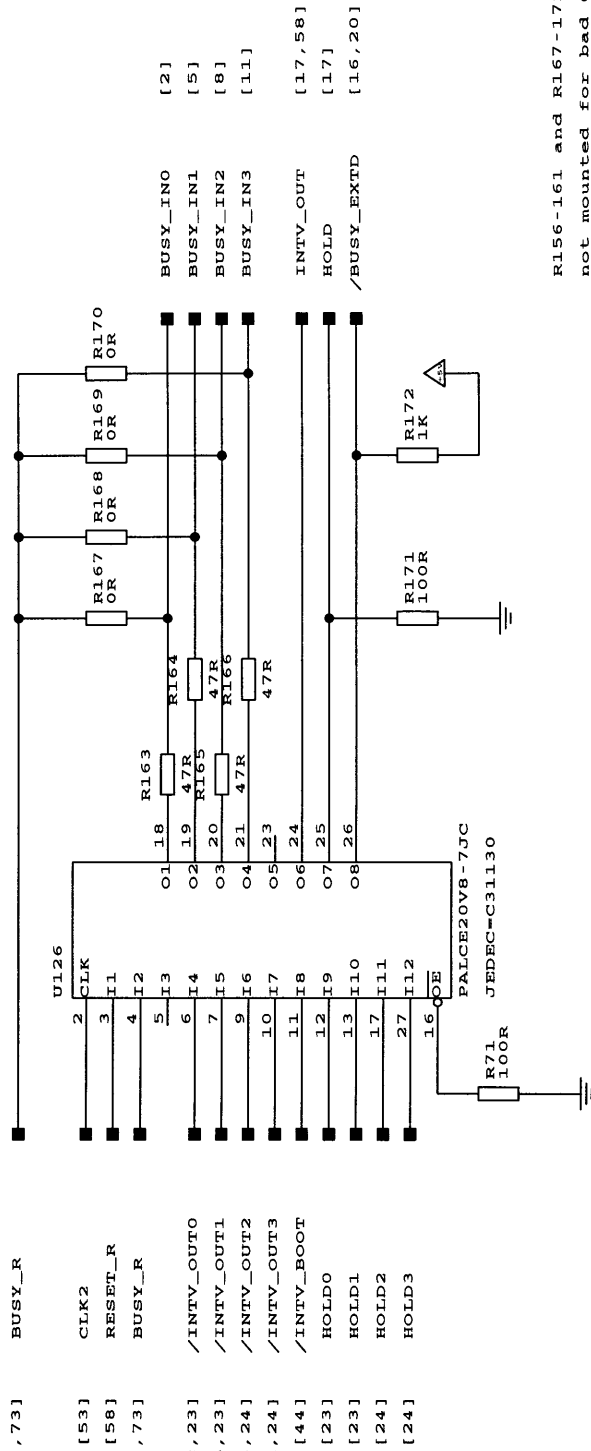
WL_OPTIONS=PLANE:VCC



Decoupling at bus connector: 22nF for 3.3 V, 12 V, POWRES and 33uF for 5 V.

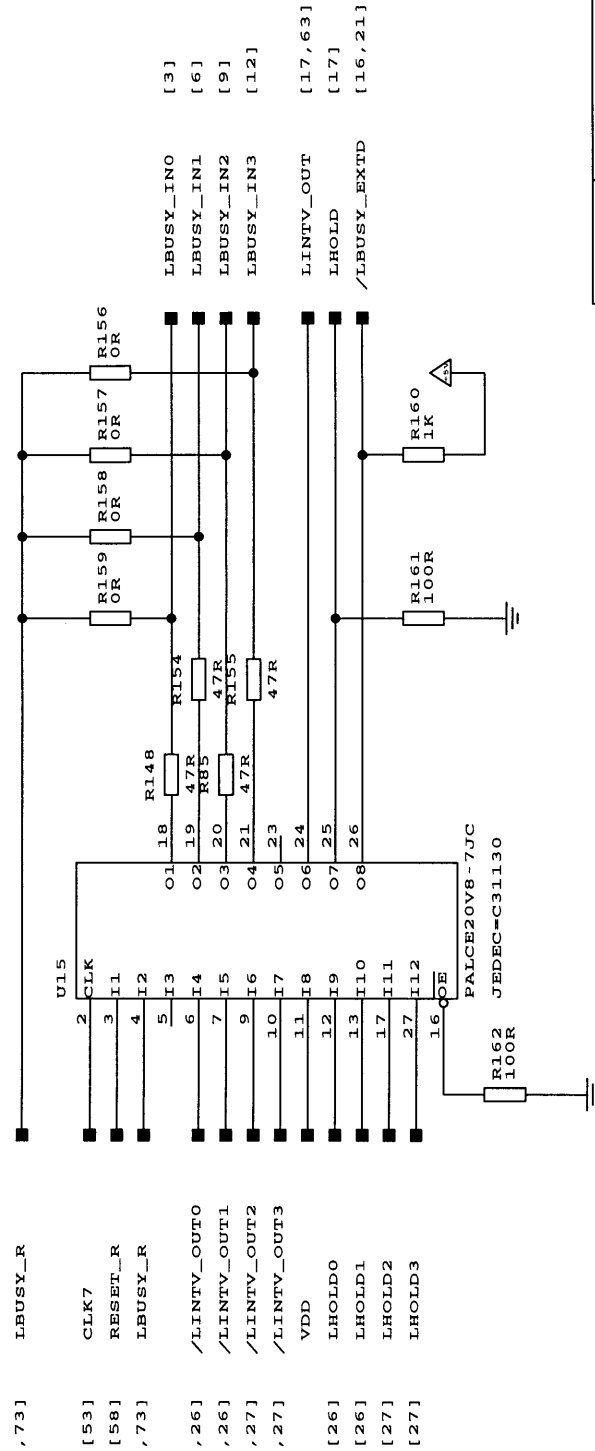
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Decoupling capacitors	
Issue 2			
Issue 3			

[20, 40, 44, 47, 58, 73]



R156-161 and R167-172 are not mounted for bad CA302.

[21, 50, 63, 73]



dde		Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module	
Issue 1	950131	Controlled intervention for bad CA302	
Issue 2			
Issue 3			

PARTS LIST

Module: CPU300-1

Date: 950911 Page: 1/2

Part no	Device	Qty	Comp
99020850	22NF	315	C1, C10-313, C322-331
99020851	4.7UF	1	C2
99020849	33UF	8	C314-321
99021413	SSF-LXH1032ID	5	D1, D5, D9, D13, D17
99021412	SSF-LXH1032GD	4	D2, D6, D10, D14
99000227	74S1050D	7	D18-24
99022027	1.000MHZ	1	OSC1
99020305	100R	54	R1-5, R5A, R6-9, R15, R17, R19, R21 R23, R25, R27, R29, R31-32, R35 R38-39, R41, R45, R60, R65, R68, R71 R108-109, R112-113, R116-117 R120-121, R124-125, R128-129 R132-133, R136-137, R139, R141 R143, R145, R147, R149, R151, R153 R162
99020307	82R	2	R10, R12
99020308	130R	2	R11, R13
99020306	220R	33	R14, R16, R18, R20, R22, R24, R26, R28 R30, R106-107, R110-111, R114-115, R118-119, R122-123, R126-127, R130-131, R134-135, R138, R140, R142, R144, R146, 148, R150, R152
99020303	4K7	7	R33, R42, R66-67, R69-70, R92
99020327	3K	2	R34, R43
99020301	1K	14	R40, R44, R50, R52, R54, R56, R62-64, R86-90
99020309	560R	17	R46-48, R72-84, R91
99020325	47R	8	R85, R148, R154-155, R163-166
99020322	0R	8	R51, R55, R58-59, R95, R98, R101, R104
99022235	Netw. 4820P-002-472	1	R36
99022234	Netw. 4820P-002-102	1	R93
99011701	CA302	4	U1, U3, U5, U7
99002411	74F1808D	2	U9, U11
99002412	74F1832D	2	U10, U12
99000831	74AS20D	1	U13
99010804	PALCE20V8-7JC	1	U126
99002413	74F377D	1	U17
99010404	PAL22V10-7JC	1	U18
99010216	PAL20R8-5JC	1	U21
99010902	MACH110-20JC	3	U20, U78, U85
99010904	MACH210-12JC	4	U22, U138-139, U141
99002222	74FCT16823BTPV	6	U26-27, U81-84
99011223	MCM6706AJ10	10	U28-29, U33-34, U38-39, U43-44, U140, U142
99002223	74FCT16244ATPV	5	U30, U35, U40, U45, U77
99002221	74FCT521BTSO	9	U31-32, U36-37, U41-42, U46-47, U70
99010908	MACH220-15JC	1	U71
99012095	N82S123AA / Am27S19AJC	2	U72-73
99002219	74FCT16501ATPV	1	U74
99002408	74F280BD	3	U75-76, U80
99012114	AM29C040-120JC	1	U79
99010604	PALCE16V8H-7JC	2	U86-87
99011218	CY7B991-7JC	1	U96
99005033	MC100H641FN	1	U97
99002500	FB2031BB	10	U98-107

PARTS LIST

Module: CPU300-1

Date: 950911 Page: 2/2

<u>Part no</u>	<u>Device</u>	<u>Qty</u>	<u>Comp</u>
99002501	FB2033BB	4	U108-110,U123
99001040	74ALS240D	2	U124-125
99000472	74LS393D	3	U127-129
99002405	74F74D	2	U130-131
99000832	74AS30D	2	U133,U150
99010022	PAL16R6-5JC	1	U136
99002407	74F244D	1	U148
99000830	74AS1004D	1	U149
99040124	3M8062011549-5	16	X00-03,X10-13,X20-23,X30-33
99040111	AMP100147-1	3	X101-102,X104
99040110	AMP100145-1	1	X103
99023228	20-pin PLCC socket	5	U72-73,U86-87,U136
99023229	28-pin PLCC socket	3	U18,U21,U126
99023230	32-pin PLCC socket	1	U79
99023231	44-pin PLCC socket	7	U20,U22,U78,U85, U138-139,U141
99023232	68-pin PLCC socket	1	U71
99030350	PCB CPU301 Issue 2	1	
99068013	Front panel CPU300	1	
	Mech. parts CPU30x	1	

PARTS LIST

Module: CPU301-1

Date: 950911 Page: 1/2

<u>Part no</u>	<u>Device</u>	<u>Qty</u>	<u>Comp</u>
99020850	22NF	315	C1, C10-313, C322-331
99020851	4.7UF	1	C2
99020849	33UF	8	C314-321
99021413	SSF-LXH1032ID	5	D1, D5, D9, D13, D17
99021412	SSF-LXH1032GD	12	D2-4, D6-8, D10-12, D14-16
99000227	74S1050D	14	D18-31
99022027	1.000MHZ	1	OSC1
99020305	100R	54	R1-5, R5A, R6-9, R15, R17, R19, R21 R23, R25, R27, R29, R31-32, R35 R38-39, R41, R45, R60, R65, R68, R71 R108-109, R112-113, R116-117 R120-121, R124-125, R128-129 R132-133, R136-137, R139, R141 R143, R145, R147, R149, R151, R153 R162
99020307	82R	2	R10, R12
99020308	130R	2	R11, R13
99020306	220R	33	R14, R16, R18, R20, R22, R24, R26, R28 R30, R106-107, R110-111, R114-115, R118-119, R122-123, R126-127, R130-131, R134-135, R138, R140, R142, R144, R146, 148, R150, R152
99020303	4K7	7	R33, R42, R66-67, R69-70, R92
99020327	3K	2	R34, R43
99020301	1K	14	R40, R44, R50, R52, R54, R56, R62-64, R86-90
99020309	560R	17	R46-48, R72-84, R91
99020325	47R	8	R85, R148, R154-155, R163-166
99020322	0R	8	R51, R55, R58-59, R95, R98, R101, R104
99022235	Netw. 4820P-002-472	1	R36
99022234	Netw. 4820P-002-102	1	R93
99011701	CA302	8	U1-8
99002411	74F1808D	2	U9, U11
99002412	74F1832D	2	U10, U12
99000831	74AS20D	2	U13-14
99010804	PALCE20V8-7JC	2	U15, U126
99002413	74F377D	2	U17, U25
99010404	PAL22V10-7JC	2	U18-19
99010216	PAL20R8-5JC	2	U21, U23
99010902	MACH110-20JC	4	U20, U78, U85, U94
99010904	MACH210-12JC	8	U22, U24, U138-139, U141, U143-144 U146
99002222	74FCT16823BTPV	8	U26-27, U48-49, U81-84
99011223	MCM6706AJ10	20	U28-29, U33-34, U38-39, U43-44 U50-51, U55-56, U60-61, U65-66 U140, U142, U145, U147
99002223	74FCT16244ATPV	14	U30, U35, U40, U45, U52, U57, U62, U67 U77, U89-93
99002221	74FCT521BTSO	18	U31-32, U36-37, U41-42, U46-47 U53-54, U58-59, U63-64, U68-70, U88
99010908	MACH220-15JC	1	U71
99012095	N82S123AA / Am27S19AJC	2	U72-73
99002219	74FCT16501ATPV	1	U74
99002408	74F280BD	3	U75-76, U80
99012114	AM29C040-120JC	1	U79
99010604	PALCE16V8H-7JC	3	U86-87, U95

PARTS LIST

Module: CPU301-1

Date: 950911 Page: 2/2

<u>Part no</u>	<u>Device</u>	<u>Qty</u>	<u>Comp</u>
99011218	CY7B991-7JC	1	U96
99005033	MC100H641FN	1	U97
99002500	FB2031BB	20	U98-107, U111-120
99002501	FB2033BB	6	U108-110, U121-123
99001040	74ALS240D	2	U124-125
99000472	74LS393D	3	U127-129
99002405	74F74D	2	U130-131
99000832	74AS30D	4	U133-134, U150-151
99010022	PAL16R6-5JC	2	U136-137
99002407	74F244D	1	U148
99000830	74AS1004D	1	U149
99040124	3M8062011549-5	16	X00-03, X10-13, X20-23, X30-33
99040111	AMP100147-1	3	X101-102, X104
99040110	AMP100145-1	1	X103
99023228	20-pin PLCC socket	7	U72-73, U86-87, U95, U136-137
99023229	28-pin PLCC socket	6	U15, U18-19, U21, U23, U126
99023230	32-pin PLCC socket	1	U79
99023231	44-pin PLCC socket	12	U20, U22, U24, U78, U85, U94, U138-139, U141, U143-144, U146
99023232	68-pin PLCC socket	1	U71
99030350	PCB CPU301 Issue 2	1	
99068005	Front panel CPU301	1	
	Mech. parts CPU30x	1	

PLD list

Part no: 99750023
 Status: Preliminary
 Init: OHM

Module: CPU300-1
 Date: 950817

Pcb no:
 Page: 1 / 1

<u>Label</u>	<u>Pos.</u>	<u>Part no.</u>	<u>Type</u>	<u>X-pgm.</u>	<u>File</u>	<u>Checksum</u>
c31011	U18	99010404	PAL22V10-7JC		c31011.jed	5623
c31022	U136	99010022	PAL16R6-5JC		c31022.jed	3ED4
c31030	U20	99010902	MACH110-20JC		c31030.jed	B930
c31041	U21	99010216	PAL20R8-5JC		c31041.jed	6BC4
c31051	U22	99010904	MACH210-12JC		c31051.jed	88BD
c31061	U138	99010904	MACH210-12JC		c31061.jed	807D
c31071	U139	99010904	MACH210-12JC		c31071.jed	C79D
c31071	U141	99010904	MACH210-12JC		c31071.jed	C79D
c31080	U71	99010908	MACH220-15JC		c31080.jed	004F
c31090	U78	99010902	MACH110-20JC		c31090.jed	E876
c31100	U85	99010902	MACH110-20JC		c31100.jed	604D
c31110	U86	99010604	PALCE16V8H-7JC	R6	c31110.jed	234F
c31120	U87	99010604	PALCE16V8H-7JC	R8	c31120.jed	2470
c31130	U126	99010804	PALCE20V8H-7JC		c31130.jed	7914

PLD list

Part no: 99750020
 Status: Preliminary
 Init: OHM

Module: CPU301-1
 Date: 950817

Pcb no:
 Page: 1 / 1

<u>Label</u>	<u>Pos.</u>	<u>Part no.</u>	<u>Type</u>	<u>X-pgm.</u>	<u>File</u>	<u>Checksum</u>
c31011	U18	99010404	PAL22V10-7JC		c31011.jed	5623
c31011	U19	99010404	PAL22V10-7JC		c31011.jed	5623
c31022	U136	99010022	PAL16R6-5JC		c31022.jed	3ED4
c31022	U137	99010022	PAL16R6-5JC		c31022.jed	3ED4
c31030	U20	99010902	MACH110-20JC		c31030.jed	B930
c31041	U21	99010216	PAL20R8-5JC		c31041.jed	6BC4
c31041	U23	99010216	PAL20R8-5JC		c31041.jed	6BC4
c31051	U22	99010904	MACH210-12JC		c31051.jed	88BD
c31051	U24	99010904	MACH210-12JC		c31051.jed	88BD
c31061	U138	99010904	MACH210-12JC		c31061.jed	807D
c31061	U143	99010904	MACH210-12JC		c31061.jed	807D
c31071	U139	99010904	MACH210-12JC		c31071.jed	C79D
c31071	U141	99010904	MACH210-12JC		c31071.jed	C79D
c31071	U144	99010904	MACH210-12JC		c31071.jed	C79D
c31071	U146	99010904	MACH210-12JC		c31071.jed	C79D
c31080	U71	99010908	MACH220-15JC		c31080.jed	004F
c31090	U78	99010902	MACH110-20JC		c31090.jed	E876
c31100	U85	99010902	MACH110-20JC		c31100.jed	604D
c31100	U94	99010902	MACH110-20JC		c31100.jed	604D
c31110	U86	99010604	PALCE16V8H-7JC	R6	c31110.jed	234F
c31110	U95	99010604	PALCE16V8H-7JC	R6	c31110.jed	234F
c31120	U87	99010604	PALCE16V8H-7JC	R8	c31120.jed	2470
c31130	U126	99010804	PALCE20V8H-7JC		c31130.jed	7914
c31130	U15	99010804	PALCE20V8H-7JC		c31130.jed	7914

Supermax Field Change Notice no. 149

Module:	CPU300-1 and CPU301-1 CPU module
Date:	95.11.20 (Revision 1)

Editorial change:

This FCN149 replaces the earlier FCN149 dated 95.09.01. The latter refers to the position of the FCN PROM as U72, which correctly should be U73. The device is still **FCN149**.

Category:

- Production change.
- Mandatory field change.

Corrects the error:

The module hitherto has been unable to operate at a bus frequency of 33.3 MHz. In addition, the module name on the front panel may be wrong.

Needed tools:

Hand tools.

Supermax FCN149-kit, stock number 95101490, consisting of:

- One PAL device labelled **C31022**.
- Five PAL labels **C31051**, **C31061**, 2x **C31071**, and **C31130**.
- Front panel marked **CPU300**.
- One PROM device labelled **FCN149**.

Description:

- U136: PAL **X31021** -> **C31022**.
- U22: PAL label **X31051** -> **C31051**.
- U138: PAL label **X31061** -> **C31061**.
- U139: PAL label **X31071** -> **C31071**.
- U141: PAL label **X31071** -> **C31071**.
- U126: PAL label **X31130** -> **C31130**.

- U96: Connect CY7B991 pin 4 and 32 (GND) together. Pin 1 is marked by an indented dot.
- U96: Connect CY7B991 pin 6 and 13 (via-hole, GND) together.
- R60: Remove the resistor located in the center of the connector side.
- If the module ID PROM claims that the module is a CPU300 then change the module front panel and return the old to the factory.
- Finally, replace the FCN PROM in U73 with the new **FCN149**.

Circuits involved:

Due to the idiosyncrasies of the ISO9000 requirements I shall reiterate the circuits involved:

- U136, U22, U138, U139, U141, U126: PAL
- U96: CY7B991
- R60: Resistor
- U73: PROM

Previous FCN:

None.

PRODUCTION CHANGE NOTICE

PCN NO:	95-5 (revision 1)
Date:	November 23, 1995
FCN:	149
Author:	OHM
Module:	CPU300-1 and CPU301-1 CPU module
Part No:	99750023 and 99750020
Introduced from:	TBD by Production

Editorial change:

This PCN 95-5 replaces the earlier PCN 95-5 dated August 25, 1995. The latter refers to the position of the FCN PROM as U72, which correctly should be U73. Further, a reference to the PCN 95-7 is deleted.

Reasons for change:

With this change the module will be capable of operating at a bus frequency of 33.3 MHz. This PCN is thus a prerequisite for PCN 95-6. In addition, the module name on the front panel may be wrong.

Description of change:

U136: PAL x31021 -> c31022.
U22: PAL label x31051 -> c31051.
U138: PAL label x31061 -> c31061.
U139: PAL label x31071 -> c31071.
U141: PAL label x31071 -> c31071.
U126: PAL label x31130 -> c31130.
U96: Connect pin 4 and 32 (GND) together.
U96: Connect pin 6 and 13 (via-hole, GND) together.
R60: Remove it.

If the module ID PROM claims that the module is a CPU300 then change the front panel accordingly.

Finally, replace the FCN PROM in U73 with the new FCN149.

Stock:

All modules must be modified.

Enclosures:

Field change notice no. 149.