CPU300-303
Design document

Name:	CPU300-303 Design document
Date:	951130
Author:	ohm
Version:	1.2
Document ID:	1-0216
Status:	Preliminary

Contents **page**

1 REVISION HISTORY

Changes from version 1.1 to 1.2:

The document now defines CPU300-303 as follows:

CPU300: 1 MB snooper. Global bus only.
CPU301: 1 MB snooper.
CPU302: 4 MB snooper. Global bus only.
CPU303: 4 MB snooper.

An old reference to the local TTL interface has been removed.

Changes from version 1.0 to 1.1:

The reference list has been updated.

The LED labels have been changed.

Version 1.0:

Although this is the initial version of the document it is based on the MCU301 Design document from which it differs in the following respects:

The local bus has been changed to all BTL, thus the global and local bus are symmetrical.

All processor modules on a base module must have the same secondary cache size, thus reducing the number of sets of snooper address jumpers from two to one.

The CPU301 and CPU302 support 1-MB and 4-MB secondary cache, respectively, thus the above set of jumpers is fixed for each module.

The boot PROM is a flash EEPROM for re-use.

2 REFERENCES

1. MCU301/302/304 Kravspecifikation
   1-0101

2. SPC/3 System bus specification
   1-0201

3. MIPS R4000 Microprocessor User's Manual
   Integrated Device Technology, Inc.
   Part number M8-00040

4. MIPS R4000 Microprocessor User's Manual Errata
   Revision 2.0
   March 13, 1992
   MIPS Technology Products Group

5. CPU Agent Design document
   1-0203

3 INTRODUCTION

The CPU module for the SPC/3 computer series consists of a base module CPU300-303 and one to four detachable processor modules, e.g. PMD301 with a 75-MHz R4400MC and 1-MB secondary cache. The base modules, which each take up one backplane position, are defined as follows:

CPU300: 1 MB snooper. Global bus only.
CPU301: 1 MB snooper.
CPU302: 4 MB snooper. Global bus only.
CPU303: 4 MB snooper.

Each of the up to four processors modules connects to a global and a local bus interface through two agents. These identical agents, which are implemented with highly complex gate arrays, provide data buffers, address registers, and control for the commands that originate in the associated processor and for those commands on the associated bus that require cache coherency.

Both the global and local bus interface are BTL.

There is a global control space, which contains the following special registers intended for identification, control, error logging, interrupt, and debugging.

Status register
Control register
Module ID
Module FCN
Interrupt register
Debug register
Processor module identification register
Bus error register

There is a control, interrupt, and debug register for each subposition corresponding to each possible processor module. The global control space may be accessed both via the global bus and by the four processors although a processor must not write to the interrupt register of its own subposition.

The local control space, although structured in the same way, only contains interrupt registers.

In addition to the control spaces there are separate address spaces for the internal registers of each agent, these may only be accessed by the associated processor.

The module is equipped with a 1/2-MB detachable boot flash EEPROM, which is common to all processors.

Finally, the choice of little or big endians is made by a fixed signal on the bus.

4 SPECIFICATIONS

4.1 Performance

Bus frequency	33.3 MHz
Bus burst rate	267 MB/s
Bus read rate (32 words)	178 MB/s
Bus write rate (32 words)	213 MB/s

4.2 Secondary cache requirements

Block size	32 words
Cache size, CPU300-301	1 MB
Cache size, CPU302-303	4 MB

4.3 Interfaces

System bus interface:

SPC/3 system bus [2], both global and local bus.

Indicators on front panel:

PARITY ERROR	Red LED that indicates a parity error on the global or local bus.
ERROR(0-3)	One red programmable LED per processor.
BUSY(0-3)	One green programmable LED per processor.
A(0-3)	One green programmable LED per processor.
B(0-3)	One green programmable LED per processor.

Internal processor/base module interface:

SAD(63:0)	System interface address/data
SADP(7:0)	System interface address/data parity
SCMD(8:0)	System interface command
SCMDP	System interface command parity
/VALIN	System interface valid to processor
/VALOUT	System interface valid from processor
/EXTRQ	System interface request from agents
/RELEASE	System interface release from processor
/RDRDY	Read ready
/WRRDY	Write ready
/IVDACK	Invalidate acknowledge
/IVDERR	Invalidate error
RCLK(1:0)	Receive clocks (identical)
TCLK(1:0)	Transmit clocks (identical)
/INT	Error interrupt
/NMI	Non-maskable interrupt

SRE	Selective reset
C2MS	2-ms period clock
C262MS	262-ms period clock
PM_ID(3:0)	Processor module identification
/PRESENT	Processor module present
BIG	Big endian

4.4 Dimensions

Board height	415.0 mm
Board depth	335.0 mm
Module pitch	30.0 mm

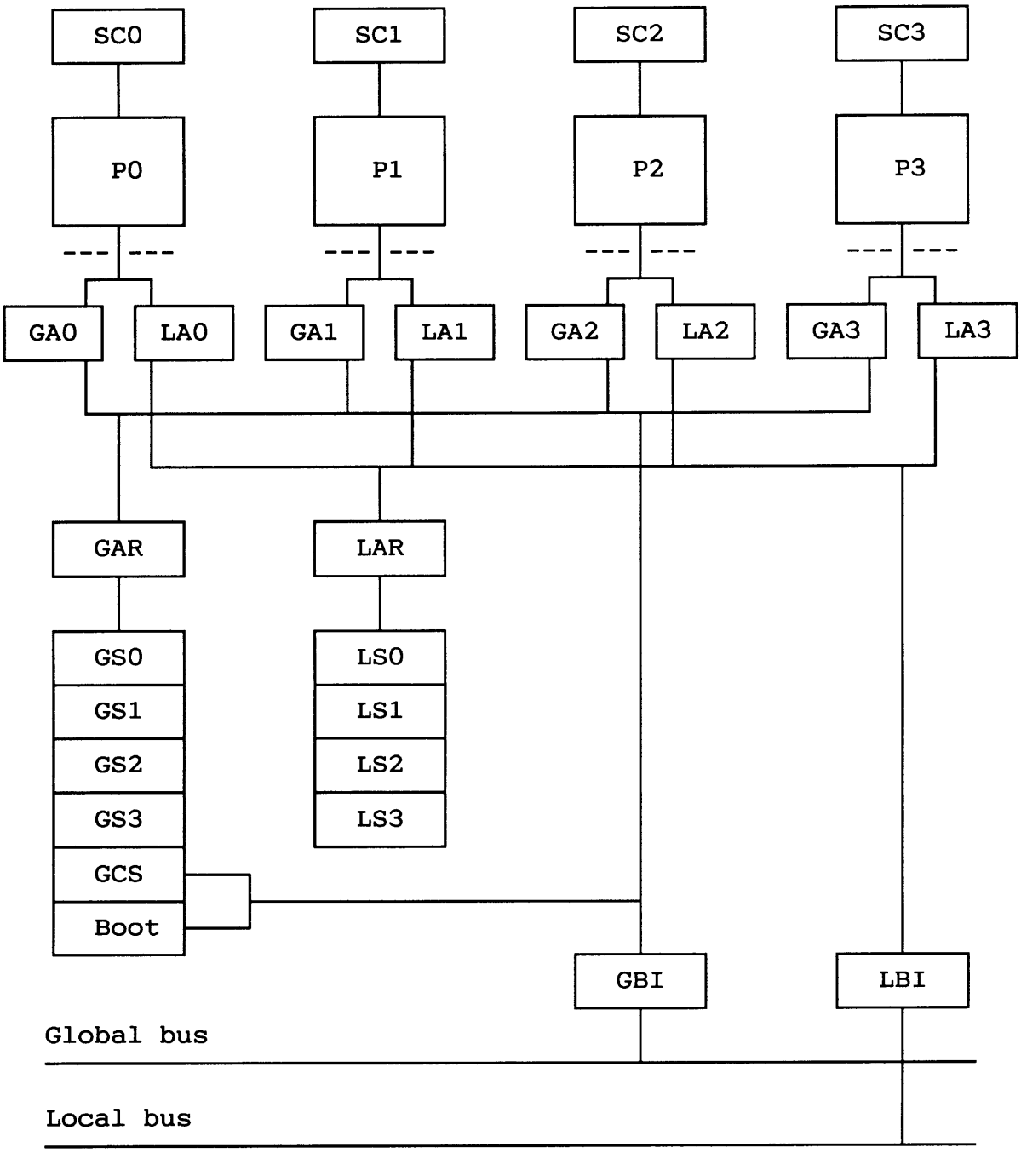
4.5 Power

Voltage		5 V ± 5 %
Current	(CPU300/302)	5 A max.
Current	(CPU301/303)	9 A max.

5 Functional description

The block diagram below shows the base module CPU300-303 below the connector interface (---) and four processor modules above.

Each processor module consists of a processor (P) with a secondary cache (SC) and a connector. Associated with each possible processing module, but placed on the base module are a global and a a local agent (GA and LA), and a global and a local snooper (GS and LS). In addition, the base module provides a global and a local bus interface (GBI and LBI) with associated address registers (GAR and LAR), a global control spaces (GCS), and finally a boot PROM. A part of the global control space and all of the local control space are inside the respective agents.



5.1 Base module

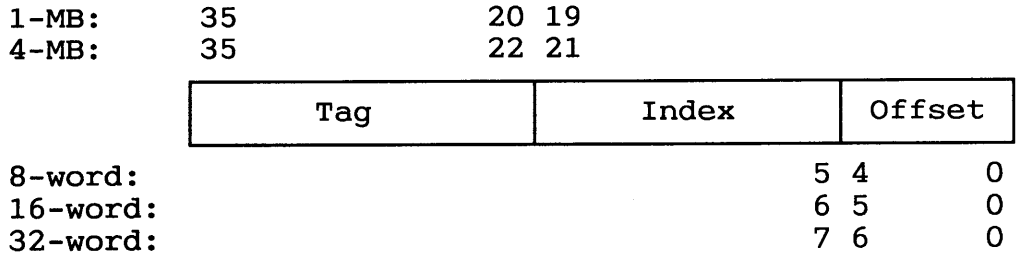
The main components of the base module are eight agents, two bus interfaces, two address registers, eight snoopers, a global control space, and a boot PROM.

The agent is described in [5] and contains all data buffers, data and address registers, and control required to link a processor to a bus interface. An agent also contains an agent space, which is only accessible from the associated processor, and an interrupt register and a debug register, which are a part of the respective control spaces.

One of the important tasks of the agent is to sequence transactions from the processor and system bus correctly when they pertain the same cache line. Another is to ensure continued snooping on a retained link address, when the link is evicted from the secondary cache and retained by the processor, whereby the link address is evicted from the snooper and therefore must be retained in the agent.

Each bus interface contains a number of registered BTL transceivers and a bus master control including arbitration control.

The task of a snooper is to keep a copy of the physical address tags of the secondary cache tags such that bus snooping can take place without disturbing the respective processor excessively. The format of the snooper depends on the size and block size of the secondary cache:



The index gives the entry in the snooper, and, in order for a snoop hit to occur, the tag must match the corresponding bits of the bus address. The offset does not participate in the comparison, and there is no valid bit. The contents of the snoopers are undefined upon reset.

The format of the snoopers, which must correspond to the associated secondary caches, is selected with fixed jumpers given a limit of 15 index bits corresponding to a maximum set size of 32768 entries. Surplus tag bits need not be excluded as they merely become redundant. The CPU300-301 modules are set for 1-MB / 32-word, while the CPU302-303 modules are set for 4-MB / 32-word.

When a cache line is replaced the read and the write are normally bundled together in a command called read with write forthcoming. In this case the write address tag will disappear from the snooper before disappearing from the secondary cache as it is overwritten in the snooper by that of the read, thus creating the possibility of non-coherency. Rather than try do juggle with both tags, the snooper must force hit until the start of the next command from the agent, which is a late but safe indication that the write address tag no longer is present in the secondary cache.

In addition to each snooper, which already does a good job of filtering coherency requests to the processor, there is an extension dubbed the supersnooper, which to the extent possible tracks the state changes in the secondary cache and prevents non-exclusive coherent read requests from reaching the processor if the state is shared or invalid. The contents of the supersnoopers are undefined upon reset.

The global control space contains a number of special registers as mentioned in the introduction. The control for the control space includes an address comparator that can detect a control space access to this module and a simple state machine that can perform the required access. The module FCN PROM is mounted in a socket to allow easy replacement.

There is a 1/2-MB boot PROM providing reset, diagnostic, and debugging code. The boot PROM is located at the beginning of the address range 0x01FC00000 through 0x01FFFFFFF, where the former is the physical reset address of the processor. This address range is, alas, right in the memory space. Thus, when a read address falls in this range and the boot PROM is not mapped out, as controlled by a bit in the control register of the global agent, the boot PROM must intervene and supply the data as a cache slave thus pre-empting the memory slave. The boot PROM, which is implemented with a 512 K by 8-bit flash EEPROM, is mounted in a socket.

When a master issues an access with an address for which there is no matching slave a missing target acknowledge will result. This works fine for a write, but for a read the responsible processor would wait forever on the missing 'last data element' because the agent does not provide it instead. Therefore, a dummy block generator is implemented in each bus interface to take care of this case.

6 PROGRAMMING INFORMATION

6.1 Processor

Programming information for the processor can be found in [3, 4].

The physical address space as seen from a processor consists of a global and local space, each subdivided into a memory, agent, and control space. A processor can only access its own agent spaces, while the memory and control spaces are accessible by all processors on the bus in question. The global and local control address spaces are described below. All address formats are shown in [2].

The interrupt register of the processor, whose format is shown below, contains a non-maskable interrupt (NMI), four general interrupts (I5-I2), a timer interrupt (TIM), and an error interrupt (ERR).

NMI	I5	I4	I3	I2	TIM	ERR
6	5	4	3	2	1	0

These bits result from the OR'ing of the respective bits in the two agents, and, in case of bit 0, also from the OR'ing of the bits in the Bus error register, more specifically the global and local bus parity error interrupts, and the debug interrupt. Only the timer in the global agent is active.

All interrupts are level-sensitive, thus the processor must remove an interrupt when it is accepted, but in order to so the source of the interrupt must be known. This is a problem for the general interrupts unless each in software is assigned to only one agent, thus the use of local interrupts is discouraged.

Accesses to the address space 0x01FC00000 through 0x01FFFFFFF may, under control of a bit in the control register of the appropriate global agent, be directed at either memory or the 1/2-MB boot PROM, which is located at the start of the address space and contains reset, diagnostic, and debugging code.

The selection of little or big endians is determined by a fixed signal on the system bus.

The states of the snoopers and supersnoopers are, like those of the secondary caches, undefined upon reset.

6.2 Agent space

For a description of the agent address space, please, refer to [5].

There are four programmable LEDs labelled ERROR(0-3), BUSY(0-3), A(0-3), and B(0-3) on the front panel for each of the four possible processor modules. They are controlled by the associated global agent control register bit 6 and 7, and local agent control register bit 6 and 7, respectively.

6.3 Control space

The CPU module has a global and a local control space, which are both divided into subpositions and contain a number of special registers intended for identification, configuration, error logging, interrupt, and debug. These registers have varying bit widths, but are all right justified within double words (64 bits), and any access less than a double word must take into account the subtle differences between little and big endians.

The global control space comprises all of the following special registers, while the local control space only comprises the interrupt register. Below is for every register or group of registers listed whether it can be read, written, or cleared along with its hexadecimal byte offset relative to the start of the control address space of the module.

Register	Access	Offset
Status register	Read/clear	0
Control register	Write	100
Module ID	Read	200
Module FCN	Read	300
Interrupt register	Write	400
Debug register	Write	500
Processor module register	Read	600
Bus error register	Read/clear	700

The function and format of the individual registers are described in the following. Reserved bits (r) must be 0 when written, and are undefined when read. Bits 16 through 63 are reserved, unless otherwise noted.

6.4 Status register

The Status register indicates bus parity errors found by this module. Individual bits may be cleared by writing ones in the respective positions, and the bits are all cleared by bus reset.

r	r	r	r	r	r	r	r	r	r	r	r	r	r	LPE	GPE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

GPE: Global parity error.

LPE: Local parity error.

6.5 Control register

There is a Control register for every subposition, and each contains a bit for selective reset of the corresponding processor. The bits are all set by bus reset.

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	SRE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SRE: Selective reset.

6.6 Module ID

The Module ID consists of a 32-byte string stored in 32 consecutive double words. The byte offset given earlier applies to the first double word.

r	r	r	r	r	r	r	r	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ID(7:0): Single byte of module Identification string.

The format of the string is given in [2].

6.7 Module FCN

The Module FCN consists of a 32-byte string stored in 32 consecutive double words. The byte offset given earlier applies to the first double word.

r	r	r	r	r	r	r	r	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FCN(7:0): Single byte of module Field Change Notice string.

The format of the string is given in [2].

6.8 Interrupt register

The Interrupt register, which is 32 bits wide, is used to write interrupts. There is an Interrupt register for every subposition in both the global and the local control space, and it is not possible for a master to write to its own register.

P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

r	r	r	r	r	r	r	r	r	NMI	I5	I4	I3	I2	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

I(5:2): Interrupts. Provides a direct path to the corresponding bits of the Interrupt register of the

processor.

NMI: Non-maskable interrupt. Provides a direct path to the NMI bit of the Interrupt register of the processor.

P(15:0): Peripheral interrupts. New bits are OR'ed to old ones, and the bits may be cleared by the processor.

6.9 Debug register

The Debug register is used to write a double byte to a processor during debug. There is a Debug register for every subposition, and it is not possible for a master to write to its own register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

D(15:0): Debug data.

6.10 Processor module register

The Processor module register indicates the presence and identity of each processor module.

M33	M32	M31	M30	M23	M22	M21	M20	M13	M12	M11	M10	M03	M02	M01	M00
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Mi(3:0): Identity of module i.

No module is present in position i if Mi=15.

6.11 Bus error register

There is a Bus error register for every subposition, and each indicates interrupts caused by a bus parity error or a debug request. Individual bits may be cleared by writing ones in the respective positions, and the bits are all cleared by bus reset.

r	r	r	r	r	r	r	r	r	r	r	r	r	DBI	LPI	GPI
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

GPI: Global parity error interrupt.

LPI: Local parity error interrupt.

DBI: Debug interrupt.

CPU300-303 Diagrams

CPU300: 1 MB snooper. Only global bus components mounted.
CPU301: 1 MB snooper.
CPU302: 4 MB snooper. Only global bus components mounted.
CPU303: 4 MB snooper.

Processor/agent interface

1 Connectors 0
2 Global agent 0
3 Local agent 0
4 Connectors 1
5 Global agent 1
6 Local agent 1
7 Connectors 2
8 Global agent 2
9 Local agent 2
10 Connectors 3
11 Global agent 3
12 Local agent 3
13 Programmable LEDs
14 Reset counters
15 Gating towards processors
16 Gating towards system bus

Bus control

17 Global and local output enable control
18 Pull-down for address and data valid
19 Global and local bus request decoder
20 Global bus arbitration
21 Local bus arbitration

Snooper control

22 Global snooper control
23 Global super snooper 0-1
24 Global super snooper 2-3
25 Local snooper control
26 Local super snooper 0-1
27 Local super snooper 2-3

Address and command registers and snoopers

28 Global and local command register
29 Global address register
30 Global snooper 0
31 Global snooper 1
32 Global snooper 2
33 Global snooper 3
34 Local address register
35 Local snooper 0
36 Local snooper 1
37 Local snooper 2
38 Local snooper 3

Global control space, boot, and dummy block generator

39 Global control space decode
40 Global control space control
41 Module ID and FCN PROMs
42 Processor module ID register
43 Global control space transceiver
44 Boot control

45 Boot PROM
46 Boot register
47 Global dummy block generator
48 Global data identifier output register

Local control space and dummy block generator

49 Local control space decode and target acknowledge
50 Local dummy block generator
51 Local dummy data
52 Local data identifier output register

Clock

53 Clock distribution

Bus interface

54 Global address/data transceiver
55 Global address/data transceiver
56 Global command and valid transceiver
57 Global bus request transceiver
58 Global control transceiver
59 Local address/data transceiver
60 Local address/data transceiver
61 Local command and valid transceiver
62 Local bus request transceiver
63 Local control transceiver
64 Connector (row 1-25)
65 Connector (row 26-50)
66 Connector (row 51-75)
67 Connector (row 76-100)

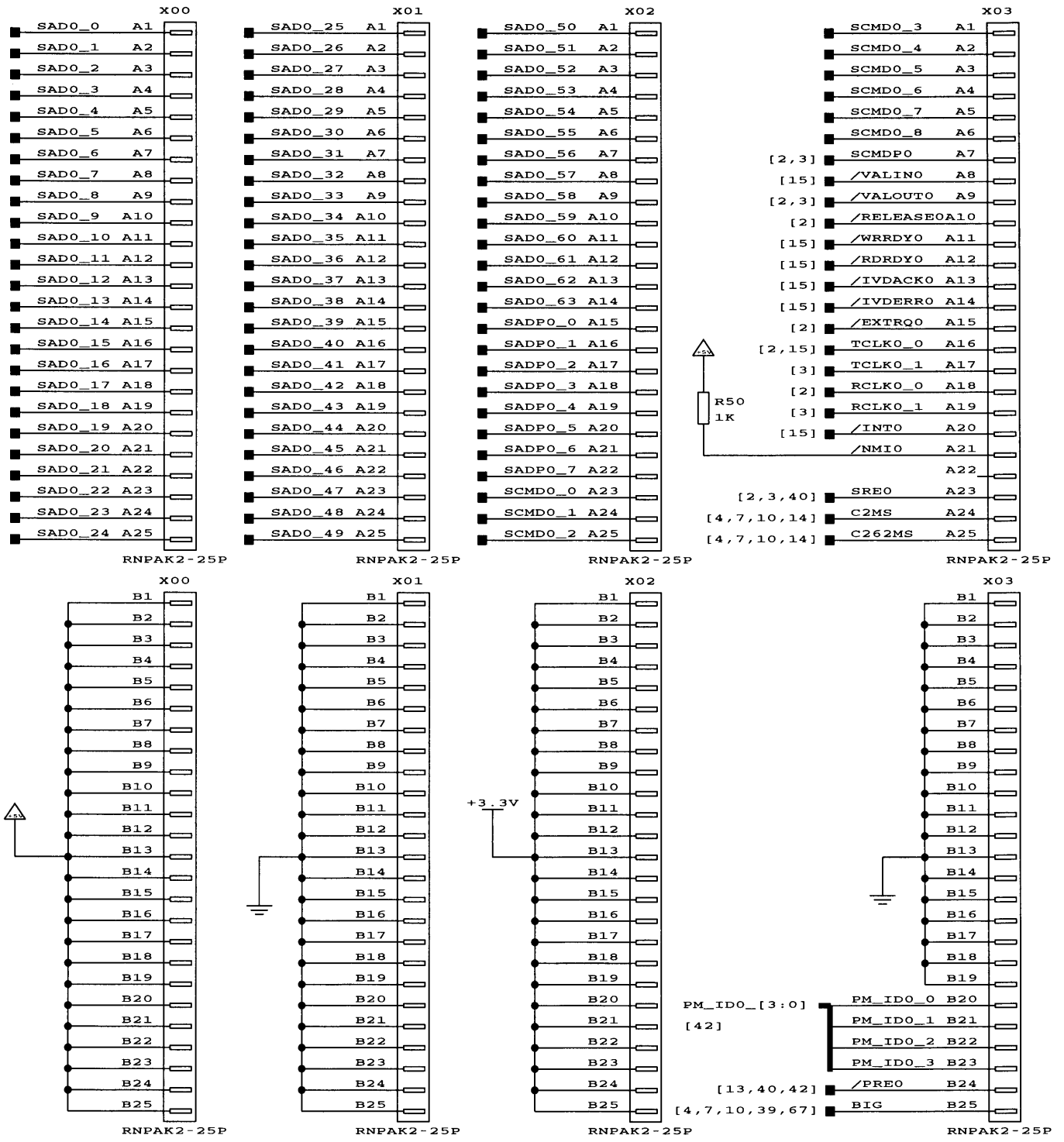
Termination and decoupling

68 Internal global bus termination
69 Internal local bus termination
70 Decoupling capacitors
71 Decoupling capacitors
72 Decoupling capacitors

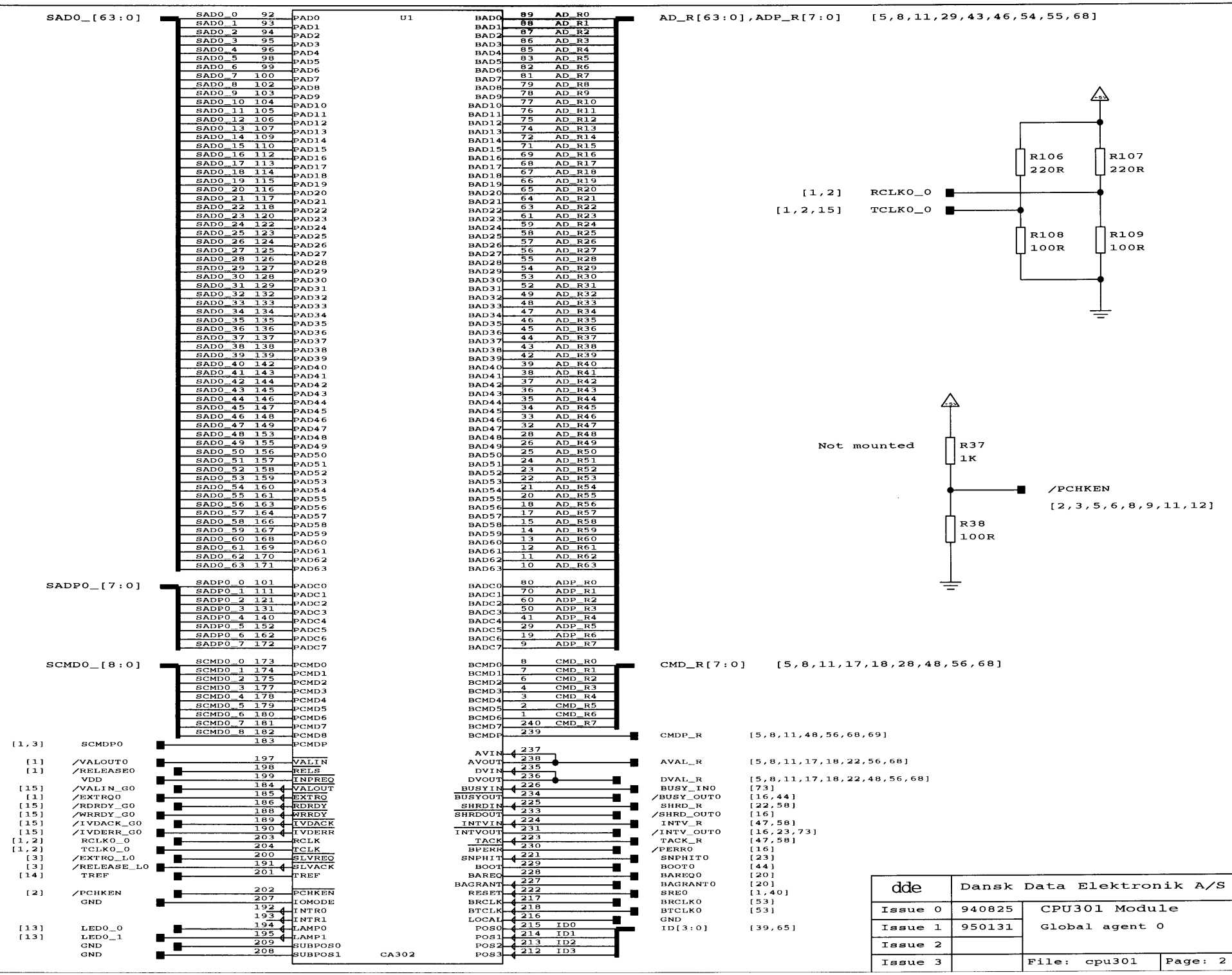
Fix of bad agent

73 Controlled intervention for bad CA302

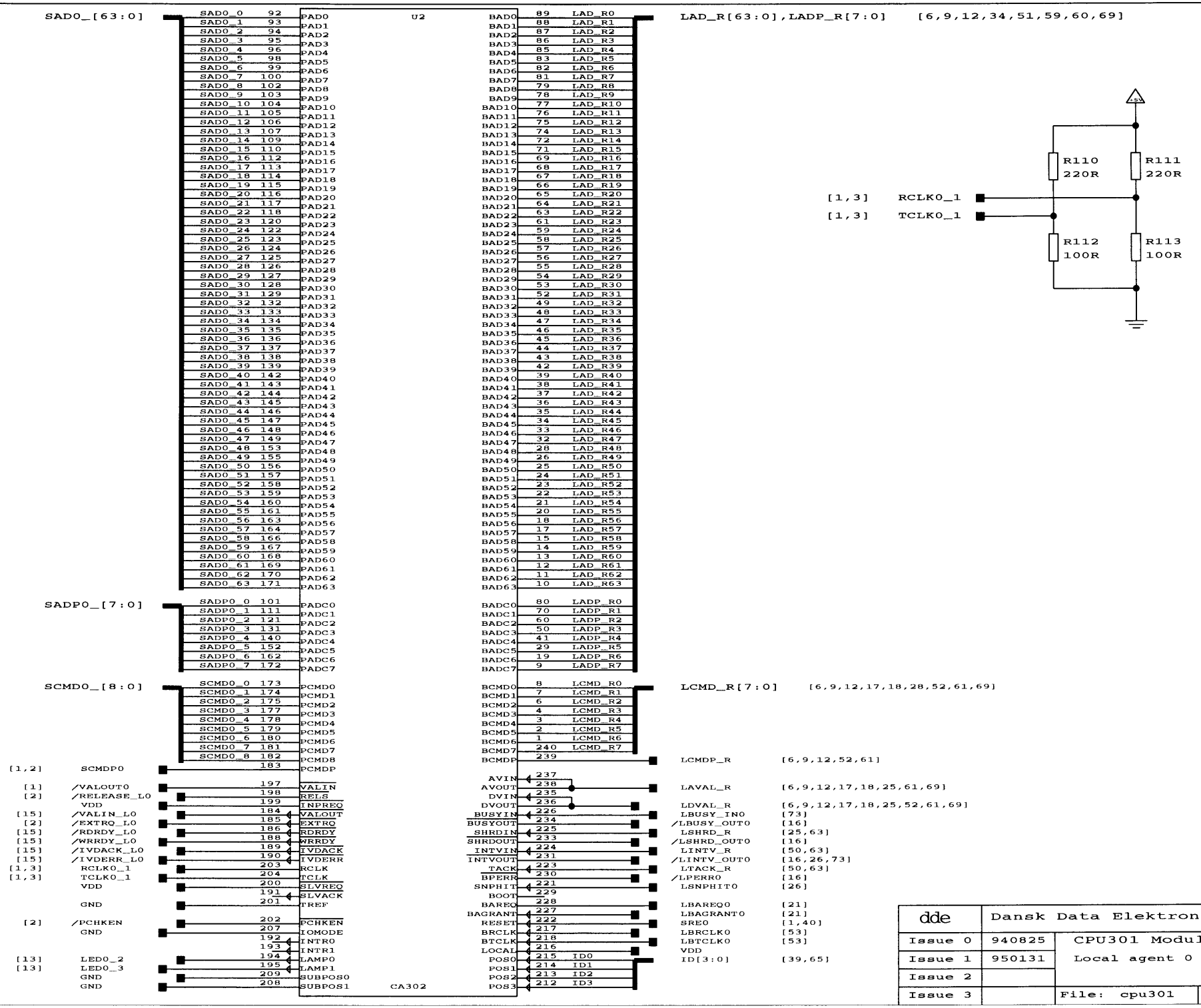
(Page 73 only present for CPU30x-1)



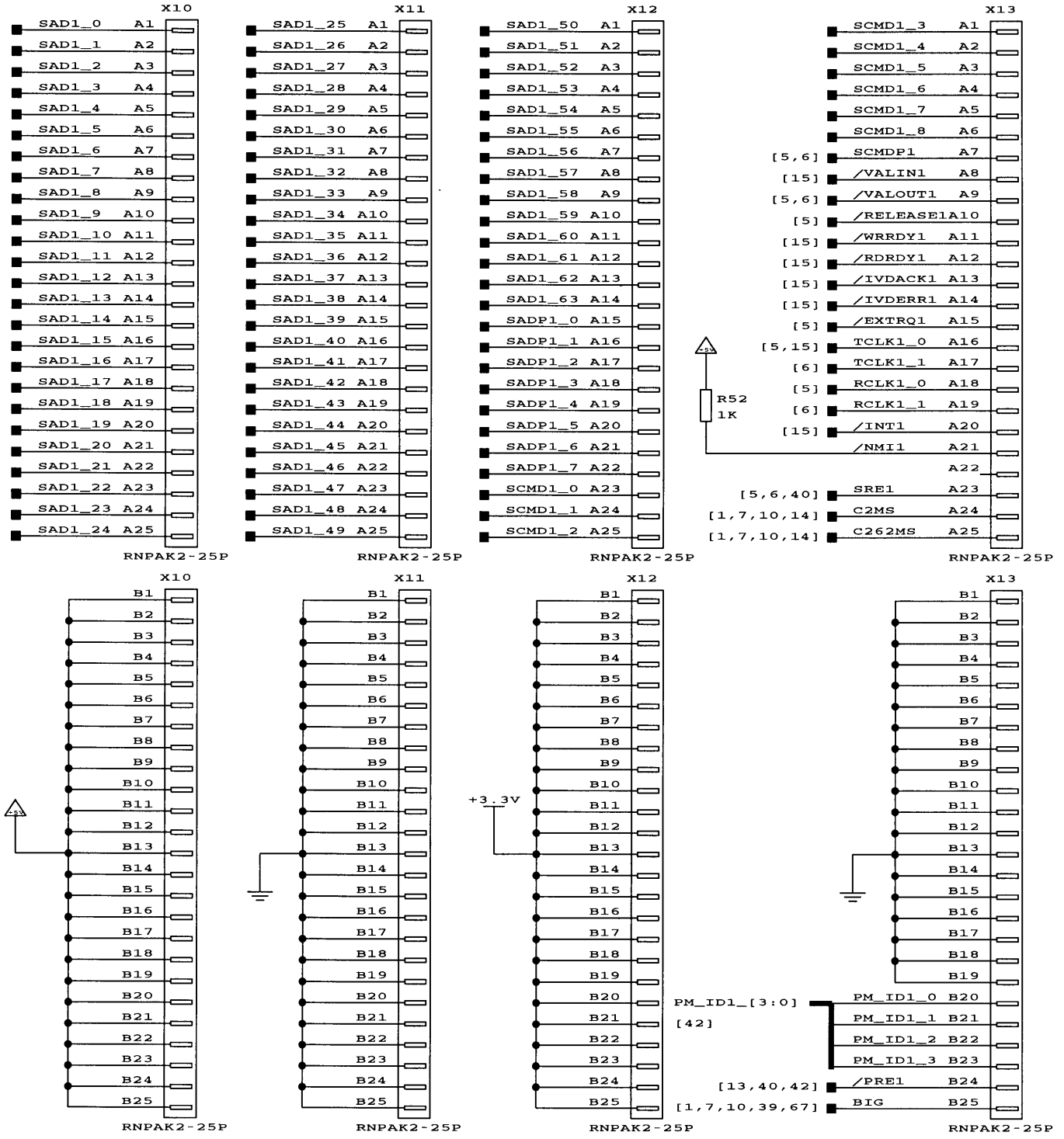
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connectors 0	
Issue 2			
Issue 3		File: cpu301	Page: 1 of 73



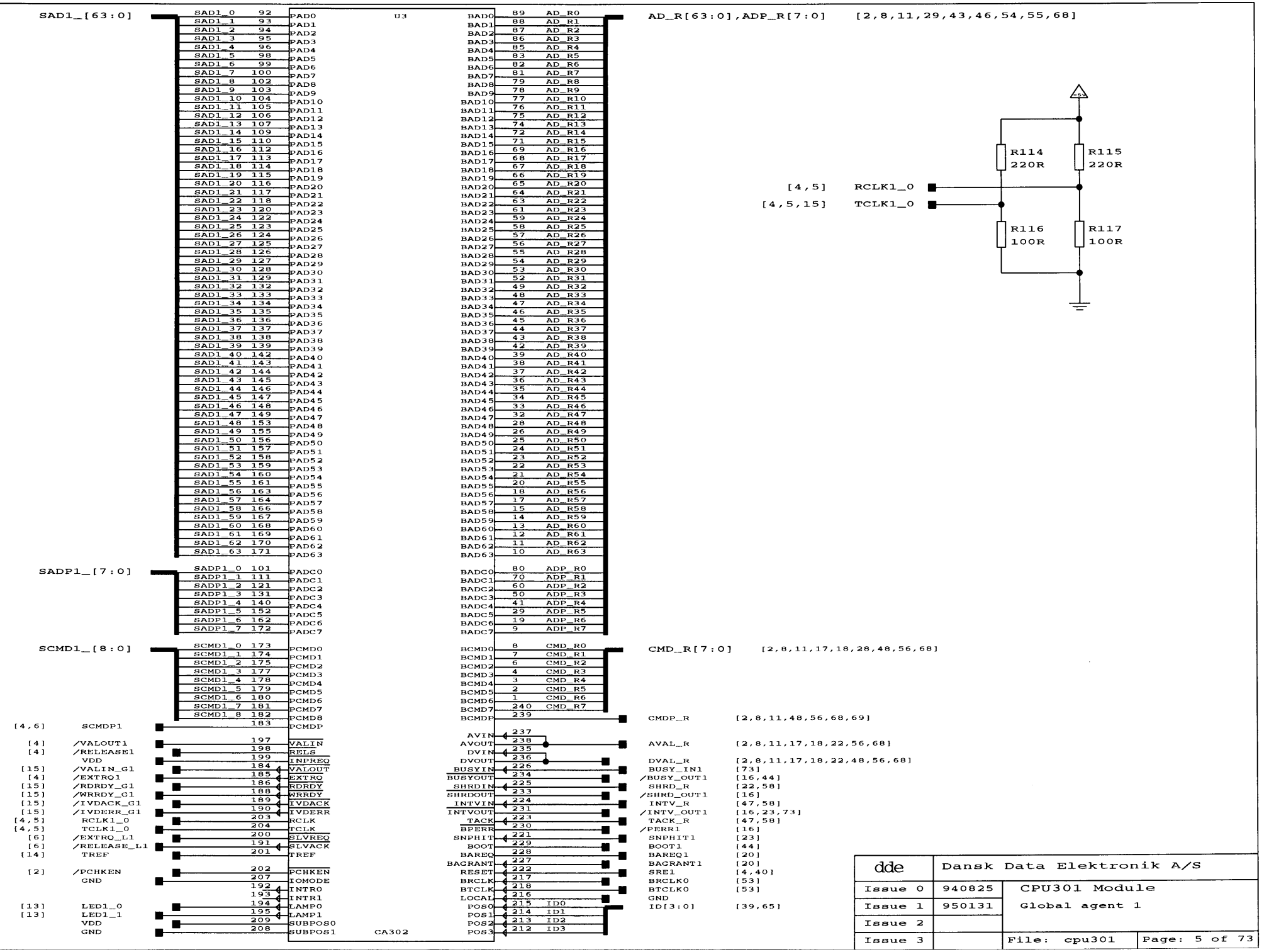
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global agent 0	
Issue 2			
Issue 3		File: cpu301	Page: 2 of 73



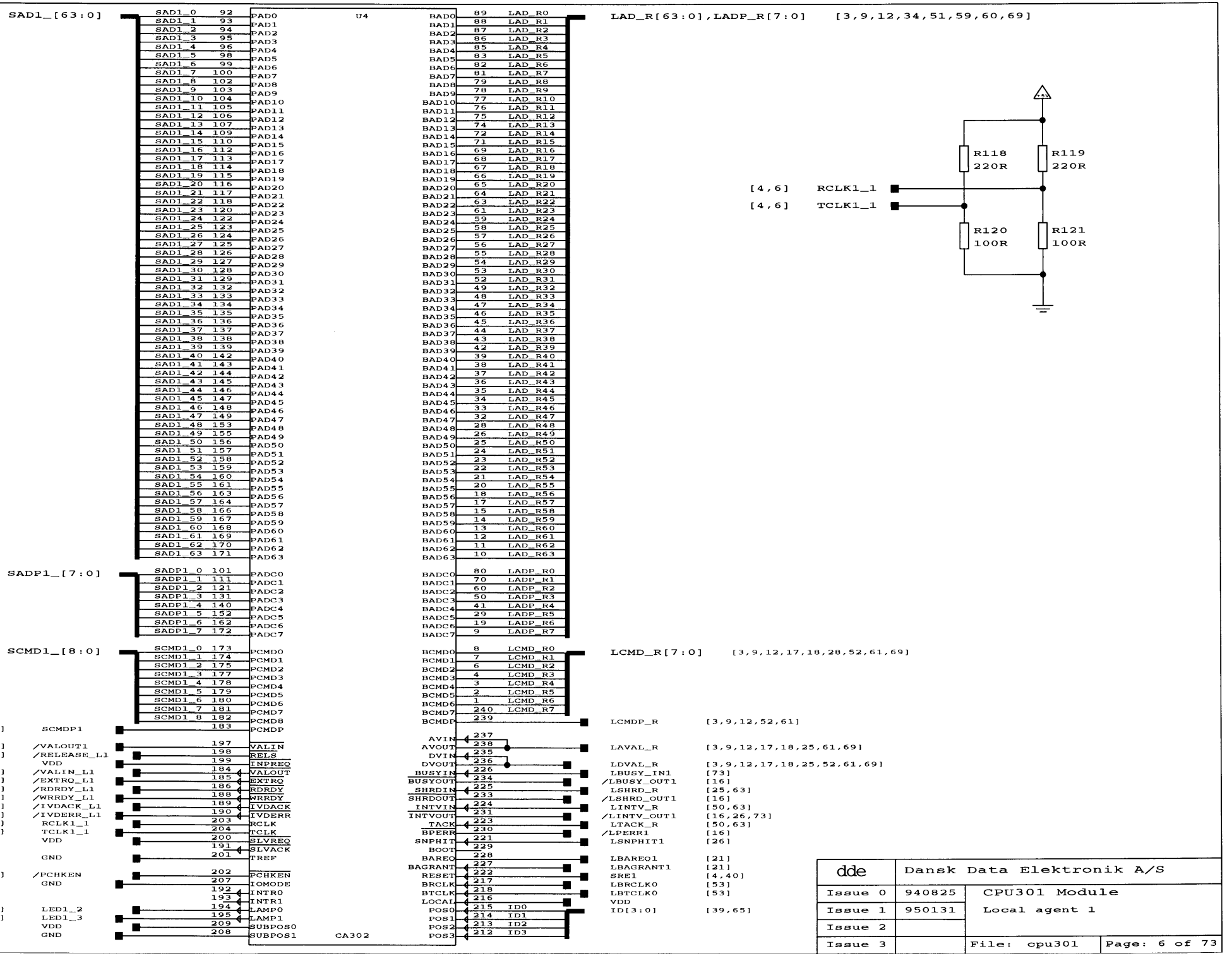
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local agent 0	
Issue 2			
Issue 3		File: cpu301	Page: 3 of 73



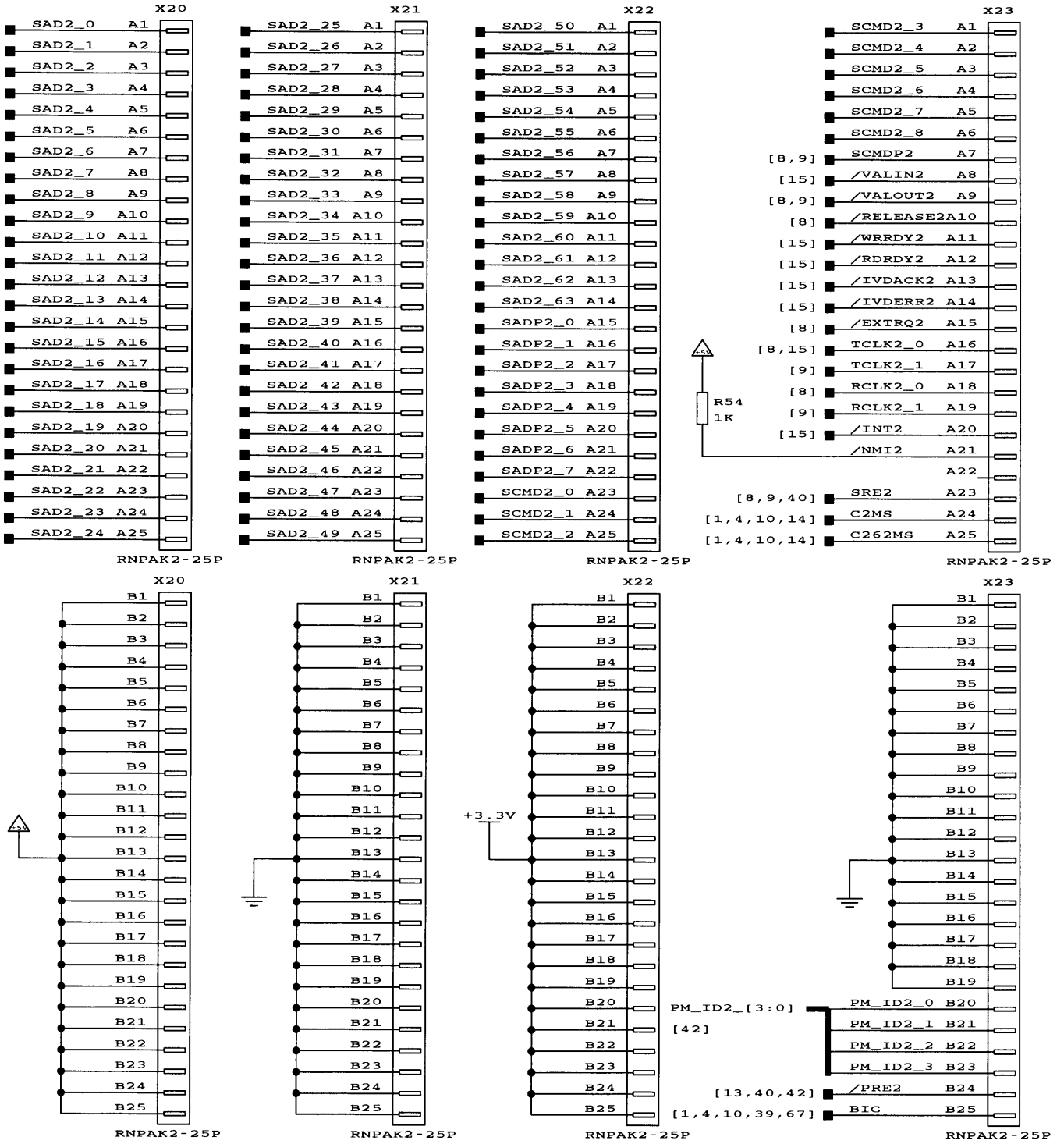
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connectors 1	
Issue 2			
Issue 3		File: cpu301	Page: 4 of 73



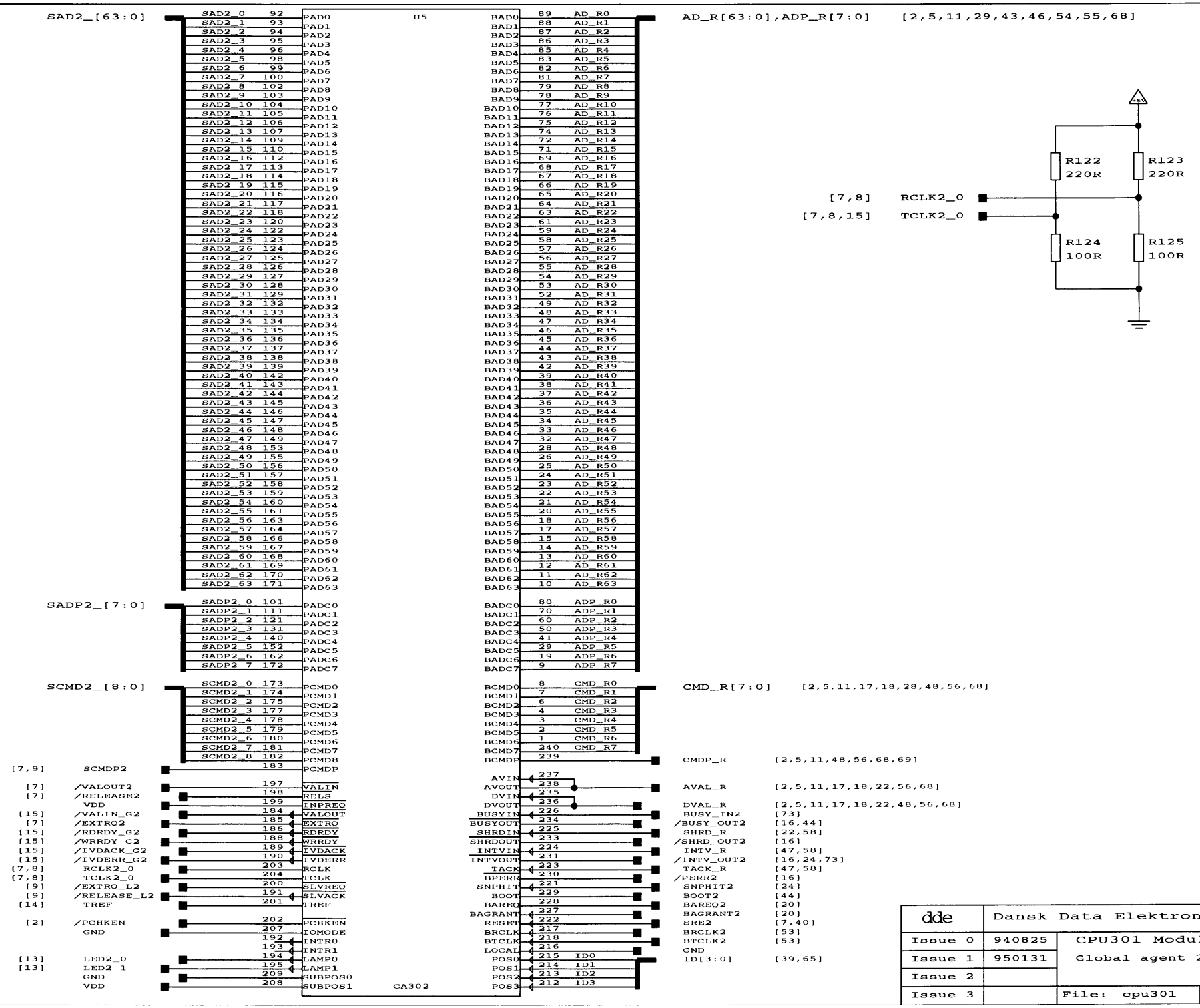
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global agent 1	
Issue 2			
Issue 3		File: cpu301	Page: 5 of 73



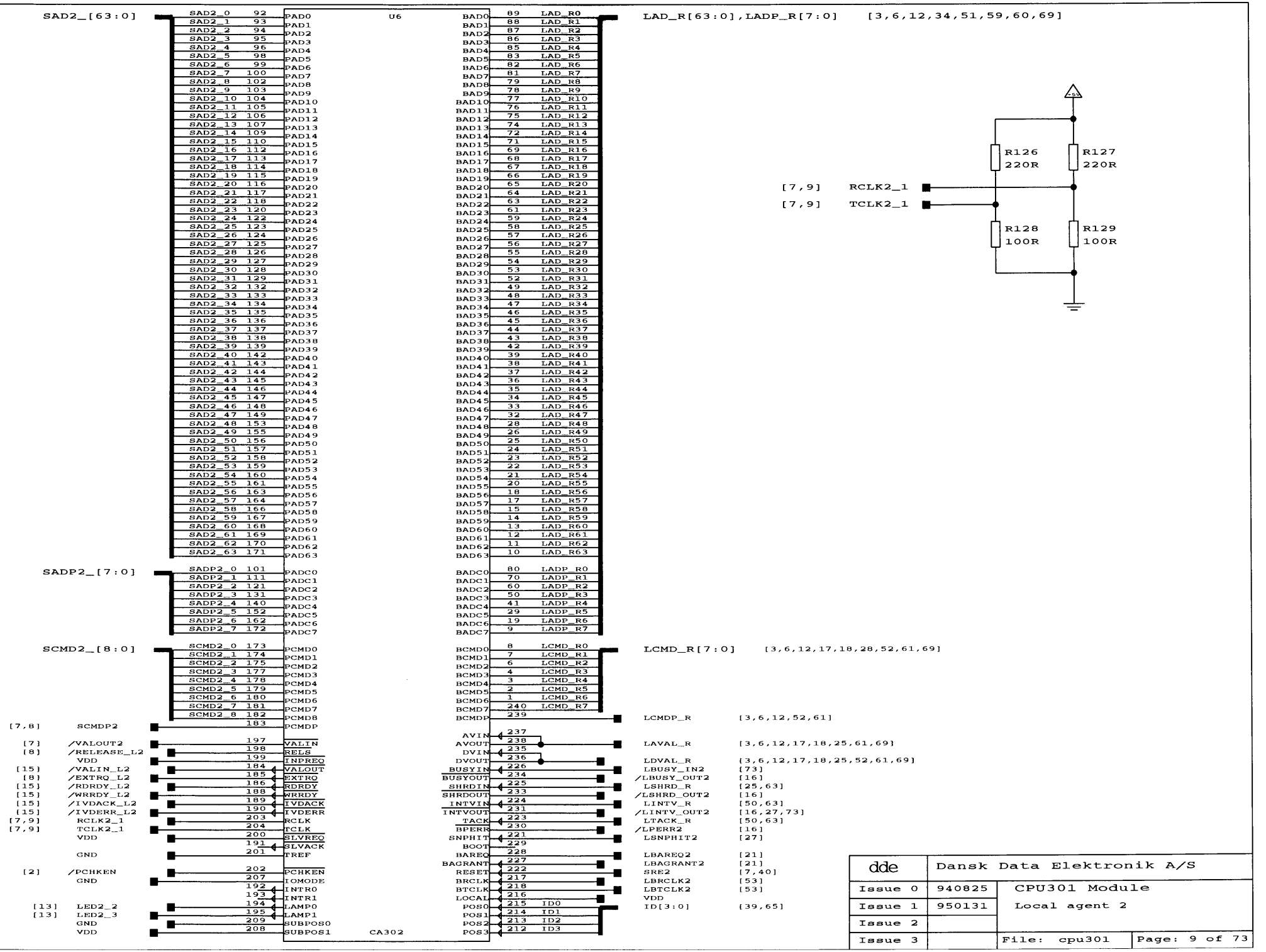
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local agent 1	
Issue 2			
Issue 3		File: cpu301	Page: 6 of 73



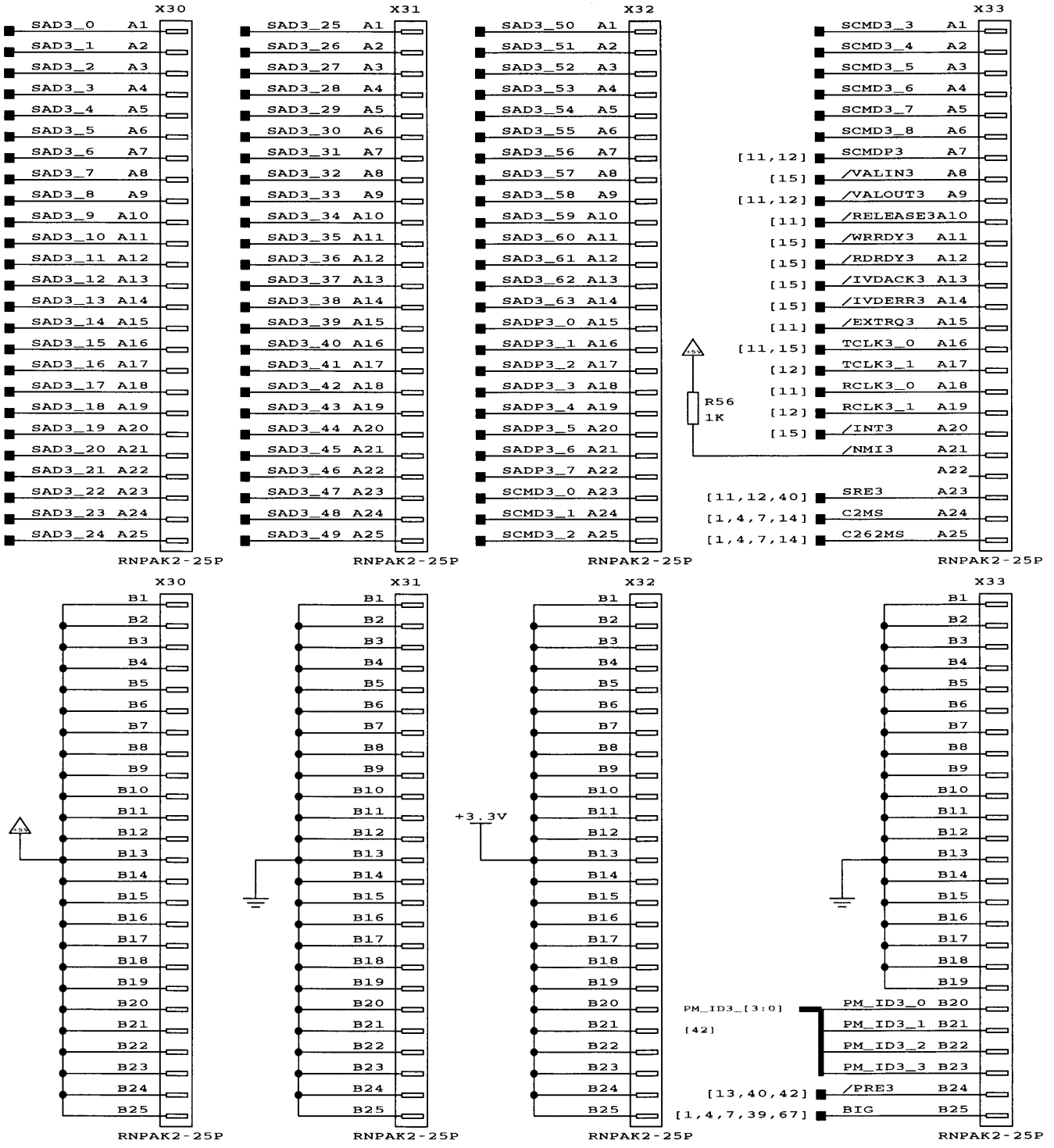
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connectors 2	
Issue 2			
Issue 3		File: cpu301	Page: 7 of 73



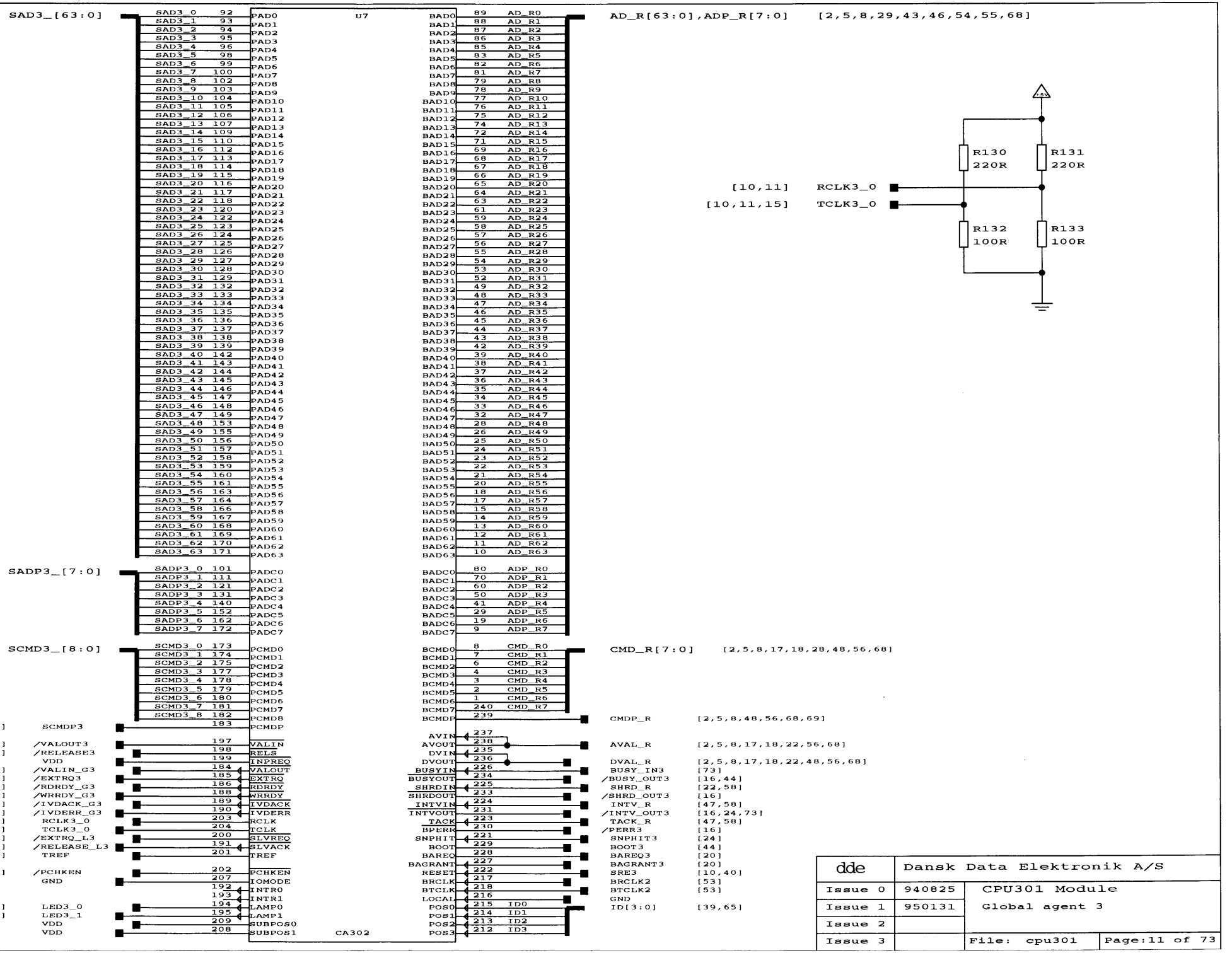
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global agent 2	
Issue 2			
Issue 3		File: cpu301	Page: 8 of 73



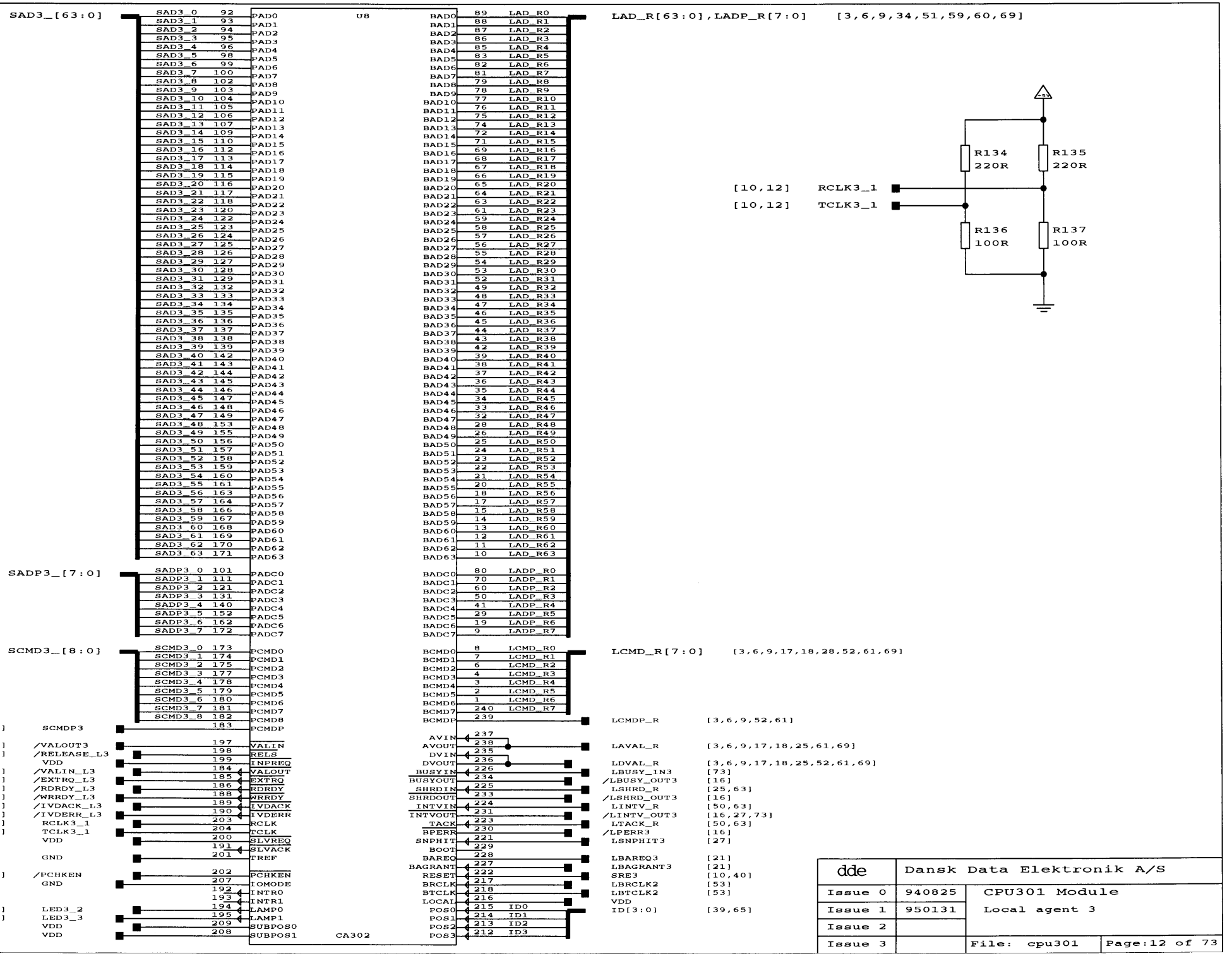
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local agent 2	
Issue 2			
Issue 3		File: cpu301	Page: 9 of 73

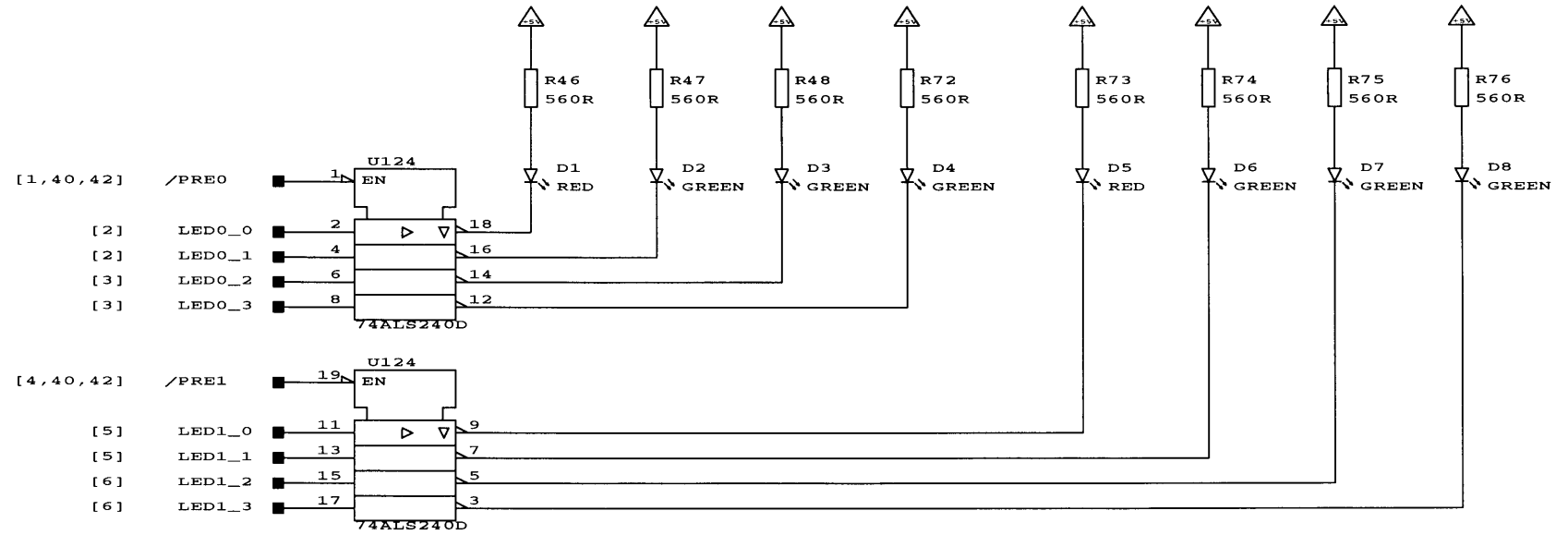


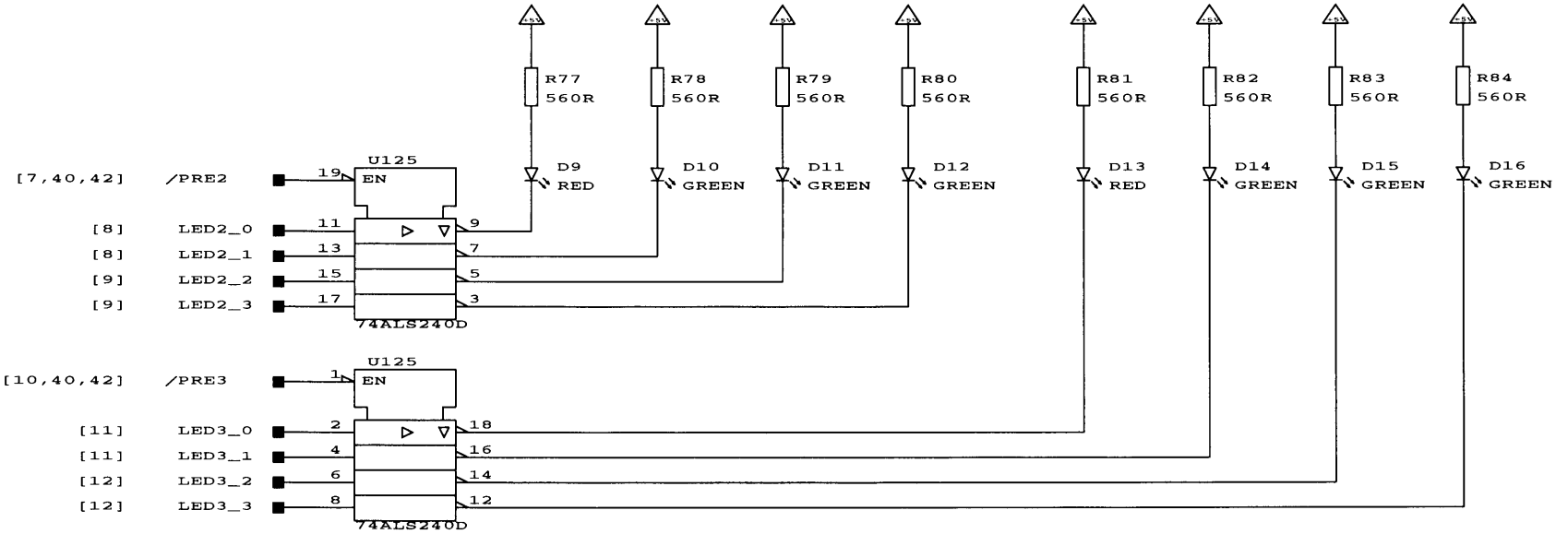
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connectors 3	
Issue 2			
Issue 3		File: cpu301	Page:10 of 73



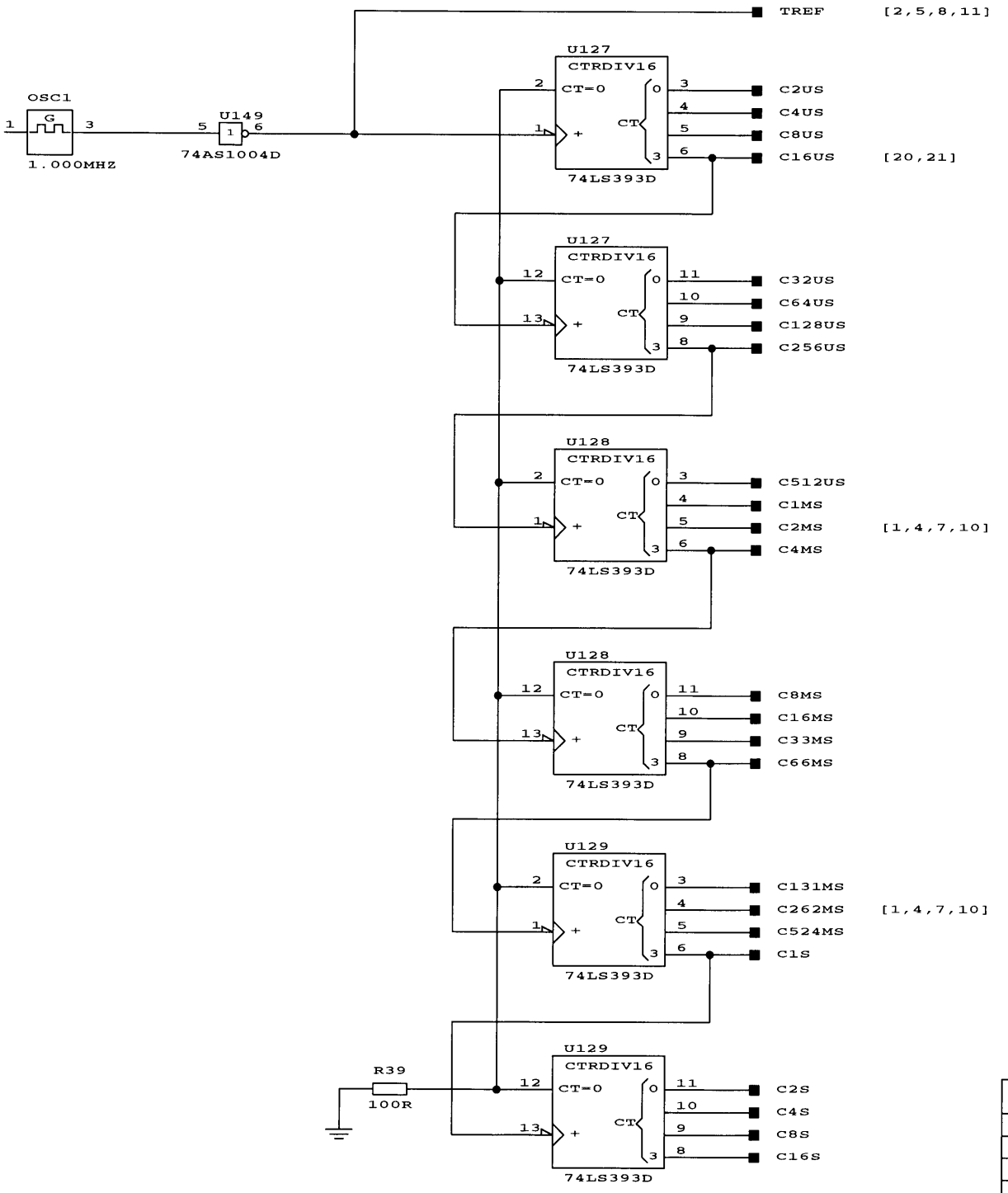
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global agent 3	
Issue 2			
Issue 3		File: cpu301	Page:11 of 73


SAD3_[63:0]
SADP3_[7:0]
SCMD3_[8:0]
U8
CA302
PAD0
PAD1
PAD2
PAD3
PAD4
PAD5
PAD6
PAD7
PAD8
PAD9
PAD10
PAD11
PAD12
PAD13
PAD14
PAD15
PAD16
PAD17
PAD18
PAD19
PAD20
PAD21
PAD22
PAD23
PAD24
PAD25
PAD26
PAD27
PAD28
PAD29
PAD30
PAD31
PAD32
PAD33
PAD34
PAD35
PAD36
PAD37
PAD38
PAD39
PAD40
PAD41
PAD42
PAD43
PAD44
PAD45
PAD46
PAD47
PAD48
PAD49
PAD50
PAD51
PAD52
PAD53
PAD54
PAD55
PAD56
PAD57
PAD58
PAD59
PAD60
PAD61
PAD62
PAD63
PADC0
PADC1
PADC2
PADC3
PADC4
PADC5
PADC6
PADC7
PCMD0
PCMD1
PCMD2
PCMD3
PCMD4
PCMD5
PCMD6
PCMD7
PCMD8
PCMDP
VALIN
RELS
INPREQ
VALOUT
EXTRQ
RDRDY
WRRDY
IVDACK
IVDERR
RCLK
TCLK
SLVREQ
SLVACK
TREF
PCHKEN
IOMODE
INTR0
INTR1
LAMP0
LAMP1
SUBPOS0
SUBPOS1
BAD0
BAD1
BAD2
BAD3
BAD4
BAD5
BAD6
BAD7
BAD8
BAD9
BAD10
BAD11
BAD12
BAD13
BAD14
BAD15
BAD16
BAD17
BAD18
BAD19
BAD20
BAD21
BAD22
BAD23
BAD24
BAD25
BAD26
BAD27
BAD28
BAD29
BAD30
BAD31
BAD32
BAD33
BAD34
BAD35
BAD36
BAD37
BAD38
BAD39
BAD40
BAD41
BAD42
BAD43
BAD44
BAD45
BAD46
BAD47
BAD48
BAD49
BAD50
BAD51
BAD52
BAD53
BAD54
BAD55
BAD56
BAD57
BAD58
BAD59
BAD60
BAD61
BAD62
BAD63
BADC0
BADC1
BADC2
BADC3
BADC4
BADC5
BADC6
BADC7
BCMD0
BCMD1
BCMD2
BCMD3
BCMD4
BCMD5
BCMD6
BCMD7
BCMDP
AVIN
AVOUT
DVIN
DVOUT
BUSYIN
BUSYOUT
SHRDIN
SHRDOUT
INTVIN
INTVOUT
TACK
BPERR
SNPHIT
BOOT
BAREQ
BAGRANT
RESET
BRCLK
BTCLK
LOCAL
POS0
POS1
POS2
POS3
LAD_R0
LAD_R1
LAD_R2
LAD_R3
LAD_R4
LAD_R5
LAD_R6
LAD_R7
LAD_R8
LAD_R9
LAD_R10
LAD_R11
LAD_R12
LAD_R13
LAD_R14
LAD_R15
LAD_R16
LAD_R17
LAD_R18
LAD_R19
LAD_R20
LAD_R21
LAD_R22
LAD_R23
LAD_R24
LAD_R25
LAD_R26
LAD_R27
LAD_R28
LAD_R29
LAD_R30
LAD_R31
LAD_R32
LAD_R33
LAD_R34
LAD_R35
LAD_R36
LAD_R37
LAD_R38
LAD_R39
LAD_R40
LAD_R41
LAD_R42
LAD_R43
LAD_R44
LAD_R45
LAD_R46
LAD_R47
LAD_R48
LAD_R49
LAD_R50
LAD_R51
LAD_R52
LAD_R53
LAD_R54
LAD_R55
LAD_R56
LAD_R57
LAD_R58
LAD_R59
LAD_R60
LAD_R61
LAD_R62
LAD_R63
LADP_R0
LADP_R1
LADP_R2
LADP_R3
LADP_R4
LADP_R5
LADP_R6
LADP_R7
LCMD_R0
LCMD_R1
LCMD_R2
LCMD_R3
LCMD_R4
LCMD_R5
LCMD_R6
LCMD_R7
ID0
ID1
ID2
ID3
LAD_R[63:0],LADP_R[7:0] [3,6,9,34,51,59,60,69]
LCMD_R[7:0] [3,6,9,17,18,28,52,61,69]
[10,12] RCLK3_1
[10,12] TCLK3_1
R134 220R
R135 220R
R136 100R
R137 100R
[10,11] SCMDP3
[10] /VALOUT3
[11] /RELEASE_L3
VDD
[15] /VALIN_L3
[11] /EXTRQ_L3
[15] /RDRDY_L3
[15] /WRRDY_L3
[15] /IVDACK_L3
[15] /IVDERR_L3
[10,12] RCLK3_1
[10,12] TCLK3_1
VDD
GND
[2] /PCHKEN
GND
[13] LED3_2
[13] LED3_3
VDD
VDD
LCMDP_R [3,6,9,52,61]
LAVAL_R [3,6,9,17,18,25,61,69]
LDVAL_R [3,6,9,17,18,25,52,61,69]
LBUSY_IN3 [73]
/LBUSY_OUT3 [16]
LSHRD_R [25,63]
/LSHRD_OUT3 [16]
LINTV_R [50,63]
/LINTV_OUT3 [16,27,73]
LTACK_R [50,63]
/LPERR3 [16]
LSNPHIT3 [27]
LBAREQ3 [21]
LBAGRANT3 [21]
SRE3 [10,40]
LBRCLK2 [53]
LBTCLK2 [53]
VDD
ID[3:0] [39,65]
dde
Dansk Data Elektronik A/S
Issue 0 940825
Issue 1 950131
Issue 2
Issue 3
CPU301 Module
Local agent 3
File: cpu301
Page:12 of 73

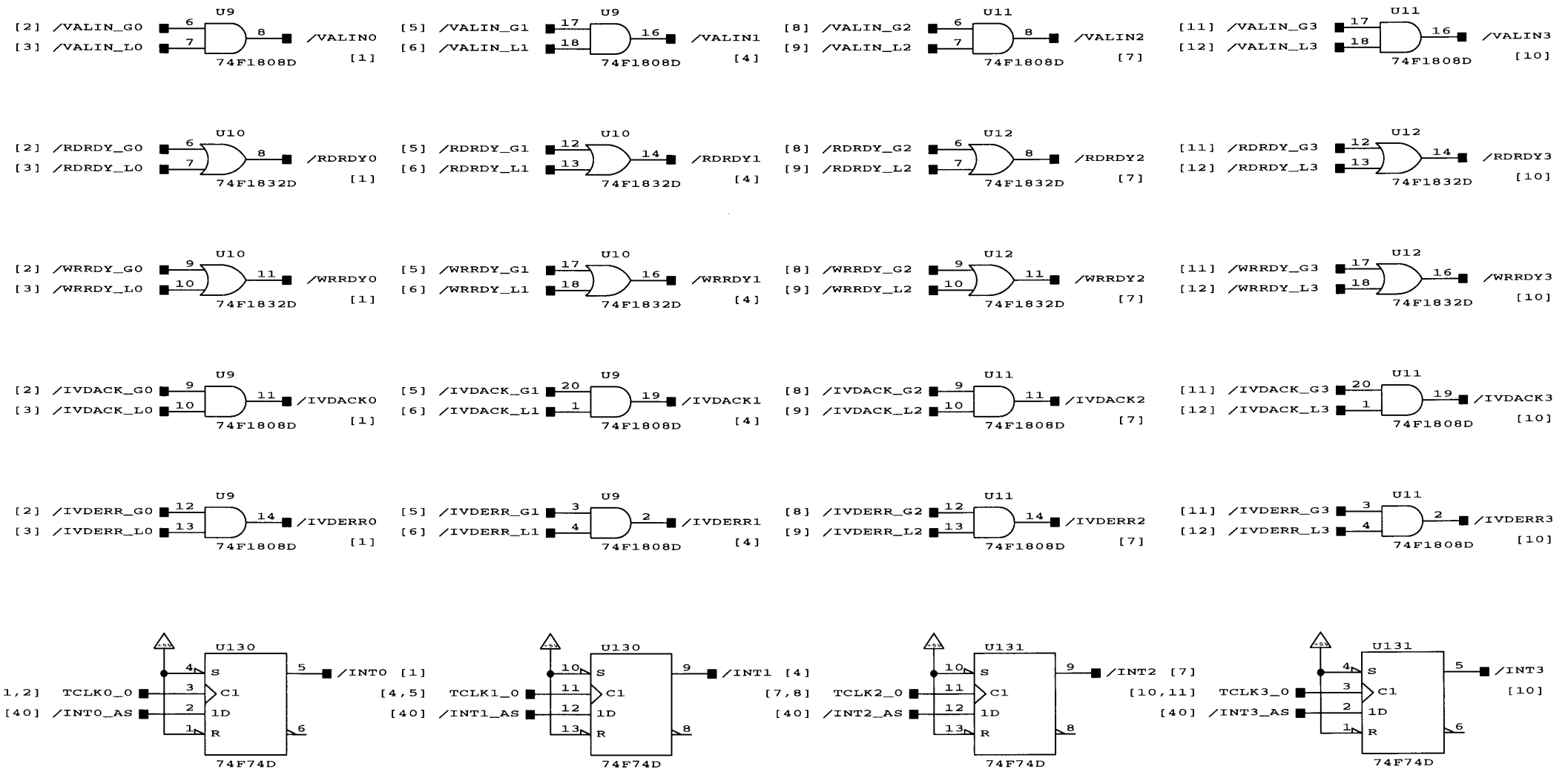




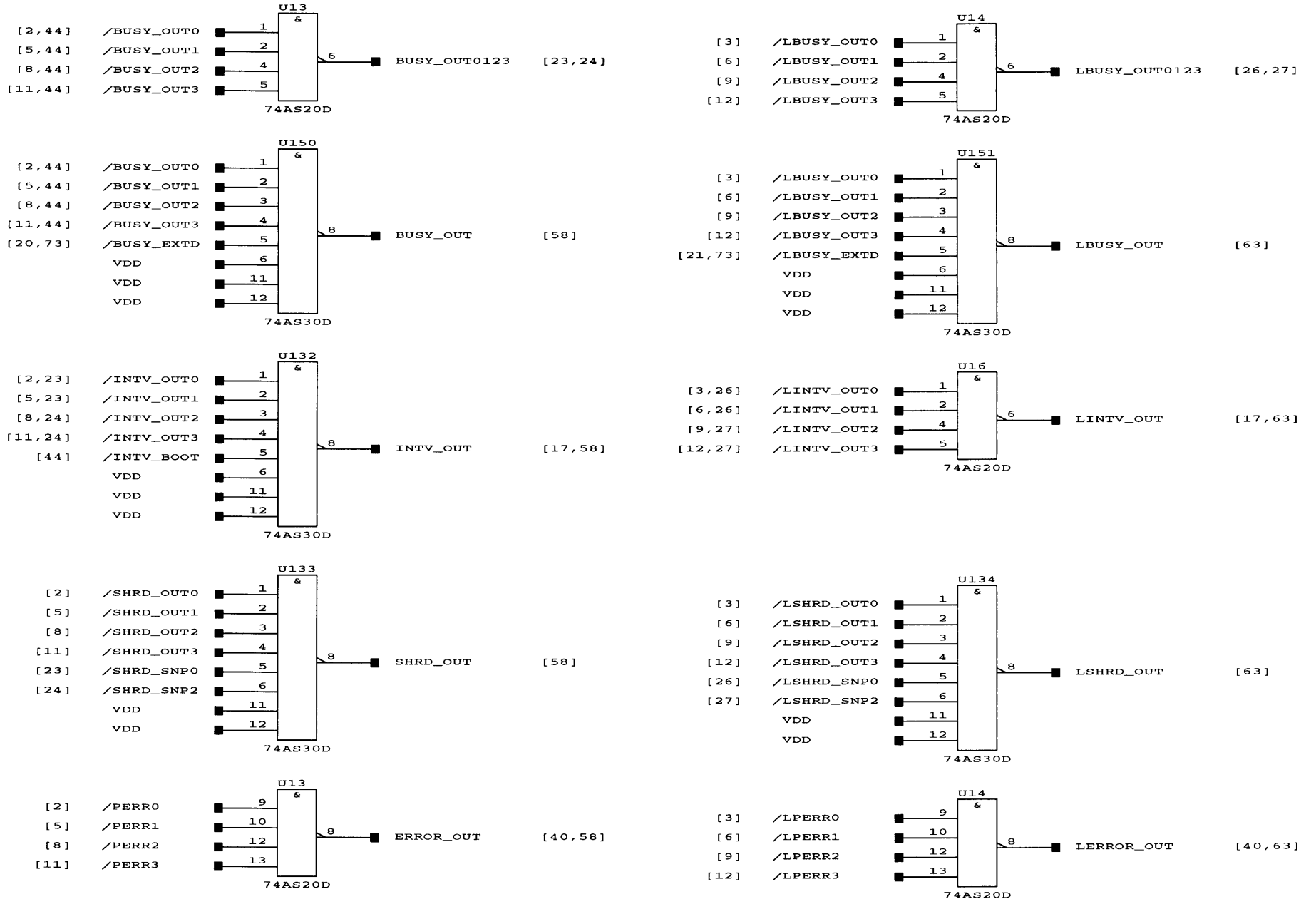
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Programmable LEDs	
Issue 2			
Issue 3		File: cpu301	Page:13 of 73



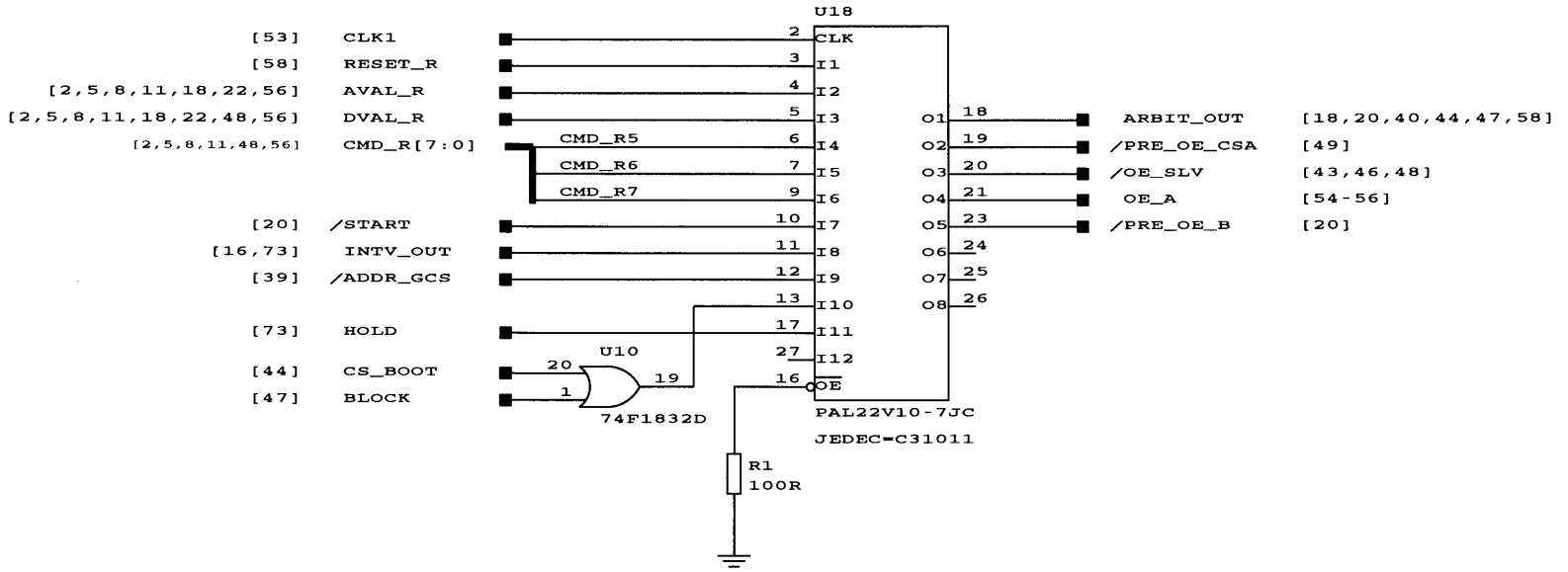
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Reset counters	
Issue 2			
Issue 3		File: cpu301	Page:14 of 73

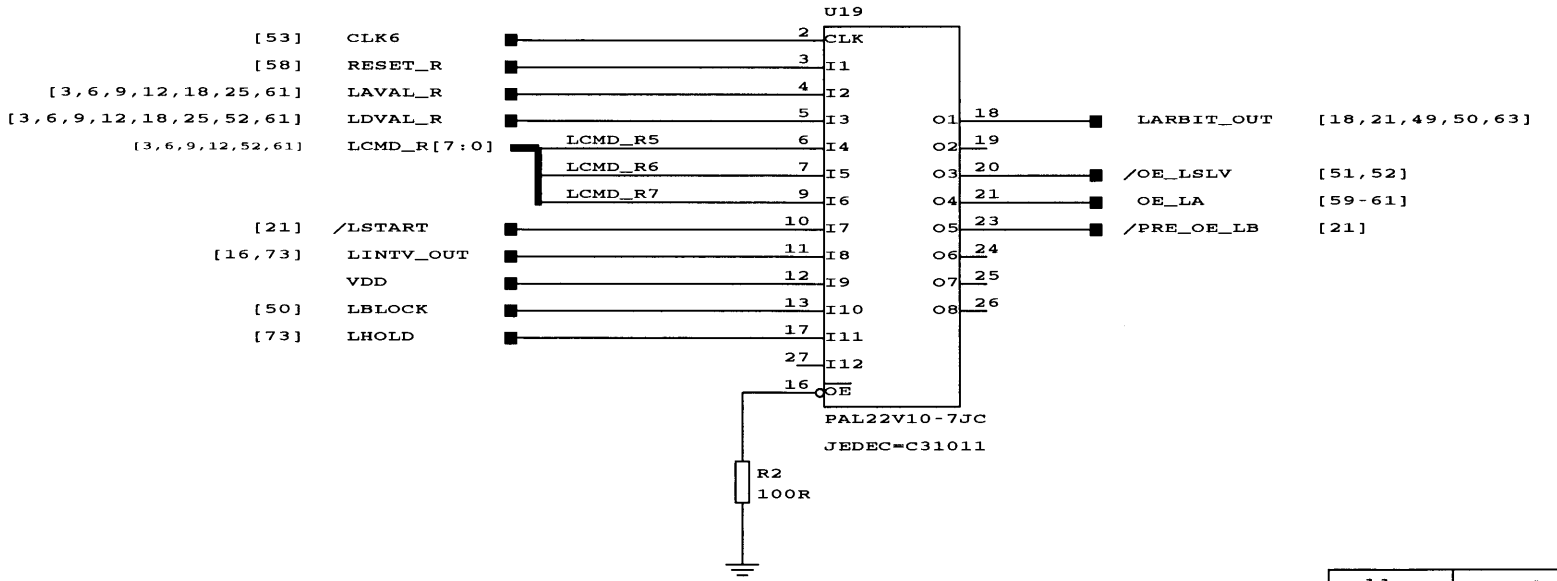


dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Gating towards processors	
Issue 2			
Issue 3		File: cpu301	Page:15 of 73

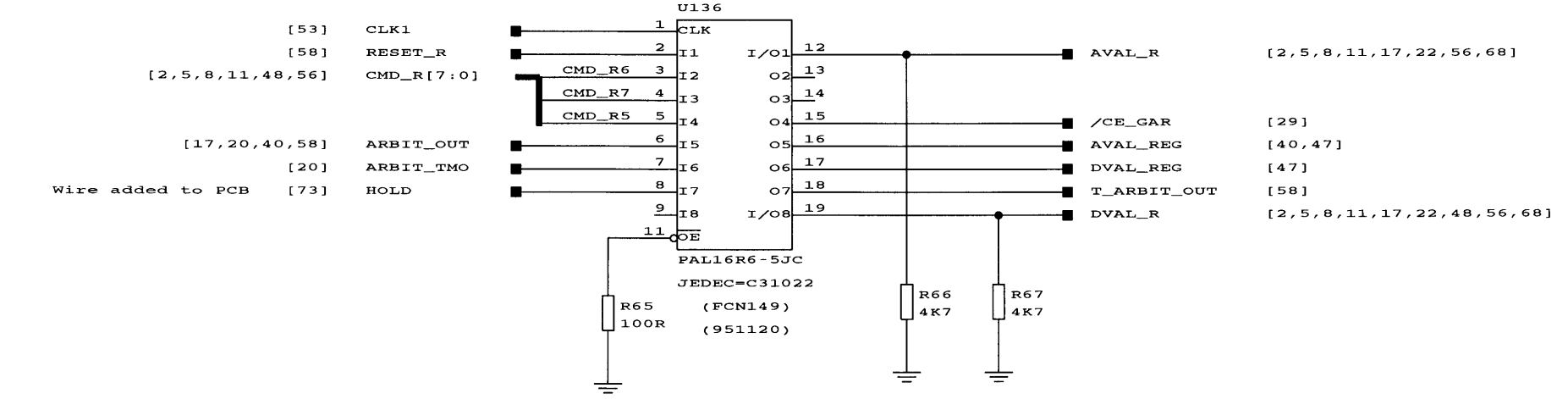


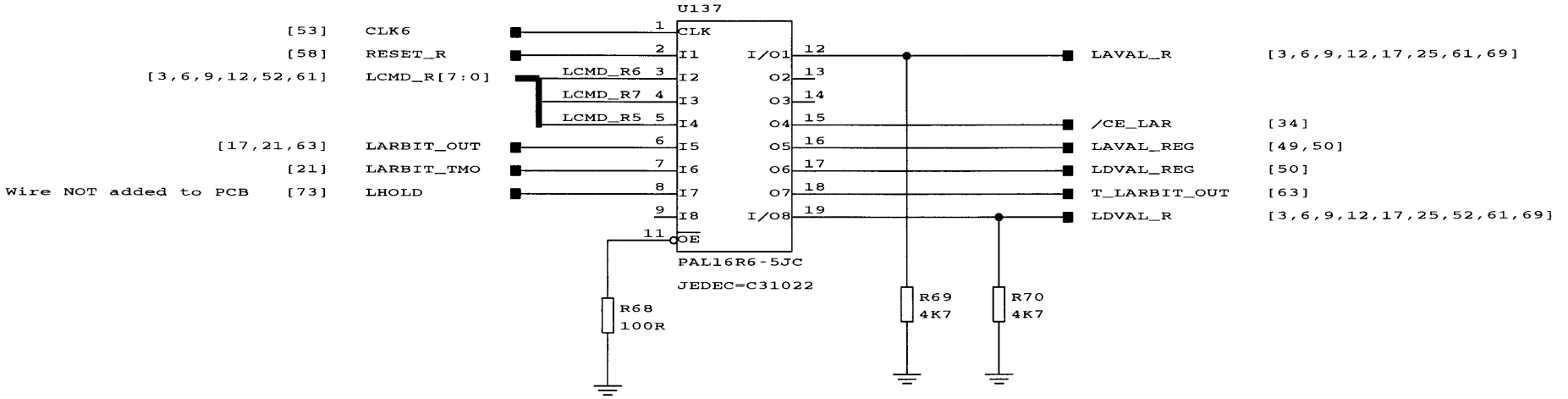
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Gating towards system bus	
Issue 2			
Issue 3		File: cpu301	Page:16 of 73



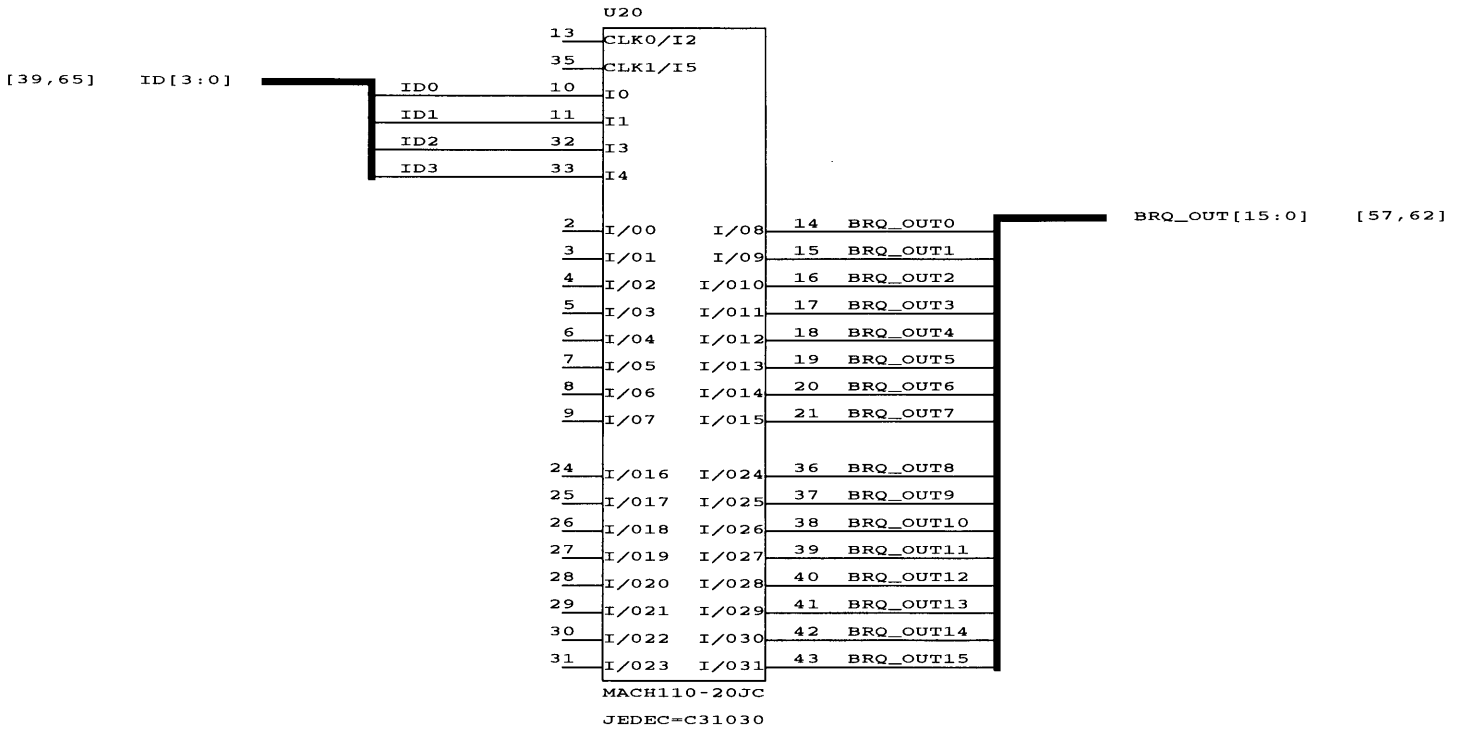


dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global and local	
Issue 2		output enable control	
Issue 3		File: cpu301	Page:17 of 73

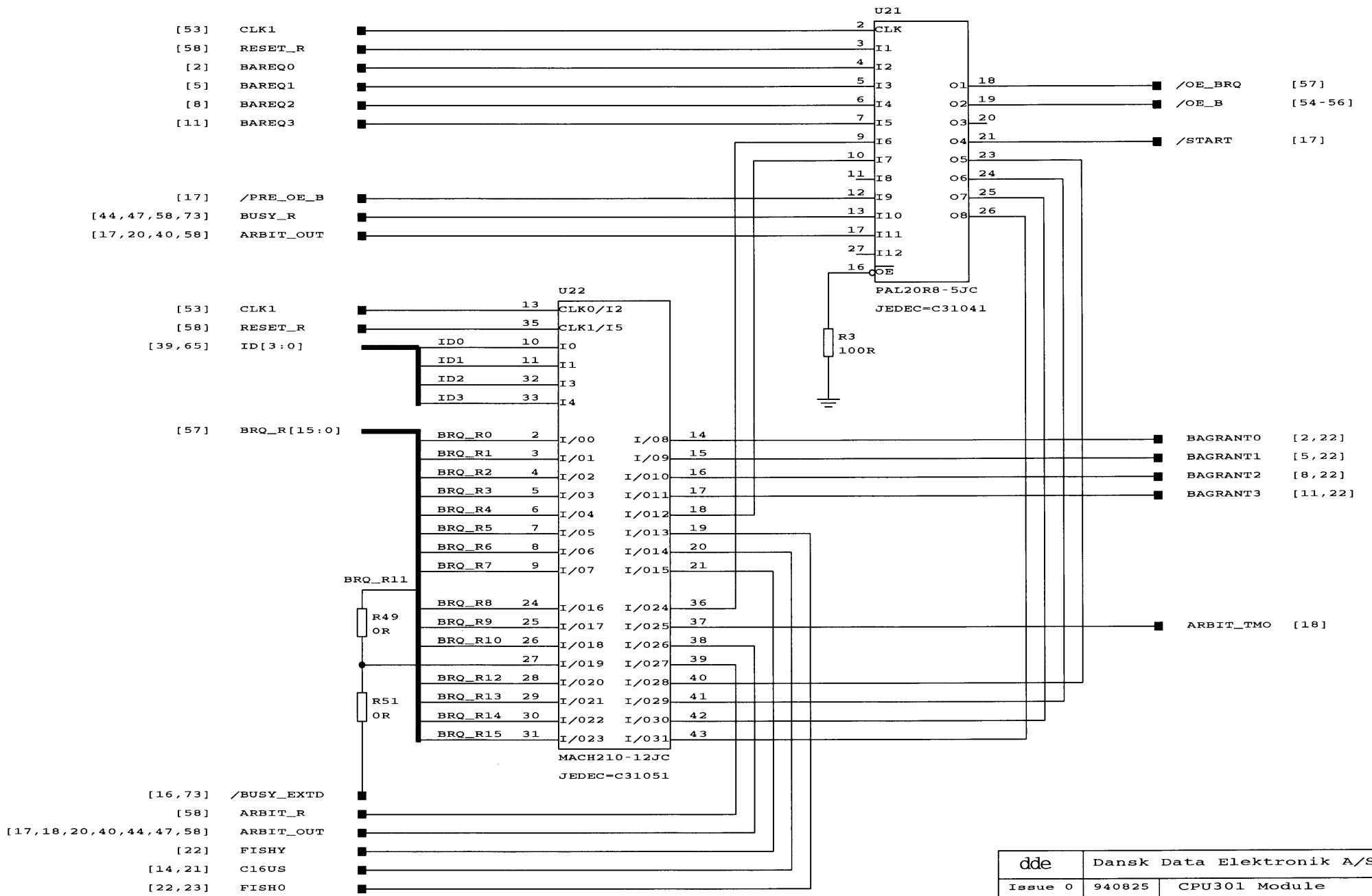




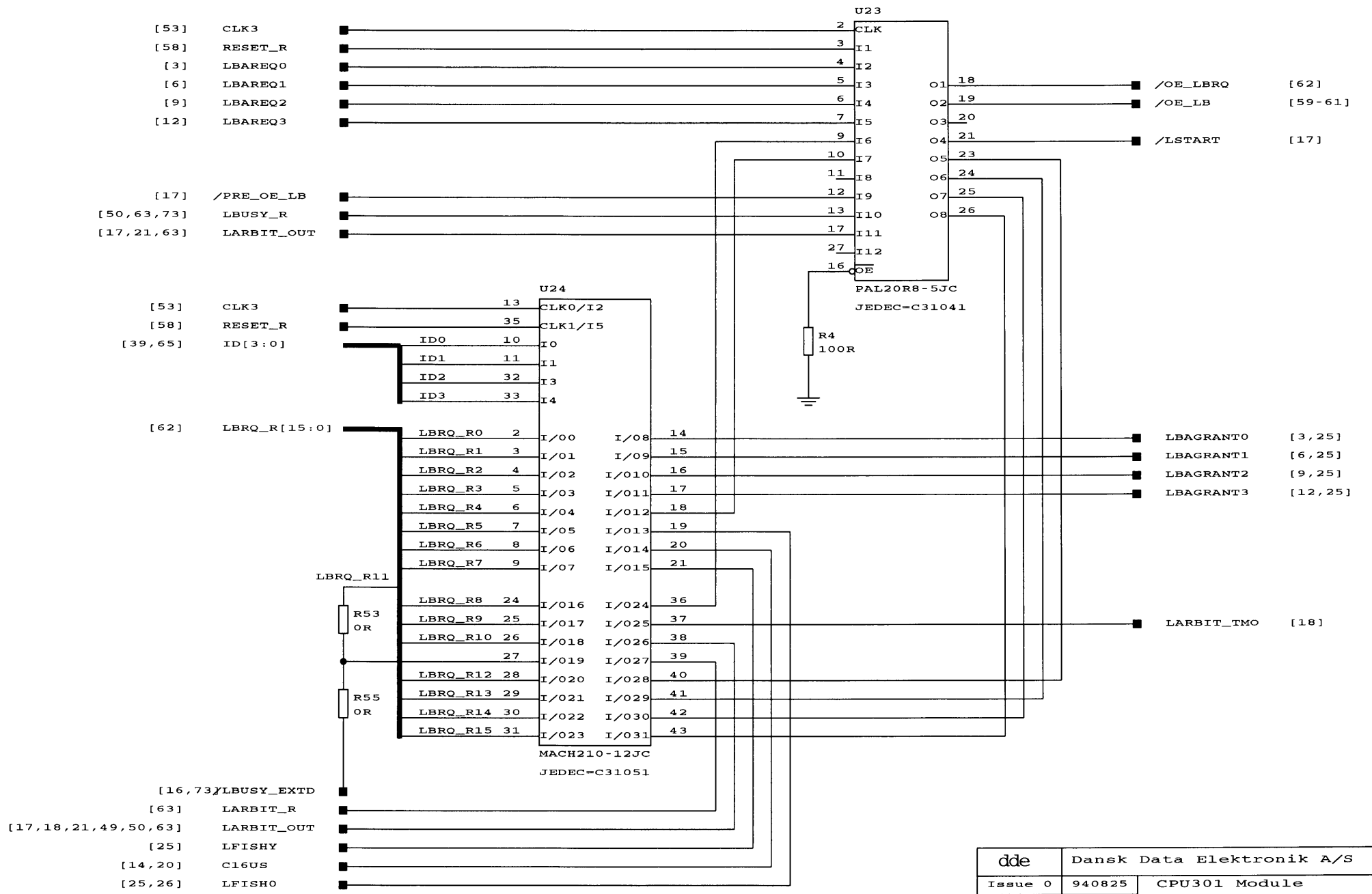
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Pull-down for	
Issue 2		address and data valid	
Issue 3		File: cpu301	Page:18 of 73



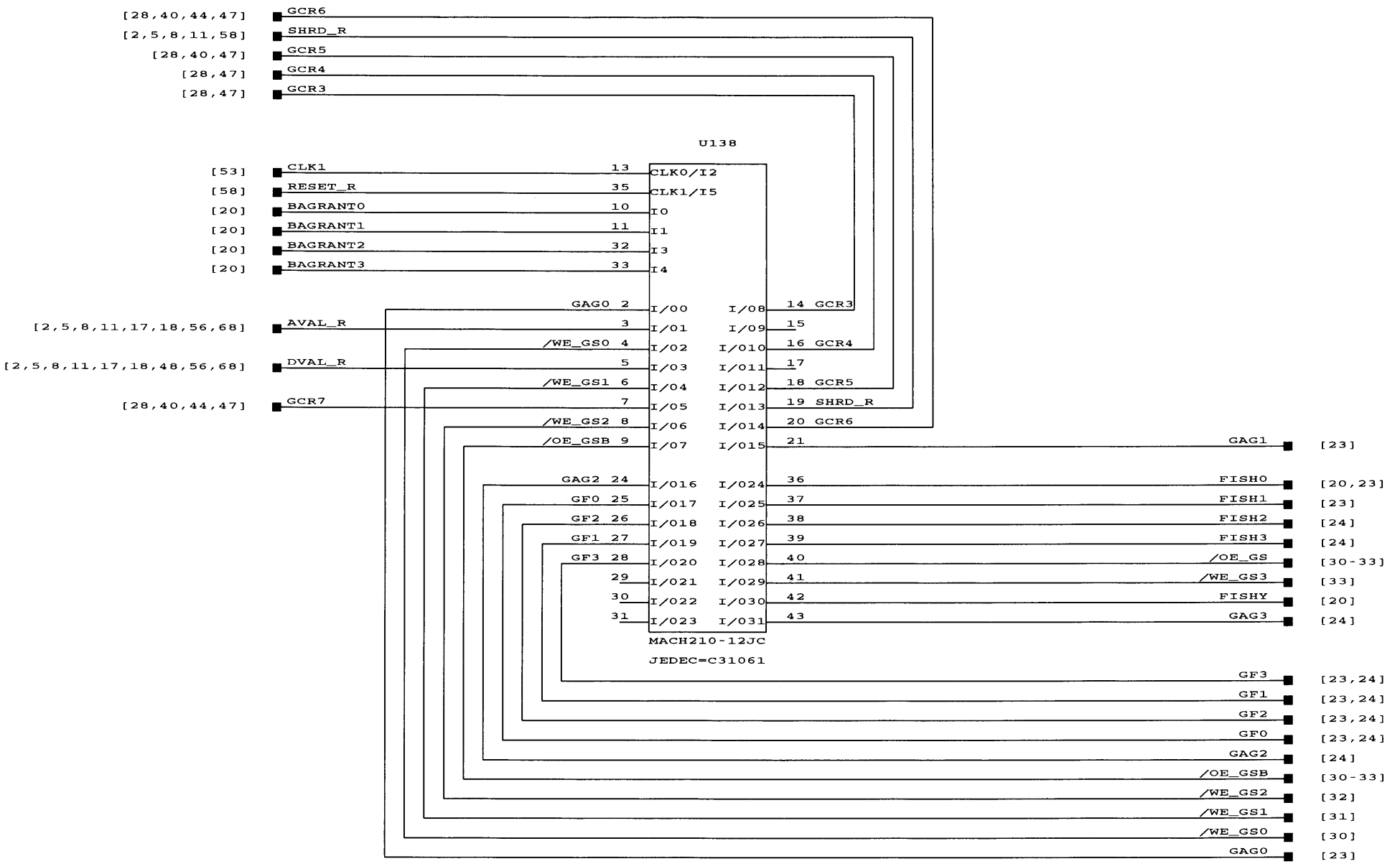
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global and local	
Issue 2		bus request decoder	
Issue 3		File: cpu301	Page:19 of 73



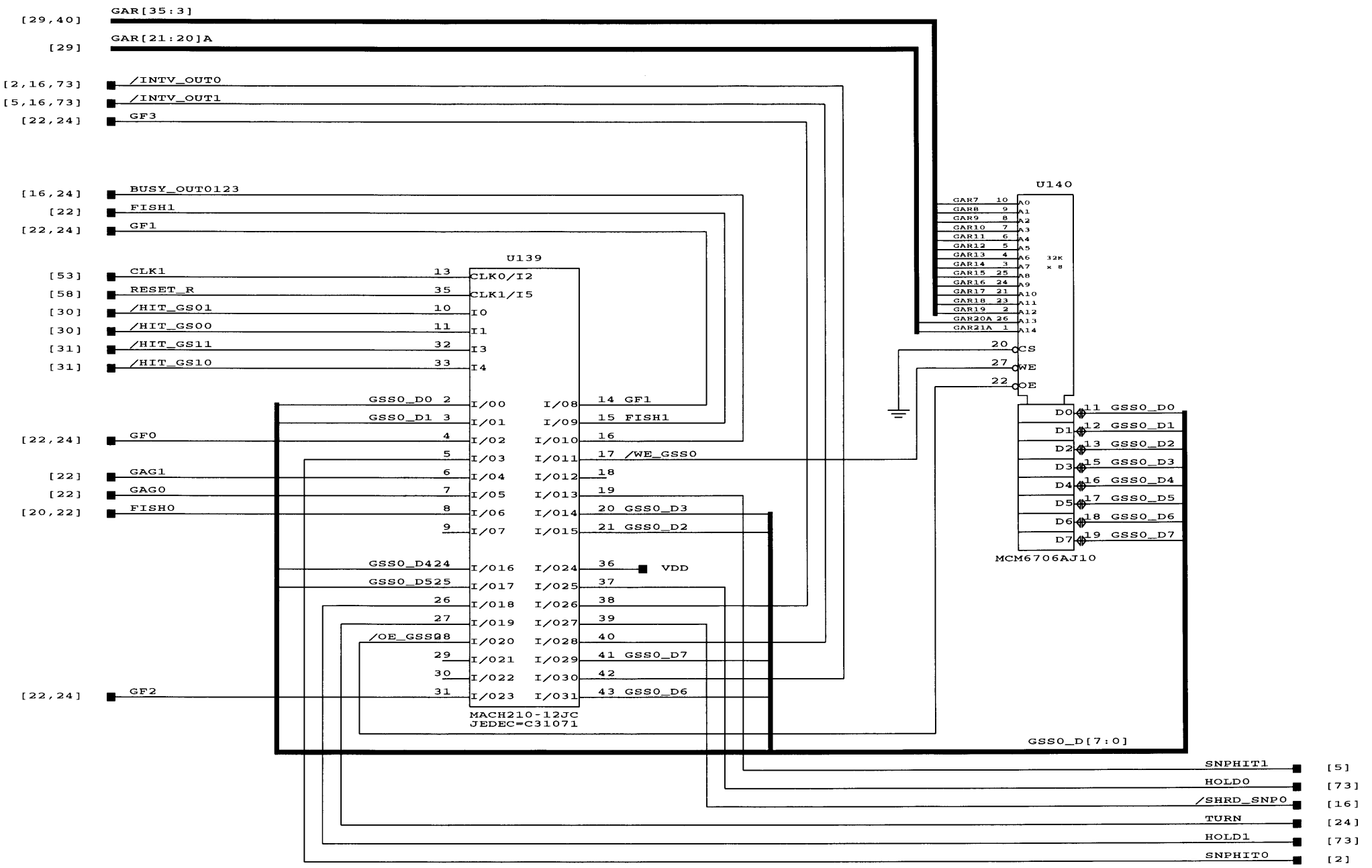
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global bus arbitration	
Issue 2			
Issue 3		File: cpu301	Page:20 of 73



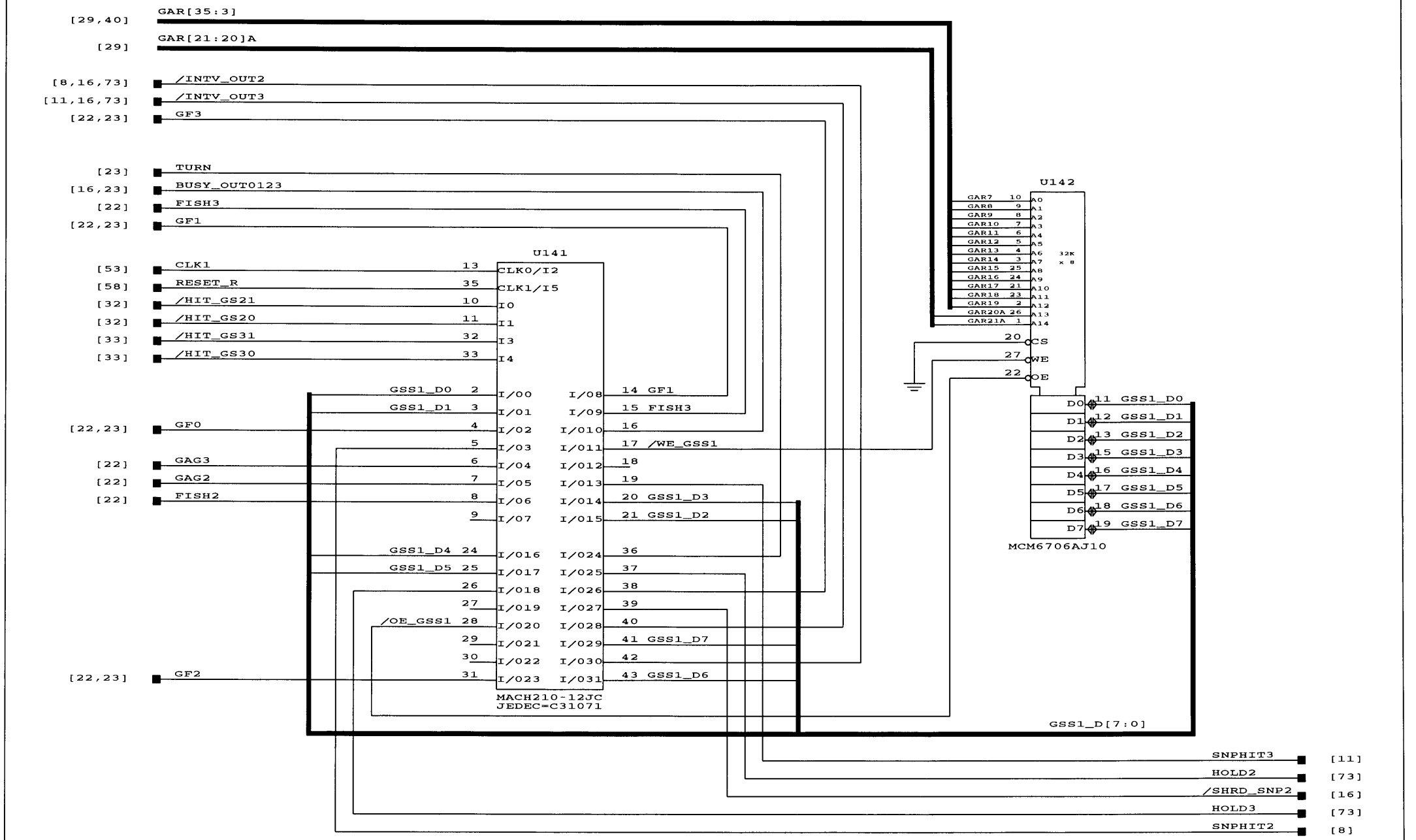
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local bus arbitration	
Issue 2			
Issue 3		File: cpu301	Page:21 of 73



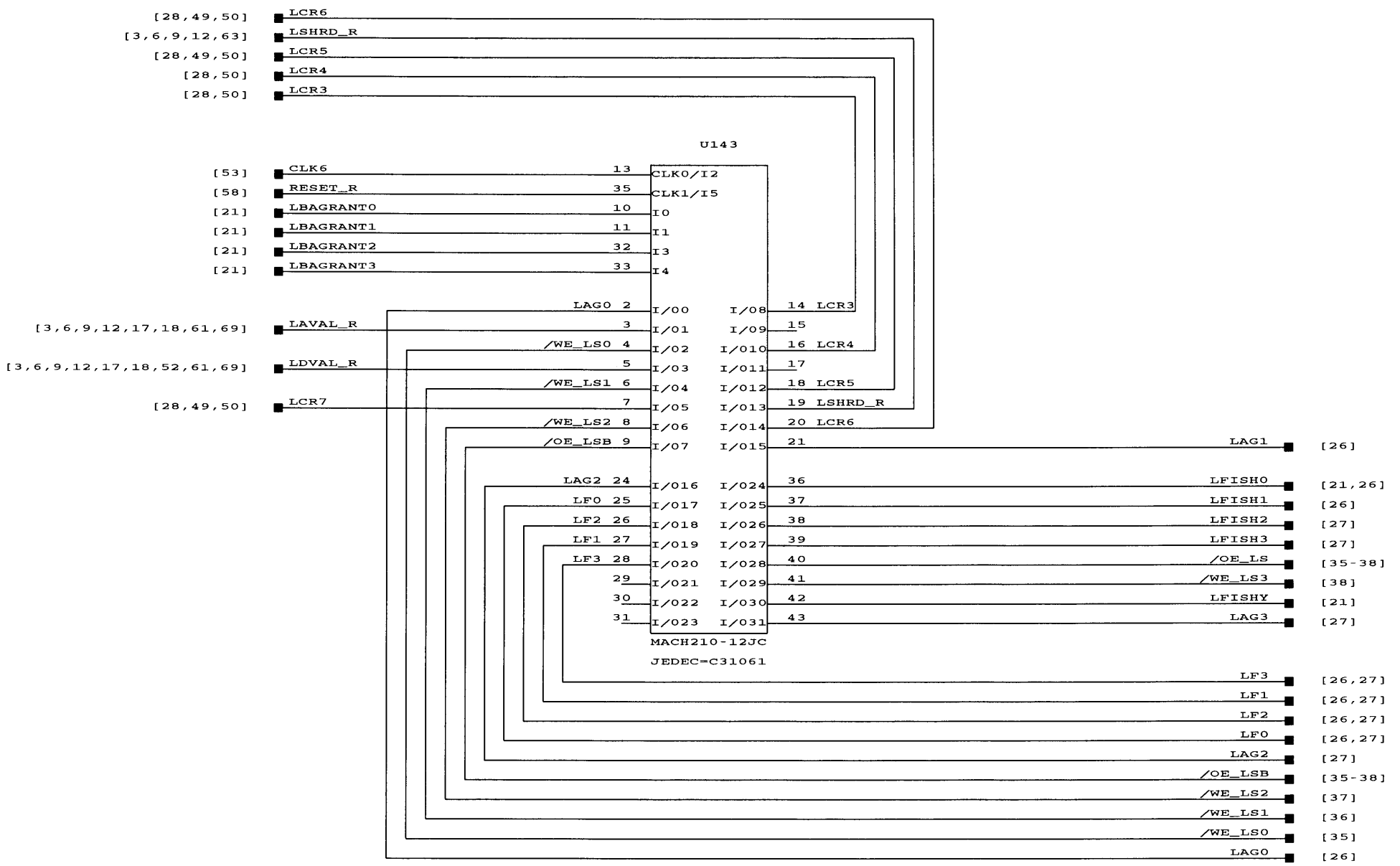
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global snooper control	
Issue 2			
Issue 3		File: cpu301	Page:22 of 73



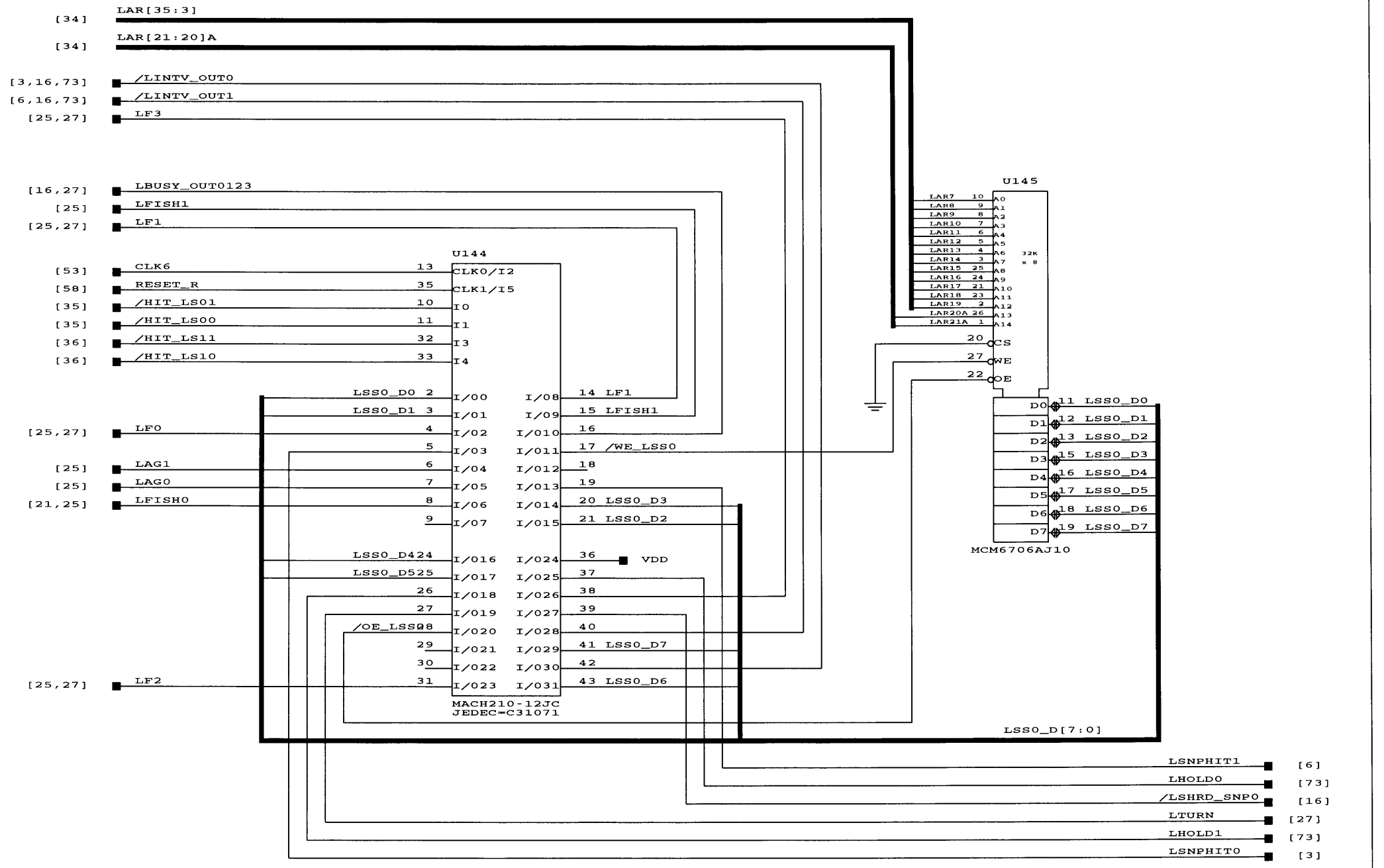
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global Super Snooper 0-1	
Issue 2			
Issue 3		File: cpu301	Page:23 of 73



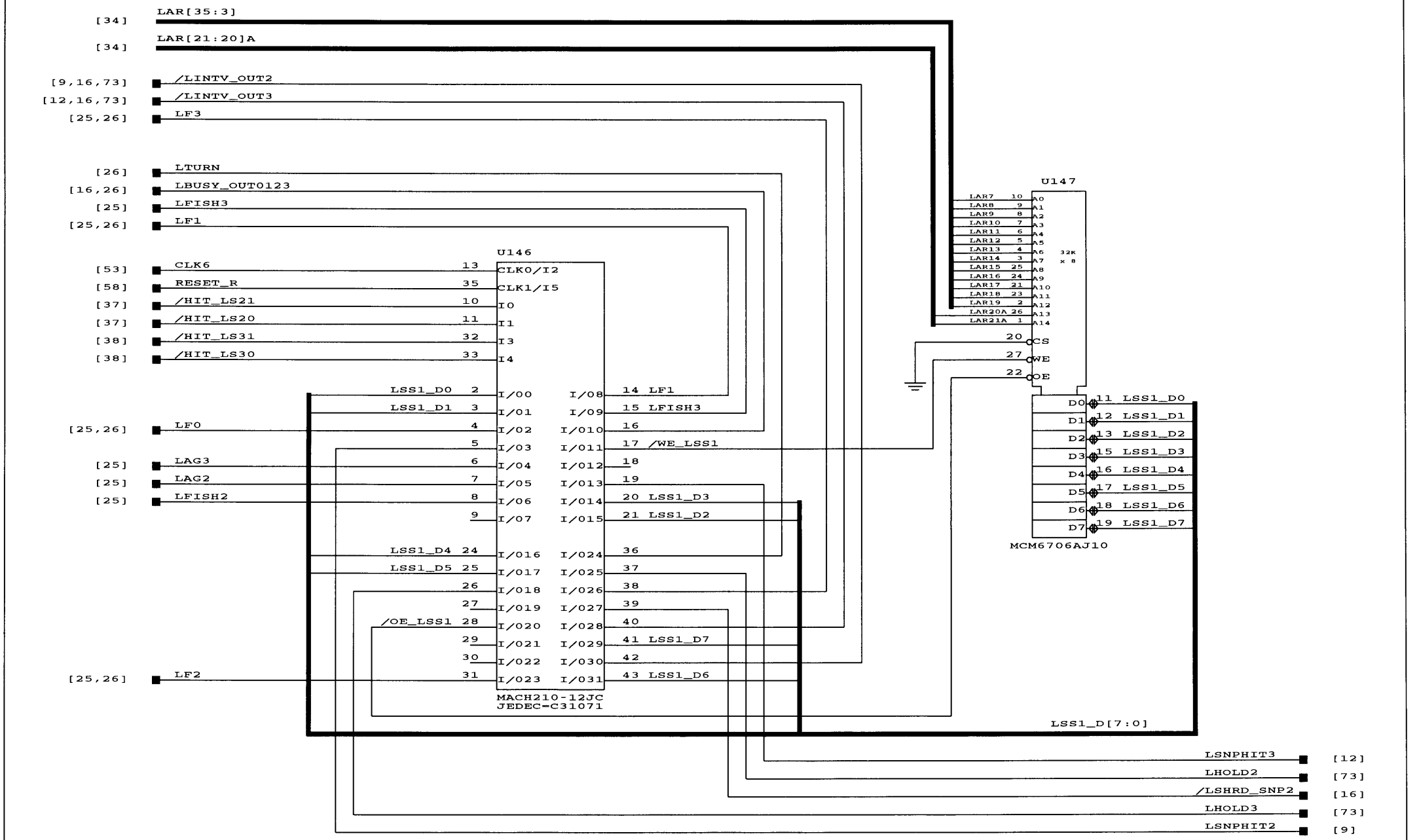
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global Super Snooper 2-3	
Issue 2			
Issue 3		File: cpu301	Page:24 of 73



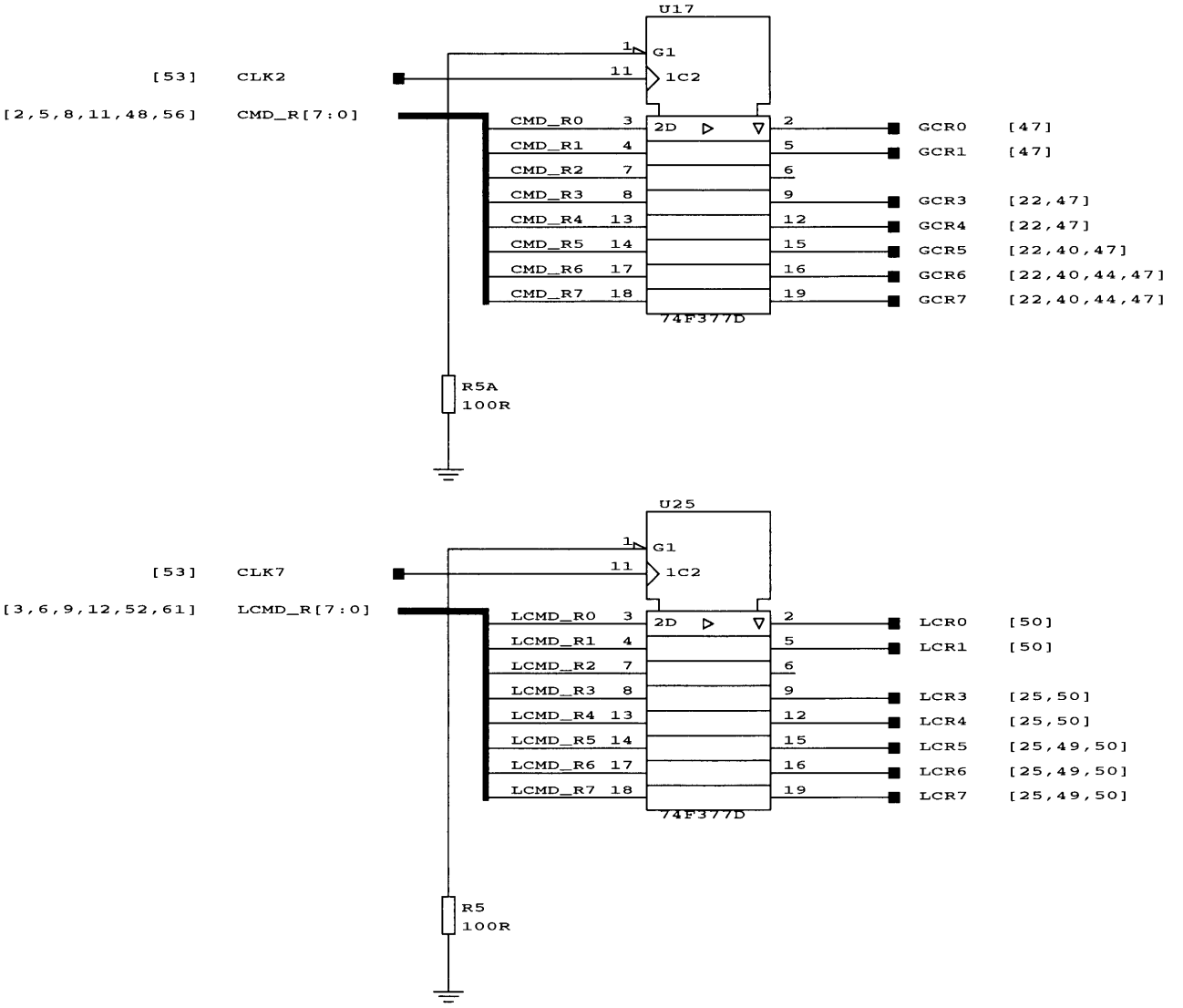
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local snooper control	
Issue 2			
Issue 3		File: cpu301	Page:25 of 73



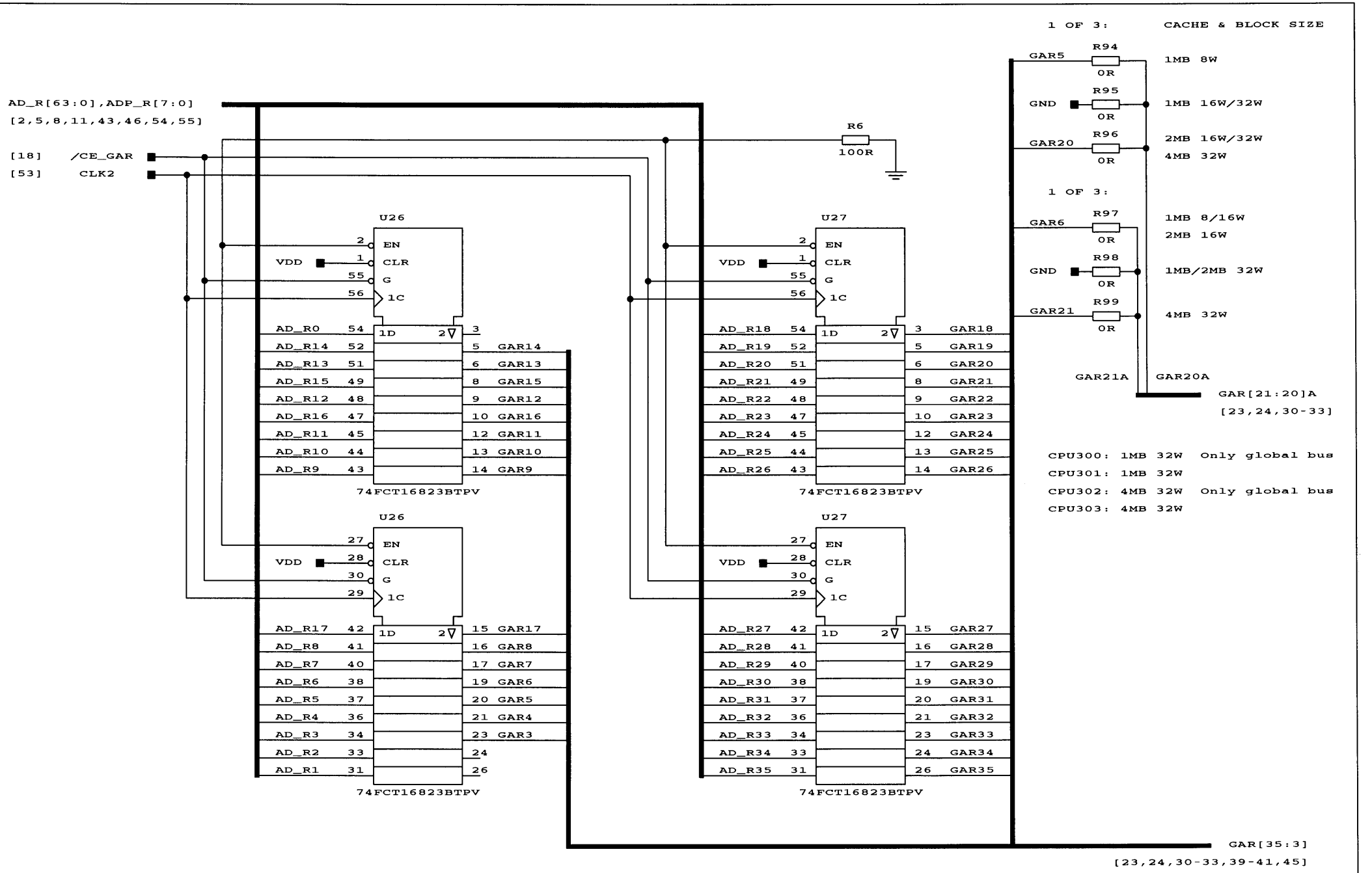
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local Super Snooper 0-1	
Issue 2			
Issue 3		File: cpu301	Page:26 of 73



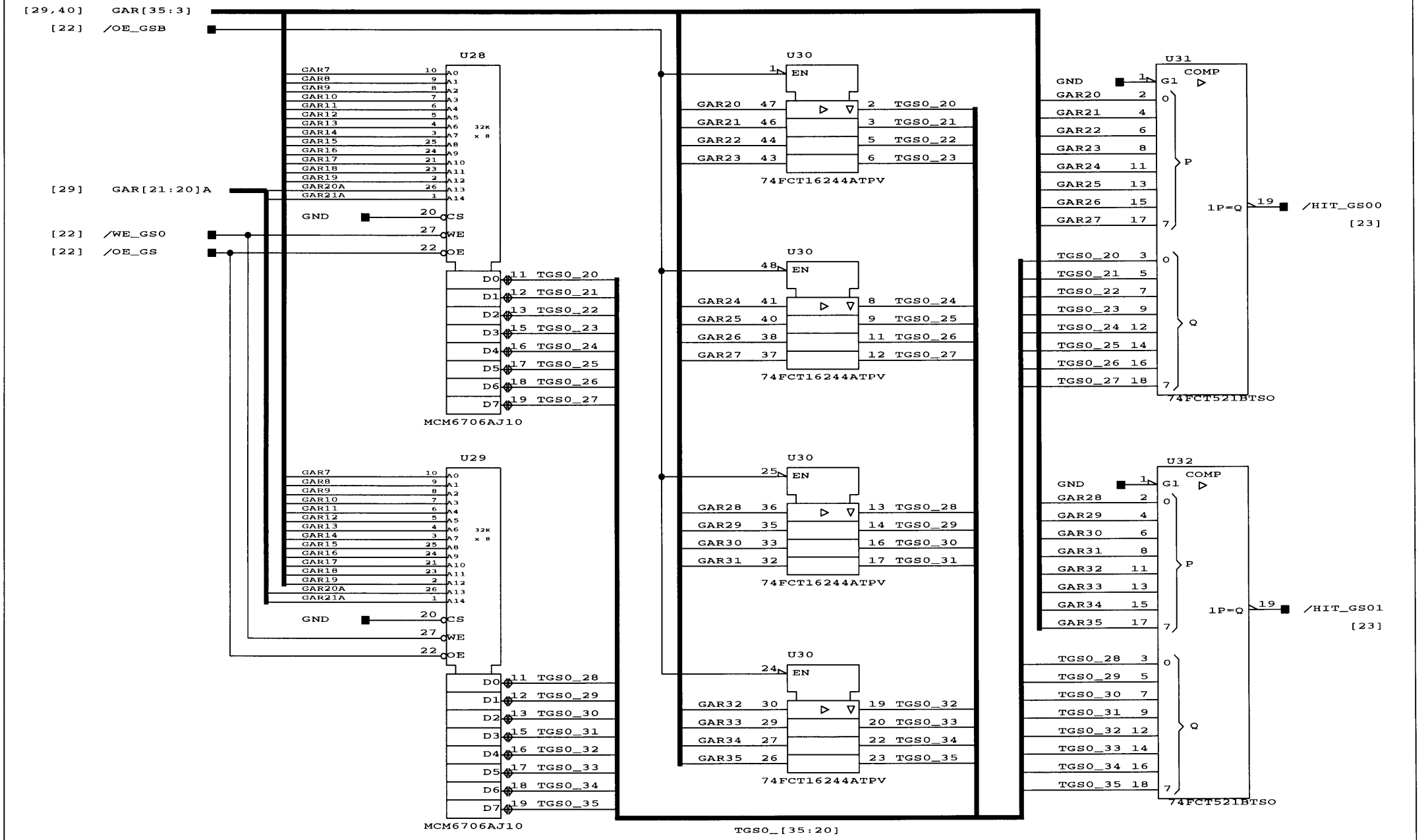
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local Super Snooper 2-3	
Issue 2			
Issue 3		File: cpu301	Page:27 of 73



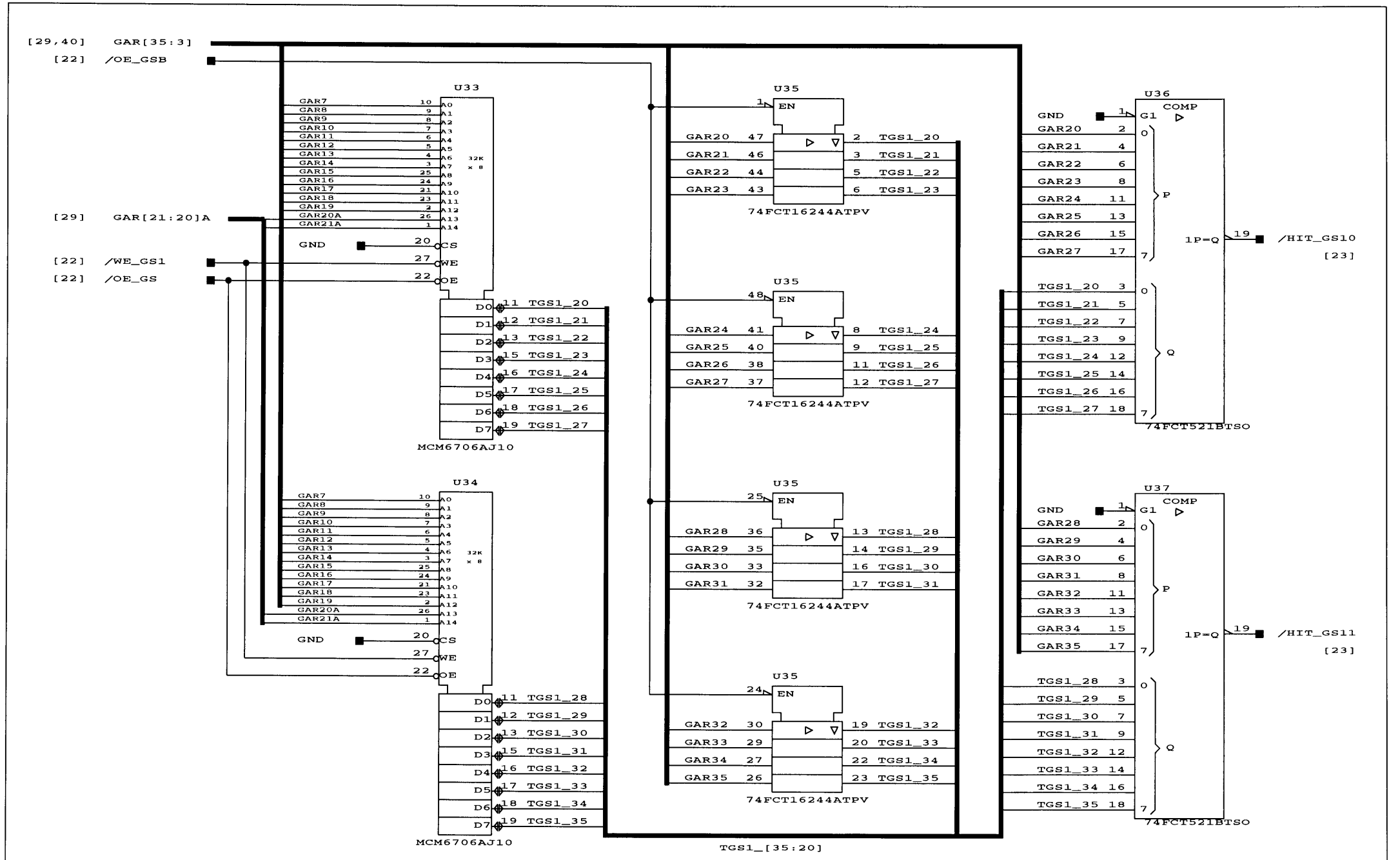
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global and local	
Issue 2		command register	
Issue 3		File: cpu301	Page:28 of 73



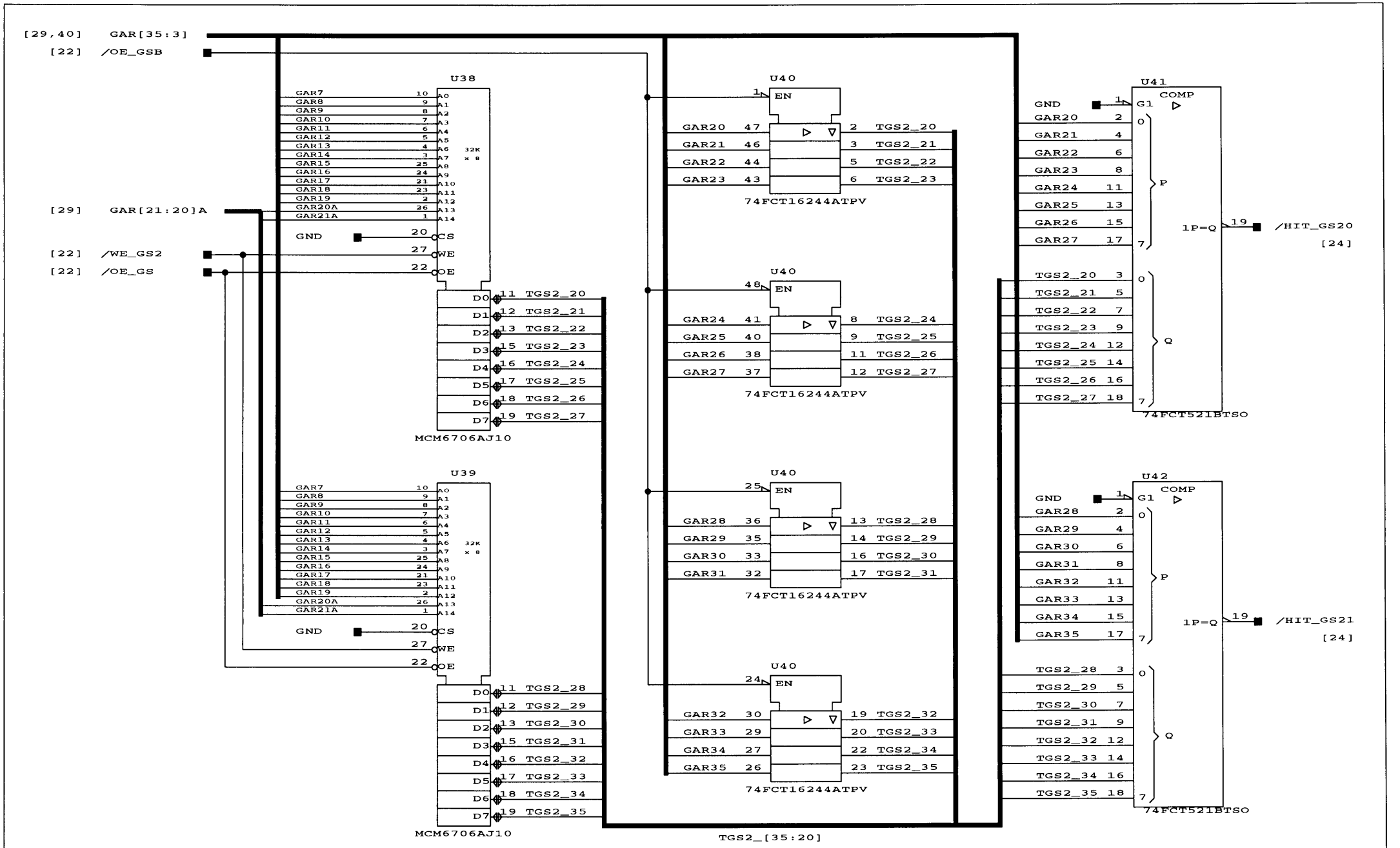
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global address register	
Issue 2			
Issue 3		File: cpu301	Page:29 of 73



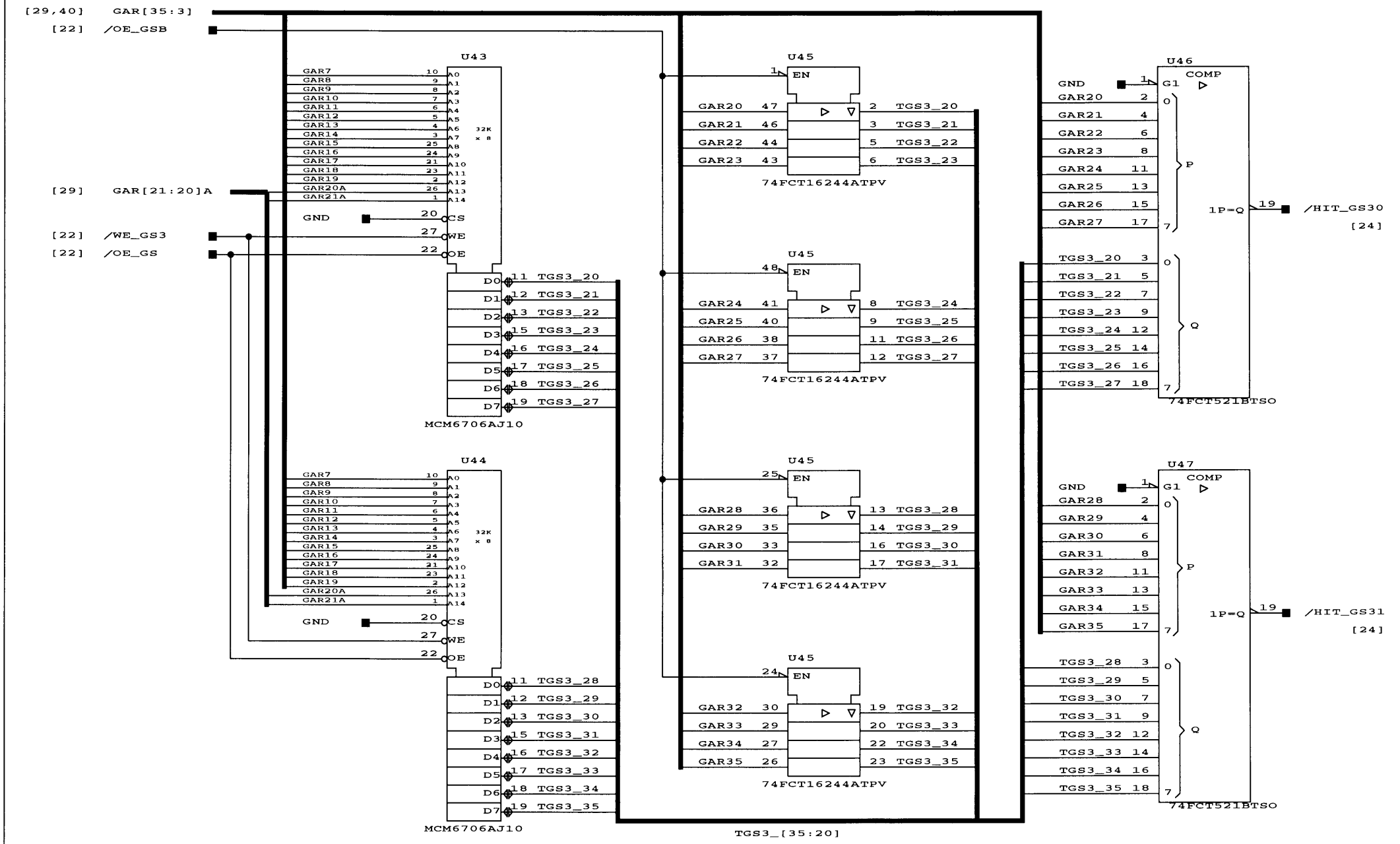
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global snooper 0	
Issue 2			
Issue 3		File: cpu301	Page:30 of 73



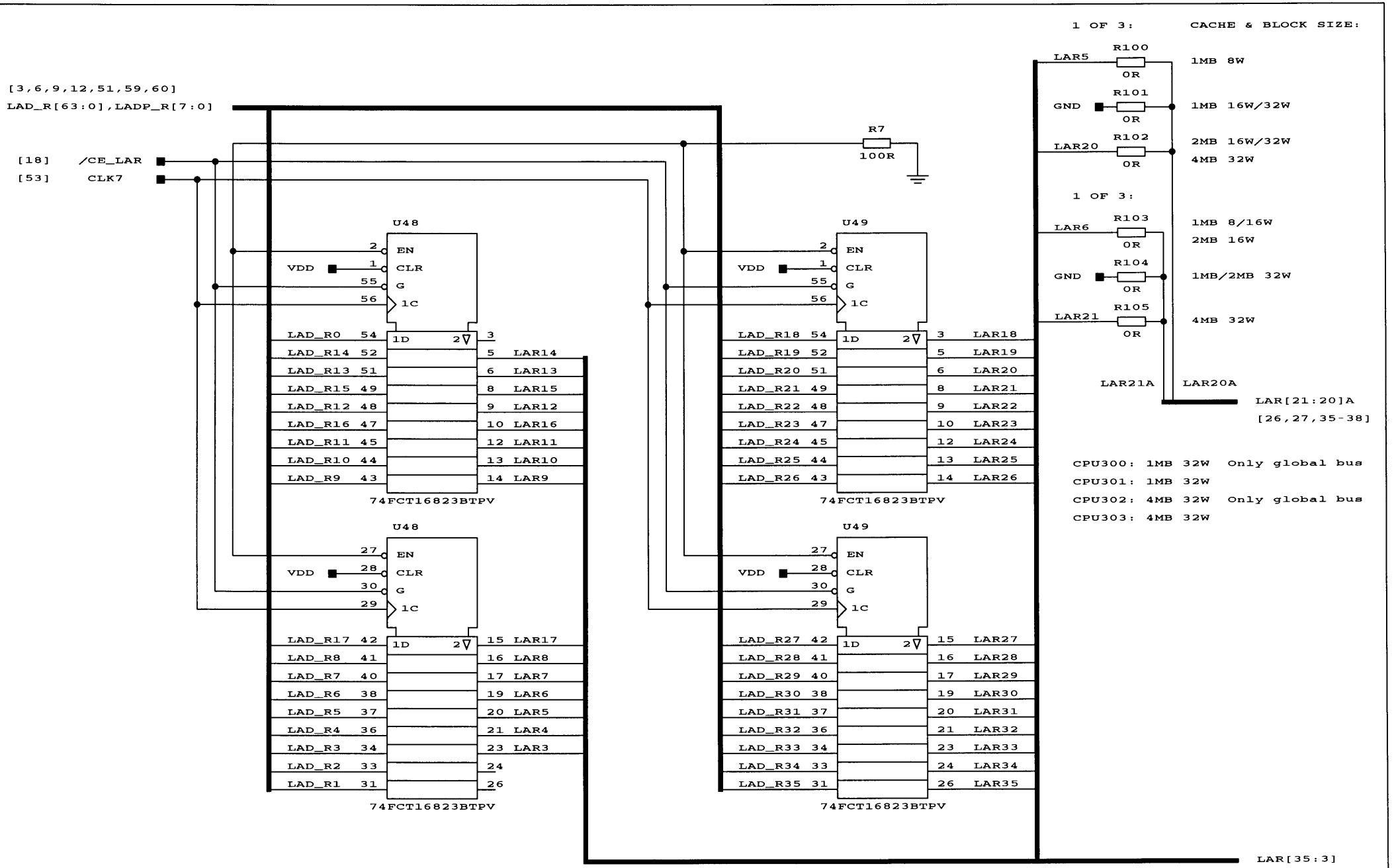
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global snooper 1	
Issue 2			
Issue 3		File: cpu301	Page:31 of 73



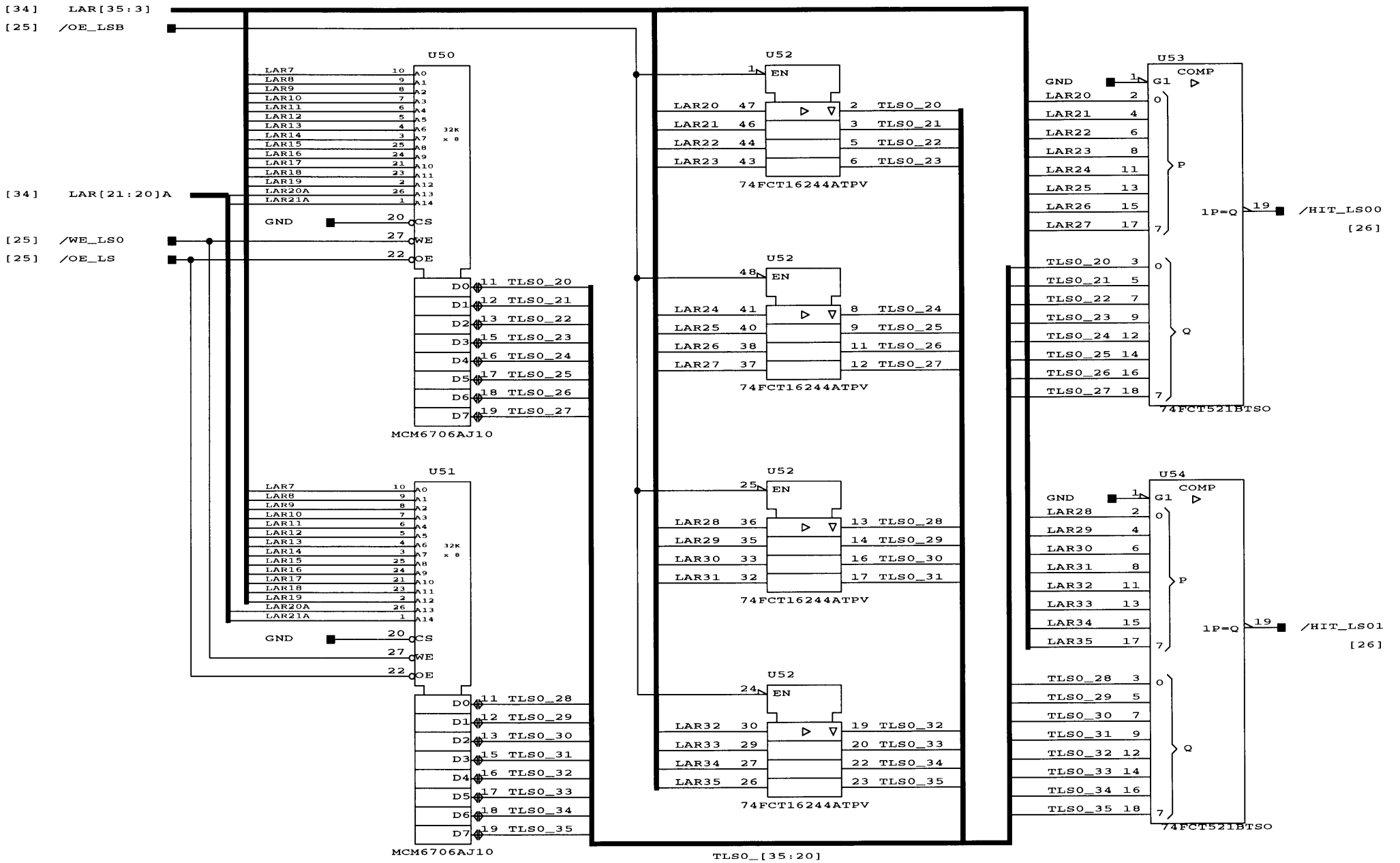
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global snooper 2	
Issue 2			
Issue 3		File: cpu301	Page:32 of 73



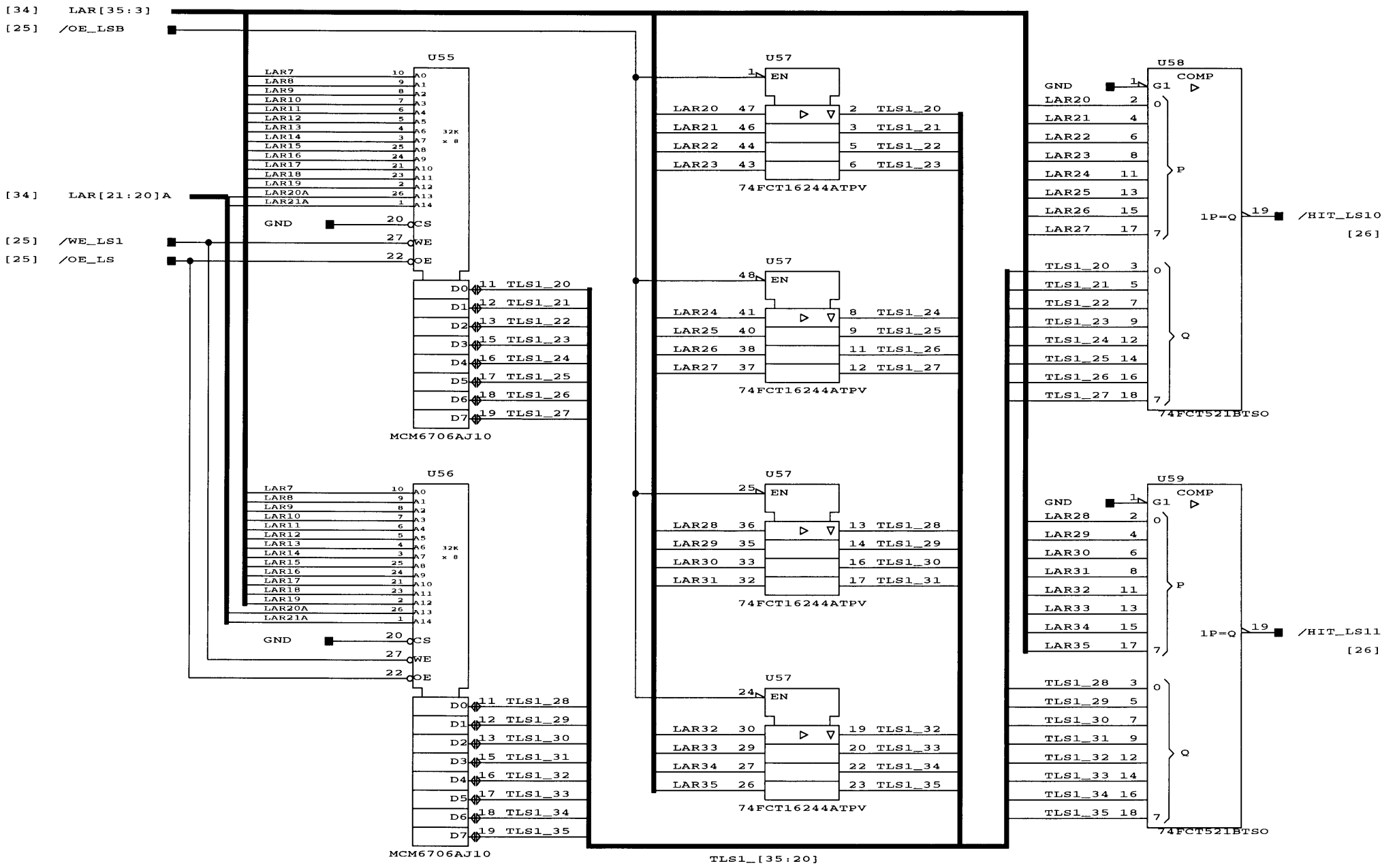
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global snooper 3	
Issue 2			
Issue 3		File: cpu301	Page:33 of 73



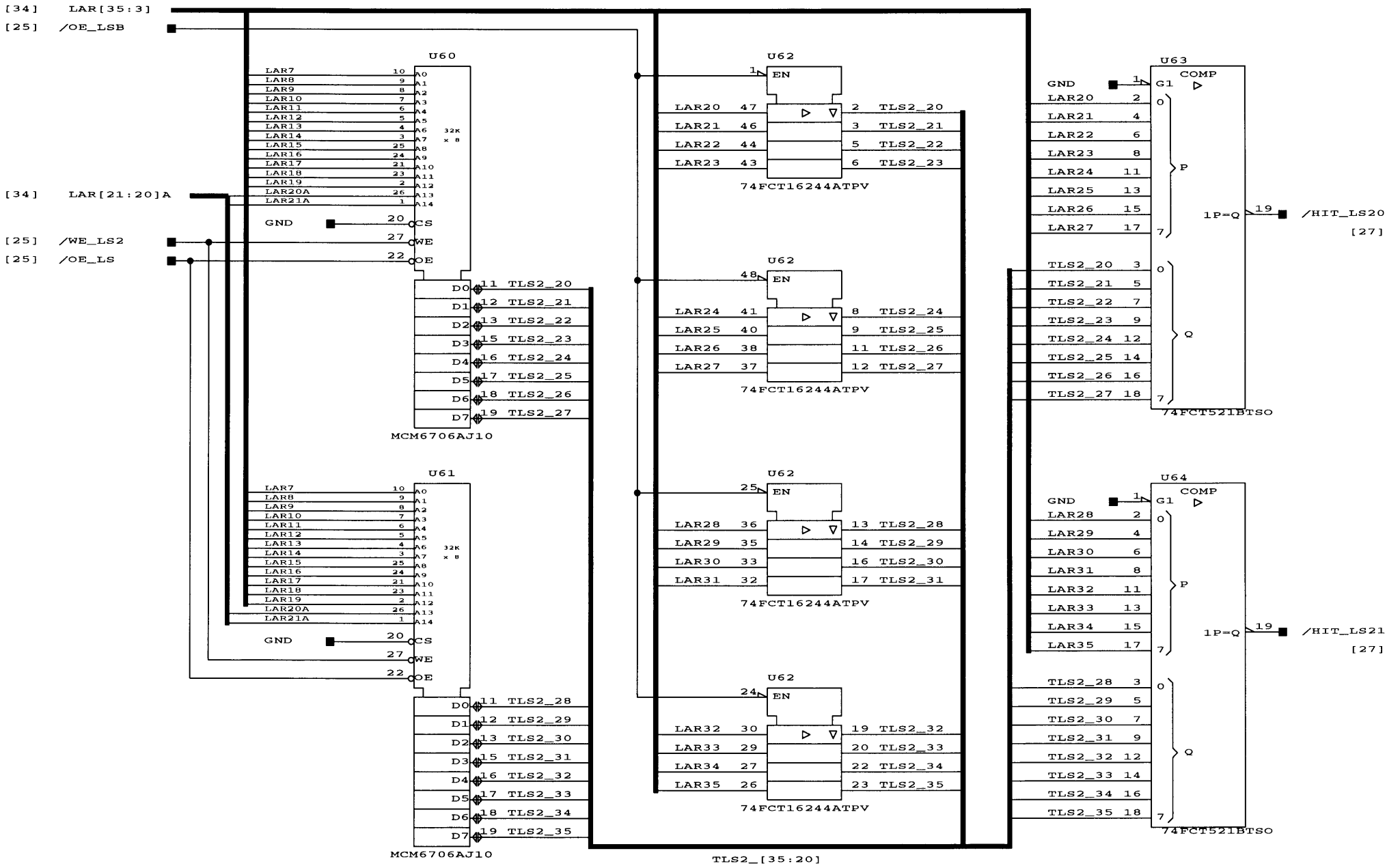
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local address register	
Issue 2			
Issue 3		File: cpu301	Page:34 of 73



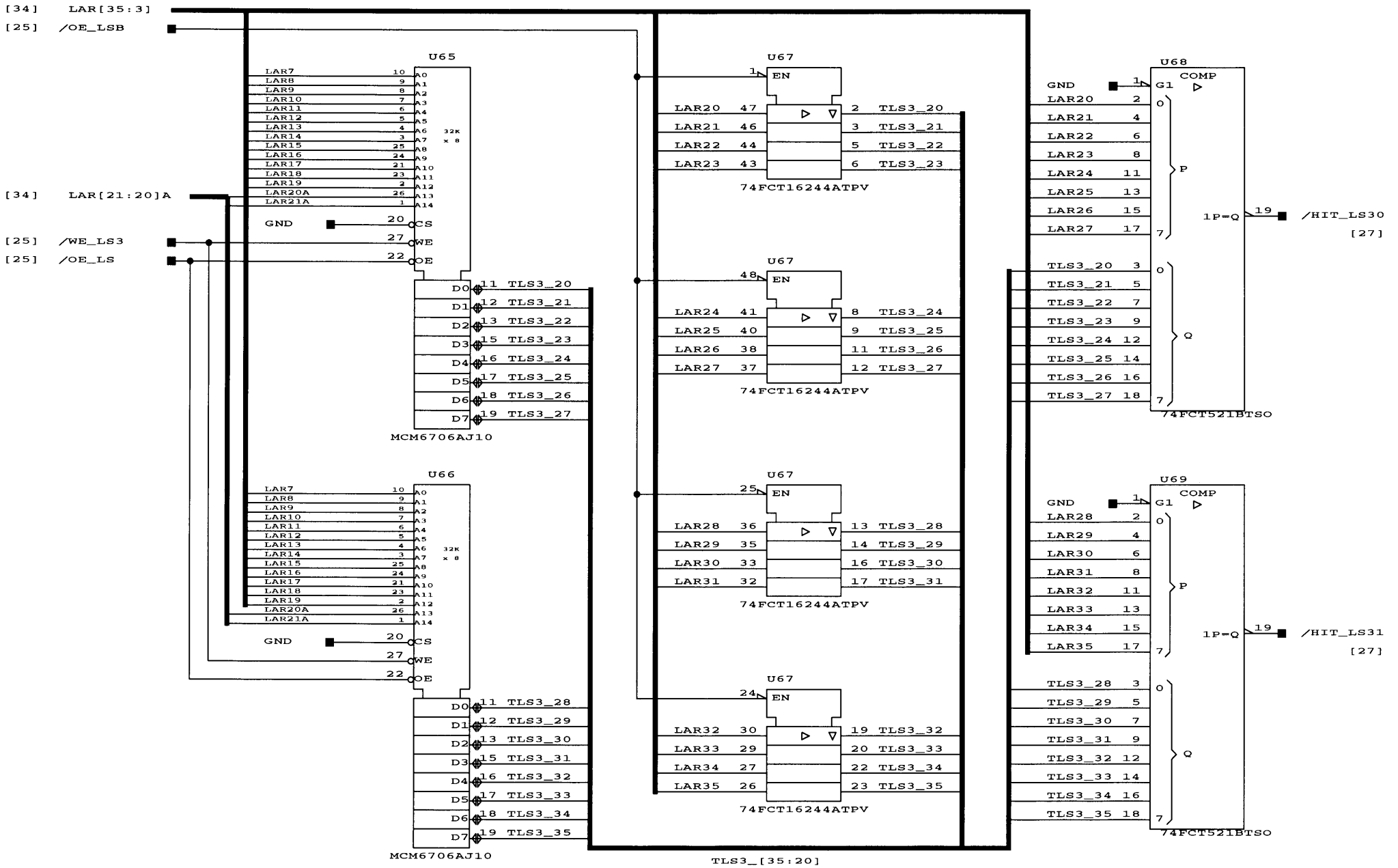
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local snooper 0	
Issue 2			
Issue 3		File: cpu301	Page:35 of 73



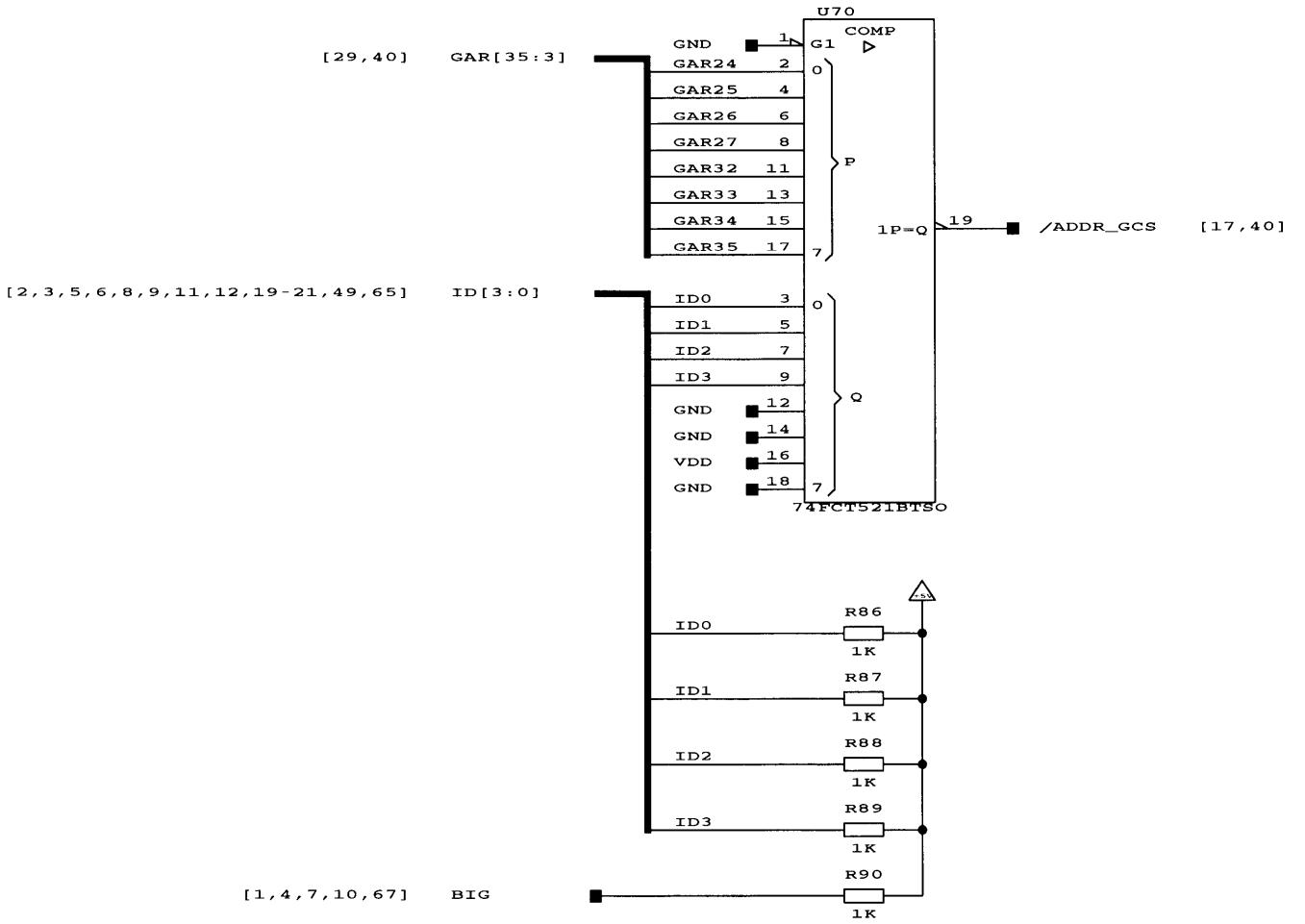
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local snooper 1	
Issue 2			
Issue 3		File: cpu301	Page:36 of 73



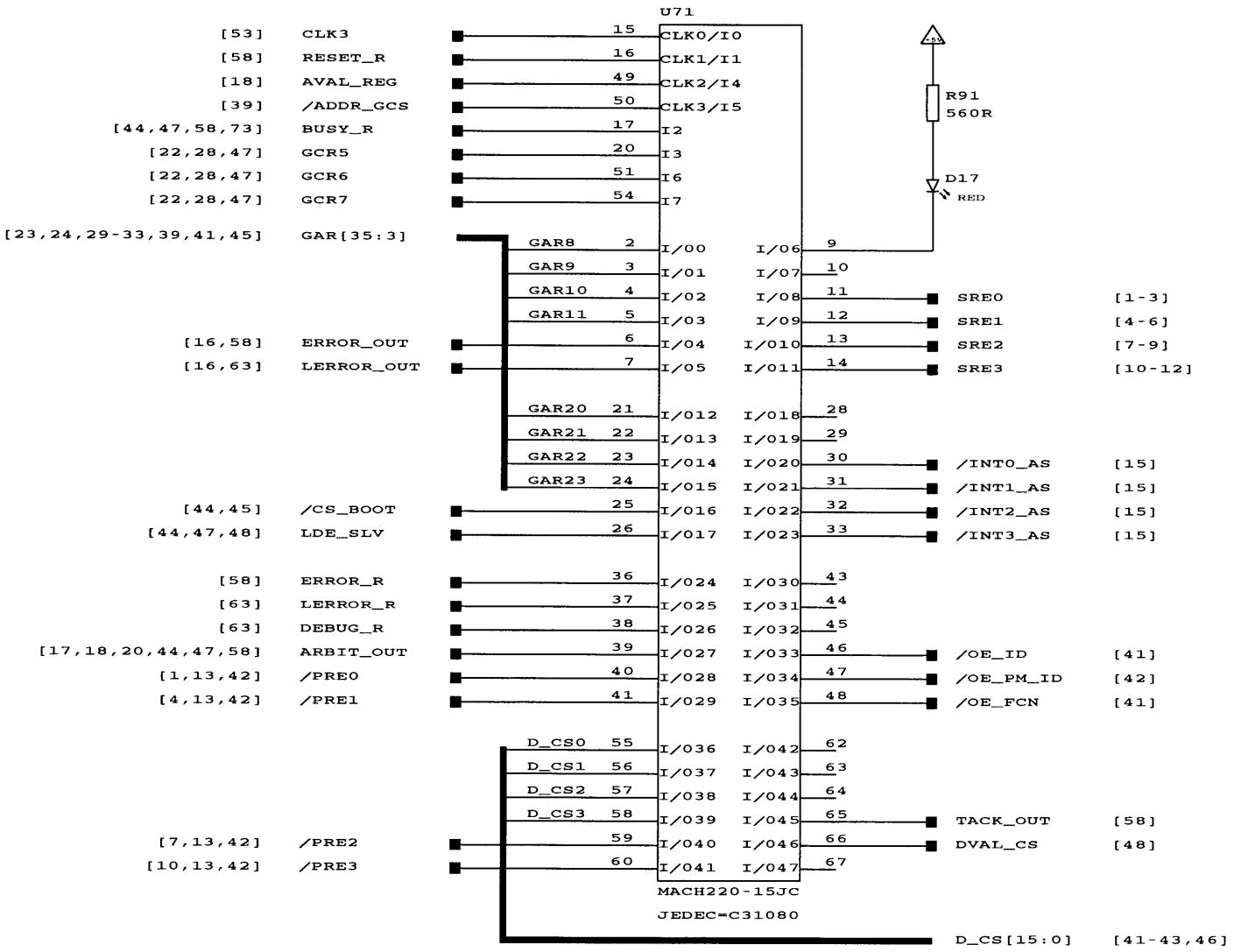
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local snooper 2	
Issue 2			
Issue 3		File: cpu301	Page:37 of 73



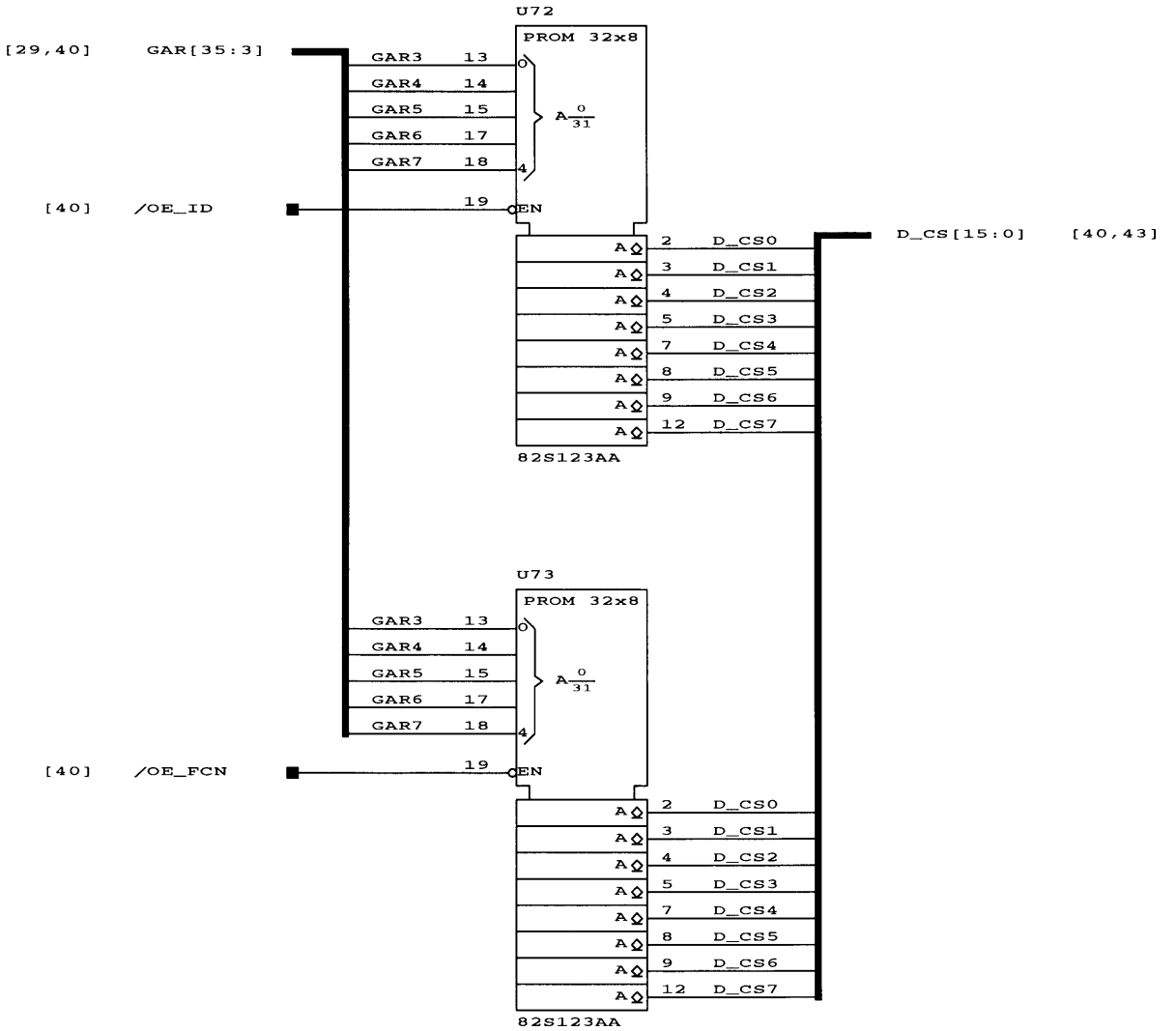
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local snooper 3	
Issue 2			
Issue 3		File: cpu301	Page:38 of 73



dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global control	
Issue 2		space decode	
Issue 3		File: cpu301	Page:39 of 73

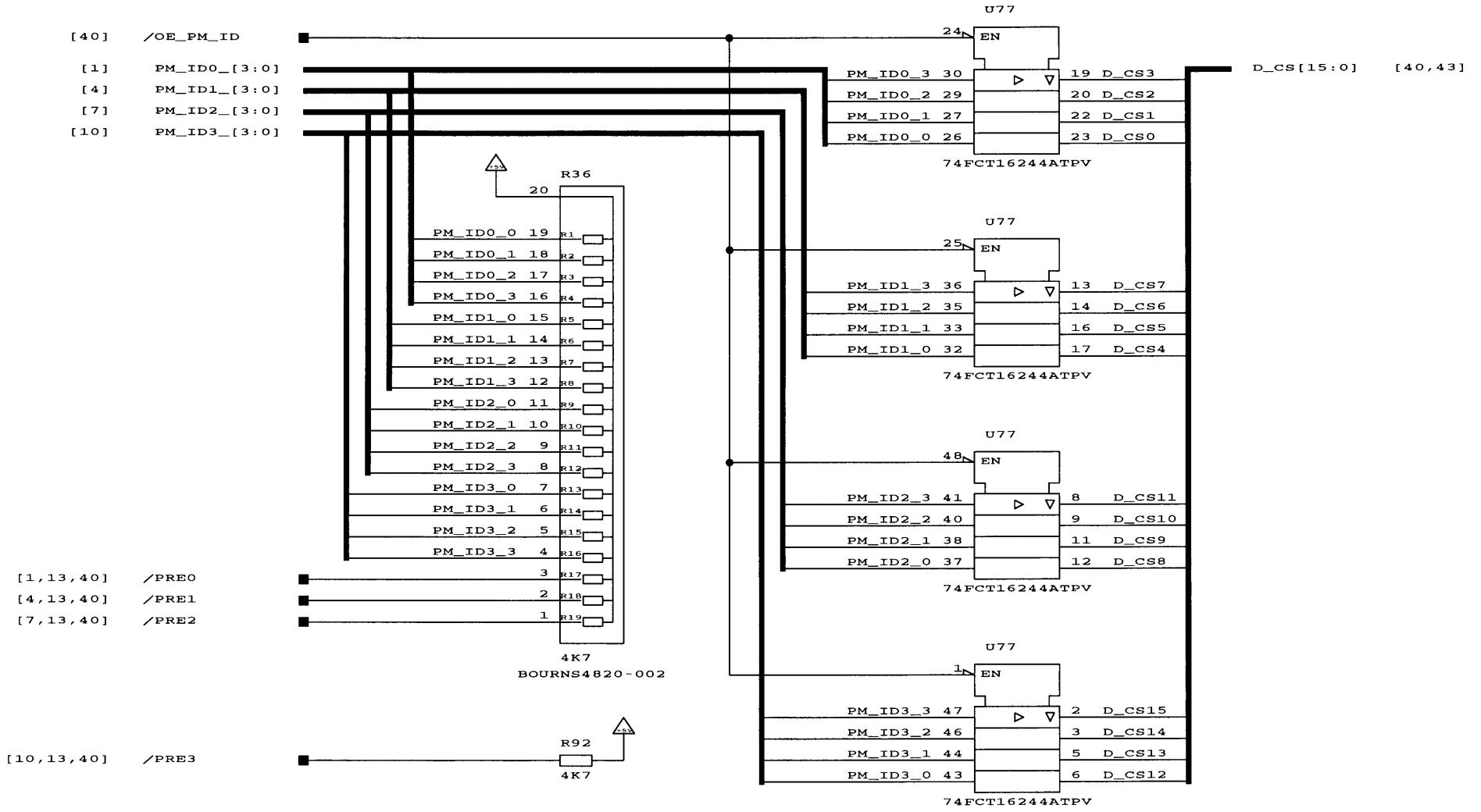


dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global control space	
Issue 2		control	
Issue 3		File: cpu301	Page:40 of 73

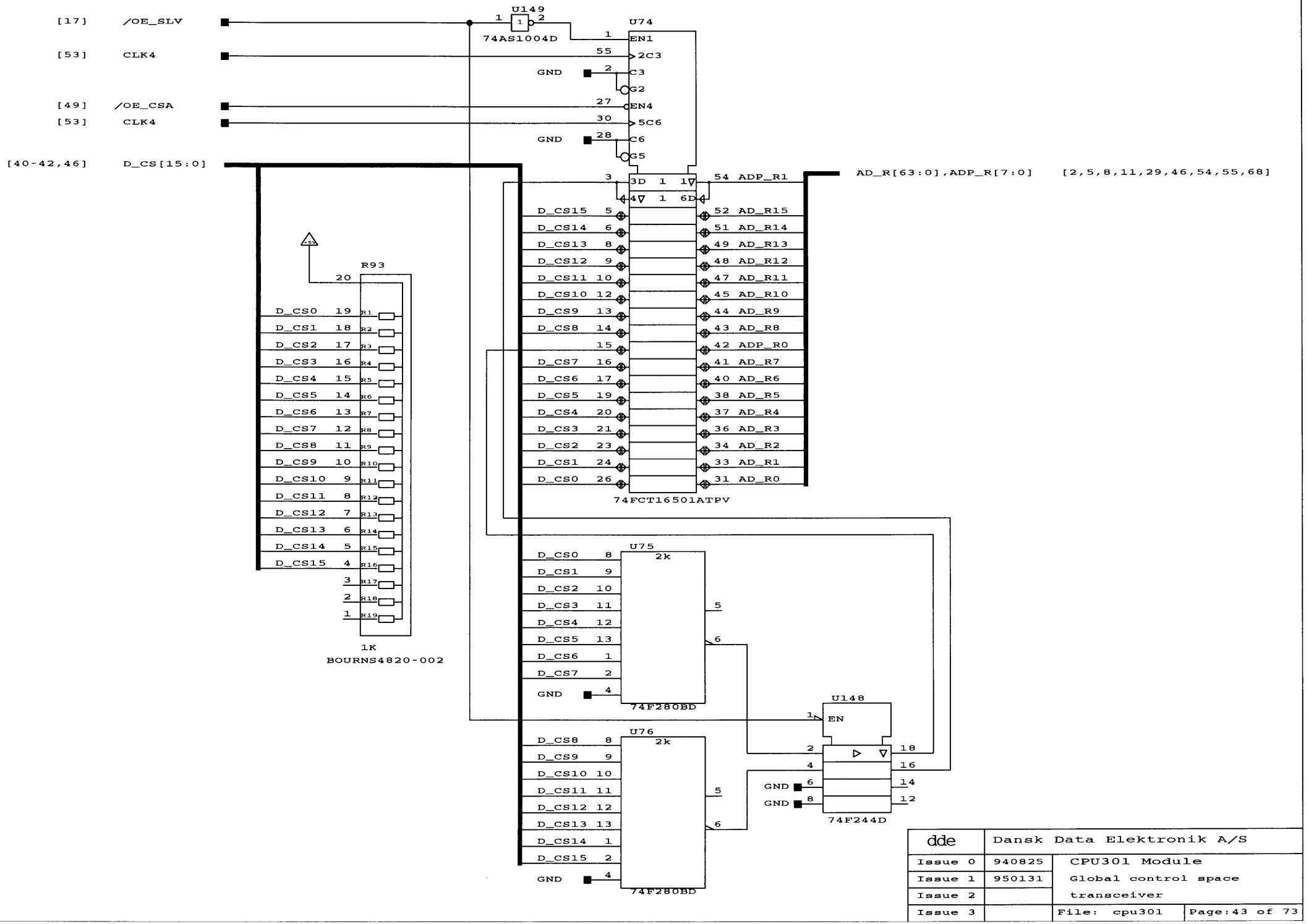


FCN PROM mounted in socket.

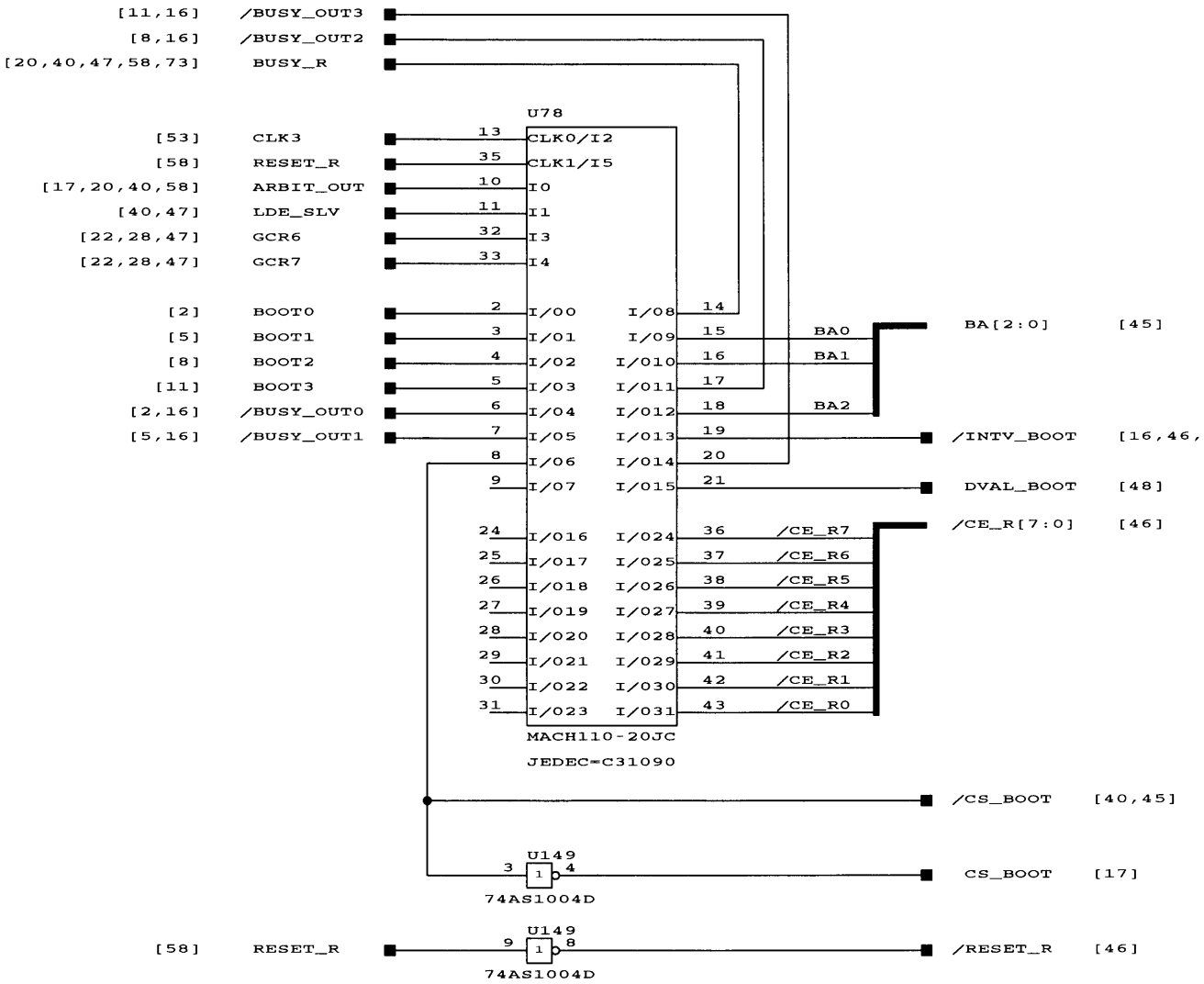
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Module ID and FCN PROMs.	
Issue 2			
Issue 3		File: cpu301	Page:41 of 73



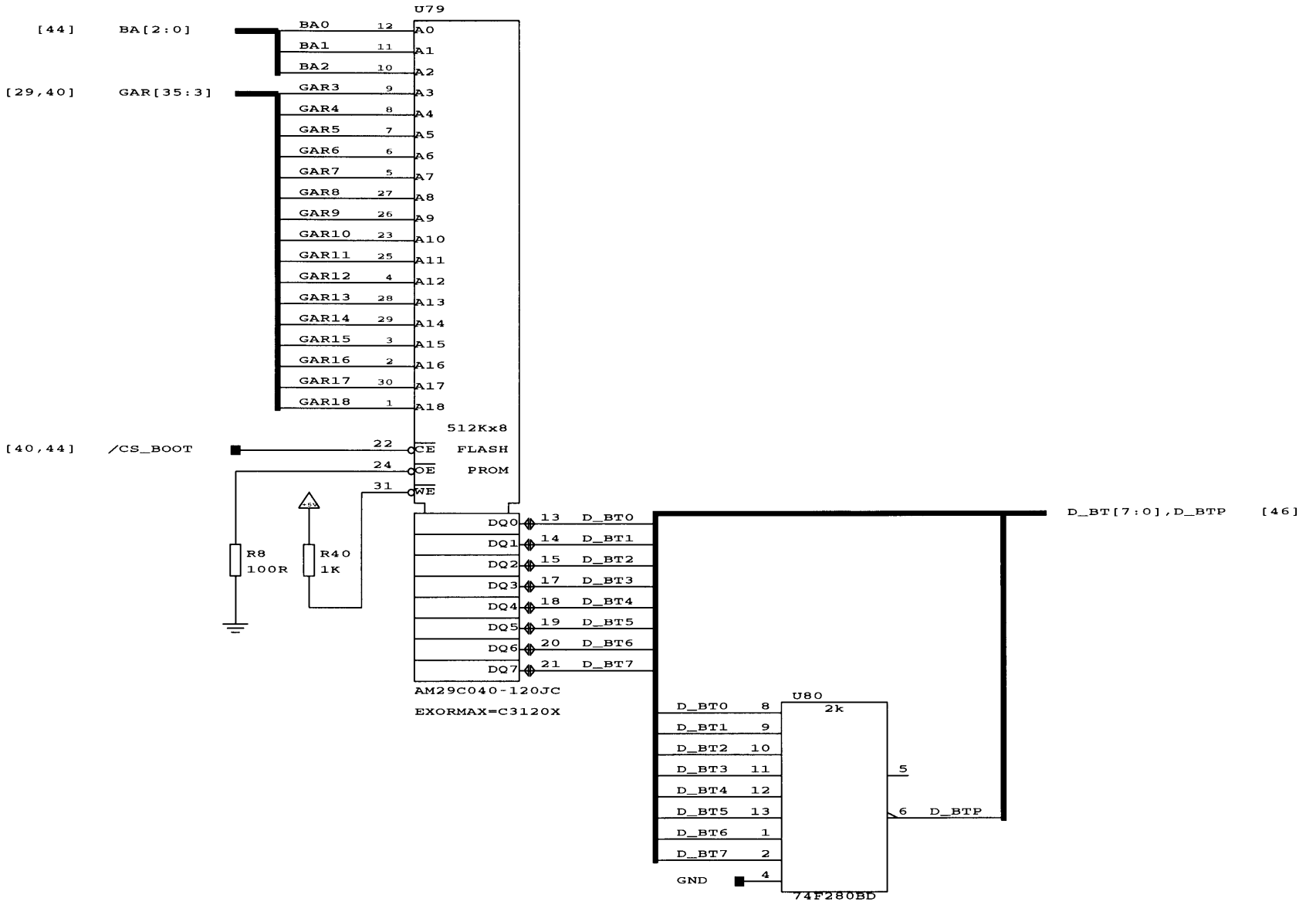
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Processor module	
Issue 2		ID register	
Issue 3		File: cpu301	Page:42 of 73



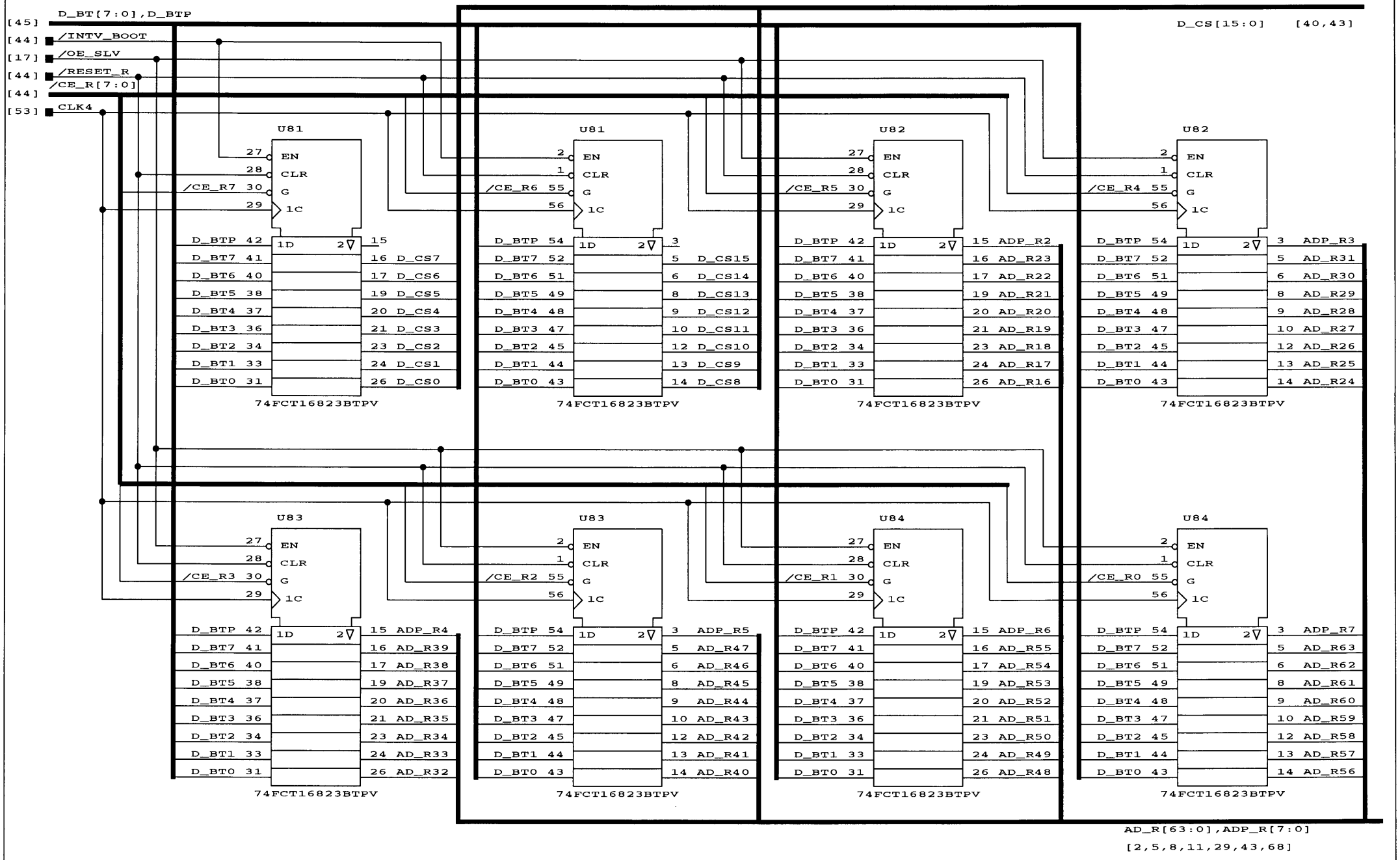
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global control space	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:43 of 73



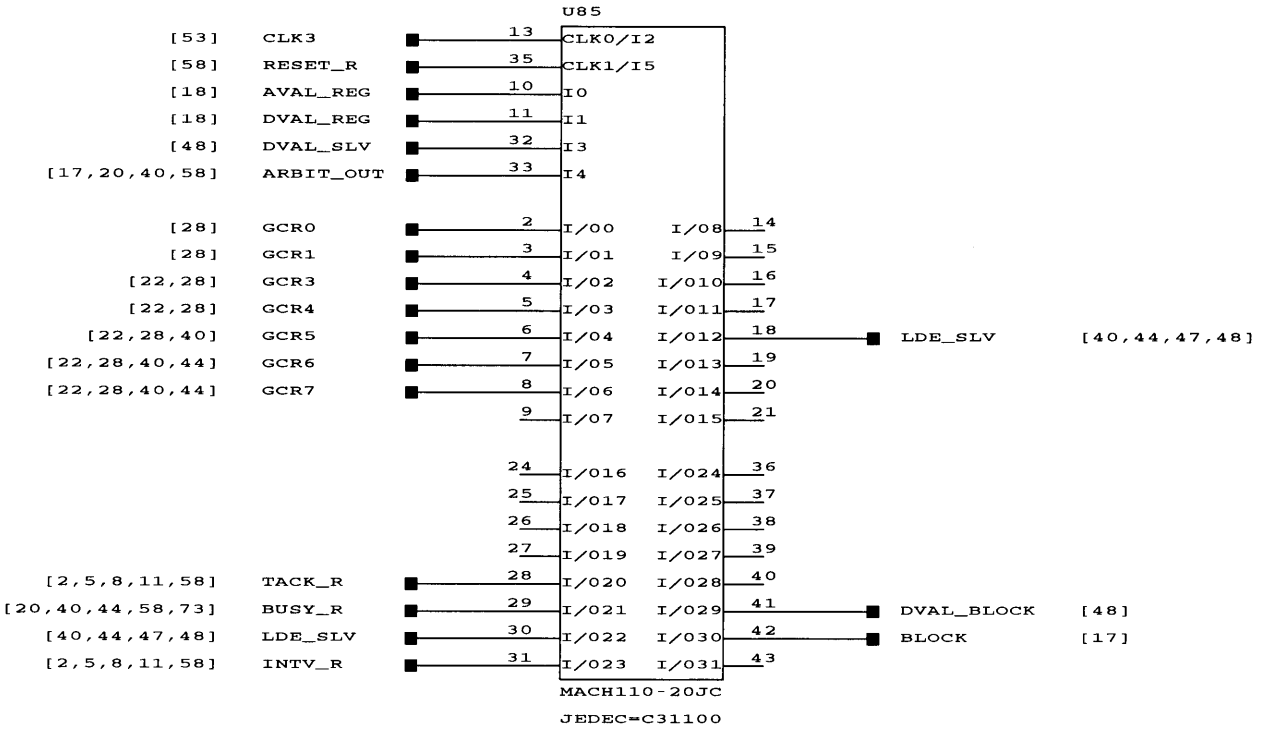
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Boot control	
Issue 2			
Issue 3		File: cpu301	Page:44 of 73



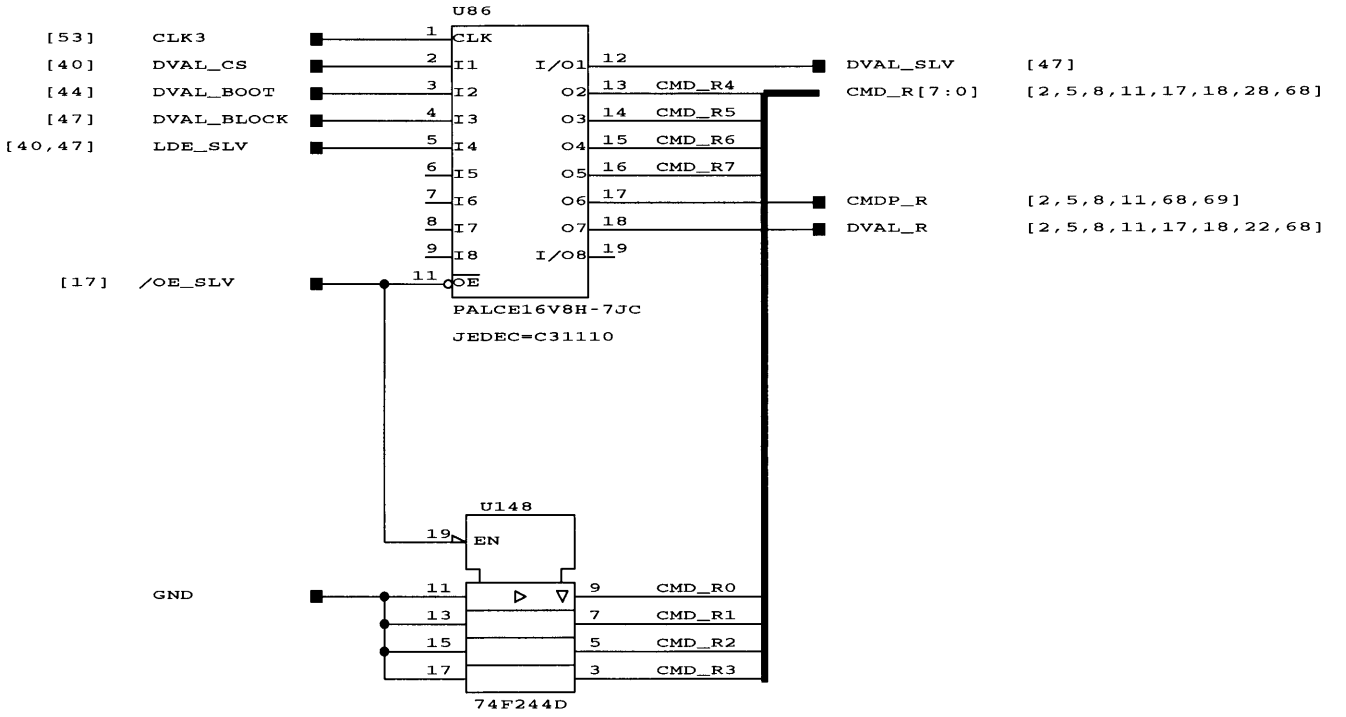
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Boot PROM	
Issue 2			
Issue 3		File: cpu301	Page:45 of 73



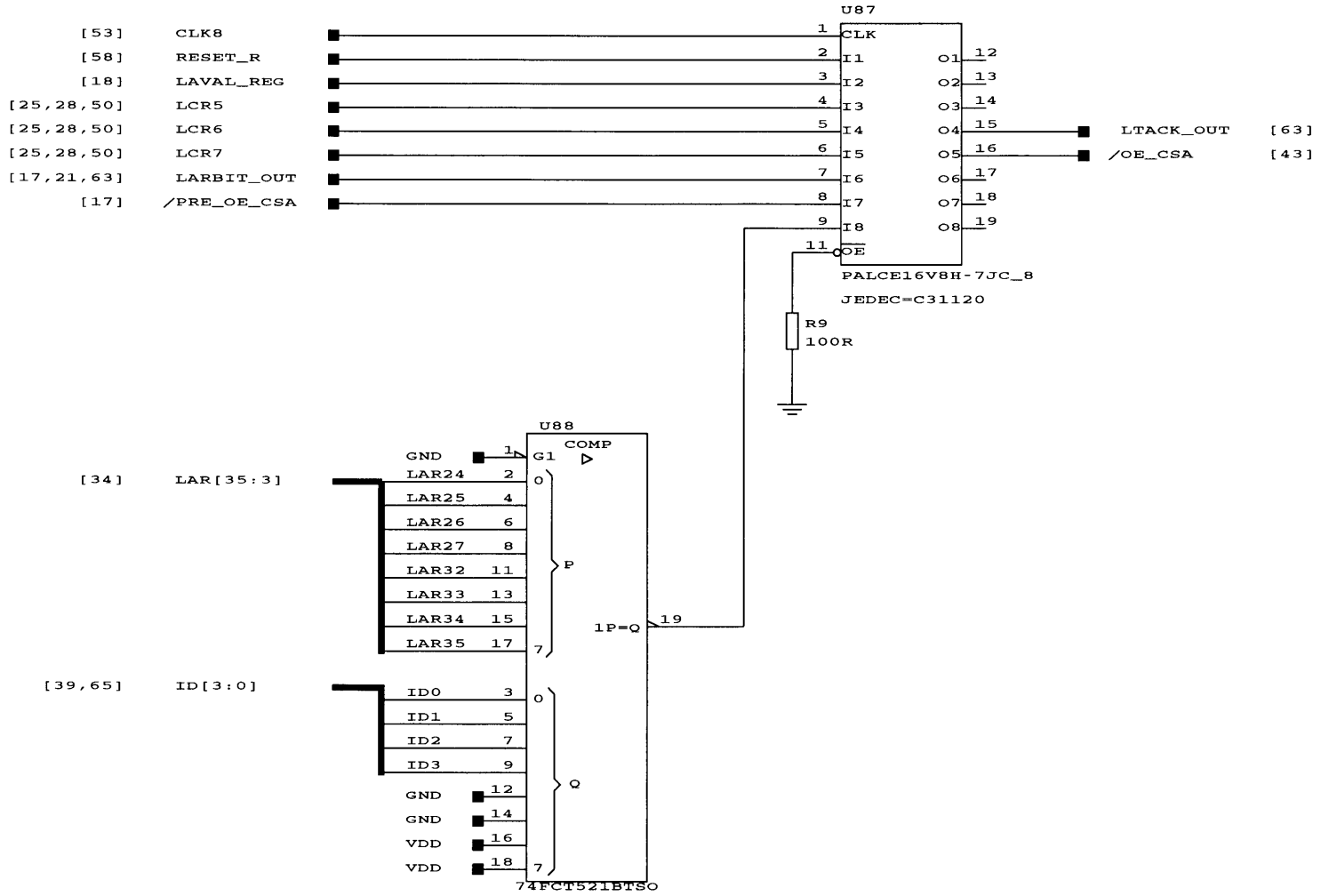
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Boot register	
Issue 2			
Issue 3		File: cpu301	Page:46 of 73



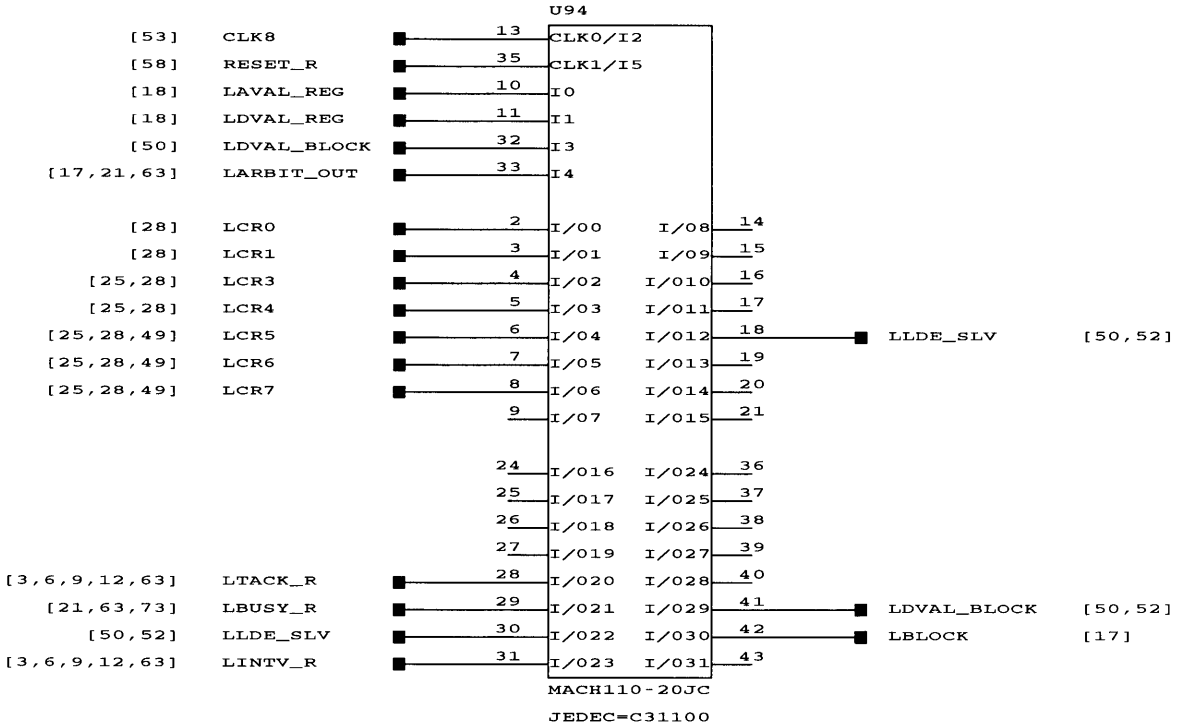
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global dummy	
Issue 2		block generator	
Issue 3		File: cpu301	Page:47 of 73



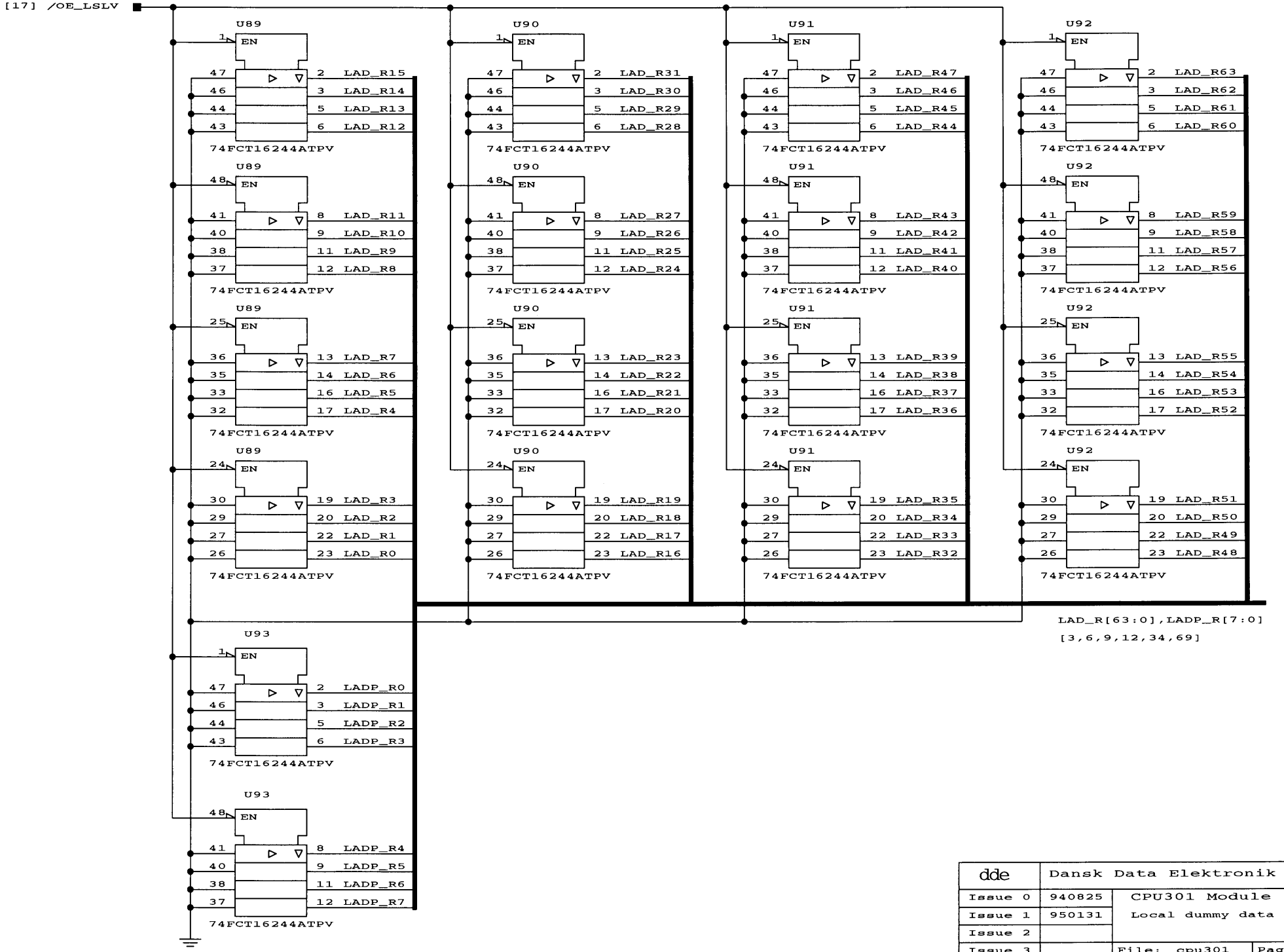
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global data identifier	
Issue 2		output register	
Issue 3		File: cpu301	Page:48 of 73



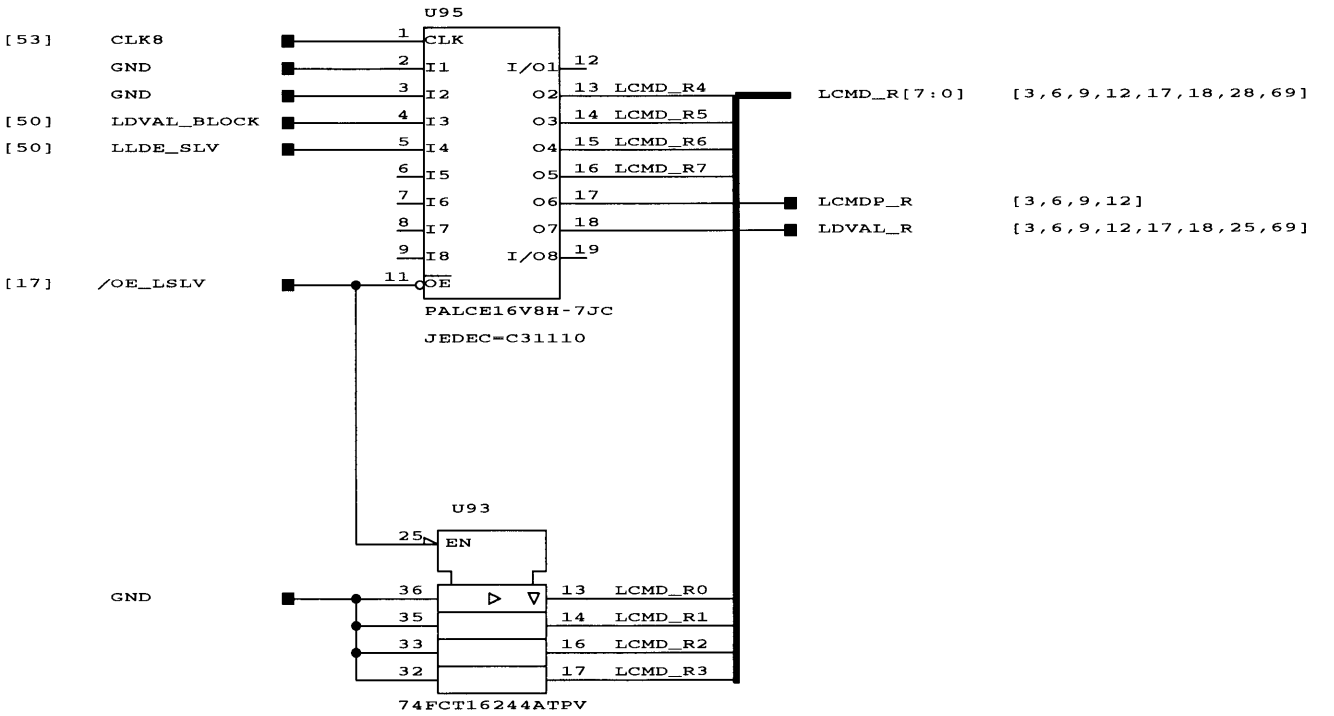
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local control space decode	
Issue 2		and target acknowledge	
Issue 3		File: cpu301	Page:49 of 73



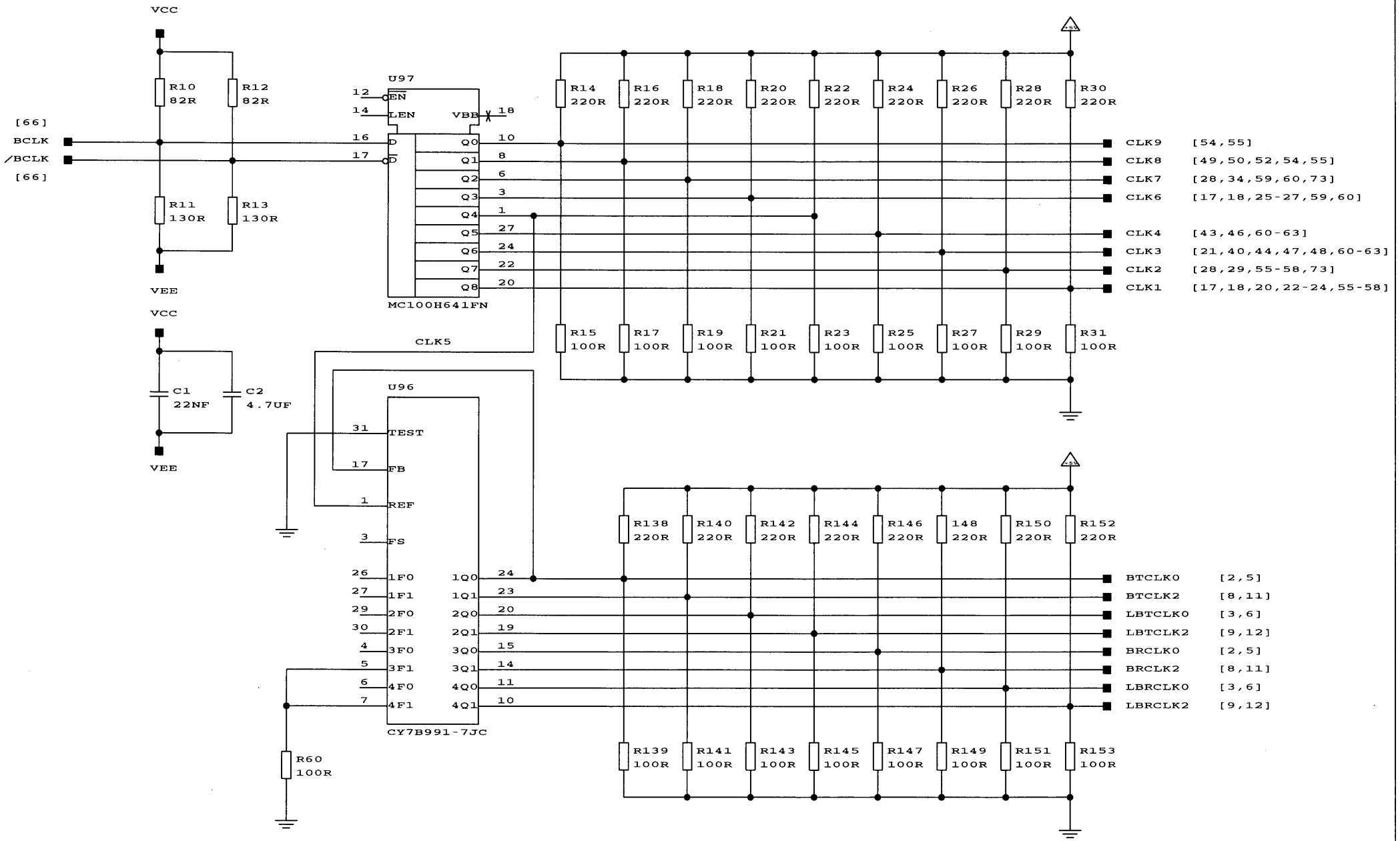
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local dummy block generator	
Issue 2			
Issue 3		File: cpu301	Page:50 of 73



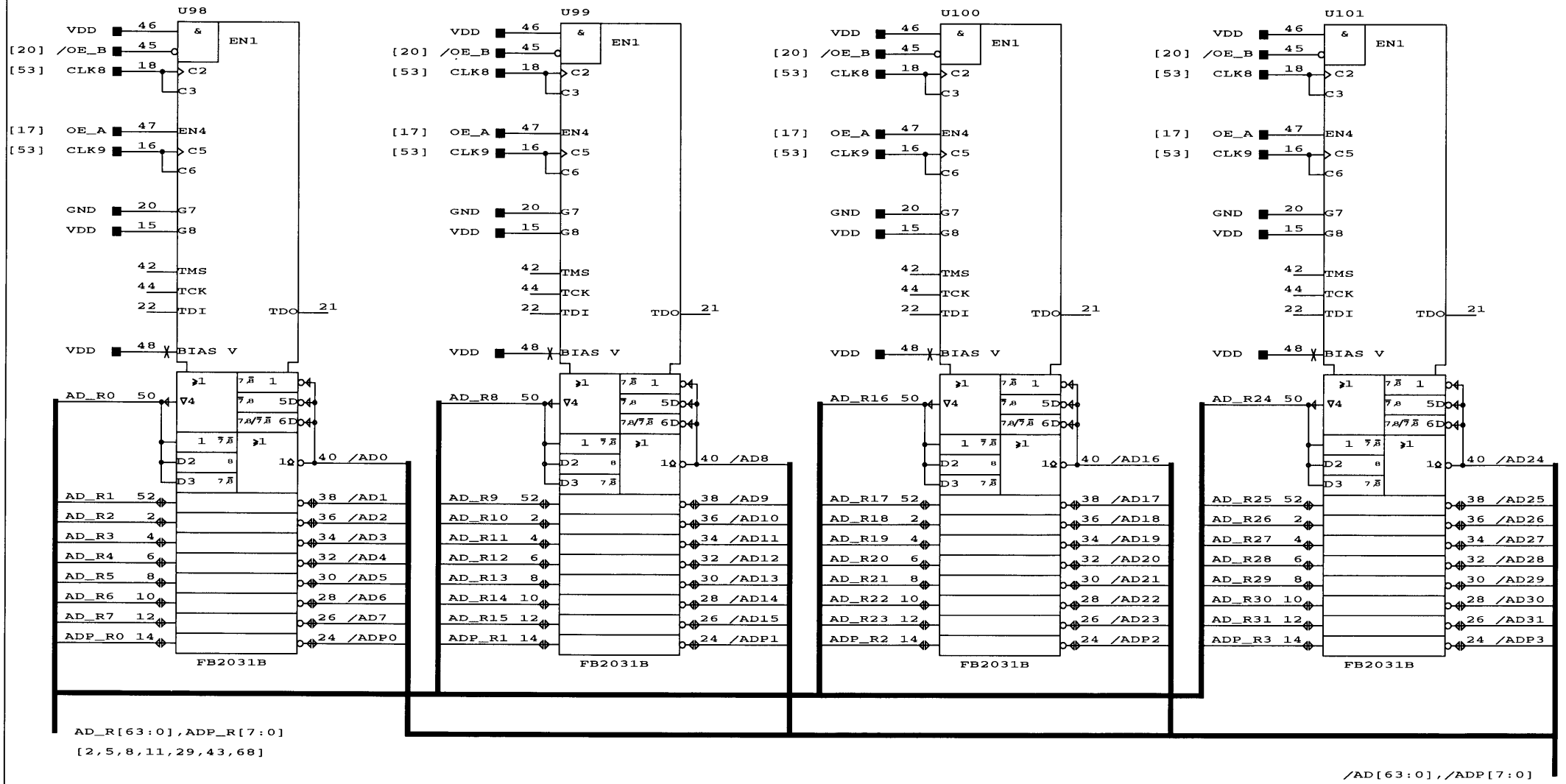
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local dummy data	
Issue 2			
Issue 3		File: cpu301	Page:51 of 73



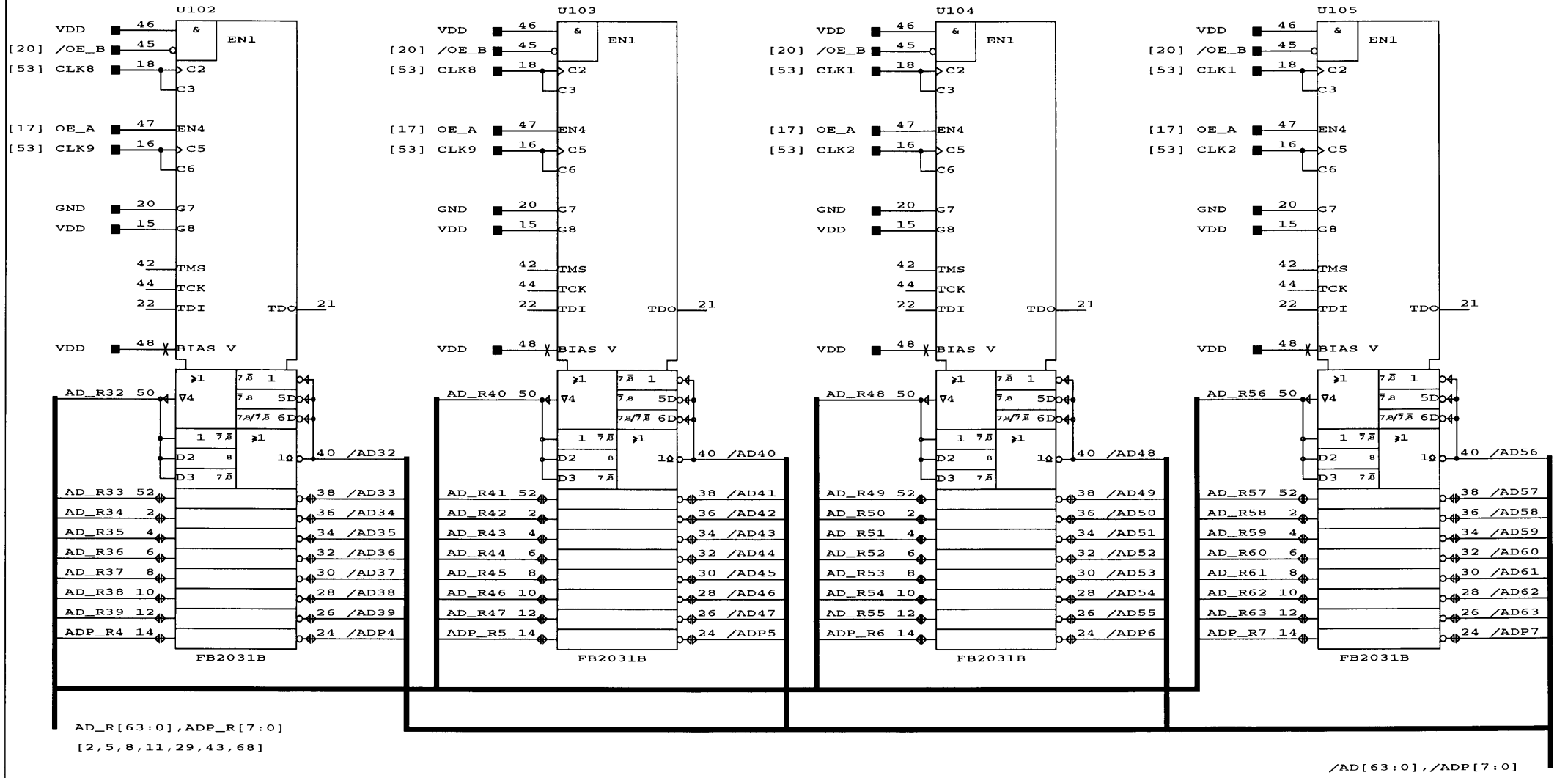
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local data identifier	
Issue 2		output register	
Issue 3		File: cpu301	Page:52 of 73



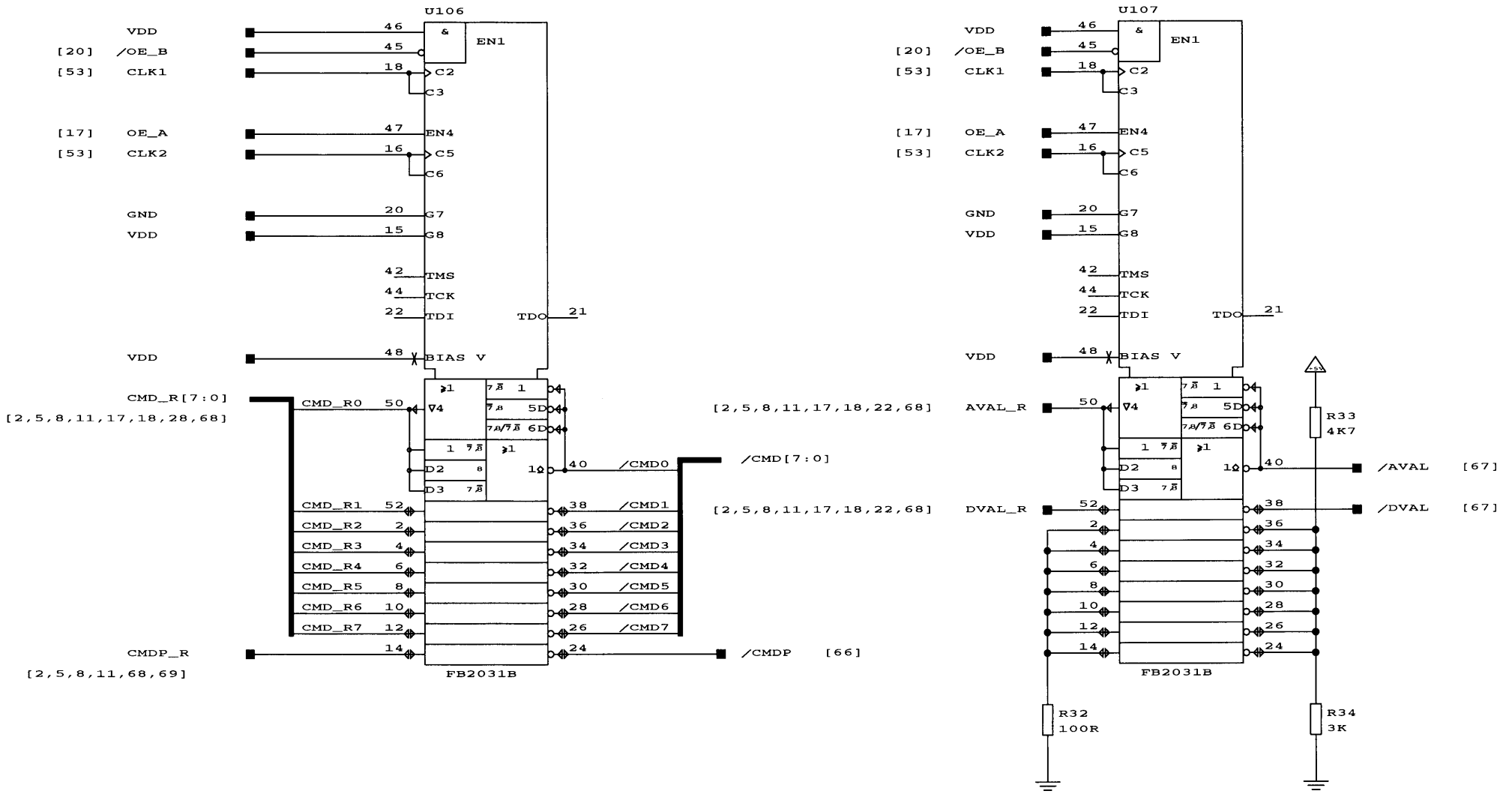
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Clock distribution	
Issue 2			
Issue 3		File: cpu301	Page:53 of 73



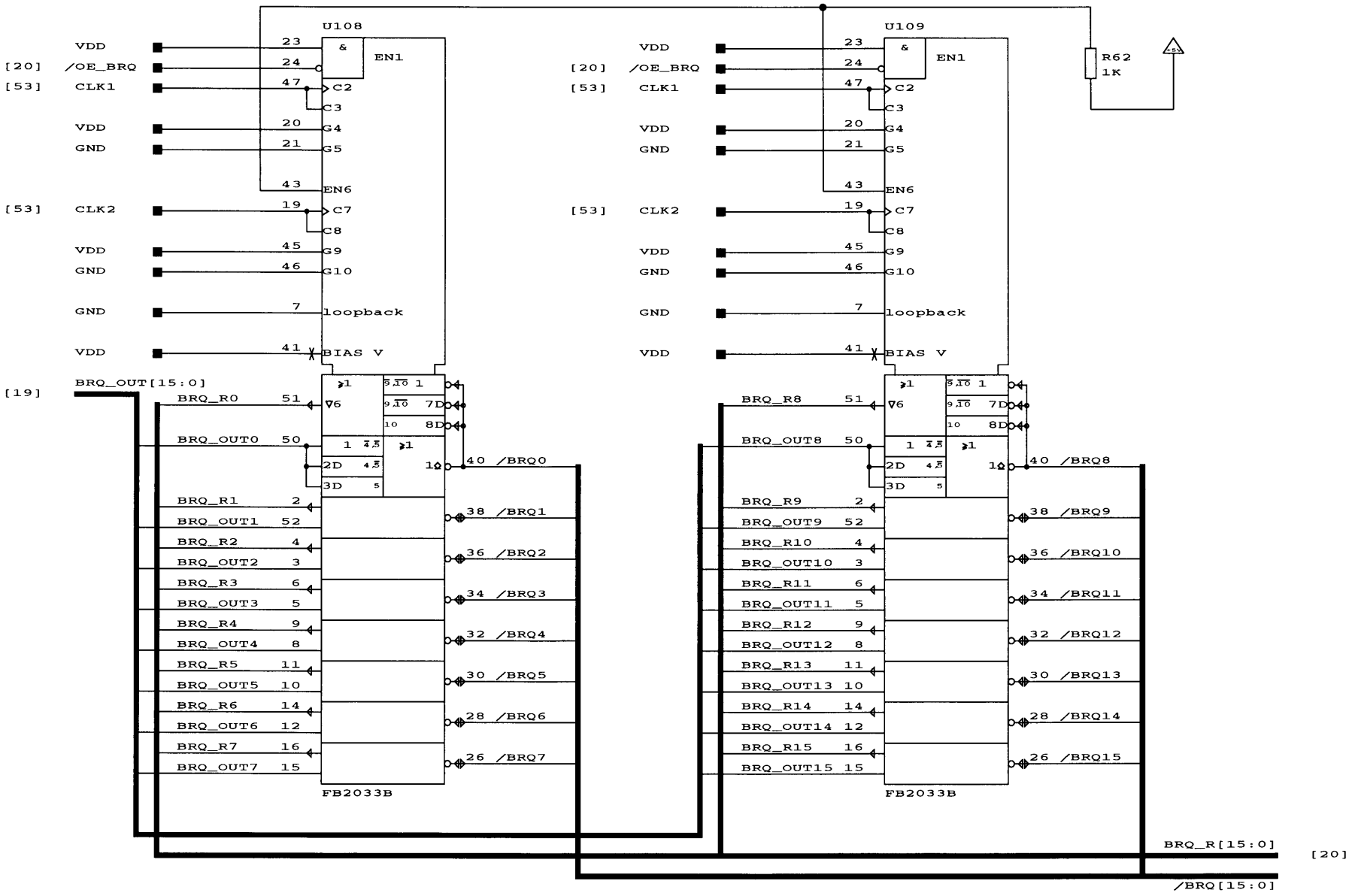
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global address/data	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:54 of 73



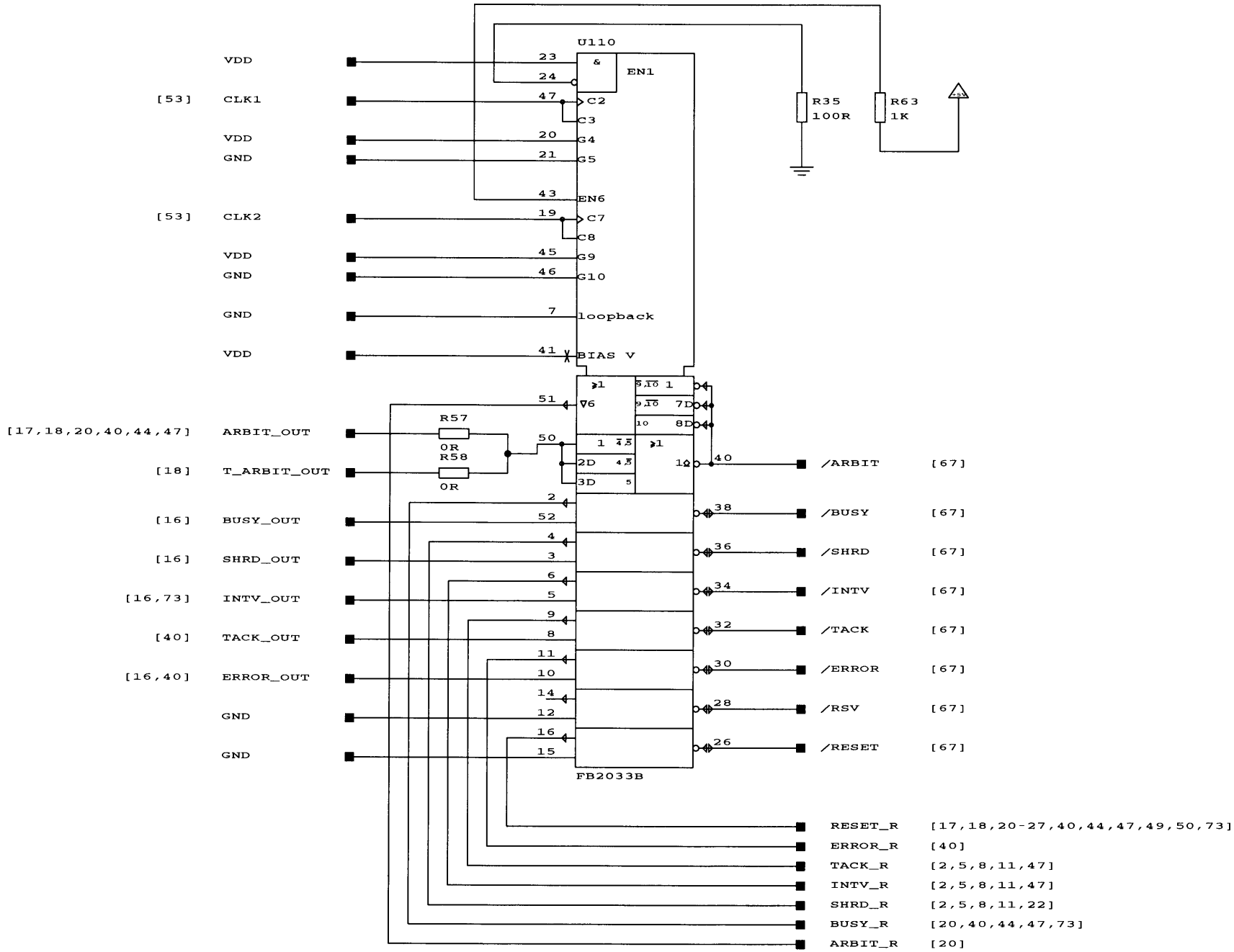
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global address/data	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:55 of 73



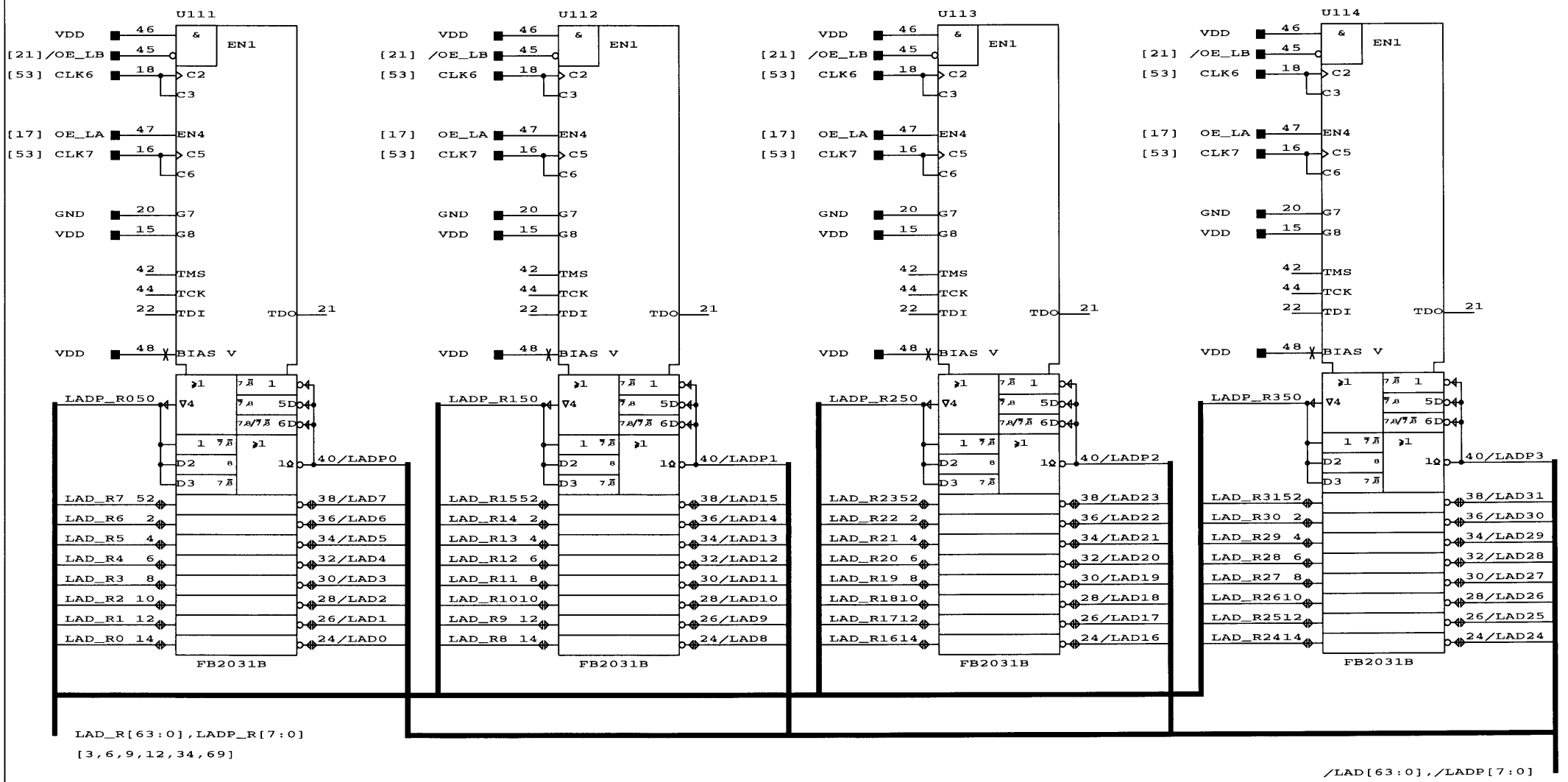
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global command and valid	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:56 of 73



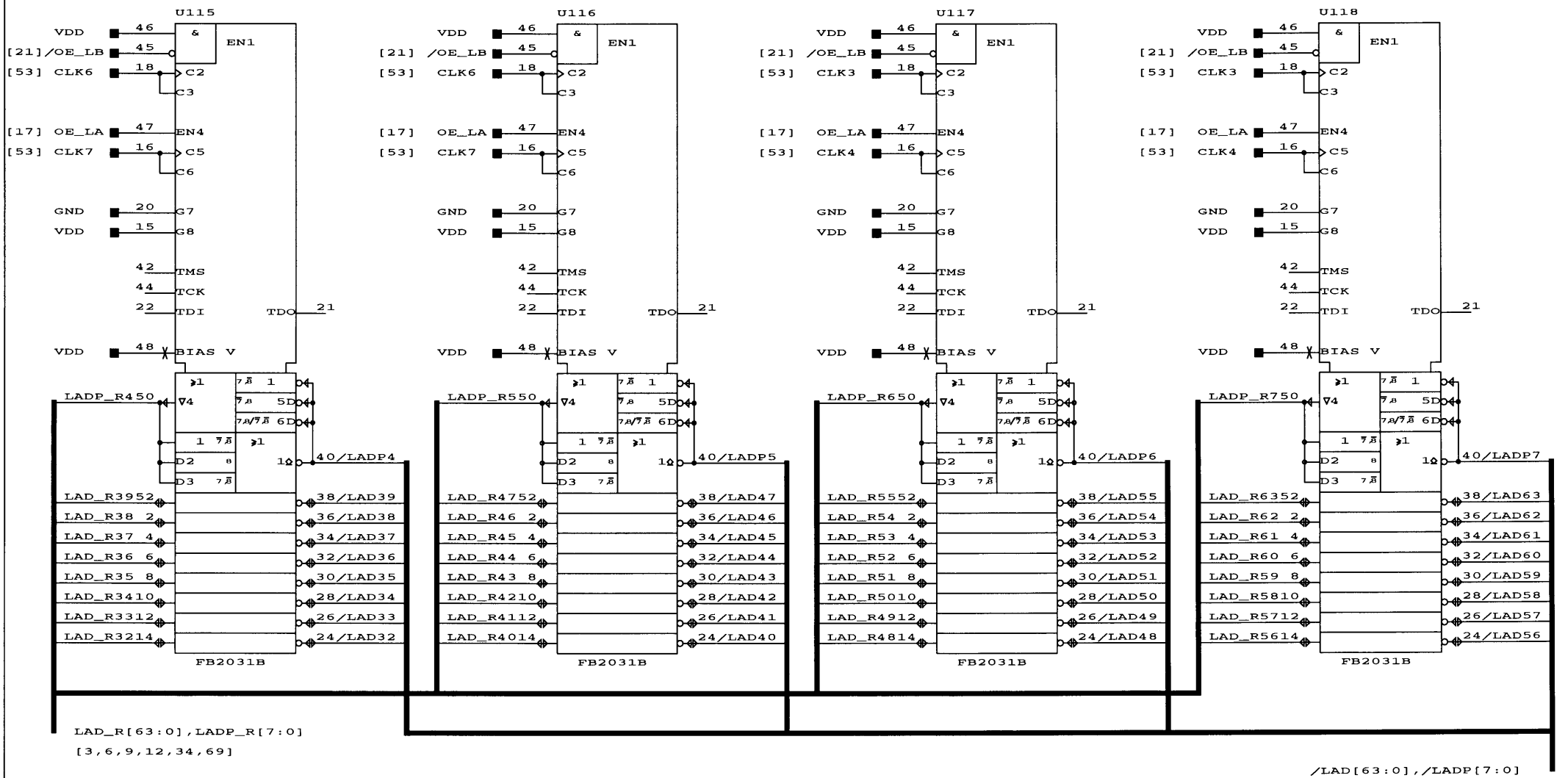
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global bus request	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:57 of 73



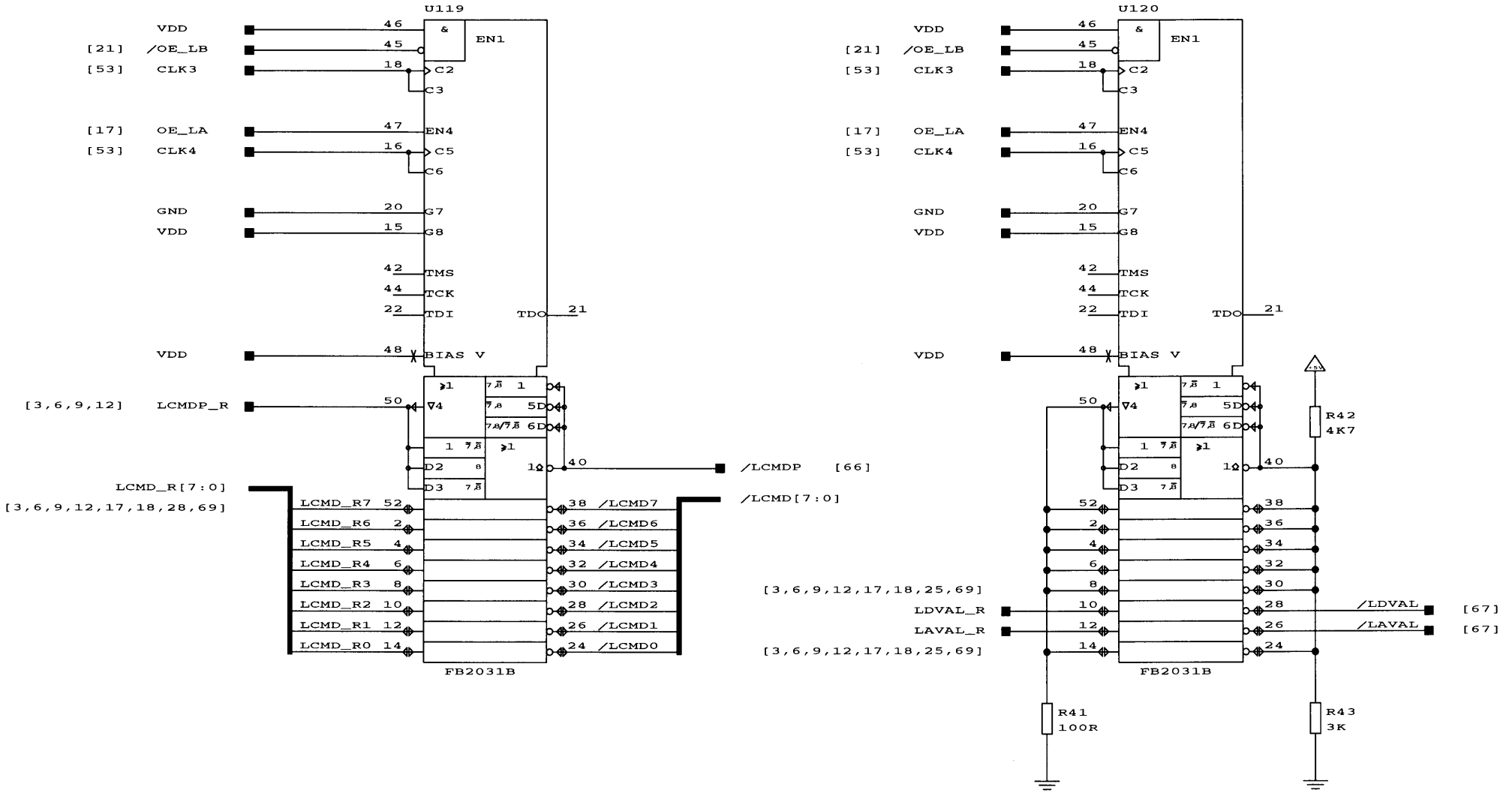
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Global control transceiver	
Issue 2			
Issue 3		File: cpu301	Page:58 of 73



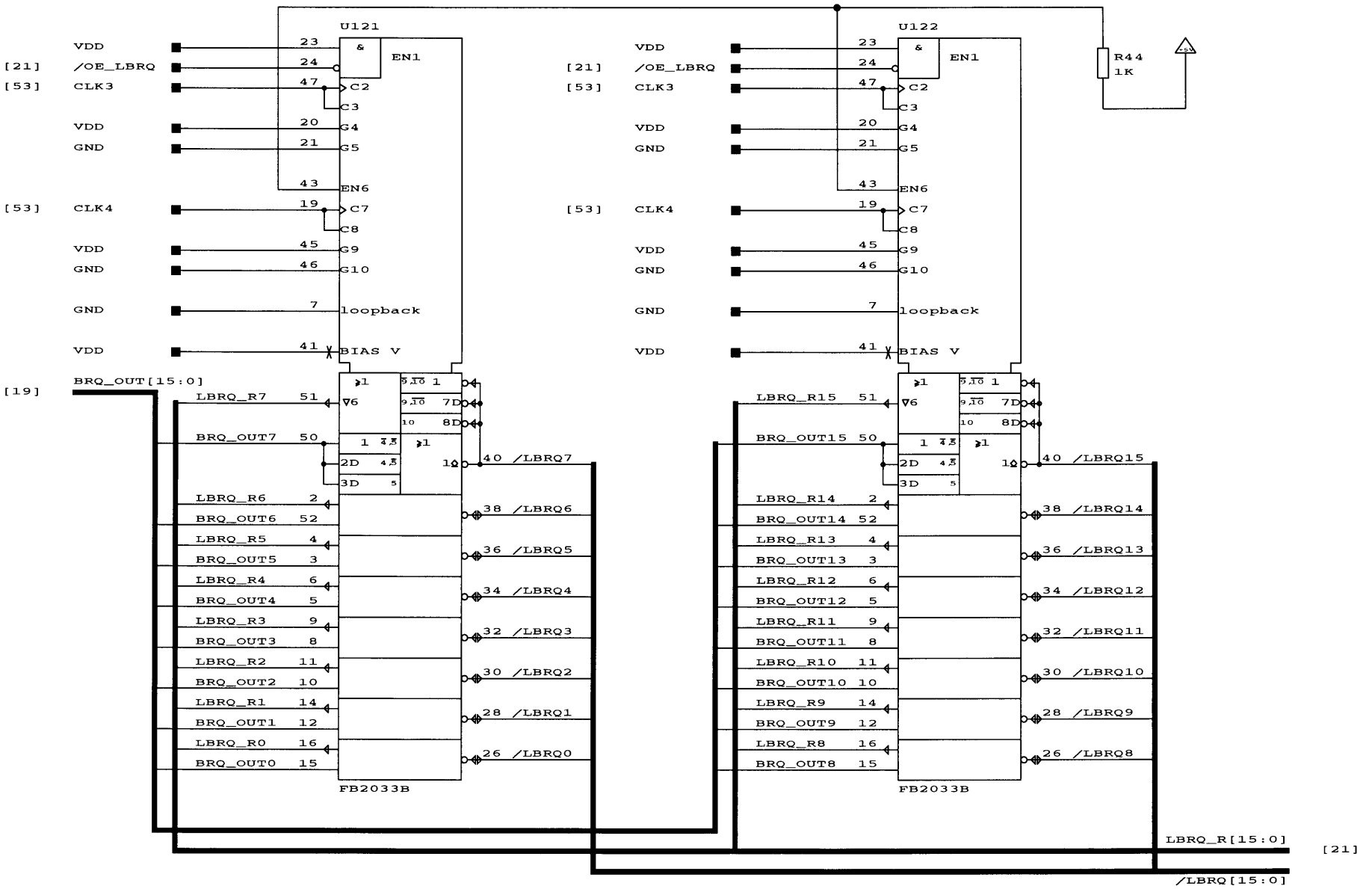
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local address/data	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:59 of 73



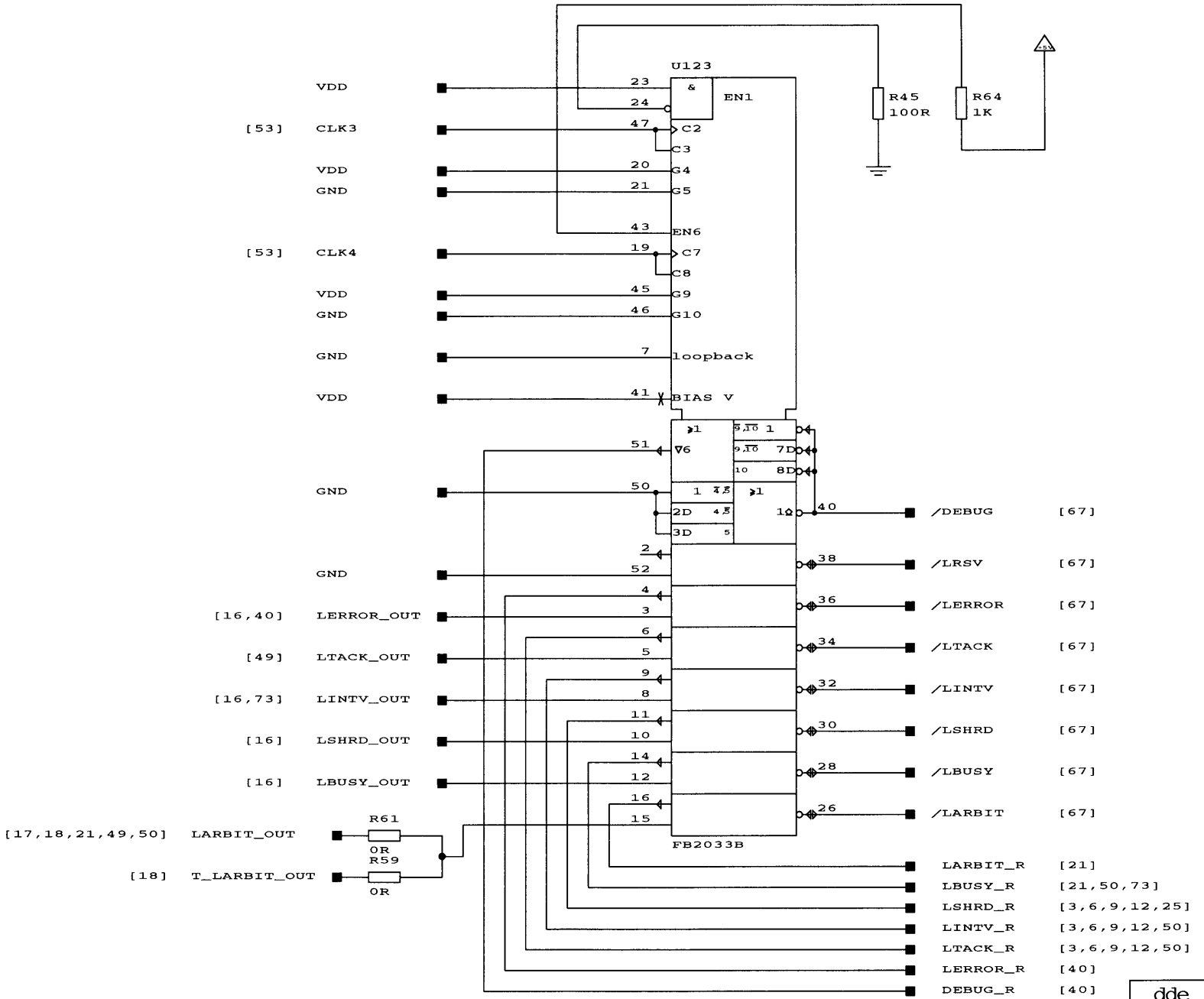
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local address/data	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:60 of 73



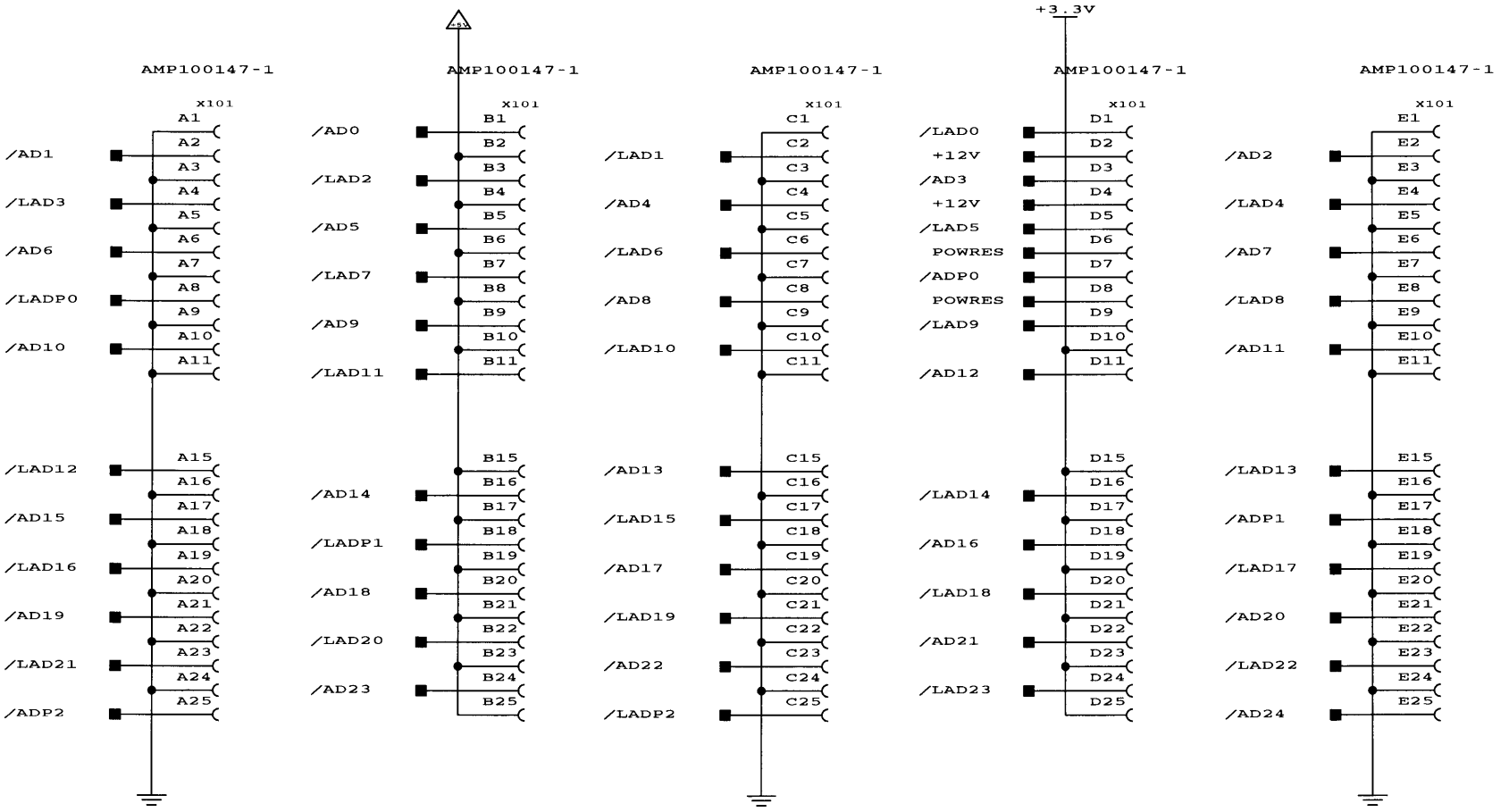
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local command and valid	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:61 of 73



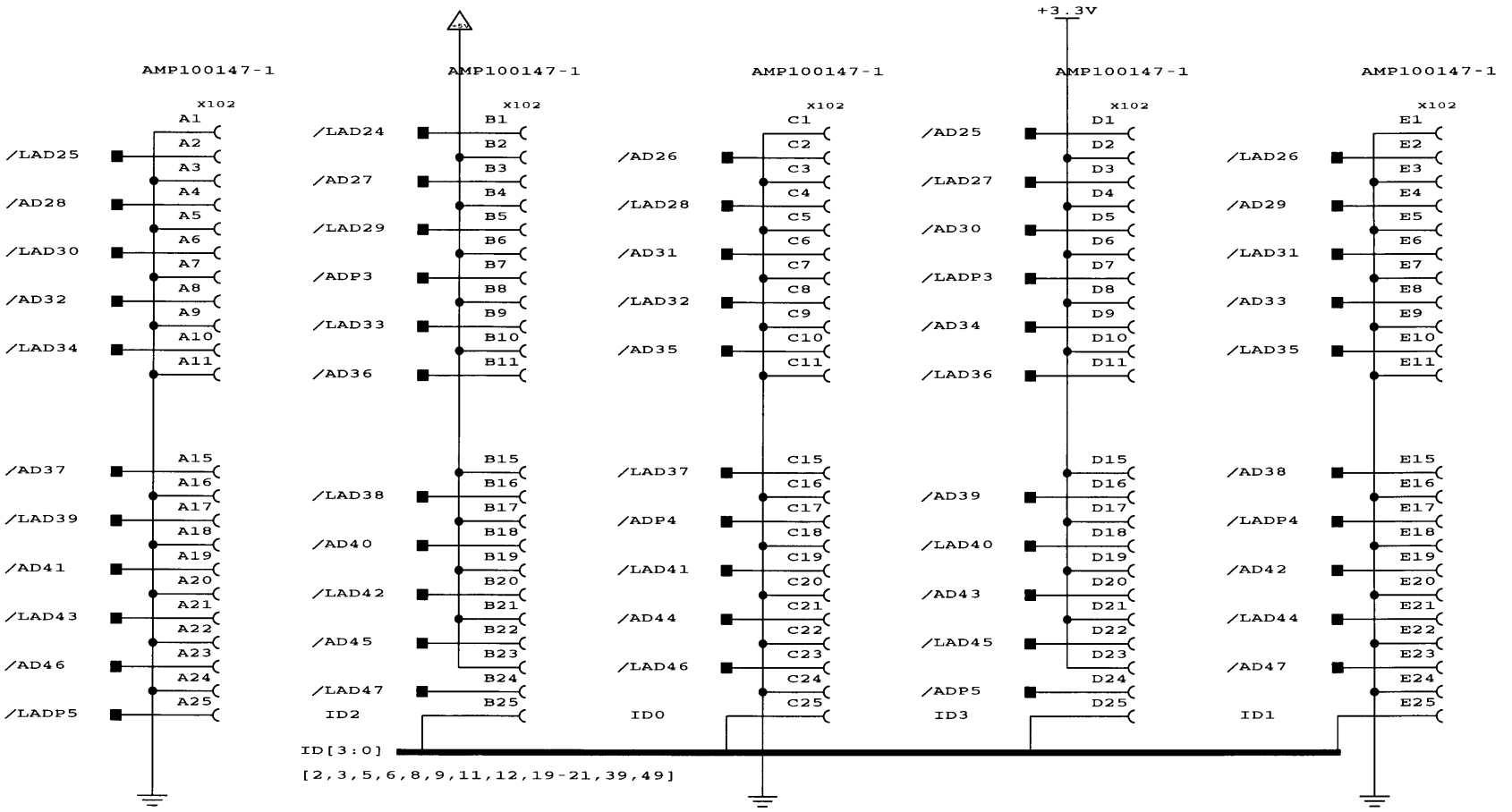
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local bus request	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:62 of 73



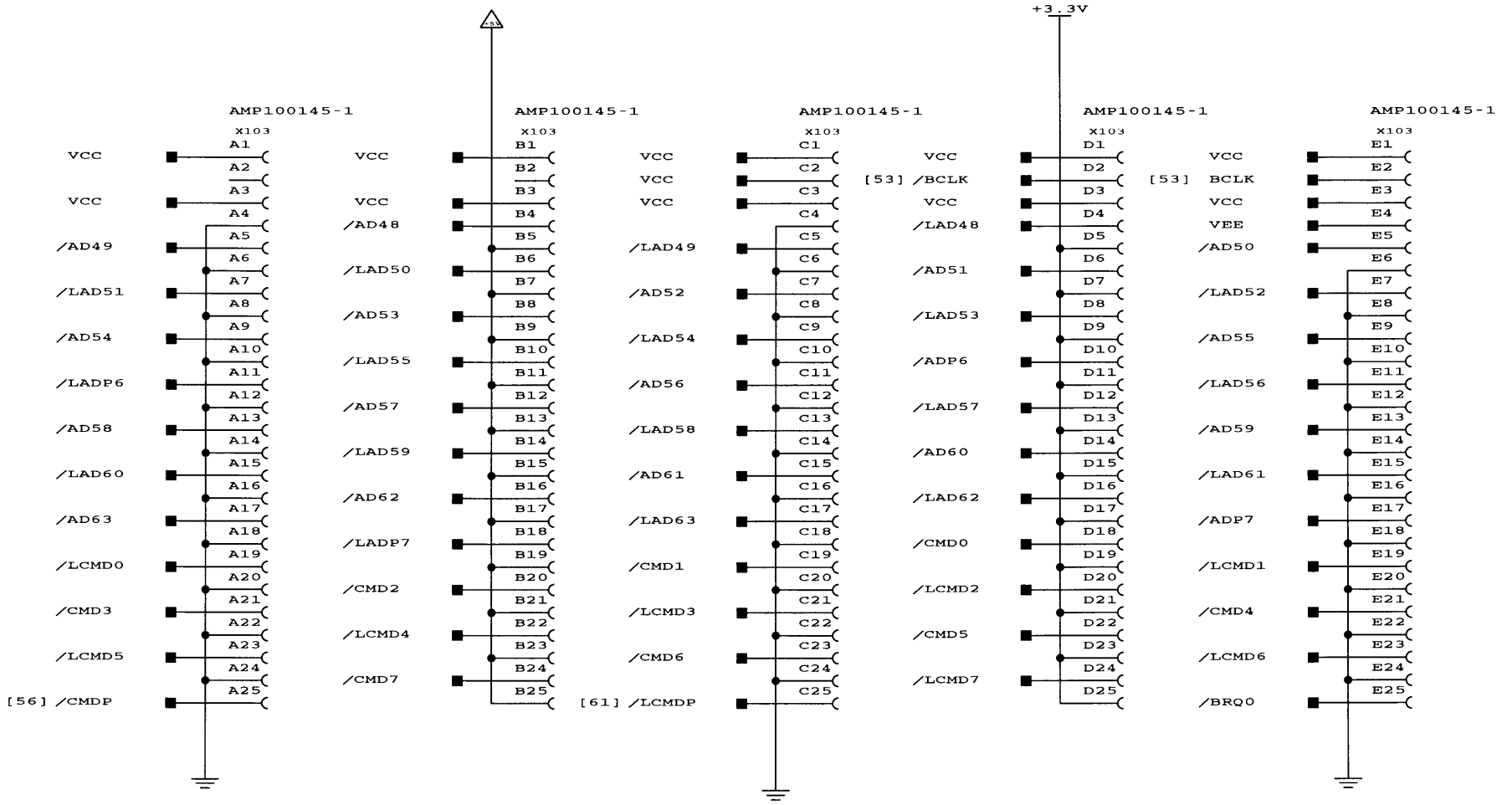
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Local control transceiver	
Issue 2			
Issue 3		File: cpu301	Page:63 of 73



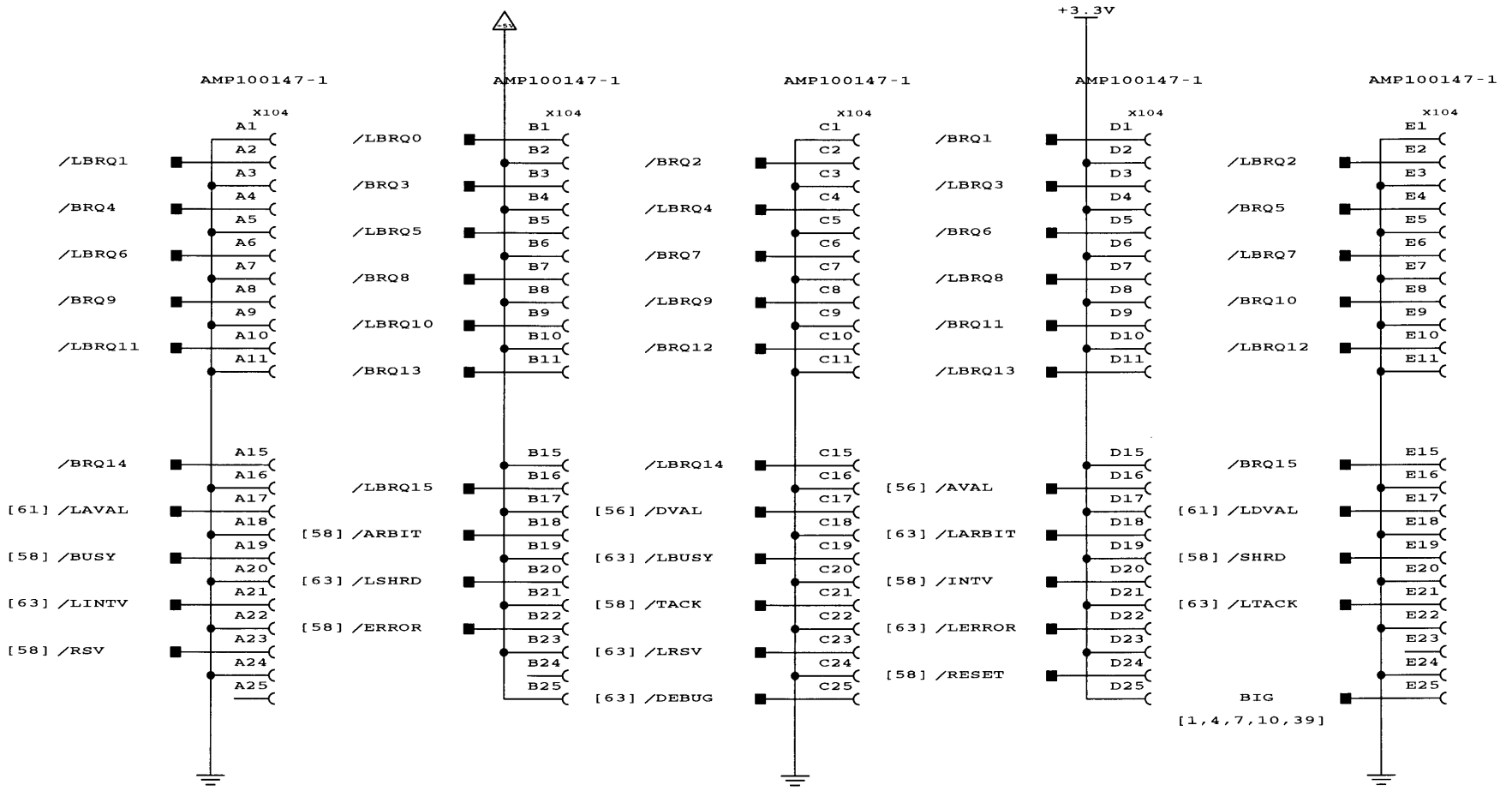
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connector (row 1-25)	
Issue 2			
Issue 3		File: cpu301	Page:64 of 73



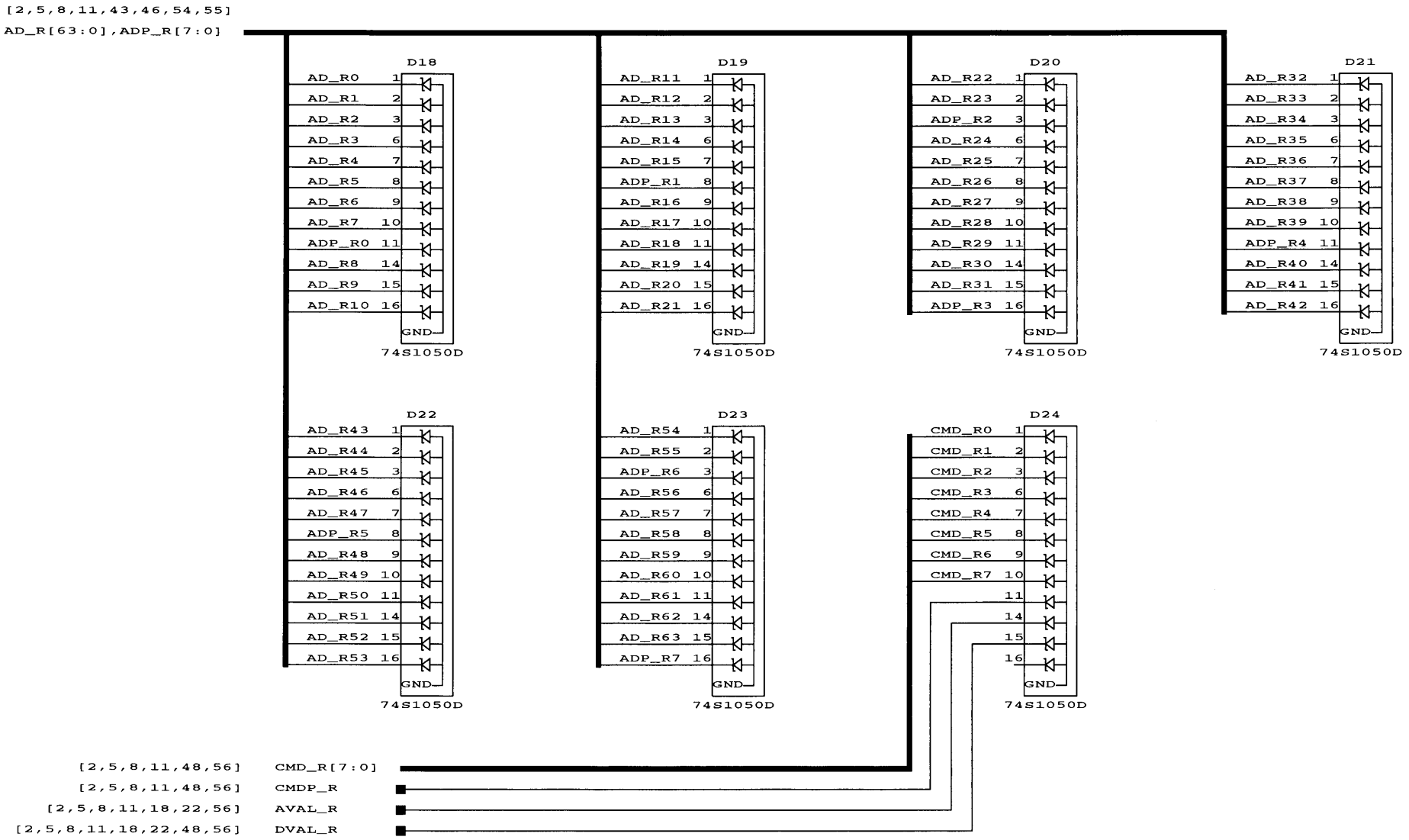
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connector (row 26-50)	
Issue 2			
Issue 3		File: cpu301	Page:65 of 73



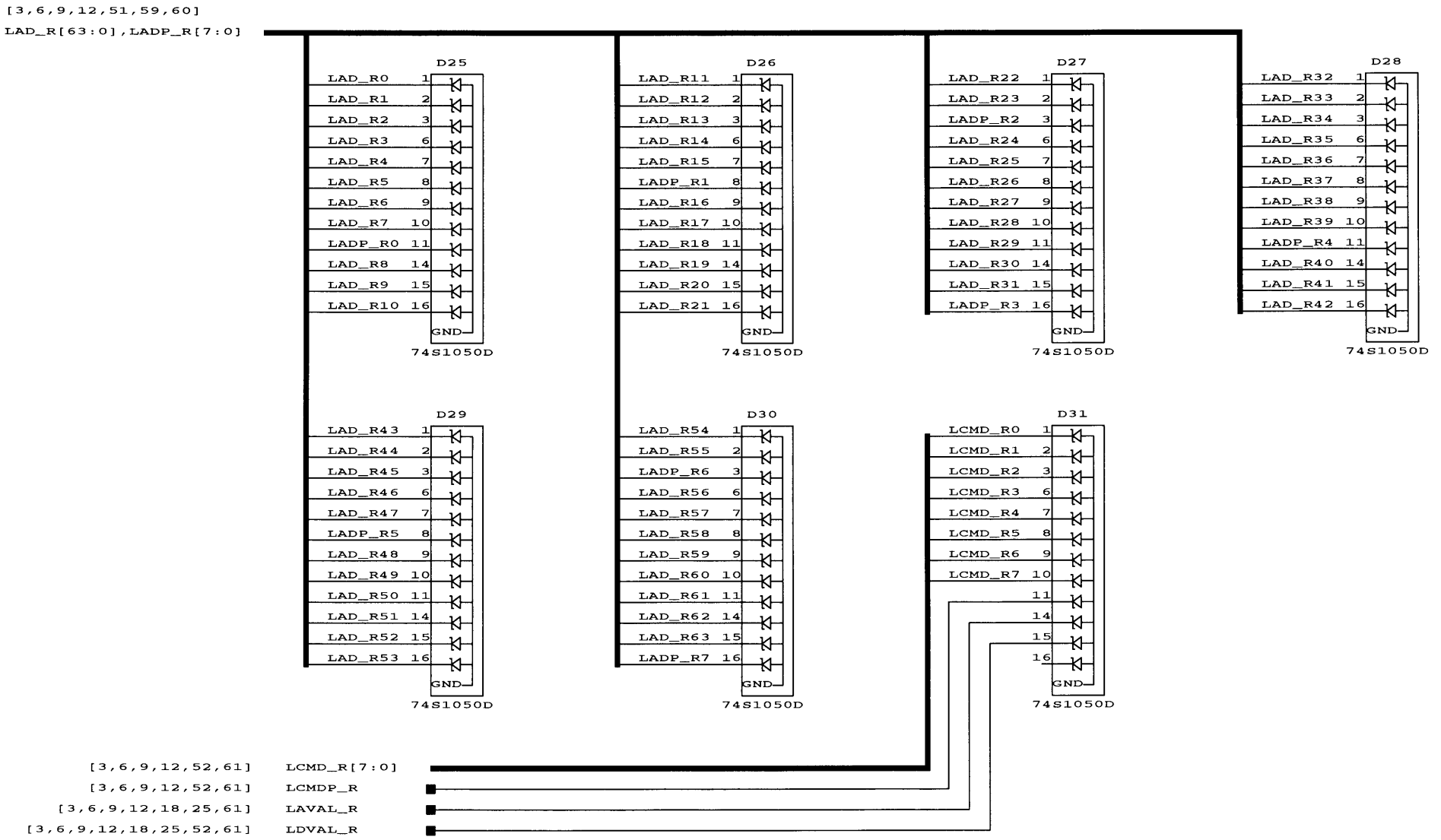
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connector (row 51-75)	
Issue 2			
Issue 3		File: cpu301	Page:66 of 73



dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Connector (row 76-100)	
Issue 2			
Issue 3		File: cpu301	Page:67 of 73

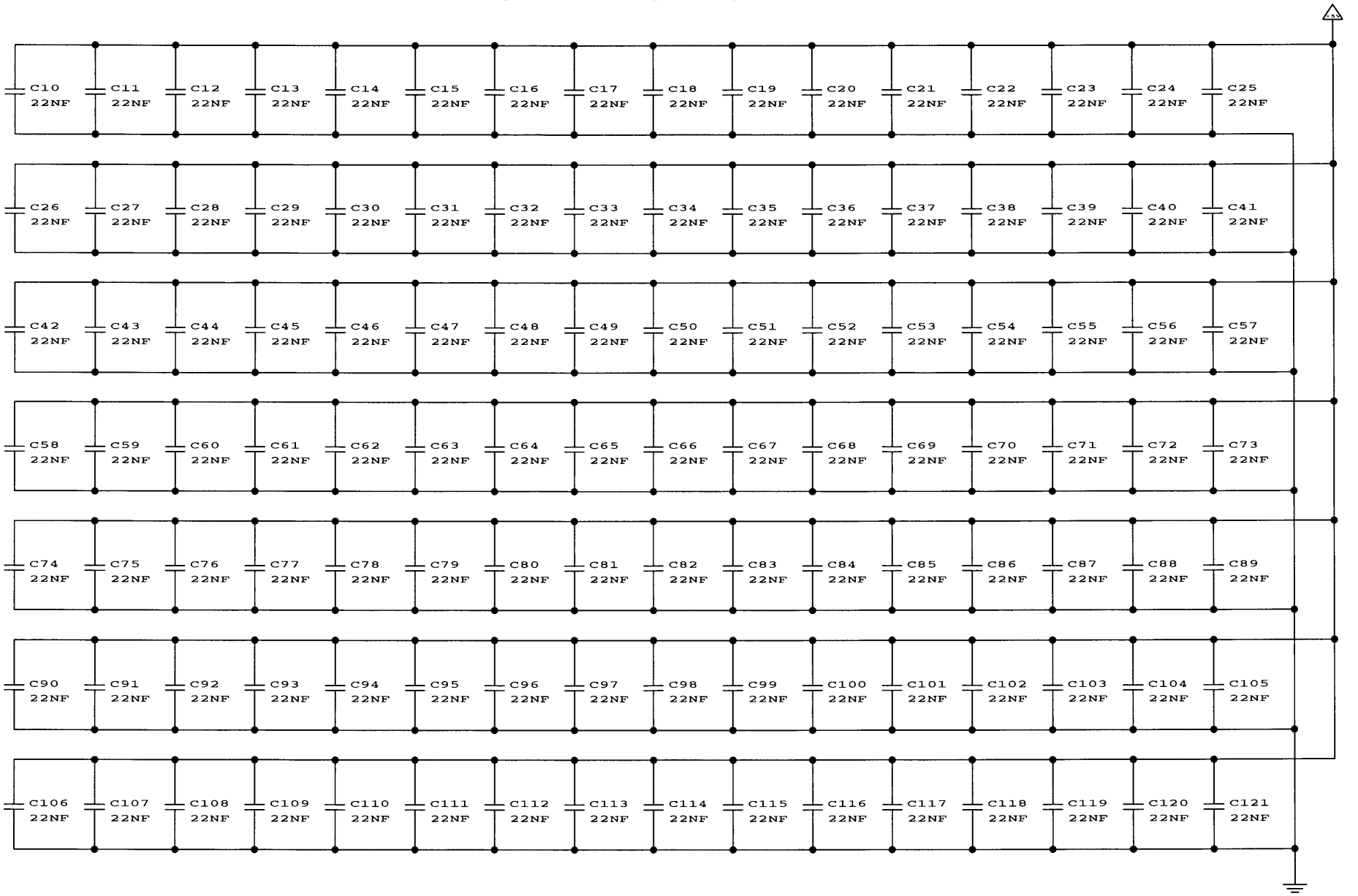


dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Internal global bus term.	
Issue 2			
Issue 3		File: cpu301	Page:68 of 73



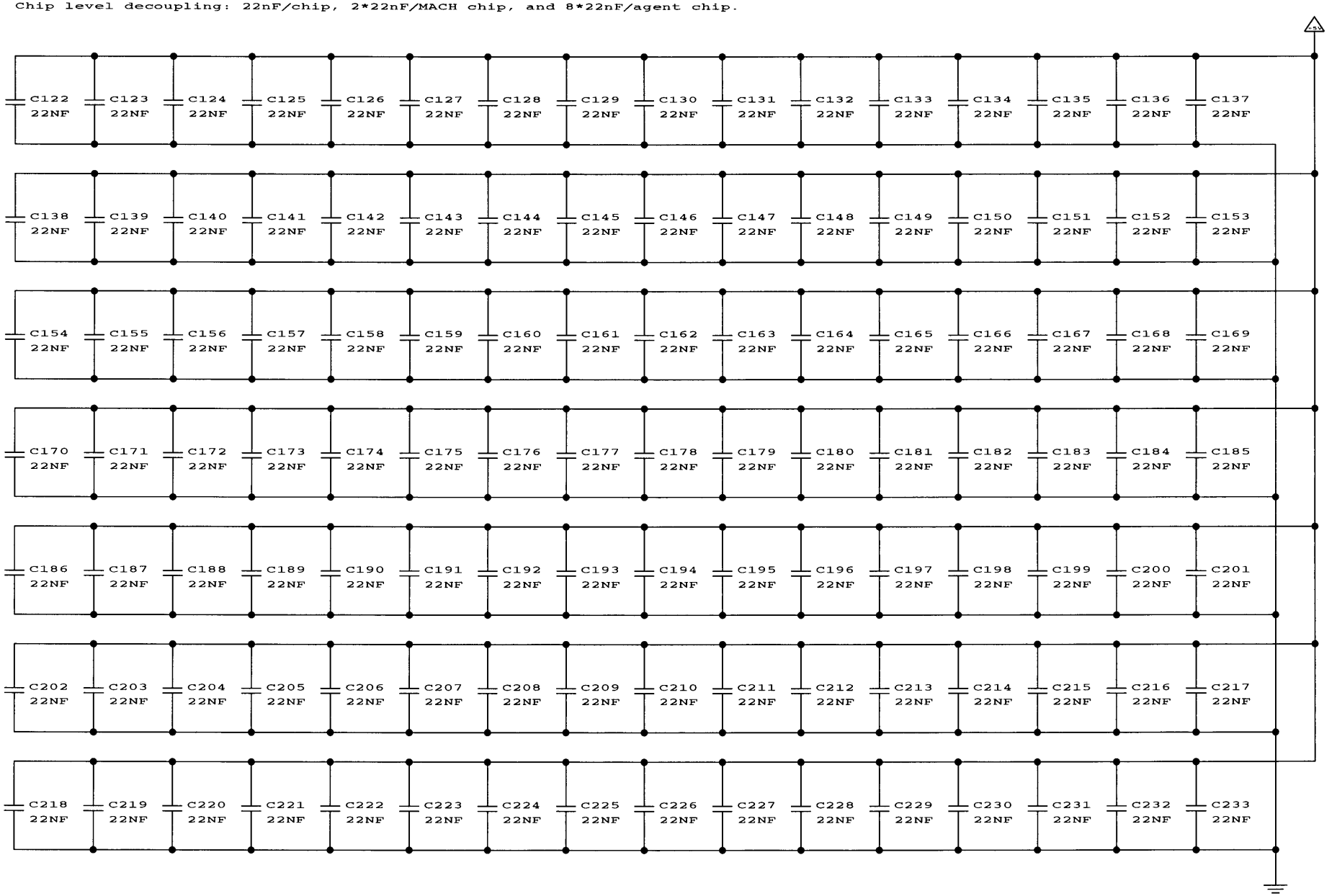
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Internal local bus term.	
Issue 2			
Issue 3		File: cpu301	Page:69 of 73

Chip level decoupling: 22nF/chip, 2*22nF/MACH chip, and 8*22nF/agent chip.



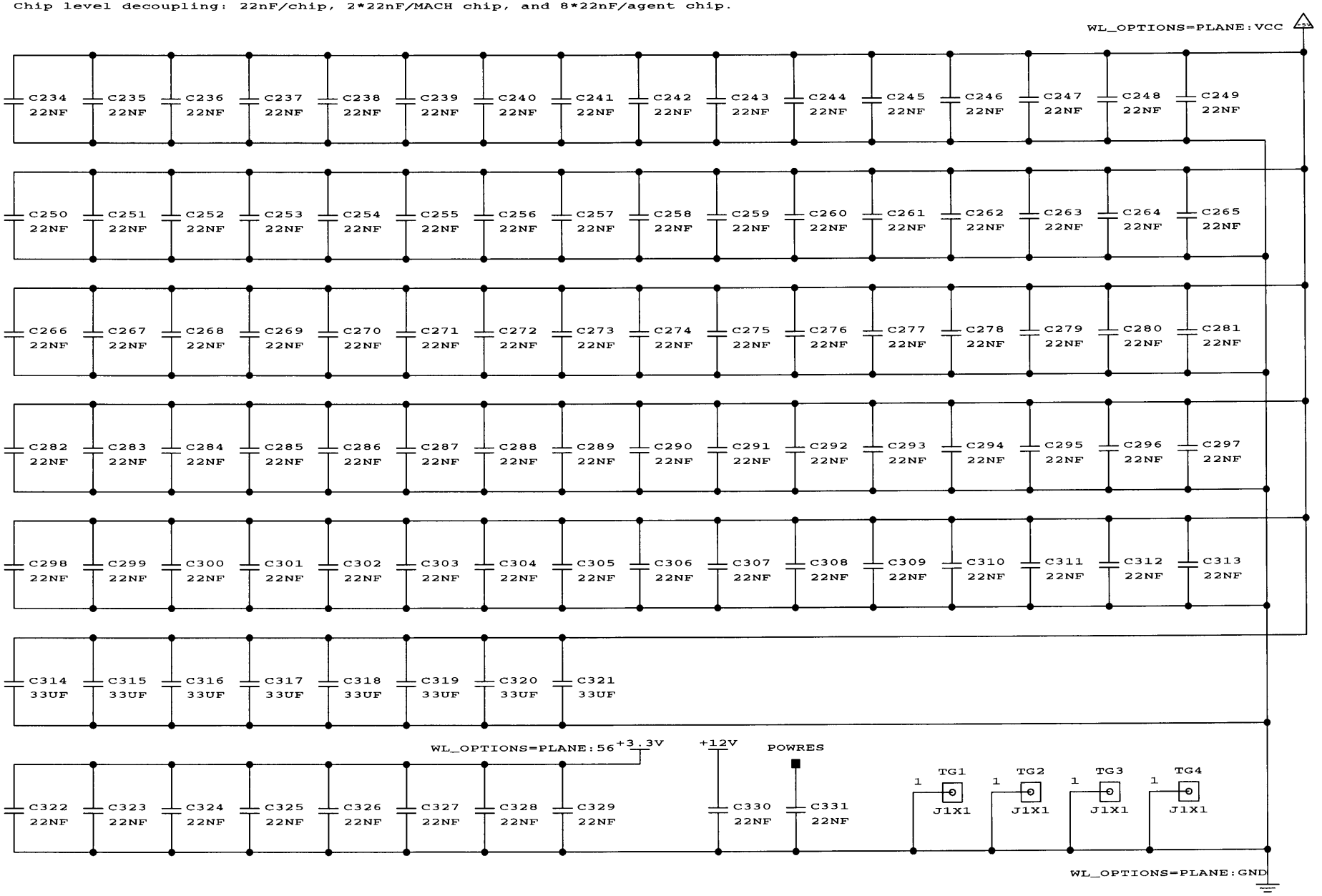
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Decoupling capacitors	
Issue 2			
Issue 3		File: cpu301	Page:70 of 73

Chip level decoupling: 22nF/chip, 2*22nF/MACH chip, and 8*22nF/agent chip.



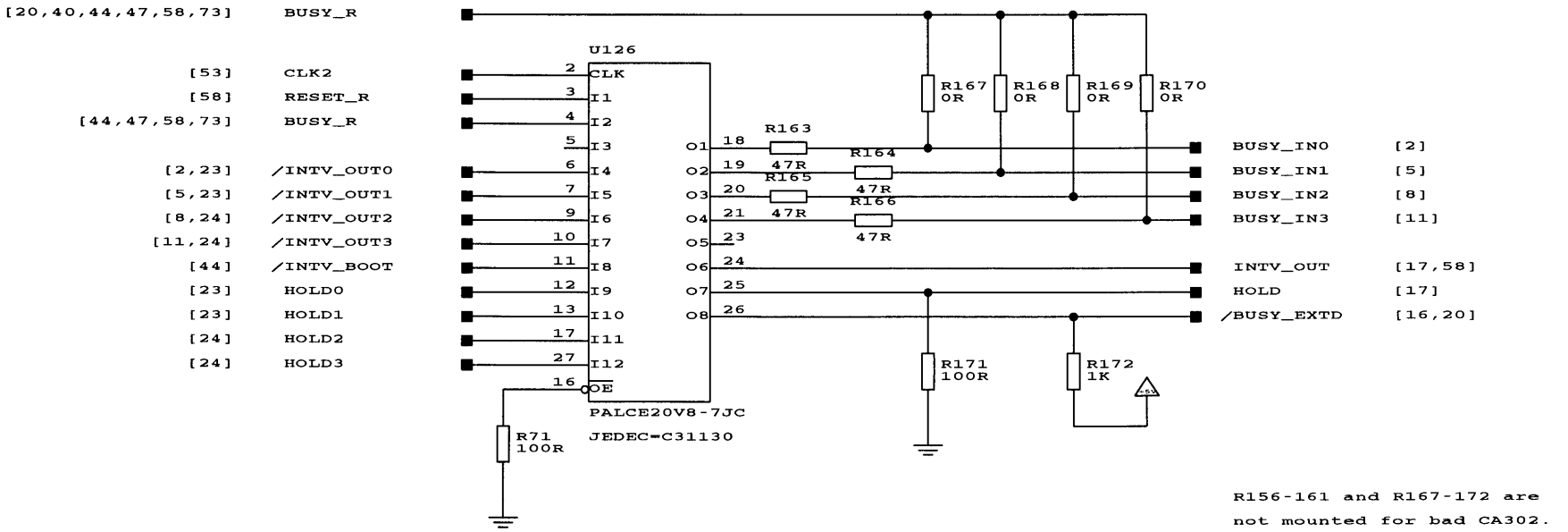
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Decoupling capacitors	
Issue 2			
Issue 3		File: cpu301	Page:71 of 73

Chip level decoupling: 22nF/chip, 2*22nF/MACH chip, and 8*22nF/agent chip.

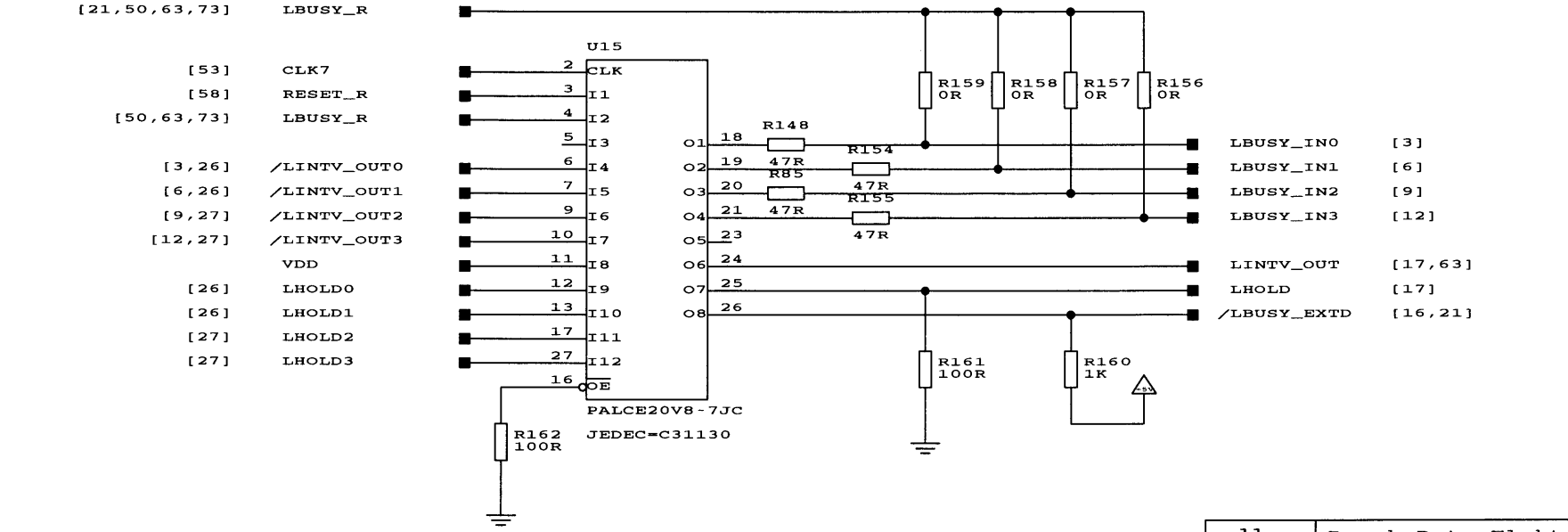


Decoupling at bus connector: 22nF for 3.3 V, 12 V, POWRES and 33uF for 5 V.

dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Decoupling capacitors	
Issue 2			
Issue 3		File: cpu301	Page:72 of 73



R156-161 and R167-172 are not mounted for bad CA302.



dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1	950131	Controlled intervention	
Issue 2		for bad CA302	
Issue 3		File: cpu301	Page:73 of 73

PARTS LIST

Module: CPU300-1 Date: 950911 Page: 1/2

Part no	Device	Qty	Comp
99020850	22NF	315	C1,C10-313,C322-331
99020851	4.7UF	1	C2
99020849	33UF	8	C314-321
99021413	SSF-LXH1032ID	5	D1,D5,D9,D13,D17
99021412	SSF-LXH1032GD	4	D2,D6,D10,D14
99000227	74S1050D	7	D18-24
99022027	1.000MHZ	1	OSC1
99020305	100R	54	R1-5,R5A,R6-9,R15,R17,R19,R21 R23,R25,R27,R29,R31-32,R35 R38-39,R41,R45,R60,R65,R68,R71 R108-109,R112-113,R116-117 R120-121,R124-125,R128-129 R132-133,R136-137,R139,R141 R143,R145,R147,R149,R151,R153 R162
99020307	82R	2	R10,R12
99020308	130R	2	R11,R13
99020306	220R	33	R14,R16,R18,R20,R22,R24,R26,R28 R30,R106-107,R110-111, R114-115,R118-119,R122-123, R126-127,R130-131,R134-135, R138,R140,R142,R144,R146, 148,R150,R152
99020303	4K7	7	R33,R42,R66-67,R69-70,R92
99020327	3K	2	R34,R43
99020301	1K	14	R40,R44,R50,R52,R54,R56, R62-64,R86-90
99020309	560R	17	R46-48,R72-84,R91
99020325	47R	8	R85,R148,R154-155,R163-166
99020322	0R	8	R51,R55,R58-59,R95,R98,R101, R104
99022235	Netw. 4820P-002-472	1	R36
99022234	Netw. 4820P-002-102	1	R93
99011701	CA302	4	U1,U3,U5,U7
99002411	74F1808D	2	U9,U11
99002412	74F1832D	2	U10,U12
99000831	74AS20D	1	U13
99010804	PALCE20V8-7JC	1	U126
99002413	74F377D	1	U17
99010404	PAL22V10-7JC	1	U18
99010216	PAL20R8-5JC	1	U21
99010902	MACH110-20JC	3	U20,U78,U85
99010904	MACH210-12JC	4	U22,U138-139,U141
99002222	74FCT16823BTPV	6	U26-27,U81-84
99011223	MCM6706AJ10	10	U28-29,U33-34,U38-39,U43-44, U140,U142
99002223	74FCT16244ATPV	5	U30,U35,U40,U45,U77
99002221	74FCT521BTSO	9	U31-32,U36-37,U41-42,U46-47, U70
99010908	MACH220-15JC	1	U71
99012095	N82S123AA / Am27S19AJC	2	U72-73
99002219	74FCT16501ATPV	1	U74
99002408	74F280BD	3	U75-76,U80
99012114	AM29C040-120JC	1	U79
99010604	PALCE16V8H-7JC	2	U86-87
99011218	CY7B991-7JC	1	U96
99005033	MC100H641FN	1	U97
99002500	FB2031BB	10	U98-107

PARTS LIST

Module: CPU300-1 Date: 950911 Page: 2/2

Part no	Device	Qty	Comp
99002501	FB2033BB	4	U108-110,U123
99001040	74ALS240D	2	U124-125
99000472	74LS393D	3	U127-129
99002405	74F74D	2	U130-131
99000832	74AS30D	2	U133,U150
99010022	PAL16R6-5JC	1	U136
99002407	74F244D	1	U148
99000830	74AS1004D	1	U149
99040124	3M8062011549-5	16	X00-03,X10-13,X20-23,X30-33
99040111	AMP100147-1	3	X101-102,X104
99040110	AMP100145-1	1	X103
99023228	20-pin PLCC socket	5	U72-73,U86-87,U136
99023229	28-pin PLCC socket	3	U18,U21,U126
99023230	32-pin PLCC socket	1	U79
99023231	44-pin PLCC socket	7	U20,U22,U78,U85, U138-139,U141
99023232	68-pin PLCC socket	1	U71
99030350	PCB CPU301 Issue 2	1	
99068013	Front panel CPU300	1	
	Mech. parts CPU30x	1	

PARTS LIST

Module: CPU301-1 Date: 950911 Page: 1/2

Part no	Device	Qty	Comp
99020850	22NF	315	C1,C10-313,C322-331
99020851	4.7UF	1	C2
99020849	33UF	8	C314-321
99021413	SSF-LXH1032ID	5	D1,D5,D9,D13,D17
99021412	SSF-LXH1032GD	12	D2-4,D6-8,D10-12,D14-16
99000227	74S1050D	14	D18-31
99022027	1.000MHZ	1	OSC1
99020305	100R	54	R1-5,R5A,R6-9,R15,R17,R19,R21 R23,R25,R27,R29,R31-32,R35 R38-39,R41,R45,R60,R65,R68,R71 R108-109,R112-113,R116-117 R120-121,R124-125,R128-129 R132-133,R136-137,R139,R141 R143,R145,R147,R149,R151,R153 R162
99020307	82R	2	R10,R12
99020308	130R	2	R11,R13
99020306	220R	33	R14,R16,R18,R20,R22,R24,R26,R28 R30,R106-107,R110-111, R114-115,R118-119,R122-123, R126-127,R130-131,R134-135, R138,R140,R142,R144,R146, 148,R150,R152
99020303	4K7	7	R33,R42,R66-67,R69-70,R92
99020327	3K	2	R34,R43
99020301	1K	14	R40,R44,R50,R52,R54,R56, R62-64,R86-90
99020309	560R	17	R46-48,R72-84,R91
99020325	47R	8	R85,R148,R154-155,R163-166
99020322	0R	8	R51,R55,R58-59,R95,R98,R101, R104
99022235	Netw. 4820P-002-472	1	R36
99022234	Netw. 4820P-002-102	1	R93
99011701	CA302	8	U1-8
99002411	74F1808D	2	U9,U11
99002412	74F1832D	2	U10,U12
99000831	74AS20D	2	U13-14
99010804	PALCE20V8-7JC	2	U15,U126
99002413	74F377D	2	U17,U25
99010404	PAL22V10-7JC	2	U18-19
99010216	PAL20R8-5JC	2	U21,U23
99010902	MACH110-20JC	4	U20,U78,U85,U94
99010904	MACH210-12JC	8	U22,U24,U138-139,U141,U143-144 U146
99002222	74FCT16823BTPV	8	U26-27,U48-49,U81-84
99011223	MCM6706AJ10	20	U28-29,U33-34,U38-39,U43-44 U50-51,U55-56,U60-61,U65-66 U140,U142,U145,U147
99002223	74FCT16244ATPV	14	U30,U35,U40,U45,U52,U57,U62,U67 U77,U89-93
99002221	74FCT521BTSO	18	U31-32,U36-37,U41-42,U46-47 U53-54,U58-59,U63-64,U68-70,U88
99010908	MACH220-15JC	1	U71
99012095	N82S123AA / Am27S19AJC	2	U72-73
99002219	74FCT16501ATPV	1	U74
99002408	74F280BD	3	U75-76,U80
99012114	AM29C040-120JC	1	U79
99010604	PALCE16V8H-7JC	3	U86-87,U95

PARTS LIST

Module: CPU301-1 Date: 950911 Page: 2/2

Part no	Device	Qty	Comp
99011218	CY7B991-7JC	1	U96
99005033	MC100H641FN	1	U97
99002500	FB2031BB	20	U98-107,U111-120
99002501	FB2033BB	6	U108-110,U121-123
99001040	74ALS240D	2	U124-125
99000472	74LS393D	3	U127-129
99002405	74F74D	2	U130-131
99000832	74AS30D	4	U133-134,U150-151
99010022	PAL16R6-5JC	2	U136-137
99002407	74F244D	1	U148
99000830	74AS1004D	1	U149
99040124	3M8062011549-5	16	X00-03,X10-13,X20-23,X30-33
99040111	AMP100147-1	3	X101-102,X104
99040110	AMP100145-1	1	X103
99023228	20-pin PLCC socket	7	U72-73,U86-87,U95,U136-137
99023229	28-pin PLCC socket	6	U15,U18-19,U21,U23,U126
99023230	32-pin PLCC socket	1	U79
99023231	44-pin PLCC socket	12	U20,U22,U24,U78,U85,U94, U138-139,U141,U143-144,U146
99023232	68-pin PLCC socket	1	U71
99030350	PCB CPU301 Issue 2	1	
99068005	Front panel CPU301	1	
	Mech. parts CPU30x	1	

PLD list

Part no: 99750023 **Module:** CPU300-1 **Pcb no:**
Status: Preliminary **Date:** 950817 **Page:** 1 / 1
Init: OHM

Label	Pos.	Part no.	Type	X-pgm.	File	Checksum
c31011	U18	99010404	PAL22V10-7JC		c31011.jed	5623
c31022	U136	99010022	PAL16R6-5JC		c31022.jed	3ED4
c31030	U20	99010902	MACH110-20JC		c31030.jed	B930
c31041	U21	99010216	PAL20R8-5JC		c31041.jed	6BC4
c31051	U22	99010904	MACH210-12JC		c31051.jed	88BD
c31061	U138	99010904	MACH210-12JC		c31061.jed	807D
c31071	U139	99010904	MACH210-12JC		c31071.jed	C79D
c31071	U141	99010904	MACH210-12JC		c31071.jed	C79D
c31080	U71	99010908	MACH220-15JC		c31080.jed	004F
c31090	U78	99010902	MACH110-20JC		c31090.jed	E876
c31100	U85	99010902	MACH110-20JC		c31100.jed	604D
c31110	U86	99010604	PALCE16V8H-7JC	R6	c31110.jed	234F
c31120	U87	99010604	PALCE16V8H-7JC	R8	c31120.jed	2470
c31130	U126	99010804	PALCE20V8H-7JC		c31130.jed	7914

PLD list

Part no: 99750020 **Module:** CPU301-1 **Pcb no:**
Status: Preliminary **Date:** 950817 **Page:** 1 / 1
Init: OHM

Label	Pos.	Part no.	Type	X-pgm.	File	Checksum
c31011	U18	99010404	PAL22V10-7JC		c31011.jed	5623
c31011	U19	99010404	PAL22V10-7JC		c31011.jed	5623
c31022	U136	99010022	PAL16R6-5JC		c31022.jed	3ED4
c31022	U137	99010022	PAL16R6-5JC		c31022.jed	3ED4
c31030	U20	99010902	MACH110-20JC		c31030.jed	B930
c31041	U21	99010216	PAL20R8-5JC		c31041.jed	6BC4
c31041	U23	99010216	PAL20R8-5JC		c31041.jed	6BC4
c31051	U22	99010904	MACH210-12JC		c31051.jed	88BD
c31051	U24	99010904	MACH210-12JC		c31051.jed	88BD
c31061	U138	99010904	MACH210-12JC		c31061.jed	807D
c31061	U143	99010904	MACH210-12JC		c31061.jed	807D
c31071	U139	99010904	MACH210-12JC		c31071.jed	C79D
c31071	U141	99010904	MACH210-12JC		c31071.jed	C79D
c31071	U144	99010904	MACH210-12JC		c31071.jed	C79D
c31071	U146	99010904	MACH210-12JC		c31071.jed	C79D
c31080	U71	99010908	MACH220-15JC		c31080.jed	004F
c31090	U78	99010902	MACH110-20JC		c31090.jed	E876
c31100	U85	99010902	MACH110-20JC		c31100.jed	604D
c31100	U94	99010902	MACH110-20JC		c31100.jed	604D
c31110	U86	99010604	PALCE16V8H-7JC	R6	c31110.jed	234F
c31110	U95	99010604	PALCE16V8H-7JC	R6	c31110.jed	234F
c31120	U87	99010604	PALCE16V8H-7JC	R8	c31120.jed	2470
c31130	U126	99010804	PALCE20V8H-7JC		c31130.jed	7914
c31130	U15	99010804	PALCE20V8H-7JC		c31130.jed	7914

Supermax Field Change Notice no. 149

Module:	CPU300-1 and CPU301-1 CPU module
Date:	95.11.20 (Revision 1)

Editorial change:

This FCN149 replaces the earlier FCN149 dated 95.09.01. The latter refers to the position of the FCN PROM as U72, which correctly should be U73. The device is still **FCN149**.

Category:

- Production change.
- Mandatory field change.

Corrects the error:

The module hitherto has been unable to operate at a bus frequency of 33.3 MHz. In addition, the module name on the front panel may be wrong.

Needed tools:

Hand tools.

Supermax FCN149-kit, stock number 95101490, consisting of:

- One PAL device labelled **C31022**.
- Five PAL labels **C31051**, **C31061**, 2x **C31071**, and **C31130**.
- Front panel marked **CPU300**.
- One PROM device labelled **FCN149**.

Description:

- U136: PAL **X31021** -> **C31022**.
- U22: PAL label **X31051** -> **C31051**.
- U138: PAL label **X31061** -> **C31061**.
- U139: PAL label **X31071** -> **C31071**.
- U141: PAL label **X31071** -> **C31071**.
- U126: PAL label **X31130** -> **C31130**.

- U96: Connect CY7B991 pin 4 and 32 (GND) together. Pin 1 is marked by an indented dot.
- U96: Connect CY7B991 pin 6 and 13 (via-hole, GND) together.
- R60: Remove the resistor located in the center of the connector side.
- If the module ID PROM claims that the module is a CPU300 then change the module front panel and return the old to the factory.
- Finally, replace the FCN PROM in U73 with the new **FCN149**.

Circuits involved:

Due to the idiosyncrasies of the ISO9000 requirements I shall reiterate the circuits involved:

- U136, U22, U138, U139, U141, U126: PAL
- U96: CY7B991
- R60: Resistor
- U73: PROM

Previous FCN:

None.

PRODUCTION CHANGE NOTICE

PCN NO:	95-5 (revision 1)
Date:	November 23, 1995
FCN:	149
Author:	OHM
Module:	CPU300-1 and CPU301-1 CPU module
Part No:	99750023 and 99750020
Introduced from:	TBD by Production

Editorial change:

This PCN 95-5 replaces the earlier PCN 95-5 dated August 25, 1995. The latter refers to the position of the FCN PROM as U72, which correctly should be U73. Further, a reference to the PCN 95-7 is deleted.

Reasons for change:

With this change the module will be capable of operating at a bus frequency of 33.3 MHz. This PCN is thus a prerequisite for PCN 95-6. In addition, the module name on the front panel may be wrong.

Description of change:

U136: PAL x31021 -> c31022.
U22: PAL label x31051 -> c31051.
U138: PAL label x31061 -> c31061.
U139: PAL label x31071 -> c31071.
U141: PAL label x31071 -> c31071.
U126: PAL label x31130 -> c31130.
U96: Connect pin 4 and 32 (GND) together.
U96: Connect pin 6 and 13 (via-hole, GND) together.
R60: Remove it.

If the module ID PROM claims that the module is a CPU300 then change the front panel accordingly.

Finally, replace the FCN PROM in U73 with the new FCN149.

Stock:

All modules must be modified.

Enclosures:

Field change notice no. 149.