

# CPU301/302 Design document

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Author:	ohm
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## 1 REVISION HISTORY

### Changes from version 1.0 to 1.1:

The reference list has been updated.

The LED labels have been changed.

### Version 1.0:

Although this is the initial version of the document it is based on the MCU301 Design document from which it differs in the following respects:

The local bus has been changed to all BTL, thus the global and local bus are symmetrical.

All processor modules on a base module must have the same secondary cache size, thus reducing the number of sets of snooper address jumpers from two to one.

The CPU301 and CPU302 support 1-MB and 4-MB secondary cache, respectively, thus the above set of jumpers is fixed for each module.

The boot PROM is a flash EEPROM for re-use.

## 2 REFERENCES

1. MCU301/302/304 Kravspecifikation  
1-0101
2. SPC/3 System bus specification  
1-0201
3. MIPS R4000 Microprocessor User's Manual  
Integrated Device Technology, Inc.  
Part number M8-00040
4. MIPS R4000 Microprocessor User's Manual Errata  
Revision 2.0  
March 13, 1992  
MIPS Technology Products Group
5. CPU Agent Design document  
1-0203

### 3 INTRODUCTION

The CPU module for the SPC/3 computer series consists of a base module CPU301/302 and one to four detachable processor modules, e.g. PMD301 with a 75-MHz R4400MC and 1-MB secondary cache. CPU301 and CPU302 support 1-MB and 4-MB secondary caches, respectively. The base module takes up one backplane position.

Each of the up to four processors modules connects to a global and a local bus interface through two agents. These identical agents, which are implemented with highly complex gate arrays, provide data buffers, address registers, and control for the commands that originate in the associated processor and for those commands on the associated bus that require cache coherency.

Both the global and local bus interface are BTL.

There is a global control space, which may be accessed by all processors and from the global bus, and contains the following special registers intended for identification, control, error logging, interrupt, and debugging. There are a control, interrupt, and debug register for each subposition corresponding to each possible processor module.

- Status register
- Control register
- Module ID
- Module FCN
- Interrupt register
- Debug register
- Processor module identification register
- Bus error register

Similarly, there is a local control space, which, however, only provides Interrupt registers.

In addition to the control spaces there are separate address spaces for the internal registers of each agent, these may only be accessed by the associated processor.

The module is equipped with a 1/2-MB detachable boot flash EEPROM, which is common to all processors.

Finally, the choice of little or big endians is made by a fixed signal on the bus.

## 4 SPECIFICATIONS

### 4.1 Performance

Bus frequency	33.3 MHz
Bus burst rate	267 MB/s
Bus read rate (32 words)	178 MB/s
Bus write rate (32 words)	213 MB/s

### 4.2 Secondary cache requirements

Block size	32 words
Cache size, CPU301	1 MB
Cache size, CPU302	4 MB

### 4.3 Interfaces

System bus interface:

SPC/3 system bus [2], both global and local bus.

Indicators on front panel:

PARITY ERROR	Red LED that indicates a parity error on the global or local bus.
ERROR(0-3)	One red programmable LED per processor.
BUSY(0-3)	One green programmable LED per processor.
A(0-3)	One green programmable LED per processor.
B(0-3)	One green programmable LED per processor.

Internal processor/base module interface:

SAD(63:0)	System interface address/data
SADP(7:0)	System interface address/data parity
SCMD(8:0)	System interface command
SCMDP	System interface command parity
/VALIN	System interface valid to processor
/VALOUT	System interface valid from processor
/EXTRQ	System interface request from agents
/RELEASE	System interface release from processor
/RDRDY	Read ready
/WRRDY	Write ready
/IVDACK	Invalidate acknowledge
/IVDERR	Invalidate error
RCLK(1:0)	Receive clocks (identical)
TCLK(1:0)	Transmit clocks (identical)
/INT	Error interrupt
/NMI	Non-maskable interrupt

SRE	Selective reset
C2MS	2-ms period clock
C262MS	262-ms period clock
PM_ID(3:0)	Processor module identification
/PRESENT	Processor module present
BIG	Big endian

#### 4.4 Dimensions

Board height	415.0 mm
Board depth	335.0 mm
Module pitch	30.0 mm

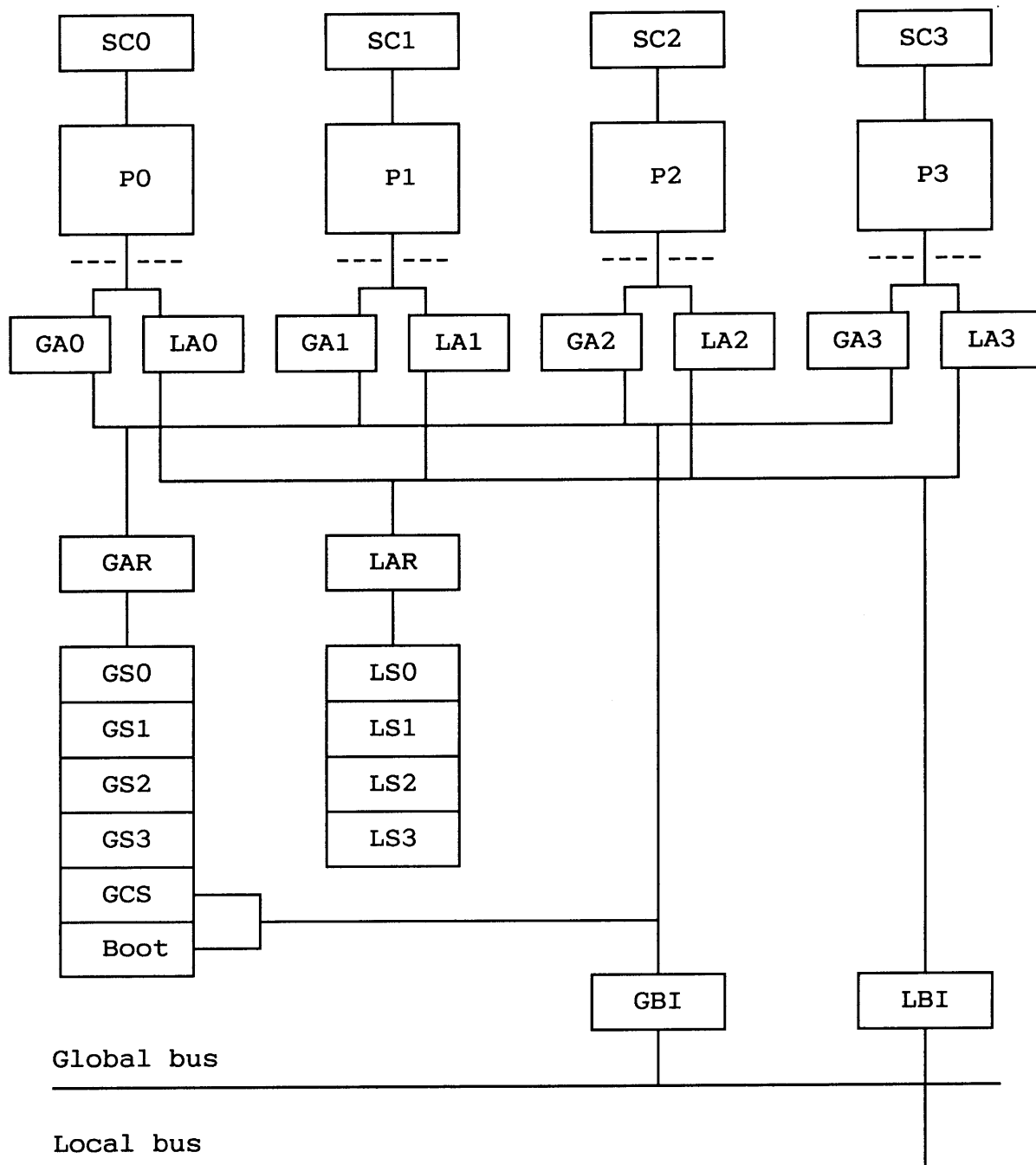
#### 4.5 Power

Voltage	5 V $\pm$ 5 %
Current	9 A max.

**5 Functional description**

The block diagram below shows the base module CPU301/302 below the connector interface (---) and four processor modules above.

Each processor module consists of a processor (P) with a secondary cache (SC) and a connector. Associated with each possible processing module, but placed on the base module are a global and a local agent (GA and LA), and a global and a local snooper (GS and LS). In addition, the base module provides a global and a local bus interface (GBI and LBI) with associated address registers (GAR and LAR), a global control spaces (GCS), and finally a boot PROM. A part of the global control space and all of the local control space are inside the respective agents.



## 5.1 Base module

The main components of the base module are eight agents, two bus interfaces, two address registers, eight snoopers, a global control space, and a boot PROM.

The agent is described in [5] and contains all data buffers, data and address registers, and control required to link a processor to a bus interface. An agent also contains an agent space, which is only accessible from the associated processor, and an interrupt register and a debug register, which are a part of the respective control spaces.

One of the important tasks of the agent is to sequence transactions from the processor and system bus correctly when they pertain the same cache line. Another is to ensure continued snooping on a retained link address, when the link is evicted from the secondary cache and retained by the processor, whereby the link address is evicted from the snoopers and therefore must be retained in the agent.

Each bus interface contains a number of registered transceivers and a bus master control including arbitration control. The global bus interface is BTL, while the local bus interface is TTL except for the control signals which are BTL.

The task of a snoopers is to keep a copy of the physical address tags of the secondary cache tags such that bus snooping can take place without disturbing the respective processor excessively. The format of the snoopers depends on the size and block size of the secondary cache:

1-MB:	35	20 19
4-MB:	35	22 21

Tag	Index	Offset
-----	-------	--------

8-word:	5 4	0
16-word:	6 5	0
32-word:	7 6	0

The index gives the entry in the snoopers, and, in order for a snoop hit to occur, the tag must match the corresponding bits of the bus address. The offset does not participate in the comparison, and there is no valid bit. The contents of the snoopers are undefined upon reset.

The format of the snoopers, which must correspond to the associated secondary caches, is selected with fixed jumpers given a limit of 15 index bits corresponding to a maximum set size of 32768 entries. Surplus tag bits need not be excluded as they merely become redundant. The CPU301 module is set for 1-MB / 32-word, while the CPU302 is set for 4-MB / 32-word.

When a cache line is replaced the read and the write are normally bundled together in a command called read with write forthcoming. In this case the write address tag will disappear from the snoopers before disappearing from the secondary cache as it is overwritten in the snoopers by that of the read, thus creating the possibility of non-coherency. Rather than try to juggle with both tags, the snoopers must force hit until the start of the next command from the

agent, which is a late but safe indication that the write address tag no longer is present in the secondary cache.

In addition to each snooper, which already does a good job of filtering coherency requests to the processor, there is an extension dubbed the supersnooper, which to the extent possible tracks the state changes in the secondary cache and prevents non-exclusive coherent read requests from reaching the processor if the state is shared or invalid. The contents of the supersnoopers are undefined upon reset.

The global control space contains a number of special registers as mentioned in the introduction. The control for the control space includes an address comparator that can detect a control space access to this module and a simple state machine that can perform the required access. The module FCN PROM is mounted in a socket to allow easy replacement.

There is a 1/2-MB boot PROM providing reset, diagnostic, and debugging code. The boot PROM is located at the beginning of the address range 0x01FC0000 through 0x01FFFFFF, where the former is the physical reset address of the processor. This address range is, alas, right in the memory space. Thus, when a read address falls in this range and the boot PROM is not mapped out, as controlled by a bit in the control register of the global agent, the boot PROM must intervene and supply the data as a cache slave thus pre-empting the memory slave. The boot PROM, which is implemented with a 512 K by 8-bit flash EEPROM, is mounted in a socket.

When a master issues an access with an address for which there is no matching slave a missing target acknowledge will result. This works fine for a write, but for a read the responsible processor would wait forever on the missing 'last data element' because the agent does not provide it instead. Therefore, a dummy block generator is implemented in each bus interface to take care of this case.



## 6 PROGRAMMING INFORMATION

### 6.1 Processor

Programming information for the processor can be found in [3, 4].

The physical address space as seen from a processor consists of a global and local space, each subdivided into a memory, agent, and control space. A processor can only access its own agent spaces, while the memory and control spaces are accessible by all processors on the bus in question. The global and local control address spaces are described below. All address formats are shown in [2].

The interrupt register of the processor, whose format is shown below, contains a non-maskable interrupt (NMI), four general interrupts (I5-I2), a timer interrupt (TIM), and an error interrupt (ERR).

NMI	I5	I4	I3	I2	TIM	ERR
6	5	4	3	2	1	0

These bits result from the OR'ing of the respective bits in the two agents, and, in case of bit 0, also from the OR'ing of the bits in the Bus error register, more specifically the global and local bus parity error interrupts, and the debug interrupt. Only the timer in the global agent is active.

All interrupts are level-sensitive, thus the processor must remove an interrupt when it is accepted, but in order to do so the source of the interrupt must be known. This is a problem for the general interrupts unless each in software is assigned to only one agent, thus the use of local interrupts is discouraged.

Accesses to the address space 0x01FC0000 through 0x01FFFFFF may, under control of a bit in the control register of the appropriate global agent, be directed at either memory or the 1/2-MB boot PROM, which is located at the start of the address space and contains reset, diagnostic, and debugging code.

The selection of little or big endians is determined by a fixed signal on the system bus.

The states of the snoopers and supersnoopers are, like those of the secondary caches, undefined upon reset.

### 6.2 Agent space

For a description of the agent address space, please, refer to [5].

There are four programmable LEDs labelled ERROR(0-3), BUSY(0-3), A(0-3), and B(0-3) on the front panel for each of the four possible processor modules. They are controlled by the associated global agent control register bit 6 and 7, and local agent control register bit 6 and 7, respectively.

### 6.3 Control space

The CPU module has a global and a local control space, which are both divided into subpositions and contain a number of special registers intended for identification, configuration, error logging, interrupt, and debug. These registers have varying bit widths, but are all right justified within double words (64 bits), and any access less than a double word must take into account the subtle differences between little and big endians.

The global control space comprises all of the following special registers, while the local control space only comprises the interrupt register. Below is for every register or group of registers listed whether it can be read, written, or cleared along with its hexadecimal byte offset relative to the start of the control address space of the module.

Register	Access	Offset
Status register	Read/clear	0
Control register	Write	100
Module ID	Read	200
Module FCN	Read	300
Interrupt register	Write	400
Debug register	Write	500
Processor module register	Read	600
Bus error register	Read/clear	700

The function and format of the individual registers are described in the following. Reserved bits (r) must be 0 when written, and are undefined when read. Bits 16 through 63 are reserved, unless otherwise noted.

### 6.4 Status register

The Status register indicates bus parity errors found by this module. Individual bits may be cleared by writing ones in the respective positions, and the bits are all cleared by bus reset.

r	r	r	r	r	r	r	r	r	r	r	r	r	r	LPE	GPE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

GPE: Global parity error.

LPE: Local parity error.

### 6.5 Control register

There is a Control register for every subposition, and each contains a bit for selective reset of the corresponding processor. The bits are all set by bus reset.

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	SRE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SRE: Selective reset.

### 6.6 Module ID

The Module ID consists of a 32-byte string stored in 32 consecutive double words. The byte offset given earlier applies to the first double word.

r	r	r	r	r	r	r	r	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ID(7:0): Single byte of module Identification string.

The format of the string is given in [2].

### 6.7 Module FCN

The Module FCN consists of a 32-byte string stored in 32 consecutive double words. The byte offset given earlier applies to the first double word.

r	r	r	r	r	r	r	r	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FCN(7:0): Single byte of module Field Change Notice string.

The format of the string is given in [2].

### 6.8 Interrupt register

The Interrupt register, which is 32 bits wide, is used to write interrupts. There is an Interrupt register for every subposition in both the global and the local control space, and it is not possible for a master to write to its own register.

P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

r	r	r	r	r	r	r	r	r	NMI	I5	I4	I3	I2	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

I(5:2): Interrupts.  
 Provides a direct path to the corresponding bits of the Interrupt register of the

processor.

NMI: Non-maskable interrupt.  
 Provides a direct path to the NMI bit of the Interrupt register of the processor.

P(15:0): Peripheral interrupts.  
 New bits are OR'ed to old ones, and the bits may be cleared by the processor.

### 6.9 Debug register

The Debug register is used to write a double byte to a processor during debug. There is a Debug register for every subposition, and it is not possible for a master to write to its own register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

D(15:0): Debug data.

### 6.10 Processor module register

The Processor module register indicates the presence and identity of each processor module.

M33	M32	M31	M30	M23	M22	M21	M20	M13	M12	M11	M10	M03	M02	M01	M00
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Mi(3:0): Identity of module i.

No module is present in position i if Mi=15.

### 6.11 Bus error register

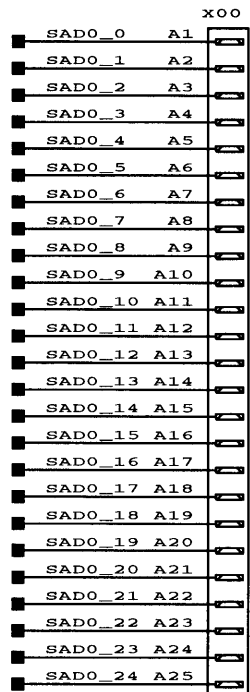
There is a Bus error register for every subposition, and each indicates interrupts caused by a bus parity error or a debug request. Individual bits may be cleared by writing ones in the respective positions, and the bits are all cleared by bus reset.

r	r	r	r	r	r	r	r	r	r	r	r	r	DBI	LPI	GPI
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

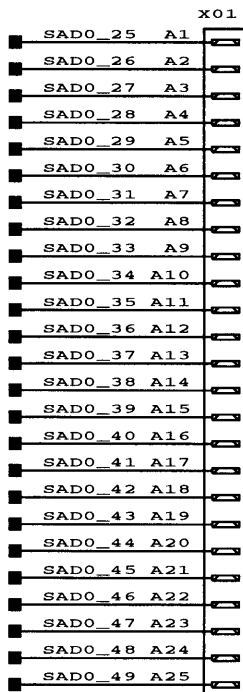
GPI: Global parity error interrupt.

LPI: Local parity error interrupt.

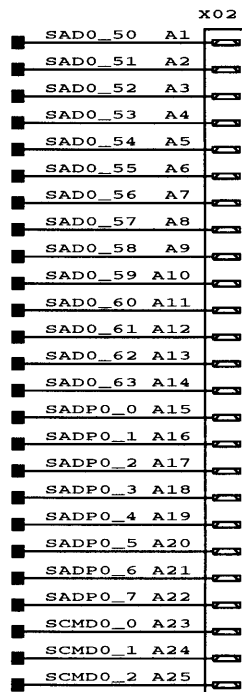
DBI: Debug interrupt.



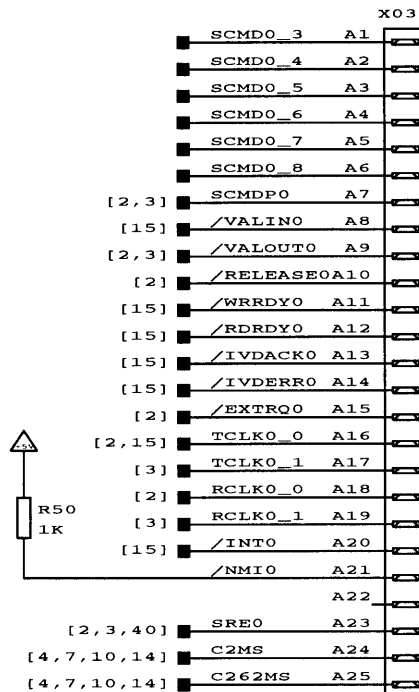
RNPAK2-25P



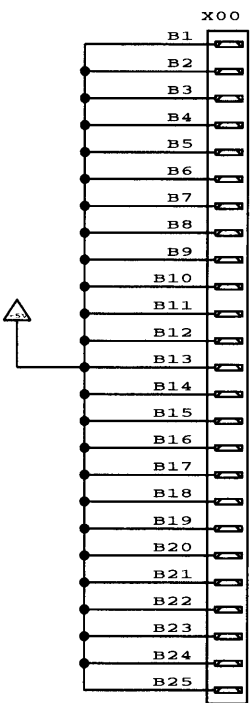
RNPAK2-25P



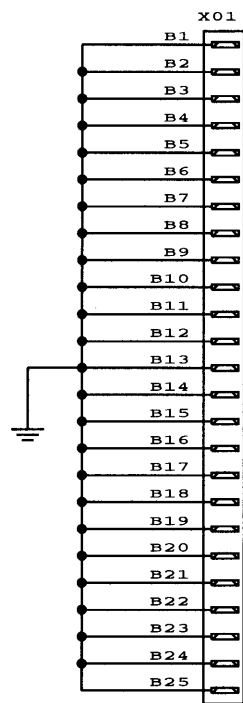
RNPAK2-25P



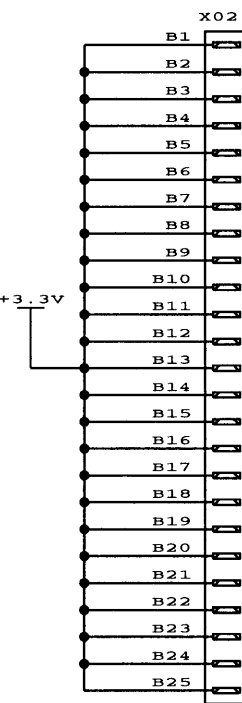
RNPAK2-25P



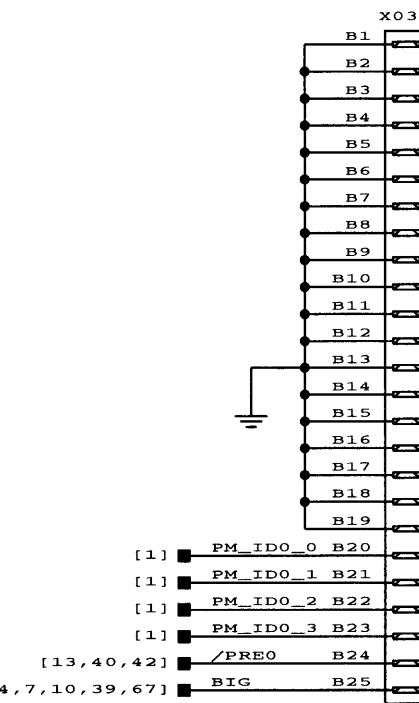
RNPAK2-25P



RNPAK2-25P



RNPAK2-25P



RNPAK2-25P

Dansk Data Elektronik A/S		
Issue 0	940811	CPU301 Module
Issue 1		Connectors 0
Issue 2		
Issue 3		File: cpu301 Page: 1 of 72

SADO\_[63:0]

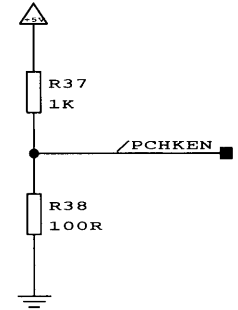
SADO_0	92	PAD0
SADO_1	93	PAD1
SADO_2	94	PAD2
SADO_3	95	PAD3
SADO_4	96	PAD4
SADO_5	98	PAD5
SADO_6	99	PAD6
SADO_7	100	PAD7
SADO_8	102	PAD8
SADO_9	103	PAD9
SADO_10	104	PAD10
SADO_11	105	PAD11
SADO_12	106	PAD12
SADO_13	107	PAD13
SADO_14	109	PAD14
SADO_15	110	PAD15
SADO_16	112	PAD16
SADO_17	113	PAD17
SADO_18	114	PAD18
SADO_19	115	PAD19
SADO_20	116	PAD20
SADO_21	117	PAD21
SADO_22	118	PAD22
SADO_23	120	PAD23
SADO_24	122	PAD24
SADO_25	123	PAD25
SADO_26	124	PAD26
SADO_27	125	PAD27
SADO_28	126	PAD28
SADO_29	127	PAD29
SADO_30	128	PAD30
SADO_31	129	PAD31
SADO_32	132	PAD32
SADO_33	133	PAD33
SADO_34	134	PAD34
SADO_35	135	PAD35
SADO_36	136	PAD36
SADO_37	137	PAD37
SADO_38	138	PAD38
SADO_39	139	PAD39
SADO_40	142	PAD40
SADO_41	143	PAD41
SADO_42	144	PAD42
SADO_43	145	PAD43
SADO_44	146	PAD44
SADO_45	147	PAD45
SADO_46	148	PAD46
SADO_47	149	PAD47
SADO_48	153	PAD48
SADO_49	155	PAD49
SADO_50	156	PAD50
SADO_51	157	PAD51
SADO_52	158	PAD52
SADO_53	159	PAD53
SADO_54	160	PAD54
SADO_55	161	PAD55
SADO_56	163	PAD56
SADO_57	164	PAD57
SADO_58	166	PAD58
SADO_59	167	PAD59
SADO_60	168	PAD60
SADO_61	169	PAD61
SADO_62	170	PAD62
SADO_63	171	PAD63

U1

BAD0	89	AD_R0
BAD1	88	AD_R1
BAD2	87	AD_R2
BAD3	86	AD_R3
BAD4	85	AD_R4
BAD5	83	AD_R5
BAD6	82	AD_R6
BAD7	81	AD_R7
BAD8	79	AD_R8
BAD9	78	AD_R9
BAD10	77	AD_R10
BAD11	76	AD_R11
BAD12	75	AD_R12
BAD13	74	AD_R13
BAD14	73	AD_R14
BAD15	71	AD_R15
BAD16	69	AD_R16
BAD17	68	AD_R17
BAD18	67	AD_R18
BAD19	66	AD_R19
BAD20	65	AD_R20
BAD21	64	AD_R21
BAD22	63	AD_R22
BAD23	61	AD_R23
BAD24	59	AD_R24
BAD25	58	AD_R25
BAD26	57	AD_R26
BAD27	56	AD_R27
BAD28	55	AD_R28
BAD29	54	AD_R29
BAD30	53	AD_R30
BAD31	52	AD_R31
BAD32	49	AD_R32
BAD33	48	AD_R33
BAD34	47	AD_R34
BAD35	46	AD_R35
BAD36	45	AD_R36
BAD37	44	AD_R37
BAD38	43	AD_R38
BAD39	42	AD_R39
BAD40	39	AD_R40
BAD41	38	AD_R41
BAD42	37	AD_R42
BAD43	36	AD_R43
BAD44	35	AD_R44
BAD45	34	AD_R45
BAD46	33	AD_R46
BAD47	32	AD_R47
BAD48	28	AD_R48
BAD49	26	AD_R49
BAD50	25	AD_R50
BAD51	24	AD_R51
BAD52	23	AD_R52
BAD53	22	AD_R53
BAD54	21	AD_R54
BAD55	20	AD_R55
BAD56	18	AD_R56
BAD57	17	AD_R57
BAD58	15	AD_R58
BAD59	14	AD_R59
BAD60	13	AD_R60
BAD61	12	AD_R61
BAD62	11	AD_R62
BAD63	10	AD_R63

AD\_R[63:0]

Not mounted



SADPO\_[7:0]

SADPO_0	101	PADC0
SADPO_1	111	PADC1
SADPO_2	121	PADC2
SADPO_3	131	PADC3
SADPO_4	140	PADC4
SADPO_5	152	PADC5
SADPO_6	162	PADC6
SADPO_7	172	PADC7

BADC0	80	ADP_R0
BADC1	70	ADP_R1
BADC2	60	ADP_R2
BADC3	50	ADP_R3
BADC4	41	ADP_R4
BADC5	39	ADP_R5
BADC6	19	ADP_R6
BADC7	9	ADP_R7

ADP\_R[7:0]

SCMD0\_[8:0]

SCMD0_0	173	PCMD0
SCMD0_1	174	PCMD1
SCMD0_2	175	PCMD2
SCMD0_3	177	PCMD3
SCMD0_4	178	PCMD4
SCMD0_5	179	PCMD5
SCMD0_6	180	PCMD6
SCMD0_7	181	PCMD7
SCMD0_8	182	PCMD8
SCMDP	183	PCMDP

BCMD0	8	CMD_R0
BCMD1	7	CMD_R1
BCMD2	6	CMD_R2
BCMD3	4	CMD_R3
BCMD4	3	CMD_R4
BCMD5	2	CMD_R5
BCMD6	1	CMD_R6
BCMD7	240	CMD_R7
BCMDP	239	CMDP_R

CMD\_R[7:0]

[1,3] SCMDP0

197	VALIN
198	DVDR
199	INPREQ
184	VALOUT
185	EXTRQ
186	RDRDY
189	WRRDY
190	IVDACK
203	IVDERR
204	RCLK
200	SLVREQ
191	SLVACK
201	TREF
202	PCHKEN
207	OMODE
192	INTR0
193	INTR1
194	LAMP0
195	LAMP1
209	SUBPOS0
208	SUBPOS1

CA302

237	AVIN
238	AVOUT
235	DVDR
236	DVOUT
226	BUSYIN
234	BUSYOUT
225	SHRDIN
223	SHRDOUT
224	INTVIN
231	INTVOUT
223	TACK
230	BPERR
221	SNPHIT
229	BOOT
228	BAREQ
227	BAGRANT
222	RRESST
217	BRCLK
218	BTCLK
216	LOCAL
215	POS0
214	POS1
213	POS2
212	POS3

ADP\_R[7:0]

CMD\_R[7:0]

CMDP\_R [5,8,11,48,56]

237	AVIN	
238	AVOUT	
235	DVDR	AVAL_R [5,8,11,17,18,22,56,68]
236	DVOUT	
226	BUSYIN	DVAL_R [5,8,11,17,18,22,48,56,68]
234	BUSYOUT	BUSY_R [44,47,58]
225	SHRDIN	/BUSY_OUT0 [16,44]
223	SHRDOUT	SHRD_R [22,58]
224	INTVIN	/SHRD_OUT0 [16]
231	INTVOUT	INTV_R [47,58]
223	TACK	/INTV_OUT0 [16,23]
230	BPERR	TACK_R [47,58]
221	SNPHIT	/PERRO [16]
229	BOOT	SNPHIT0 [23]
228	BAREQ	BOOT0 [44]
227	BAGRANT	BAREQ0 [20]
222	RRESST	BAGRANT0 [20]
217	BRCLK	SR0 [1,40]
218	BTCLK	BRCLK [53]
216	LOCAL	CLK5 [53]
215	POS0	GND
214	POS1	ID0 [65]
213	POS2	ID1 [65]
212	POS3	ID2 [65]
		ID3 [65]

dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global agent 0
Issue 2		
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SADO\_[63:0]

SADO_0	92	PAD0
SADO_1	93	PAD1
SADO_2	94	PAD2
SADO_3	95	PAD3
SADO_4	96	PAD4
SADO_5	98	PAD5
SADO_6	99	PAD6
SADO_7	100	PAD7
SADO_8	102	PAD8
SADO_9	103	PAD9
SADO_10	104	PAD10
SADO_11	105	PAD11
SADO_12	106	PAD12
SADO_13	107	PAD13
SADO_14	109	PAD14
SADO_15	110	PAD15
SADO_16	112	PAD16
SADO_17	113	PAD17
SADO_18	114	PAD18
SADO_19	115	PAD19
SADO_20	116	PAD20
SADO_21	117	PAD21
SADO_22	118	PAD22
SADO_23	120	PAD23
SADO_24	122	PAD24
SADO_25	123	PAD25
SADO_26	124	PAD26
SADO_27	125	PAD27
SADO_28	126	PAD28
SADO_29	127	PAD29
SADO_30	128	PAD30
SADO_31	129	PAD31
SADO_32	132	PAD32
SADO_33	133	PAD33
SADO_34	134	PAD34
SADO_35	135	PAD35
SADO_36	136	PAD36
SADO_37	137	PAD37
SADO_38	138	PAD38
SADO_39	139	PAD39
SADO_40	142	PAD40
SADO_41	143	PAD41
SADO_42	144	PAD42
SADO_43	145	PAD43
SADO_44	146	PAD44
SADO_45	147	PAD45
SADO_46	148	PAD46
SADO_47	149	PAD47
SADO_48	153	PAD48
SADO_49	155	PAD49
SADO_50	156	PAD50
SADO_51	157	PAD51
SADO_52	158	PAD52
SADO_53	159	PAD53
SADO_54	160	PAD54
SADO_55	161	PAD55
SADO_56	163	PAD56
SADO_57	164	PAD57
SADO_58	166	PAD58
SADO_59	167	PAD59
SADO_60	168	PAD60
SADO_61	169	PAD61
SADO_62	170	PAD62
SADO_63	171	PAD63

U2

BAD0	89	LAD_R0
BAD1	88	LAD_R1
BAD2	87	LAD_R2
BAD3	86	LAD_R3
BAD4	85	LAD_R4
BAD5	83	LAD_R5
BAD6	82	LAD_R6
BAD7	81	LAD_R7
BAD8	79	LAD_R8
BAD9	78	LAD_R9
BAD10	77	LAD_R10
BAD11	76	LAD_R11
BAD12	75	LAD_R12
BAD13	74	LAD_R13
BAD14	72	LAD_R14
BAD15	71	LAD_R15
BAD16	69	LAD_R16
BAD17	68	LAD_R17
BAD18	67	LAD_R18
BAD19	66	LAD_R19
BAD20	65	LAD_R20
BAD21	64	LAD_R21
BAD22	63	LAD_R22
BAD23	61	LAD_R23
BAD24	59	LAD_R24
BAD25	58	LAD_R25
BAD26	57	LAD_R26
BAD27	56	LAD_R27
BAD28	55	LAD_R28
BAD29	54	LAD_R29
BAD30	53	LAD_R30
BAD31	52	LAD_R31
BAD32	49	LAD_R32
BAD33	48	LAD_R33
BAD34	47	LAD_R34
BAD35	46	LAD_R35
BAD36	45	LAD_R36
BAD37	44	LAD_R37
BAD38	43	LAD_R38
BAD39	42	LAD_R39
BAD40	39	LAD_R40
BAD41	38	LAD_R41
BAD42	37	LAD_R42
BAD43	36	LAD_R43
BAD44	35	LAD_R44
BAD45	34	LAD_R45
BAD46	33	LAD_R46
BAD47	32	LAD_R47
BAD48	28	LAD_R48
BAD49	26	LAD_R49
BAD50	25	LAD_R50
BAD51	24	LAD_R51
BAD52	23	LAD_R52
BAD53	22	LAD_R53
BAD54	21	LAD_R54
BAD55	20	LAD_R55
BAD56	18	LAD_R56
BAD57	17	LAD_R57
BAD58	15	LAD_R58
BAD59	14	LAD_R59
BAD60	13	LAD_R60
BAD61	12	LAD_R61
BAD62	11	LAD_R62
BAD63	10	LAD_R63

LAD\_R[63:0]

SADPO\_[7:0]

SADPO_0	101	PADC0
SADPO_1	111	PADC1
SADPO_2	121	PADC2
SADPO_3	131	PADC3
SADPO_4	140	PADC4
SADPO_5	152	PADC5
SADPO_6	162	PADC6
SADPO_7	172	PADC7

BADC0	80	LADP_R0
BADC1	70	LADP_R1
BADC2	60	LADP_R2
BADC3	50	LADP_R3
BADC4	41	LADP_R4
BADC5	29	LADP_R5
BADC6	19	LADP_R6
BADC7	9	LADP_R7

LADP\_R[7:0]

SCMD0\_[8:0]

SCMD0_0	173	PCMD0
SCMD0_1	174	PCMD1
SCMD0_2	175	PCMD2
SCMD0_3	177	PCMD3
SCMD0_4	178	PCMD4
SCMD0_5	179	PCMD5
SCMD0_6	180	PCMD6
SCMD0_7	181	PCMD7
SCMD0_8	182	PCMD8
	183	PCMDP

BCMD0	8	LCMD_R0
BCMD1	7	LCMD_R1
BCMD2	6	LCMD_R2
BCMD3	4	LCMD_R3
BCMD4	3	LCMD_R4
BCMD5	2	LCMD_R5
BCMD6	1	LCMD_R6
BCMD7	240	LCMD_R7
BCMDP	239	

LCMD\_R[7:0]

[1,2] SCMDPO

[1]	/VALOUT0	197	VALIN
[2]	/RELEASE_LO	198	RELS
	VDD	199	INPREG
[15]	/VALIN_LO	184	VALOUT
[2]	/EXTRO_LO	185	EXTRO
[15]	/RRDRDY_LO	186	RRDRDY
[15]	/WRRDY_LO	188	WRRDY
[15]	/IVDACK_LO	189	IVDACK
[15]	/IVDERR_LO	190	IVDERR
[11]	RCLK0_1	203	RCLK
[11]	TCLK0_1	204	TCLK
	VDD	200	SLVREG
	GND	191	SLVACK
		201	TREF
[2]	/PCHKEN	202	PCHKEN
	GND	207	ICMODE
		192	INTR0
		193	INTR1
[13]	LEDO_2	194	LAMPO
[13]	LEDO_3	195	LAMP1
	GND	208	SUBPOS0
	GND	208	SUBPOS1

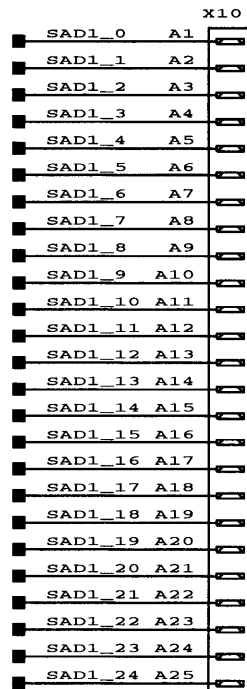
CA302

AVIN	237	
AVOUT	238	
DVIN	235	
DVOUT	236	
BUSYIN	234	
SHRDIN	225	
SHRDOUT	233	
INTVIN	224	
INTVOUT	223	
TACK	230	
BPERR	221	
SNPHIT	229	
BOOT	228	
BAGRANT	227	
RESET	217	
BRCLK	218	
BTCLK	219	
LOCAL	216	
POS0	215	
POS1	214	
POS2	213	
POS3	212	

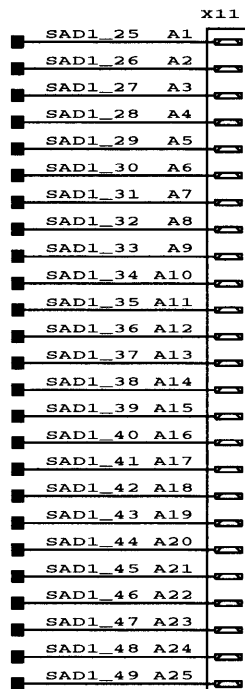
LCMDP\_R [6,9,12,52,61]

LAVAIL_R	[6,9,12,17,18,25,61,69]
LDVAL_R	[6,9,12,17,18,25,52,61,69]
LBUSY_R	[50,63]
/LBSHRO_OUT0	[16]
/LSHRD_R	[25,63]
/LSHRD_OUT0	[16]
LINTV_R	[50,63]
/LINTV_OUT0	[16,26]
LTACK_R	[50,63]
/LPKRO	[16]
LSNPHITO	[26]
LBAREQ0	[21]
LBAGRANT0	[21]
SRE0	[1,40]
BRCLK	[53]
CLKS	[53]
VDD	
ID0	[65]
ID1	[65]
ID2	[65]
ID3	[65]

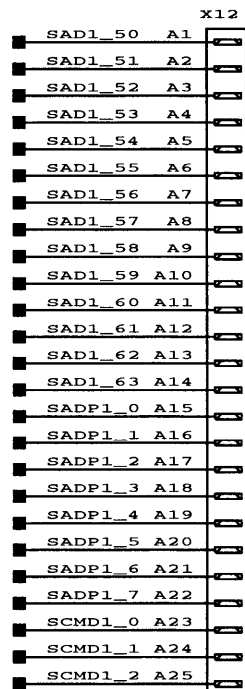
		Dansk Data Elektronik A/S	
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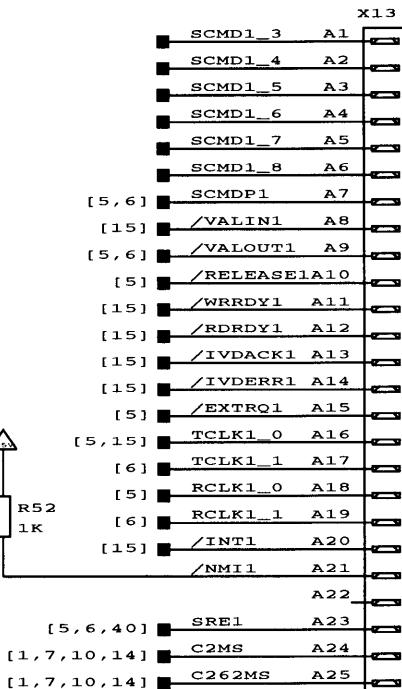
RNPAK2-25P



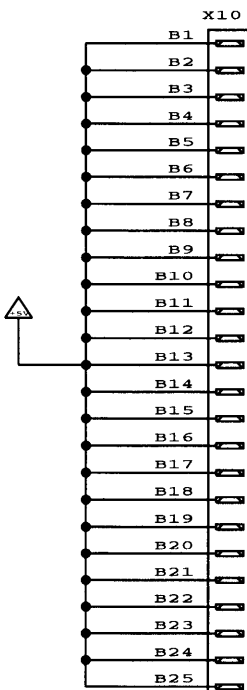
RNPAK2-25P



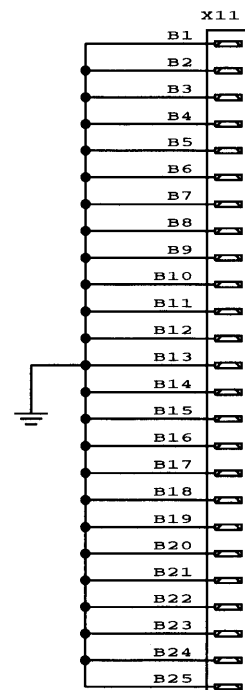
RNPAK2-25P



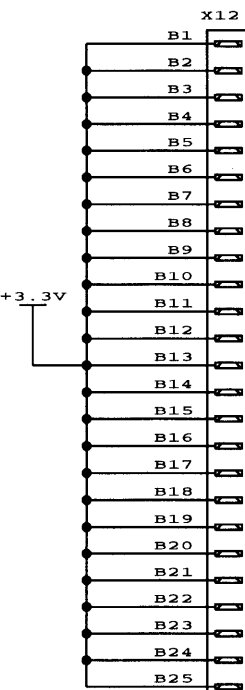
RNPAK2-25P



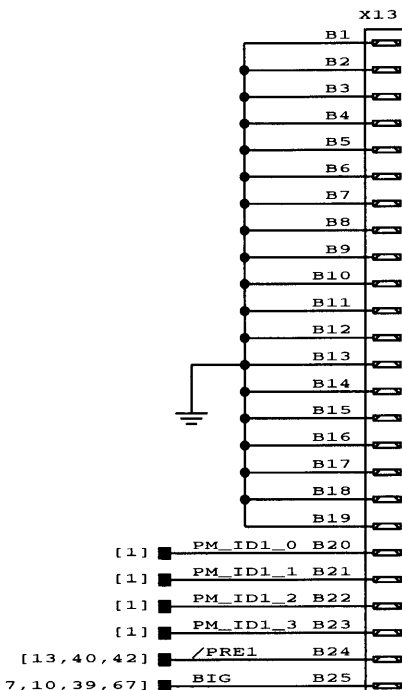
RNPAK2-25P



RNPAK2-25P



RNPAK2-25P



RNPAK2-25P

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Issue 0	940811	CPU301 Module
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Issue 2		
Issue 3		
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SAD1\_[63:0]

SAD1\_0 92
SAD1\_1 93
SAD1\_2 94
SAD1\_3 95
SAD1\_4 96
SAD1\_5 98
SAD1\_6 99
SAD1\_7 100
SAD1\_8 102
SAD1\_9 103
SAD1\_10 104
SAD1\_11 105
SAD1\_12 106
SAD1\_13 107
SAD1\_14 109
SAD1\_15 110
SAD1\_16 112
SAD1\_17 113
SAD1\_18 114
SAD1\_19 115
SAD1\_20 116
SAD1\_21 117
SAD1\_22 118
SAD1\_23 120
SAD1\_24 122
SAD1\_25 123
SAD1\_26 124
SAD1\_27 125
SAD1\_28 126
SAD1\_29 127
SAD1\_30 128
SAD1\_31 129
SAD1\_32 132
SAD1\_33 133
SAD1\_34 134
SAD1\_35 135
SAD1\_36 136
SAD1\_37 137
SAD1\_38 138
SAD1\_39 139
SAD1\_40 142
SAD1\_41 143
SAD1\_42 144
SAD1\_43 145
SAD1\_44 146
SAD1\_45 147
SAD1\_46 148
SAD1\_47 149
SAD1\_48 153
SAD1\_49 155
SAD1\_50 156
SAD1\_51 157
SAD1\_52 158
SAD1\_53 159
SAD1\_54 160
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SAD1\_56 163
SAD1\_57 164
SAD1\_58 166
SAD1\_59 167
SAD1\_60 168
SAD1\_61 169
SAD1\_62 170
SAD1\_63 171

03

PAD0
PAD1
PAD2
PAD3
PAD4
PAD5
PAD6
PAD7
PAD8
PAD9
PAD10
PAD11
PAD12
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PAD50
PAD51
PAD52
PAD53
PAD54
PAD55
PAD56
PAD57
PAD58
PAD59
PAD60
PAD61
PAD62
PAD63

AD\_R[63:0]

BAD0 89 AD\_R0
BAD1 88 AD\_R1
BAD2 87 AD\_R2
BAD3 86 AD\_R3
BAD4 85 AD\_R4
BAD5 83 AD\_R5
BAD6 82 AD\_R6
BAD7 81 AD\_R7
BAD8 79 AD\_R8
BAD9 78 AD\_R9
BAD10 77 AD\_R10
BAD11 76 AD\_R11
BAD12 75 AD\_R12
BAD13 74 AD\_R13
BAD14 72 AD\_R14
BAD15 71 AD\_R15
BAD16 69 AD\_R16
BAD17 68 AD\_R17
BAD18 67 AD\_R18
BAD19 66 AD\_R19
BAD20 65 AD\_R20
BAD21 64 AD\_R21
BAD22 63 AD\_R22
BAD23 61 AD\_R23
BAD24 59 AD\_R24
BAD25 58 AD\_R25
BAD26 57 AD\_R26
BAD27 56 AD\_R27
BAD28 55 AD\_R28
BAD29 54 AD\_R29
BAD30 53 AD\_R30
BAD31 52 AD\_R31
BAD32 49 AD\_R32
BAD33 48 AD\_R33
BAD34 47 AD\_R34
BAD35 46 AD\_R35
BAD36 45 AD\_R36
BAD37 44 AD\_R37
BAD38 43 AD\_R38
BAD39 42 AD\_R39
BAD40 39 AD\_R40
BAD41 38 AD\_R41
BAD42 37 AD\_R42
BAD43 36 AD\_R43
BAD44 35 AD\_R44
BAD45 34 AD\_R45
BAD46 33 AD\_R46
BAD47 32 AD\_R47
BAD48 28 AD\_R48
BAD49 26 AD\_R49
BAD50 25 AD\_R50
BAD51 24 AD\_R51
BAD52 23 AD\_R52
BAD53 22 AD\_R53
BAD54 21 AD\_R54
BAD55 20 AD\_R55
BAD56 18 AD\_R56
BAD57 17 AD\_R57
BAD58 15 AD\_R58
BAD59 14 AD\_R59
BAD60 13 AD\_R60
BAD61 12 AD\_R61
BAD62 11 AD\_R62
BAD63 10 AD\_R63

SADP1\_[7:0]

SADP1\_0 101
SADP1\_1 111
SADP1\_2 121
SADP1\_3 131
SADP1\_4 140
SADP1\_5 152
SADP1\_6 162
SADP1\_7 172

03

PADC0
PADC1
PADC2
PADC3
PADC4
PADC5
PADC6
PADC7

ADP\_R[7:0]

BADC0 80 ADP\_R0
BADC1 70 ADP\_R1
BADC2 60 ADP\_R2
BADC3 50 ADP\_R3
BADC4 41 ADP\_R4
BADC5 29 ADP\_R5
BADC6 19 ADP\_R6
BADC7 9 ADP\_R7

SCMD1\_[8:0]

SCMD1\_0 173
SCMD1\_1 174
SCMD1\_2 175
SCMD1\_3 177
SCMD1\_4 178
SCMD1\_5 179
SCMD1\_6 180
SCMD1\_7 181
SCMD1\_8 182
SCMD1\_9 183

03

PCMD0
PCMD1
PCMD2
PCMD3
PCMD4
PCMD5
PCMD6
PCMD7
PCMD8
PCMDP

CMD\_R[7:0]

BCMD0 8 CMD\_R0
BCMD1 7 CMD\_R1
BCMD2 6 CMD\_R2
BCMD3 4 CMD\_R3
BCMD4 3 CMD\_R4
BCMD5 2 CMD\_R5
BCMD6 1 CMD\_R6
BCMD7 240 CMD\_R7
BCMDP 239

[4,6] SCMDP1

[4] /VALOUT1
[4] /RELEASE1
VDD
[15] /VALIN\_G1
[4] /EXTRO1
[15] /RDRDY\_G1
[15] /WRRDY\_G1
[15] /IVDACK\_G1
[15] /IVDERR\_G1
[4] RCLK1\_0
[4] TCLK1\_0
[6] /EXTRO\_L1
[6] /RELEASE\_L1
[14] TREF
[2] /PCHKEN
GND
[13] LED1\_0
[13] LED1\_1
VDD
GND

197 VALIN
198 RELS
199 INPREG
184 VALOUT
185 EXTRO
186 RDRDY
188 WRRDY
189 IVDACK
190 IVDERR
203 RCLK
204 TCLK
200 RCLK
200 RCLK
191 SLVACK
201 TREF
202 PCHKEN
207 IOMODE
192 INTR0
193 INTR1
194 LAMPO
195 LAMP1
208 SUBPOS0
SUBPOS1

CA302

AVIN 237
AVOUT 238
DVIN 235
DVOUT 236
BUSYIN 234
EXTRO 225
SHRDIN 225
SHRDOUT 233
INTVIN 224
INTVOUT 223
TACK 230
HPERR 221
SNPHIT 221
BOOT 229
BAREQ 228
BAGRANT 227
RESET 217
BRCLK 218
BPCLK 216
LOCAL 216
POSO 215
POSI 214
POSI 213
POSI 212

CMDP\_R [2,8,11,48,56]

AVAL\_R [2,8,11,17,18,22,56,68]
DVAL\_R [2,8,11,17,18,22,48,56,68]
BUSY\_R [44,47,58]
/BUGY\_OUT1 [16,44]
SHRD\_R [22,58]
/SHRD\_OUT1 [16]
INTV\_R [47,58]
/INTV\_OUT1 [16,23]
TACK\_R [47,58]
/HPERR [16]
SNPHIT1 [23]
BOOT1 [44]
BAREQ1 [20]
BAGRANT1 [20]
SRE1 [4,40]
BRCLK [53]
CLK5 [53]
GND
ID0 [65]
ID1 [65]
ID2 [65]
ID3 [65]

Table with 4 columns: Issue, Part Number (940811), Module Name (CPU301 Module), and File/Page (File: cpu301 Page: 5 of 72). Includes logo for Dansk Data Elektronik A/S.

SAD1\_[63:0]

SAD1\_0 92 PAD0
SAD1\_1 93 PAD1
SAD1\_2 94 PAD2
SAD1\_3 95 PAD3
SAD1\_4 96 PAD4
SAD1\_5 98 PAD5
SAD1\_6 99 PAD6
SAD1\_7 100 PAD7
SAD1\_8 102 PAD8
SAD1\_9 103 PAD9
SAD1\_10 104 PAD10
SAD1\_11 105 PAD11
SAD1\_12 106 PAD12
SAD1\_13 107 PAD13
SAD1\_14 109 PAD14
SAD1\_15 110 PAD15
SAD1\_16 112 PAD16
SAD1\_17 113 PAD17
SAD1\_18 114 PAD18
SAD1\_19 115 PAD19
SAD1\_20 116 PAD20
SAD1\_21 117 PAD21
SAD1\_22 118 PAD22
SAD1\_23 120 PAD23
SAD1\_24 122 PAD24
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SAD1\_26 124 PAD26
SAD1\_27 125 PAD27
SAD1\_28 126 PAD28
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SAD1\_30 128 PAD30
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SAD1\_34 134 PAD34
SAD1\_35 135 PAD35
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SAD1\_38 138 PAD38
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SAD1\_41 143 PAD41
SAD1\_42 144 PAD42
SAD1\_43 145 PAD43
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SAD1\_45 147 PAD45
SAD1\_46 148 PAD46
SAD1\_47 149 PAD47
SAD1\_48 153 PAD48
SAD1\_49 155 PAD49
SAD1\_50 156 PAD50
SAD1\_51 157 PAD51
SAD1\_52 158 PAD52
SAD1\_53 159 PAD53
SAD1\_54 160 PAD54
SAD1\_55 161 PAD55
SAD1\_56 163 PAD56
SAD1\_57 164 PAD57
SAD1\_58 166 PAD58
SAD1\_59 167 PAD59
SAD1\_60 168 PAD60
SAD1\_61 169 PAD61
SAD1\_62 170 PAD62
SAD1\_63 171 PAD63

U4

BAD0 89 LAD\_R0
BAD1 88 LAD\_R1
BAD2 87 LAD\_R2
BAD3 86 LAD\_R3
BAD4 85 LAD\_R4
BAD5 83 LAD\_R5
BAD6 82 LAD\_R6
BAD7 81 LAD\_R7
BAD8 79 LAD\_R8
BAD9 78 LAD\_R9
BAD10 77 LAD\_R10
BAD11 76 LAD\_R11
BAD12 75 LAD\_R12
BAD13 74 LAD\_R13
BAD14 72 LAD\_R14
BAD15 71 LAD\_R15
BAD16 69 LAD\_R16
BAD17 68 LAD\_R17
BAD18 67 LAD\_R18
BAD19 66 LAD\_R19
BAD20 65 LAD\_R20
BAD21 64 LAD\_R21
BAD22 63 LAD\_R22
BAD23 61 LAD\_R23
BAD24 59 LAD\_R24
BAD25 58 LAD\_R25
BAD26 57 LAD\_R26
BAD27 56 LAD\_R27
BAD28 55 LAD\_R28
BAD29 54 LAD\_R29
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BAD36 45 LAD\_R36
BAD37 44 LAD\_R37
BAD38 43 LAD\_R38
BAD39 42 LAD\_R39
BAD40 39 LAD\_R40
BAD41 38 LAD\_R41
BAD42 37 LAD\_R42
BAD43 36 LAD\_R43
BAD44 35 LAD\_R44
BAD45 34 LAD\_R45
BAD46 33 LAD\_R46
BAD47 32 LAD\_R47
BAD48 28 LAD\_R48
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BAD52 23 LAD\_R52
BAD53 22 LAD\_R53
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BAD55 20 LAD\_R55
BAD56 17 LAD\_R56
BAD57 15 LAD\_R57
BAD58 14 LAD\_R58
BAD59 13 LAD\_R59
BAD60 12 LAD\_R60
BAD61 11 LAD\_R61
BAD62 10 LAD\_R62
BAD63 10 LAD\_R63

LAD\_R[63:0]

SADP1\_[7:0]

SADP1\_0 101 PADC0
SADP1\_1 111 PADC1
SADP1\_2 121 PADC2
SADP1\_3 131 PADC3
SADP1\_4 140 PADC4
SADP1\_5 152 PADC5
SADP1\_6 162 PADC6
SADP1\_7 172 PADC7

BADC0 80 LADP\_R0
BADC1 70 LADP\_R1
BADC2 60 LADP\_R2
BADC3 50 LADP\_R3
BADC4 41 LADP\_R4
BADC5 29 LADP\_R5
BADC6 19 LADP\_R6
BADC7 9 LADP\_R7

LADP\_R[7:0]

SCMD1\_[8:0]

SCMD1\_0 173 PCMD0
SCMD1\_1 174 PCMD1
SCMD1\_2 175 PCMD2
SCMD1\_3 177 PCMD3
SCMD1\_4 178 PCMD4
SCMD1\_5 179 PCMD5
SCMD1\_6 180 PCMD6
SCMD1\_7 181 PCMD7
SCMD1\_8 182 PCMD8
SCMD1\_8 183 PCMDP

BCMD0 8 LCMD\_R0
BCMD1 7 LCMD\_R1
BCMD2 6 LCMD\_R2
BCMD3 4 LCMD\_R3
BCMD4 3 LCMD\_R4
BCMD5 2 LCMD\_R5
BCMD6 1 LCMD\_R6
BCMD7 240 LCMD\_R7
BCMDP 239

LCMD\_R[7:0]

[4,5] SCMDP1

[4] /VALOUT1 197 VALIN
[5] /RELEASE\_L1 198 RELS
VDD 199 INPREQ
[15] /VALIN\_L1 184 VALOUT
[5] /EXTRO\_L1 185 EXTRO
[15] /RDRDY\_L1 186 RDRDY
[15] /WRRDY\_L1 188 WRRDY
[15] /IVDACK\_L1 189 IVDACK
[15] /IVDERR\_L1 190 IVDERR
[4] RCLK1\_1 204 RCLK
[4] TCLK1\_1 200 TCLK
VDD 203 SIVREG
GND 191 SILVACK
GND 201 TREF
[2] /PCHKEN 202 PCHKEN
GND 207 COMODE
GND 192 INTR0
GND 193 INTR1
[13] LED1\_2 194 LAMP0
[13] LED1\_3 195 LAMP1
VDD 209 SUBPOS0
GND 208 SUBPOS1

CA302

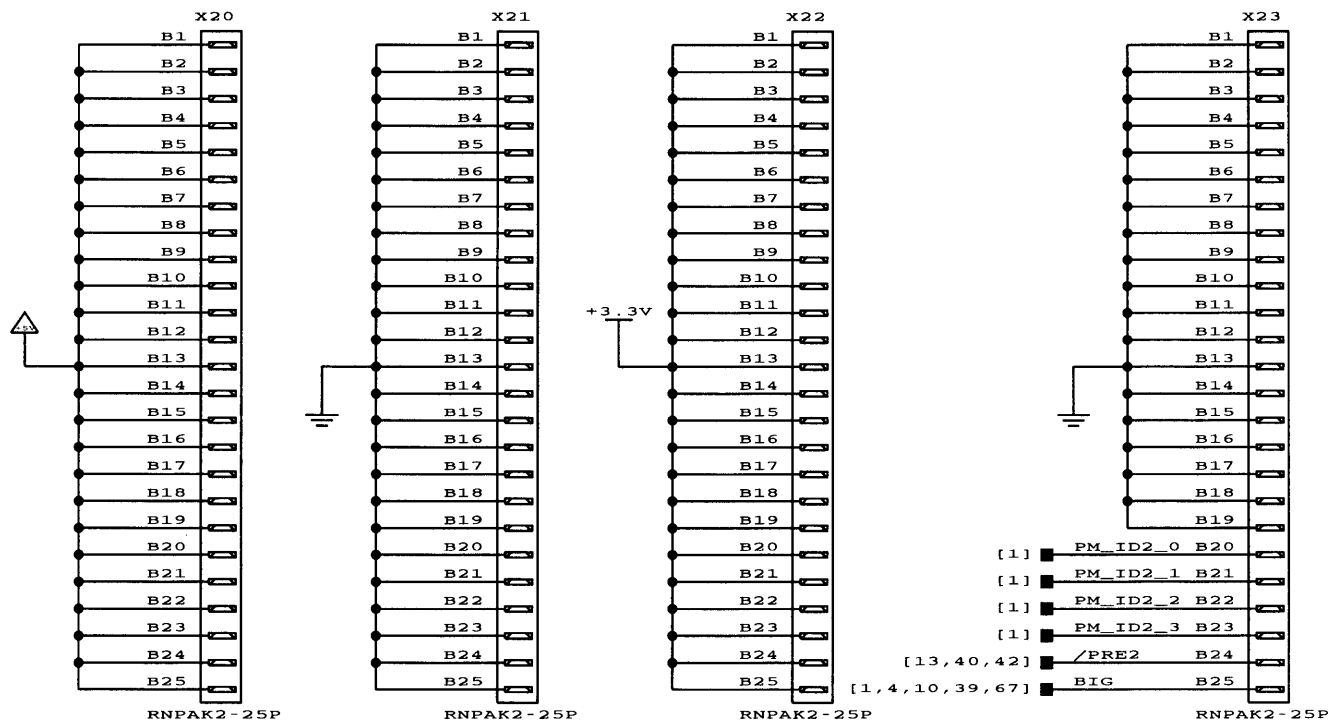
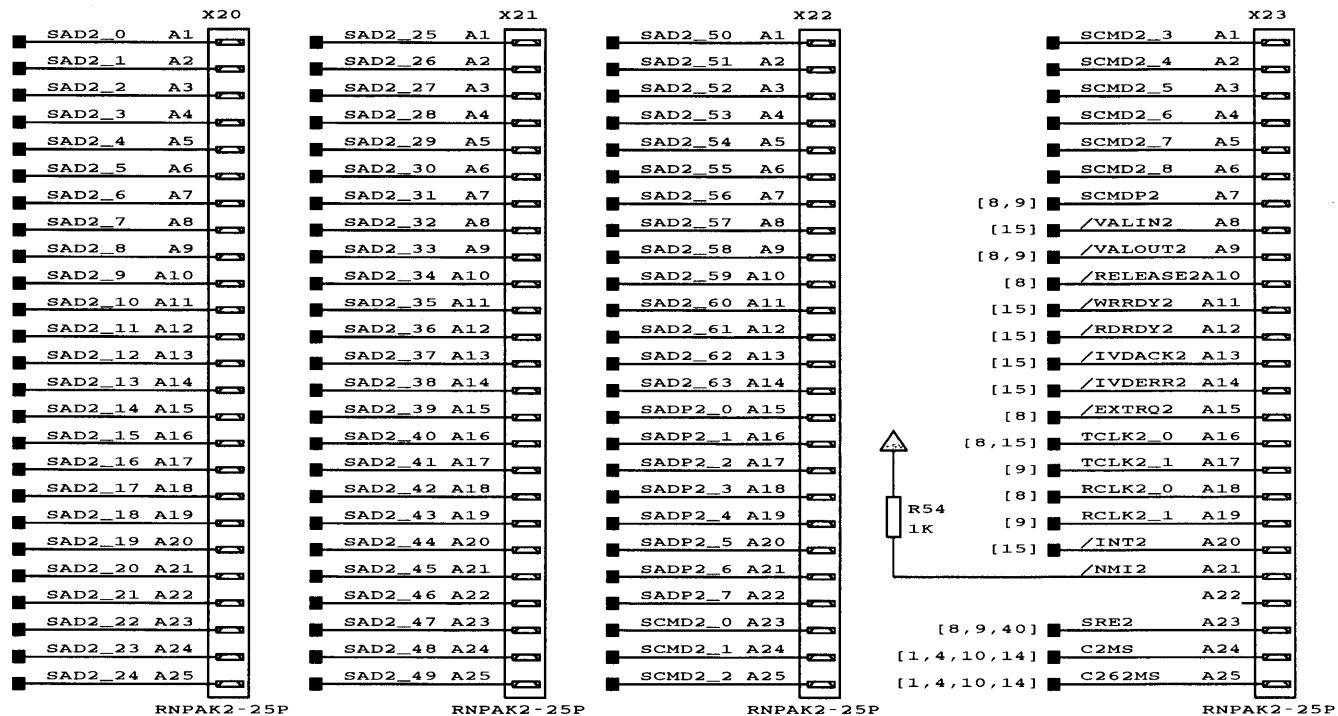
AVIN 237
AVOUT 238
DVIN 235
DVOUT 236
BUSYIN 234
BUSYOUT 234
SHRDIN 225
SHRDOUT 233
INTVIN 224
INTVOUT 223
TACK 230
BPERR 221
SNPHIT 221
BOOI 229
BAREQ 228
BAGRANT 227
BRCLK 217
BTCLK 218
LOCAL 216
POS0 215
POS1 214
POS2 213
POS3 212

LCMDP\_R [3,9,12,52,61]

LAVAL\_R [3,9,12,17,18,25,61,69]
LDVAL\_R [3,9,12,17,18,25,52,61,69]
LBUSY\_R [50,63]
LSHRD\_R [25,63]
/LSHRD\_OUT1 [16]
/LINTV\_OUT1 [16]
/LTACK\_R [50,63]
/LSPHIT1 [26]

[21] LBAREQ1
[21] LBAGRANT1
[4,40] SRE1
BRCLK [53]
CLK5 [53]
VDD
ID0 [65]
ID1 [65]
ID2 [65]
ID3 [65]

Table with 3 columns: Issue, Part Number (940811), and Description (CPU301 Module, Local agent 1). Includes logo for Dansk Data Elektronik A/S.



		Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module	
Issue 1		Connectors 2	
Issue 2			
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SAD2\_[63:0]

SAD2\_0 92 PAD0
SAD2\_1 93 PAD1
SAD2\_2 94 PAD2
SAD2\_3 95 PAD3
SAD2\_4 96 PAD4
SAD2\_5 98 PAD5
SAD2\_6 99 PAD6
SAD2\_7 100 PAD7
SAD2\_8 102 PAD8
SAD2\_9 103 PAD9
SAD2\_10 104 PAD10
SAD2\_11 105 PAD11
SAD2\_12 106 PAD12
SAD2\_13 107 PAD13
SAD2\_14 109 PAD14
SAD2\_15 110 PAD15
SAD2\_16 112 PAD16
SAD2\_17 113 PAD17
SAD2\_18 114 PAD18
SAD2\_19 115 PAD19
SAD2\_20 116 PAD20
SAD2\_21 117 PAD21
SAD2\_22 118 PAD22
SAD2\_23 120 PAD23
SAD2\_24 122 PAD24
SAD2\_25 123 PAD25
SAD2\_26 124 PAD26
SAD2\_27 125 PAD27
SAD2\_28 126 PAD28
SAD2\_29 127 PAD29
SAD2\_30 128 PAD30
SAD2\_31 129 PAD31
SAD2\_32 132 PAD32
SAD2\_33 133 PAD33
SAD2\_34 134 PAD34
SAD2\_35 135 PAD35
SAD2\_36 136 PAD36
SAD2\_37 137 PAD37
SAD2\_38 138 PAD38
SAD2\_39 139 PAD39
SAD2\_40 142 PAD40
SAD2\_41 143 PAD41
SAD2\_42 144 PAD42
SAD2\_43 145 PAD43
SAD2\_44 146 PAD44
SAD2\_45 147 PAD45
SAD2\_46 148 PAD46
SAD2\_47 149 PAD47
SAD2\_48 153 PAD48
SAD2\_49 155 PAD49
SAD2\_50 156 PAD50
SAD2\_51 157 PAD51
SAD2\_52 158 PAD52
SAD2\_53 159 PAD53
SAD2\_54 160 PAD54
SAD2\_55 161 PAD55
SAD2\_56 163 PAD56
SAD2\_57 164 PAD57
SAD2\_58 166 PAD58
SAD2\_59 167 PAD59
SAD2\_60 168 PAD60
SAD2\_61 169 PAD61
SAD2\_62 170 PAD62
SAD2\_63 171 PAD63

U5

BAD0 89 AD\_R0
BAD1 88 AD\_R1
BAD2 87 AD\_R2
BAD3 86 AD\_R3
BAD4 85 AD\_R4
BAD5 83 AD\_R5
BAD6 82 AD\_R6
BAD7 81 AD\_R7
BAD8 79 AD\_R8
BAD9 78 AD\_R9
BAD10 77 AD\_R10
BAD11 76 AD\_R11
BAD12 75 AD\_R12
BAD13 74 AD\_R13
BAD14 72 AD\_R14
BAD15 71 AD\_R15
BAD16 69 AD\_R16
BAD17 68 AD\_R17
BAD18 67 AD\_R18
BAD19 66 AD\_R19
BAD20 65 AD\_R20
BAD21 64 AD\_R21
BAD22 63 AD\_R22
BAD23 61 AD\_R23
BAD24 59 AD\_R24
BAD25 58 AD\_R25
BAD26 57 AD\_R26
BAD27 56 AD\_R27
BAD28 55 AD\_R28
BAD29 54 AD\_R29
BAD30 53 AD\_R30
BAD31 52 AD\_R31
BAD32 49 AD\_R32
BAD33 48 AD\_R33
BAD34 47 AD\_R34
BAD35 46 AD\_R35
BAD36 45 AD\_R36
BAD37 44 AD\_R37
BAD38 43 AD\_R38
BAD39 42 AD\_R39
BAD40 39 AD\_R40
BAD41 38 AD\_R41
BAD42 37 AD\_R42
BAD43 36 AD\_R43
BAD44 35 AD\_R44
BAD45 34 AD\_R45
BAD46 33 AD\_R46
BAD47 32 AD\_R47
BAD48 31 AD\_R48
BAD49 25 AD\_R49
BAD50 25 AD\_R50
BAD51 24 AD\_R51
BAD52 23 AD\_R52
BAD53 22 AD\_R53
BAD54 21 AD\_R54
BAD55 20 AD\_R55
BAD56 19 AD\_R56
BAD57 17 AD\_R57
BAD58 15 AD\_R58
BAD59 14 AD\_R59
BAD60 13 AD\_R60
BAD61 12 AD\_R61
BAD62 11 AD\_R62
BAD63 10 AD\_R63

AD\_R[63:0]

SADP2\_[7:0]

SADP2\_0 101 PADC0
SADP2\_1 111 PADC1
SADP2\_2 121 PADC2
SADP2\_3 131 PADC3
SADP2\_4 140 PADC4
SADP2\_5 152 PADC5
SADP2\_6 162 PADC6
SADP2\_7 172 PADC7

BADC0 80 ADP\_R0
BADC1 70 ADP\_R1
BADC2 60 ADP\_R2
BADC3 50 ADP\_R3
BADC4 41 ADP\_R4
BADC5 29 ADP\_R5
BADC6 19 ADP\_R6
BADC7 9 ADP\_R7

ADP\_R[7:0]

SCMD2\_[8:0]

SCMD2\_0 173 PCMD0
SCMD2\_1 174 PCMD1
SCMD2\_2 175 PCMD2
SCMD2\_3 177 PCMD3
SCMD2\_4 178 PCMD4
SCMD2\_5 179 PCMD5
SCMD2\_6 180 PCMD6
SCMD2\_7 181 PCMD7
SCMD2\_8 182 PCMD8
SCMD2\_9 183 PCMD9

BCMD0 8 CMD\_R0
BCMD1 7 CMD\_R1
BCMD2 6 CMD\_R2
BCMD3 4 CMD\_R3
BCMD4 3 CMD\_R4
BCMD5 2 CMD\_R5
BCMD6 1 CMD\_R6
BCMD7 240 CMD\_R7
BCMD9 239

CMD\_R[7:0]

[7,9] SCMDP2

197 VALIN
198 RELEAS2
199 VDD
200 INTPREQ
201 EXTREQ
202 RDRDY
203 WRRDY
204 IVACK
205 IVERR
206 RCLK
207 SLVREQ
208 SLVACK
209 TREF
210 PCHKEN
211 IOMODE
212 INTR1
213 LAMP0
214 LAMP1
215 SUBPOS0
216 SUBPOS1

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237 AVIN
238 AVOUT
239 DVIN
240 DVOUT
241 VALOUT
242 EXTREQ
243 RDRDY
244 WRRDY
245 IVACK
246 IVERR
247 RCLK
248 SNPHIT
249 BOOT
250 BAREQ
251 BAGRANT
252 RESET
253 BRCLK
254 BTCLK
255 LOCAL
256 POS0
257 POS1
258 POS2
259 POS3

CMDP\_R [2,5,11,48,56]

AVIN [237]
AVOUT [238]
DVIN [239]
DVOUT [240]
VALOUT [241]
EXTREQ [242]
RDRDY [243]
WRRDY [244]
IVACK [245]
IVERR [246]
RCLK [247]
SNPHIT [248]
BOOT [249]
BAREQ [250]
BAGRANT [251]
RESET [252]
BRCLK [253]
BTCLK [254]
LOCAL [255]
POS0 [256]
POS1 [257]
POS2 [258]
POS3 [259]
AVAL\_R [2,5,11,17,18,22,56,68]
DVAL\_R [2,5,11,17,18,22,48,56,68]
BUSY\_R [44,47,58]
BUSY\_OUT2 [16,44]
SHRD\_R [22,58]
SHRD\_OUT2 [16]
INTV\_R [47,58]
INTV\_OUT2 [16,24]
TACK\_R [47,58]
PERR2 [16]
SNPHIT2 [24]
BOOT2 [44]
BAREQ2 [20]
BAGRANT2 [20]
SRE2 [7,40]
BRCLK [53]
CLK5 [53]
GND
ID0 [65]
ID1 [65]
ID2 [65]
ID3 [65]

db Dansk Data Elektronik A/S
Issue 0 940811 CPU301 Module
Issue 1 Global agent 2
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SAD2\_[63:0]

SAD2_0	92	PAD0
SAD2_1	93	PAD1
SAD2_2	94	PAD2
SAD2_3	95	PAD3
SAD2_4	96	PAD4
SAD2_5	98	PAD5
SAD2_6	99	PAD6
SAD2_7	100	PAD7
SAD2_8	102	PAD8
SAD2_9	103	PAD9
SAD2_10	104	PAD10
SAD2_11	105	PAD11
SAD2_12	106	PAD12
SAD2_13	107	PAD13
SAD2_14	109	PAD14
SAD2_15	110	PAD15
SAD2_16	112	PAD16
SAD2_17	113	PAD17
SAD2_18	114	PAD18
SAD2_19	115	PAD19
SAD2_20	116	PAD20
SAD2_21	117	PAD21
SAD2_22	118	PAD22
SAD2_23	120	PAD23
SAD2_24	122	PAD24
SAD2_25	123	PAD25
SAD2_26	124	PAD26
SAD2_27	125	PAD27
SAD2_28	126	PAD28
SAD2_29	127	PAD29
SAD2_30	128	PAD30
SAD2_31	129	PAD31
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SAD2_33	133	PAD33
SAD2_34	134	PAD34
SAD2_35	135	PAD35
SAD2_36	136	PAD36
SAD2_37	137	PAD37
SAD2_38	138	PAD38
SAD2_39	139	PAD39
SAD2_40	142	PAD40
SAD2_41	143	PAD41
SAD2_42	144	PAD42
SAD2_43	145	PAD43
SAD2_44	146	PAD44
SAD2_45	147	PAD45
SAD2_46	148	PAD46
SAD2_47	149	PAD47
SAD2_48	153	PAD48
SAD2_49	155	PAD49
SAD2_50	156	PAD50
SAD2_51	157	PAD51
SAD2_52	158	PAD52
SAD2_53	159	PAD53
SAD2_54	160	PAD54
SAD2_55	161	PAD55
SAD2_56	163	PAD56
SAD2_57	164	PAD57
SAD2_58	166	PAD58
SAD2_59	167	PAD59
SAD2_60	168	PAD60
SAD2_61	169	PAD61
SAD2_62	170	PAD62
SAD2_63	171	PAD63

U6

BAD0	89	LAD_R0
BAD1	88	LAD_R1
BAD2	87	LAD_R2
BAD3	86	LAD_R3
BAD4	85	LAD_R4
BAD5	83	LAD_R5
BAD6	82	LAD_R6
BAD7	81	LAD_R7
BAD8	79	LAD_R8
BAD9	78	LAD_R9
BAD10	77	LAD_R10
BAD11	76	LAD_R11
BAD12	75	LAD_R12
BAD13	74	LAD_R13
BAD14	72	LAD_R14
BAD15	71	LAD_R15
BAD16	69	LAD_R16
BAD17	68	LAD_R17
BAD18	67	LAD_R18
BAD19	66	LAD_R19
BAD20	65	LAD_R20
BAD21	64	LAD_R21
BAD22	63	LAD_R22
BAD23	61	LAD_R23
BAD24	59	LAD_R24
BAD25	58	LAD_R25
BAD26	57	LAD_R26
BAD27	56	LAD_R27
BAD28	55	LAD_R28
BAD29	54	LAD_R29
BAD30	53	LAD_R30
BAD31	52	LAD_R31
BAD32	49	LAD_R32
BAD33	48	LAD_R33
BAD34	47	LAD_R34
BAD35	46	LAD_R35
BAD36	45	LAD_R36
BAD37	44	LAD_R37
BAD38	43	LAD_R38
BAD39	42	LAD_R39
BAD40	39	LAD_R40
BAD41	38	LAD_R41
BAD42	37	LAD_R42
BAD43	36	LAD_R43
BAD44	35	LAD_R44
BAD45	34	LAD_R45
BAD46	33	LAD_R46
BAD47	32	LAD_R47
BAD48	28	LAD_R48
BAD49	26	LAD_R49
BAD50	25	LAD_R50
BAD51	24	LAD_R51
BAD52	23	LAD_R52
BAD53	22	LAD_R53
BAD54	21	LAD_R54
BAD55	20	LAD_R55
BAD56	18	LAD_R56
BAD57	17	LAD_R57
BAD58	15	LAD_R58
BAD59	14	LAD_R59
BAD60	13	LAD_R60
BAD61	12	LAD_R61
BAD62	11	LAD_R62
BAD63	10	LAD_R63

LAD\_R[63:0]

SADP2\_[7:0]

SADP2_0	101	PADC0
SADP2_1	111	PADC1
SADP2_2	121	PADC2
SADP2_3	131	PADC3
SADP2_4	140	PADC4
SADP2_5	152	PADC5
SADP2_6	162	PADC6
SADP2_7	172	PADC7

BADC0	80	LADP_R0
BADC1	70	LADP_R1
BADC2	60	LADP_R2
BADC3	50	LADP_R3
BADC4	41	LADP_R4
BADC5	29	LADP_R5
BADC6	19	LADP_R6
BADC7	9	LADP_R7

LADP\_R[7:0]

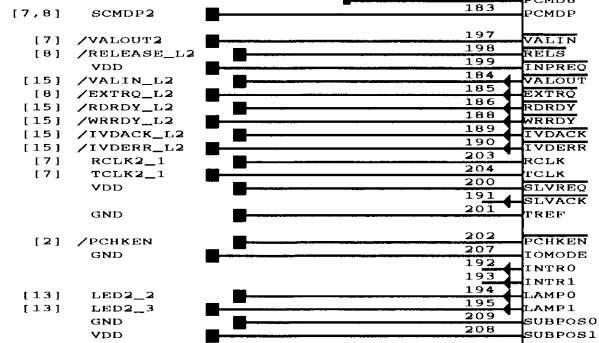
SCMD2\_[8:0]

SCMD2_0	173	PCMD0
SCMD2_1	174	PCMD1
SCMD2_2	175	PCMD2
SCMD2_3	177	PCMD3
SCMD2_4	178	PCMD4
SCMD2_5	179	PCMD5
SCMD2_6	180	PCMD6
SCMD2_7	181	PCMD7
SCMD2_8	182	PCMD8
SCMDP	183	PCMDP

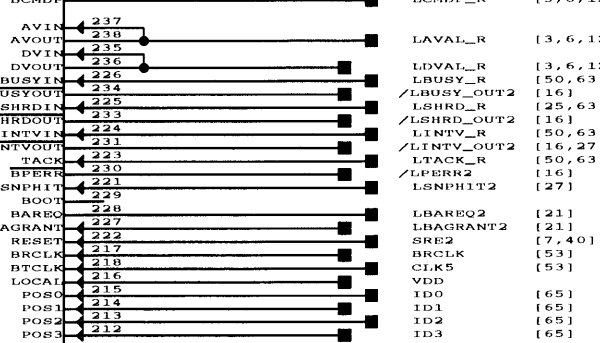
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BCMD1	7	LCMD_R1
BCMD2	6	LCMD_R2
BCMD3	4	LCMD_R3
BCMD4	3	LCMD_R4
BCMD5	2	LCMD_R5
BCMD6	1	LCMD_R6
BCMD7	240	LCMD_R7
BCMDP	239	LCMDP_R

LCMD\_R[7:0]

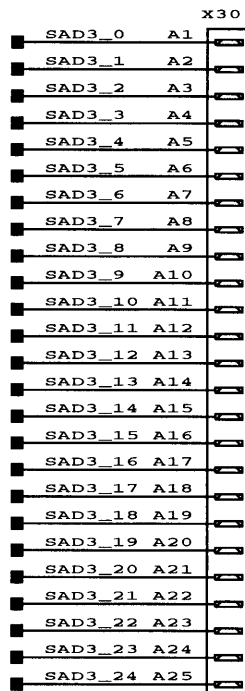
LCMDP\_R [3,6,12,52,61]



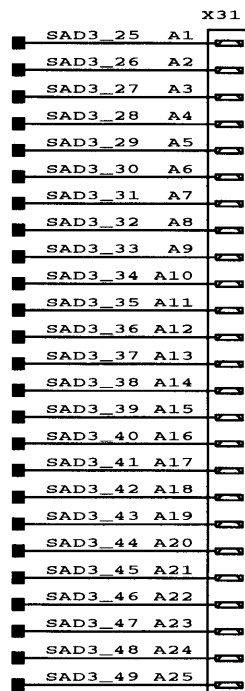
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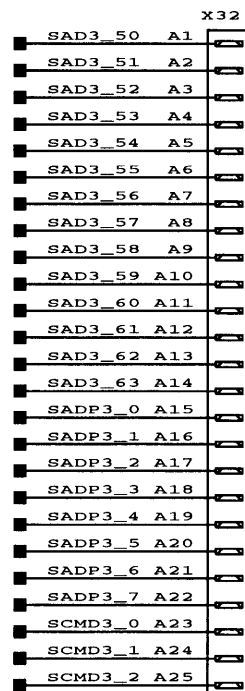
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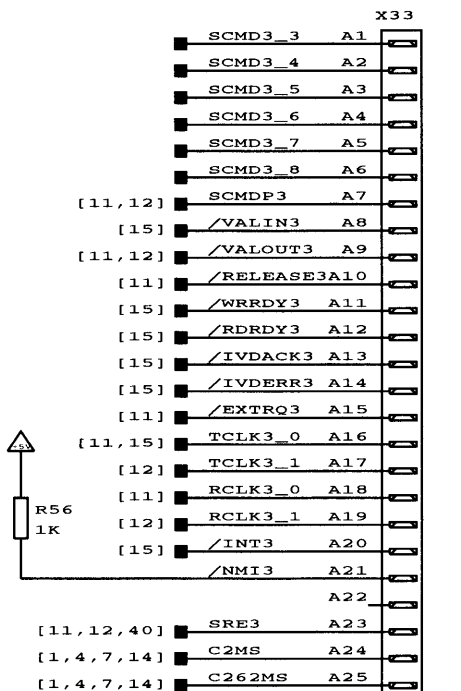
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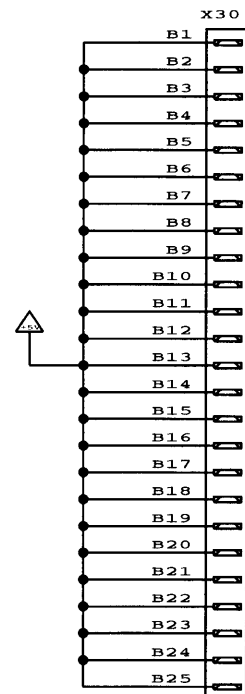
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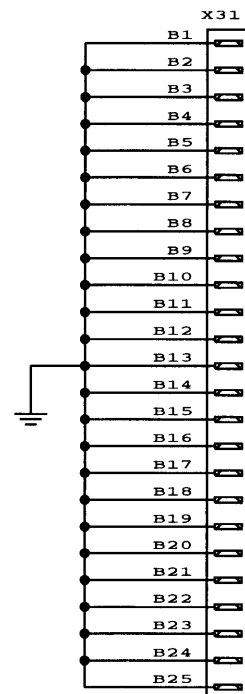
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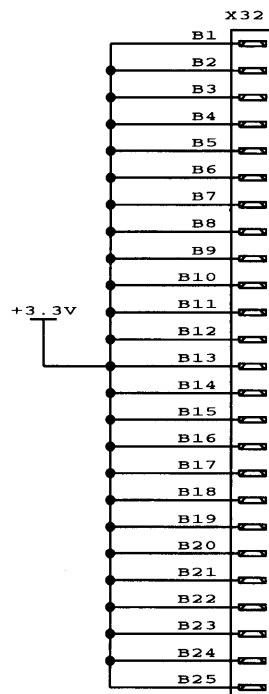
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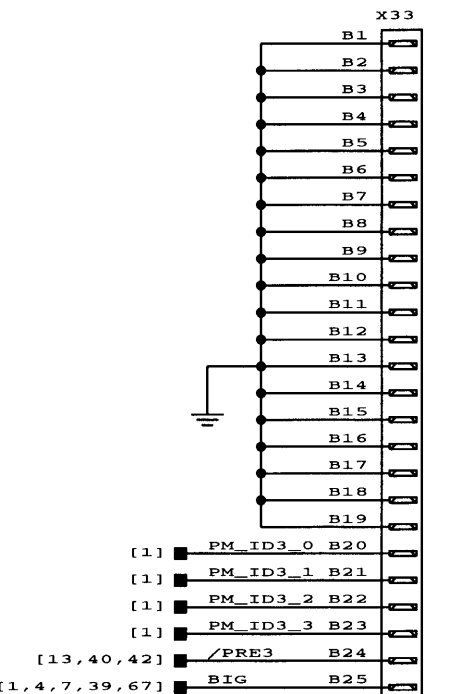
RNP25P



RNP25P



RNP25P



RNP25P

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Issue 0	940811	CPU301 Module	
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Issue 2			
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SAD3\_[63:0]

SAD3_0	92	PAD0
SAD3_1	93	PAD1
SAD3_2	94	PAD2
SAD3_3	95	PAD3
SAD3_4	96	PAD4
SAD3_5	98	PAD5
SAD3_6	99	PAD6
SAD3_7	100	PAD7
SAD3_8	102	PAD8
SAD3_9	103	PAD9
SAD3_10	104	PAD10
SAD3_11	105	PAD11
SAD3_12	106	PAD12
SAD3_13	107	PAD13
SAD3_14	109	PAD14
SAD3_15	110	PAD15
SAD3_16	112	PAD16
SAD3_17	113	PAD17
SAD3_18	114	PAD18
SAD3_19	115	PAD19
SAD3_20	116	PAD20
SAD3_21	117	PAD21
SAD3_22	118	PAD22
SAD3_23	120	PAD23
SAD3_24	122	PAD24
SAD3_25	123	PAD25
SAD3_26	124	PAD26
SAD3_27	125	PAD27
SAD3_28	126	PAD28
SAD3_29	127	PAD29
SAD3_30	128	PAD30
SAD3_31	129	PAD31
SAD3_32	132	PAD32
SAD3_33	133	PAD33
SAD3_34	134	PAD34
SAD3_35	135	PAD35
SAD3_36	136	PAD36
SAD3_37	137	PAD37
SAD3_38	138	PAD38
SAD3_39	139	PAD39
SAD3_40	142	PAD40
SAD3_41	143	PAD41
SAD3_42	144	PAD42
SAD3_43	145	PAD43
SAD3_44	146	PAD44
SAD3_45	147	PAD45
SAD3_46	148	PAD46
SAD3_47	149	PAD47
SAD3_48	153	PAD48
SAD3_49	155	PAD49
SAD3_50	156	PAD50
SAD3_51	157	PAD51
SAD3_52	158	PAD52
SAD3_53	159	PAD53
SAD3_54	160	PAD54
SAD3_55	161	PAD55
SAD3_56	163	PAD56
SAD3_57	164	PAD57
SAD3_58	166	PAD58
SAD3_59	167	PAD59
SAD3_60	168	PAD60
SAD3_61	169	PAD61
SAD3_62	170	PAD62
SAD3_63	171	PAD63

U7

BAD0	89	AD_R0
BAD1	88	AD_R1
BAD2	87	AD_R2
BAD3	86	AD_R3
BAD4	85	AD_R4
BAD5	83	AD_R5
BAD6	82	AD_R6
BAD7	81	AD_R7
BAD8	79	AD_R8
BAD9	78	AD_R9
BAD10	77	AD_R10
BAD11	76	AD_R11
BAD12	75	AD_R12
BAD13	74	AD_R13
BAD14	72	AD_R14
BAD15	71	AD_R15
BAD16	69	AD_R16
BAD17	68	AD_R17
BAD18	67	AD_R18
BAD19	66	AD_R19
BAD20	65	AD_R20
BAD21	64	AD_R21
BAD22	63	AD_R22
BAD23	61	AD_R23
BAD24	59	AD_R24
BAD25	58	AD_R25
BAD26	57	AD_R26
BAD27	56	AD_R27
BAD28	55	AD_R28
BAD29	54	AD_R29
BAD30	53	AD_R30
BAD31	52	AD_R31
BAD32	49	AD_R32
BAD33	48	AD_R33
BAD34	47	AD_R34
BAD35	46	AD_R35
BAD36	45	AD_R36
BAD37	44	AD_R37
BAD38	43	AD_R38
BAD39	42	AD_R39
BAD40	39	AD_R40
BAD41	38	AD_R41
BAD42	37	AD_R42
BAD43	36	AD_R43
BAD44	35	AD_R44
BAD45	34	AD_R45
BAD46	33	AD_R46
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BAD49	26	AD_R49
BAD50	25	AD_R50
BAD51	24	AD_R51
BAD52	23	AD_R52
BAD53	22	AD_R53
BAD54	21	AD_R54
BAD55	20	AD_R55
BAD56	18	AD_R56
BAD57	17	AD_R57
BAD58	15	AD_R58
BAD59	14	AD_R59
BAD60	13	AD_R60
BAD61	12	AD_R61
BAD62	11	AD_R62
BAD63	10	AD_R63

AD\_R[63:0]

SADP3\_[7:0]

SADP3_0	101	PADC0
SADP3_1	111	PADC1
SADP3_2	121	PADC2
SADP3_3	131	PADC3
SADP3_4	140	PADC4
SADP3_5	152	PADC5
SADP3_6	162	PADC6
SADP3_7	172	PADC7

BADC0	80	ADP_R0
BADC1	76	ADP_R1
BADC2	60	ADP_R2
BADC3	50	ADP_R3
BADC4	41	ADP_R4
BADC5	29	ADP_R5
BADC6	19	ADP_R6
BADC7	9	ADP_R7

ADP\_R[7:0]

SCMD3\_[8:0]

SCMD3_0	173	PCMD0
SCMD3_1	174	PCMD1
SCMD3_2	175	PCMD2
SCMD3_3	177	PCMD3
SCMD3_4	178	PCMD4
SCMD3_5	179	PCMD5
SCMD3_6	180	PCMD6
SCMD3_7	181	PCMD7
SCMD3_8	182	PCMD8
SCMDP	183	PCMDP

BCMD0	8	CMD_R0
BCMD1	7	CMD_R1
BCMD2	6	CMD_R2
BCMD3	4	CMD_R3
BCMD4	3	CMD_R4
BCMD5	2	CMD_R5
BCMD6	1	CMD_R6
BCMD7	240	CMD_R7
BCMDP	239	

CMD\_R[7:0]

[10,12] SCMDP3


[10]	/VALOUT3	197
[10]	/RELEASE3	198
	VDD	199
[15]	/VALIN_G3	184
[10]	/EXTRO3	185
[15]	/RDRDY_G3	186
[15]	/WRRDY_G3	188
[15]	/VDACK_G3	190
[15]	/IVERR_G3	203
[10]	/RCLK3_0	204
[10]	/TCLK3_0	200
[12]	/EXTRO_L3	191
[12]	/RELEASE_L3	201
[14]	TREF	202
[2]	/PCHKEN	207
	GND	192
		193
		194
[13]	LED3_0	195
[13]	LED3_1	209
	VDD	208

VALIN	197
RELS	198
INTFREQ	199
VALOUT	184
EXTRO	185
RDRDY	186
WRRDY	188
IVDACK	190
IVERR	203
TCLK	204
SLVREQ	200
SLVACK	191
TREF	201
PCHKEN	202
OMODE	207
INTRO	192
INTR1	193
LAMP0	194
LAMP1	195
SUBPOS0	209
SUBPOS1	208

CA302

AVIN	237
AVOUT	235
DVIN	236
BUSYOUT	226
SHRDIN	234
SHRDOUT	225
INTVIN	233
TACK	224
INTVOUT	231
TACK	223
BPERR	230
SNPHIT	221
BOOT	229
BAREQ	228
BAGRANT	227
RESPT	222
BRCLK	217
BTCLK	218
LOCAL	216
POS0	215
POS1	214
POS2	213
POS3	212

AVAIL_R	[2,5,8,17,18,22,56,68]
DVAL_R	[2,5,8,17,18,22,48,56,68]
BUSY_R	[44,47,58]
/BUSY_OUT3	[16,44]
SHRD_R	[22,58]
/SHRD_OUT3	[16]
INTV_R	[47,58]
/INTV_OUT3	[16,24]
TACK_R	[47,58]
/PERR3	[16]
SNPHIT3	[24]
BOOT3	[44]
BAREQ3	[20]
BAGRANT3	[20]
SRE3	[10,40]
BRCLK	[53]
CLK5	[53]
GND	
ID0	[65]
ID1	[65]
ID2	[65]
ID3	[65]

		Dansk Data Elektronik A/S	
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Issue 1		Global agent 3	
Issue 2			
Issue 3		File: cpu301	Page:11 of 72

SAD3\_[63:0]

SAD3_0	92	PAD0
SAD3_1	93	PAD1
SAD3_2	94	PAD2
SAD3_3	95	PAD3
SAD3_4	96	PAD4
SAD3_5	98	PAD5
SAD3_6	99	PAD6
SAD3_7	100	PAD7
SAD3_8	102	PAD8
SAD3_9	103	PAD9
SAD3_10	104	PAD10
SAD3_11	105	PAD11
SAD3_12	106	PAD12
SAD3_13	107	PAD13
SAD3_14	109	PAD14
SAD3_15	110	PAD15
SAD3_16	112	PAD16
SAD3_17	113	PAD17
SAD3_18	114	PAD18
SAD3_19	115	PAD19
SAD3_20	116	PAD20
SAD3_21	117	PAD21
SAD3_22	118	PAD22
SAD3_23	120	PAD23
SAD3_24	122	PAD24
SAD3_25	123	PAD25
SAD3_26	124	PAD26
SAD3_27	125	PAD27
SAD3_28	126	PAD28
SAD3_29	127	PAD29
SAD3_30	128	PAD30
SAD3_31	129	PAD31
SAD3_32	132	PAD32
SAD3_33	133	PAD33
SAD3_34	134	PAD34
SAD3_35	135	PAD35
SAD3_36	136	PAD36
SAD3_37	137	PAD37
SAD3_38	138	PAD38
SAD3_39	139	PAD39
SAD3_40	142	PAD40
SAD3_41	143	PAD41
SAD3_42	144	PAD42
SAD3_43	145	PAD43
SAD3_44	146	PAD44
SAD3_45	147	PAD45
SAD3_46	148	PAD46
SAD3_47	149	PAD47
SAD3_48	153	PAD48
SAD3_49	155	PAD49
SAD3_50	156	PAD50
SAD3_51	157	PAD51
SAD3_52	158	PAD52
SAD3_53	159	PAD53
SAD3_54	160	PAD54
SAD3_55	161	PAD55
SAD3_56	163	PAD56
SAD3_57	164	PAD57
SAD3_58	166	PAD58
SAD3_59	167	PAD59
SAD3_60	168	PAD60
SAD3_61	169	PAD61
SAD3_62	170	PAD62
SAD3_63	171	PAD63

U8

BAD0	89	LAD_R0
BAD1	88	LAD_R1
BAD2	87	LAD_R2
BAD3	86	LAD_R3
BAD4	85	LAD_R4
BAD5	83	LAD_R5
BAD6	82	LAD_R6
BAD7	81	LAD_R7
BAD8	79	LAD_R8
BAD9	78	LAD_R9
BAD10	77	LAD_R10
BAD11	76	LAD_R11
BAD12	75	LAD_R12
BAD13	74	LAD_R13
BAD14	72	LAD_R14
BAD15	71	LAD_R15
BAD16	69	LAD_R16
BAD17	68	LAD_R17
BAD18	67	LAD_R18
BAD19	66	LAD_R19
BAD20	65	LAD_R20
BAD21	64	LAD_R21
BAD22	63	LAD_R22
BAD23	61	LAD_R23
BAD24	59	LAD_R24
BAD25	58	LAD_R25
BAD26	57	LAD_R26
BAD27	56	LAD_R27
BAD28	55	LAD_R28
BAD29	54	LAD_R29
BAD30	53	LAD_R30
BAD31	52	LAD_R31
BAD32	49	LAD_R32
BAD33	48	LAD_R33
BAD34	47	LAD_R34
BAD35	46	LAD_R35
BAD36	45	LAD_R36
BAD37	44	LAD_R37
BAD38	43	LAD_R38
BAD39	42	LAD_R39
BAD40	39	LAD_R40
BAD41	38	LAD_R41
BAD42	37	LAD_R42
BAD43	36	LAD_R43
BAD44	35	LAD_R44
BAD45	34	LAD_R45
BAD46	33	LAD_R46
BAD47	32	LAD_R47
BAD48	28	LAD_R48
BAD49	26	LAD_R49
BAD50	25	LAD_R50
BAD51	24	LAD_R51
BAD52	23	LAD_R52
BAD53	22	LAD_R53
BAD54	21	LAD_R54
BAD55	20	LAD_R55
BAD56	18	LAD_R56
BAD57	17	LAD_R57
BAD58	15	LAD_R58
BAD59	14	LAD_R59
BAD60	13	LAD_R60
BAD61	12	LAD_R61
BAD62	11	LAD_R62
BAD63	10	LAD_R63

LAD\_R[63:0]

SADP3\_[7:0]

SADP3_0	101	PADC0
SADP3_1	111	PADC1
SADP3_2	121	PADC2
SADP3_3	131	PADC3
SADP3_4	140	PADC4
SADP3_5	152	PADC5
SADP3_6	162	PADC6
SADP3_7	172	PADC7

U8

BADC0	80	LADP_R0
BADC1	70	LADP_R1
BADC2	60	LADP_R2
BADC3	50	LADP_R3
BADC4	41	LADP_R4
BADC5	29	LADP_R5
BADC6	19	LADP_R6
BADC7	9	LADP_R7

LADP\_R[7:0]

SCMD3\_[8:0]

SCMD3_0	173	PCMD0
SCMD3_1	174	PCMD1
SCMD3_2	175	PCMD2
SCMD3_3	177	PCMD3
SCMD3_4	178	PCMD4
SCMD3_5	179	PCMD5
SCMD3_6	180	PCMD6
SCMD3_7	181	PCMD7
SCMD3_8	182	PCMD8
SCMDP3	183	PCMDP

U8

BCMD0	8	LCMD_R0
BCMD1	7	LCMD_R1
BCMD2	6	LCMD_R2
BCMD3	4	LCMD_R3
BCMD4	3	LCMD_R4
BCMD5	2	LCMD_R5
BCMD6	1	LCMD_R6
BCMD7	240	LCMD_R7
BCMDP	239	LCMDP_R

LCMD\_R[7:0]

[10,11] SCMDP3

[10] /VALOUT3

[11] /RELEASE\_L3

VDD

[15] /VALIN\_L3

[11] /EXTREQ\_L3

[15] /RDRDY\_L3

[15] /WRRDY\_L3

[15] /IVDACK\_L3

[15] /IVDERR\_L3

[10] RCLK3\_1

[10] /RCLK3\_1

GND

[2] /PCHKEN

GND

[13] LED3\_2

[13] LED3\_3

VDD

VDD

197 VALIN

198 RELS

199 INPREG

184 VALOUT

185 EXTREQ

186 RDRDY

188 WRRDY

189 IVDACK

190 IVERR

203 RCLK

204 /RCLK

200 SLVREQ

191 SLVACK

201 TREF

202 PCHKEN

207 ICMODE

192 INTR0

193 INTR1

194 LAMP0

195 LAMP1

209 SUBPOS0

208 SUBPOS1

CA302

237 AVIN

238 AVOUT

235 DVIN

236 DVOUT

226

234 BUSYIN

225 SHRDIN

233 SHRDOUT

224 INTVIN

223 INTVOUT

223 TACK

230 BPERK3

221 SNPHIT

229 BOOT

228 BAREQ

227 BAGRANT

222 BRCLK

218 BRCLK

216 LOCAL

215 POS0

214 POS1

213 POS2

212 POS3

LAVAL\_R [3,6,9,17,18,25,61,69]

LDVAL\_R [3,6,9,17,18,25,52,61,69]

LBUSY\_R [50,63]

LEXTREQ [16]

LSHRD\_R [25,63]

LSHRD\_OUT3 [16]

LINTV\_R [50,63]

LINTV\_OUT3 [16,27]

LTACK\_R [50,63]

LPERR3 [16]

LSPHIT3 [27]

LBAREQ3 [21]

LBAGRANT3 [21]

SRE3 [10,40]

BRCLK [53]


CLK5 [53]

ID0 [65]

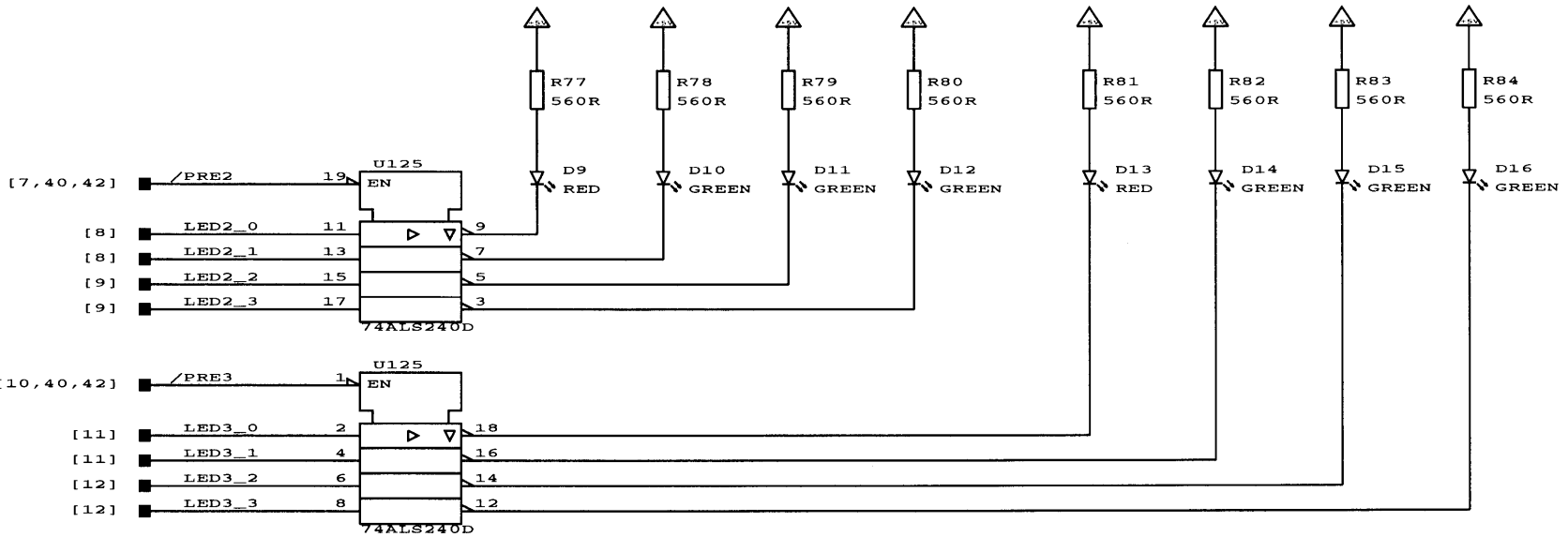
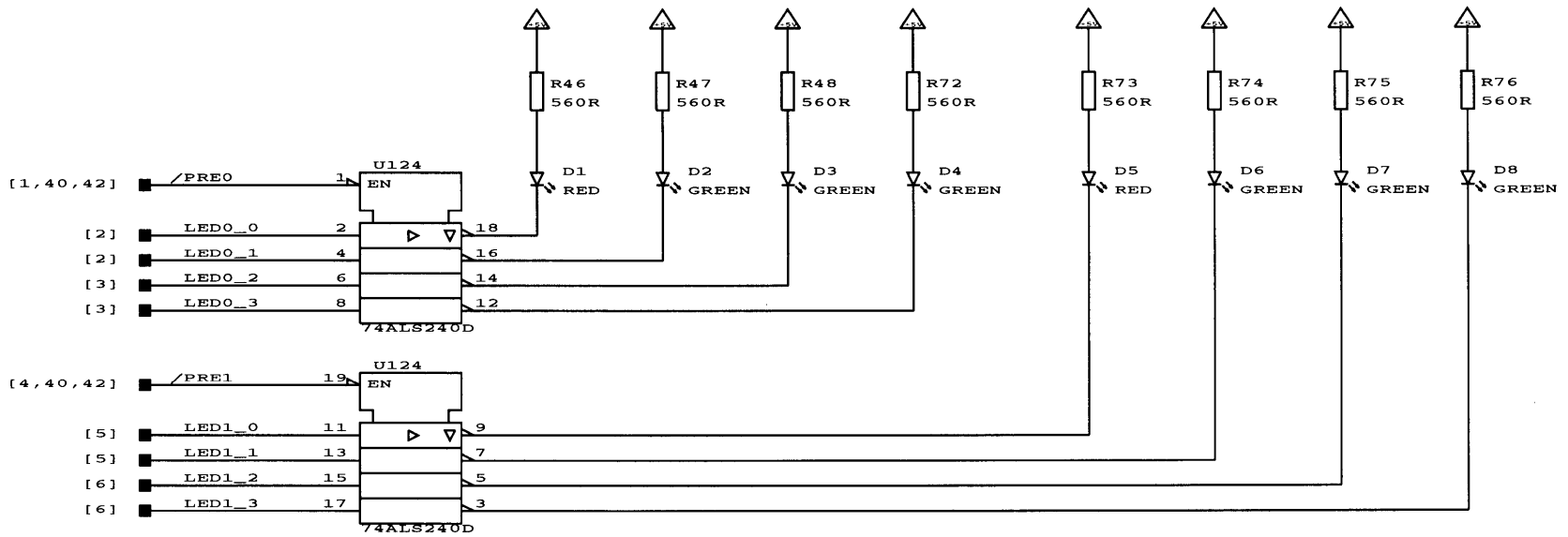
ID1 [65]

ID2 [65]

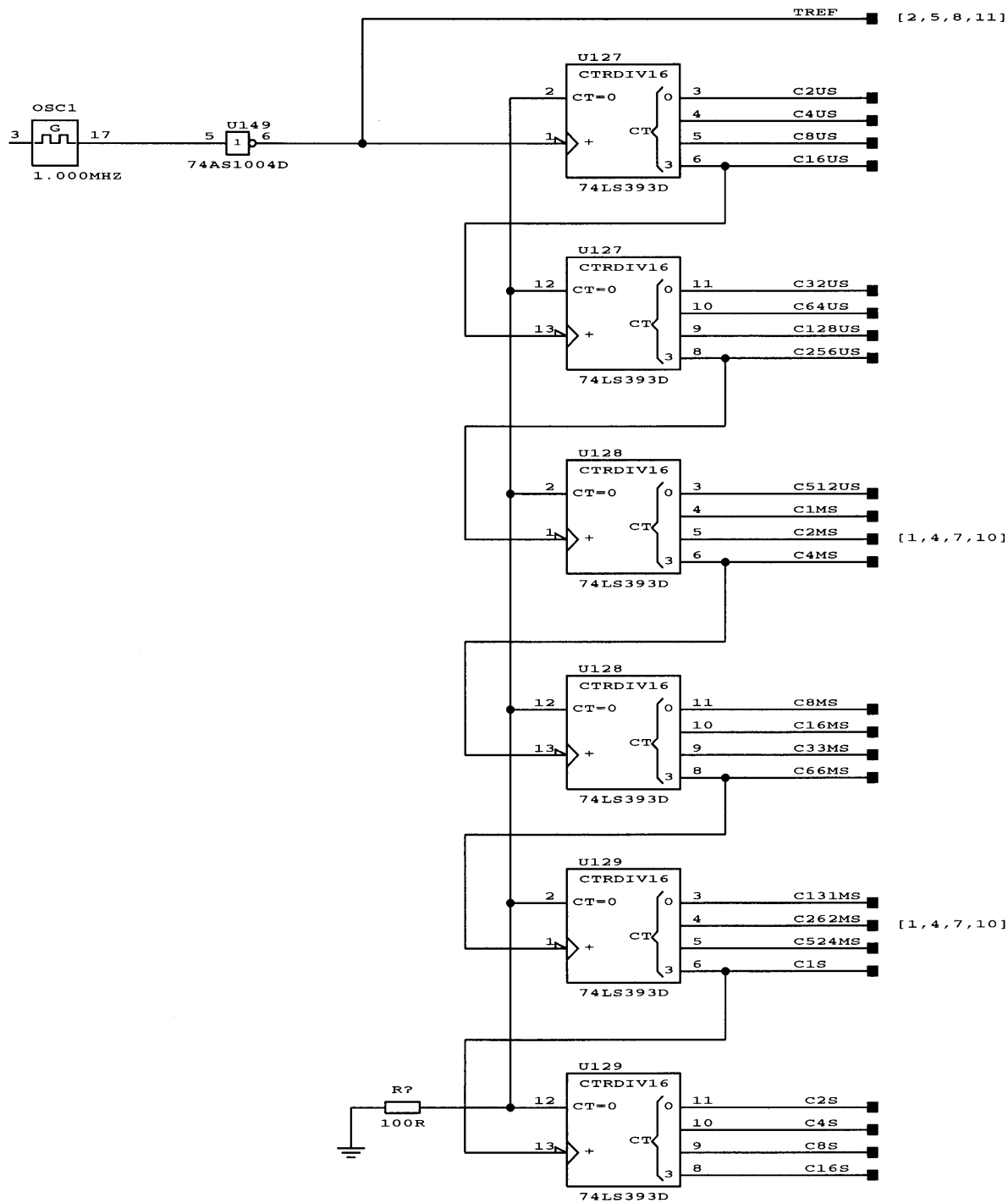
ID3 [65]


		Dansk Data Elektronik A/S	
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Issue 2			
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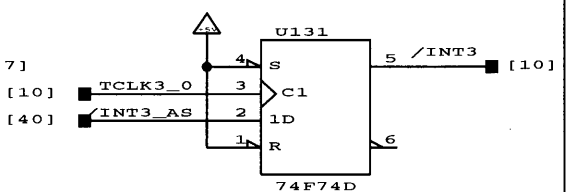
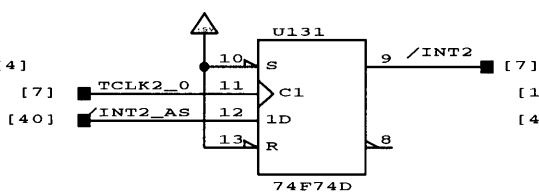
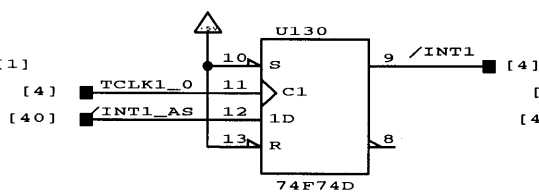
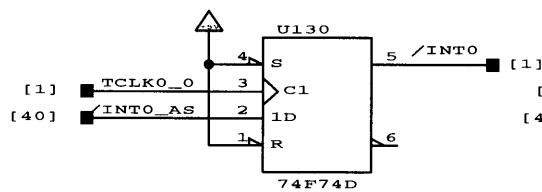
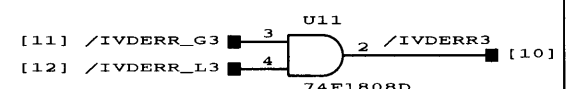
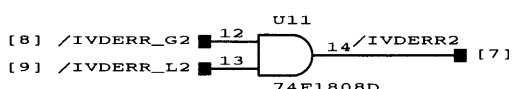
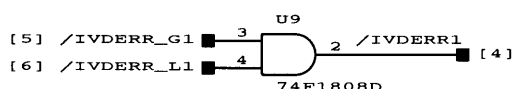
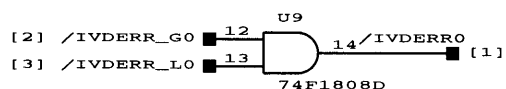
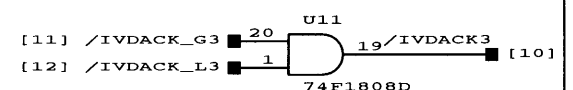
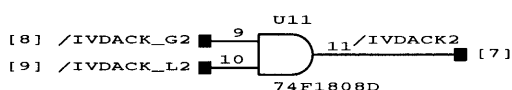
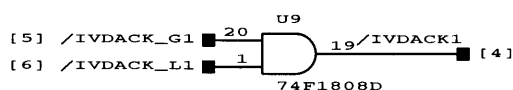
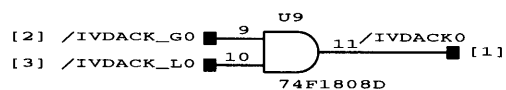
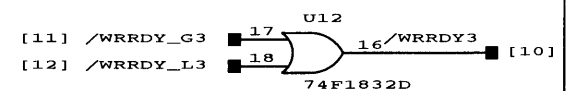
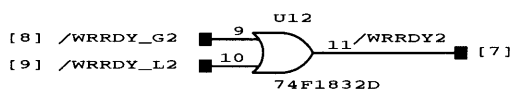
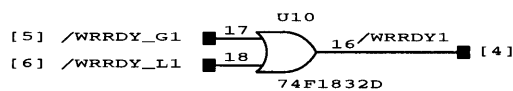
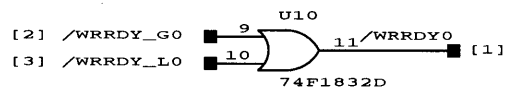
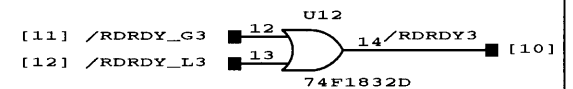
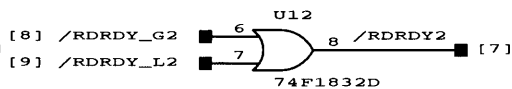
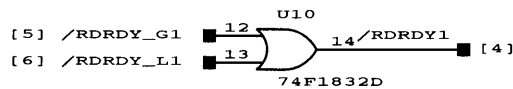
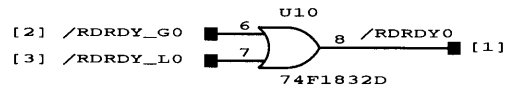
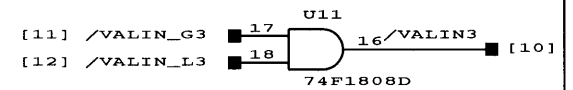
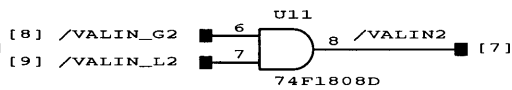
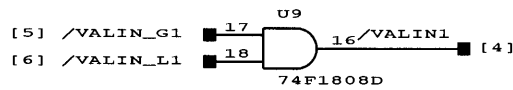
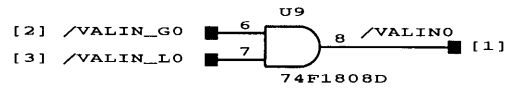




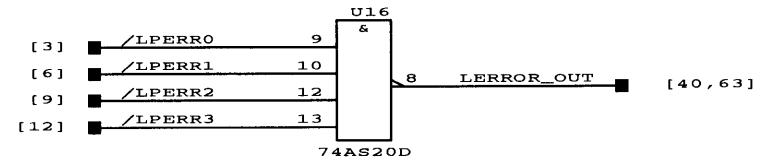
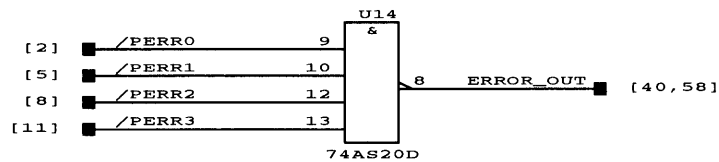
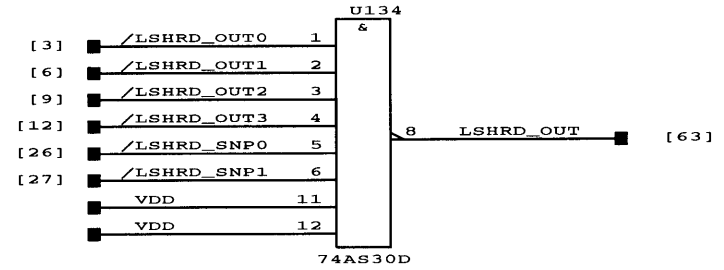
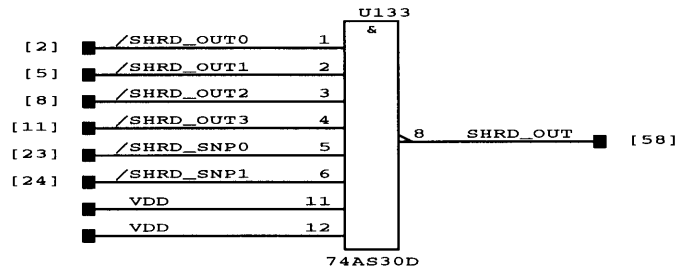
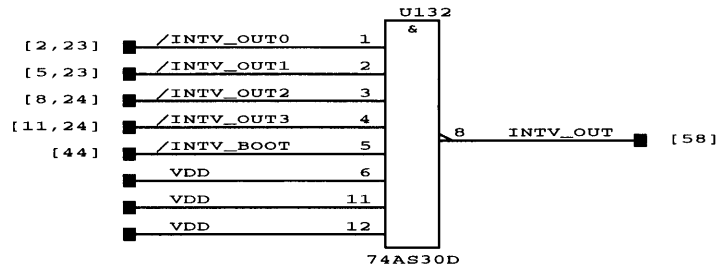
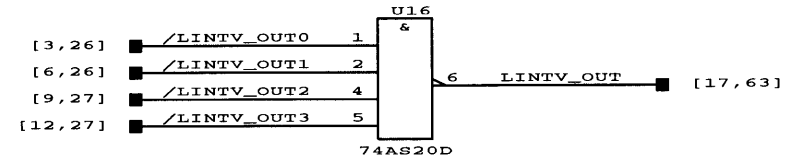
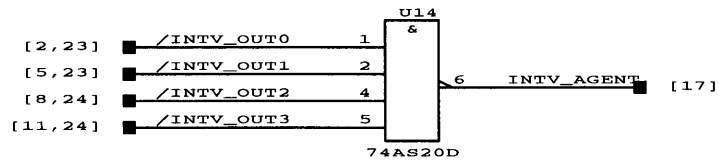
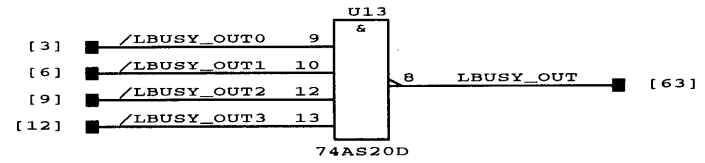
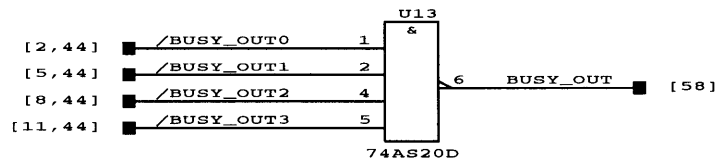
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Issue 0	940811	CPU301 Module Programmable LEDs	
Issue 1			
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Issue 3		File: cpu301	Page: 13 of 72

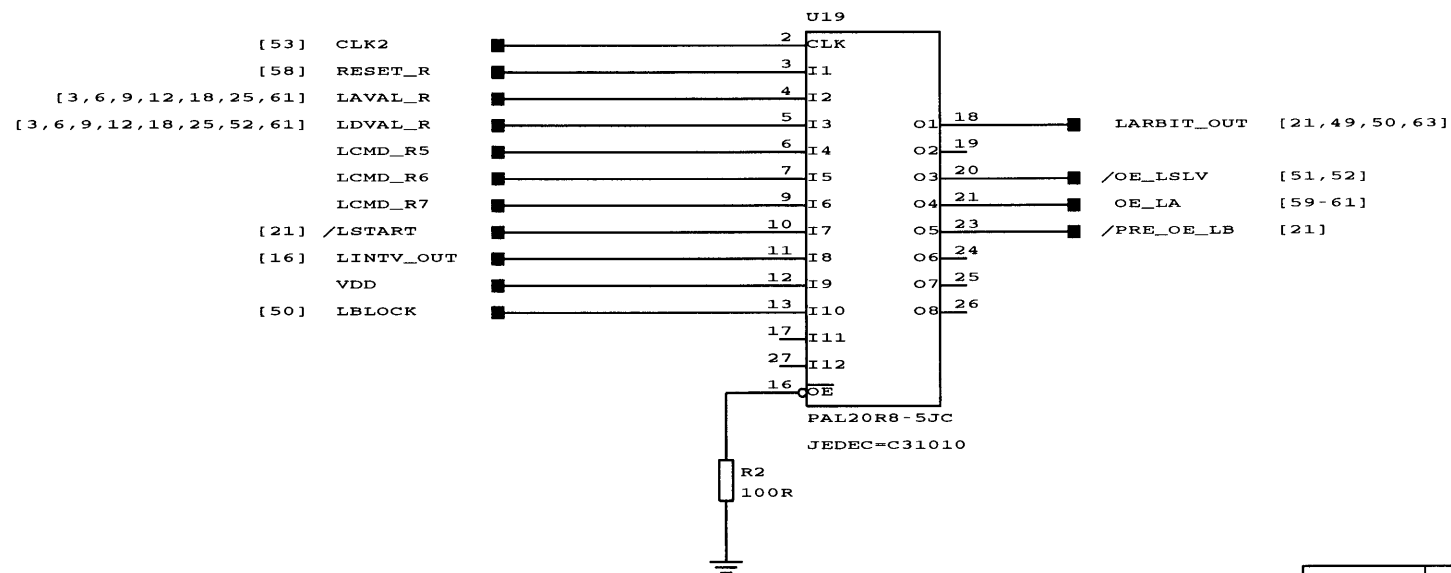
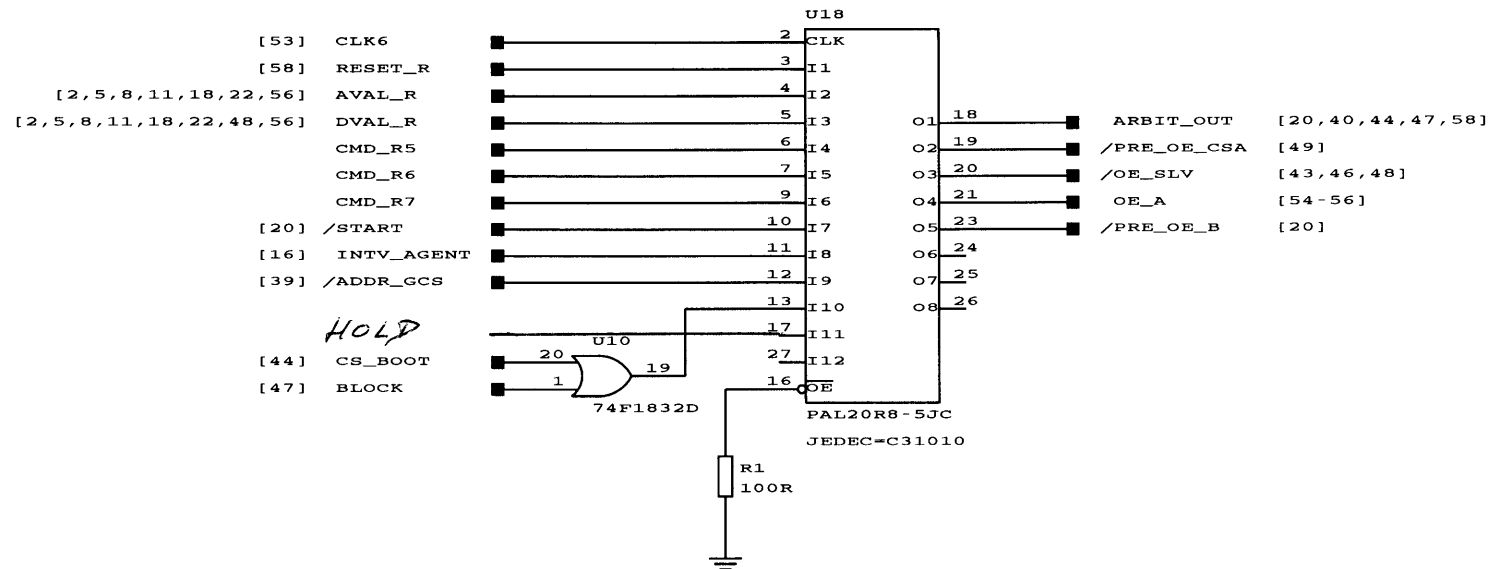


	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Reset counters
Issue 2		
Issue 3		
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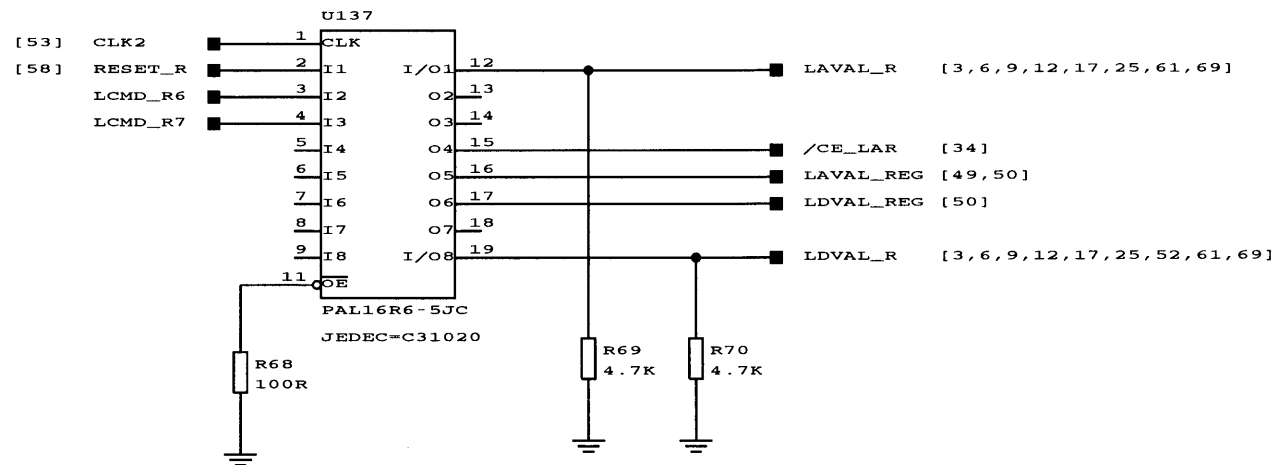
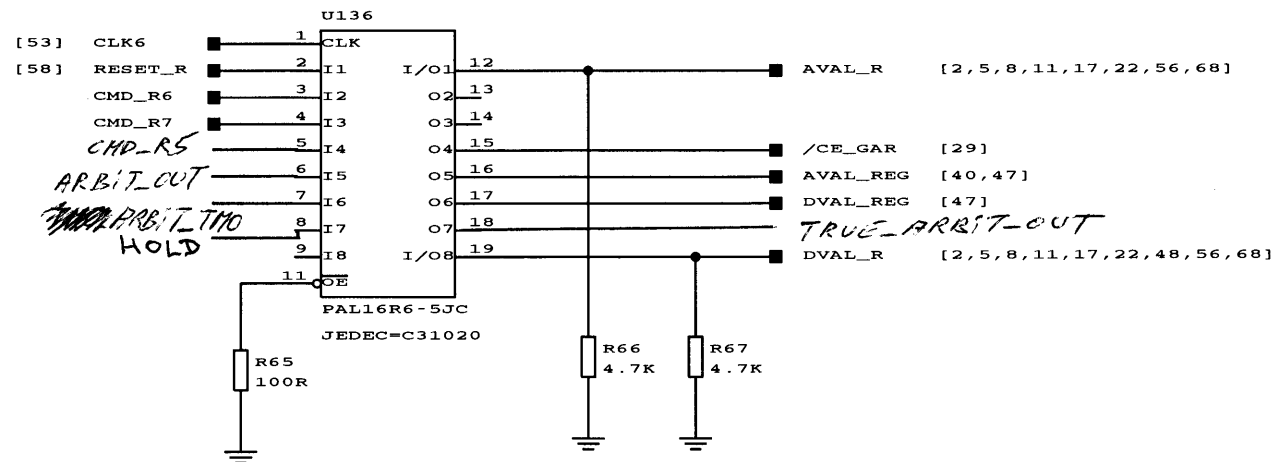


		Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module Gating towards processors	
Issue 1			
Issue 2			
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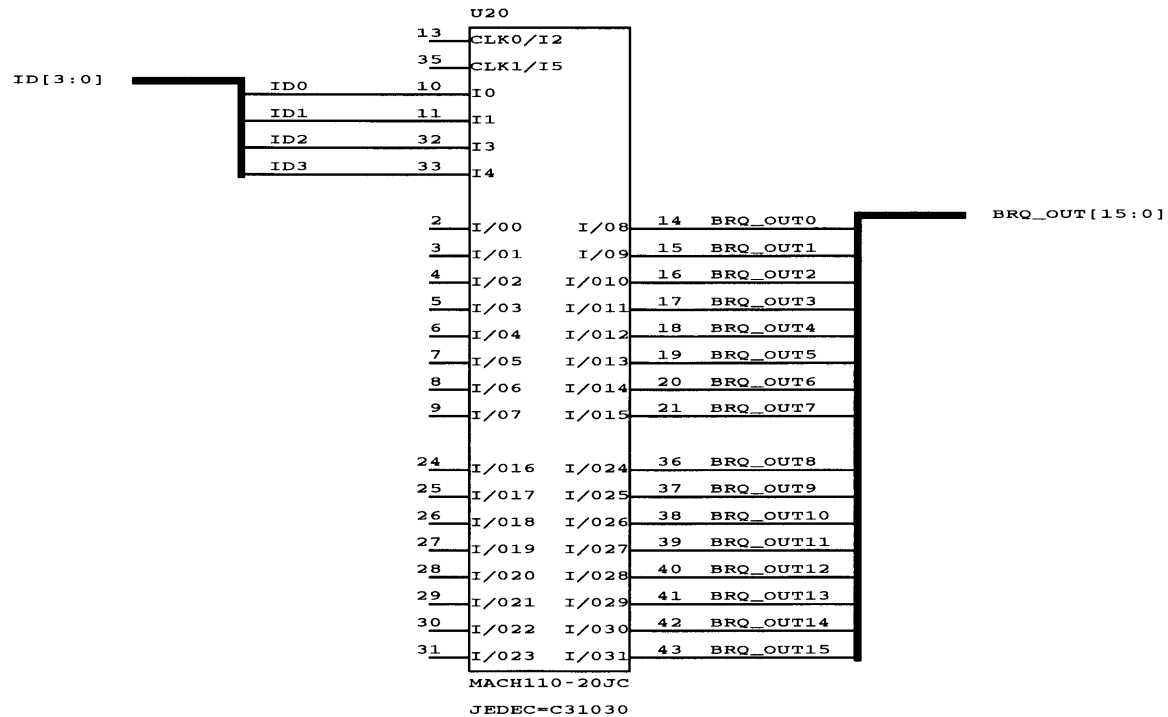





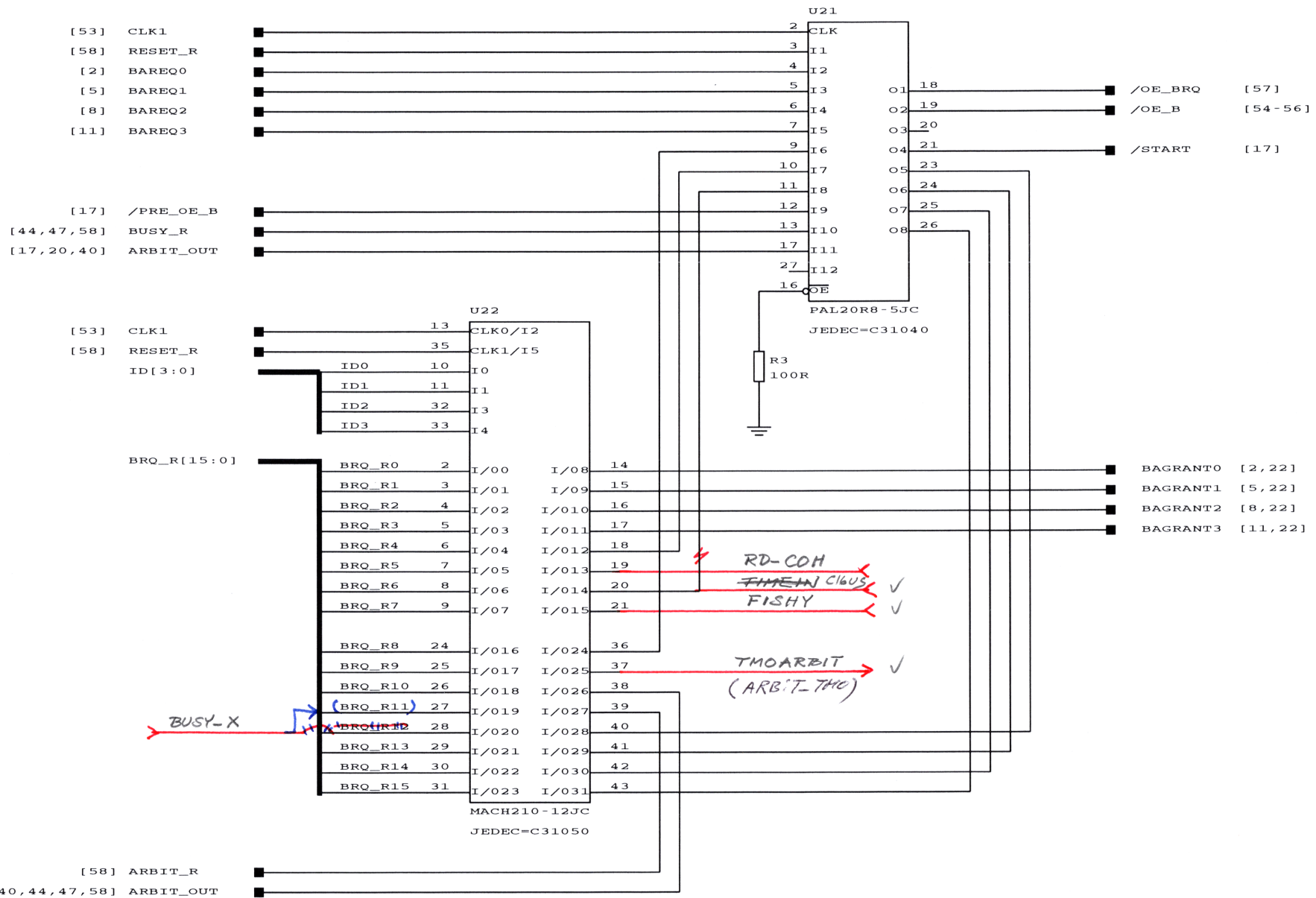
	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Global and local
Issue 2		output enable control
Issue 3		File: cpu301 Page:17 of 72



	Dansk Data Elektronik A/S	
Issue 0	940506	CPU301 Module
Issue 1	CHG	Pull-down for
Issue 2		address and data valid
Issue 3		File: cpu301 Page:18 of 72

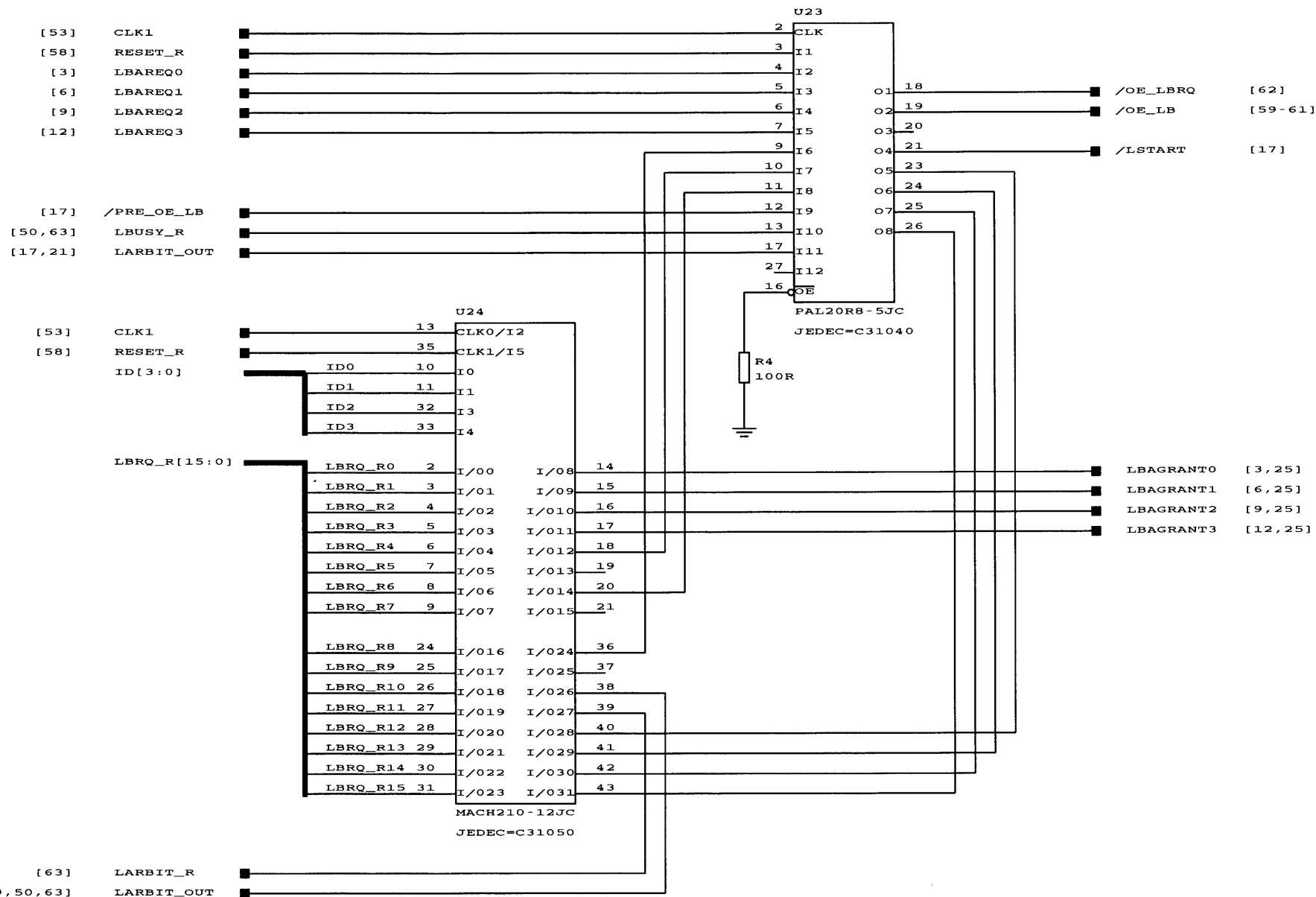


	Dansk Data Elektronik A/S	
Issue 0	940506	CPU301 Module
Issue 1	CHG	Global and local
Issue 2		bus request decoder
Issue 3		File: cpu301 Page:19 of 72

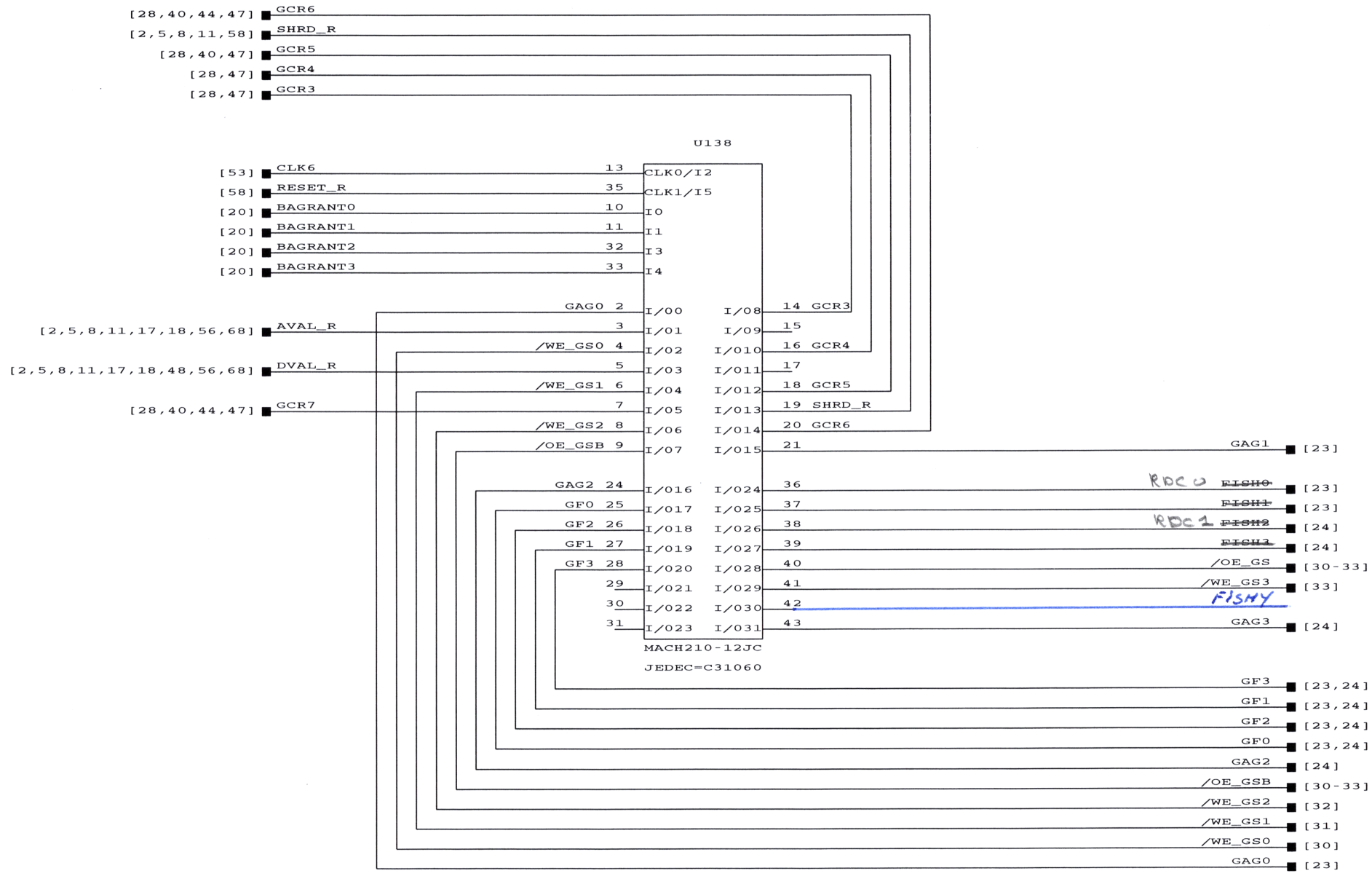


	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Global bus arbitration
Issue 2		
Issue 3		File: cpu301 Page:20 of 72

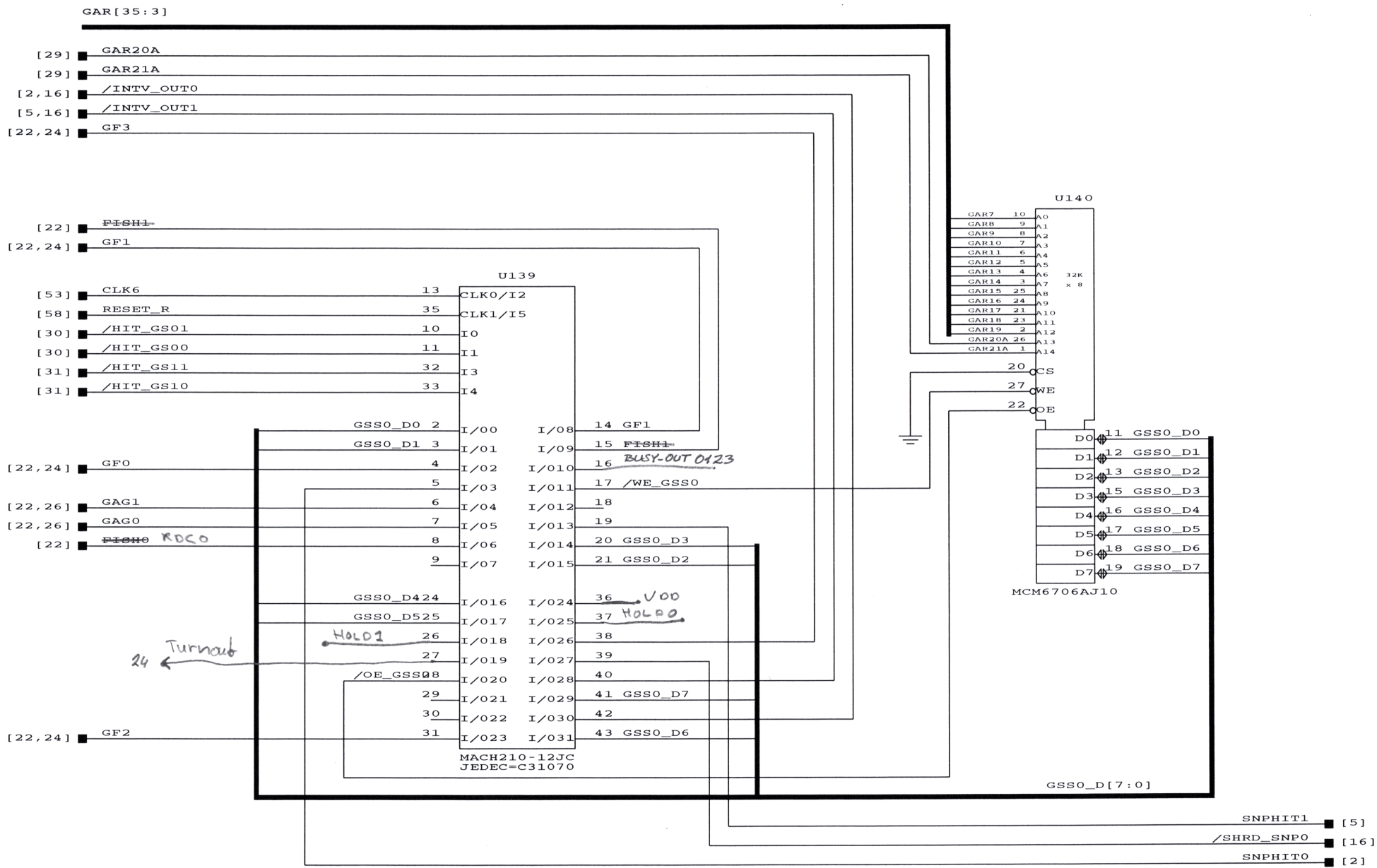




	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Local bus arbitration
Issue 2		
Issue 3		File: cpu301 Page:21 of 72



dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global snooper control
Issue 2		
Issue 3		File: cpu301 Page:22 of 72



24 Turnout

HOLD1

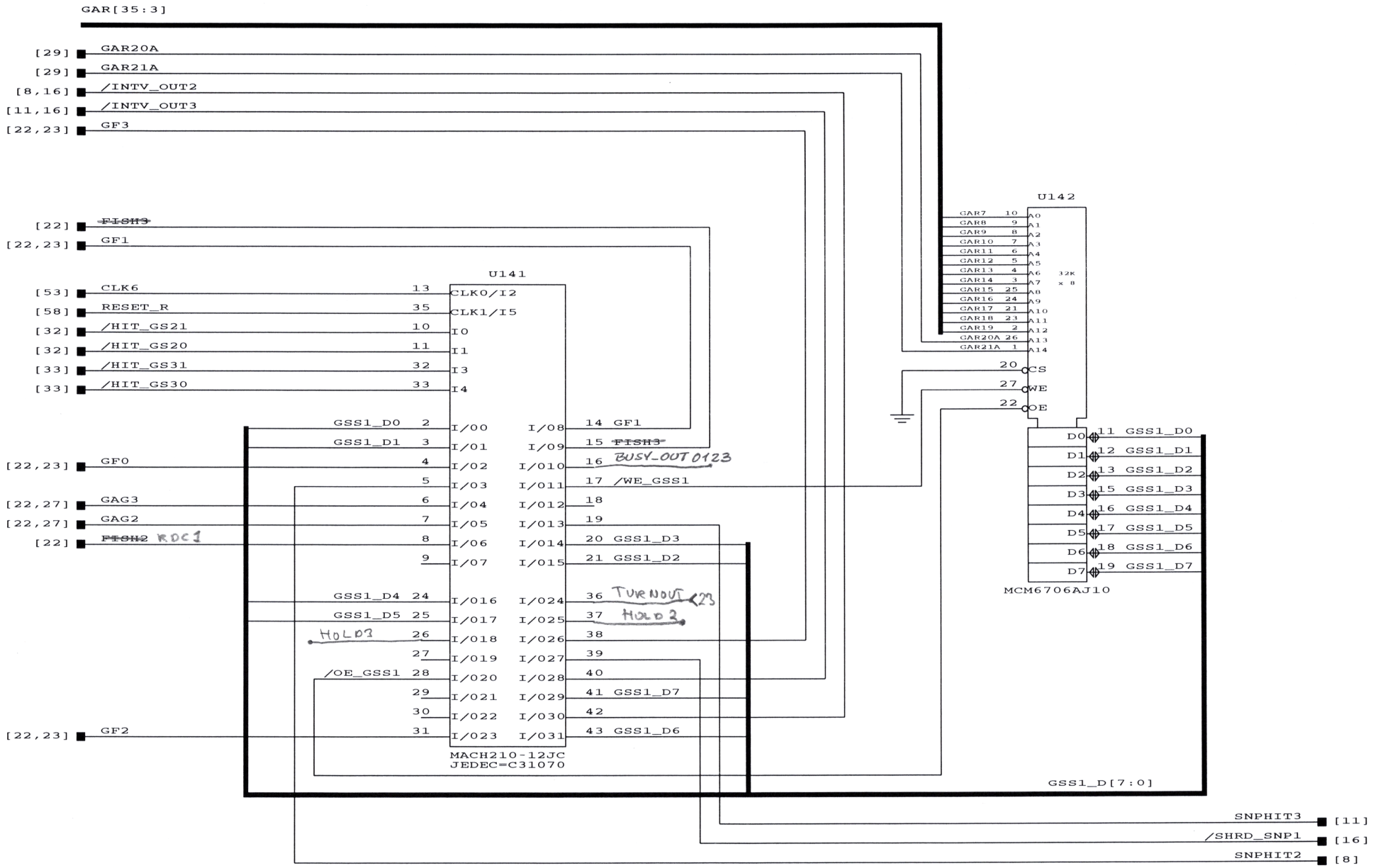
BUSY-OUT 0123

MACH210-12JC  
JEDEC=C31070

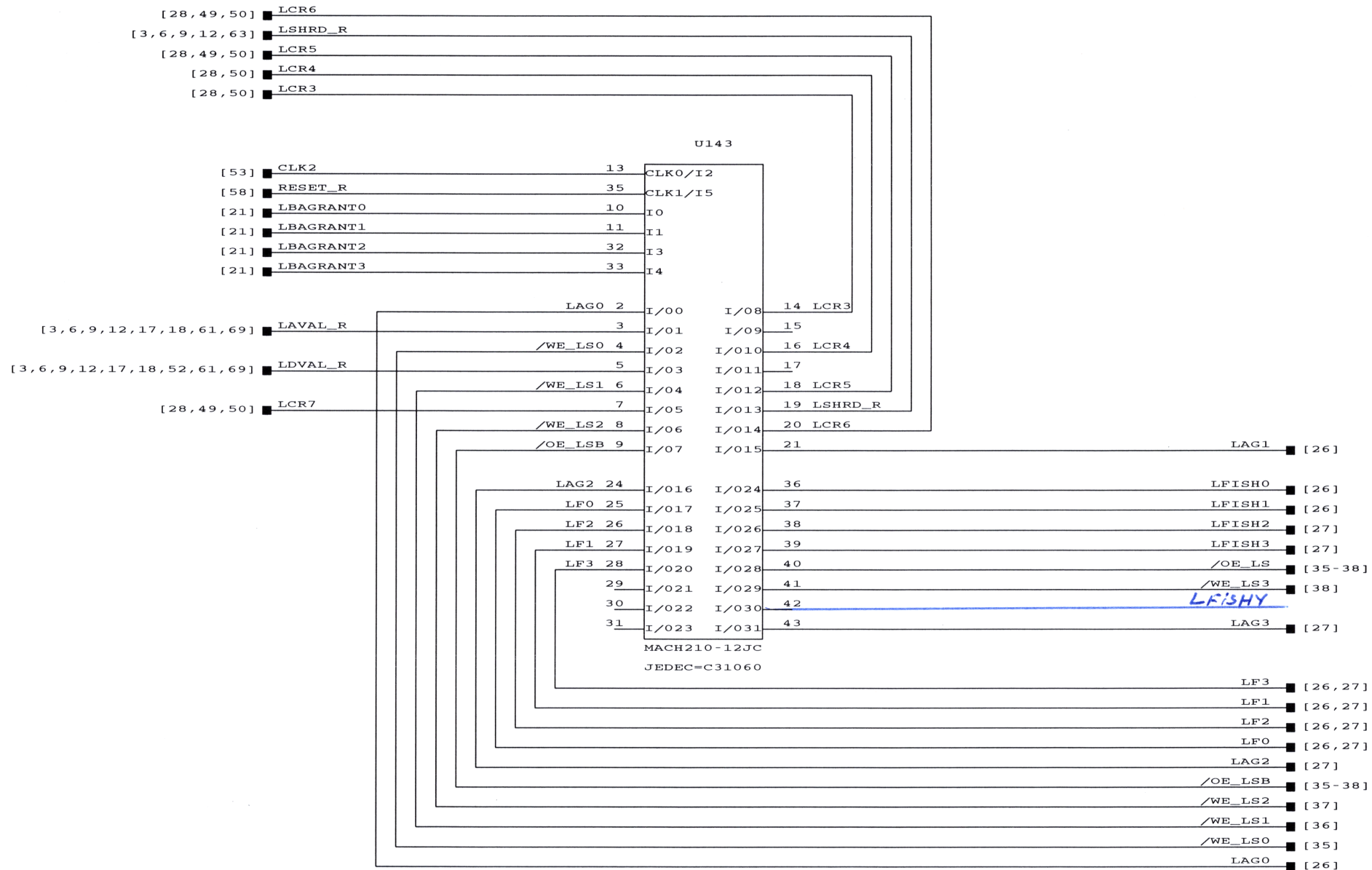
MCM6706AJ10

GSS0\_D[7:0]

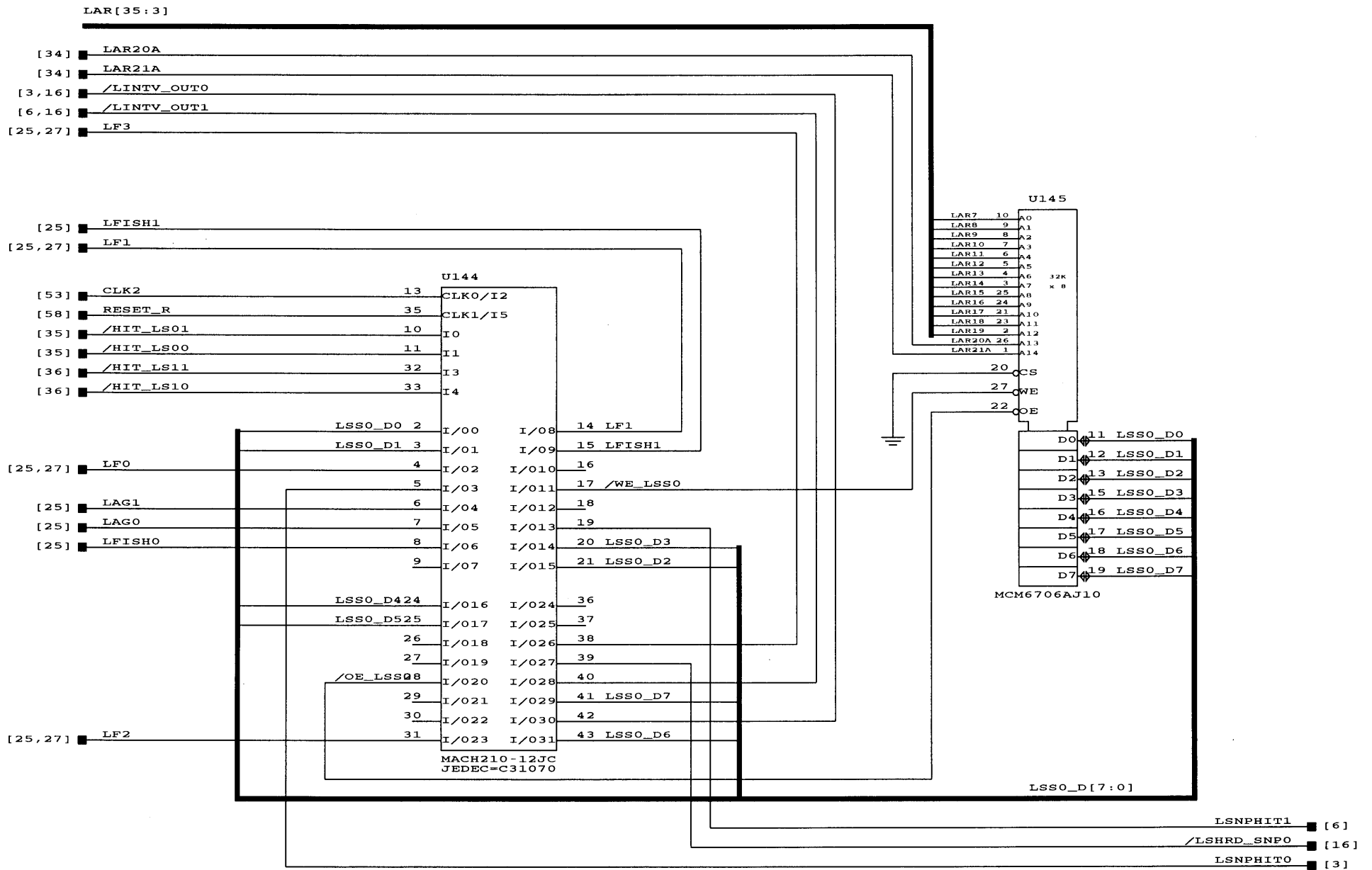
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global Super Snooper 0-1
Issue 2		
Issue 3		File: cpu301 Page: 23 of 72



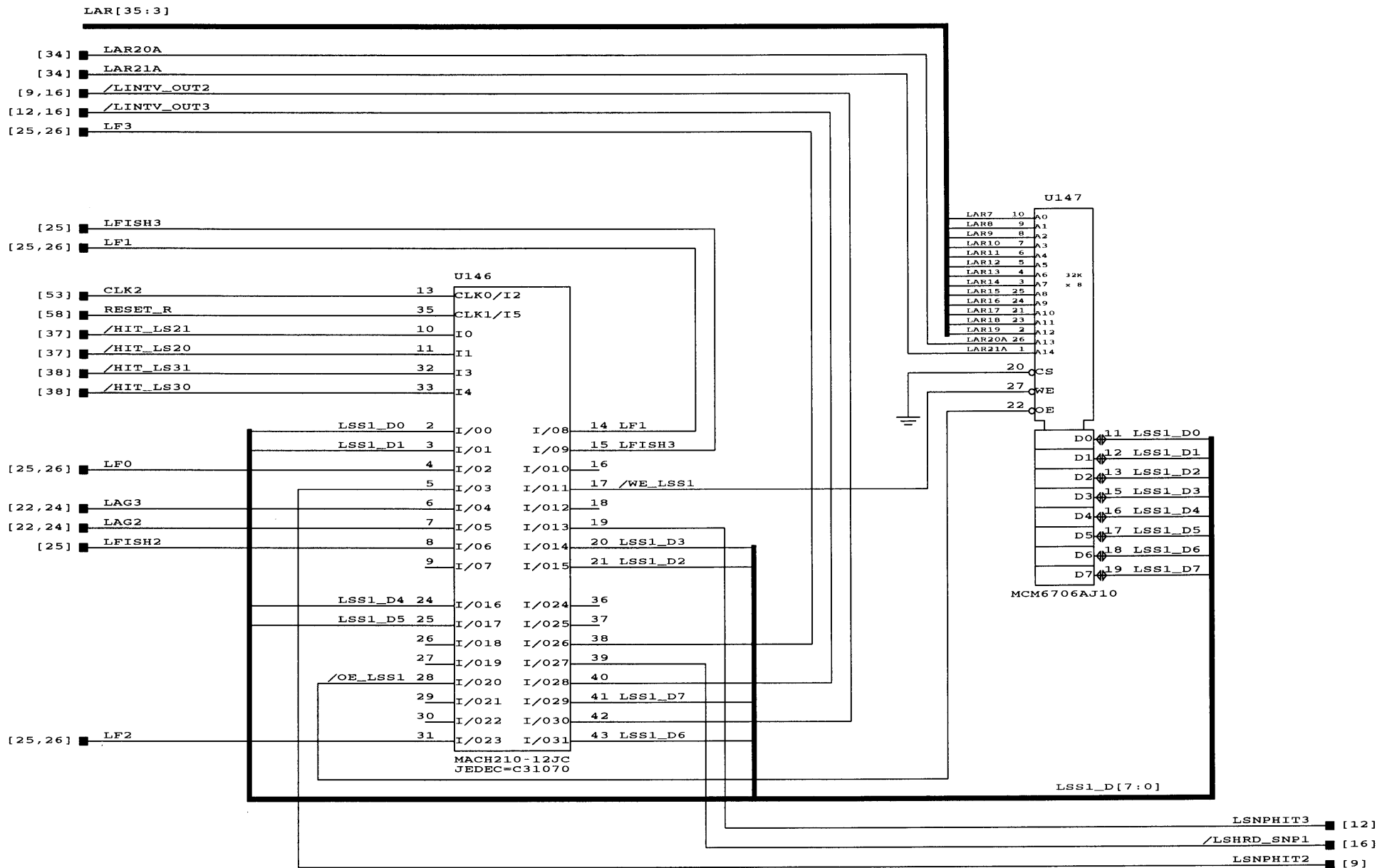
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global Super Snooper 2-3
Issue 2		
Issue 3		File: cpu301 Page:24 of 72



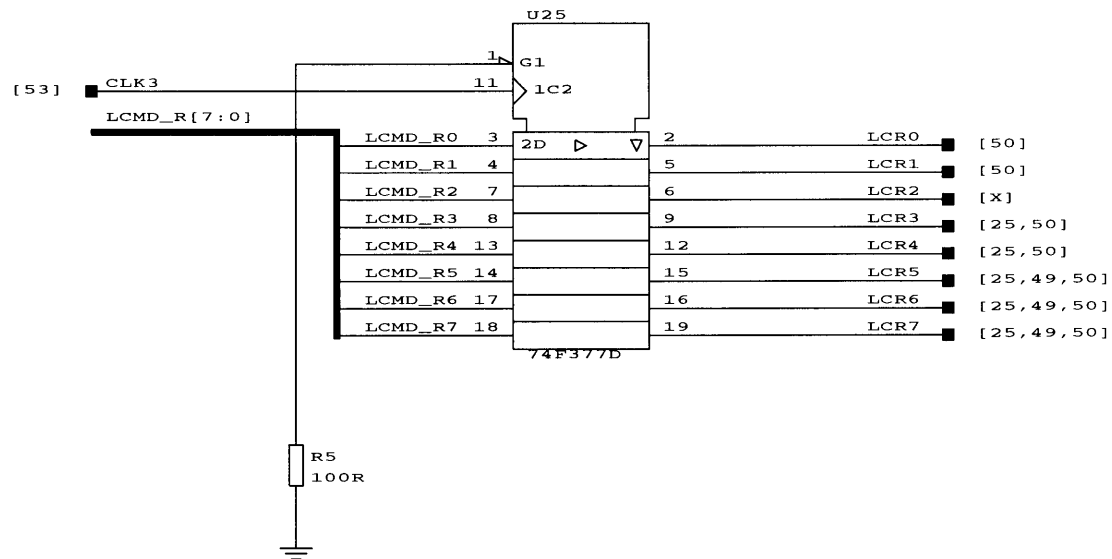
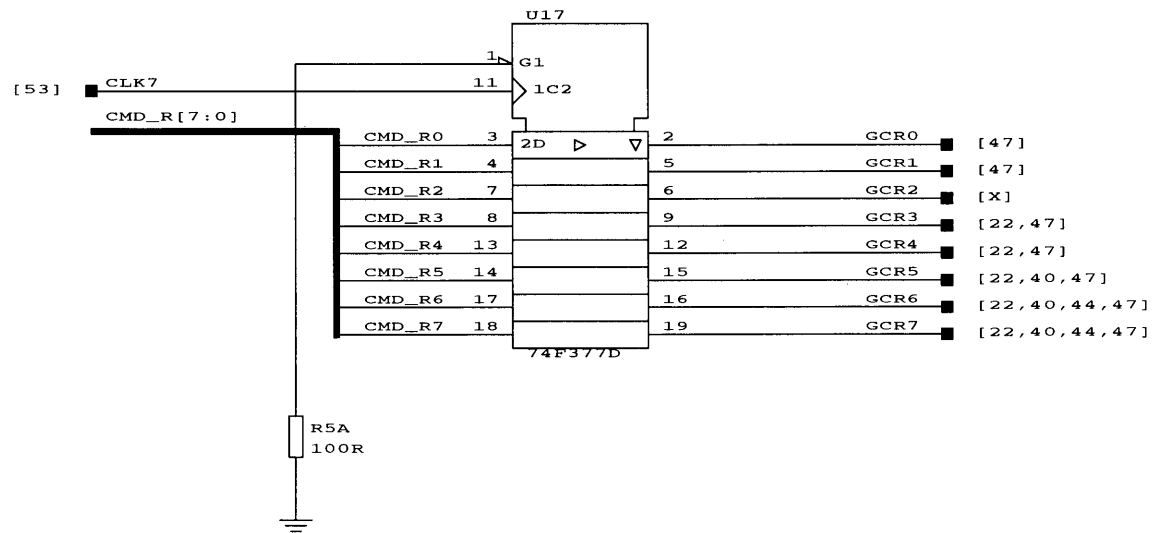
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Local snooper control
Issue 2		
Issue 3		File: cpu301 Page:25 of 72



dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Local Super Snooper 0-1
Issue 2		
Issue 3		File: cpu301 Page:26 of 72

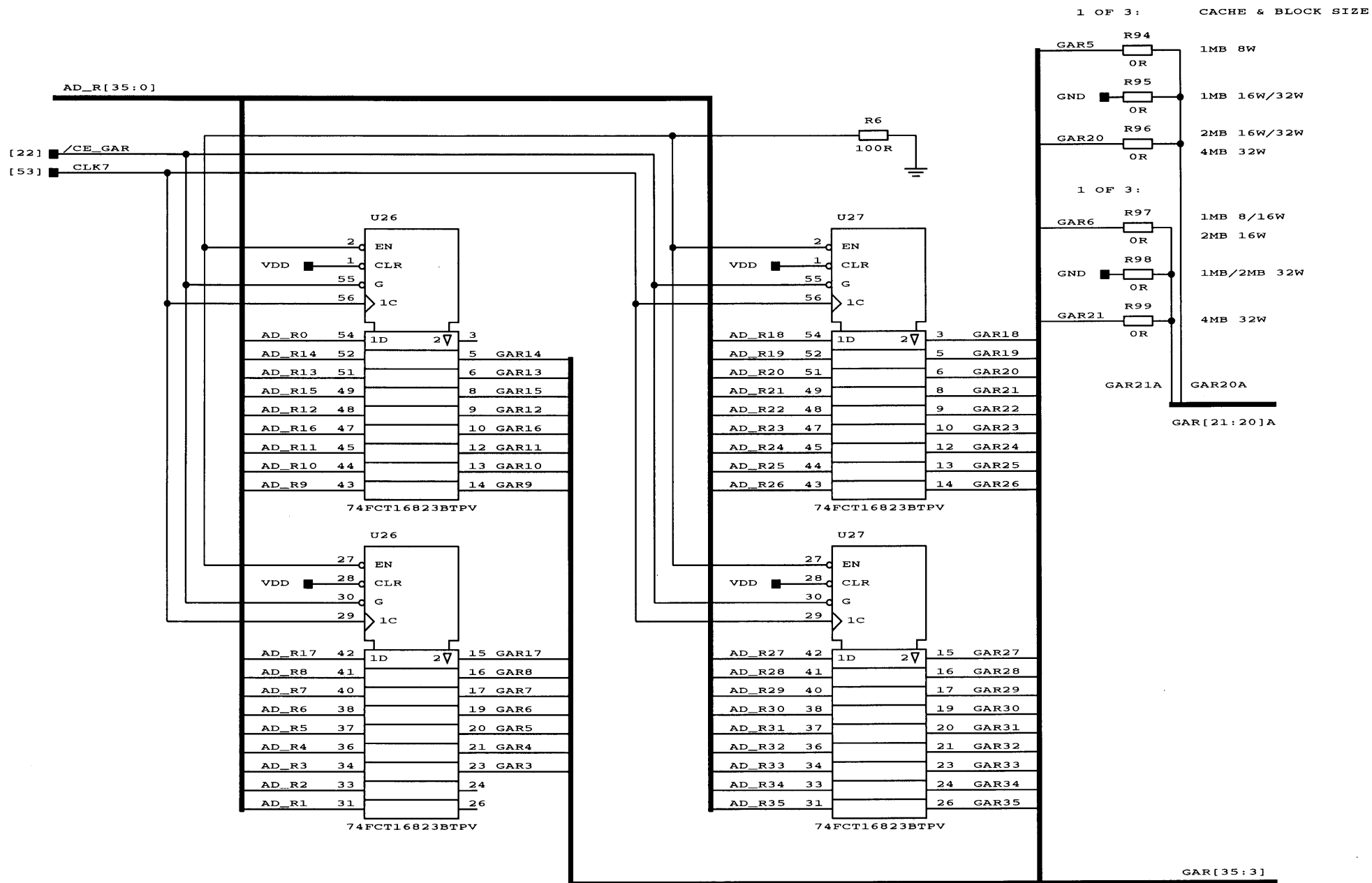


dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Local Super Snooper 2-3
Issue 2		
Issue 3		File: cpu301 Page:27 of 72



dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global and local
Issue 2		command register
Issue 3		File: cpu301 Page:28 of 72





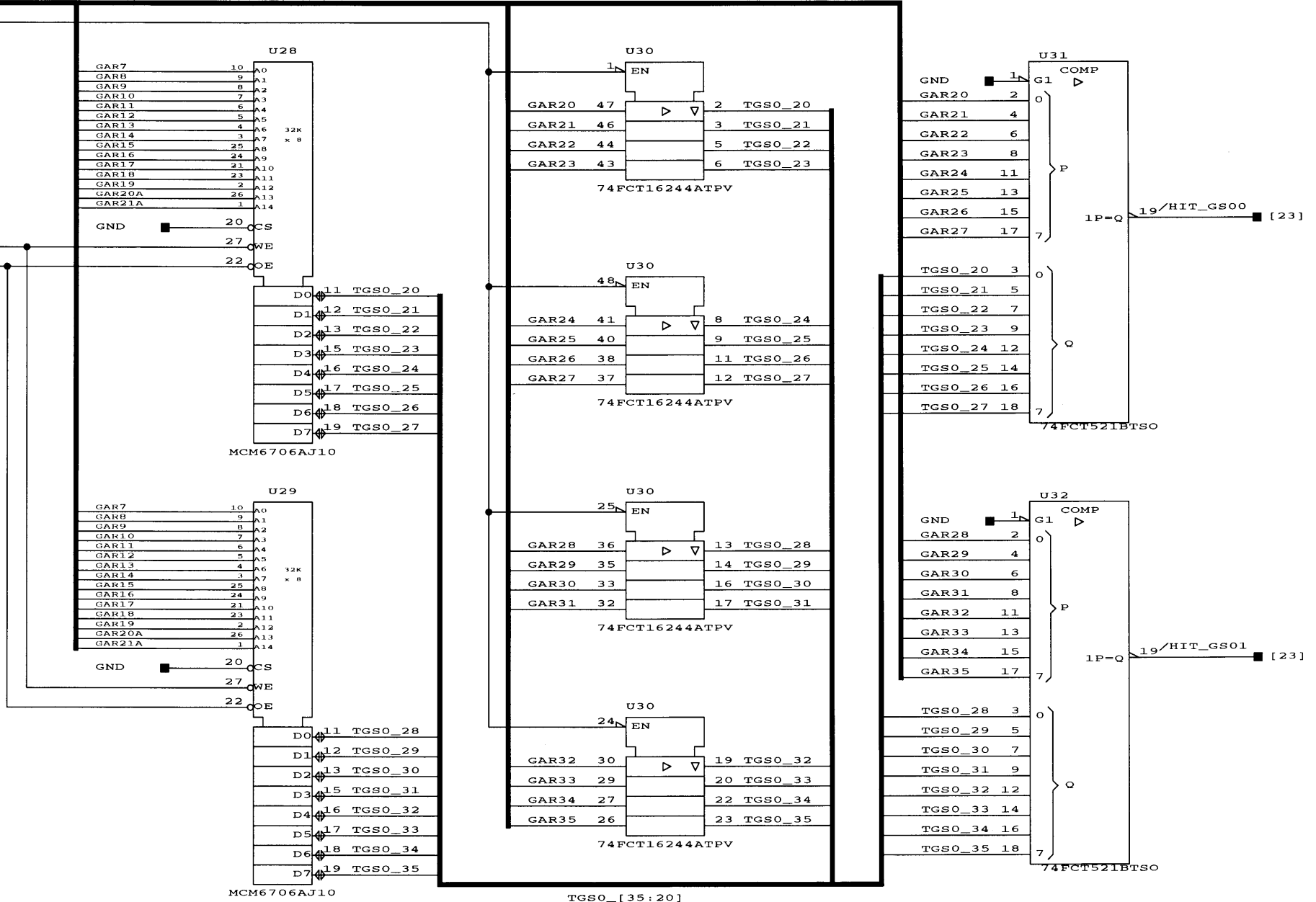
	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Global address register
Issue 2		
Issue 3		File: cpu301 Page:29 of 72

GAR[35:3],GAR[21:20]A

[22] /OE\_GSB

[22] /WE\_GS0

[22] /OE\_GS



TGS0\_[35:20]

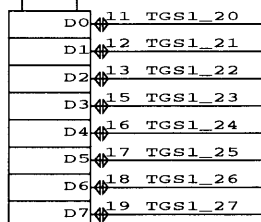
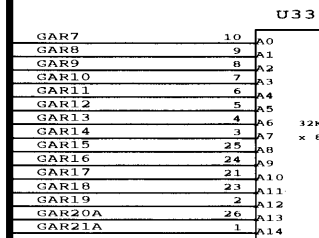
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global snooper 0
Issue 2		
Issue 3		File: cpu301 Page:30 of 72

GAR[35:3], GAR[21:20]A

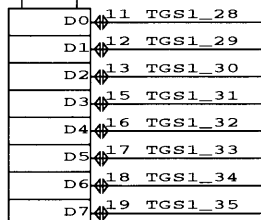
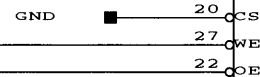
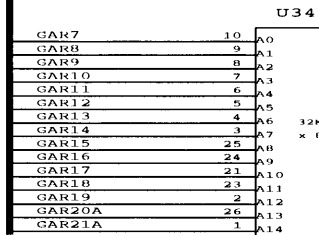
[22] /OE\_GSB

[22] /WE\_GS1

[22] /OE\_GS

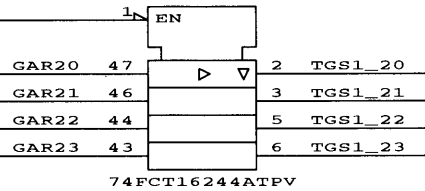


MCM6706AJ10

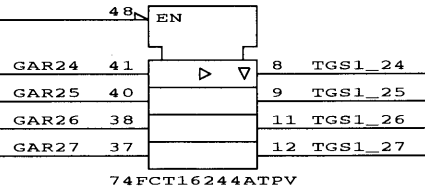


MCM6706AJ10

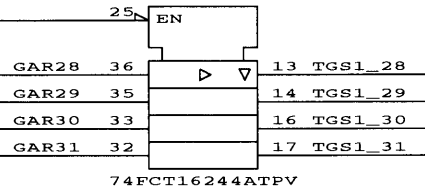
U35



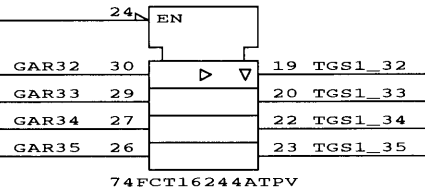
U35



U35

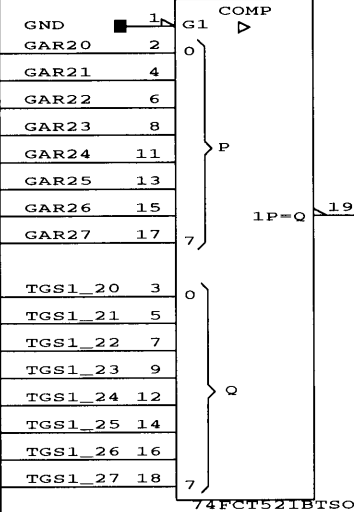


U35



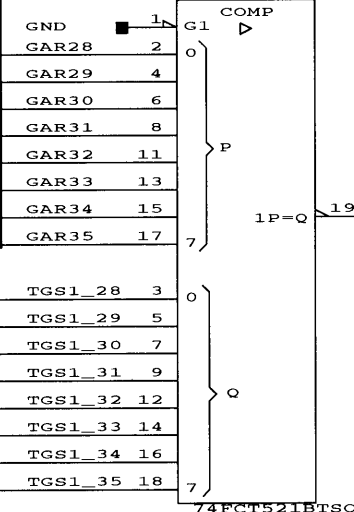
TGS1\_[35:20]

U36



1P=Q 19 /HIT\_GS10 [23]

U37



1P=Q 19 /HIT\_GS11 [23]

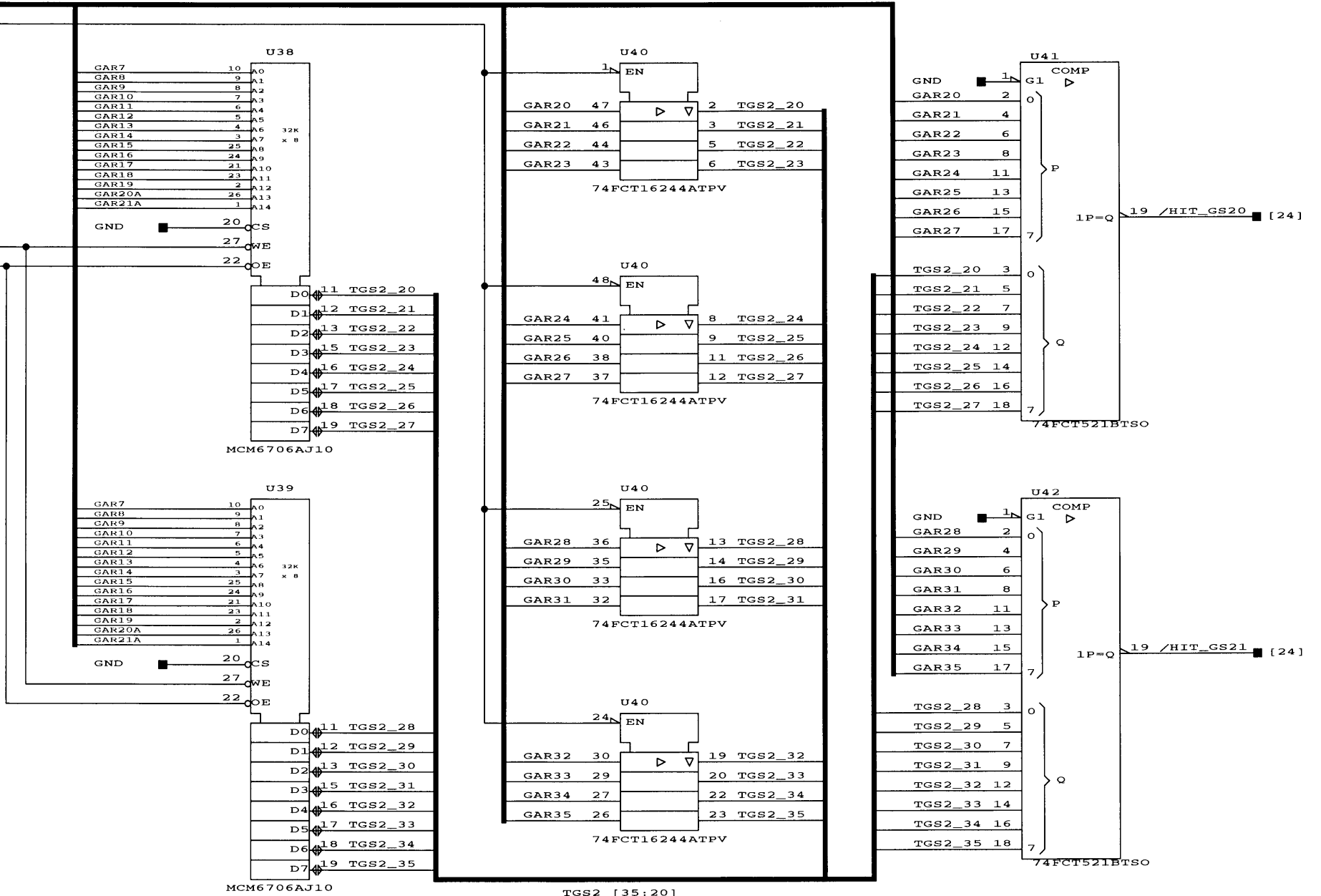
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global snooper 1
Issue 2		
Issue 3		File: cpu301 Page:31 of 72

GAR[35:3], GAR[21:20]A

[22] /OE\_GSB

[22] /WE\_GS2

[22] /OE\_GS



TGS2\_[35:20]

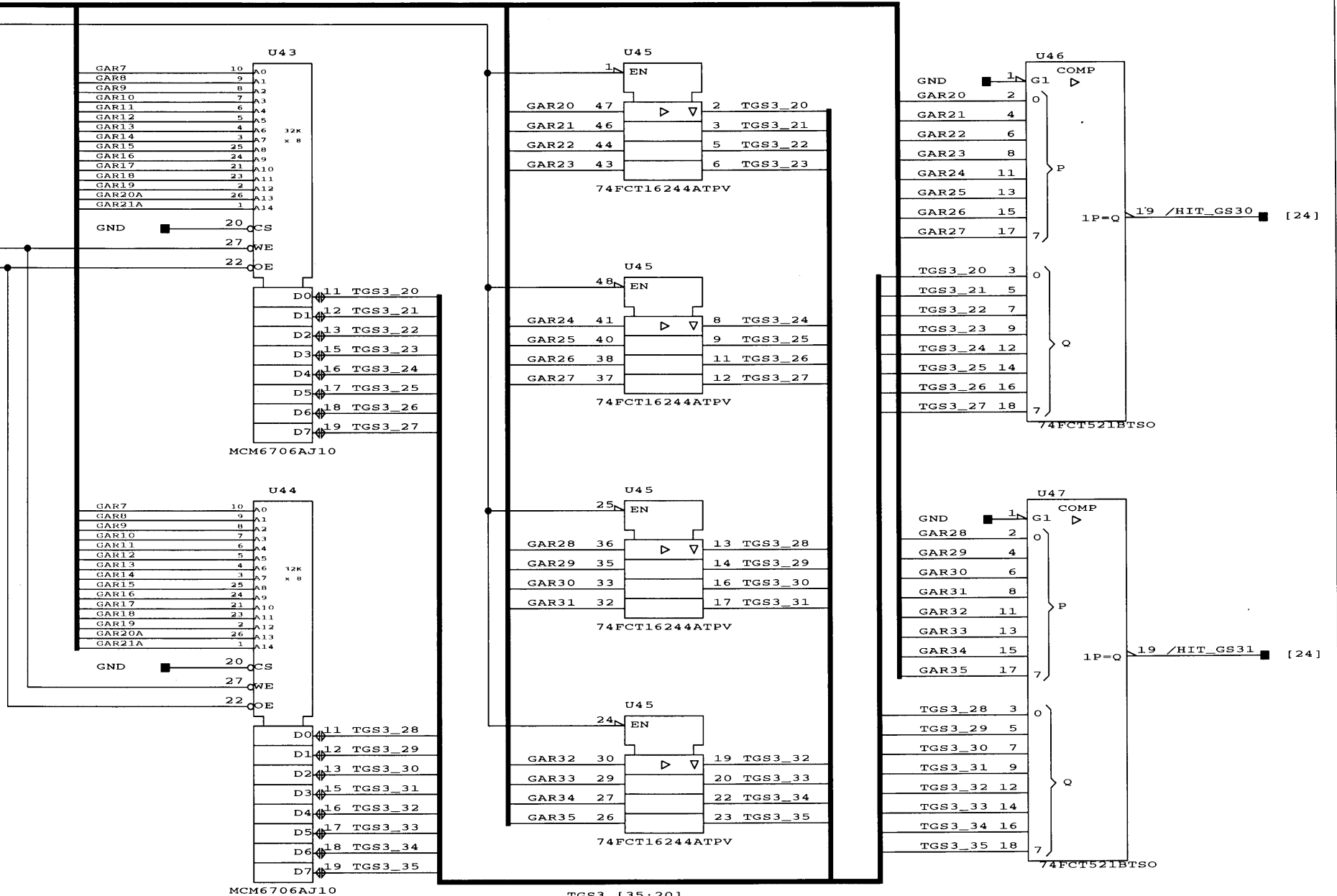
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global snooper 2
Issue 2		
Issue 3		File: cpu301 Page:32 of 72

GAR[35:3],GAR[21:20]A

[22] /OE\_GSB

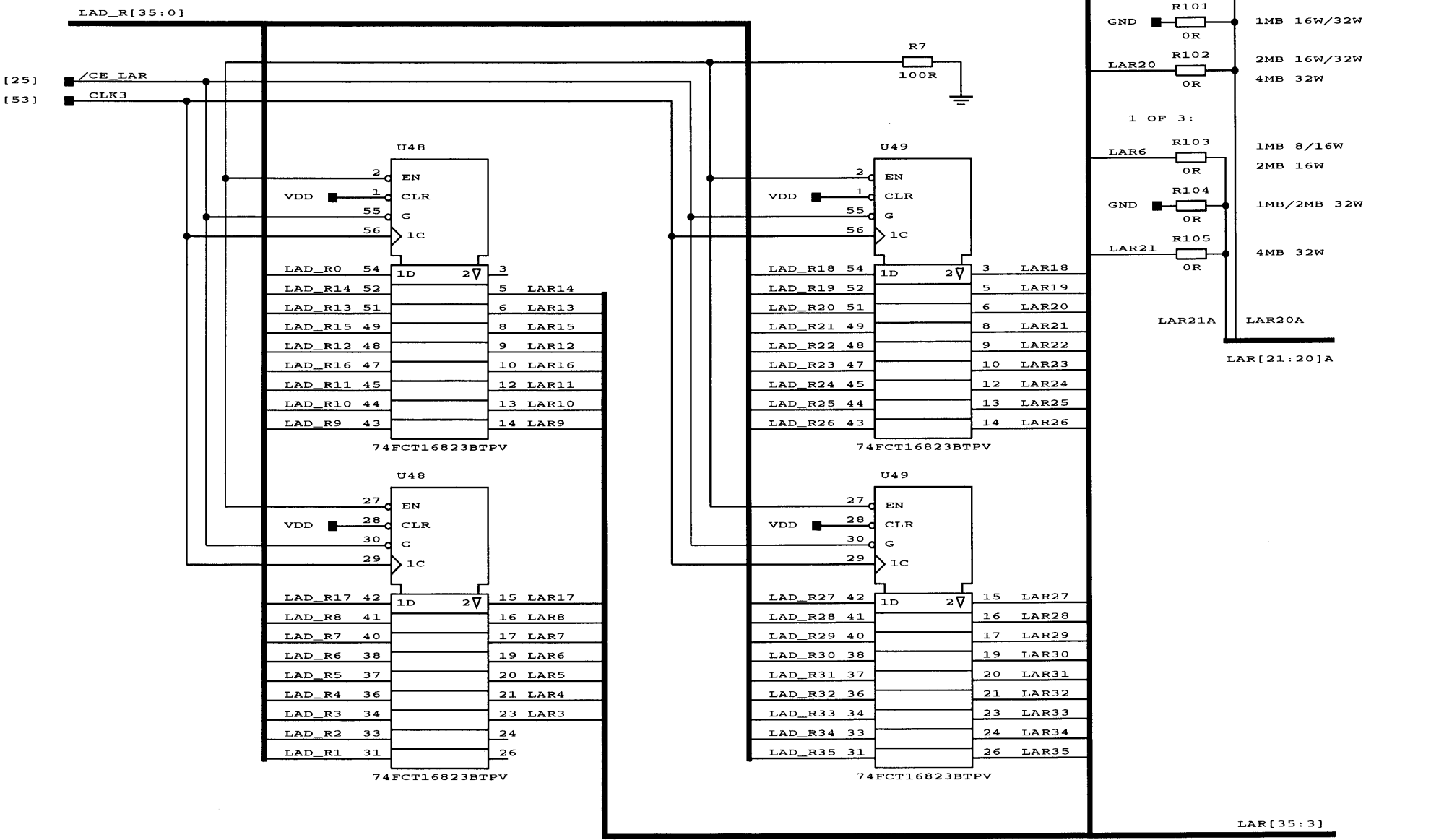
[22] /WE\_GS3

[22] /OE\_GS



TGS3\_[35:20]

dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global snooper 3
Issue 2		
Issue 3		File: cpu301
		Page:33 of 72

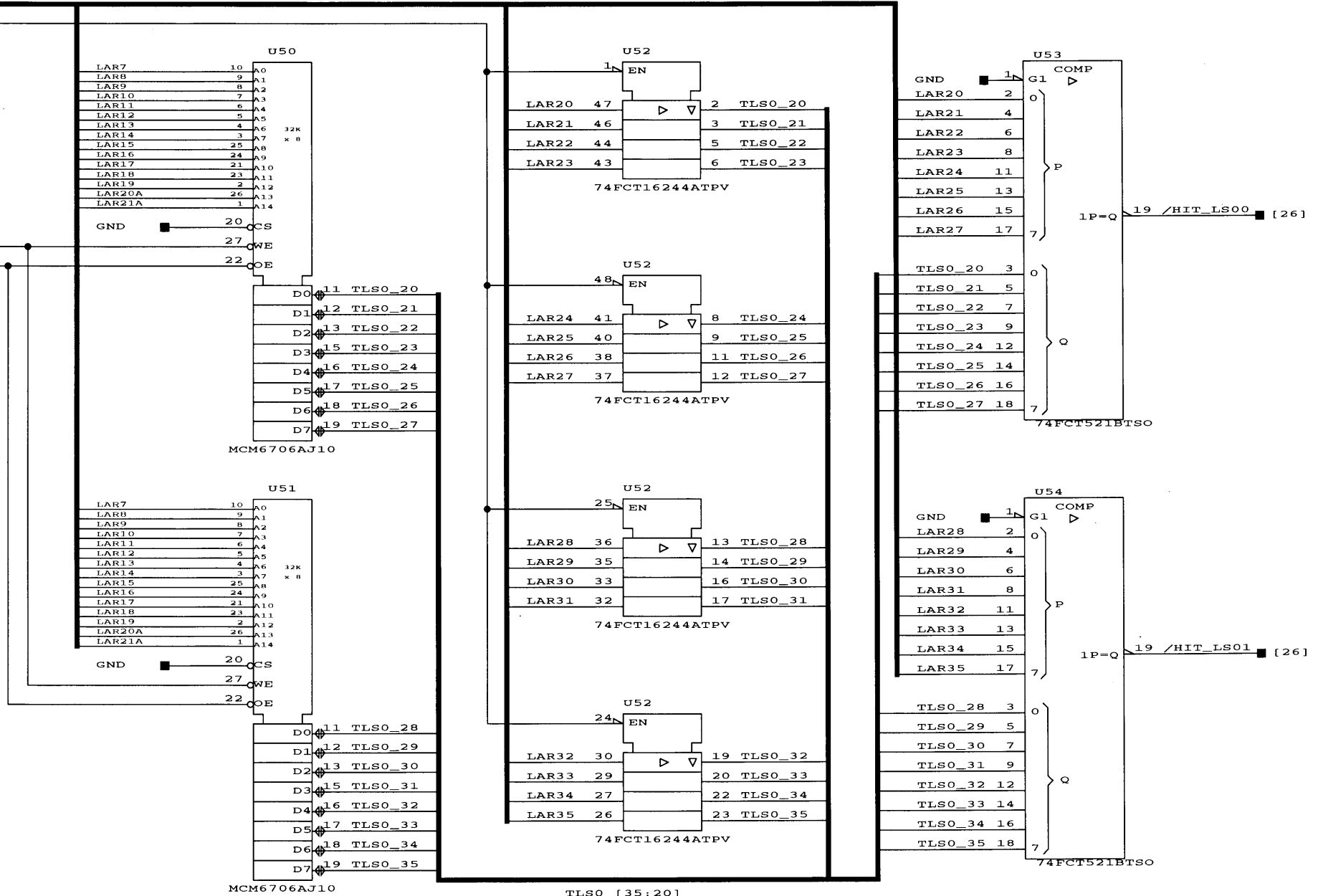


LAR[35:3], LAR[21:20]A

[25] /OE\_LSB

[25] /WE\_LSO

[25] /OE\_LS



TLSO\_[35:20]

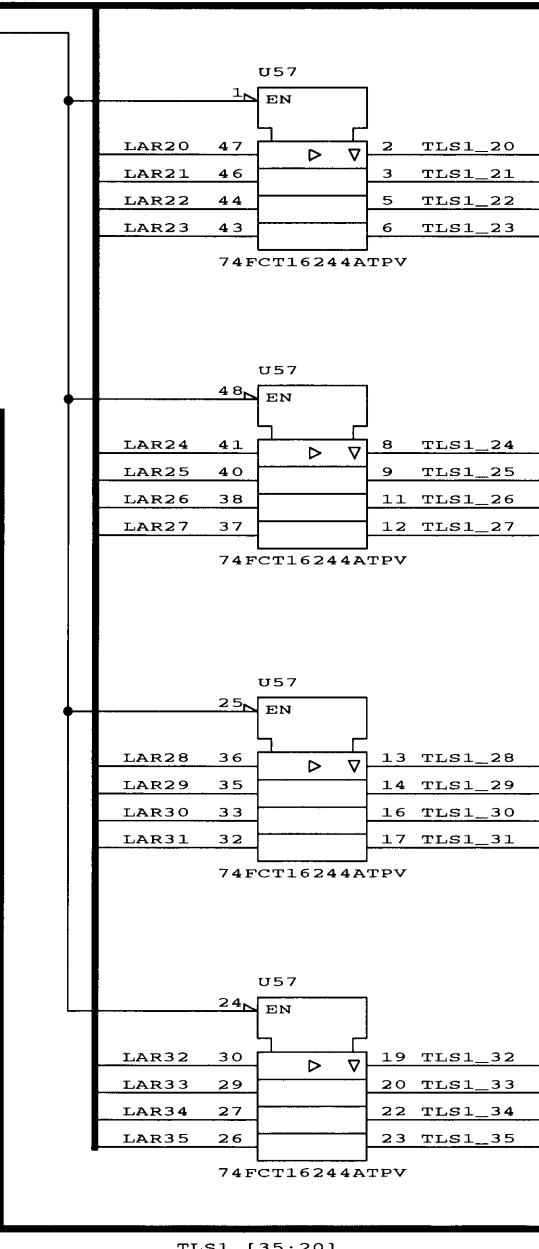
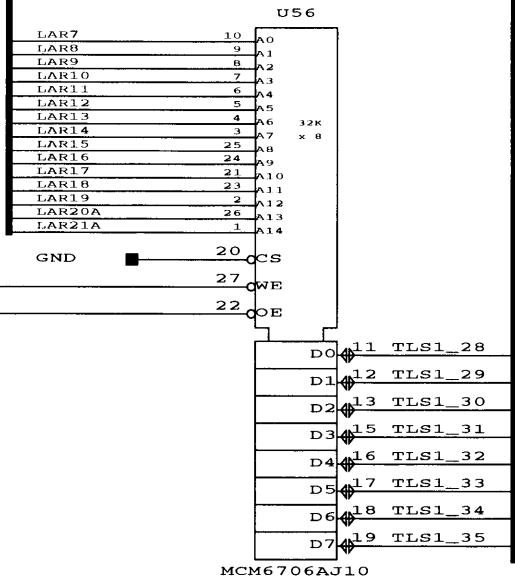
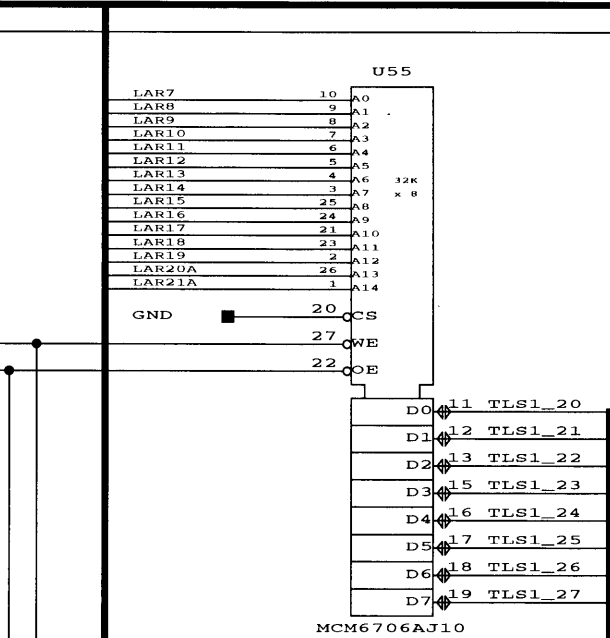
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Local snooper 0
Issue 2		
Issue 3		File: cpu301 Page:35 of 72

LAR[35:3],LAR[21:20]A

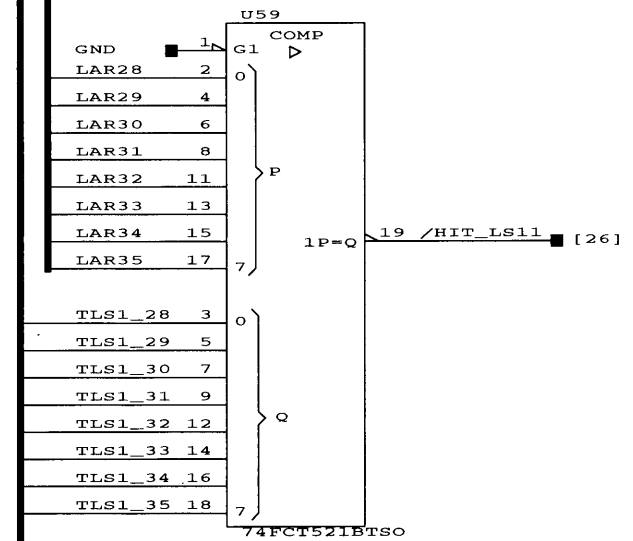
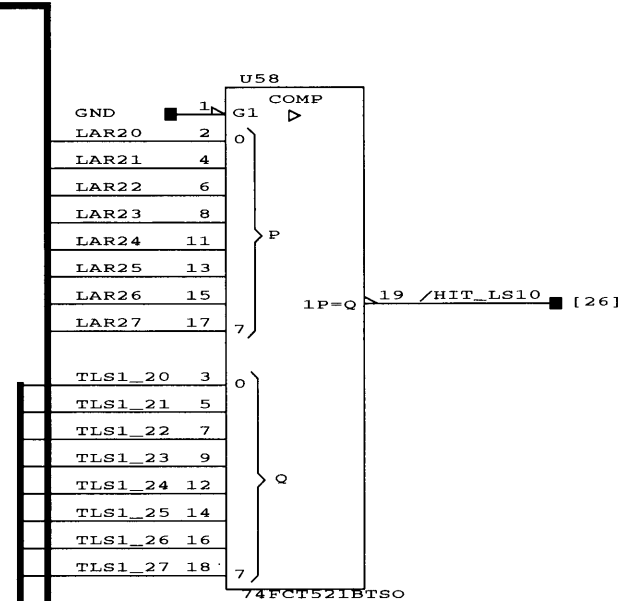
[25] /OE\_LSB

[25] /WE\_LS1

[25] /OE\_LS



TLS1\_[35:20]



dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Local snooper 1
Issue 2		
Issue 3		File: cpu301 Page:36 of 72

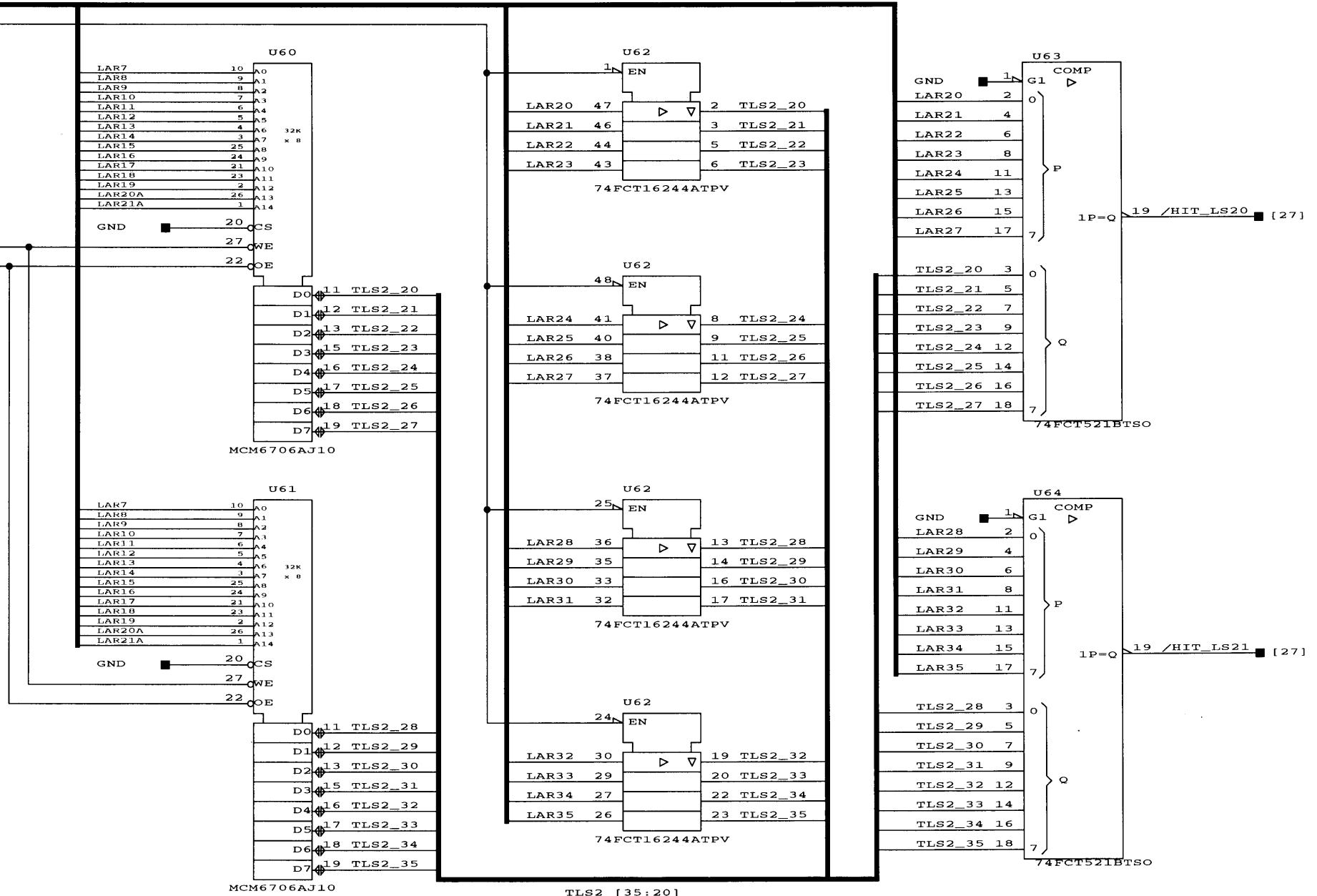


LAR[35:3],LAR[21:20]A

[25] /OE\_LSB

[25] /WE\_LS2

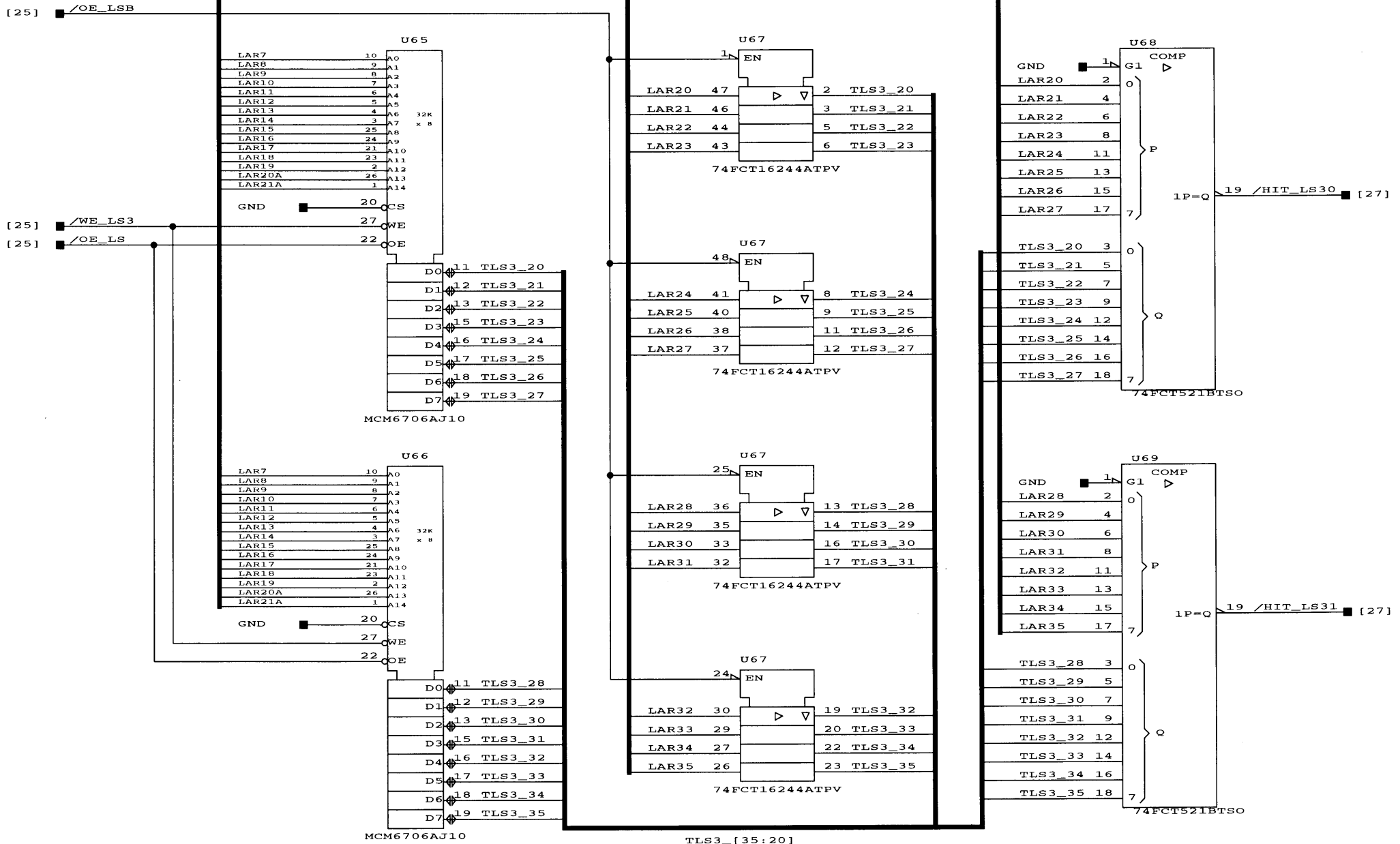
[25] /OE\_LS



TLS2\_[35:20]

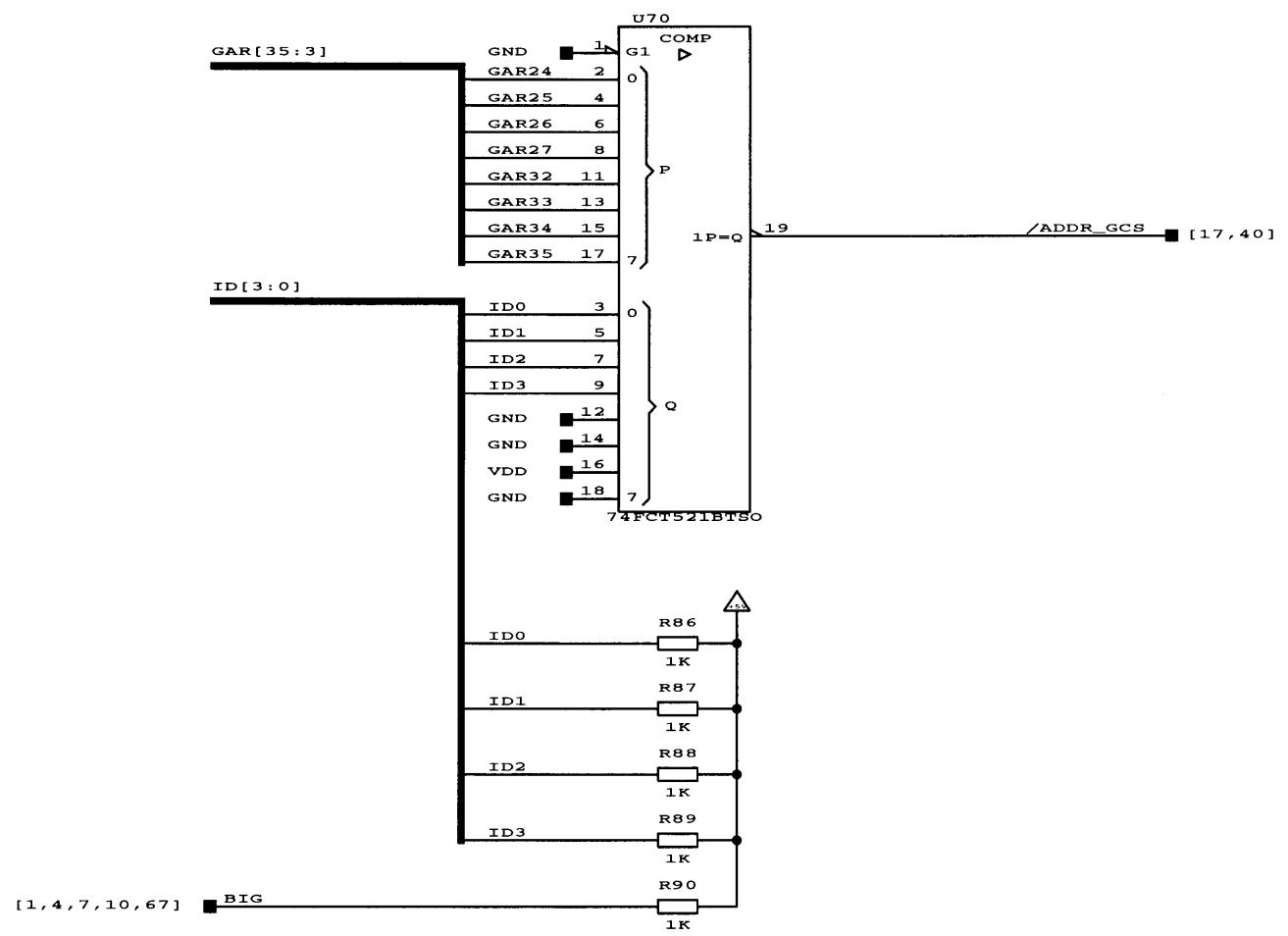
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Local snooper 2
Issue 2		
Issue 3		File: cpu301 Page:37 of 72

LAR[35:3], LAR[21:20]A

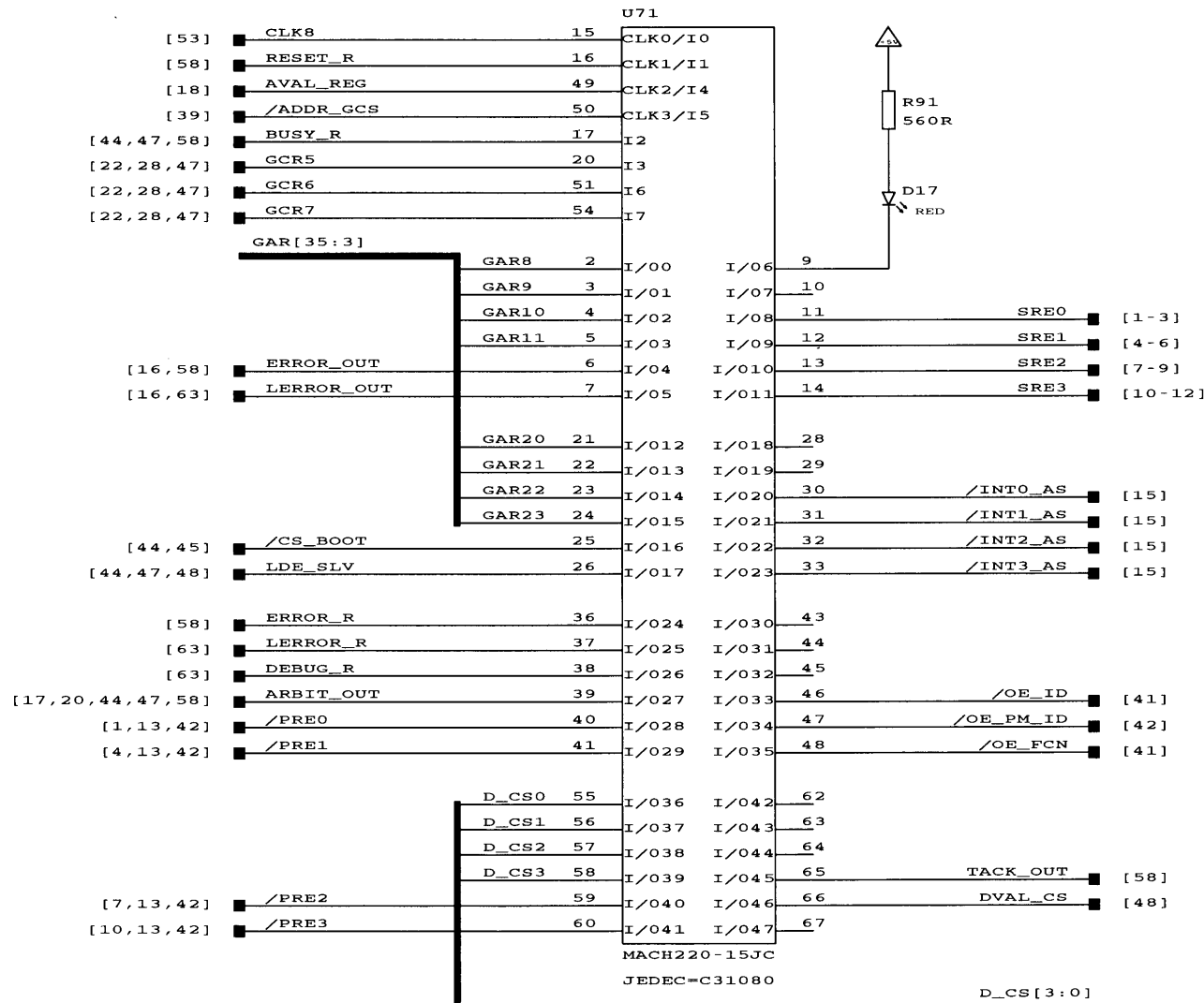


TLS3\_[35:20]

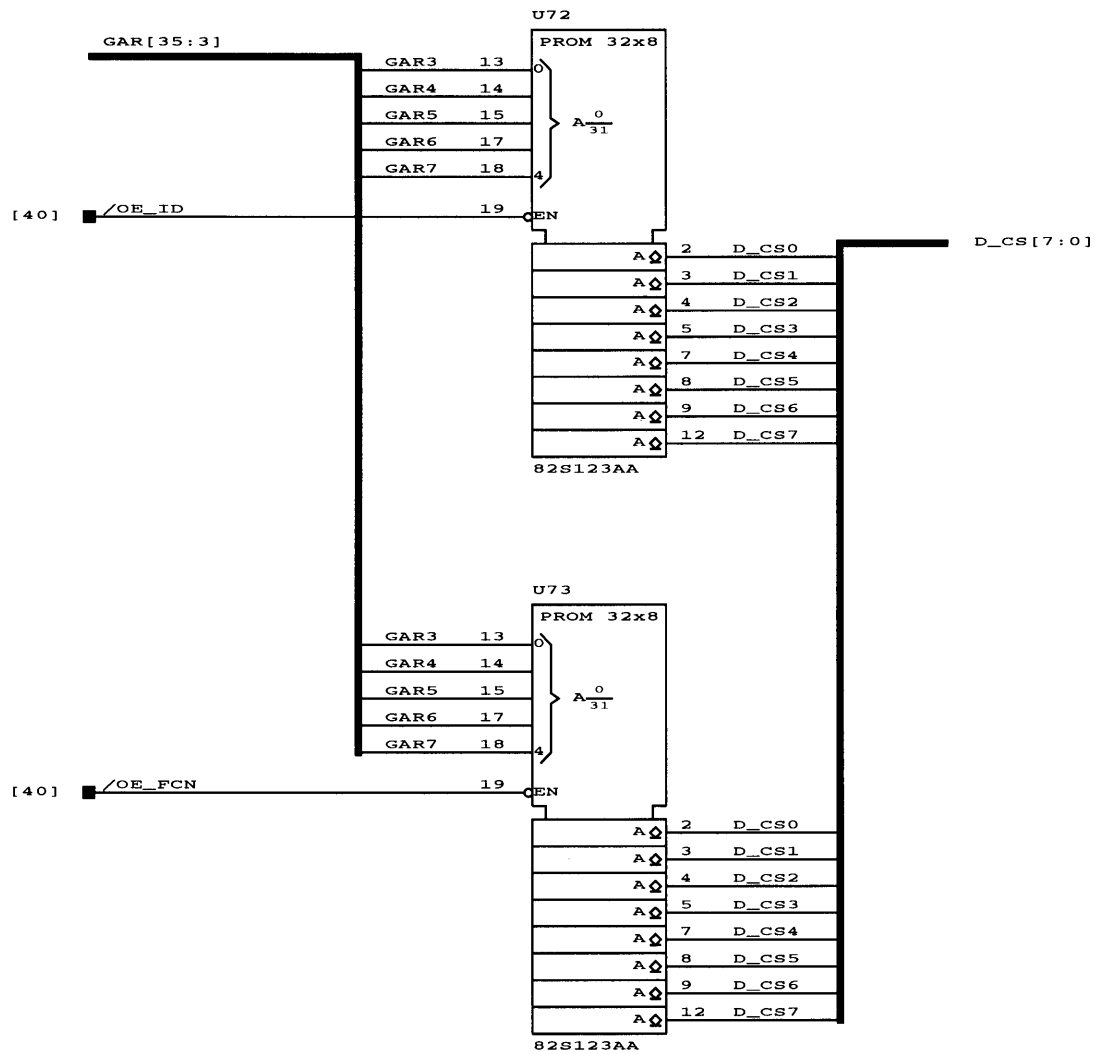
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Local snooper 3
Issue 2		
Issue 3		File: cpu301 Page:38 of 72




		Dansk Data Elektronik A/S	
Issue 0	940506	CPU301 Module	
Issue 1		Global control	
Issue 2		space decode	
Issue 3		File: cpu301	Page: 39 of 72

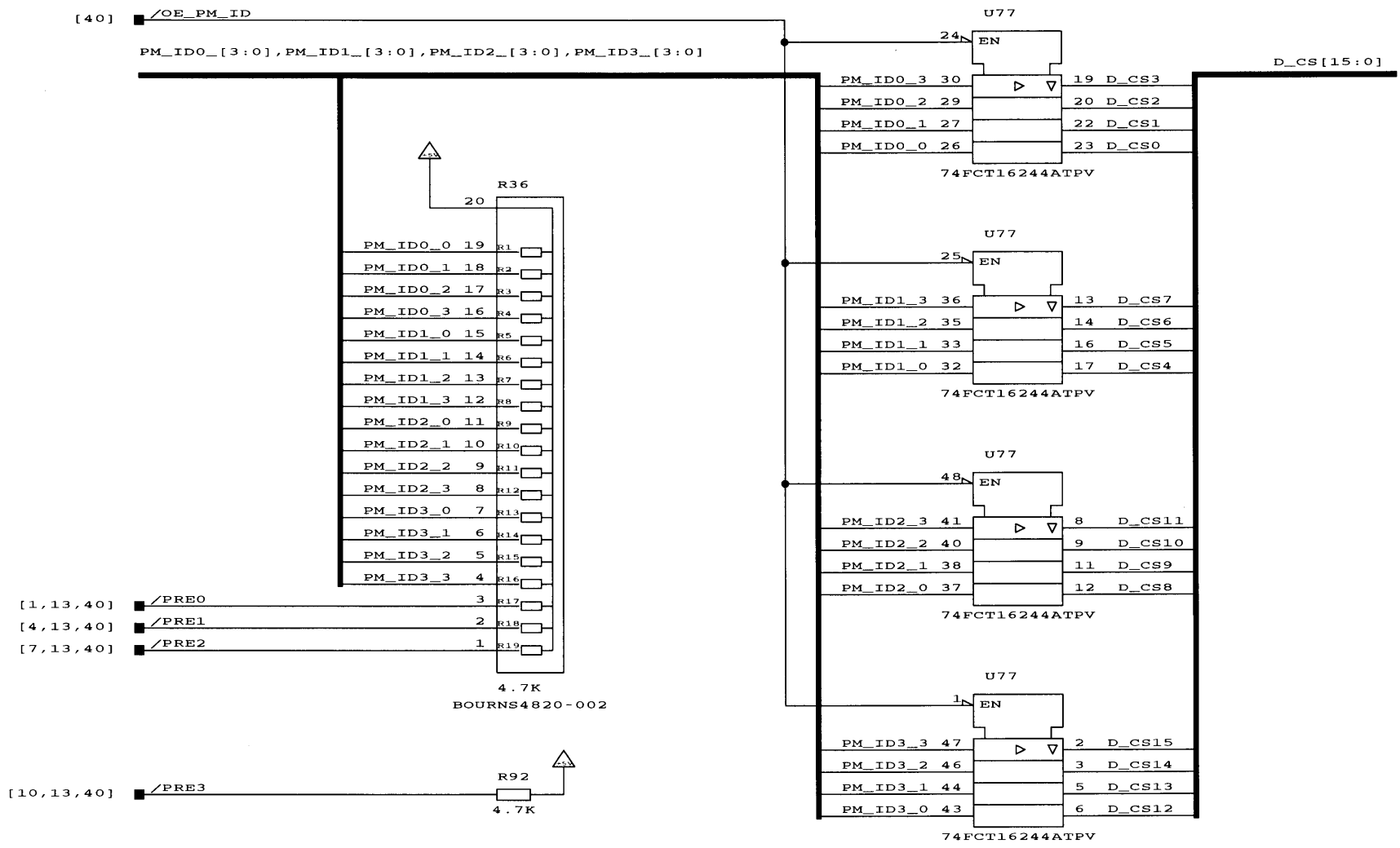


dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global control space
Issue 2		control
Issue 3		File: cpu301 Page: 40 of 72

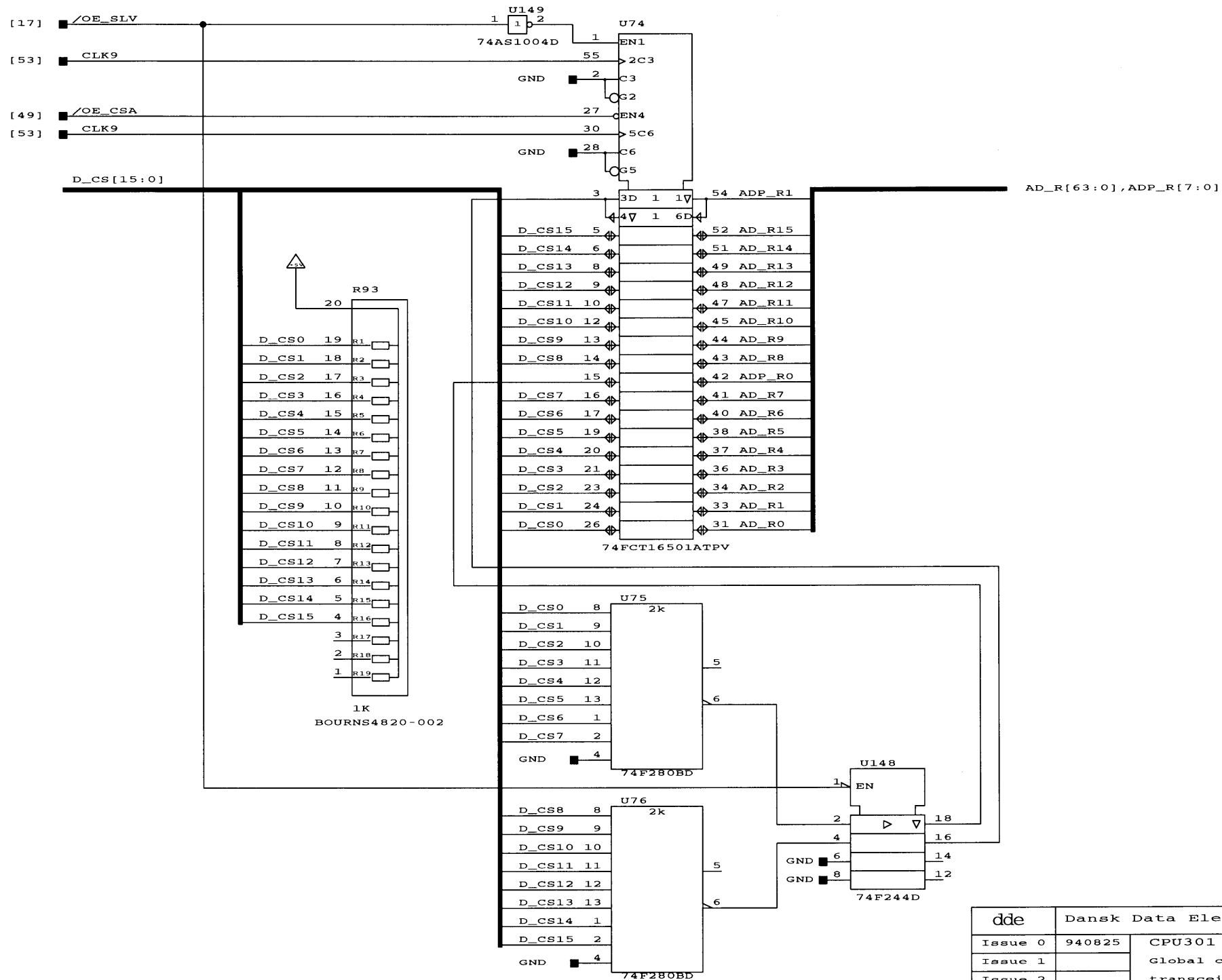


FCN PROM mounted in socket.

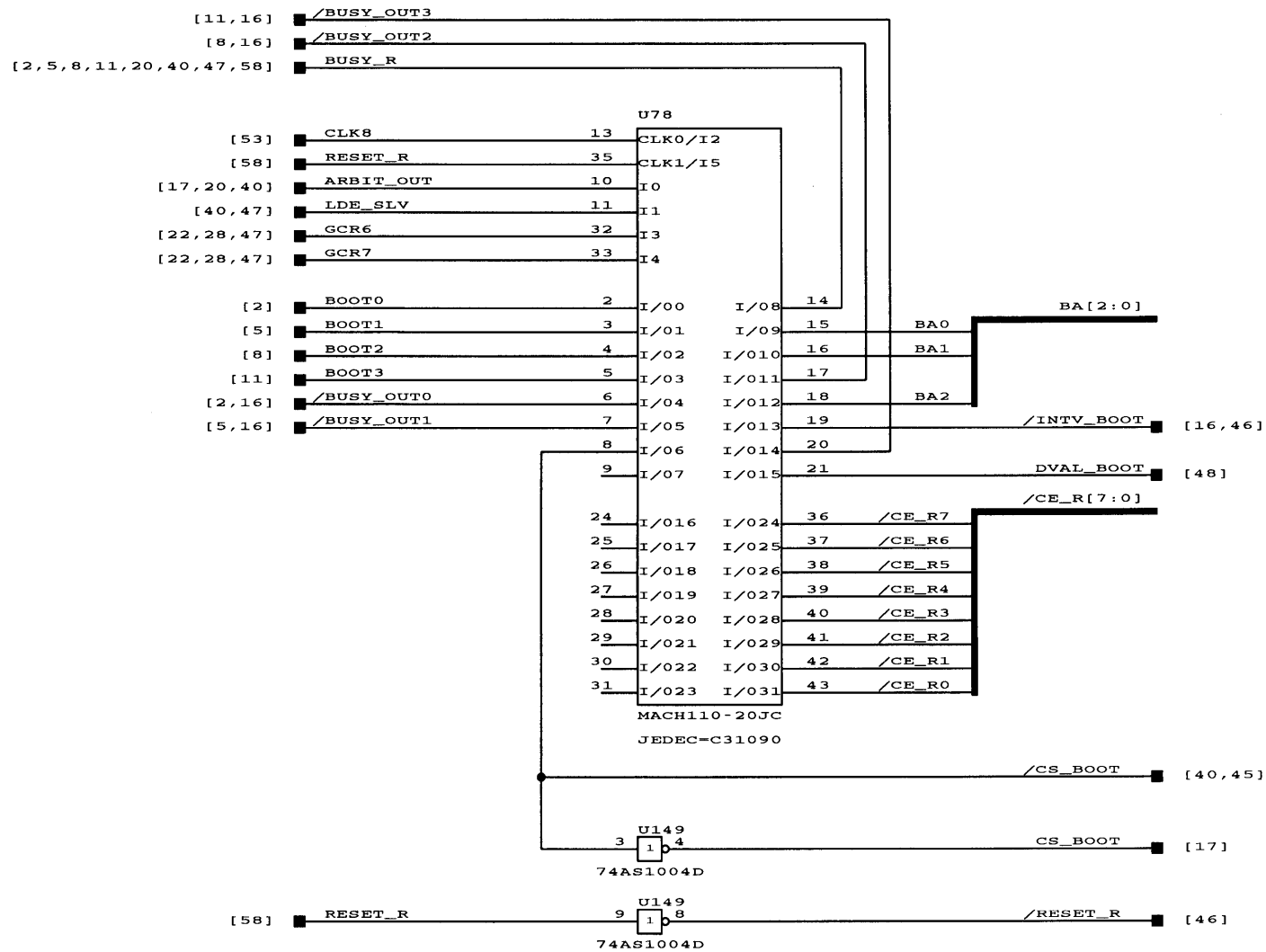
	Dansk Data Elektronik A/S	
Issue 0	940506	CPU301 Module
Issue 1		Module ID and FCN PROMs.
Issue 2		
Issue 3		File: cpu301 Page: 41 of 72




dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Processor module
Issue 2		ID register
Issue 3		File: cpu301
		Page: 42 of 72

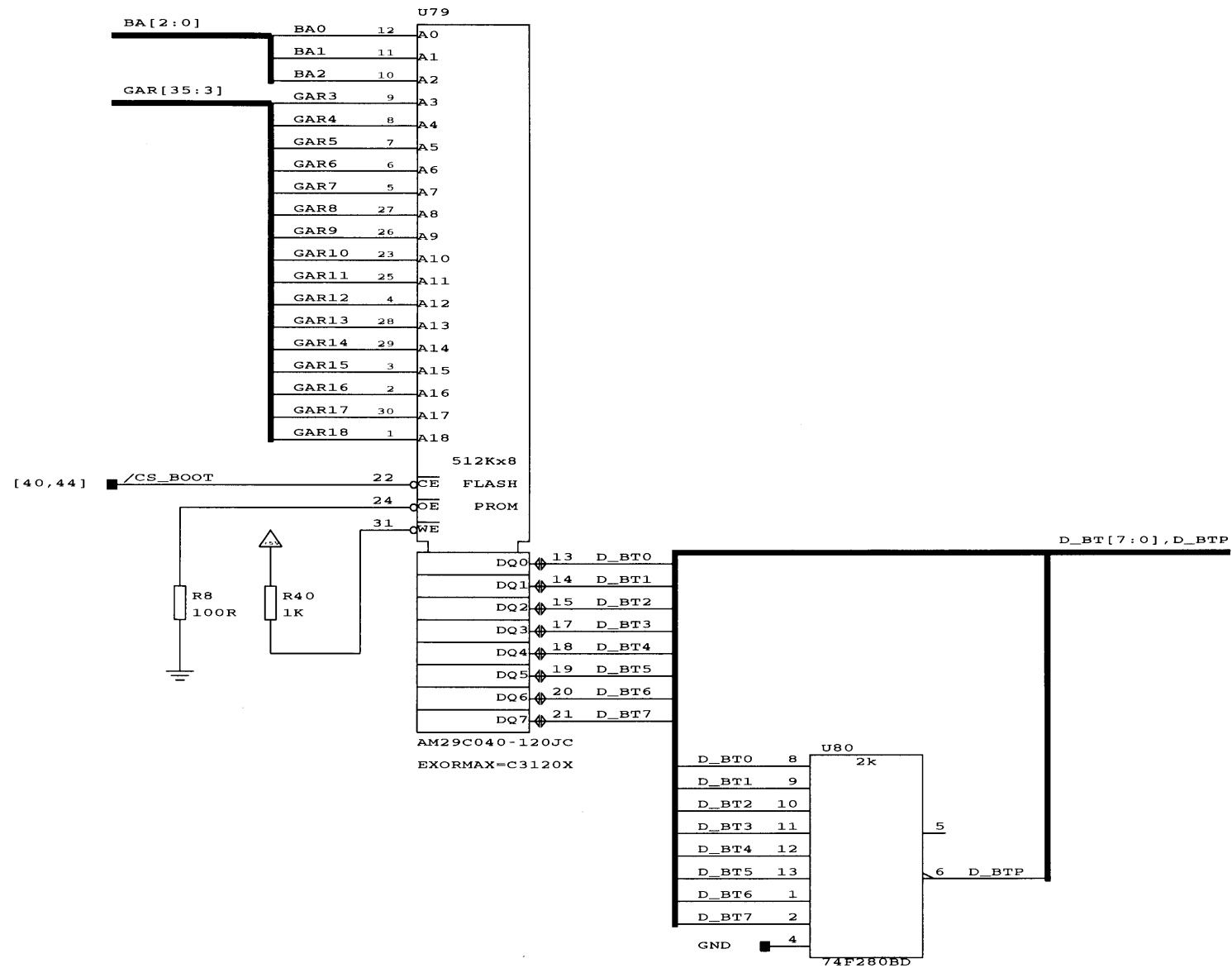


dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global control space
Issue 2		transceiver
Issue 3		File: cpu301
		Page:43 of 72

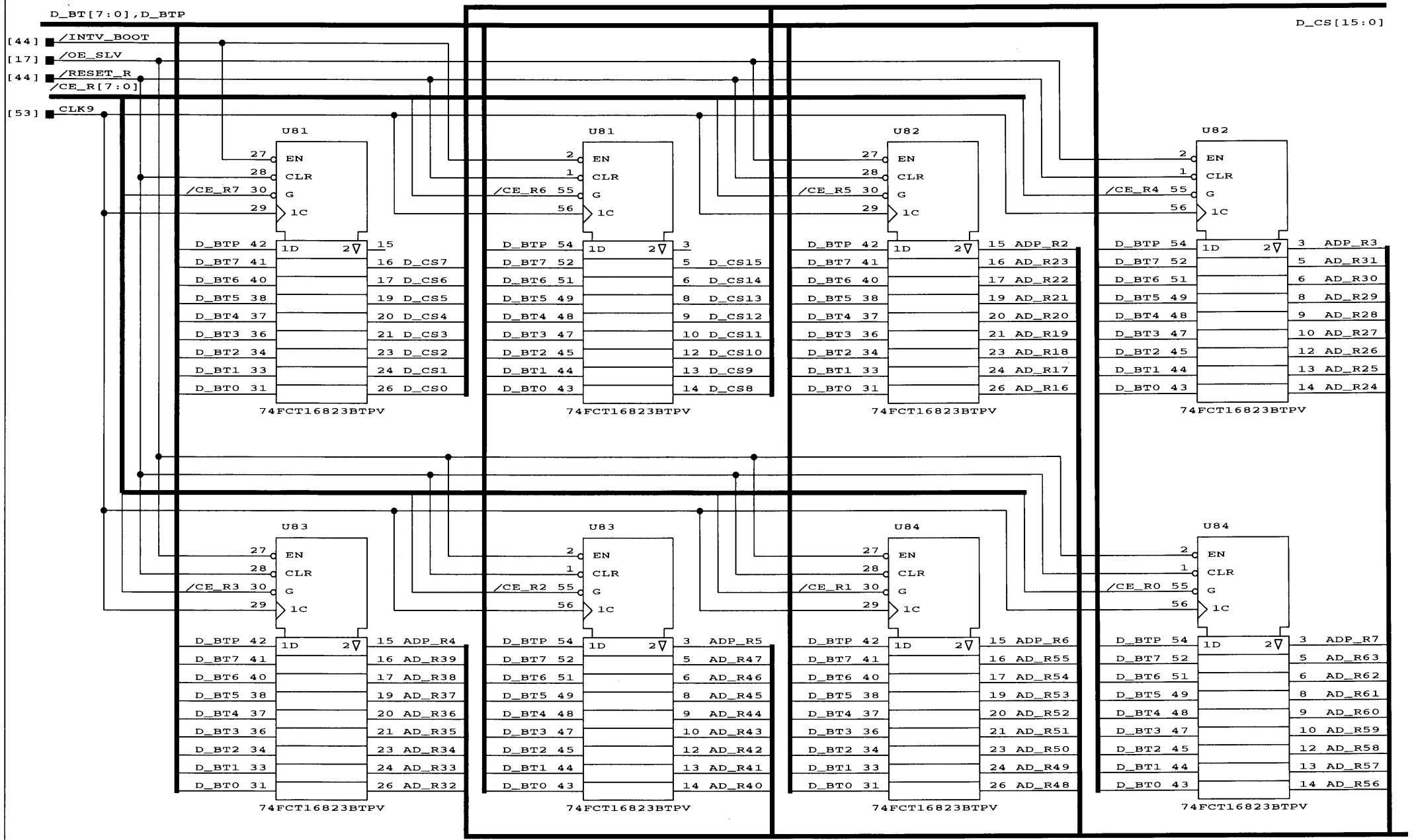


	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Boot control
Issue 2		
Issue 3		
		File: cpu301 Page:44 of 72



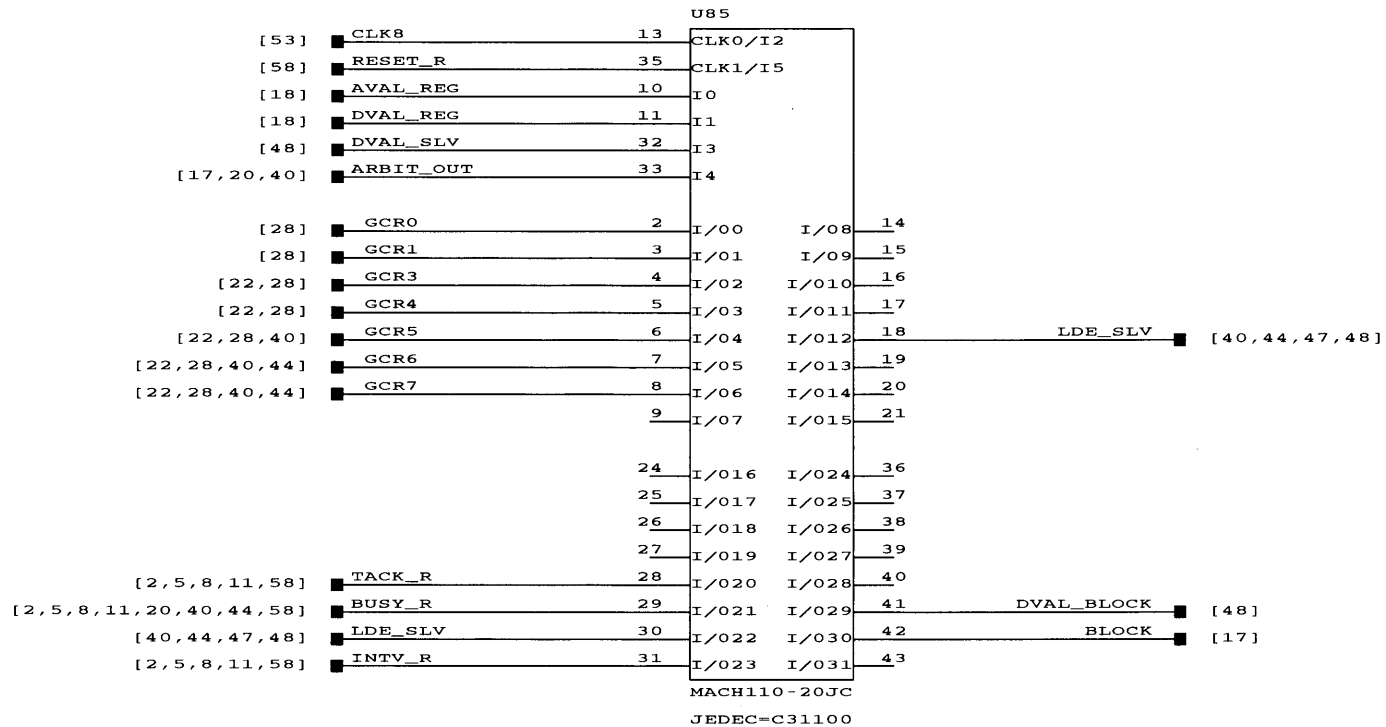


dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Boot PROM
Issue 2		
Issue 3		File: cpu301 Page:45 of 72

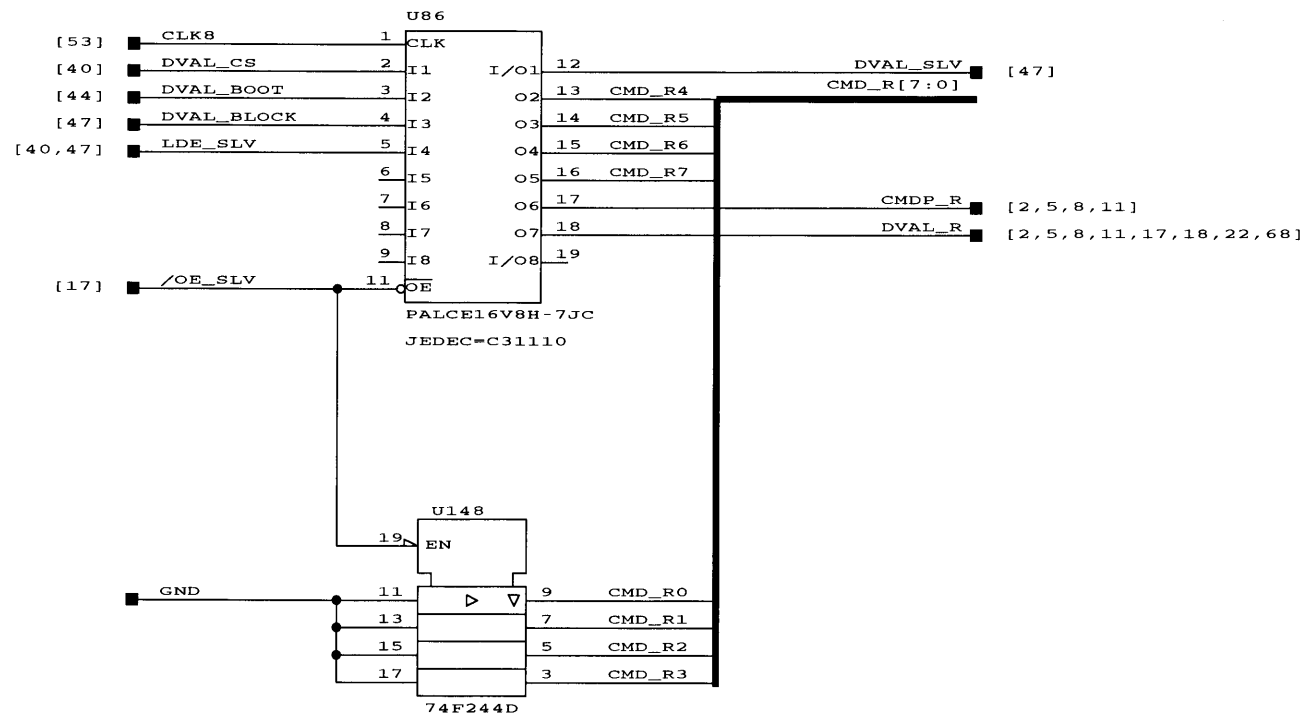


AD\_R[63:0], ADP\_R[7:0]

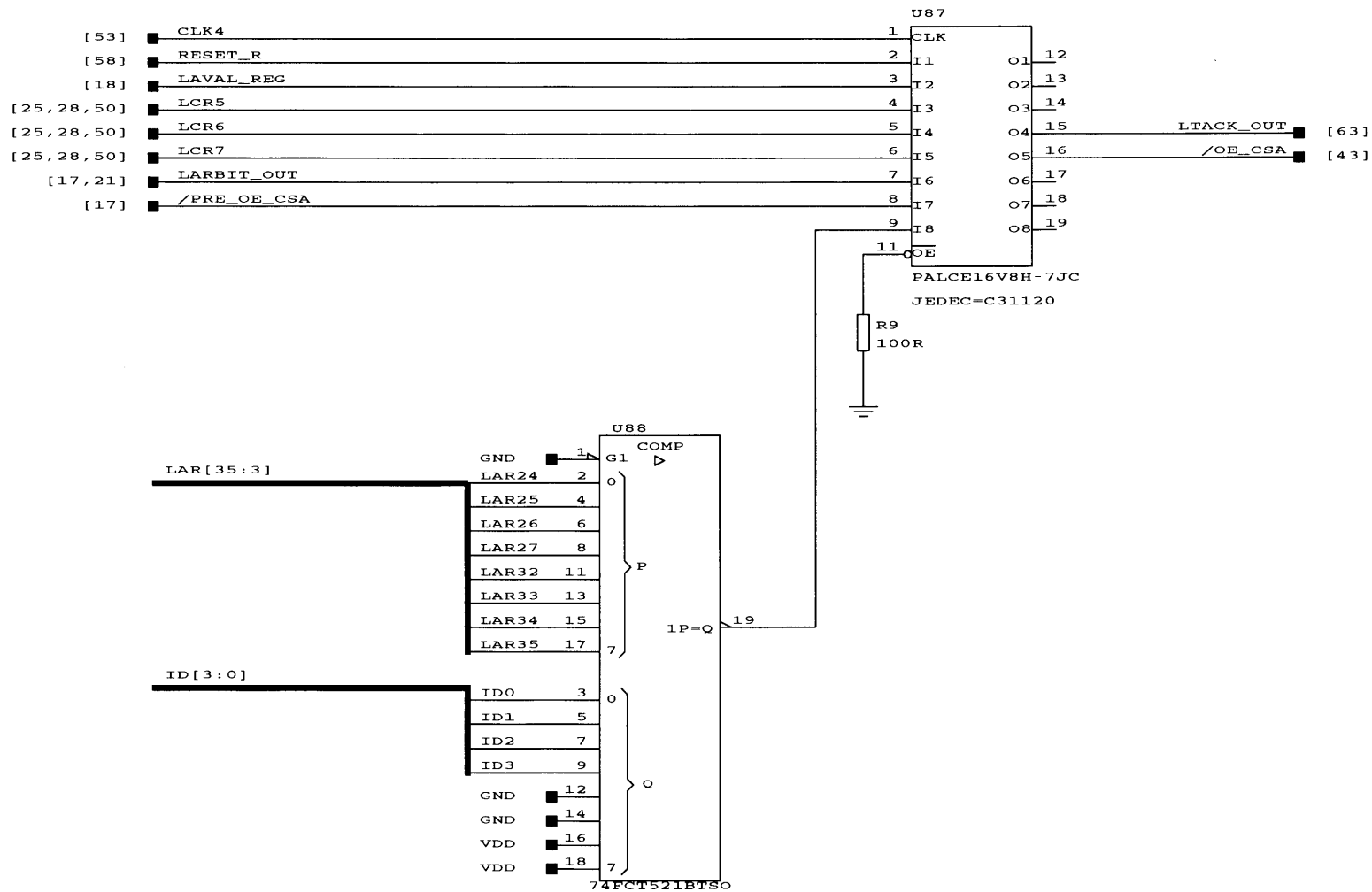
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Boot register
Issue 2		
Issue 3		File: cpu301 Page:46 of 72



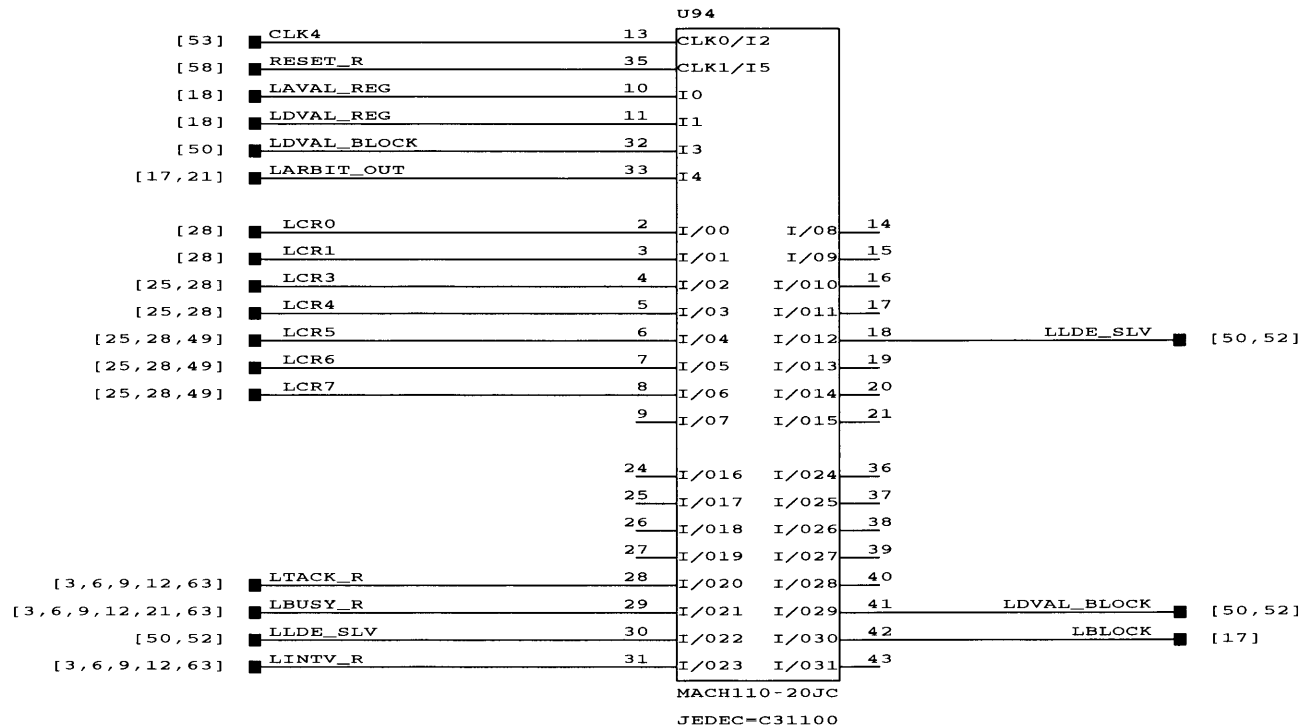
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1		Global dummy	
Issue 2		block generator	
Issue 3		File: cpu301	Page: 47 of 72



dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Global data identifier
Issue 2		output register
Issue 3		File: cpu301 Page: 48 of 72

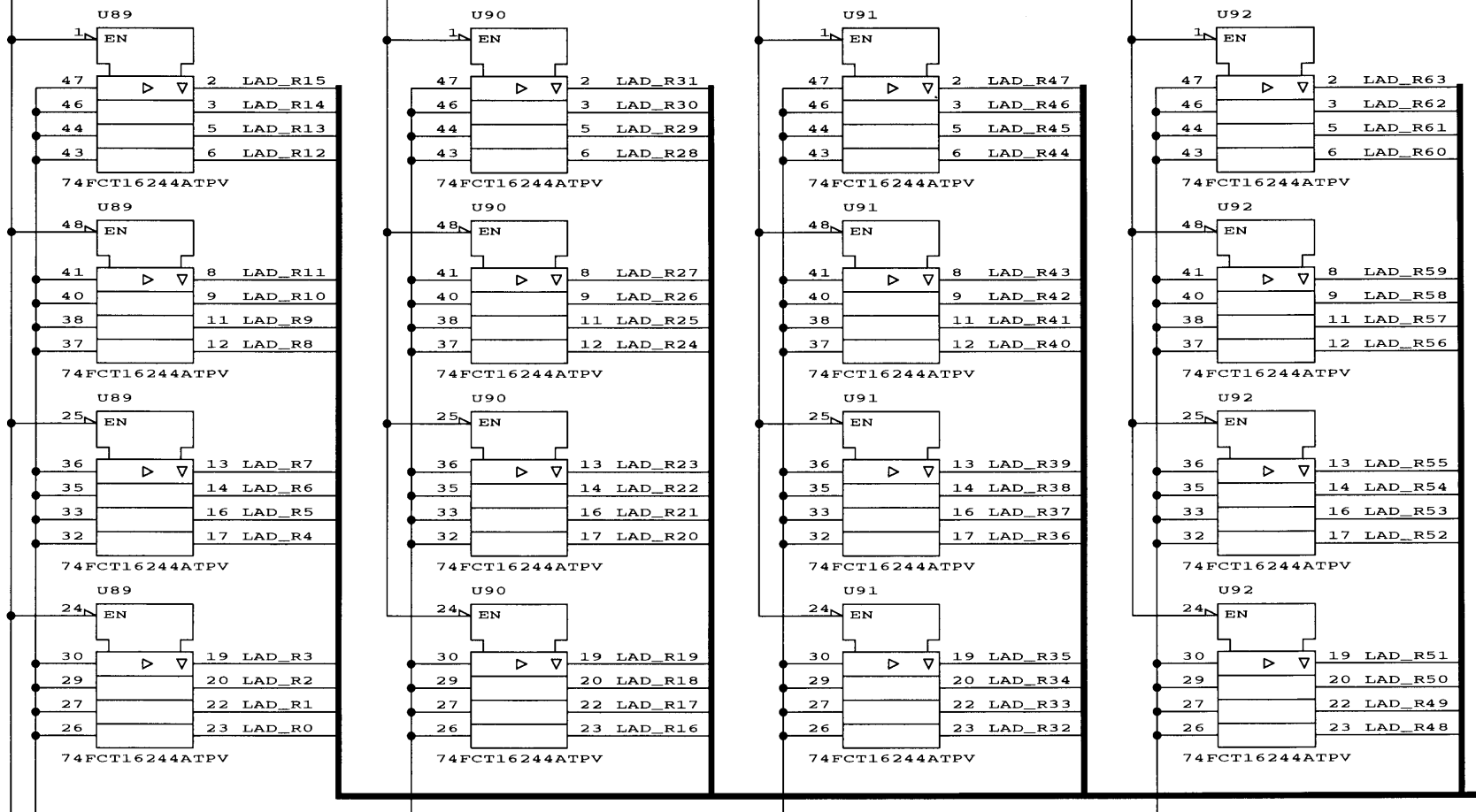


dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Local control space decode
Issue 2		and target acknowledge
Issue 3		File: cpu301 Page:49 of 72



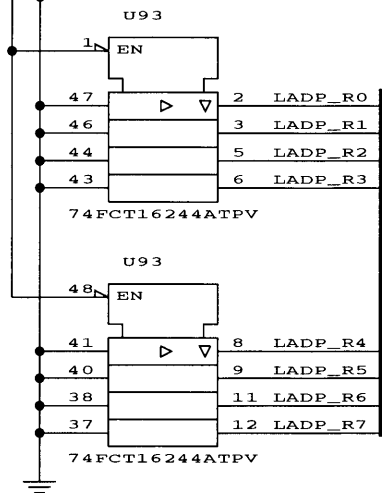
dde	Dansk Data Elektronik A/S		
Issue 0	940825	CPU301 Module	
Issue 1		Local dummy block generator	
Issue 2			
Issue 3		File: cpu301	Page: 50 of 72

[17] /OE\_LSLV

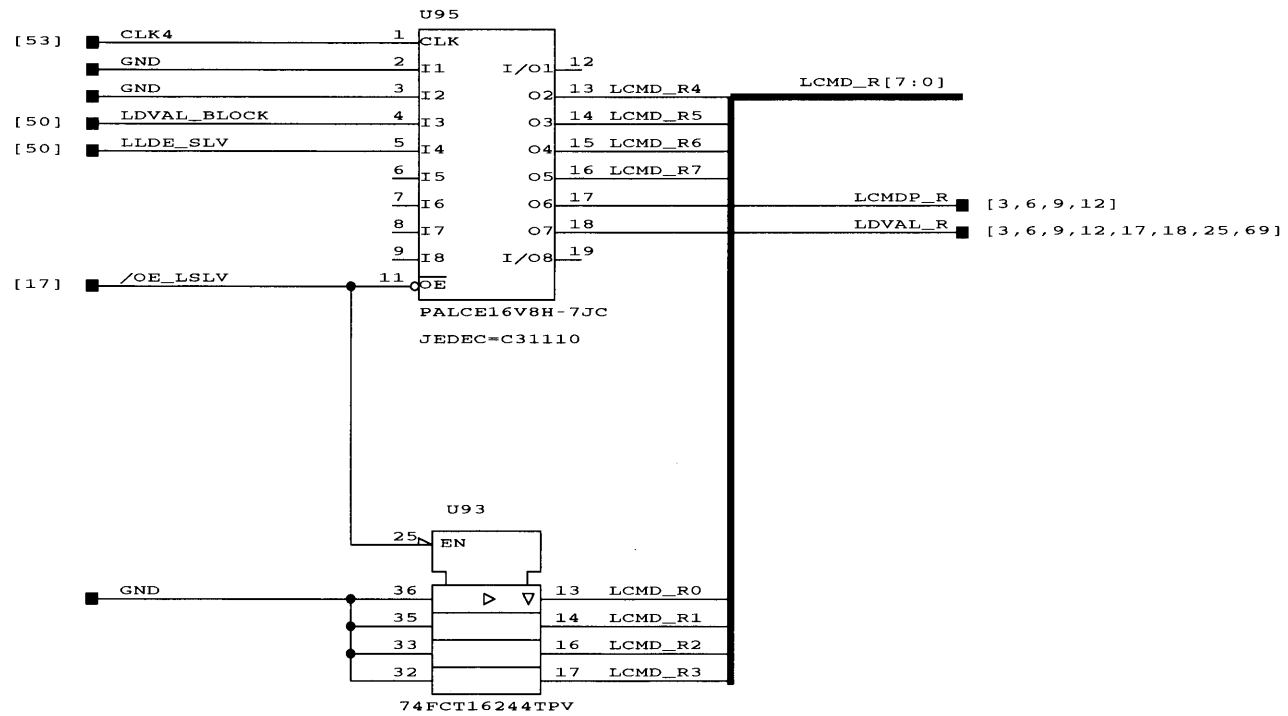


LAD\_R[63:0]

LADP\_R[7:0]

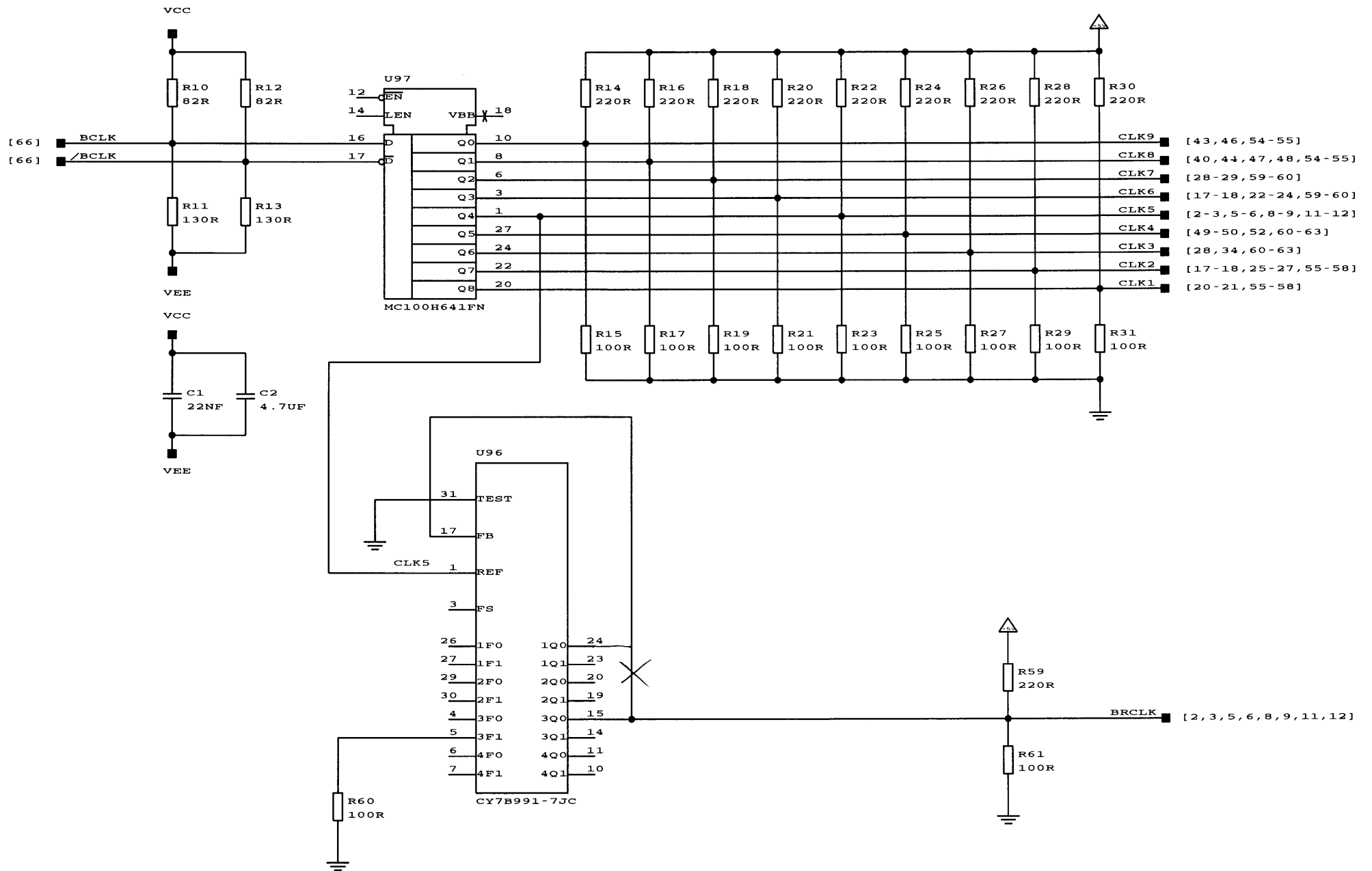


dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Local dummy data
Issue 2		
Issue 3		File: cpu301 Page:51 of 72

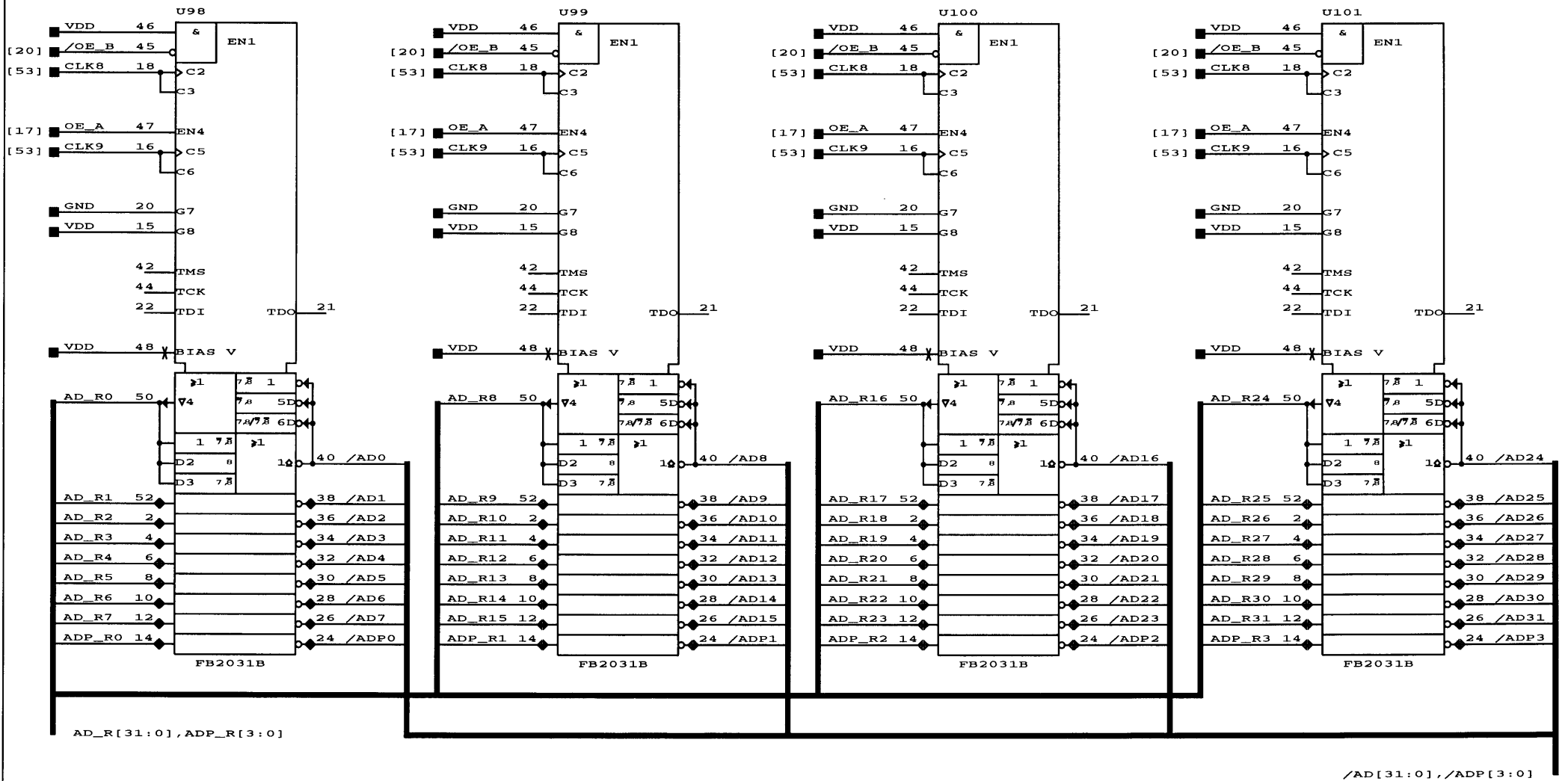



dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Local data identifier
Issue 2		output register
Issue 3		File: cpu301 Page:52 of 72

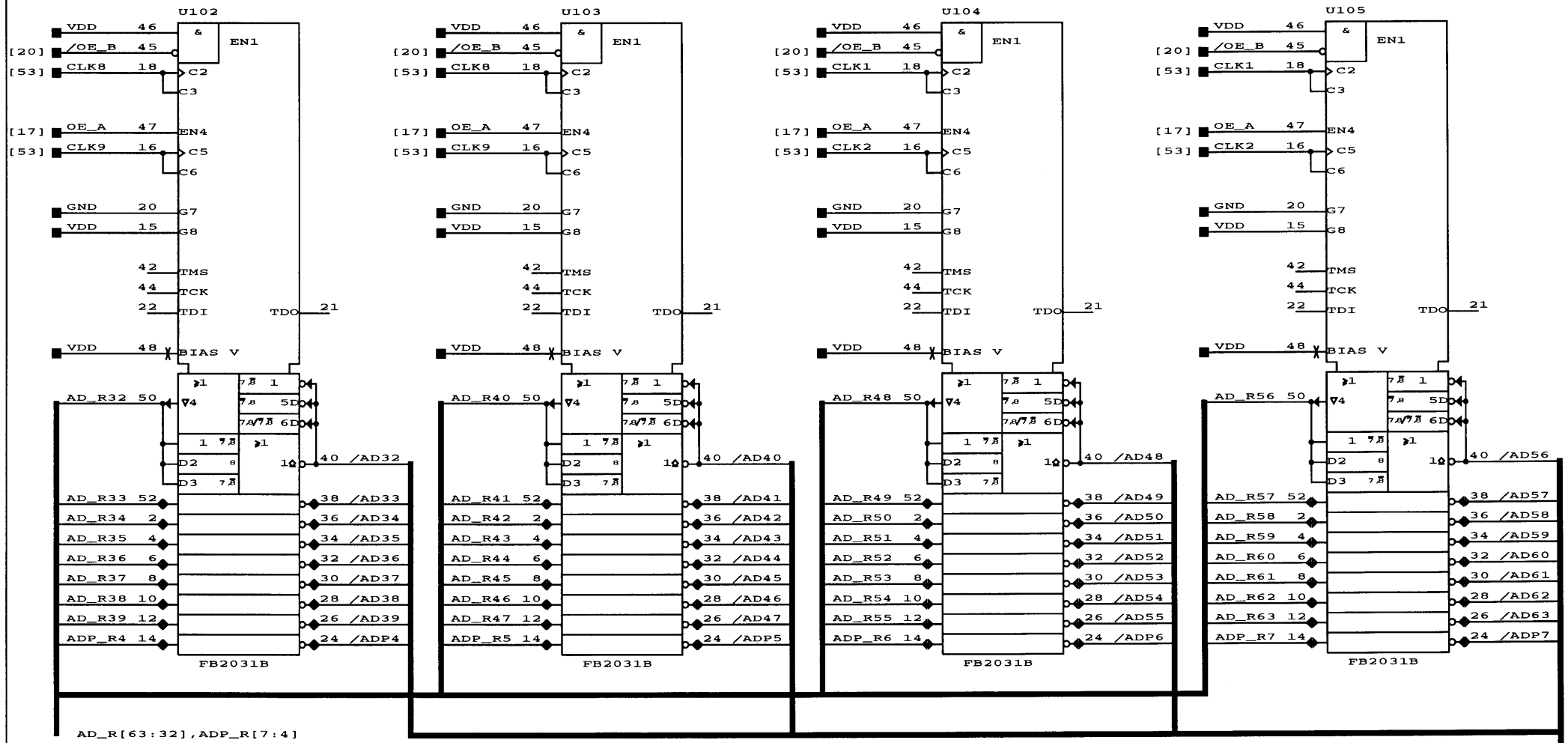




	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Clock distribution
Issue 2		
Issue 3		File: cpu301 Page: 53 of 72



 Dansk Data Elektronik A/S		
Issue 0	940506	CPU301 Module
Issue 1	CHG	Global address/data
Issue 2		transceiver
Issue 3		File: cpu301 Page: 54 of 72

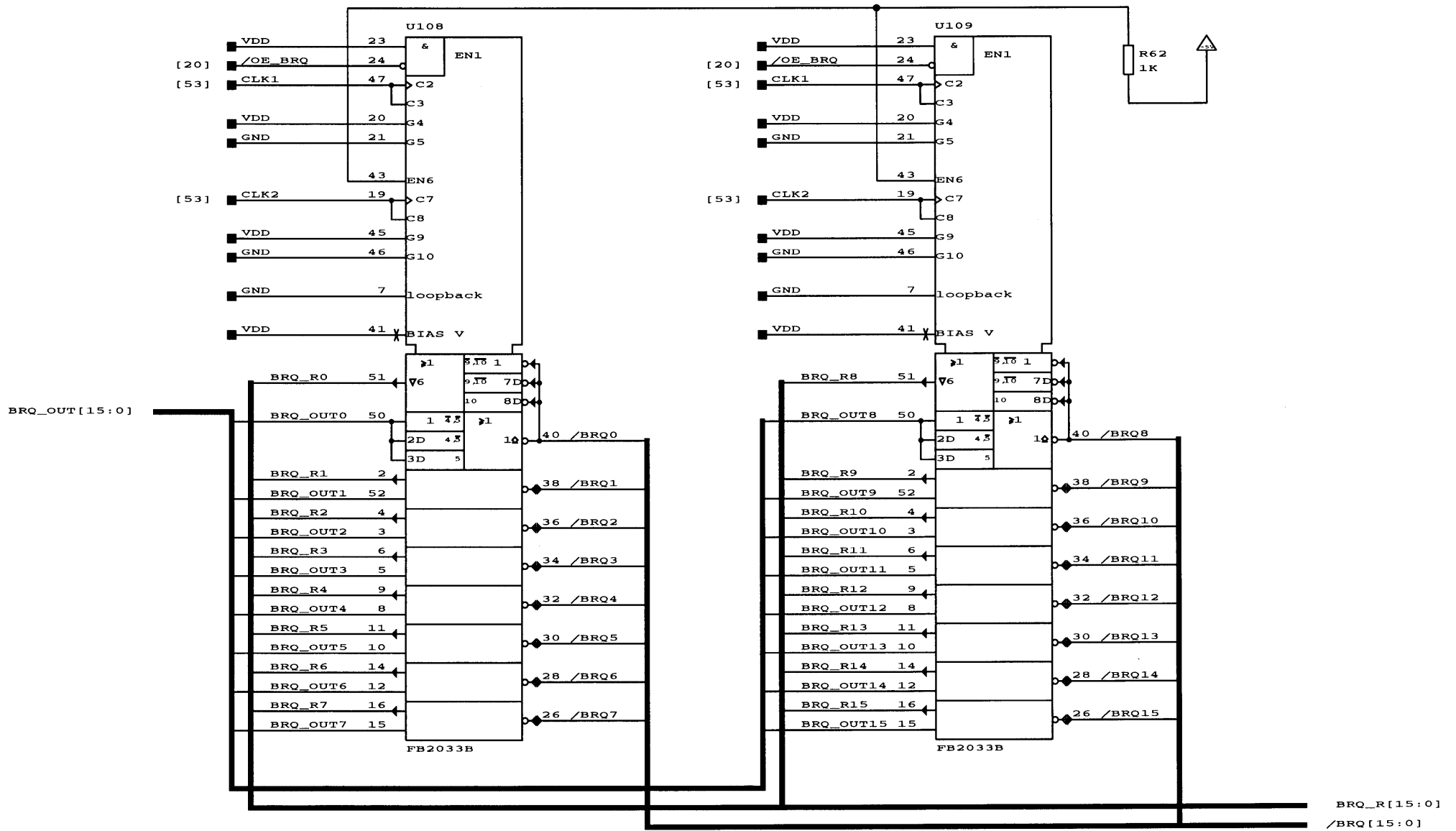


AD\_R[63:32], ADP\_R[7:4]

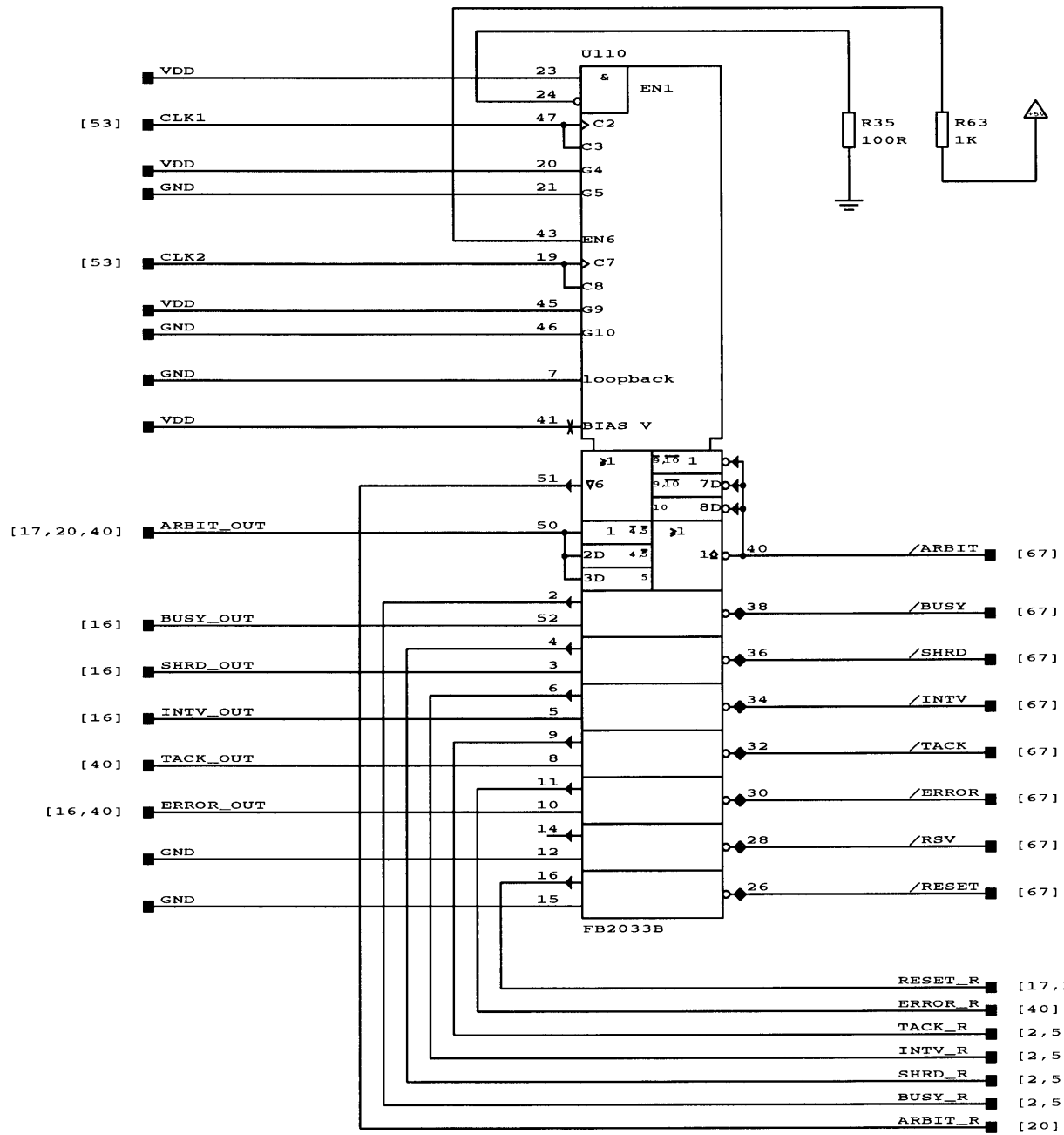
/AD[63:32], /ADP[7:4]

Issue 0	940506	CPU301 Module
Issue 1	CHG	Global address/data
Issue 2		transceiver
Issue 3		File: cpu301 Page:55 of 72

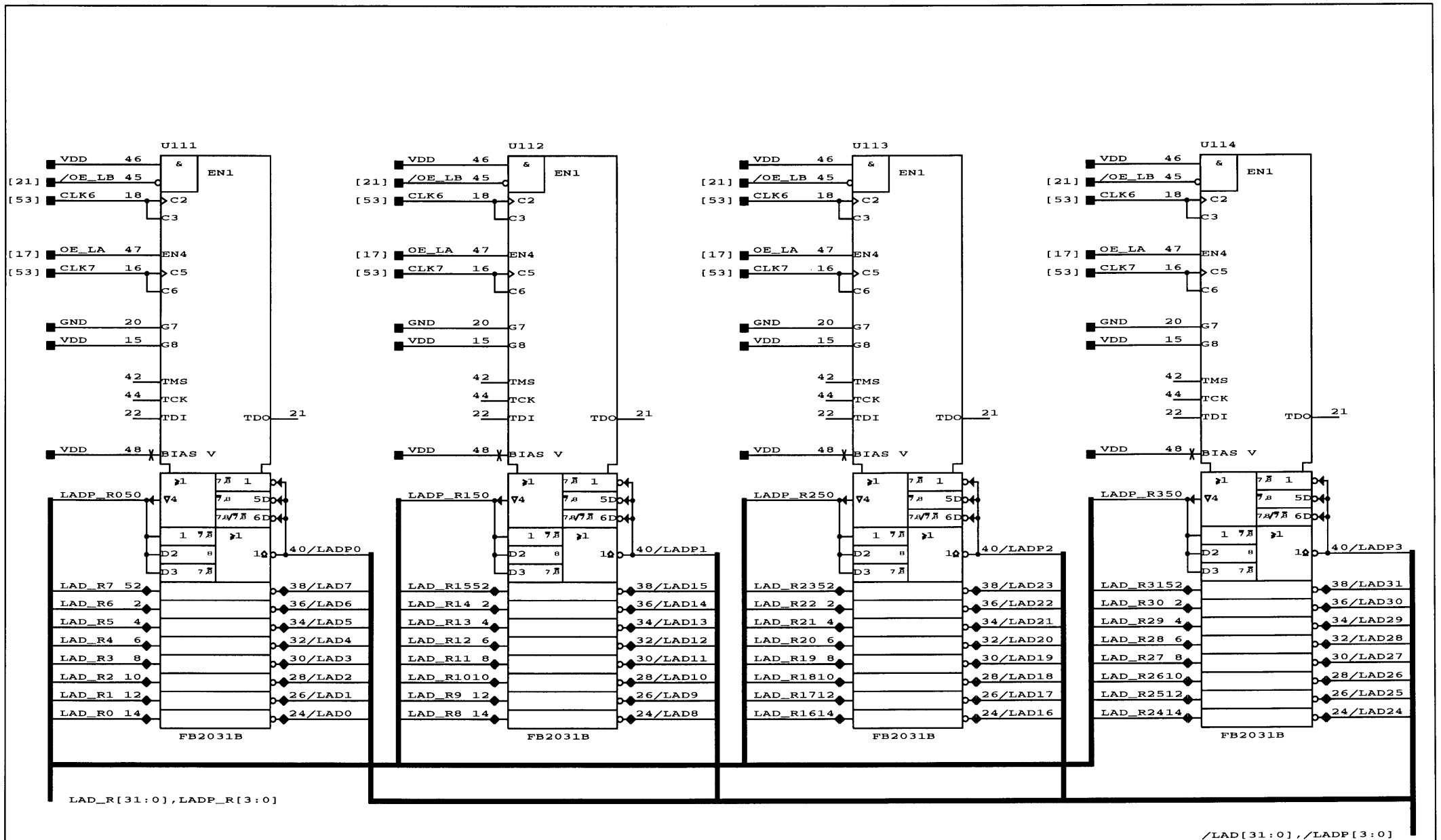





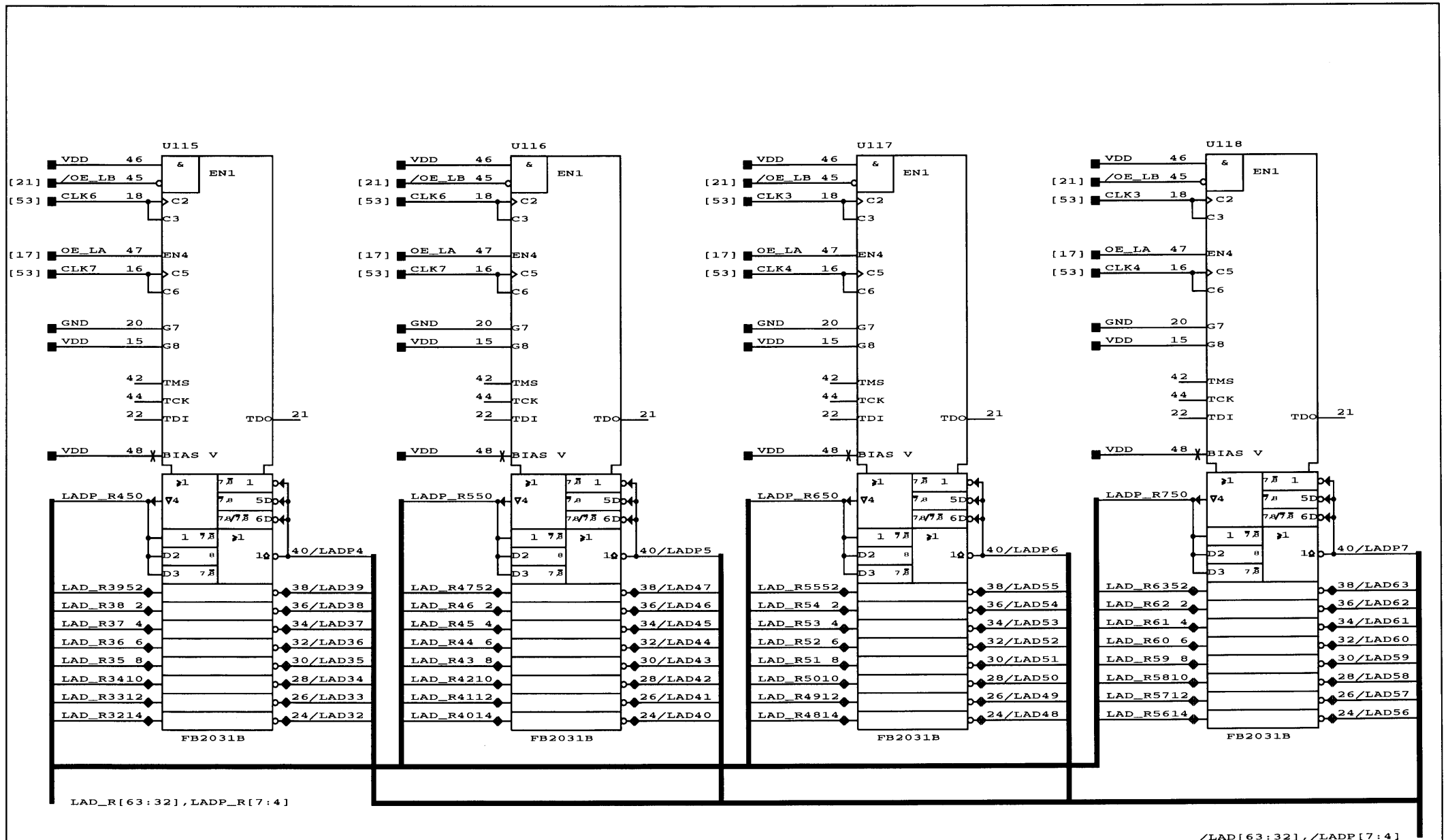
	Dansk Data Elektronik A/S	
Issue 0	940506	CPU301 Module
Issue 1		Global bus request
Issue 2		transceiver
Issue 3		File: cpu301
		Page: 57 of 72



	Dansk Data Elektronik A/S	
Issue 0	940506	CPU301 Module
Issue 1	CHG	Global control transceiver
Issue 2		
Issue 3		File: cpu301 Page:58 of 72

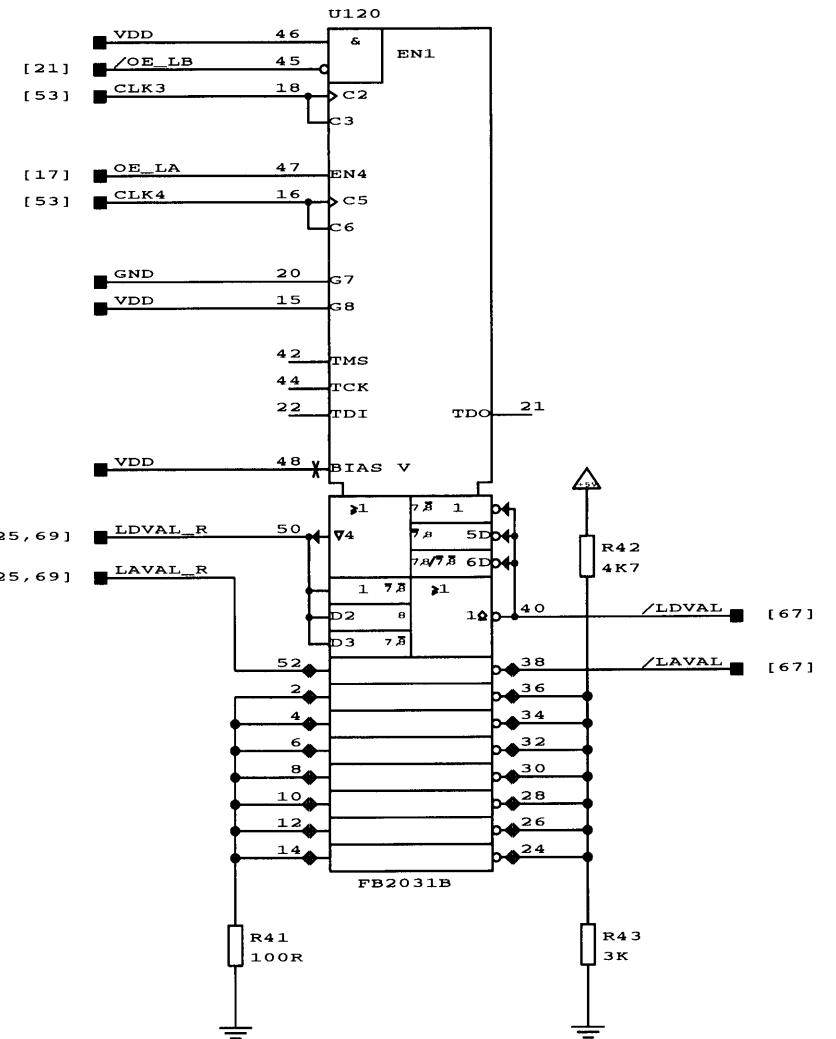
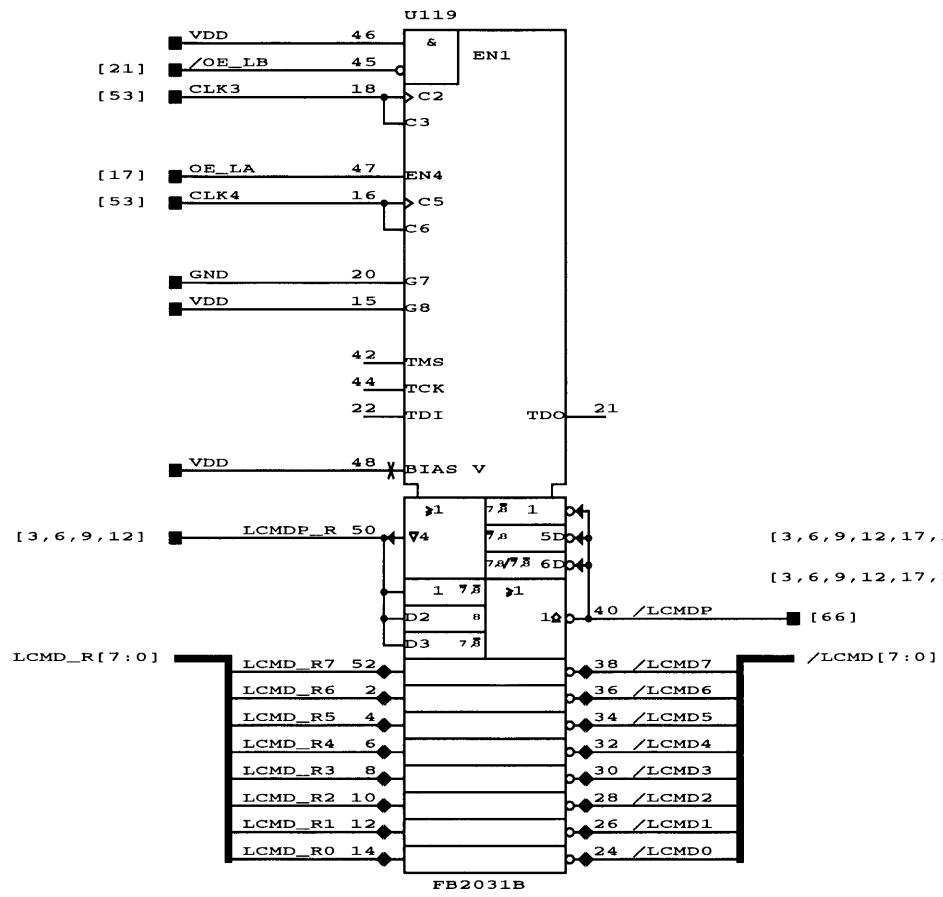


 Dansk Data Elektronik A/S		
Issue 0	940506	CPU301 Module
Issue 1	CHG	Local address/data
Issue 2		transceiver
Issue 3		File: cpu301 Page:59 of 72

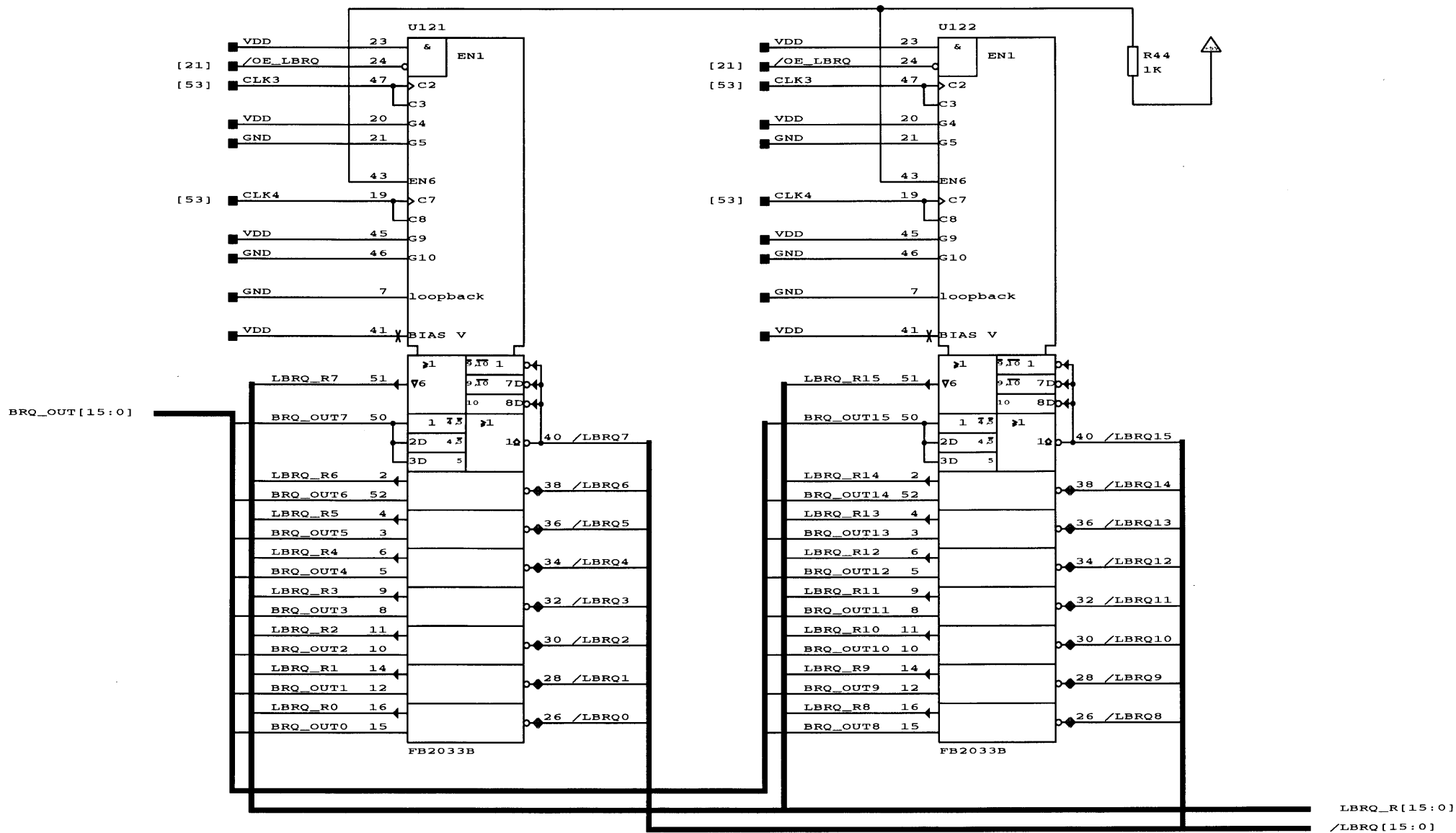


Dansk Data Elektronik A/S		
Issue 0	940506	CPU301 Module
Issue 1	CHG	Local address/data
Issue 2		transceiver
Issue 3		File: cpu301 Page:60 of 70

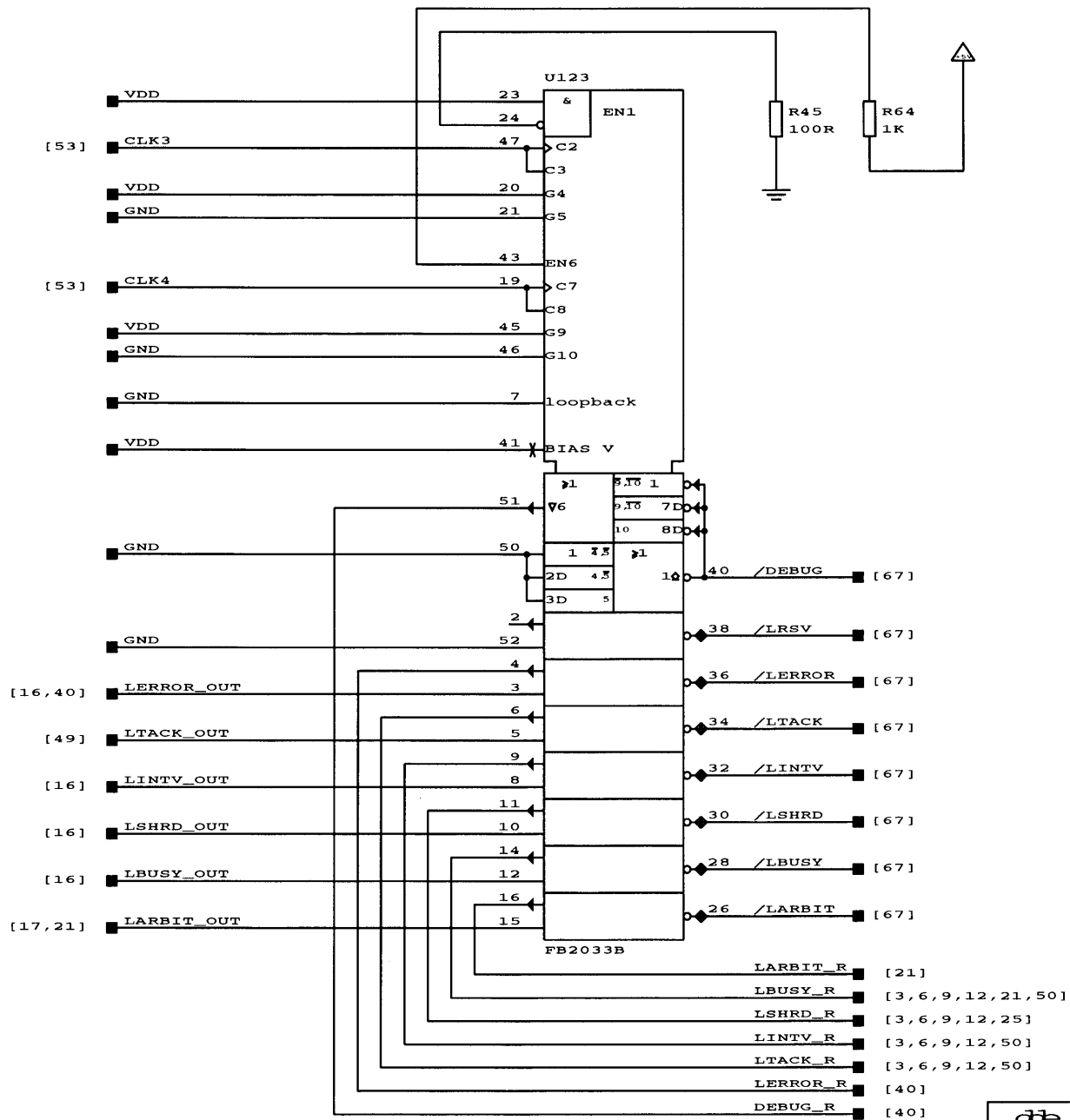




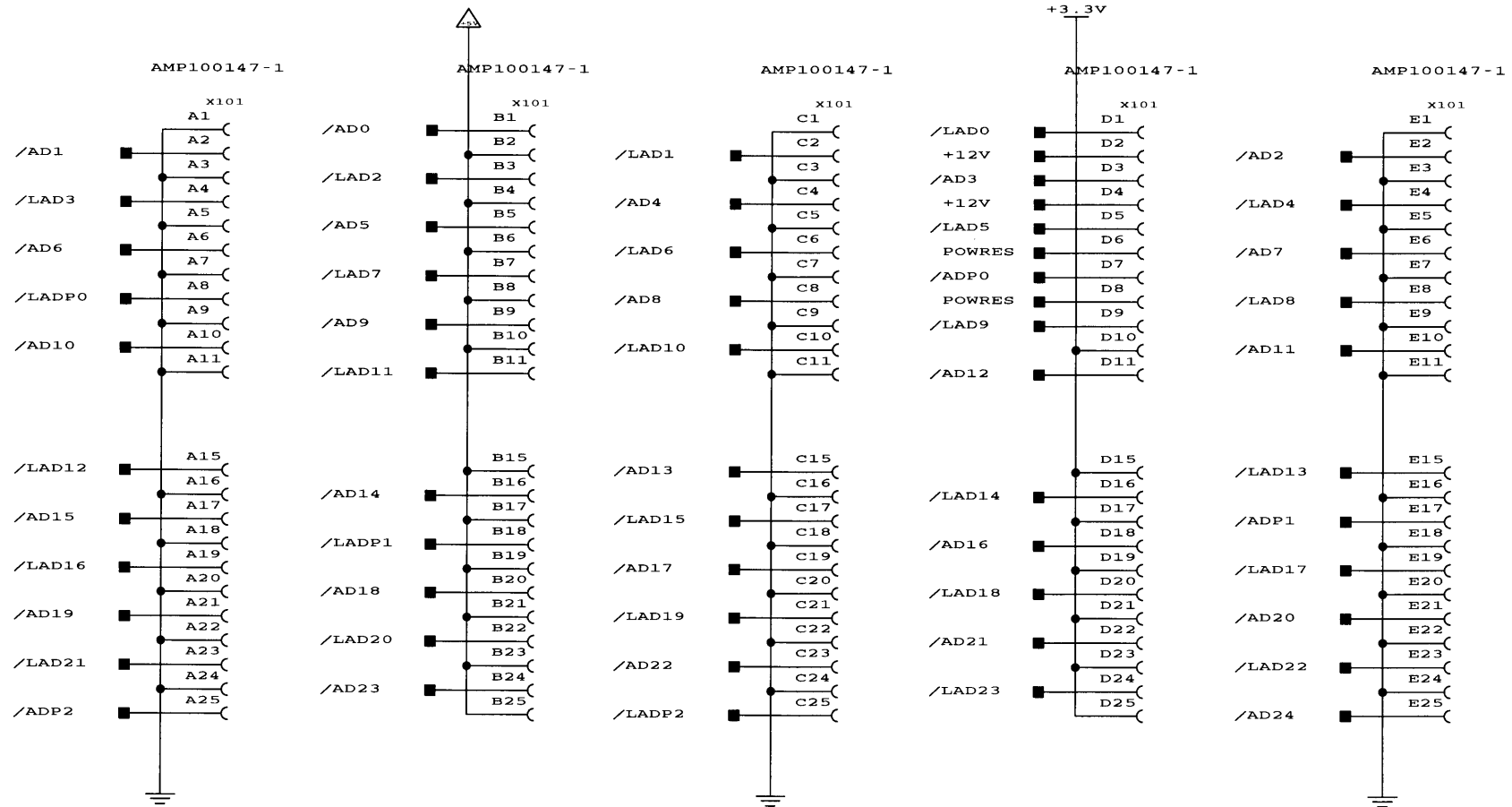
db Dansk Data Elektronik A/S			
Issue 0	940506	CPU301 Module	
Issue 1	CHG	Local command and valid	
Issue 2		transceiver	
Issue 3		File: cpu301	Page:61 of 72



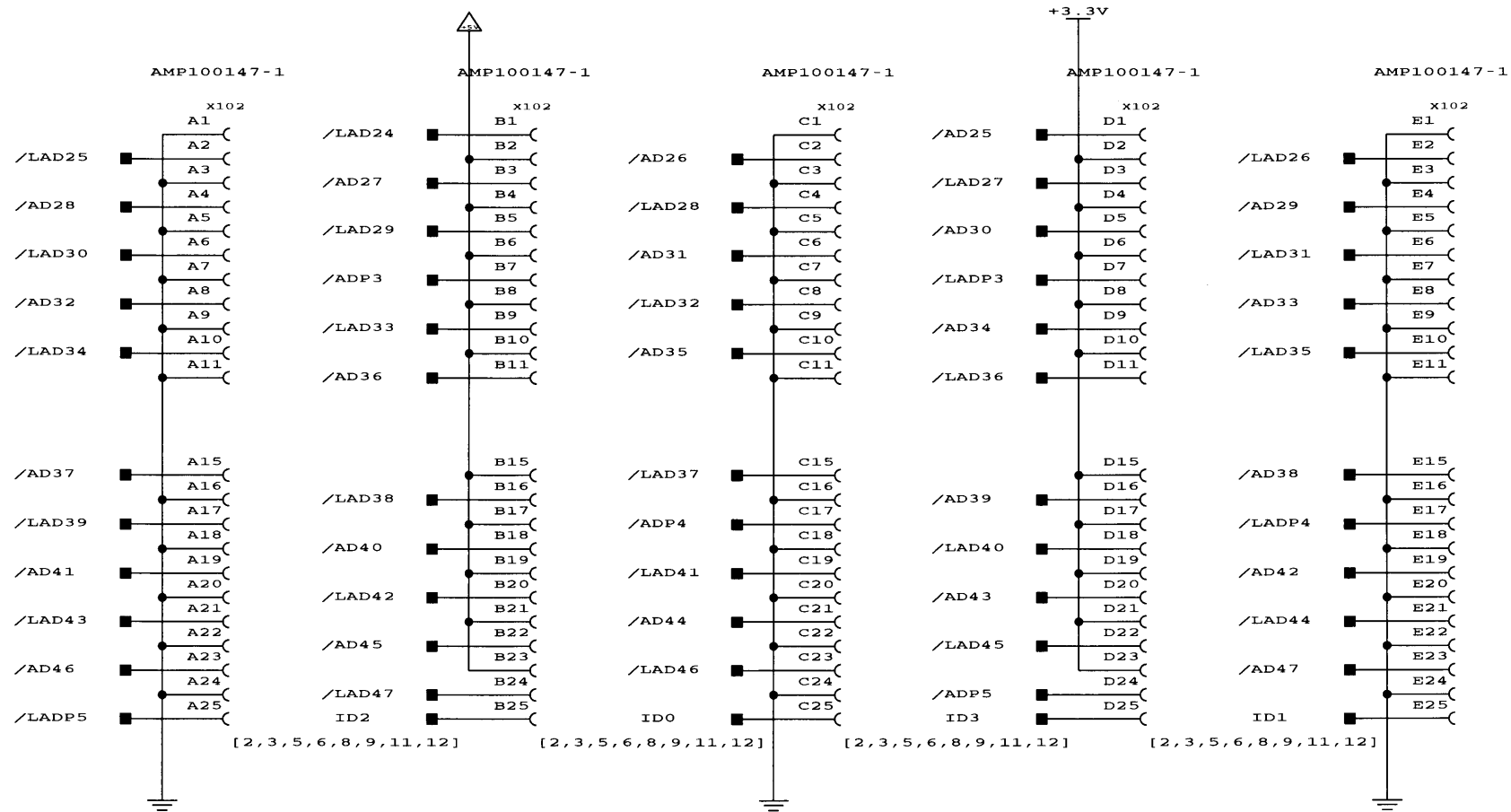
	Dansk Data Elektronik A/S	
Issue 0	940506	CPU301 Module
Issue 1	CHG	Local bus request
Issue 2		transceiver
Issue 3		File: cpu301 Page:62 of 72



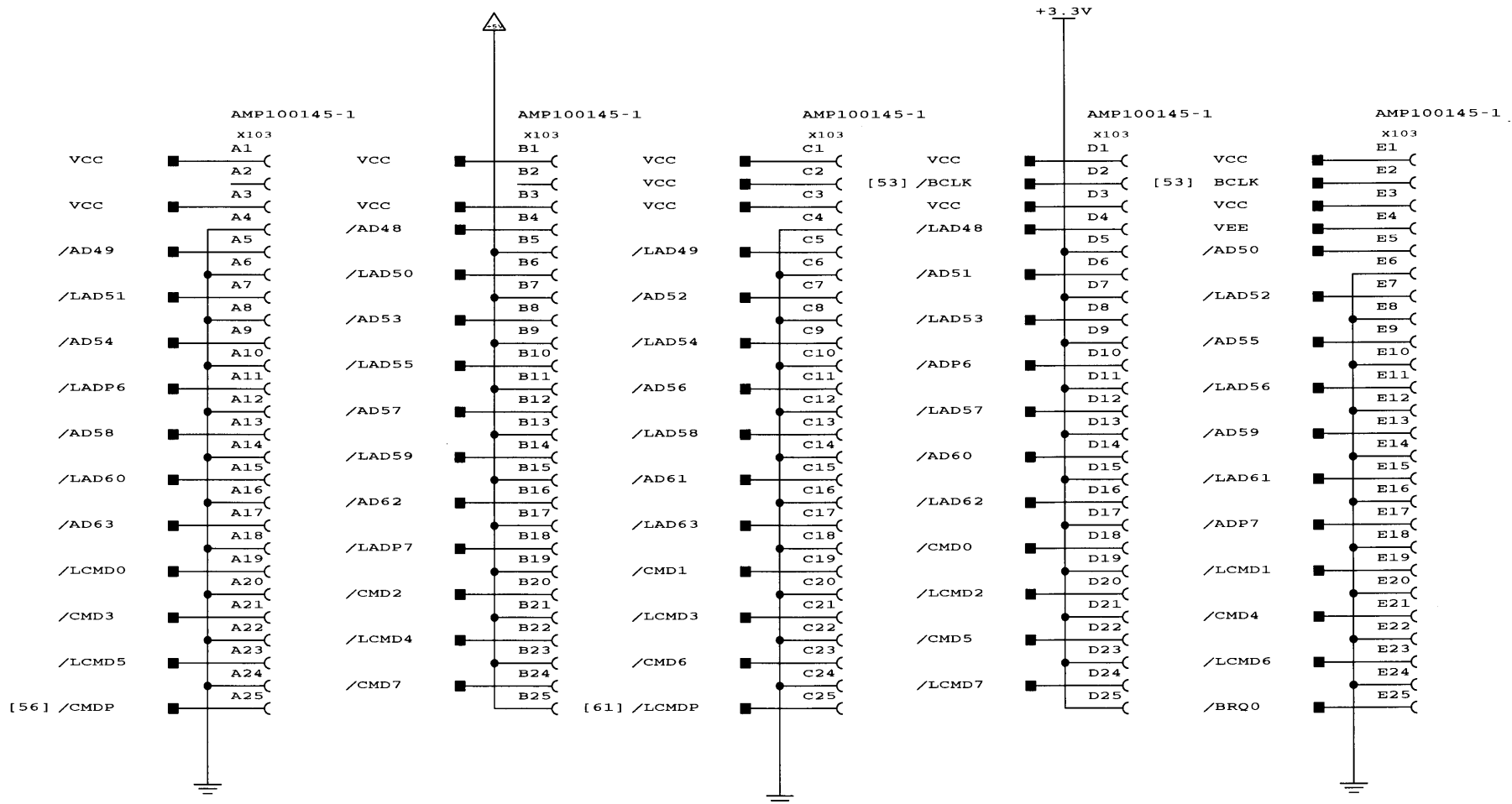
	Dansk Data Elektronik A/S	
Issue 0	940506	CPU301 Module
Issue 1	CHG	Local control transceiver
Issue 2		
Issue 3		
File: cpu301		Page: 63 of 72



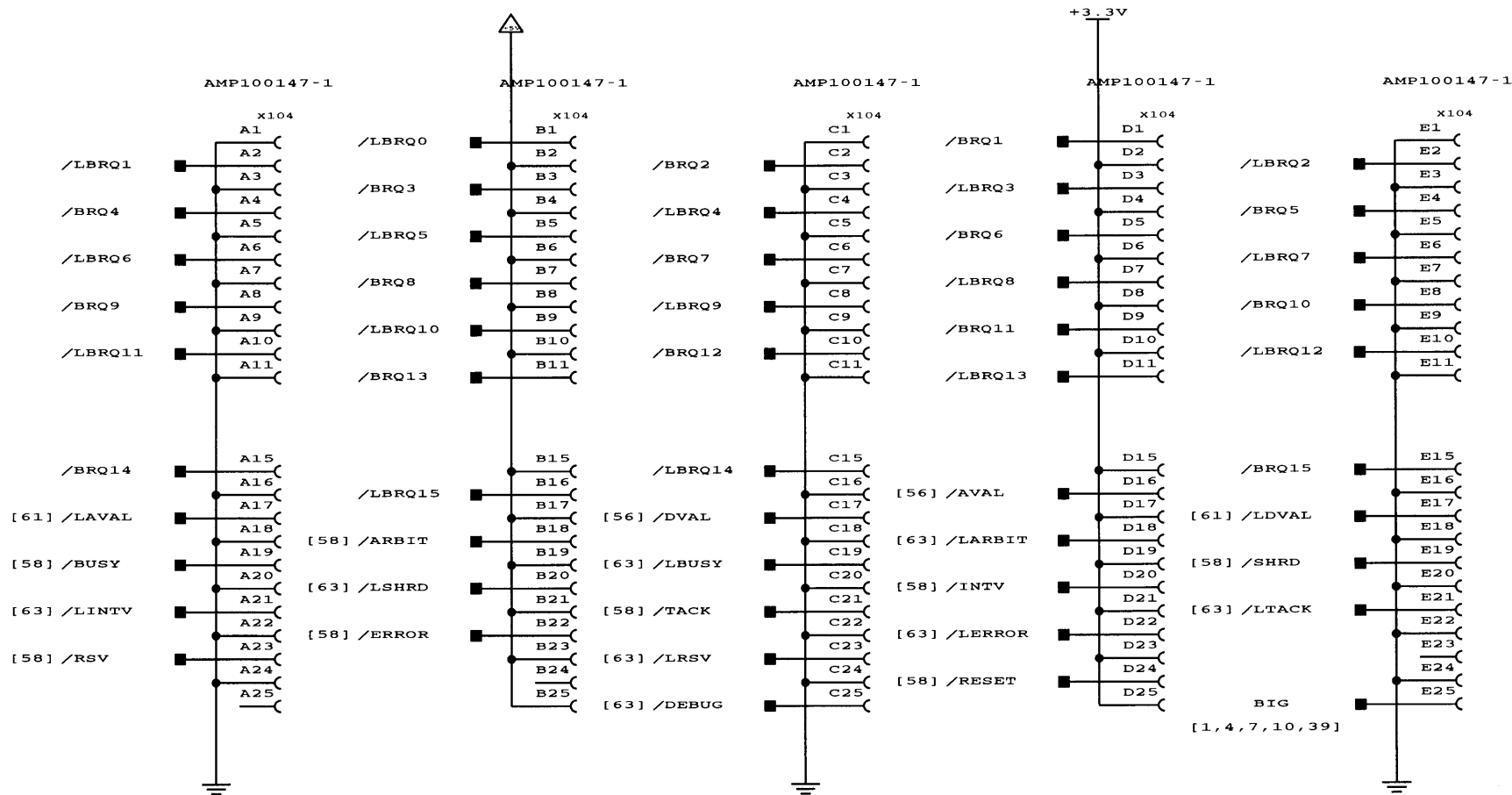
dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Connector (row 1-25)
Issue 2		
Issue 3		File: cpu301 Page: 64 of 72



dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Connector (row 26-50)
Issue 2		
Issue 3		File: cpu301 Page:65 of 72

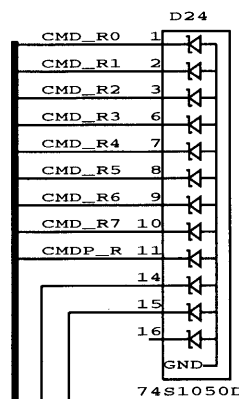
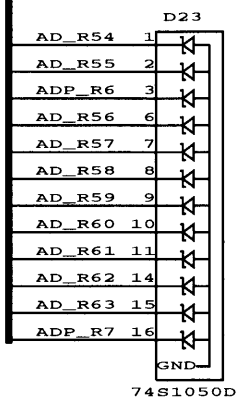
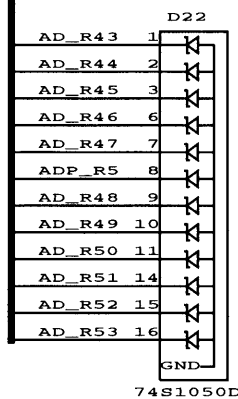
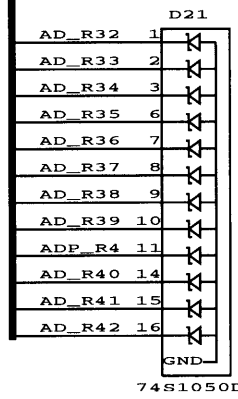
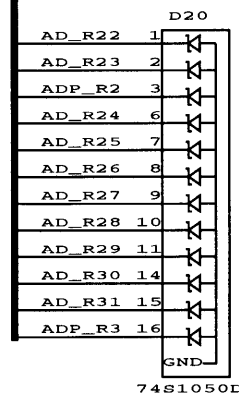
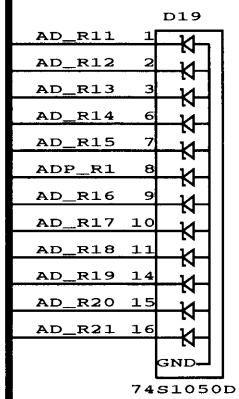
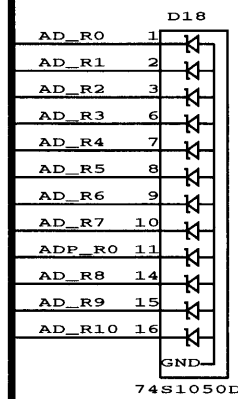


dde	Dansk Data Elektronik A/S	
Issue 0	940825	CPU301 Module
Issue 1		Connector (row 51-75)
Issue 2		
Issue 3		File: cpu301
		Page: 66 of 72



	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Connector (row 76-100)
Issue 2		
Issue 3	File: cpu301	Page: 67 of 72

AD\_R[63:0],ADP\_R[7:0]



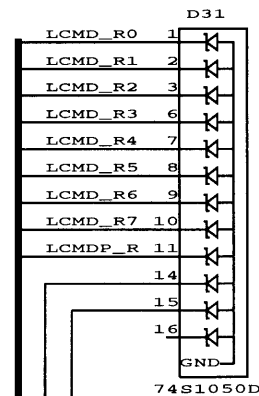
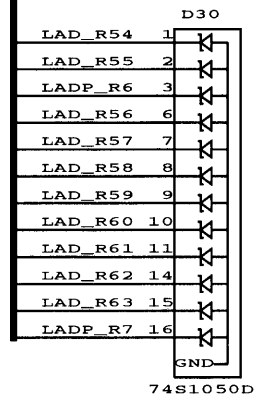
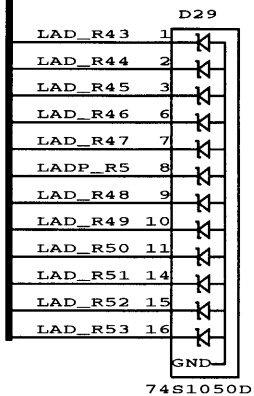
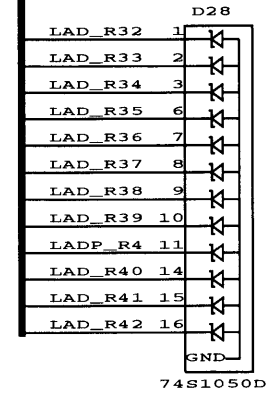
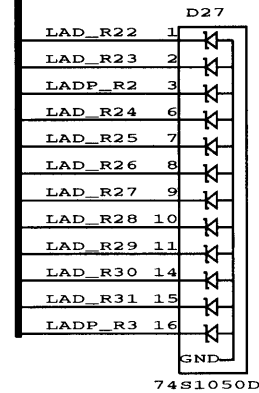
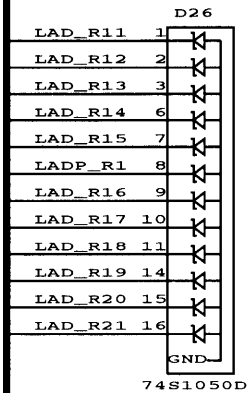
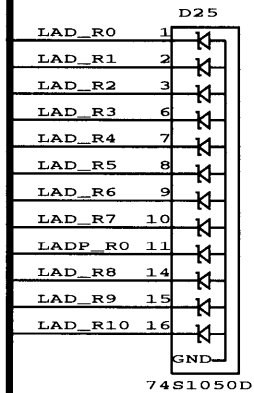
CMD\_R[7:0],CMDP\_R

[2,5,8,11,18,22,56] ■ AVAL\_R  
 [2,5,8,11,18,22,48,56] ■ DVAL\_R

		Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module	
Issue 1		Internal global bus term.	
Issue 2			
Issue 3		File: cpu301	Page:68 of 72



LAD\_R[63:0],LADP\_R[7:0]

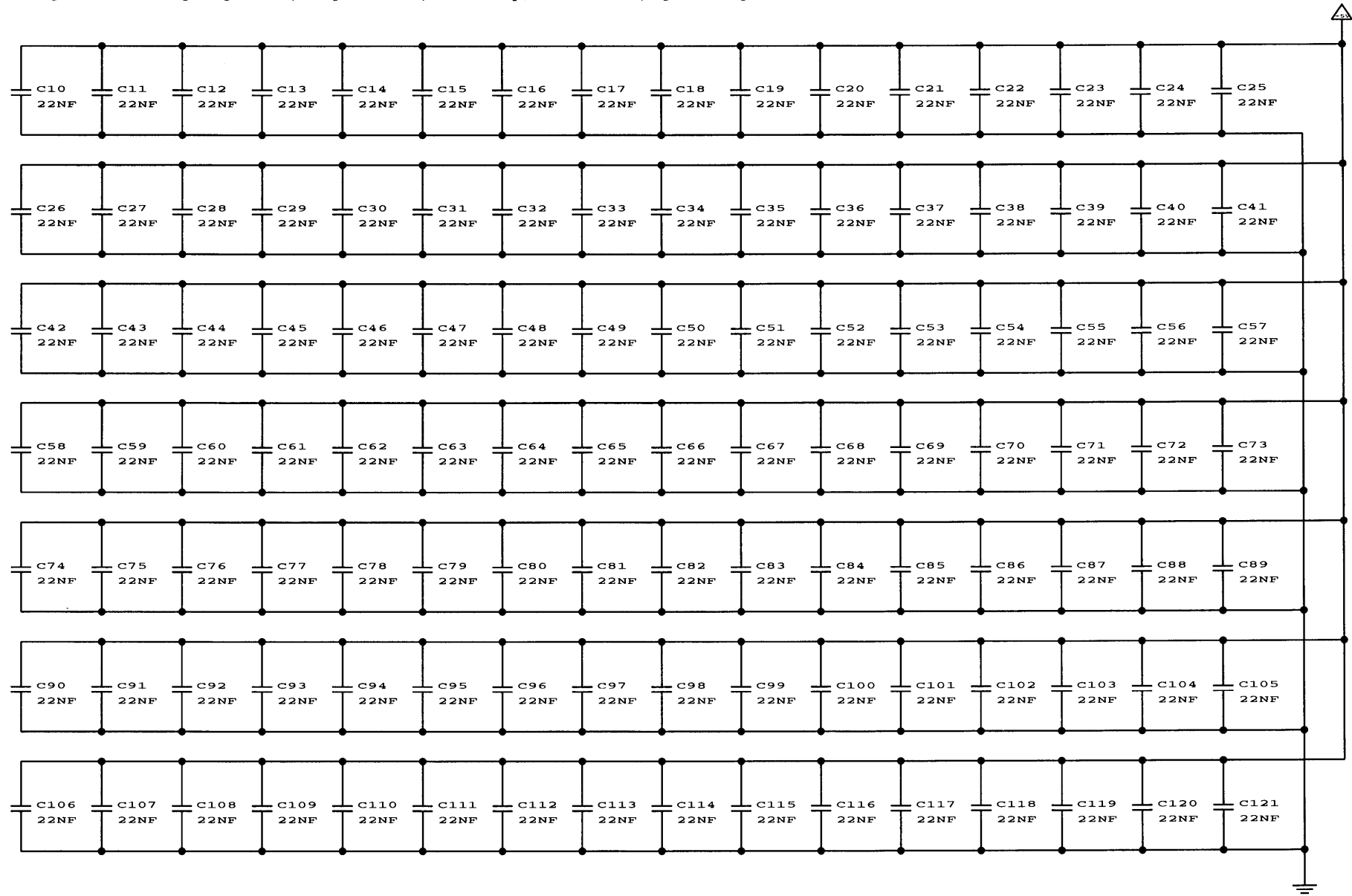



LCMD\_R[7:0],LCMDP\_R

[3,6,9,12,18,25,61] ■ LAVAL\_R  
 [3,6,9,12,18,25,52,61] ■ LDVAL\_R

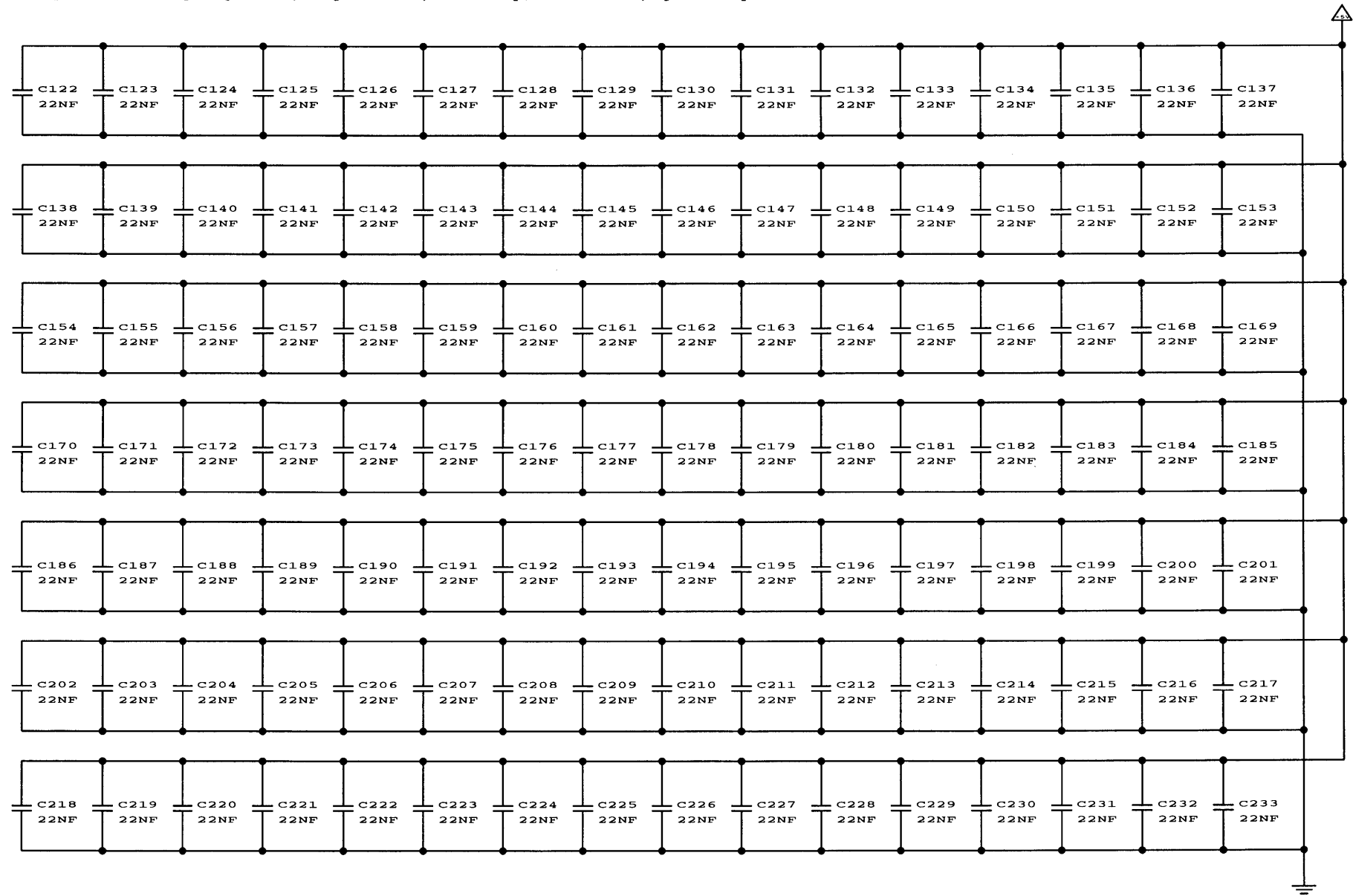
	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Internal local bus term.
Issue 2		
Issue 3		File: cpu301 Page:69 of 72


Chip level decoupling: 22nF/chip, 2\*22nF/MACH chip, and 8\*22nF/agent chip.



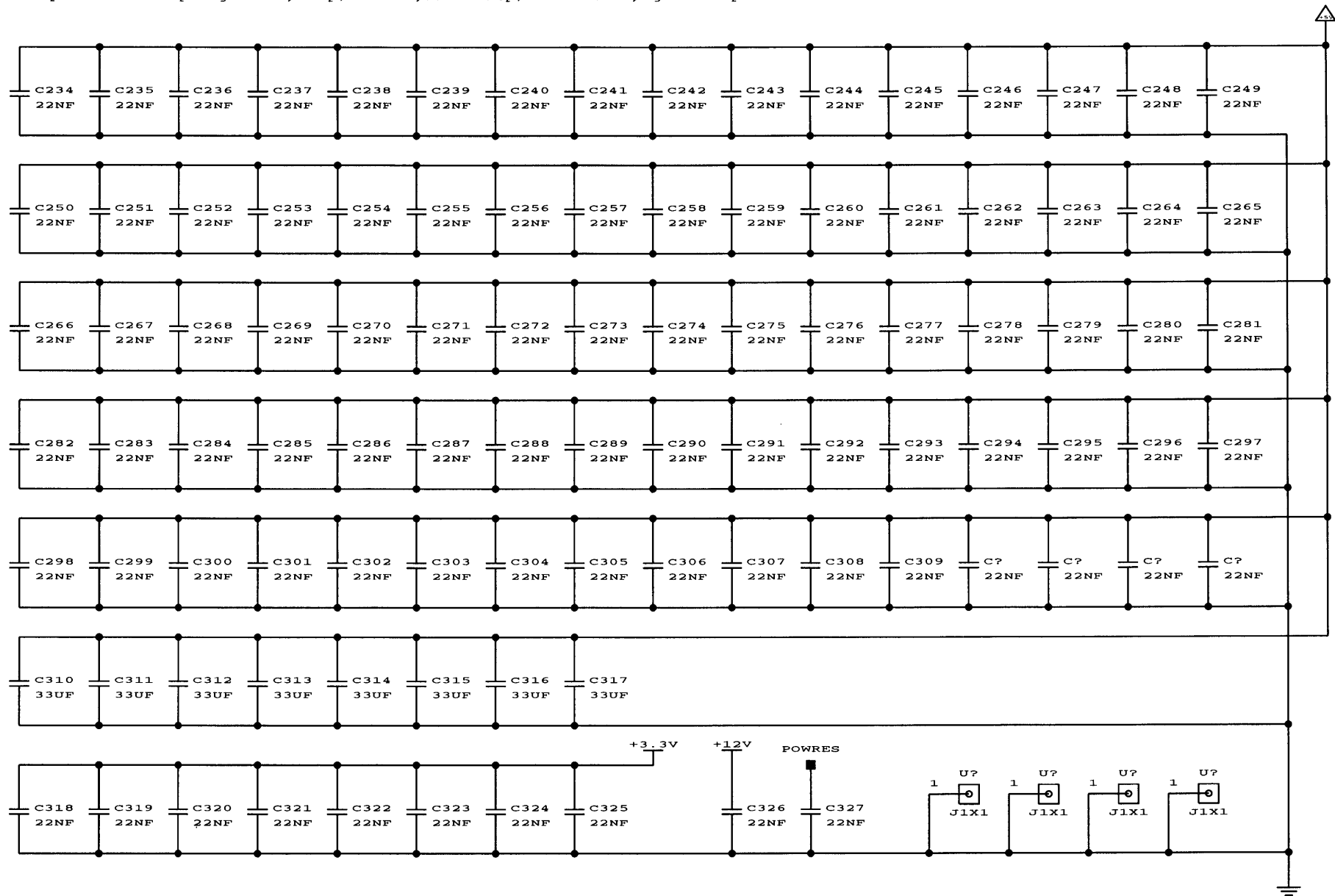
	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module Decoupling capacitors
Issue 1		
Issue 2		
Issue 3		File: cpu301 Page:70 of 72

Chip level decoupling: 22nF/chip, 2\*22nF/MACH chip, and 8\*22nF/agent chip.




	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Decoupling capacitors
Issue 2		
Issue 3		File: cpu301 Page:71 of 72

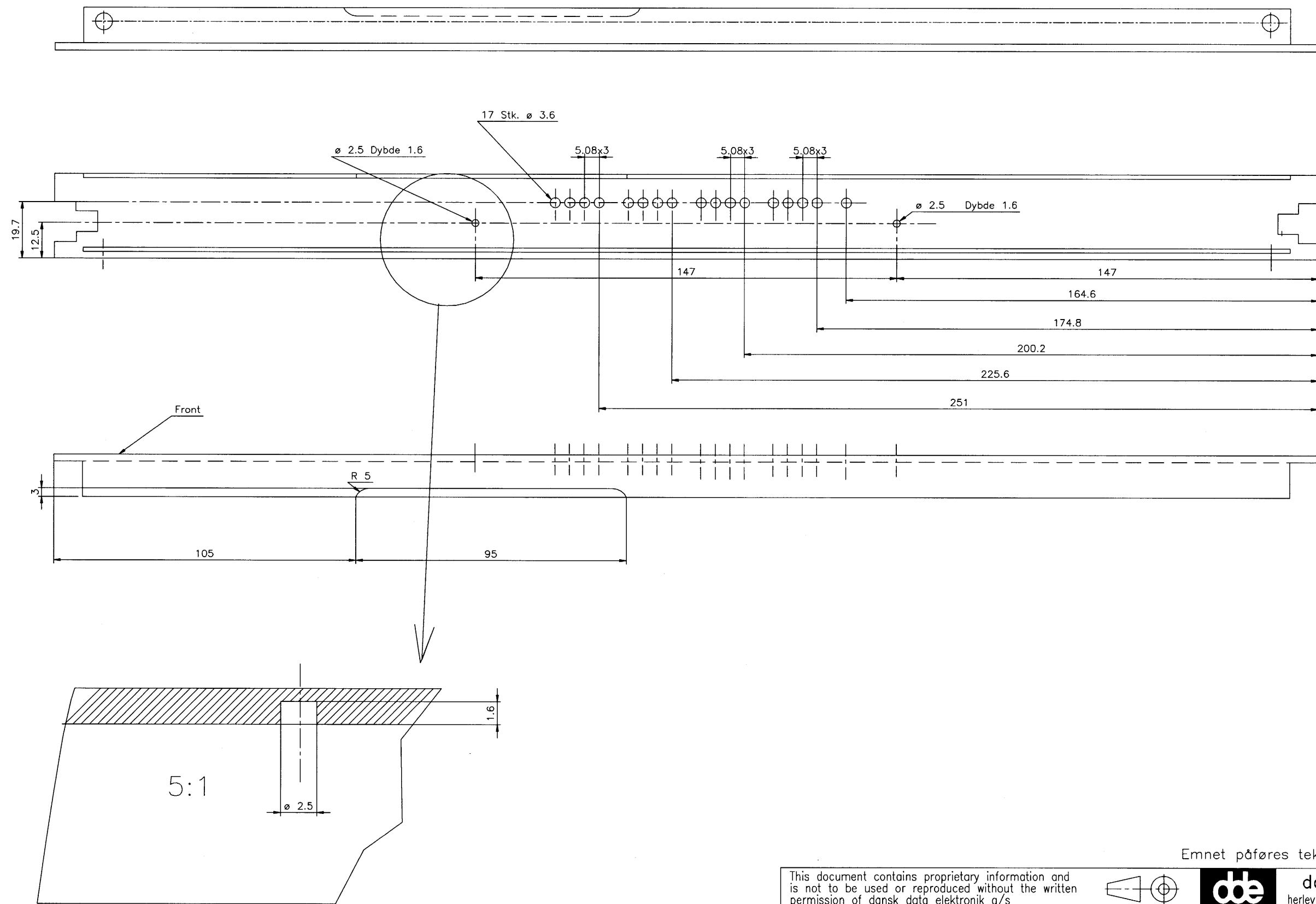
Chip level decoupling: 22nF/chip, 2\*22nF/MACH chip, and 8\*22nF/agent chip.



Decoupling at bus connector: 22nF for 3.3 V, 12 V, POWRES and 33uF for 5 V.

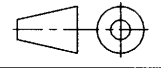

	Dansk Data Elektronik A/S	
Issue 0	940811	CPU301 Module
Issue 1		Decoupling capacitors
Issue 2		
Issue 3		File: cpu301
		Page: 72 of 72

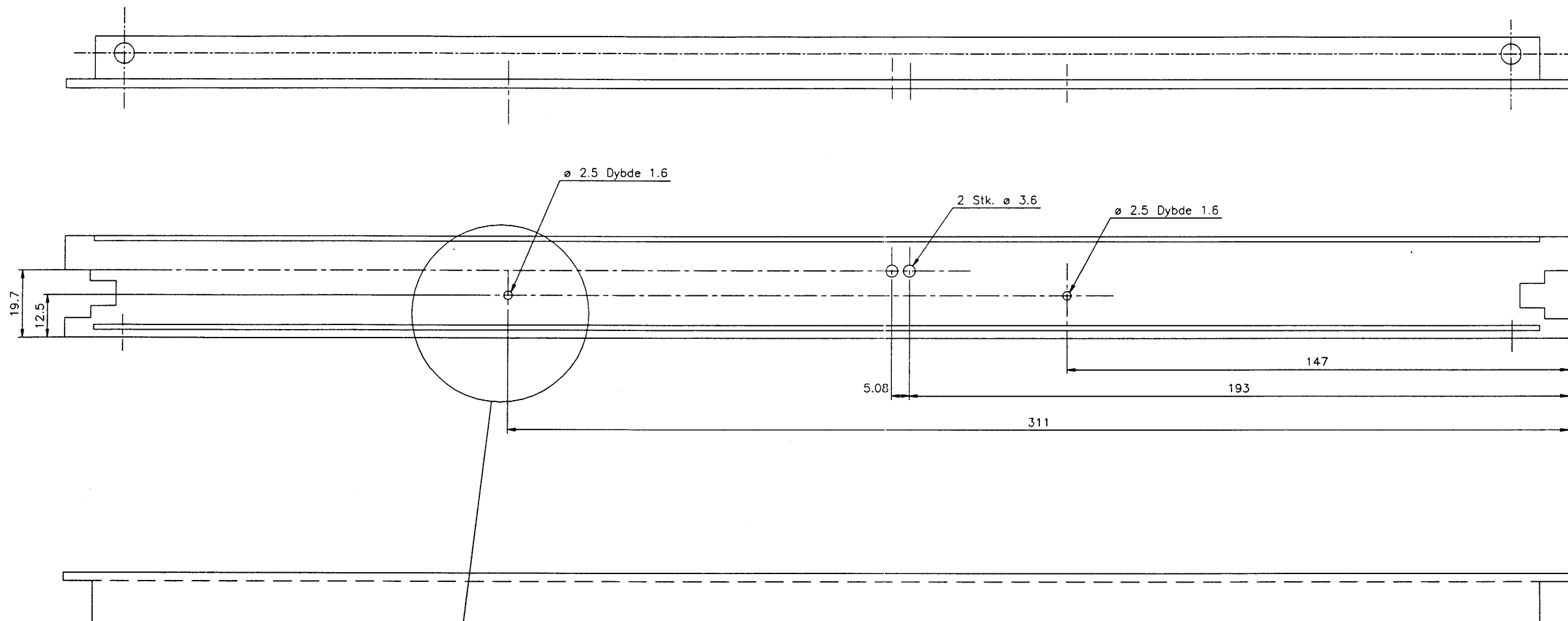




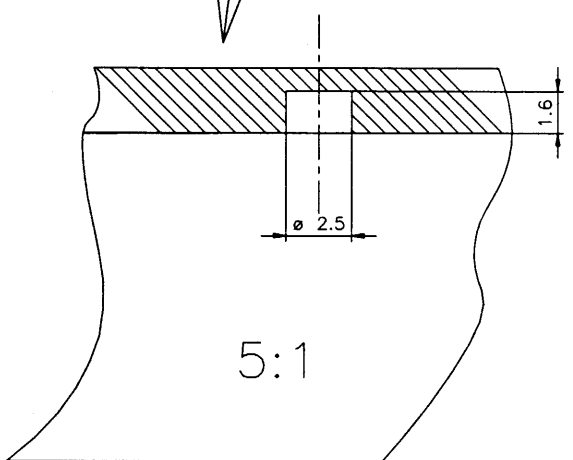
TOP

Emnet påføres tekst. Teksttegnning 99068013

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Issue	Date	Drawn	Approv.	Tol. DS/ISO 2768-m		Title SPC3 5 og 8-Pos.	
1	95.05.24	Lex		Scale:		Subjekt Forplade CPU300	
				Material		Dir. File	
				Profil 99063261		Dwg.no.	
				Finish Emnet børstes i længderetning på front AINi 20p		99063562	



TOP



Emnet børstes i længderetning, på front inden overfladebehandling  
 Overfladebehandling. Al/Ni 20p  
 Emnet påføres tekst. Teksttegning 99068010

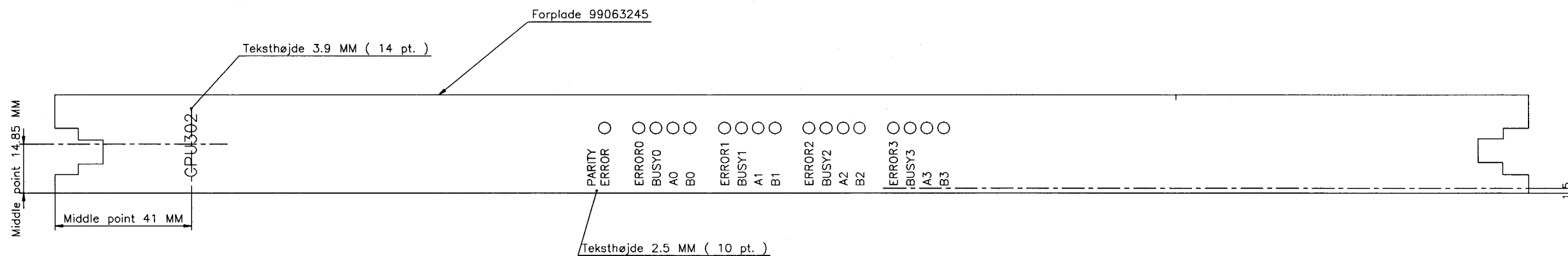
Emnet er mekanisk identisk med 99063246. Men teksten er ændret

Materiale. Forplade 99063261

Stk.	Genstand	Mrk. Nr.	Tegn. Nr.	Materiale	Model Nr.	Vegt
Firma:				Målforhold	Tegn.	941101
				1.5:1	Konf.	
					Normpr.	
Genstand:				Eretning for:		
Forplade LMEM301				99063290		
				Erettet af:		

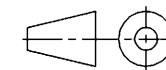






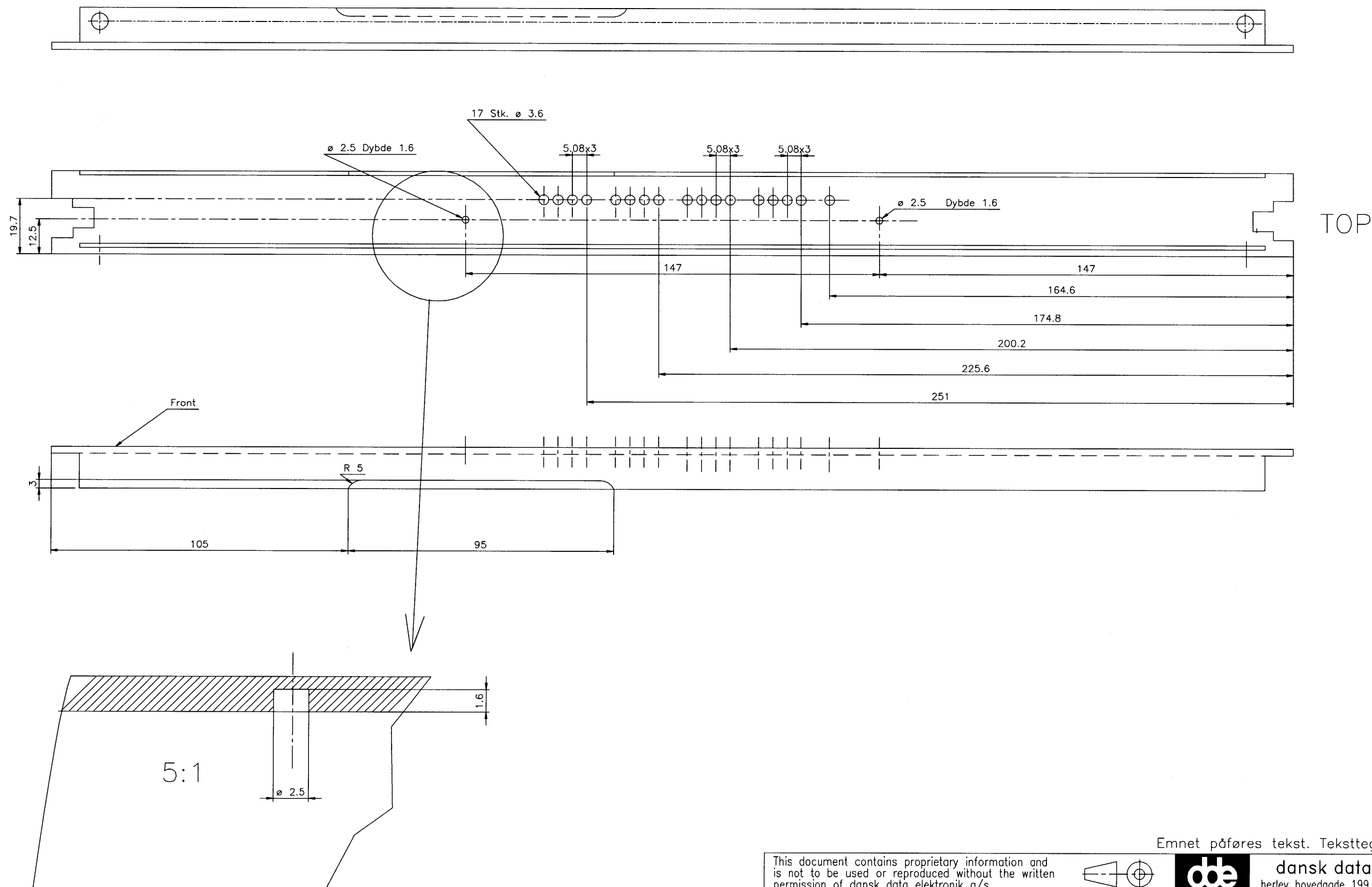
Skrifttype. Helvetica Light Farve sort

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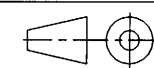
dansk data elektronik a/s  
 herlev hovedgade 199, 2730 herlev, tlf.4284 5011

Issue	Date	Drawn	Approv.	Tol. DS/ISO 2768-m	Title sPC3 CPU302
1	95.05.24	Lex		Scale: 1.5:1	Subjekt Teksttegnig
				Material	Dir. File
				Finish	Dwg.no.
					99068014



Emnet påføres tekst. Teksttegnig 99068014

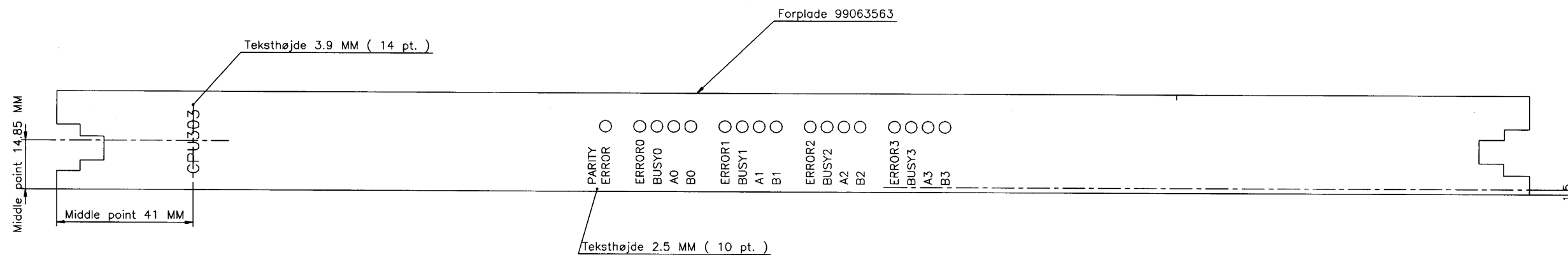
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dansk data elektronik a/s  
herlev hovedgade 199, 2730 herlev, tlf.4284 5011

Issue	Date	Drawn	Approv.	Tol. DS/ISO 2768-m
1	95.05.24	Lex		Scale:
				Material Profil 99063261
				Finish Emnet børstes i længderetning på front AINi 20p

Title SPC3 5 og 8-Pos.
Subjekt Forplade CPU302
Dir. File
Dwg.no. 99063563



Skrifttype. Helvetica Light Farve sort

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Issue	Date	Drawn	Approv.	Tol. DS/ISO 2768-m		Title SPC3 CPU303	
1	95.08.31	Lex		Scale: 1.5:1		Subjekt Teksttegnig	
				Material		Dir. File	
				Finish		Dwg.no. 99068017	

## PARTS LIST

Module: CPU301-0

Date: 941209

Page: 1/2

Part no	Device	Qty	Comp
99020850	22NF	315	C1, C10-313, C322-331
99020851	4.7UF	1	C2
99020849	33UF	8	C314-321
99021413	LED 3mm red h.prf.	5	D1, D5, D9, D13, D17
99021412	LED 3mm green h.prf.	12	D2-4, D6-8, D10-12, D14-16
99000227	74S1050D	14	D18-31
99022027	1.000MHZ	1	OSC1
99020305	100R	28	R1-9, R15, R17, R19, R21, R23, R25 R27, R29, R31-32, R35, R38-39, R41 R45, R60-61, R65, R68
99020307	82R	2	R10, R12
99020308	130R	2	R11, R13
99020306	220R	10	R14, R16, R18, R20, R22, R24, R26, R28 R30, R59
99020303	4K7	7	R33, R42, R66-67, R69-70, R92
99020327	3K	2	R34, R43
99020301	1K	14	R40, R44, R50, R52, R54, R56, R62-64, R86-90
99020309	560R	17	R46-48, R72-84, R91
99022235	Netw. 4820P-002-472	1	R36
99022234	Netw. 4820P-002-102	1	R93
99020322	OR	4	R95, R98, R101, R104
99011701	CA302	8	U1-8
99002411	74F1808D	2	U9, U11
99002412	74F1832D	2	U10, U12
99000831	74AS20D	3	U13-14, U16
99002413	74F377D	2	U17, U25
99010216	PAL20R8-5JC	4	U18-19, U21, U23
99010902	MACH110-20JC	4	U20, U78, U85, U94
99010904	MACH210-12JC	8	U22, U24, U138-139, U141, U143-144 U146
99002222	74FCT16823BTPV	8	U26-27, U48-49, U81-84
99011223	MCM6706AJ10	20	U28-29, U33-34, U38-39, U43-44 U50-51, U55-56, U60-61, U65-66 U140, U142, U145, U147
99002223	74FCT16244ATPV	14	U30, U35, U40, U45, U52, U57, U62, U67 U77, U89-93
99002221	74FCT521BTSO	18	U31-32, U36-37, U41-42, U46-47 U53-54, U58-59, U63-64, U68-70, U88
99010908	MACH220-15JC	1	U71
99012095	N82S123AA / Am27S19AJC	2	U72-73
99002219	74FCT16501ATPV	1	U74
99002408	74F280BD	3	U75-76, U80
99012114	AM29C040-120JC	1	U79
99010604	PALCE16V8H-7JC	3	U86-87, U95
99011218	CY7B991-7JC	1	U96
99005033	MC100H641FN	1	U97
99002500	FB2031BB	20	U98-107, U111-120
99002501	FB2033BB	6	U108-110, U121-123
99001040	74ALS240D	2	U124-125
99000472	74LS393D	3	U127-129
99002405	74F74D	2	U130-131
99000832	74AS30D	3	U132-134
99010022	PAL16R6-5JC	2	U136-137
99002407	74F244D	1	U148
99000830	74AS1004D	1	U149
99040124	3M8062011549-5	16	X00-03, X10-13, X20-23, X30-33
99040111	AMP100147-1	3	X101-102, X104

PARTS LIST

Module: CPU301-0

Date: 941209 Page: 2/2

<u>Part no</u>	<u>Device</u>	<u>Qty</u>	<u>Comp</u>
99040110	AMP100145-1	1	X103
99023228	20-pin PLCC socket	7	U72-73,U86-87,U95,U136-137
99023229	28-pin PLCC socket	4	U18-19,U21,U23
99023230	32-pin PLCC socket	1	U79
99023231	44-pin PLCC socket	12	U20,U22,U24,U78,U85,U94, U138-139,U141,U143-144,U146
99023232	68-pin PLCC socket	1	U71
99750101	Mech. parts CPU301	1	
99030320	PCB CPU301 Issue 1	1	

PLD list

Part no: 99750020  
 Status: Preliminary  
 Init: OHM

Module: CPU301-0  
 Date: 941031

Pcb no:  
 Page: 1 / 1

<u>Label</u>	<u>Pos.</u>	<u>Part no.</u>	<u>Type</u>	<u>X-pgm.</u>	<u>File</u>	<u>Checksum</u>
c31010	U18	99010216	PAL20R8-5JC		c31010.jed	DEF0
c31010	U19	99010216	PAL20R8-5JC		c31010.jed	DEF0
c31020	U136	99010022	PAL16R6-5JC		c31020.jed	2BE2
c31020	U137	99010022	PAL16R6-5JC		c31020.jed	2BE2
c31030	U20	99010902	MACH110-20JC		c31030.jed	B930
c31040	U21	99010216	PAL20R8-5JC		c31040.jed	B626
c31040	U23	99010216	PAL20R8-5JC		c31040.jed	B626
c31050	U22	99010904	MACH210-12JC		c31050.jed	2E46
c31050	U24	99010904	MACH210-12JC		c31050.jed	2E46
c31060	U138	99010904	MACH210-12JC		Ikke klar	
c31060	U143	99010904	MACH210-12JC		Ikke klar	
c31070	U139	99010904	MACH210-12JC		Ikke klar	
c31070	U141	99010904	MACH210-12JC		Ikke klar	
c31070	U144	99010904	MACH210-12JC		Ikke klar	
c31070	U146	99010904	MACH210-12JC		Ikke klar	
c31080	U71	99010908	MACH220-15JC		c31080.jed	004F
c31090	U78	99010902	MACH110-20JC		c31090.jed	E876
c31100	U85	99010902	MACH110-20JC		c31100.jed	604D
c31100	U94	99010902	MACH110-20JC		c31100.jed	604D
c31110	U86	99010604	PALCE16V8H-7JC	R6	c31110.jed	234F
c31110	U95	99010604	PALCE16V8H-7JC	R6	c31110.jed	234F
c31120	U87	99010604	PALCE16V8H-7JC	R8	c31120.jed	2470

Dansk Data Elektronik A/S  
 Herlev Hovedgade 199, 2730 Herlev  
 tlf.: (+45) 42 84 50 11, fax: (+45) 42 84 52 20

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\*\*\*\*\*li2\*\*\*\*\*

Dato : 04.03.94.  
 Udgave : 0-3

<u>BETEGNELSE</u>	<u>LEV.</u>	<u>INTVARENR</u>	<u>TEGN</u>	<u>ARKIV</u>
Mekaniske dele CPU 301	dde	750101		

UNDERPRODUKTER

<u>POS</u>	<u>BETEGNELSE</u>	<u>i</u>	<u>LEV.</u>	<u>ANT.</u>	<u>INTVARENR</u>	<u>TEGN</u>	<u>ARKIV</u>
1	Forplade CPU301		pum	1	99063245		
2	Vinkel for SPC 3 kort		pum	1	99063221		
3	Stag M 3 6-kt L8MM(R6332-02)		sfc	4	99062998		
4	Printlås sort Schroff20839-073		kwe	2	99062994		
5	EMC-Fjeder Venstre		pum	1	99062990		
6	Tape for EMC Fjeder		mmm	1	99062991		
7	skrue M 3x5 PHJX-Z 9041		hfc	8	99060561		
8	skrue M2.5x8 PHJX-Z 9041		hfc	2	99060504		
9	Skive 2.5 DIN6798A HFC 1221		hfc	2	99062995		
10	Styretap Schroff 60839-035		kwe	2	99063224		
11	skive 3 DIN 6798A HFC 1221		hfc	4	99060562		
12	Tekst CPU301	*	dpr		99068005		

'\*' i 'i' : dele med egen stykliste

**DESIGN NOTE**

Name:	CA302 Pin Assignment
Date:	94-08-02
Author:	aaj
Version:	4.0
Document:	design note 6

**Contents**

**page**

1	CA302 PIN ASSIGNMENTS .....	2
2	GND and VDD CALCULATIONS .....	6





**1 CA302 PIN ASSIGNMENTS**

LOAD				LOAD			
PIN	SIGNAL	BUFFER	pF	PIN	SIGNAL	BUFFER	pF
✓ 1	BC60	IOS1G	80	✓ 31	VDD	PWRCO	
✓ 2	BC50	IOS1G	80	✓ 32	B470	IOS1G	80
✓ 3	BC40	IOS1G	80	✓ 33	B460	IOS1G	80
✓ 4	BC30	IOS1G	80	✓ 34	B450	IOS1G	80
✓ 5	VDD	PWRPY		✓ 35	B440	IOS1G	80
✓ 6	BC20	IOS1G	80	✓ 36	B430	IOS1G	80
✓ 7	BC10	IOS1G	80	✓ 37	B420	IOS1G	80
✓ 8	BC00	IOS1G	80	✓ 38	B410	IOS1G	80
✓ 9	<u>BP70</u>	IOS1G	80	✓ 39	B400	IOS1G	80
✓ 10	<u>B630</u>	IOS1G	80	✓ 40	GND	GNDPY	
✓ 11	B620	IOS1G	80	✓ 41	<u>BP40</u>	IOS1G	80
✓ 12	B610	IOS1G	80	✓ 42	B390	IOS1G	80
✓ 13	B600	IOS1G	80	✓ 43	B380	IOS1G	80
✓ 14	B590	IOS1G	80	✓ 44	B370	IOS1G	80
✓ 15	B580	IOS1G	80	✓ 45	B360	IOS1G	80
✓ 16	GND	GNDPY		✓ 46	B350	IOS1G	80
✓ 17	B570	IOS1G	80	✓ 47	B340	IOS1G	80
✓ 18	B560	IOS1G	80	✓ 48	B330	IOS1G	80
✓ 19	<u>BP60</u>	IOS1G	80	✓ 49	B320	IOS1G	80
✓ 20	B550	IOS1G	80	✓ 50	<u>BP30</u>	IOS1G	80
✓ 21	B540	IOS1G	80	✓ 51	VDD	PWRPY	
✓ 22	B530	IOS1G	80	✓ 52	B310	IOS1G	80
✓ 23	B520	IOS1G	80	✓ 53	B300	IOS1G	80
✓ 24	B510	IOS1G	80	✓ 54	B290	IOS1G	80
✓ 25	B500	IOS1G	80	✓ 55	B280	IOS1G	80
✓ 26	B490	IOS1G	80	✓ 56	B270	IOS1G	80
✓ 27	VDD	PWRPY		✓ 57	B260	IOS1G	80
✓ 28	B480	IOS1G	80	✓ 58	B250	IOS1G	80
✓ 29	<u>BP50</u>	IOS1G	80	✓ 59	B240	IOS1G	80
✓ 30	GND	GNDCO		✓ 60	<u>BP20</u>	IOS1G	80

				LOAD					LOAD
	PIN	SIGNAL	BUFFER	pF		PIN	SIGNAL	BUFFER	pF
✓	61	B230	IOS1G	80	✓	91	VDD	PWRCO	
✓	62	GND	GNDPY		✓	92	P000	IOS1G	50
✓	63	B220	IOS1G	80	✓	93	P010	IOS1G	50
✓	64	B210	IOS1G	80	✓	94	P020	IOS1G	50
✓	65	B200	IOS1G	80	✓	95	P030	IOS1G	50
✓	66	B190	IOS1G	80	✓	96	P040	IOS1G	50
✓	67	B180	IOS1G	80	✓	97	VDD	PWRPY	
✓	68	B170	IOS1G	80	✓	98	P050	IOS1G	50
✓	69	B160	IOS1G	80	✓	99	P060	IOS1G	50
✓	70	BP10	IOS1G	80	✓	100	P070	IOS1G	50
✓	71	<del>B150</del>	IOS1G	80	✓	101	<del>PP00</del>	IOS1G	50
✓	72	B140	IOS1G	80	✓	102	P080	IOS1G	50
✓	73	VDD	PWRPY		✓	103	P090	IOS1G	50
✓	74	B130	IOS1G	80	✓	104	P100	IOS1G	50
✓	75	B120	IOS1G	80	✓	105	P110	IOS1G	50
✓	76	B110	IOS1G	80	✓	106	P120	IOS1G	50
✓	77	B100	IOS1G	80	✓	107	P130	IOS1G	50
✓	78	B090	IOS1G	80	✓	108	GND	GNDPY	
✓	79	B080	IOS1G	80	✓	109	P140	IOS1G	50
✓	80	<del>BP00</del>	IOS1G	80	✓	110	P150	IOS1G	50
✓	81	<del>B070</del>	IOS1G	80	✓	111	<del>PP10</del>	IOS1G	50
✓	82	B060	IOS1G	80	✓	112	P160	IOS1G	50
✓	83	B050	IOS1G	80	✓	113	P170	IOS1G	50
✓	84	GND	GNDPY		✓	114	P180	IOS1G	50
✓	85	B040	IOS1G	80	✓	115	P190	IOS1G	50
✓	86	B030	IOS1G	80	✓	116	P200	IOS1G	50
✓	87	B020	IOS1G	80	✓	117	P210	IOS1G	50
✓	88	B010	IOS1G	80	✓	118	P220	IOS1G	50
✓	89	B000	IOS1G	80	✓	119	VDD	PWRPY	
✓	90	GND	GNDCO		✓	120	P230	IOS1G	50

LOAD				LOAD			
PIN	SIGNAL	BUFFER	pF	PIN	SIGNAL	BUFFER	pF
✓ 121	PP20	IOS1G	50	✓ 151	VDD	PWRCO	
✓ 122	P240	IOS1G	50	✓ 152	PP50	IOS1G	50
✓ 123	P250	IOS1G	50	✓ 153	P480	IOS1G	50
✓ 124	P260	IOS1G	50	✓ 154	GND	GNDPY	
✓ 125	P270	IOS1G	50	✓ 155	P490	IOS1G	50
✓ 126	P280	IOS1G	50	✓ 156	P500	IOS1G	50
✓ 127	P290	IOS1G	50	✓ 157	P510	IOS1G	50
✓ 128	P300	IOS1G	50	✓ 158	P520	IOS1G	50
✓ 129	P310	IOS1G	50	✓ 159	P530	IOS1G	50
✓ 130	GND	GNDPY		✓ 160	P540	IOS1G	50
✓ 131	PP30	IOS1G	50	✓ 161	P550	IOS1G	50
✓ 132	P320	IOS1G	50	✓ 162	PP60	IOS1G	50
✓ 133	P330	IOS1G	50	✓ 163	P560	IOS1G	50
✓ 134	P340	IOS1G	50	✓ 164	P570	IOS1G	50
✓ 135	P350	IOS1G	50	✓ 165	VDD	PWRPY	
✓ 136	P360	IOS1G	50	✓ 166	P580	IOS1G	50
✓ 137	P370	IOS1G	50	✓ 167	P590	IOS1G	50
✓ 138	P380	IOS1G	50	✓ 168	P600	IOS1G	50
✓ 139	P390	IOS1G	50	✓ 169	P610	IOS1G	50
✓ 140	PP40	IOS1G	50	✓ 170	P620	IOS1G	50
✓ 141	VDD	PWRPY		✓ 171	P630	IOS1G	50
✓ 142	P400	IOS1G	50	✓ 172	PP70	IOS1G	50
✓ 143	P410	IOS1G	50	✓ 173	PC00	IOS1G	50
✓ 144	P420	IOS1G	50	✓ 174	PC10	IOS1G	50
✓ 145	P430	IOS1G	50	✓ 175	PC20	IOS1G	50
✓ 146	P440	IOS1G	50	✓ 176	GND	GNDPY	
✓ 147	P450	IOS1G	50	✓ 177	PC30	IOS1G	50
✓ 148	P460	IOS1G	50	✓ 178	PC40	IOS1G	50
✓ 149	P470	IOS1G	50	✓ 179	PC50	IOS1G	50
✓ 150	GND	GNDCO		✓ 180	PC60	IOS1G	50

LOAD				LOAD			
PIN	SIGNAL	BUFFER	pF	PIN	SIGNAL	BUFFER	pF
✓ 181	PC70	IOS1G	50	✓ 211	VDD	PWRCO	
✓ 182	PC80	IOS1G	50	✓ 212	POS3	IPS8G	
✓ 183	PCPO	IOS1G	50	✓ 213	POS2	IPS8G	
✓ 184	VALO	OPS1T	25	✓ 214	POS1	IPS8G	
✓ 185	EXRQ	OPS1T	25	✓ 215	POS0	IPS8G	
✓ 186	RRDY	OPS1T	25	✓ 216	LCAL	IPS8G	
✓ 187	VDD	PWRPY		✓ 217	RBCK	IPS8G	
✓ 188	WRDY	OPS1T	25	✓ 218	TBCK	IPS8G	
✓ 189	IACK	OPS1T	25	✓ 219	GND	CKBUF25	
✓ 190	IERR	OPS1T	25	✓ 220	VDD	CKBUF25	
✓ 191	SACK	OPS1T	25	✓ 221	SHIT	IPS8G	
✓ 192	ITRO	OPS0T	25	✓ 222	RSET	IPS8G	
✓ 193	ITR1	OPS0T	25	✓ 223	TAKI	IPS8G	
✓ 194	LMPO	OPS0T	25	✓ 224	ITVI	IPS8G	
✓ 195	LMP1	OPS0T	25	✓ 225	SHRI	IPS8G	
✓ 196	GND	GNDPY		✓ 226	BSYI	IPS8G	
✓ 197	VALI	IPS8I		✓ 227	BAGR	IPS8G	
✓ 198	RELS	IPS8I		✓ 228	BARQ	OPS1T	25
✓ 199	INRQ	IPS8I		✓ 229	BOOT	OPS1T	25
✓ 200	SREQ	IPS8G		✓ 230	BPER	OPS1T	25
✓ 201	TREF	IPS8G		✓ 231	ITVO	OPS1T	25
✓ 202	PCEN	IPS8G		✓ 232	GND	GNDPY	
✓ 203	RCLK	IPS8G		✓ 233	SHRO	OPS1T	25
✓ 204	TCLK	IPS8G		✓ 234	BSYO	OPS1T	25
✓ 205	GND	CKBUF25		✓ 235	DVAI	IPS8G	
✓ 206	VDD	CKBUF25		✓ 236	DVAO	OPS1V	80
✓ 207	IOMD	IPS8G		✓ 237	AVAI	IPS8G	
✓ 208	SPS1	IPS8G		✓ 238	AVAO	OPS1V	80
✓ 209	SPS0	IPS8G		✓ 239	BCPO	IOS1G	80
✓ 210	GND	GNDCO		✓ 240	BC70	IOS1G	80

**2 GND and VDD CALCULATIONS**

Input buffer pads:	IPS8G:	24
	IPS8T:	3
Output buffer pads:	OPS0T:	4
	OPS1T:	13
	OPS1V:	2
Bidirectional buffer pads:	IOS1G:	163
Core power pads:	PWRCO:	4
	GNDCO:	4
I/O power pads:	PWRPY:	9
	GNDPY:	10
Clock buffer pads (CKBUF25):	VDD:	2
	GND:	2
-----		
Total no. of pads		240

**Core Power:**

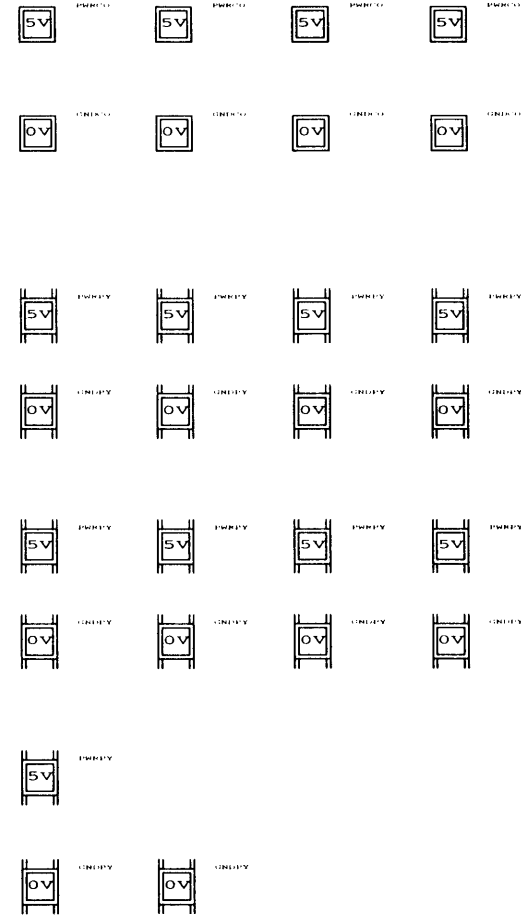
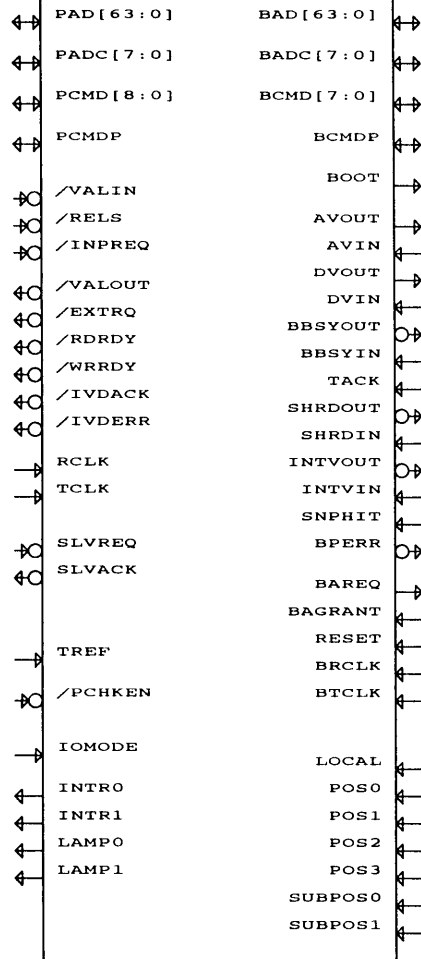
Required no. of PWRCO/GNDCO pad pairs:  $240/64 = 3.75$

**I/O Power:**

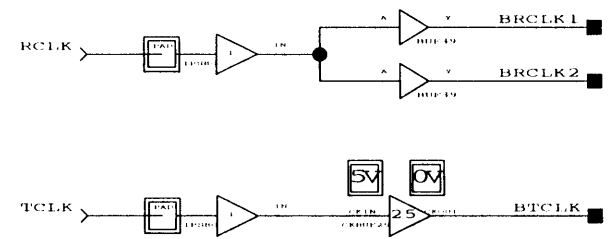
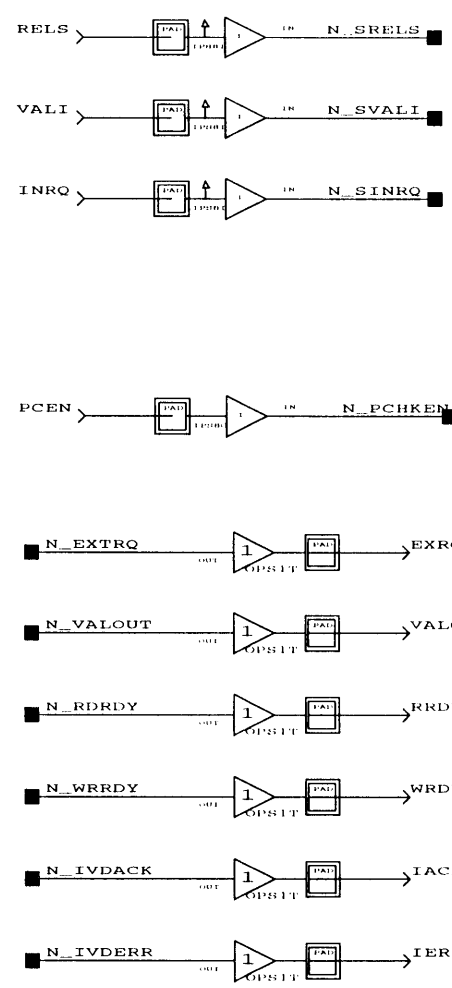
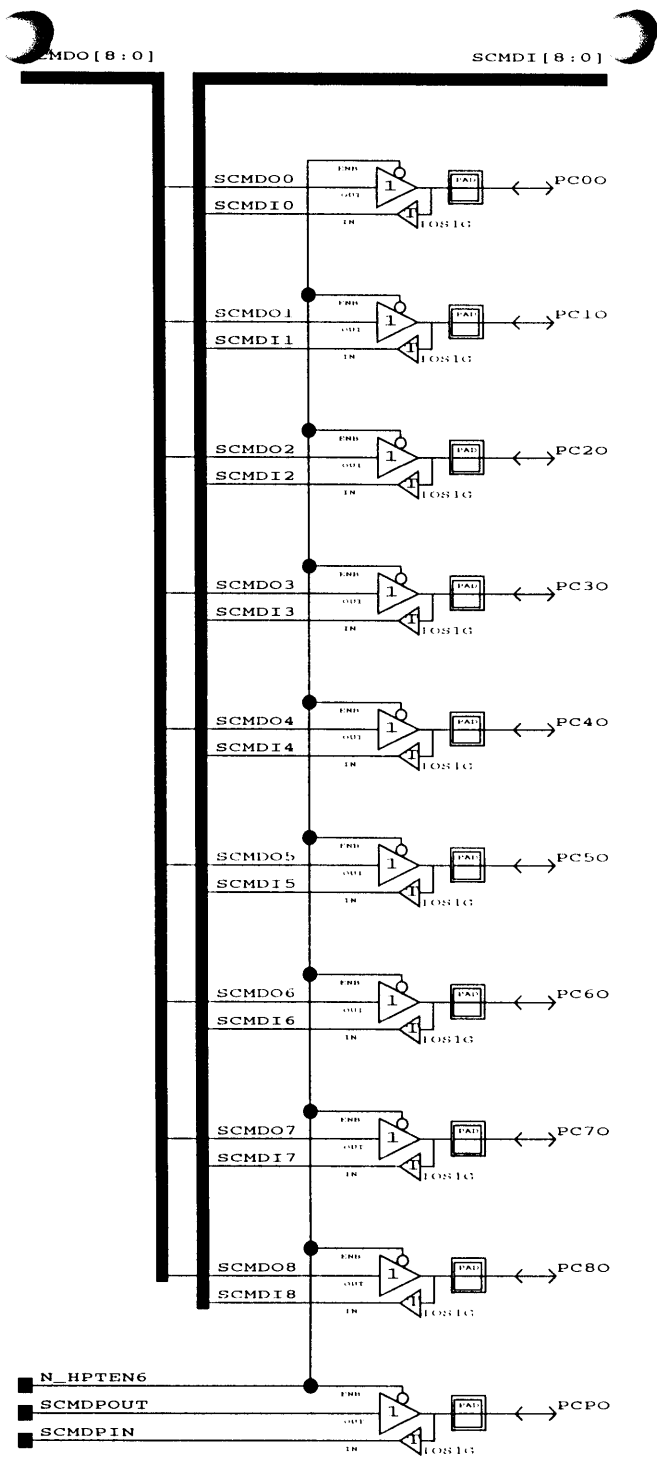
I/O current:	OPS0T:	4 x 2.75 =	11.0 mA
	OPS1T:	13 x 5.5 =	71.5 -
	OPS1V:	2 x 5.5 =	11.0 -
	IOS1G:	163 x 5.5 =	896.5 -
-----			
Total I/O current			990.0 mA

Required no. of PWRPY/GNDPY pairs:  $990/110 = 9$

CA302

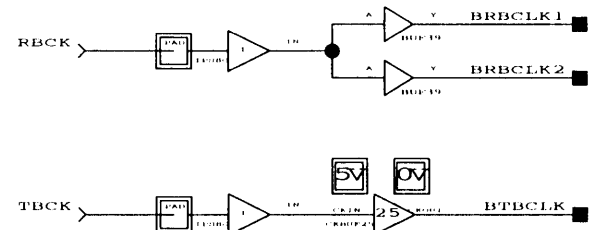
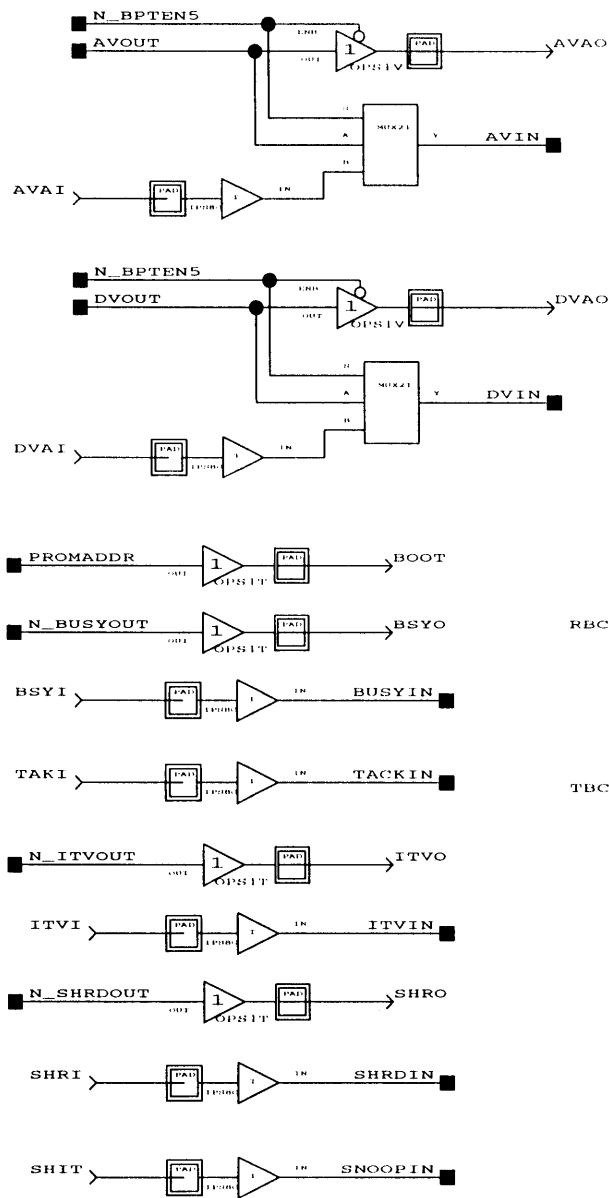
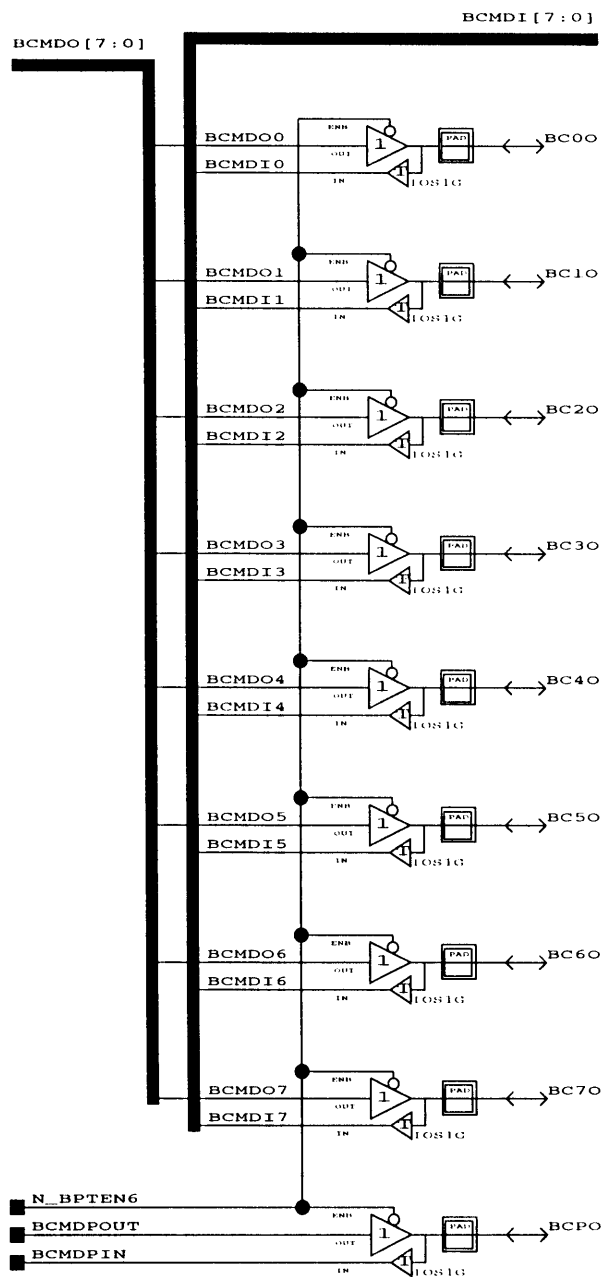


		Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302 Power Pads	
Issue 1	94-08-02		
Issue 2			
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<b>dde</b>		Dansk Data Elektronik A/S	
Issue 0	93-04-23	CPU AGENT - CA302	
Issue 1	94-08-02	Host Port I/O Buffers	
Issue 2			
Issue 3		File: cpa.2	Page: 2 of 42





dde		Dansk Data Elektronik A/S	
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Issue 1	94-08-02	Bus Port I/O Buffers	
Issue 2			
Issue 3		File: epa.6	Page: 6 of 42

Til Aage, Knud Arne og Lars Bo.

cc: Henrik Bøje

Henrik Bøje har overbevist mig om, at problemet med link index registre i de to agenter kun er tilsyneladende, hvilket beskrives nedenfor. Endvidere har jeg et forslag til, hvorledes problemet med forkert paritet, når R4400 melder hus forbi, kan løses.

Som udgangspunkt skal (sekundær) cachens tags være en delmængde af den globale og lokale snoopers tags under et. Ved indlæsning af en blok skal en indgang i den ene snooper opdateres, mens den tilsvarende indgang i den anden snooper enten kan invalideres eller lades urørt. Invalidering har den store ulempe, at der også kræves tilgang til den anden agent og snooper (og bustilgang!), men til gengæld undgås falske hit i snooperne. Det er i virkeligheden denne metode, der giver det frygtede problem vedrørende opdatering af begge link index registre.

Når der sker en link retained operation erstatter en ny cache linie, en, hvori der allerede findes et link. I den anden metode, der er den der bruges i SPC/3, vil der da ske følgende: Hvis begge cache linier vedrører den samme snooper, vil linkets tag blive overskrevet i snooperen, og man må nøjes med det fælles index, der gemmes i agentens link index register. Hvis de vedrører forskellige snooper vil en opdatering af den ene snooper med den ny cache liniens tag betyde, at den anden snooper fortsat indeholder den gamle cache liniens tag. Idet det ikke er muligt at afgøre hvilket af de to tilfælde, der er tale om, skal man altid gemme indexet som omtalt. Der er interessant at bemærke, at snooperne tag således ikke altid er tro kopier af tagene i cachem.

Vedrørende paritetsproblemet vil jeg foreslå, at det sidste ledige signal i processor modulets stik, hvis der ikke er andre planer, bruges til at lade det enkelte processor modul afgøre, hvorvidt paritet skal checkes på udadgående data, således at det aldrig sker med den nuværende R4400 revision, men kan ske i en evt. fremtidig korrekt version. Forbindelserne mellem processor og agenter bliver under alle omstændigheder checket ved indgående data.

Hilsen, Ole.