Dansk Data Elektronik A/S

Technical Data Sheet

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SECTION 1.0

Supermax Technical Data Sheet

SUPERMAX technical data sheet.
Module: CIOC 0900

Type: CIOC 0900

Data sheet no.: 7

Revision no.: 0

Date: 851008

General description:

The CIOC is the intelligent Communication IO Controller in a SUPERMAX system. The CIOC is built around a microprocessor and and contains the following interfaces:

- 2 seriel interface channels with RS-232 or RS-422 interface.
- Asynchronous or byte-synchronous transmission.
- HDLC or SDLC transmission.

Interface to I/O bus:

The CIOC has a standard interface to the common SUPERMAX I/O bus. The local memory bus is not used.

Active cycles : Byte read and write.
Dobbelt word read and write.

Passive cycles: Byte read and write.
Word read and write.
Read modify write.

Interface to peripheral equipment:

Seriel Channels:

The selection of interface standard and type is programmable.

All interface signals are situated in a 50 pin flatcable header.

PIN	SIGNAL	SIGNAL	PIN
01	T(B)0	T(B)1	02
03	T(A)0	T(A)1	04
05	C(B)0	C(B)1	06
07	C(A)0	C(A)1	08
09	S(B)0	S(B)1	10
11	S(A)0	S(A)1	12
13	I(B)0	I(B)1	14
15	I(A)0	I(A)1	16
17	R(B)0	R(B)1	18
19	R(A)0	R(A)1	20
21	GND	GND	22
23	GND	GND	24
25	GND	GND	26
27	GND	GND	28
29	+12V	+12V	30
31	-12V	-12V	32
33	DTR0	DTR1	34
35	RTS0	RTS1	36
37	RXC0	RXC1	38
39	TXC0	TXC1	40
41	TXD0	TXD1	42
43	RXD0	RXD1	44
45	CTS0	CTS1	46
47	DSR0	DSR1	48
49	CD0	CD1	50

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

Power requirements:

Voltage	Typ. current
+ 5 +-5%	6.5 A
+12 +-5%	0.1 A
-12 +-5%	0.1 A

Physical dimension:

Standard SUPERMAX module.

Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a CIOC module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Straps.
- Pull down resistors for the service port.
- Flat cables for the serial channels.
- Firmware.

These items are described in details in the following text.

Unit number/Priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. The address is called the unit number. The unit number of the CIOC module is coded in a PAL located in position I1. This PAL is called the unit PAL.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot used the same priority. The CIOC module uses two priorities. The priorities of the CIOC module are coded in two PALs located in position N1 and N3. This PALs are called the priority PALs.

Pull down resistors for the service port:

Output signals from the service port are open collector signals. These signals must be pulled down to -12v by one and only one module in a Supermax system. Pull down resistors are placed in position Q3.

Firmware:

The firmware is situated in an EPROM mounted in position E4.

CIOCBOOT, V. 0100, 840618.

The CIOC with the this firmware will be able to be bootstraped of another module in a Supermax system.

Straps and jumpers:

+ designates factory installed position.

Strap 1.

Function: Real time clock.

Position: A 7,11

Name: SK3 and SK4

```
* * * * *
* * * * *
1 2 3 4 5
```

Jumper	Clock
1	1.28 milliseconds
2	6.4 milliseconds
+ 3	12.8 milliseconds
4	64.0 milliseconds
5	128.0 milliseconds

Strap 2.

Function: Baud rate to service port. Connected to both Txclk and Rxclk.

Position: A 9,10

Name: SK1 and SK2

```
* * * *
* * * *
1 2 3 4
```

Jumper	Clock
+ 1	9600 x 16 baud.
2	4800 x 16 baud.
3	2400 x 16 baud.
4	1200 x 16 baud.

Strap 3.

Function: Special option for hardware service.

Position: B 5,1

Name: SM1

Under normal circumstances, the jumper must be in position two.

Strap 4.

Function: Transmitter/receiver clocks to the HDLC controller.
Data-communication port 0.

Position: B 6,8

Name: SV1 and SV2

```
* * * * * *
* * * * * *
1 2 3 4 5 6
```

Jumper

1	HDLC-C pin 32xClk grounded.
2	HDLC-C pin 32xClk connected to counter output OUT02
3	HDLC-C pin DPLL connected to RxC input pin on HDLC-C
4	HDLC-C pin DPLL connected to TxC input pin on HDLC-C
+ 5	HDLC-C pin RxC connected to line interface signal.
+ 6	HDLC-C pin TxC connected to line interface signal.

Jumper 3 and 5 may not both be mounted.
Jumper 4 and 6 may not both be mounted.

Strap 5.

Function: Transmitter/receiver clocks to the HDLC controller.
Data-communication port 1.

Position: B 9,9

Name: SW1 and SW2

```
* * * * * *
* * * * * *
1 2 3 4 5 6
```

Jumper

1	HDLC-C pin 32xClk grounded.
2	HDLC-C pin 32xClk connected to counter output OUT12
3	HDLC-C pin DPLL connected to RxC input pin on HDLC-C
4	HDLC-C pin DPLL connected to TxC input pin on HDLC-C
+ 5	HDLC-C pin RxC connected to line interface signal.
+ 6	HDLC-C pin TxC connected to line interface signal.

Jumper 3 and 5 may not both be mounted.
Jumper 4 and 6 may not both be mounted.

Strap 6.

Function: Transmitter-clock to data communication port 0.

Position: C 3,7

Name: STX0

```
* * *
1 2 3
```

Jumper

+ 1-2	The TxC signal is an input to the CIOC.
2-3	The CIOC drives the TxC signal.

Strap 7.

Function: Receiver-clock to data communication port 0.

Position: C 3,7

Name: SRX0

```
* * *
1 2 3
```

Jumper

+ 1-2 The RxC signal is an input to the CIOC.
  2-3 The CIOC drives the RxC signal.

Strap 8.

Function: Transmitter-clock to data communication port 1.

Position: C 3,7

Name: STX1

```
* * *
1 2 3
```

Jumper

+ 1-2 The TxC signal is an input to the CIOC.
  2-3 The CIOC drives the TxC signal.

Strap 9.

Function: Receiver-clock to data communication port 1.

Position: C 3,7

Name: SRX1

```
* * *
1 2 3
```

Jumper

+ 1-2 The RxC signal is an input to the CIOC.
  2-3 The CIOC drives the RxC signal.

Strap socket 1.

Function: Possible to connect two switches: One is able to generate an internal reset pulse and the other is able to generate a hardware interrupt. (TRAP)

Position: C 3,1

Name: S11

Under normal circumstances the strap socket is mounted as follows:

```
     * *_* * * * * *

  1. * *_* * * * * *
```

An internal reset pulse is generated if the connection between pin 2 and 3 is removed, and pins 1 and 2 are connected together.

A non-maskable interrupt TRAP is generated if the connection between pin 14 and 15 is removed, and pins 15 and 16 are connected together.

Strap socket 2.

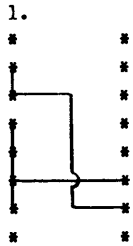
Function: Interrupts from data-communication port 0.

Position: B 3,7

Name: A13

```
                1.
                *        *  RST7
Rxrdy X0        *        *  RST6
Txrdy X0        *        *  RST5
Rxrdy D0        *        *  RST4
Txrdy D0        *        *  RST3
Rxi 0           *        *  RST2
Txi 0           *        *  RST1
                *        *  RST0
```

Factory installed strap:



Strap socket 3.

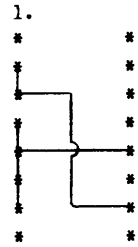
Function: Interrupts from data-communication port 1.

Position: B 6,6

Name: A14

	1.		
	*	*	RST7
Rxrdy X1	*	*	RST6
Txrdy X1	*	*	RST5
Rxrdy D1	*	*	RST4
Txrdy D1	*	*	RST3
Rxi 1	*	*	RST2
Txi 1	*	*	RST1
	*	*	RST0

Factory installed strap:



Cables and connectors:

The connection between the CIOC module and the CIOC backplane is made with one flat cable.

The header is mounted in position: C 4,8. 50 pin.
Service port : C 5,3. 20 pin

The flat cable is connected to the CIOC back panel. The CIOC back panel is mounted on the rear of the SUPERMAX card cabinet.

Indicator Leds:

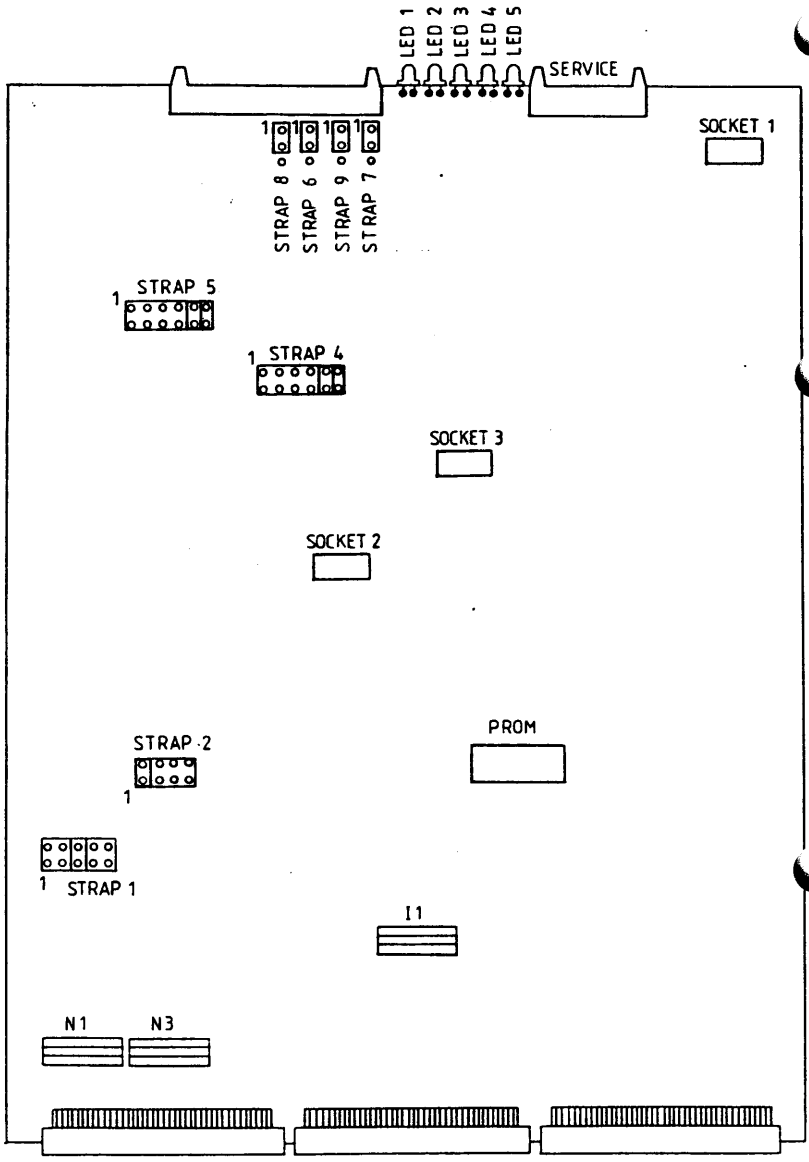
LED1: On: The boot prom is enabled.
Off: The boot prom is disabled.
Upon power up: On

LED2: On: A time out is pending.
Off: No time out.
Upon power up: Off.

LED3: On: A buserror is received.
Off: No buserror.
Upon power up: Off.

LED4: On: The ERROR line is active. The error line is set by the program or because of a parity error.
Off: No error.
Upon power up: On

LED5: On: The CIOC has activated the buserror signal.
Off: No error.
Upon power up: Off.


LED 1
LED 2
LED 3
LED 4
LED 5
SERVICE
SOCKET 1
STRAP 8
STRAP 6
STRAP 9
STRAP 7
STRAP 5
STRAP 4
SOCKET 3
SOCKET 2
PROM
STRAP 2
STRAP 1
I1
N1
N3

SUPERMAX technical data sheet.
Module: CPU 0100

Type: CPU 0100

Data sheet no.: 3

Revision no.: 0

Date: 851015

General description:

The CPU 0100 is the CPU module in a SUPERMAX system. The CPU module contains a 10 Mhz 68000 and the following interfaces:

- Interface to I/O bus.
- Interface to memory modules.
- Front pannel display.
- Service port.

Interface to I/O bus:

The CPU has a standard interface to the common SUPERMAX I/O bus.

Active cycles : Byte read and write.
Word read and write.
Read modify write.

Passive cycles: Byte read and write.
Word read and write.
Double word read and write.
Read modify write.

Interface to memory modules:

The CPU module controls memory modules type 0200 and type 1400.

Memory modules are connected to the CPU module via the local memory bus. The CPU module controls the memory modules and takes care of error detection and correction. The CPU module executes the following cycles in memory modules:

Refresh cycle
Word read cycle
Word write cycle
double word read cycle
double word write cycle

The local memory bus is multiplexed between address and data. In the first part of a memory cycle the bus transfers address from the CPU module to the memory modules, and in the second part the bus transfers data between CPU module and memory modules.

Interface to front pannel display:

The front panel display consists of two seven segment displays, a red LED, and a green LED. The seven segment displays are under program control and used by the operating system to display various error information. The red LED is on, when the CPU performs a cycle in supervisor mode. The green LED is on, when the CPU performs a cycle in user mode. If both LED´s are off the CPU has entered the HALT state. The CPU module is connected to the front panel display via a 20 pin flat cable.

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

Power requirements:

Voltage		Typ. current
+ 5	+-5%	9.5 A
+12	+-5%	200 mA
-12	+-5%	200 mA

Physical dimension:

Standard SUPERMAX module.

Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a CPU module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Pull up resistors.
- Bus clock.
- Pull down resistors.
- Straps.

These items are described in details in the following text.

Unit number/Priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. The address is called the unit number. The unit number of the CPU module is coded in a PAL located in position B8. This PAL is called the unit PAL.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot used the same priority. The CPU module uses one priority. The priority of the CPU module is coded in a PAL located in position B9. This PAL is called the priority PAL.

Current lables on Unit and Priority PALs:

Unit number	Unit PAL	Priority PAL	Priority
0	U000	P000	00
1	U010	P010	01
2	U020	P020	02
3	U030	P030	03
4	U040	P040	04
5	U050	P100	10
6	U060	P110	11
7	U070	P120	12

Older lables on Unit and Priority PALs

Unit number	Unit PAL	Priority PAL	Priority
0	C170	C160	00
1	C171	C161	01
2	C172	C162	02
3	C173	C163	03
4	C174	C164	14
5	C175	C165	10
6	C176	C166	11
7	C177	C167	12

Unit PALs marked C17x is identical to unit PALs marked U0x0 Priority PALs marked C16x belong to an older family of priority PALs. This old family must not be mixed with priority PALs marked Pxy0

Pull up resistors:

One and only one CPU module in a Supermax system must contain pull up resistors for various signals in the I/O bus. These resistors are:

SI25: 150 ohms. 10 pins single in line.
SI26: 150 ohms. 10 pins single in line.
SI27: 1000 ohms. 10 pins single in line.

Bus clock:

The arbitrating scheme in the I/O bus uses a clock. One and only one CPU module in a Supermax system must drive the bus clock.

The BUS CLOCK is strapped in the clock strap. See below.

Pull down resistors for the service port:

Output signals from the service port are open collector signals. These signals must be pulled down to -12v by one and only one module in a Supermax system. Pull down resistors are placed in position Z9.

Straps and jumpers:

+ designates factory installed position.

Clock strap:

Clock strap position Z6:

6 Mhz 0	0	CPU CLOCK (PIN 16)
8 Mhz 0	0	CPU CLOCK
10 Mhz 0	0	CPU CLOCK
10 Mhz 0	0	BUS CLOCK
12 Mhz 0	0	BUS CLOCK
16 Mhz 0	0	BUS CLOCK
16 Mhz 0	0	INTERNAL CLOCK
20 Mhz 0	0	INTERNAL CLOCK

Clock rates selected from factory:

CPU CLOCK:	10 MHz
INTERNAL CLOCK:	16 Mhz
BUS CLOCK:	8 Mhz

Factory installed clock strap:

6 Mhz 0	0	CPU CLOCK (PIN 16)
8 Mhz 0	0	CPU CLOCK
10 Mhz 0	0	CPU CLOCK
10 Mhz 0	0	BUS CLOCK
12 Mhz 0	0	BUS CLOCK
16 Mhz 0	0	BUS CLOCK
16 Mhz 0	0	INTERNAL CLOCK
20 Mhz 0	0	INTERNAL CLOCK

TIMER STRAP.

Position Z4

Function: Selects baud rate for the service port.
Selects time between timer interrupts.

Baud rate input	0	0 5 ms output(PIN 16)
9600 baud output	0	0 interrupt input
4800 baud output	0	0 10 ms output
2400 baud output	0	0 20 ms output
1200 baud output	0	0 interrupt input
600 baud output	0	0 40 ms output
300 baud output	0	0 80 ms output
	0	0 interrupt input

Factory strapping:

Baud rate: 9600 baud
Timer interrupt: 40 ms

Baud rate input	0	0 5 ms output(PIN 16)
9600 baud output	0	0 interrupt input
4800 baud output	0	0 10 ms output
2400 baud output	0	0 20 ms output
1200 baud output	0	0 interrupt input
600 baud output	0	0 40 ms output
300 baud output	0	0 80 ms output
	0	0 interrupt input

Interrupt strap:

Position Z5

Function: Connects interrupt sources to interrupt levels.

Power failure	0	0 not used(PIN 16)
Error in unit	0	0 interrupt level 6
Protection violation	0	0 interrupt level 5
Memory fault	0	0 interrupt level 4
Timer interrupt	0	0 interrupt level 3
Service port	0	0 interrupt level 2
XINT0	0	0 interrupt level 1
XINT1	0	0 not used

Factory installed interrupt strap:

Timer interrupt connected to level 6
Service port connected to level 1

Power failure	0	0 not used(PIN 16)
Error in unit	0	0 interrupt level 6
Protection violation	0	0 interrupt level 5
Memory fault	0	0 interrupt level 4
Timer interrupt	0	0 interrupt level 3
Service port	0	0 interrupt level 2
XINT0	0	0 interrupt level 1
XINT1	0	0 not used

SUPERMAX technical data sheet.
Module: CPU 0101

Type: CPU 0101

Data sheet no.: 2

Revision no.: 0

Date: 850827

General description:

The CPU 0101 is the CPU module in a SUPERMAX system. The CPU module contains a 12 Mhz 68000 and the following interfaces:

- Interface to I/O bus.
- Interface to memory modules.
- Front pannel display.
- Service port.

The CPU 0101 is an enhanced version of CPU 0100. The two modules are program compatible. CPU 0101 has a 2 Kb cache memory and an optional floating point unit.

Interface to I/O bus:

The CPU has a standard interface to the common SUPERMAX I/O bus.

Active cycles : Byte read and write.
Word read and write.
Read modify write.

Passive cycles: Byte read and write.
Word read and write.
Double word read and write.
Read modify write.

Interface to memory modules:

The CPU module controls memory modules type 0200 and type 1400.

Memory modules are connected to the CPU module via the local memory bus. The CPU module controls the memory modules and takes care of error detection and correction. The CPU module executes the following cycles in memory modules:

Refresh cycle
Word read cycle
Word write cycle
double word read cycle
double word write cycle

The local memory bus is multiplexed between address and data. In the first part of a memory cycle the bus transfers address from the CPU module to the memory modules, and in the second part the bus transfers data between CPU module and memory modules.

Interface to front pannel display:

The front panel display consists of two seven segment displays, a red LED, and a green LED. The seven segment displays are under program control and used by the operating system to display various error information. The red LED is on, when the CPU performs a cycle in supervisor mode. The green LED is on, when the CPU performs a cycle in user mode. If both LED's are off the CPU has entered the HALT state. The CPU module is connected to the front panel display via a 20 pin flat cable.

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

Power requirements:

Voltage		Typ. current
+ 5	+-5%	10.5 A
+12	+-5%	200 mA
-12	+-5%	200 mA

Physical dimension:

Standard SUPERMAX module.

Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a CPU module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Pull up resistors.
- Bus clock.
- Pull down resistors.
- Straps.

These items are described in details in the following text.

Unit number/Priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. The address is called the unit number.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot used the same priority. The CPU module uses one priority. The CPU module is equiped with a unit number switch. The switch gives the module a unit number and one priority.

Switch position	Unit number	Priority
0	0x00	00
1	0x01	01
2	0x02	02
3	0x03	03
4	0x04	04
5	0x05	10
6	0x06	11
7	0x07	12
8	0x08	13
9	0x09	14
A	0x0a	20
B	0x0b	21
C	0x0c	22
D	0x0d	23
E	0x0e	24
F	0x0f	30

Pull up resistors:

One and only one CPU module in a Supermax system must contain pull up resistors for various signals in the I/O bus. These resistors are:

SI25: 150 ohms. 10 pins single in line.
SI26: 150 ohms. 10 pins single in line.
SI27: 1000 ohms. 10 pins single in line.

Bus clock:

The arbitrating scheme in the I/O bus uses a clock. One and only one CPU module in a Supermax system must drive the bus clock.

If jumper ST1 is installed the CPU module drives the bus clock.

If jumper ST1 is removed the CPU module does not drive the bus clock.

Jumper ST1 is installed from the factory.

Pull down resistors for the service port:

Output signals from the service port are open collector signals. These signals must be pulled down to -12v by one and only one module in a Supermax system. Pull down resistors are placed in position Z9.

Straps and jumpers:

+ designates factory installed position.

Strap 2: ST2

Function: Number of wait states in cache.
ST2 is located between ZD and ZC.

```
ST2:    *  *  *
        1  2  3
```

+ Jumper between pin 1 and pin 2: zero wait state in cache.
  Jumper between pin 2 and pin 3: one wati state in cache.

STRAP 3: ST3

Function: Controls enable/disable of cache.
ST3 is loacated between N8 and C6.

```
ST3:    *  *  *
        1  2  3
```

  Jumper between pin 1 and pin 2: Cache enabled by bit 11 in command register

+ Jumper between pin 2 and pin 3: Cache enabled by bit 6 in command register: boot PROM disable.

Clock strap:

Clock strap position Z6:

```
10 Mhz 0      0  CPU CLOCK (PIN 16)
12 Mhz 0      0  CPU CLOCK
16 Mhz 0      0  20 Mhz
16 Mhz 0      0  INTERNAL CLOCK
 8 Mhz 0      0  BUS CLOCK
 6 Mhz 0      0  10 Mhz
 8 Mhz 0      0
10 Mhz 0      0
```

Clock rates selected from factory:

CPU CLOCK:	12 MHz
INTERNAL CLOCK:	20 Mhz
BUS CLOCK:	8 Mhz

Factory installed clock strap:

```
10 Mhz 0      0  CPU CLOCK (PIN 16)
12 Mhz 0------0  CPU CLOCK
16 Mhz 0     ┌0  20 Mhz
16 Mhz 0     └0  INTERNAL CLOCK
 8 Mhz 0------0  BUS CLOCK
 6 Mhz 0      0  10 Mhz
 8 Mhz 0      0
10 Mhz 0      0
```

TIMER STRAP.

Position Z4

Function: Selects baud rate for the service port.
Selects time between timer interrupts.

Baud rate input	0	0	5 ms output(PIN 16)
9600 baud output	0	0	interrupt input
4800 baud output	0	0	10 ms output
2400 baud output	0	0	20 ms output
1200 baud output	0	0	interrupt input
600 baud output	0	0	40 ms output
300 baud output	0	0	80 ms output
	0	0	interrupt input

Factory strapping:

Baud rate: 9600 baud
Timer interrupt: 40 ms

Baud rate input	0	0	5 ms output(PIN 16)
9600 baud output	0	0	interrupt input
4800 baud output	0	0	10 ms output
2400 baud output	0	0	20 ms output
1200 baud output	0	0	interrupt input
600 baud output	0	0	40 ms output
300 baud output	0	0	80 ms output
	0	0	interrupt input

Interrupt strap:

Position Z5

Function: Connects interrupt sources to interrupt levels.

Power failure	0	0 not used(PIN 16)
Error in unit	0	0 interrupt level 6
Protection violation	0	0 interrupt level 5
Memory fault	0	0 interrupt level 4
Timer interrupt	0	0 interrupt level 3
Service port	0	0 interrupt level 2
XINT0	0	0 interrupt level 1
XINT1	0	0 not used

Factory installed interrupt strap:

Timer interrupt connected to level 6
Service port connected to level 1

Power failure	0	0 not used(PIN 16)
Error in unit	0	0 interrupt level 6
Protection violation	0	0 interrupt level 5
Memory fault	0	0 interrupt level 4
Timer interrupt	0	0 interrupt level 3
Service port	0	0 interrupt level 2
XINT0	0	0 interrupt level 1
XINT1	0	0 not used

Basic CPU module:

Supermax systems are delivered with one basic CPU module 0101.

The basic CPU module differs from the standard CPU modules described above on the following points:

Unit number cannot be changed. It is fixed to unit number three.

Priority cannot be changed. It is fixed to priority 03.

Pull up resistors SI25, SI26, and SI27 are installed.

The basic module drives the bus clock.

Pull down resistors to the service port are installed.

Type: CPU 3400

Data sheet no.: 12

Revision no.: 1

Date: 870623

General description:

The CPU 3400 is a CPU module in a Supermax system. The CPU module contains a 68020 CPU, a 68881 FPU, and the following interfaces:

- Interface to I/O bus.
- Interface to memory modules.
- Front pannel display.
- Service port.

The CPU 3400 is not compatible with CPU 0101. CPU 3400 has a program cache and a data cache. Each cache contains 8 kb.

Interface to I/O bus:

The CPU has a standard interface to the common Supermax I/O bus.

Active cycles : Byte read and write.
Word read and write.
Double word read and write.
Read modify write.

Passive cycles: Byte read and write.
Word read and write.
Double word read and write.
Read modify write.

Interface to memory modules:

The CPU 3400 module is designed to control memory modules type RAM 3100. As an option CPU 3400 can be strapped to control memory modules of type 0200, 1400, and 3000.

Memory modules are connected to the CPU module via the local memory bus. The CPU module controls the memory modules and takes care of error detection and correction. The CPU module executes the following cycles in memory modules:

Refresh cycle
Double word read cycle
Double word write cycle
Burst mode read cycle

The local memory bus is multiplexed between address and data. In the first part of a memory cycle the bus transfers address from the CPU module to the memory modules, and in the second part the bus transfers data between CPU module and memory modules. In a burst mode read cycle one block of data is read from memory and written in cache. A block is one, two , or four double words depending upon the block size in the cache.

Interface to front pannel display:

The front panel display consists of two seven segment displays, a red LED, and a green LED. The seven segment displays are under program control and used by the operating system to display various error information. The red LED is on, when the CPU performs a cycle in supervisor mode. The green LED is on, when the CPU performs a cycle in user mode. If both LED's are off the CPU has entered the HALT state. The CPU module is connected to the front panel display via a 20 pin flat cable.

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

Power requirements:

Voltage		Typ. current
+ 5	+-5%	11.0 A
+12	+-5%	200 mA
-12	+-5%	200 mA

Installation:

Before a CPU module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Pull up resistors.
- Bus clock.
- Pull down resistors.
- Straps.

These items are described in details in the following text.

Unit number/Priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. This address is called the unit number.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot used the same priority. The CPU module uses one priority. The CPU module is equiped with a unit number switch. The switch gives the module a unit number and one priority. Notice that unit number X and unit number X+8 has the same priority.

Switch position	Unit number	Priority
0	0x00	00
1	0x01	01
2	0x02	02
3	0x03	03
4	0x04	04
5	0x05	10
6	0x06	11
7	0x07	12
8	0x08	00
9	0x09	01
A	0x0a	02
B	0x0b	03
C	0x0c	04
D	0x0d	10
E	0x0e	11
F	0x0f	12

Pull up resistors:

One and only one CPU module in a Supermax system must contain pull up resistors for various signals in the I/O bus. All these pull up resistors on CPU 3400 are connected to signals in the IO bus by switches. The pull up resistors and the corresponding switches are:

SI0 : 150 ohms. 10 pins single in line.
Connected by switch Z10.

SI1 : 150 ohms. 10 pins single in line.
Connected by switch Z11.

SI2 : 1000 ohms. 10 pins single in line.
Connected by switch Y17.

Bus clock:

The arbitrating scheme in the I/O bus uses a clock. One and only one CPU module in a Supermax system must drive the bus clock.

The CPU module drives the bus clock when switch Y17 bit 7 is in the ON position.

Pull down resistors for the service port:

Output signals from the service port are open collector signals. These signals must be pulled down to -12v by one and only one module in a Supermax system. Pull down resistors are connected to output signals in the service port when all switches in Q10 are in the ON position.

Block Size in Caches:

Block sizes in cache 0 and cache 1 are set by a number of straps.

Block size in cache 0, program cache, is set by the following straps: ST2, ST3, and ST15.

Cache 0 disabled:

ST2 : don't care
ST3 : don't care
ST15: pin 1 connected to pin 2 and pin 3 connected to pin 4.

Cache 0: Block size: 1 double word.

ST2 : pin 1 connected to pin 2.
ST3 : pin 1 connected to pin 2.
ST15: pin 1 not connected to pin 2 and
pin 3 connected to pin 4.

Cache 0: Block size: 2 double words.

ST2 : pin 1 connected to pin 2.
ST3 : pin 2 connected to pin 3.
ST15: pin 1 connected to pin 2 and
pin 3 not connected to pin 4.

Cache 0: Block size: 4 double words. Factory setting.

ST2 : pin 2 connected to pin 3.
ST3 : pin 2 connected to pin 3.
ST15: pin 1 not connected to pin 2 and
pin 3 not connected to pin 4.

Block size in cache 1, data cache, is set by the following straps: ST4, ST5, ST6, ST7,ST15, ST17, and ST18.

Cache 1 disabled.

ST4 : don't care.
ST5 : don't care.
ST6 : don't care.
ST7 : don't care.
ST15: pin 5 connected to pin 6 and
pin 7 connected to pin 8.
ST17: don't care.
ST18: don't care.

Cache 1: Block size: 1 double word.

ST4 : pin 1 connected to pin 2.
ST5 : pin 1 connected to pin 2.
ST6 : pin 1 connected to pin 2.
ST7 : pin 1 connected to pin 2.
ST15: pin 5 not connected to pin 6 and
pin 7 connected to pin 8.
ST17: pin 1 connected to pin 2.
ST18: pin 1 connected to pin 2.

Cache 1: Block size: 2 double words.

ST4 : pin 1 connected to pin 2.
ST5 : pin 2 connected to pin 3.
ST6 : pin 1 connected to pin 2.
ST7 : pin 2 connected to pin 3.
ST15: pin 5 connected to pin 6 and
pin 7 not connected to pin 1.
ST17: pin 1 connected to pin 2.
ST18: pin 2 connected to pin 3.

Cache 1: Block size: 4 double words. Factory setting.

ST4 : pin 2 connected to pin 3.
ST5 : pin 2 connected to pin 3.
ST6 : pin 2 connected to pin 3.
ST7 : pin 2 connected to pin 3.
ST15: pin 5 not connected to pin 6 and
pin 7 not connected to pin 1.
ST17: pin 2 connected to pin 3.
ST18: pin 2 connected to pin 3.

Straps and jumpers:

+ designates factory installed position.

ST1

Function: Controls the use of the two caches.

```
ST1:    *  *  *
        1  2  3
```

+ Pin 1 connected to pin 2:

Cache 0 is used for program and cache 1 is used for data.

Pin 2 connected to pin 3:

The use of the two caches is controlled by address bit 13. This position is for test purpose and will only work with a non standard population of PALs on the board.

ST2

Function: Controls the block size in cache 0.

```
ST2:    *  *  *
        1  2  3
```

Pin 1 connected to pin 2:

Address bit 3 is used as an address index bit to cache 0.

+ Pin 2 connected to pin 3:

Address bit 12 is used as an address index bit to cache 0.

ST3

Function: Controls the block size in cache 0.

```
ST3:    *  *  *
        1  2  3
```

Pin 1 connected to pin 2:

Address bit 2 is used as an address index bit to cache 0.

+ Pin 2 connected to pin 3:

Address bit 11 is used as an address index bit to cache 0.

ST4

Function: Controls the block size in cache 1.

```
ST4:    *  *  *
        1  2  3
```

pin 1 connected to pin 2:

Address bit 3 is used as an address index bit to cache 1.

+ pin 2 connected to pin 3:

Address bit 12 is used as an address index bit to cache 1.

ST5

Function: Controls the block size in cache 1.

```
ST5:    *  *  *
        1  2  3
```

Pin 1 connected to pin 2:

Address bit 2 is used as an address index bit to cache 1.

+ Pin 2 connected to pin 3:

Address bit 11 is used as an address index bit to cache 1.

ST6

Function: Controls the block size in physical cache comparator. Must be strapped as ST4.

```
ST6:    *  *  *
        1  2  3
```

Pin 1 connected to pin 2:

Address bit 3 is used as an address index bit to the physical cache comparator.

+ Pin 2 connected to pin 3:

Address bit 12 is used as an address index bit to the physical cache comparator.

ST7

Function: Controls the block size in the physical cache comparator. Must be strapped as ST5.

```
ST7:    *  *  *
        1  2  3
```

Pin 1 connected to pin 2:

Address bit 2 is used as an address index bit to the physical cache comparator.

+ Pin 2 connected to pin 3:

Address bit 11 is used as an address index bit to the physical cache comparator.

ST8

Function: Controls the size of the boot PROM.

```
ST8:    *  *  *
        1  2  3
```

Pin 1 connected to pin 2:

Pin 1 on the boot PROM is pulled up.
This position is used, when the boot prom is of type 27256.

+ Pin 2 connected to pin 3:

Pin 1 on the boot prom is connected to address bit 15.
This position is used, when the boot prom is of type 27512.

ST9

Function: Controls the clock frequency to 68020.

```
        2  4  6  8
ST9:    *  *  *  *
        *  *  *  *
        1  3  5  7
```

68020 clock frequency.

```
  Pin 1 connected to pin 2: 25   MHz
+ Pin 3 connected to pin 4: 20   MHz
  Pin 5 connected to pin 6: 16   MHz
  Pin 7 connected to pin 8: 12.5 MHz
```

ST10

Function: Controls the clock frequency to 68881.

```
        2  4  6  8
ST10:   *  *  *  *
        *  *  *  *
        1  3  5  7
```

68881 clock frequency.

```
  Pin 1 connected to pin 2: 25   MHz
  Pin 3 connected to pin 4: 20   MHz
+ Pin 5 connected to pin 6: 16   MHz
  Pin 7 connected to pin 8: 12.5 MHz
```

ST11

Function: Controls the frequency of the bus clock.

```
        2  4  6  8
ST11    *  *  *  *
        *  *  *  *
        1  3  5  7
```

IO bus clock frequency.

```
  Pin 1 connected to pin 2: 12.5 MHz
  Pin 3 connected to pin 4: 10   MHz
+ Pin 5 connected to pin 6:  8   MHz
```

ST12

Function: Controls the baud rate of the service port.

```
        2  4  6  8 10 12 14
```

```
ST12:   *  *  *  *  *  *  *
        *  *  *  *  *  *  *
        1  3  5  7  9 11 13
```

Baud rate.

```
  Pin 1  connected to pin 2 : Not used
+ Pin 3  connected to pin 4 : 9600
  Pin 5  connected to pin 6 : 4800
  Pin 7  connected to pin 8 : 2400
  Pin 9  connected to pin 10: 1200
  Pin 11 connected to pin 12: 600
  Pin 13 connected to pin 14: 300
```

ST13

Function: Controls the clock frequency of the internal logic on the CPU module.

```
        2  4  6
ST13:   *  *  *
        *  *  *
        1  3  5
```

Clock for internal logic

```
  Pin 1 connected to pin 2: CPU clock. Frequency set by ST9.
+ Pin 3 connected to pin 4: 20   MHz
  Pin 5 connected to pin 5: 16   MHz
```

ST15

Function: Controls the block size in cache 0 and cache 1.

```
        2  4  6  8
ST15:   *  *  *  *
        *  *  *  *
        1  3  5  7
```

Jumpers between pin 1 and pin 2 and between pin 3 and pin 4 control the block size in cache 0.

Pin 1 connected to pin 2 and pin 3 connected to pin 4: cache 0 disabled.

Pin 1 not connected to pin 2 and pin 3 connected to pin 4: block size in cache 0: 1 double word.

Pin 1 connected to pin 2 and pin 3 not connected to pin 4: block size in cache 0: 2 double words.

+ Pin 1 not connected to pin 2 and pin 3 not connected to pin 4: block size in cache 0: 4 double words.

Jumpers between pin 5 and pin 6 and between pin 7 and pin 8 control the block size in cache 1.

Pin 5 connected to pin 6 and pin 7 connected to pin 8: cache 1 disabled.

Pin 5 not connected to pin 6 and pin 7 connected to pin 8: block size in cache 1: 1 double word.

Pin 5 connected to pin 6 and pin 7 not connected to pin 8: block size in cache 1: 2 double words.

+ Pin 5 not connected to pin 6 and pin 7 not connected to pin 8: block size in cache 1: 4 double words.

<u>ST16</u>

Function: Controls the internal cache in 68020.

```
ST16:   *  *
        1  2
```

Pin 1 connected to pin 2: The internal cache is disabled.

+ Pin 1 not connected to pin 2: The internal cache is enabled.

ST17

Function: Controls the block size in the physical cache comparator. Must be strapped as ST4.

```
ST17:   *  *  *
        1  2  3
```

Pin 1 connected to pin 2:

Physical address bit 12 is used as a tag bit in the physical cache comparator.

+ Pin 2 connected to pin 3:

Physical address bit 28 is used as a tag bit in the physical cache comparator.

ST18

Function: Controls the block size in the physical cache comparator. Must be strapped as ST5.

```
ST18:   *  *  *
        1  2  3
```

Pin 1 connected to pin 2:

Physical address bit 11 is used as a tag bit in the physical cache comparator.

+ Pin 2 connected to pin 3:

Physical address bit 27 is used as a tag bit in the physical cache comparator.

CPU 3400 and memory modules type 0200, 1400, and 3000.

If CPU 3400 is used together with memory modules type 0200, 1400, or 3000 the following changes must be made on CPU 3400:

Block size in cache 0 must be strapped to one double word.

Block size in cache 1 must be strapped to one double word.

PAL in position F1 must be changed from CP1x to CP16x.

PAL in position F4 must be changed from CP12x to CP17x.

x is the current revision level.

Basic CPU module:

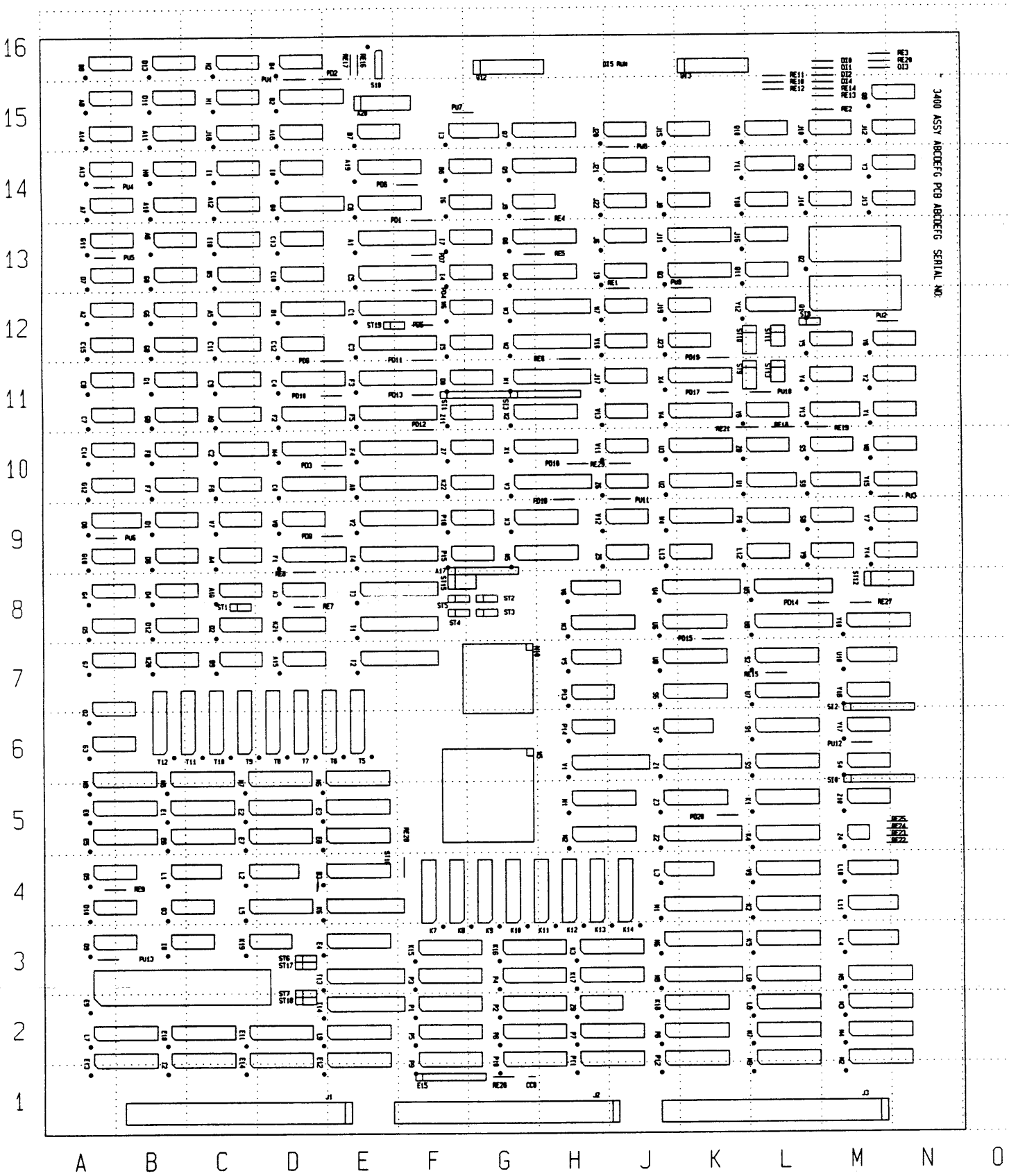
Supermax systems are delivered with one basic CPU module 3400.

The basic CPU module differs from the standard CPU modules described above on the following points:

Unit number cannot be changed. It is fixed to unit number three.

Priority cannot be changed. It is fixed to priority 03.

PRELIMINARY



Component locations				
PCB: 3400 / 68020	Issue:	Date:	dde	dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11

PRELIMINARY

Name	Type	Pos
A0	PAL20L8	E10
A1	PAL20R8	E13
A2	74AS20	A12
A3	74AS20	D8
A4	74AS20	C9
A5	74AS20	C12
A6	74AS74	B13
A7	74AS74	A14
A8	74AS74	A15
A9	74AS27	C11
A10	74S32	B14
A11	74S04	B15
A12	74S00	C14
A13	74S08	A14
A14	74S11	A15
A15	74S08	D7
A16	74S04	C8
A17	SIL	F9
A18	74AS74	D15
A19	PAL16R8	E14
A20	CON	E15
B0	74AS573	D14
B1	74AS573	D12
B2	PAL16R6	D15
B3	74ALS574	D4
B4	74AS74	D16
B5	74AS04	C13
B6	74AS74	F14
B7	74AS02	E15
B8	74AS32	A16
B9	74AS74	C7
CC0	Capacitor	G1
C0	PAL16R8	D10
C1	PAL20R8	E12
C2	74S158	C10
C3	PAL20R8	E12
C4	PAL16R8	D11
C5	PAL20R8	E13
C6	PAL16R8	E14
C7	74AS74	A11
C8	74AS00	A11
C9	74AS10	C11
C10	74AS08	D13
C11	74AS04	C12
C12	74AS32	D12
C13	74AS04	D13
C14	74AS32	A10
C15	74AS08	A12
DI0	DIODE	L16
DI1	DIODE	L16
DI2	DIODE	L16
DI3	DIODE	N16
DI4	DIODE	L15
DI5	LED	H16
D0	74AS20	F11
D1	74AS00	B9
D2	74AS32	C8
D3	74AS04	B4
D4	74AS00	B8
D5	74AS20	A4
D6	74S112	A9
D7	74AS74	A13
D8	74AS74	B9
D9	74AS74	A3
D10	74AS10	A4
D11	74AS08	B15
D12	74AS08	B8
D13	74AS74	B16
E0	74ALS573	A5
E1	74ALS573	B5
E2	74ALS573	C5
E3	74ALS573	D5
E4	74ALS574	D3
E5	74ALS573	A5
E6	74ALS573	B5
E7	74ALS573	C5
E8	74ALS573	D5
E9	74ALS632	A2

Name	Type	Pos
E10	74ALS645	B2
E11	74ALS645	C2
E12	74ALS645	D1
E13	74ALS645	A1
E14	74ALS645	C1
E15	SIL	F1
F0	74AS74	K9
F1	PAL16R8	D9
F2	PAL16R8	D11
F3	PAL20R8	E11
F4	PAL20R8	E10
F5	PAL20R8	E11
F6	74AS04	C10
F7	74AS04	B10
F8	74AS08	B10
G0	74AS32	B13
G1	74AS08	B11
G2	74AS32	A6
G3	74AS08	A6
G4	74AS32	A8
G5	74AS08	A8
G6	74AS32	B12
G7	74AS04	A7
G8	74AS11	B12
G9	74AS11	B11
G10	74AS32	A9
G11	74AS10	A13
G12	74AS02	A10
H0	74AS10	B14
H1	74AS00	C15
H2	74AS74	C16
I0	74AS20	D14
I1	74AS74	C14
I2	74LS541	B1
I3	74S112	F15
I4	74AS20	F13
I5	74AS10	F12
I6	74AS00	F14
I7	74AS08	F13
I8	74AS04	B3
I9	74LS14	H13
I10	74AS21	C13
J1	CON	E1
J2	CON	J1
J3	CON	M1
J6	74AS74	H13
J7	74AS74	J14
J8	74AS74	J14
J9	74AS21	G14
J10	74AS09	L15
J11	74ALS244	J13
J12	74AS04	M15
J13	74LS14	M14
J14	74AS00	L14
J15	74AS32	J15
J16	74AS74	K13
J17	74AS00	H11
J18	74AS20	C15
J19	74AS30	J12
J20	74AS32	H15
J21	74AS74	H14
J22	74AS74	H14
J23	74AS74	J12
K1	74ALS574	L5
K2	74ALS573	L4
K3	74ALS244	H3
K4	74ALS573	L5
K5	74ALS573	L3
K6	74ALS873	D4
K7	6168-45	F4
K8	6168-45	F4
K9	6168-45	G4
K10	6168-45	G4
K11	6168-45	H4
K12	6168-45	H4
K13	6168-45	H4
K14	6168-45	J4
K15	74ALS645	F3

Name	Type	Pos
K16	74ALS645	G3
K17	74ALS645	H3
K18	74ALS645	J2
K19	74AS08	C3
K20	74AS32	B7
K21	74AS32	D8
K22	74AS00	F10
L1	74S283	B4
L2	74S283	C4
L3	74S283	J4
L4	74S283	M3
L5	74ALS573	C4
L6	74ALS573	L3
L7	74ALS573	A2
L8	74ALS573	L2
L9	74ALS573	D2
L10	74S85	M4
L11	74S85	M4
L12	74AS08	K9
L13	74AS04	J9
M1	74ALS873	J4
M2	74ALS573	M1
M3	74ALS573	M2
M4	74ALS573	M2
M5	74ALS573	M3
M6	74ALS873	J3
M7	74ALS574	L2
M8	74ALS873	J3
M9	74ALS573	L1
N1	74ALS573	H5
N2	74ALS573	H5
N3	74ALS573	H8
N4	74ALS573	D10
N5	68020	G6
N6	74ALS645	D5
N7	74ALS645	C5
N8	74ALS645	B5
N9	74ALS645	A5
N10	68881	G7
PD1		F14
PD2		D16
PD3		D10
PD4		F13
PD5		F12
PD6		D12
PD7		F13
PD8		E14
PD9		D9
PD10		D11
PD11		F12
PD12		F11
PD13		F11
PD14		L8
PD15		K8
PD16		H10
PD17		K11
PD18		H10
PD19		K12
PD20		K5
PU1		D16
PU2		M12
PU3		M10
PU4		A14
PU5		A13
PU6		A9
PU7		F15
PU8		H15
PU9		J13
PU10		K11
PU11		H10
PU12		M6
PU13		A3
P1	74ALS573	F2
P2	74ALS573	G2
P3	74ALS573	F3
P4	74ALS573	G3
P5	74ALS573	F2
P6	74ALS573	G2

Component locations

PCB: 3400 / 68020 | Issue: | Date:

dansk data elektronik a/s
herlev hovedgade 199. 2730 herlev. tlf. 02-84 50 11

PRELIMINARY

Name	Type	Pos
P7	74ALS573	H2
P8	74ALS573	J2
P9	74ALS573	F1
P10	74ALS573	G1
P11	74ALS573	H1
P12	74ALS573	J1
P13	74AS32	H7
P14	74AS08	H6
P15	74AS08	F9
P16	74AS32	F9
Q1	27512	L12
Q2	8251	L13
Q3	74ALS645	J13
Q4	74ALS574	G13
Q5	74LS641-1	G14
Q6	74ALS574	G13
Q7	74LS641-1	G15
Q8	75188	M15
Q9	75189	L14
Q10	SWITCH	K15
Q11	74LS32	K13
Q12	3M20	G16
Q13	3M20	K16
RE1	RES4M	H13
RE2	RES4M	L15
RE3	RES4M	M16
RE4	RES4M	G14
RE5	RES4M	G13
RE6	RES4M	H12
RE7	RES4M	D8
RE8	RES4M	D9
RE9	RES4M	A4
RE10	RES4M	L15
RE11	RES4M	L16
RE12	RES4M	L15
RE13	RES4M	L15
RE14	RES4M	L15
RE15	RES4M	L7
RE16	RES4M	E16
RE17	RES4M	E16
RE18	RES4M	L11
RE19	RES4M	L11
RE20	RES4M	M16
RE21	RES4M	K11
RE22	RES4M	N5
RE23	RES4M	N5
RE24	RES4M	N5
RE25	RES4M	N5
RE26	RES4M	G1
RE27	RES4M	M8
RE28	RES4M	F4
RE29		J10
RUN	LED	J16
SI0	RESISTOR	M6
SI1	RESISTOR	F11
SI2	RESISTOR	M7
SI3	RESISTOR	G11
ST1	STRAP	C8
ST2	STRAP	G8
ST3	STRAP	G8
ST4	STRAP	F8
ST5	STRAP	F8
ST6	STRAP	D3
ST7	STRAP	D3
ST8	STRAP	L12
ST9	STRAP	K11
ST10	STRAP	K12
ST11	STRAP	L12
ST12	STRAP	M8
ST13	STRAP	L11
ST15	STRAP	F8
ST16	STRAP	E5
ST17	STRAP	D3
ST18	STRAP	D2
ST19	STRAP	E12
S1	74ALS580	L6
S2	74ALS573	L7
S3	74ALS574	L6

Name	Type	Pos
S4	74LS38	M6
S5	74LS38	L10
S6	74ALS574	J7
S7	74LS148	J6
S8	74LS74	L9
S9	74LS353	L10
S10	SWITCH	E16
T1	TMS2150-4	E8
T2	TMS2150-4	E7
T3	TMS2150-4	E8
T4	TMS2150-4	E9
T5	6168-45	E6
T6	6168-45	E6
T7	6168-45	D6
T8	6168-45	D6
T9	6168-45	C6
T10	6168-45	C6
T11	6168-45	C6
T12	6168-45	B6
T13	TMS2150-4	D3
T14	TMS2150-4	D2
U1	74LS590	K10
U2	74ALS574	J10
U3	74ALS573	J10
U4	TMM2018D-35	J8
U5	PAL20R8A	L8
U6	74ALS573	J8
U7	74ALS573	L7
U8	PAL20R8A	L8
U9	PAL16R6A	J7
U10	74LS353	M7
V1	PAL20L8A	H6
V2	PAL20L8A	E9
V3	PAL20R8A	G10
V4	PAL16R8A	J11
V5	74AS138	H7
V6	74AS138	H8
V7	74AS30	C9
V8	74AS02	D9
V9	74ALS642	L4
V10	74AS74	H12
V11	74AS20	H10
V12	74AS32	H9
V13	74AS32	H11
W1	PAL20R6A	G11
W2	PAL20R6A	G12
W3	PAL20R6A	G12
W4	74LS273	J9
W5	74LS273	G9
W6	74AS74	F12
W7	74AS11	H12
W8	74AS74	M10
X1	PAL16R8A	G10
X2	PAL16R8A	G11
X3	PAL16R8A	G9
X4	PAL16R8A	J11
Y1	XOSC40M	M11
Y2	XOSC33M	M11
Y3	XOSC50M	M14
Y4	74AS74	L11
Y5	74AS74	L12
Y6	74AS74	M12
Y7	74AS74	M9
Y8	74AS74	K11
Y9	74LS14	L9
Y10	74ALS642	M8
Y11	74LS390	K14
Y12	74LS390	K12
Y13	74LS390	L11
Y14	74LS393	M9
Y15	74LS393	M10
Y16	74S140	M7
Y17	SWITCH	M6
Y18	74AS04	K14
Z1	PAL20L8A	J6
Z2	PAL20R8A	J5
Z3	74ALS641-1	J5
Z4	SWITCH	M5

Name	Type	Pos
Z5	74AS74	H9
Z6	74AS74	H10
Z7	74LS14	F10
Z8	74AS32	K10
Z9	74LS14	H2
Z10	SWITCH	M5
Z11	SWITCH	F11

Component locations

PCB: 3400 / 68020 | Issue: | Date:

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Supermax Technical Data Sheet

Type:	CPU 68030 Module. PCB 4101.
Data sheet no:	21
Revision no:	0
Date:	90-10-15

General Description

The CPU 68030 is a CPU module in a Supermax system. The CPU module contains a 68030 CPU, a 68882 FPC, and the following interfaces:

- Interface to I/O bus.
- Interface to memory modules.
- Front panel display.
- Service port.

The CPU 68030 is not compatible with earlier CPU modules. The CPU 68030 has a physical cache that contains 128 Kb.

Interface to I/O bus

The CPU has a standard interface to the common Supermax I/O bus.

Active cycles	Passive cycles
8 bit read/write	8 bit read/write
16 bit read/write	16 bit read/write
32 bit read/write	32 bit read/write
Read-modify-write	Read-modify-write
	Burst read/write

Interface to memory modules

The CPU 68030 module is designed to control memory modules type RAM 3100. Memory modules are connected to the CPU module via the local memory bus. The CPU module controls the memory modules and takes care of error detection and correction. The CPU module executes the following cycles in memory modules:

- Refresh cycle
- Double word read cycle
- Double word write cycle
- Burst mode read cycle

The local memory bus is multiplexed between address and data. In the first part of a memory cycle the bus transfers address from the CPU module to the memory modules, and in the second part the bus transfers the data between CPU module and the memory modules. In a burst mode read cycle one block of data is read from the memory and written in the cache. The block size is four double words that is 16 bytes.

Interface to front panel display

The front panel display consists of two seven segment displays, a red LED, and a green LED. The seven segment displays are under program control and used by the operating system to display various error information. The red LED and the green LED are also under program control. The operating system will turn the red LED on, when it is running, and the green LED on when a user program is running. The front panel display is connected to the CPU module via a 20 pin flat cable.

Interface to service port

The interface to the service port is a modified RS-232C interface. All output signals are *open collector* signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to −12 V when not driven by an output.

Power Requirements

Voltage	Typical current
+ 5 V ±5%	13.0 A
+12 V ±5%	0.2 A
−12 V ±5%	0.2 A

Installation

Before a CPU module is installed in a Supermax system the following items must be selected or checked:

- Unit number/priority.
- Pull-up resistors.
- Bus clock.
- Pull-down resistors.
- Straps.

These items are described in detail in the following text.

Unit number/Priority

Each intelligent Supermax module connected to the common I/O bus has a unique address. This address is called the unit number.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot use the same priority. The CPU module uses one priority. The CPU module is equipped with a unit number switch. The switch gives the module a unit number and one priority.

Switch position	Unit number	Priority
0	0x00	00
1	0x01	01
2	0x02	02
3	0x03	03
4	0x04	04
5	0x05	10
6	0x06	11
7	0x07	12
8	0x08	13
9	0x09	14
A	0x0A	20
B	0x0B	21
C	0x0C	22
D	0x0D	23
E	0x0E	24
F	0x0F	30

Pull-up resistors

One and only one CPU module in a Supermax system must contain pull-up resistors for various signals and drive the bus clock in the I/O bus. In a 24 position Supermax system that CPU should be placed in the first position in the second cabinet. In a 24 position Supermax system an additional CPU module must have pull-up resistors for the arbitration signals only. The position of that CPU module is not significant. All the pull-up resistors are connected to the signals through a switch. The switches are:

U6 Contains the pull-up resistors for the arbitration signals

W14 Contains the pull-up resistors for other signals

T20 Contains the pull-up resistors for other signals

Pull-down resistors

Output signals from the service port are open collector signals. These signals must be pulled down to −12V by one module in a Supermax system. Pull-down resistors are connected to output signals when all switches in P10 are in the **ON** position.

Bus clock

The arbitration scheme in the I/O bus uses a clock. One and only one CPU module in a Supermax system must drive the bus clock.

The CPU module drives the bus clock when switch P10 bit 7 is in the ON position.

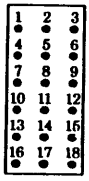
Straps

* designates factory installed position.

STE1:

Size of external cache		
*	1-3	128 Kb
*	2-4	128 Kb
	3-5	64 Kb
	4-6	64 Kb

STP1:



Size of the EPROM.		
*	4-5	27512

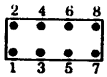
STQ1:

Start-up		
	1-2	Debug operation
*	2-3	Normal operation

STR1:

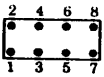
Inhibit the internal caches.		
*	NC	Cache content is controlled by software
	1-2	Cache content is not changed

STT1:



Clock frequency, 68030		
	1-2	33.3 MHz
*	3-4	25.0 MHz
	5-6	20.0 MHz
	7-8	16.6 MHz

STT2:



Clock frequency, 68882		
	1-2	33.3 MHz
	3-4	25.0 MHz
*	5-6	20.0 MHz
	7-8	16.6 MHz

STT3:

Clock frequency, control logic		
	1-2	25.0 MHz
*	3-4	20.0 MHz
	5-6	16.6 MHz

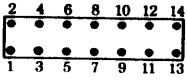
STT4:

Clock frequency, bus clock		
	1-2	10.0 MHz
*	3-4	8.3 MHz

STT5:

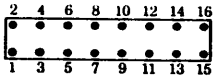
Clock frequency, time out clock		
	1-2	100 kHz (10 µs)
*	2-3	10 kHz (100 µs)

STT6:



Baud rate service port		
	1-2	19200
*	3-4	9600
	5-6	4800
	7-8	2400
	9-10	1200
	11-12	600
	13-14	300

STT7:



Delay time in clock circuitry		
*	1-3	Do not change
*	5-7	Do not change
*	9-10	Do not change
*	11-12	Do not change
*	13-15	Do not change

STT8:

Cache enable, external cache		
*	1-2	Control register bit 6
	2-3	Address bit 20

STZ1:

Disable internal caches		
*	NC	Controlled by software
	1-2	Disabled

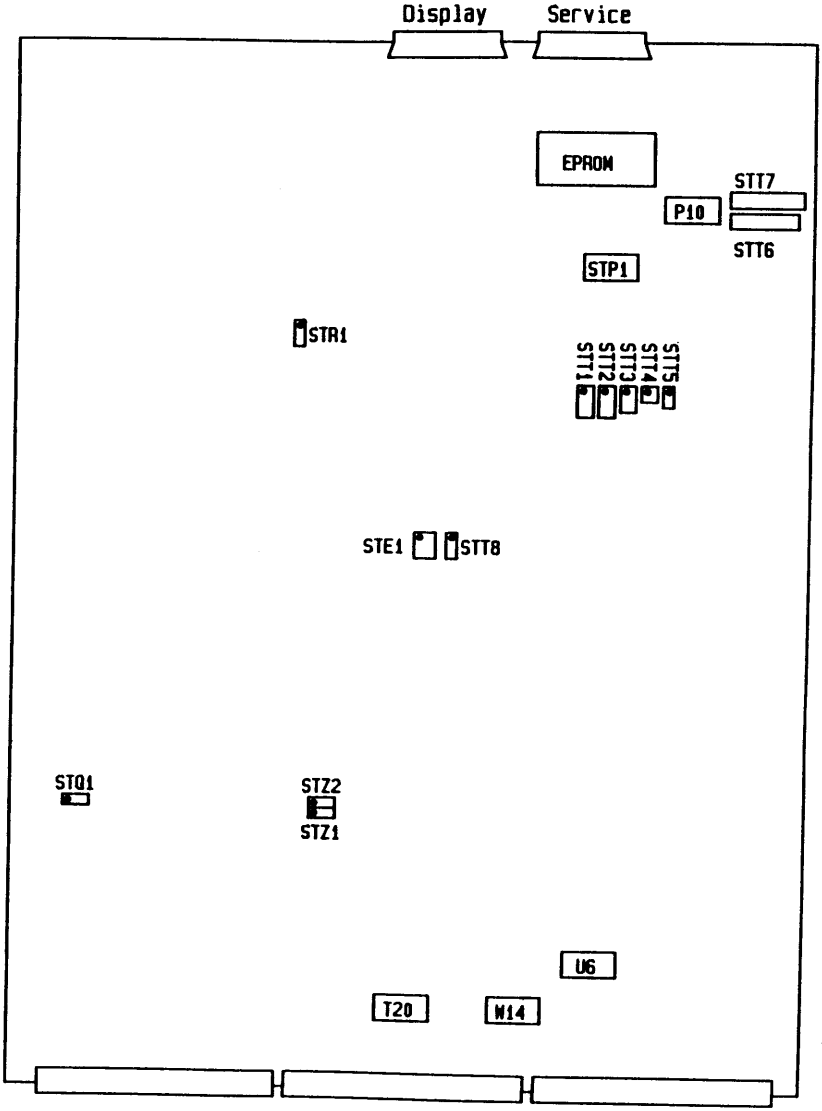
STZ2:

Disable PMMU		
*	NC	Controlled by software
	1-2	Disabled

Basic CPU module

Supermax systems are delivered with one basic CPU 68030 module. The basic CPU module differs from the standard CPU modules described above on the following points:

- Unit number cannot be changed. It is fixed to unit number 0x03.
- Priority cannot be changed. It is fixed to priority 03.


Display
Service
EPROM
STT7
P10
STT6
STP1
STR1
STT1
STT2
STT3
STT4
STT5
STE1
STT8
STQ1
STZ2
STZ1
U6
T20
M14

Type: CPU 4100

Data sheet no.: 18

Revision no.: 1

Date: 881013

General description:

The CPU 4100 is a CPU module in a Supermax system. The CPU module contains a 68030 CPU, a 68882 FPC, and the following interfaces:

- Interface to I/O bus.
- Interface to memory modules.
- Front pannel display.
- Service port.

The CPU 4100 is not compatible with earlier CPU modules. The CPU 4100 has a physical cache that contains 128 Kb.

Interface to I/O bus:

The CPU has a standard interface to the common Supermax I/O bus.

Active cycles : Byte read and write.
Word read and write.
Double word read and write.
Read modify write.

Passive cycles: Byte read and write.
Word read and write.
Double word read and write.
Read modify write.
Burst mode read and write.

Interface to memory modules:

The CPU 4100 module is designed to control memory modules type RAM 3100. The CPU 4100 module cannot control memory modules of type 0200, 1400, and 3000.

Memory modules are connected to the CPU module via the local memory bus. The CPU module controls the memory modules and takes care of error detection and correction. The CPU module executes the following cycles in memory modules:

Refresh cycle
Double word read cycle
Double word write cycle
Burst mode read cycle

The local memory bus is multiplexed between address and data. In the first part of a memory cycle the bus transfers address from the CPU module to the memory modules, and in the second part the bus transfers the data between CPU module and the memory modules. In a burst mode read cycle one block of data is read from the memory and written in the cache. The block size is four double words that is 16 bytes.

Interface to front panel display:

The front panel display consists of two seven segment displays, a red LED, and a green LED. The seven segment displays are under program control and used by the operating system to display various error information. The red LED and the green LED are also under program control. The operating system will turn the red LED on, when it is running, and the green LED on when a user program is running. The front panel display is connected to the CPU module via a 20 pin flat cable.

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

Power requirements:

Voltage		Typ. current
+ 5	+-5%	13.0 A
+12	+-5%	200 mA
-12	+-5%	200 mA

Installation:

Before a CPU module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Pull up resistors.
- Bus clock.
- Pull down resistors.
- Straps.

These items are described in details in the following text.

Unit number/Priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. This address is called the unit number.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot use the same priority. The CPU module uses one priority. The CPU module is equiped with a unit number switch. The switch gives the module a unit number and one priority.

Switch position	Unit number	Priority
0	0x00	00
1	0x01	01
2	0x02	02
3	0x03	03
4	0x04	04
5	0x05	10
6	0x06	11
7	0x07	12
8	0x08	13
9	0x09	14
A	0x0a	20
B	0x0b	21
C	0x0c	22
D	0x0d	23
E	0x0e	24
F	0x0f	30

Pull up resistors:

One and only one CPU module in a Supermax system must contain pull up resistors for various signals in the I/O bus. All these pull up resistors on CPU 4100 are connected to signals in the IO bus by switches. The switches are:

T20

W14

U6

P10

Bus clock:

The arbitration scheme in the I/O bus uses a clock. One and only one CPU module in a Supermax system must drive the bus clock.

The CPU module drives the bus clock when switch T20 bit 7 is in the ON position.

Pull down resistors for the service port:

Output signals from the service port are open collector signals. These signals must be pulled down to -12v by one and only one module in a Supermax system. Pull down resistors are connected to output signals in the service port when all switches in P10 are in the ON position.

Straps and jumpers:

+ designates factory installed position.

STE1

Function: Controls the size of the external cache.

```
        2  4  6
STE1:   *  *  *
        *  *  *
        1  3  5
```

+ Pin 1 connected to pin 3 and pin 2 connected to pin 4:

The size of the external cache is 128 Kb.

Pin 3 connected to pin 5 and pin 4 connected to pin 6:

The size of the external cache is 64 Kb.

STP1

Function: Must be strapped according to the size of the EPROM.

```
        1  2  3
STP1:   *  *  *
      4 *  *  *
      7 *  *  *
     10 *  *  *
     13 *  *  *
        *  *  *
       16 17 18
```

+ Pin 4 connected to pin 5: Corresponds to EPROM type 27512.

STQ1

Function: Not used.

```
STQ1:   *  *  *
        1  2  3
```

+ No connections.

STR1

Function: Inhibits the internal caches.

```
STR1:   *  *
        1  2
```

+ pin 1 not connected to pin 2:

The use of the internal caches is controlled by software.

pin 1 connected to pin 2:

The content of the internal caches is not changed.

STT1

Function: Controls the frequency of the clock to the 68030.

```
        2  4  6  8
STT1:   *  *  *  *
        *  *  *  *
        1  3  5  7
```

	Pin 1 connected to pin 2:	33.3 MHz
+	Pin 3 connected to pin 4:	25.0 MHz
	Pin 5 connected to pin 6:	20.0 MHz
	Pin 7 connected to pin 8:	16.6 Mhz

STT2

Function: Controls the frequency of the clock to the 68882.

```
        2  4  6  8
STT2:   *  *  *  *
        *  *  *  *
        1  3  5  7
```

```
  Pin 1 connected to pin 2:     33.3 MHz
  Pin 3 connected to pin 4:     25.0 MHz
+ Pin 5 connected to pin 6:     20.0 MHz
  Pin 7 connected to pin 8:     16.6 Mhz
```

STT3

Function: Controls the frequency of the clock to the control logic.

```
        2  4  6
STT3:   *  *  *
        *  *  *
        1  3  5
```

```
  Pin 1 connected to pin 2:     25.0 MHz
+ Pin 3 connected to pin 4:     20.0 MHz
  Pin 5 connected to pin 6:     16.6 MHz
```

STT4

Function: Controls the frequency of the bus clock.

```
        2  4
STT4:   *  *
        *  *
        1  3
```

```
  Pin 1 connected to pin 2:     10.0 MHz
+ Pin 3 connected to pin 4:      8.3 MHz
```

STT5

Function: Controls the frequency of the time out clock.

```
STT5:   *  *  *
        1  2  3
```

```
  Pin 1 connected to pin 2:     100 KHz  (10 us)
+ Pin 2 connected to pin 3:      10 KHz  (100 us)
```

STT6

Function: Controls the baud rate of the service port.

```
        2  4  6  8 10 12 14
STT6:   *  *  *  *  *  *  *
        *  *  *  *  *  *  *
        1  3  5  7  9 11 13
```

Baud rate.

```
  Pin 1  connected to pin 2 : 19200
```

+ Pin 3 connected to pin 4 : 9600
  Pin 5 connected to pin 6 : 4800
  Pin 7 connected to pin 8 : 2400
  Pin 9 connected to pin 10: 1200
  Pin 11 connected to pin 12: 600
  Pin 13 connected to pin 14: 300

STZ1

Function: Disables the internal caches.

```
STZ1:   *  *
        1  2
```

+ Pin 1 not connected to pin 2:

The use of the internal caches is controlled by software.

  Pin 1 connected to pin 2:

The internal caches are disabled.

STZ2

Function: Disables the PMMU.

```
STZ2:   *  *
        1  2
```

+ Pin 1 not connected to pin 2:

The use of PMMU is controlled by software.

  Pin 1 connected to pin 2:

The PMMU is disabled.

Basic CPU module:

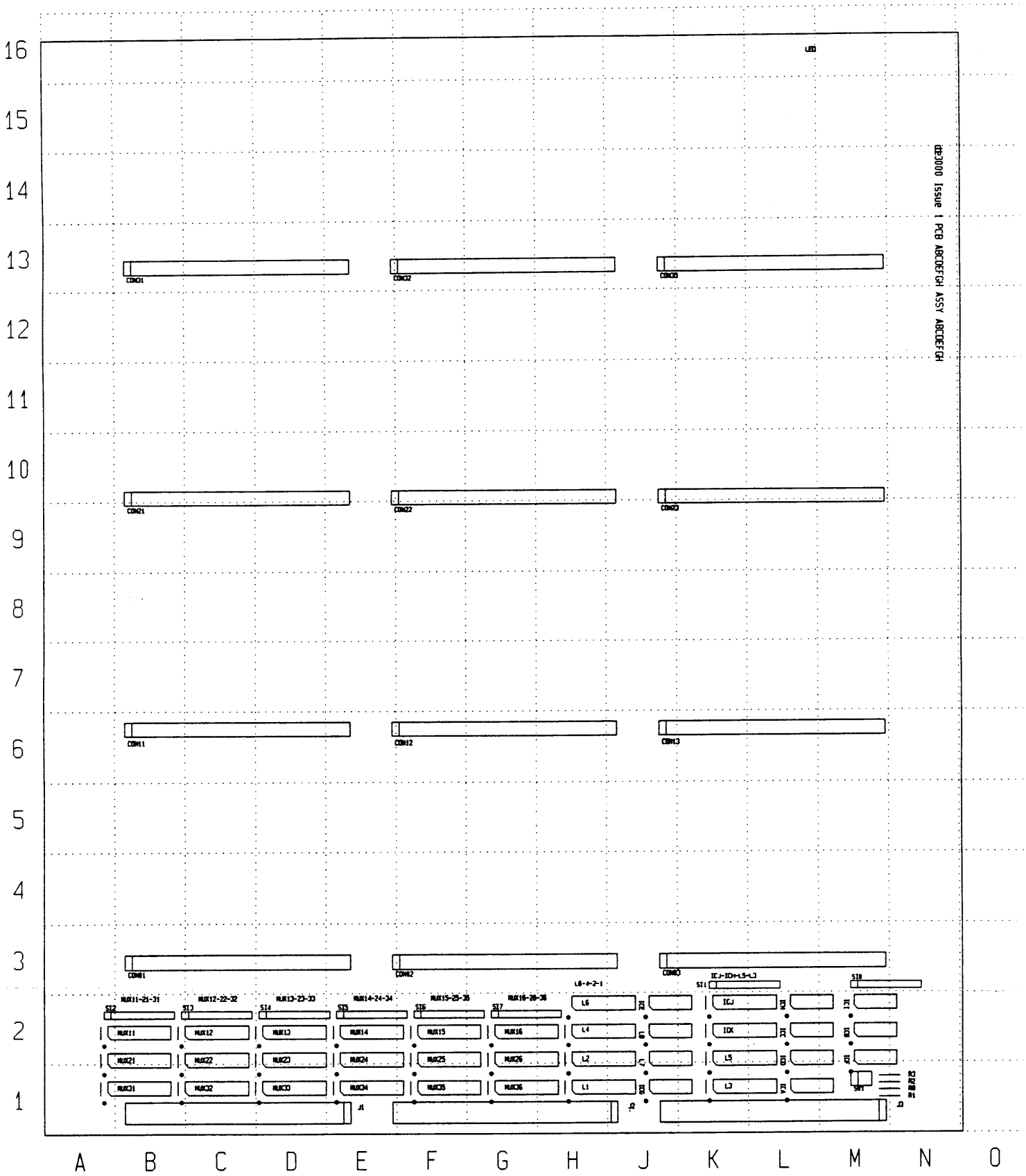
Supermax systems are delivered with one basic CPU module 4100.

The basic CPU module differs from the standard CPU modules described above on the following points:

Unit number cannot be changed. It is fixed to unit number three.

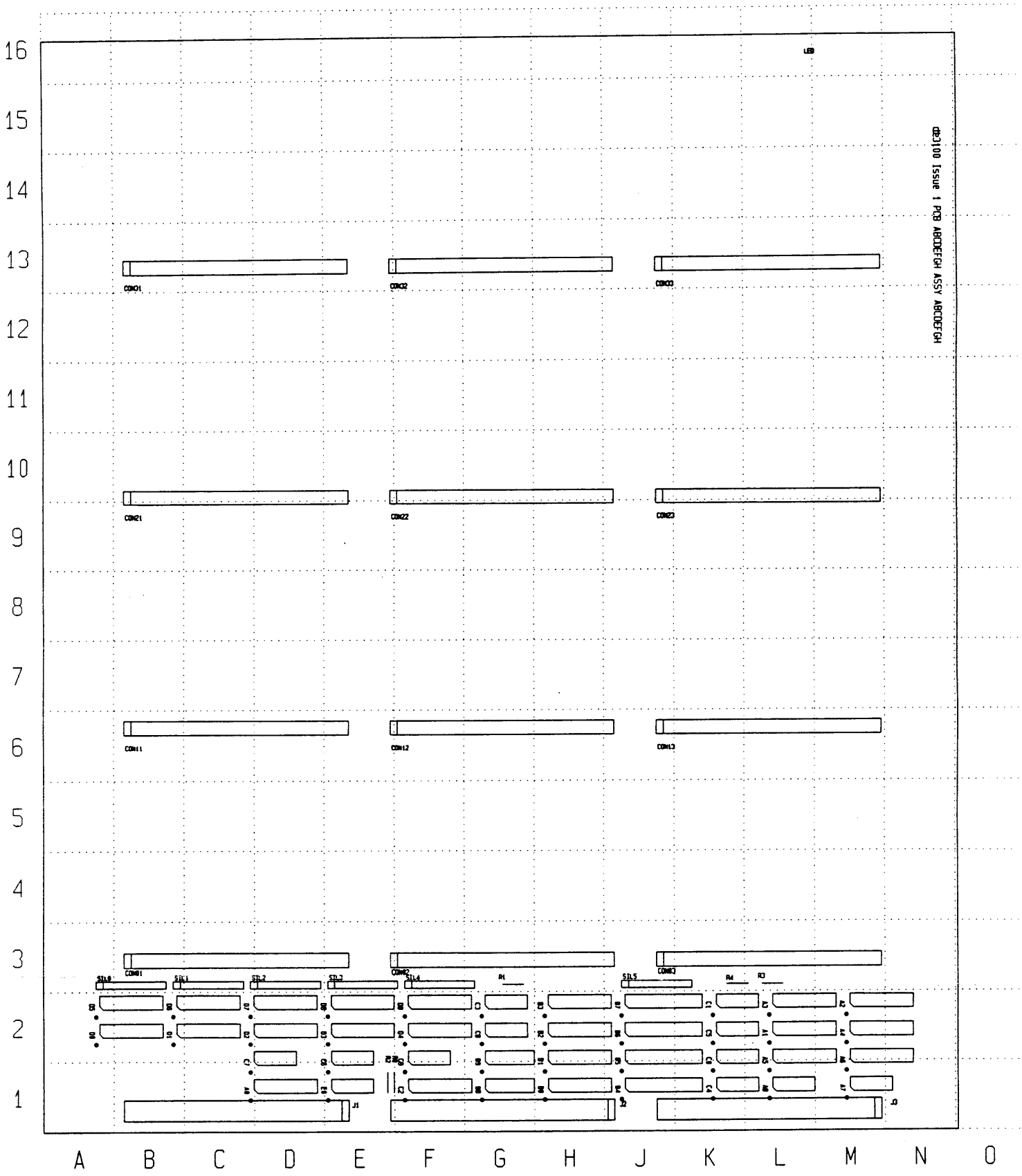
Priority cannot be changed. It is fixed to priority 03.

PRELIMINARY



Component locations				
PCB: Memory	Issue:	Date:	dde	dansk data elektronik a/s herlev hovedgade 199. 2730 herlev. tlf. 02-84 50 11

PRELIMINARY



Component locations				
PCB: Memory	Issue:	Date:	dde	dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11

PRELIMINARY

Name	Type	Pos
:LABEL		0-1
CON01	CON64	B3
CON02	CON64	E3
CON03	CON64	J3
CON11	CON64	B6
CON12	CON64	E6
CON13	CON64	J6
CON21	CON64	B10
CON22	CON64	E10
CON23	CON64	J10
CON31	CON64	B13
CON32	CON64	E13
CON33	CON64	J13
ICA	74LS14	L1
ICB	74S00	M2
ICC	74S02	L2
ICD	74S10	L1
ICE	74LS14	J2
ICF	74S10	M1
ICG	74LS14	J1
ICH	74S10	L2
ICI	74S05	M2
ICJ	PAL20L8	K2
ICK	74ALS576	K2
J1	CON96	E1
J2	CON96	J1
J3	CON96	M1
LED	LED	L16
L1	74ALS244	H1
L2	74ALS244	H1
L3	74ALS573	K1
L4	74ALS573	H2
L5	74ALS573	K1
L6	74ALS573	H2
L7	74LS393	J1
L8	74LS393	J2
MUX11	74ALS244	A2
MUX12	74ALS244	B2
MUX13	74ALS244	D2
MUX14	74ALS244	E2
MUX15	74ALS244	F2
MUX16	74ALS244	G2
MUX21	74ALS244	A1
MUX22	74ALS244	B1
MUX23	74ALS244	D1
MUX24	74ALS244	E1
MUX25	74ALS244	F1
MUX26	74ALS244	G1
MUX31	74ALS244	A1
MUX32	74ALS244	B1
MUX33	74ALS244	D1
MUX34	74ALS244	E1
MUX35	74ALS244	F1
MUX36	74ALS244	G1
R0	RES4M	M1
R1	RES4M	M1
R2	RES4M	M1
R3	RES4M	M1
SI0	SIL10	M3
SI1	SIL10	K3
SI2	SIL10	A2
SI3	SIL10	B2
SI4	SIL10	D2
SI5	SIL10	E2
SI6	SIL10	F2
SI7		G2
SW1		M1

Component locations

PCB: Memory | Issue: | Date:

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PRELIMINARY

Name	Type	Pos	Name	Type	Pos	Name	Type	Pos
:LABEL		O-1						
A0	74AS573	C1						
A1	74AS573	L2						
A2	74AS573	M2						
A3	74AS573	L2						
A4	74AS573	M2						
A5	74ALS244	L1						
A6	74ALS244	M1						
A7	74LS393	M1						
A8	74LS393	L1						
B0	PAL16L8	H1						
B1	PAL16L8	H1						
B2	PAL16L8	H2						
B3	PAL16L8	H2						
B4	PAL20L8	J1						
B5	PAL20L8	J1						
B6	PAL20L8	J2						
B7	PAL20L8	J2						
B8	74LS175	G1						
B9	74LS175	G1						
CON01	CON64	B3						
CON02	CON64	E3						
CON03	CON64	J3						
CON11	CON64	B6						
CON12	CON64	E6						
CON13	CON64	J6						
CON21	CON64	B10						
CON22	CON64	E10						
CON23	CON64	J10						
CON31	CON64	B13						
CON32	CON64	E13						
CON33	CON64	J13						
C0	74S20	K1						
C1	74S20	K2						
C2	74ALS240	F1						
C3	74S38	G2						
C4	74S20	K1						
C5	74S00	K2						
C6	74S00	E1						
C7	74S02	C1						
C8	74LS14	G2						
C9	74LS14	F1						
D0	74AS573	A2						
D1	74AS573	B2						
D2	74AS573	C2						
D3	74AS573	E2						
D4	74AS573	F2						
D5	74ALS244	A2						
D6	74ALS244	B2						
D7	74ALS244	C2						
D8	74ALS244	E2						
D9	74ALS244	F2						
E0	74LS74	E1						
J1	CON96	E1						
J2	CON96	J1						
J3	CON96	M1						
LED	LED	L16						
R0	RES4M	E1						
R1	RES4M	G3						
R2	RES4M	E1						
R3	RES4M	L3						
R4	RES4M	K3						
SIL0	SIL10	A3						
SIL1	SIL10	B3						
SIL2	SIL10	C3						
SIL3	SIL10	E3						
SIL4	SIL10	F3						
SIL5	SIL10	J3						

Component locations

PCB: Memory | Issue: | Date:

dansk data elektronik a/s
herlev hovedgade 199. 2730 herlev. tlf. 02-84 50 11

Supermax Technical Data Sheet

Type:	CPU R3000 Module
Data sheet no:	20
Revision no:	0
Date:	90-05-07

General Description

CPU modules are the main processing elements in a Supermax system.

The CPU R3000 module is based on a 25 MHz MIPS R3000 microprocessor and contains this microprocessor and the following elements:

- Cache memory
- Write Buffers
- Boot loader PROM
- Service port
- Interrupt unit
- Floating Point Accelerator, FPA
- Memory control circuitry
- Interface to the local memory bus
- Interface to the I/O bus

Cache Memory

The cache memory is a fast static RAM that stores frequently used instructions and data. The cache memory consists of two independent caches, one for instructions and one for data. Each cache contains 2048 entries and each entry contains 8 double words, that is a total of 2 × 64 Kb.

When the R3000 executes an instruction fetch cycle, the content of the instruction cache is examined. If the address is found in the cache, the cache content is sent to the R3000 with one double word per clock cycle. During the same clock cycle the R3000 can execute a data read cycle and then the content of the data cache is examined. If the address is found in the cache, the cache content is sent to the R3000 with one double word per clock cycle. The total transfer rate will be two double words per clock cycle.

If the address is not found in the instruction cache, eight double words are read from the main memory in burst mode. The eight instructions will be executed by the R3000 and at the same time stored in the instruction cache.

If the address is not found in the data cache, eight double words are read from the main memory in burst mode. The eight double words will be read by the R3000 and stored in the data cache.

In burst mode the transfer rate will be:

- Memory to cache – 100 Mb/s.
- Cache to R3000 – 200 Mb/s

The performance of the CPU module is appx. 20 mips (million instructions per second).

Write Buffers

When the R3000 executes a write cycle, data will be written in the four R3020 Write Buffers, which are able to receive a write access in one clock cycle. The Write Buffers will then write the data to the *slower* main memory. In this case the R3000 will not be hung up by the memory cycle. The Write Buffers can hold up to four pending write cycles.

Boot Loader PROM

The boot loader PROM consists of 256Kb of UV erasable memory. This memory is used for a boot load program and a diagnostic program. The starting address of the PROM is 0x1fc0000. After reset, the R3000 starts executing instructions in that address in the PROM. The PROM is always enabled.

Service Port

Like all other units in the Supermax the CPU module has a service port. The interface to the service port is a modified RS-232C interface. All output signals are *open collector* signals and may be wired together with the corresponding output signals from other units of a Supermax system. Pull down resistors are used to pull the signals down to –12V when they are not driven by an output.

Interrupt Unit

The interrupt unit generates interrupts to the R3000. Interrupts are caused by events on the CPU module itself, internal interrupts, or generated by the I/O bus, external interrupts. The R3000 has one interrupt level, but six interrupt inputs. The CPU module has 10 interrupt sources, so more than one source is connected to each input.

Units connected to the I/O bus may interrupt the CPU by writing in a certain part of its main memory. The interrupt unit decodes the write address and generates an interrupt on the corresponding level.
Interrupts are enabled and disabled by a mask register.

Floating Point Accelerator

The Floating Point Accelerator, FPA, is a 25 Mhz MIPS R3010. The FPA fully conforms to the requirements of ANSI/IEEE Standard 754–1985, "IEEE Standard for Binary Floating– Arithmetic", including all recommendations. The operands are 64 bits, of which 53 bits are used as mantissa.

Memory Control Circuitry

This circuitry controls the memory modules connected to the CPU module. It generates and checks ECC bit, corrects single bit errors, detects double bit errors, implements byte write, word write and burst read/write, refreshes the memory modules etc.
The CPU module is designed to control memory mother modules type 4400 only. This module must contain an even number of memory daughter modules. A maximum of four mother modules can be connected to the CPU module.

Interface to the local Memory Bus

A CPU module has its own private memory consisting of one or more memory mother modules. The local memory bus is the connection between a CPU module and its main memory. The local memory bus is 39 bits wide. It is used for both address and data transfers. In the first part of a memory cycle the address is transferred to the memory modules and in the second part the local memory bus is used for data transfer.
The maximum amount of memory that can be connected to a CPU module is 256 Mb.

Interface to the I/O Bus

The interface to the I/O bus consists of two different interfaces. One interface is used by the CPU module when it addresses other units on the I/O bus. Here the CPU module is the active part in a bus transfer. This interface drives the full 34 bit wide address bus and the full 32 bit data bus.

The other interface is used when units connected to the I/O bus address the main memory of the CPU module. Here the CPU module is the passive part in a bus transfer.

The active and the passive part of these interfaces implements the following bus cycles:

Active cycles	Passive cycles
8 bit read/write	8 bit read/write
16 bit read/write	16 bit read/write
32 bit read/write	32 bit read/write
Read-modify-write	Read-modify-write
	Burst read/write

Indicators

The CPU module has a 20 pin flat cable connector located near the front edge of the module. This connector drives a front panel display. The front panel display consists of two seven segment displays, a red LED and a green LED. They are all controlled by the operating system.

The seven segment displays are used for status and error codes. The red LED is turned on by the operating when it is running, and the green LED is turned on when a user program is running.

Power Requirements

Voltage	Typical current
+ 5 V ±5%	14.5 A
+12 V ±5%	0.2 A
−12 V ±5%	0.2 A

Installation

Before a CPU module is installed in a Supermax system, the following items must be selected or checked.

- Unit number/priority.
- Pull-up resistors.
- Bus clock.
- Pull-down resistors.
- Straps.

These items are described in detail in the following text.

Unit number/Priority

The unit number and the priority of the CPU module is selected by turning a hexadecimal switch. The CPU R3000 module uses one priority.

Switch position	Unit number	Priority
0	0x00	00
1	0x01	01
2	0x02	02
3	0x03	03
4	0x04	04
5	0x05	10
6	0x06	11
7	0x07	12
8	0x08	13
9	0x09	14
A	0x0A	20
B	0x0B	21
C	0x0C	22
D	0x0D	23
E	0x0E	24
F	0x0F	30

Pull-up resistors

One and only one CPU module in a Supermax system must contain pull-up resistors for various signals and drive the bus clock in the I/O bus. In a 24 position Supermax system that CPU should be placed in the first position in the second cabinet. In a 24 position Supermax system an additional CPU module must have pull-up resistors for the arbitration signals only. The position of that CPU module is not significant. All the pull-up resistors are connected to the signals through a switch. The switches are:

H11 Contains the pull-up resistors for the arbitration signals

H14 Contains the pull-up resistors for other signals

G25 Contains the pull-up resistors for other signals

Pull-down resistors

Output signals from the service port are open collector signals. These signals must be pulled down to −12V by one module in a Supermax system. Pull-down resistors are connected to output signals when all switches in F12 are in the **ON** position.

Straps

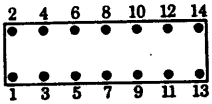
Straps T1, T2, T3, T4, T8 are installed for factory testing only. Do not short circuit any of those straps.

* designates factory installed position.

ST1:

EPROM size		
*	1-2	512 Kbit
	2-3	1 Mbit

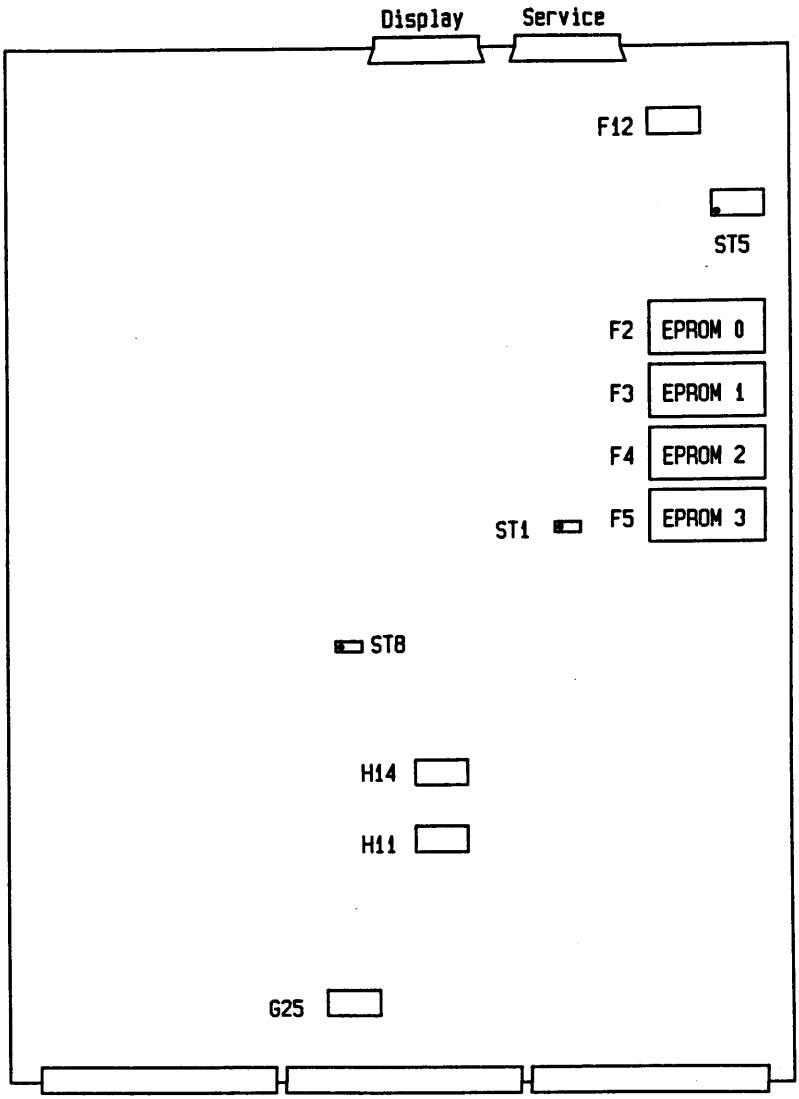
ST5:



Baud rate service port		
	1-2	19200
*	3-4	9600
	5-6	4800
	7-8	2400
	9-10	1200
	11-12	600
	13-14	300

ST8:

Self test output mode		
*	1-2	No output from self test on service port
	NC	Output from self test on service port


Display
Service
F12
ST5
F2
EPROM 0
F3
EPROM 1
F4
EPROM 2
ST1
F5
EPROM 3
ST8
H14
H11
G25

SUPERMAX technical data sheet.
Module: DIOC 0400

Type: DIOC 0400

Data sheet no.: 6

Revision no.: 0

Date: 851008

General description:

The DIOC is the intelligent Disk IO Controller in a SUPERMAX system. The DIOC is built around a microprocessor and contains the following interfaces:

- floppy disk interface
- streaming tape interface
- winchester disk interface

Interface to I/O bus:

The DIOC has a standard interface to the common SUPERMAX I/O bus. The local memory bus is not used.

Active cycles : Byte read and write.
Dobbelt word read and write.

Passive cycles: Byte read and write.
Word read and write.
Read modify write.

Interface to peripheral equipment:

Winchester disk interface:

The winchester disk interface is the Small Computer System Interface ANSI X3T9.2, SCSI.
The connector is a 50 pin flatcable header. DIN-41651.

PIN	Signal	Signal	PIN
01	GND	-DB(0)	02
03	GND	-DB(1)	04
05	GND	-DB(2)	06
07	GND	-DB(3)	08
09	GND	-DB(4)	10
11	GND	-DB(5)	12
13	GND	-DB(6)	14
15	GND	-DB(7)	16
17	GND	-DB(P)	18
19	GND	GND	20
21	GND	GND	22
23	GND	GND	24
25	open	open	26
27	GND	GND	28
29	GND	GND	30
31	GND	-atn	32
33	GND	GND	34
35	GND	-bsy	36
37	GND	-ack	38
39	GND	-rst	40
41	GND	-msg	42
43	GND	-sel	44
45	GND	-c/d	46
47	GND	-req	48
49	GND	-i/o	50

- designates active low signals.

Streaming tape interface:

The streaming tape interface is Quarter-inch Interchange Committee interface, QIC II.
The connector is a 50 pin flatcable header. DIN-41651.

PIN	Signal	Signal	PIN
01	GND	open	02
03	GND	open	04
05	GND	open	06
07	GND	open	08
09	GND	open	10
11	GND	-DB(7)	12
13	GND	-DB(6)	14
15	GND	-DB(5)	16
17	GND	-DB(4)	18
19	GND	-DB(3)	20
21	GND	-DB(2)	22
23	GND	-DB(1)	24
25	GND	-DB(0)	26
27	GND	-onl	28
29	GND	-req	30
31	GND	-rst	32
33	GND	-tfer	34
35	GND	-ack	36
37	GND	-rdy	38
39	GND	-exc	40
41	GND	-dir	42
43	GND	open	44
45	GND	open	46
47	GND	open	48
49	GND	open	50

- designates active low signals.

Floppy disk drive interface:

The DIOC module is mounted with components for interface to an 8 or 5.25 inch floppy disk drive.

The connector is a 50 pin flatcable header for 8 inch disk drive interface. DIN-41651.

PIN	Signal	Signal	PIN
01	GND	open	02
03	GND	open	04
05	GND	open	06
07	GND	-tg43	08
09	GND	open	10
11	GND	open	12
13	GND	side sel	14
15	GND	open	16
17	GND	-head load	18
19	GND	-index	20
21	GND	-ready	22
23	GND	open	24
25	GND	-sel0	26
27	GND	-sel1	28
29	GND	-sel2	30
31	GND	-sel3	32
33	GND	direction	34
35	GND	-step	36
37	GND	-write data	38
39	GND	-write gate	40
41	GND	-track 00	42
43	GND	-write prt	44
45	GND	-read data	46
47	GND	open	48
49	GND	open	50

- designates active low signals.

The connector is a 34 pin flatcable header for 5.25 inch disk drive interface. DIN-41651.

PIN	Signal	Signal	PIN
01	GND	-head load	02
03	GND	-open	04
05	GND	nc	06
07	GND	-index	08
09	GND	-sel0	10
11	GND	-sel1	12
13	GND	-sel2	14
15	GND	-motor on	16
17	GND	direction	18
19	GND	-step	20
21	GND	-write data	22
23	GND	-write gate	24
25	GND	-track 00	26
27	GND	-write prt	28
29	GND	-read data	30
31	GND	side sel	32
33	GND	-ready	34

- designates active low signals.

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

Power requirements:

Voltage		Typ. current
+ 5	+-5%	7.0 A
+12	+-5%	0.06 A
-12	+-5%	0.06 A

Physical dimension:

Standard SUPERMAX module.

Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a DIOC module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Straps.
- Pull down resistors for the service port.
- Flat cables for the disks.
- Firmware.

These items are described in details in the following text.

Unit number/Priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. The address is called the unit number. The unit number of the DIOC module is coded in a PAL located in position I1. This PAL is called the unit PAL.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot used the same priority. The DIOC module uses two priorities. The priorities of the DIOC module are coded in two PALs located in position N1 and N3. This PALs are called the priority PALs.

Pull down resistors for the service port:

Output signals from the service port are open collector signals. These signals must be pulled down to -12v by one and only one module in a Supermax system. Pull down resistors are placed in position DILJ.

Firmware:

The firmware is situated in an EPROM mounted in position D7.

1. DBOOT, V. 0100, 830401.

The DIOC with the this firmware will bootstrap all other modules in a Supermax system from an 8 or from a 5.25 inch floppy disk drive.

Notice: The firmware will not activate the motor on signal in the 5.25 inch floppy disk interface.

2. DCDRONE.

The DIOC with the this firmware will not bootstrap a Supermax system. The DIOC will be able to be bootstraped of another DIOC.

Straps and jumpers:

+ designates factory installed position.

Strap 1.

Function: Real time clock. Position: C 3,2

```
* * * * *
* * * * *
1 2 3 4 5
```

Jumper	Clock
1	1.28 milliseconds
2	6.40 milliseconds
3	12.80 milliseconds
4	64.00 milliseconds
+ 5	128.00 milliseconds

Strap 2.

Function: Baud rate to service port. Connected to both TxClk and RxClk.

Position: B 7,3

```
* * * *
* * * *
1 2 3 4
```

Jumper	Clock
+ 1	9600 x 16 baud.
2	4800 x 16 baud.
3	2400 x 16 baud.
4	1200 x 16 baud.

Strap socket 1.

Function: Possible to connect two swithes. One is able to generate an internal reset pulse and one is able to generate a hardware "TRAP" interrupt to the 8085.

Position: C 4,1.

Factory installed strapsocket:

```
* *_* * * * * *

* *_* * * * * *
1.
```

Testpoints:

Testpoints for adjustment of floppy disk controller.

```
   4
   *
*  *  *
1  2  3
```

PIN

1	TP1	
2	TP2	
3	TP3	
4	TPGND	GND reference point.

Adjustments:

The PPL in the floppy disk interface can be adjusted with multiturn resistor PU1 and PU2. For further details see Supermax technical note no. 1.

Cables and connectors:

The connection between the DIOC module and the disks is made with three flat cable connectors.

The headers mounted on the PCB are positioned as follows:

Winchester disk	:	C 1,8.	50 pin
Floppy disk	:	C 3,8.	50 pin or 34 pin.
Streaming tape	:	C 5,8	50 pin
Service port	:	C 5,3	20 pin

Indicator Leds:

LED1: On: The boot prom is enabled.
Off: The boot prom is disabled.
Upon power up: On

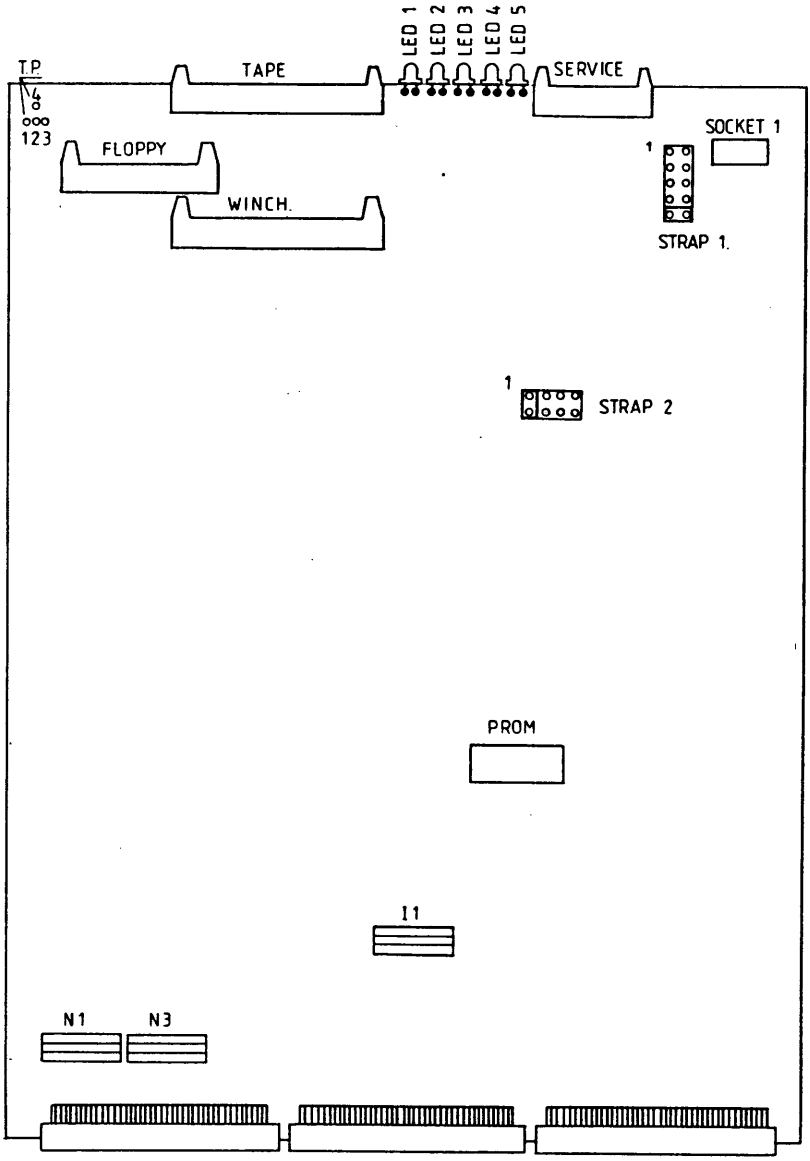
LED2: On: A time out is pending.
Off: No time out.
Upon power up: Off.

LED3: On: A buserror is received.
Off: No buserror.
Upon power up: Off.

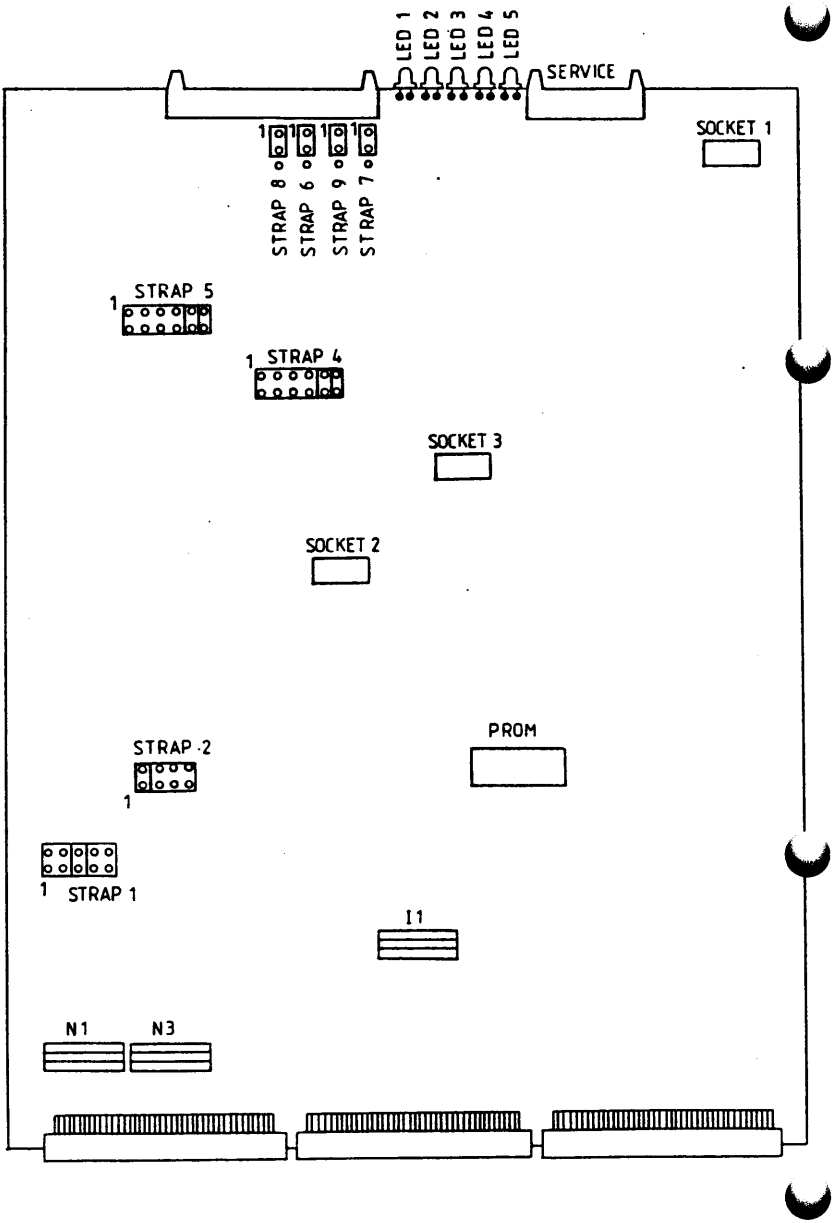
LED4: On: The ERROR line is active. The error line is set by the program or because of a parity error.
Off: No error.
Upon power up: On

LED5: On: The DIOC has activated the buserror signal.
Off: No error.
Upon power up: Off.

SUPERMAX technical data sheet.
Module: DIOC 0400



SUPERMAX technical data sheet.
Module: CIOC 0900



Type: DIOC 1100

Data sheet no.: 8

Revision no.: 0

Date: 851008

General description:

The DIOC is the intelligent Disk IO Controller in a SUPERMAX system. The DIOC is built around a microprocessor and contains the following interfaces:

- floppy disk interface
- streaming tape interface
- winchester disk interface
- 4 seriel RS-232 channels

Interface to I/O bus:

The DIOC has a standard interface to the common SUPERMAX I/O bus. The local memory bus is not used.

Active cycles : Byte read and write.
Dobbelt word read and write.

Passive cycles: Byte read and write.
Word read and write.
Read modify write.

Interface to peripheral equipment:

Winchester disk interface:

The winchester disk interface is the Small Computer System Interface ANSI X3T9.2, SCSI.
The connector is a 50 pin flatcable header. DIN-41651.

PIN	Signal	Signal	PIN
01	GND	-DB(0)	02
03	GND	-DB(1)	04
05	GND	-DB(2)	06
07	GND	-DB(3)	08
09	GND	-DB(4)	10
11	GND	-DB(5)	12
13	GND	-DB(6)	14
15	GND	-DB(7)	16
17	GND	-DB(P)	18
19	GND	GND	20
21	GND	GND	22
23	GND	GND	24
25	open	open	26
27	GND	GND	28
29	GND	GND	30
31	GND	-atn	32
33	GND	GND	34
35	GND	-bsy	36
37	GND	-ack	38
39	GND	-rst	40
41	GND	-msg	42
43	GND	-sel	44
45	GND	-c/d	46
47	GND	-req	48
49	GND	-i/o	50

- designates active low signals.

Streaming tape interface:

The streaming tape interface is Quarter-inch Interchange Committee interface, QIC II.
The connector is a 50 pin flatcable header. DIN-41651.

PIN	Signal	Signal	PIN
01	GND	open	02
03	GND	open	04
05	GND	open	06
07	GND	open	08
09	GND	open	10
11	GND	-DB(7)	12
13	GND	-DB(6)	14
15	GND	-DB(5)	16
17	GND	-DB(4)	18
19	GND	-DB(3)	20
21	GND	-DB(2)	22
23	GND	-DB(1)	24
25	GND	-DB(0)	26
27	GND	-onl	28
29	GND	-req	30
31	GND	-rst	32
33	GND	-tfer	34
35	GND	-ack	36
37	GND	-rdy	38
39	GND	-exc	40
41	GND	-dir	42
43	GND	open	44
45	GND	open	46
47	GND	open	48
49	GND	open	50

- designates active low signals.

Floppy disk drive interface:

The DIOC module is equiped with a 50 pin flatcable header for connection to the floppy disk drives. DIN-41651. The module is strapped for interface to either 8 or 5.25 inch disk drives.

Connector when strapped for 8 inch interface:

PIN	Signal	Signal	PIN
01	GND	-tg43	02
03	GND	open	04
05	GND	open	06
07	GND	open	08
09	GND	open	10
11	GND	open	12
13	GND	side sel	14
15	GND	open	16
17	GND	-head load	18
19	GND	-index	20
21	GND	-ready	22
23	GND	open	24
25	GND	-sel0	26
27	GND	-sel1	28
29	GND	-sel2	30
31	GND	-sel3	32
33	GND	direction	34
35	GND	-step	36
37	GND	-write data	38
39	GND	-write gate	40
41	GND	-track 00	42
43	GND	-write prt	44
45	GND	-read data	46
47	GND	side sel	48
49	GND	open	50

- designates active low signals.

When a 5.25 inch disk drive is used the conncetion between the module and the drive is made with a 34 pin flat cable. The cable is connected to the 50 pin header with pin 34 in the cable connected to pin 50 in the header, see the table.

Connector when strapped for 5.25 inch interface:

PIN	Signal	Signal	PIN	
01	GND	tg43	02	
03	GND	open	04	
05	GND	open	06	
07	GND	open	08	
09	GND	open	10	
11	GND	open	12	
13	GND	side sel	14	Cable:
15	GND	open	16	
17	GND	-head load	18	2
19	GND	-in use	20	4
21	GND	nc	22	6
23	GND	-index	24	8
25	GND	-sel0	26	10
27	GND	-sel1	28	12
29	GND	-sel2	30	14
31	GND	-motor on	32	16
33	GND	direction	34	18
35	GND	-step	36	20
37	GND	-write data	38	22
39	GND	-write gate	40	24
41	GND	-track 00	42	26
43	GND	-write prt	44	28
45	GND	-read data	46	30
47	GND	side sel	48	32
49	GND	-ready	50	34

- designates active low signals.

Serial channels:
The four serial channels are RS-232 compatible. The connector is a 34 pin flatcable header. DIN-41651.

PIN	Signal	Signal	PIN
01	TxD0	RTS0	02
03	GND	DTR0	04
05	RxD0	CTS0	06
07	GND	DSR0	08
09	TxD1	RTS1	10
11	GND	DTR1	12
13	RxD1	CTS1	14
15	GND	DSR1	16
17	TxD2	RTS2	18
19	GND	DTR2	20
21	RxD2	CTS2	22
23	GND	DSR2	24
25	TxD3	RTS3	26
27	GND	DTR3	28
29	RxD3	CTS3	30
31	GND	DSR3	32
33	+12V	-12V	34

Line receivers and transmitters:

	Receiver	Transmitter
Channel 0:	D5	D4
Channel 1:	D5,D7	D4,D6
Channel 2:	D7,D9	D6,D8
Channel 3:	D9	D8

Receiver type : TI 75189 or MC1489
Transmitter type: TI 75188 or MC1488

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

Power requirements:

Voltage		Typ. current
+ 5	+-5%	9.5 A
+12	+-5%	0.1 A
-12	+-5%	0.1 A

Physical dimension:

Standard SUPERMAX module.

Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a DIOC module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Straps.
- Flat cables for the disks.

These items are described in details in the following text.

Unit number/priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. The address is called the unit number.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot used the same priority. The DIOC module use two priorities. The DIOC module is equiped with a unit number switch. The switch gives the module a unit number and two priorities. The priorities are compatible with priority PALs marked PxyO.

Basic DIOC module:

Supermax systems are delivered with one basic DIOC module. The basic module differs from the standard module on the following points:

The unit number is fixed to number 14.

The priorities are fixed to 41 and 42.

Switch position	Unit number	Priority 1	Priority 0
0	0x00	14	20
1	0x01	21	22
2	0x02	23	24
3	0x03	30	31
4	0x04	32	33
5	0x05	34	40
6	0x06	41	42
7	0x07	43	44
8	0x08	14	20
9	0x09	21	22
A	0x0a	23	24
B	0x0b	30	31
C	0x0c	32	33
D	0x0d	34	40
E	0x0e	41	42
F	0x0f	43	44

Straps and jumpers:

+ designates factory installed position.

Strap 1.

Function: Real time clock. Position: C 3,2

```
* * * *
* * * *
1 2 3 4
```

Jumper	Clock
1	10.0 milliseconds
2	20.0 milliseconds
3	40.0 milliseconds
+ 4	80.0 milliseconds

Strap 2.

Function: Baud rate to service port. Connected to both TxClk and RxClk.

Position: B 7,3

```
* * * * * * * *
* * * * * * * *
1 2 3 4 5 6 7 8
```

Jumper	Clock
+ 1	9600 x 16 baud.
2	4800 x 16 baud.
3	2400 x 16 baud.
4	1200 x 16 baud.
5	600 x 16 baud.

6	300 x 16 baud.
7	150 x 16 baud.
8	75 x 16 baud.

Strap 3.

Function: Use of the RS-232-C "open collector" service port.

Position: C 3,2

```
  *  *  *
  *  *  *
  1  2  3
```

Jumper 1-3	Function
installed	RS-232-C interface
+ open	Open collector RS-232-C

Strap 4.

Function: Choice of 8 inch or 5.25 inch floppy interface.

Position: C 3,2

8 inch floppy disk interface:

```
    1 *] *] *] *] *] *] *] *]
    2 *] *] *] *] *] *] *] *]
  + 3 *  *  *  *  *  *  *  *
```

5.25 inch floppy disk interface:

```
    1 *  *  *  *  *  *  *  *
    2 *] *] *] *] *] *] *] *]
    3 *] *] *] *] *] *] *] *]
```

Strap 5.

Function: Adjustment of floppy disk controller.

Position: C 3,2

Jumper	Function
mounted	Adjustment.
+ open	Normal use.

Strap 6.

Testpoints for adjustment of floppy disk controller.

```
* * * * *
1 2 3 4 5
```

PIN

1	GND
2	WD
3	TG43
4	DIRC
5	GND

Strap 7.

Function: EPROM size.

Position: A 11,3

```
* * *
1 2 3
```

Jumper	Function
+ 1-2	EPROM 2764-3 or 27128-3.
2-3	EPROM 27256-3.

Cables and connectors:

The connection between the DIOC module and the disks and serial channels is made with four flat cable connectors.

The headers mounted on the PCB are positioned as follows:

Winchester disk	:	C 5,7.	50 pin
Floppy disk	:	C 4,7.	50 pin
Streaming tape	:	C 3,7.	50 pin
Seriel interface	:	C 5,4	34 pin
Service port	:	C 5,2	20 pin

Adjustments:

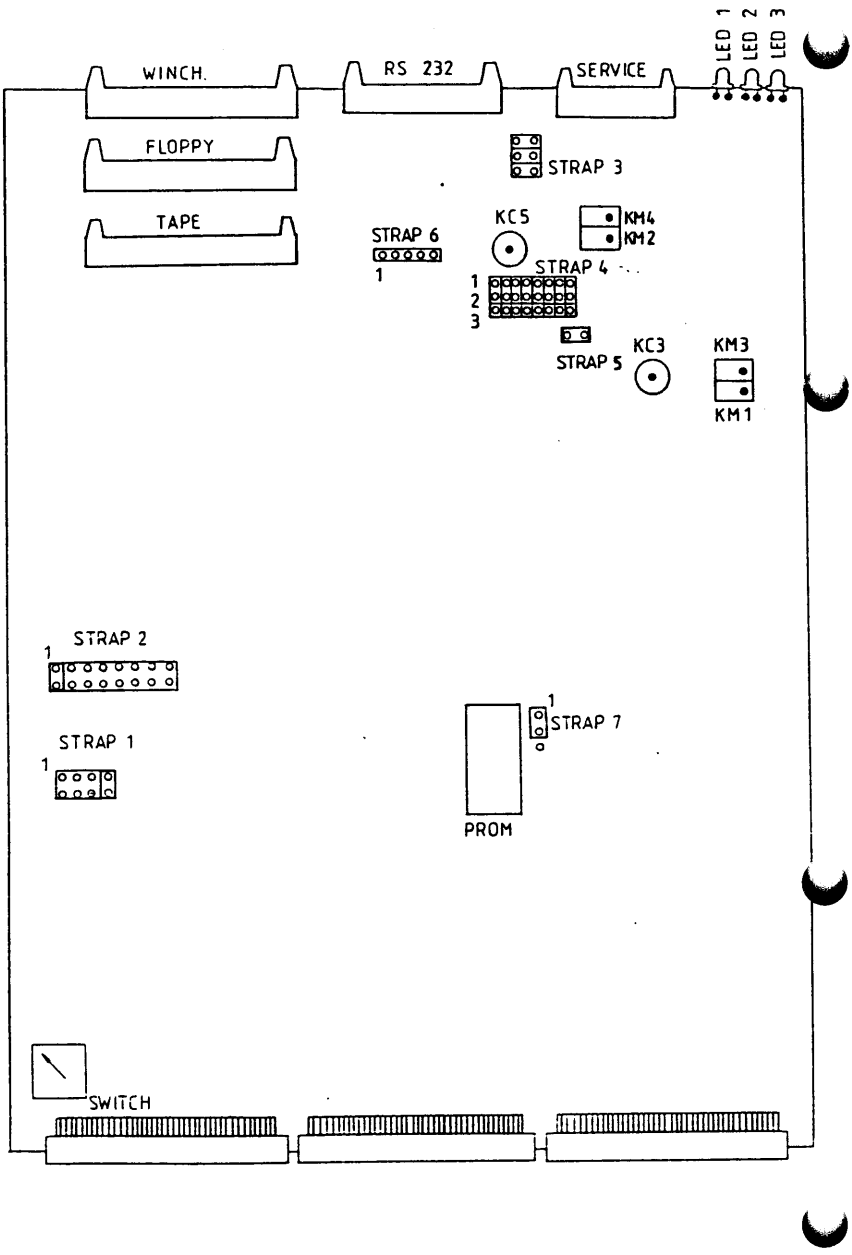
Adjustment of PPL in the floppy interface see supermax technical note 3, revision 1.

Indicator LEDs.

LED1: Off: No error. Upon power up.
On: DIOC program loaded. Waiting for first command.

LED2: Off: No error. Upon power up.
On: Hard error on disk during bootstrap.

LED3: Off: Selftest completed.
On: Upon power up reset.


LED 1
LED 2
LED 3
WINCH.
RS 232
SERVICE
FLOPPY
TAPE
STRAP 3
KC5
KM4
KM2
STRAP 6
1
STRAP 4
1
2
3
STRAP 5
KC3
KM3
KM1
STRAP 2
1
STRAP 1
1
1
STRAP 7
PROM
SWITCH

Supermax technical data sheet.
Module: DIOC 4000

Type: DIOC 4000

Data sheet no.: 17

Revision no.: 0

Date: 880916

General description:

The DIOC is a high performance Disk IO Controller for the Supermax system. The DIOC is built around a 32 bit microprocessor and contains two Small Computer Standard Interfaces, SCSI, and 4 or 8 Mbyte disk cache memory.

Architecture:

The DIOC is based on a 20 MHz Motorola 68020 processor. The memory system consists of three parts.

1. 1 Mbyte high speed local DRAM with byte parity for the MC68020 program and data. The organisation is 256k by 36 bit.

2. 4 Mbyte high speed multiport DRAM with byte parity used as disk cache and data buffer. The organisation is 1M by 36 bit.

3. Additional 4 Mbyte high speed multiport DRAM with byte parity used as disk cache. The organisation is 1M by 36 bit.

Two fully independent DMA channels transfer data between the SCSI interfaces and the disk cache memory. The SCSI ports are 8 bit wide and data are packed to 32 bit words before data are transferred through a pipeline to and from the disk cache memory.

Data are transferred between the disk cache memory and the main memory modules with a Block Transfer Unit, BTU. The BTU is a device used to move blocks of data. Data are transferred through a pipeline in 32 bit words and the BTU uses single word or burst transfers on the Supermax I/O bus. Burst transfers are used for high speed and small I/O bus load.

The DIOC contains firmware for bootstrapping, selftest and diagnostics.

Interface to I/O bus:

The DIOC has a standard interface to the common Supermax I/O bus. The local memory bus is not used.

Active cycles : Byte (8 bit) read and write.
Word (16 bit) read and write.
Double word (32 bit) read and write.
Read modify write.

Passive cycles: Byte read and write.
Word read and write.
Double word read and write.
Read modify write.

Interface to peripheral equipment:

The interface is the Small Computer Standard Interface ANSI X3T9.2, SCSI. The interfaces are based on a VLSI design and supports the optional features like arbitration, disconnect, reconnect and parity.

The two connectors are 50 pin flatcable headers. DIN-41651.

PIN	Signal	Signal	PIN
01	GND	-DB(0)	02
03	GND	-DB(1)	04
05	GND	-DB(2)	06
07	GND	-DB(3)	08
09	GND	-DB(4)	10
11	GND	-DB(5)	12
13	GND	-DB(6)	14
15	GND	-DB(7)	16
17	GND	-DB(P)	18
19	GND	GND	20
21	GND	GND	22
23	GND	GND	24
25	GND	TPOW	26
27	GND	GND	28
29	GND	GND	30
31	GND	-atn	32
33	GND	GND	34
35	GND	-bsy	36
37	GND	-ack	38
39	GND	-rst	40
41	GND	-msg	42
43	GND	-sel	44
45	GND	-c/d	46
47	GND	-req	48
49	GND	-i/o	50

- designates active low signals.

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units in a Supermax system.

Power requirements:

Voltage		Typ. current
+ 5	+-5%	15.0 A
+12	+-5%	0.1 A
-12	+-5%	0.1 A

Physical dimension:

Standard Supermax module.

Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a DIOC module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Straps.
- Flat cables for the interfaces.

These items are described in details in the following text.

Unit number/priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. The address is called the unit number.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot use the same priority. The DIOC module uses two priorities. The DIOC module is equiped with a unit number switch. The switch gives the module a unit number and two priorities. The priorities are compatible with priority PALs marked PxyO.

Switch position	Unit number	Priority 1	Priority 0
0	0x00	14	20
1	0x01	21	22
2	0x02	23	24
3	0x03	30	31
4	0x04	32	33
5	0x05	34	40
6	0x06	41	42
7	0x07	43	44
8	0x08	14	20
9	0x09	21	22
A	0x0a	23	24
B	0x0b	30	31
C	0x0c	32	33
D	0x0d	34	40
E	0x0e	41	42
F	0x0f	43	44

Straps and jumpers:

+ designates factory installed position.

Strap 1.

Function: Baud rate to service port. Connected to both TxClk and RxClk.
Name : ST2
Position: L-12

```
* * * * * * *
* * * * * * *
1 2 3 4 5 6 7
```

Jumper	Clock
1	19200 baud.
+ 2	9600 baud.
3	4800 baud.
4	2400 baud.
5	1200 baud.
6	600 baud.
7	300 baud.

Strap 2.

Function: MC68020 internal cache disable.
Name : ST3
Position: H-6

Jumper	Function
installed	Cache disable.
+ open	Cache enable.

Strap 3.

Function: Termination power to SCSI interface connector CN1.
Name : ST8
Position: C-14

```
  *  *  *
  1  2  3
```

Jumper	Function
1-2	No termination power.
+ 2-3	Termination power to the cable.

Strap 4.

Function: Termination power to SCSI interface connector CN3.
Name : ST10
Position: C-14

```
  *  *  *
  1  2  3
```

Jumper	Function
1-2	No termination power.
+ 2-3	Termination power to the cable.

Cables and connectors:

The headers mounted on the PCB are positioned as follows:

SCSI interface 0 :
Connector name CN1, position C-16.

SCSI interface 1 :
Connector name CN3, position C-14.

Service port
Connector name CONJ4, position K-16.

Indicator LEDs.

LED1, position M-16.

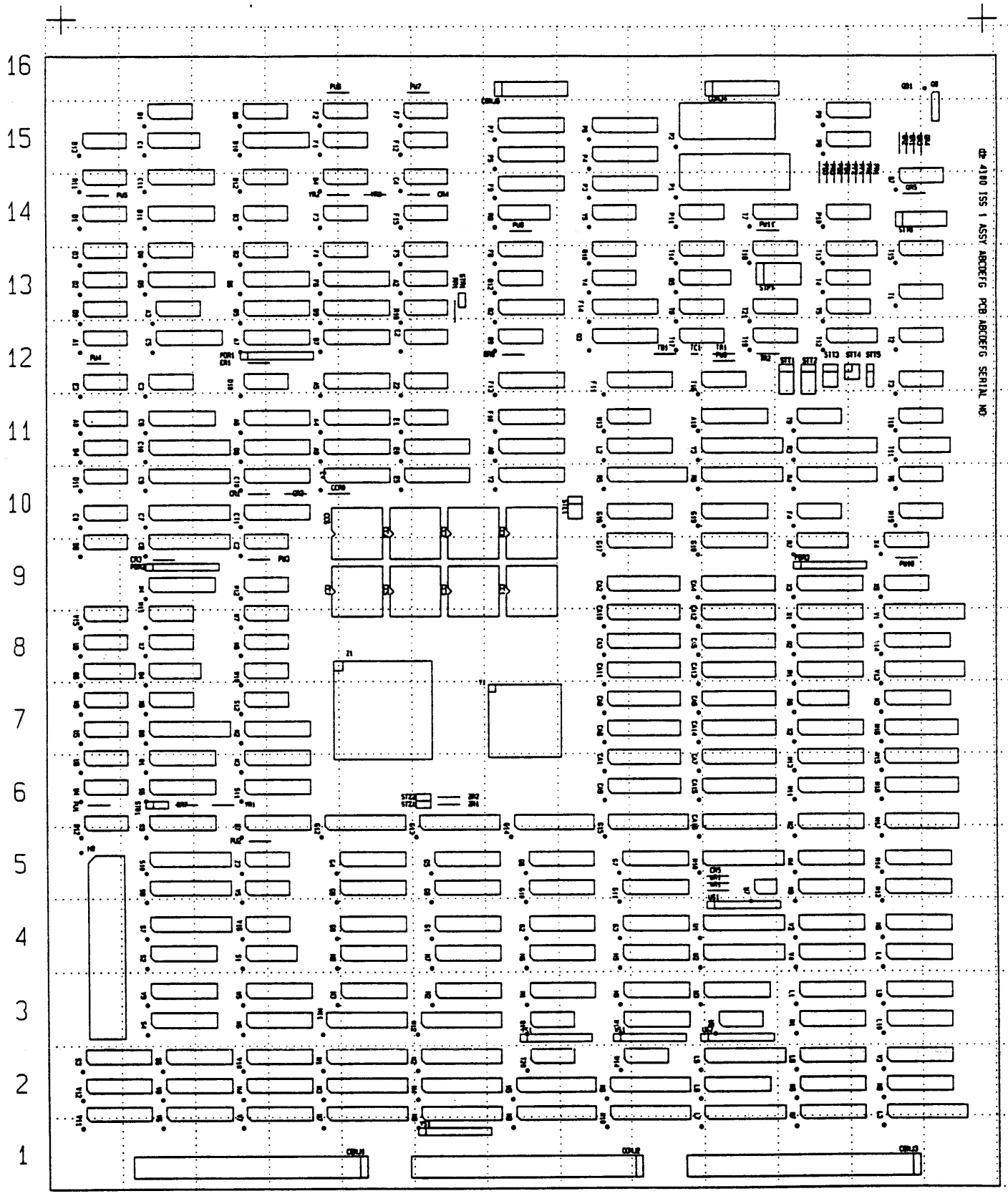
Off: No error.
On: Parity error in program memory.

LED2, position M-16.

Off: The processor is halted.
On: The processor is running.

LED3, position M-16.

Off: No error.
On: The program has detected a fault condition.



	dansk data elektronik a/s	
Issue	Date	dde 4100
0	880312	
1	880617	Component-ID
2		
3		
4		Parts no.
5		Dwg. no.

PRELIMINARY

Name	Type	Pos
A0	74F74	A11
A1	74F74	A12
A2	74F74	E13
A3	74AS04	B13
A4	74AS573	D11
A5	74AS573	D12
A6	C3240	C11
A7	C3200	C12
A8	C3233	G11
A9	C3210	D11
A10	C3220	J11
B0	74F74	C15
B1	74F74	B15
B2	74F74	C13
B3	74AS04	C14
B4	74F74	D14
B5	74AS573	C13
B6	74AS573	C13
B7	C3280	D12
B8	C3290	B7
B9	C3252	D13
B10	C3262	C15
B11	C3271	B14
B12	74AS02	C14
B13	74AS08	A15
CA0	HM6788HP-15	H7
CA1	HM6788HP-15	H6
CA2	HM6788HP-15	H9
CA3	HM6788HP-15	H8
CA4	HM6788HP-15	J9
CA5	HM6788HP-15	J8
CA6	HM6788HP-15	J7
CA7	HM6788HP-15	J6
CA8	HM6788HP-15	H7
CA9	HM6788HP-15	H6
CA10	HM6788HP-15	H8
CA11	HM6788HP-15	H8
CA12	HM6788HP-15	J8
CA13	HM6788HP-15	J8
CA14	HM6788HP-15	J7
CA15	HM6788HP-15	J6
CA16	HM6788HP-15	J5
CCR0	res270	D10
CC0	TACT2152-25	G10
CC1	TACT2152-25	G9
CC2	TACT2152-25	F10
CC3	TACT2152-25	F9
CC4	TACT2152-25	E10
CC5	TACT2152-25	E9
CC6	TACT2152-25	E10
CC7	TACT2152-25	E9
CONJ1	DIN96	E1
CONJ2	DIN96	J1
CONJ3	DIN96	M1
CONJ4	3M20	K16
CONJ5	3M20	G16
CR1	NOT USED	C10
CR2	NOT USED	D10
CR3	res270	B9
CR4	res330	E14
CR5	res1K	J5
CT0	C3301	C10
CT1	C3311	C10
C0	74F74	A10
C1	74S112	B15
C2	74AS04	C9
C3	74AS04	B12
C4	74LS14	E14
C5	C3390	B12
C6	C3400	B11
C7	C3410	B10
C8	C3420	B9
C9	C3430	B10
C10	C3440	B11
C11	C3380	B14
D0	74F74	B13
D1	74F74	A14
D2	74F74	A13

Name	Type	Pos
D3	74F74	A13
D4	74F74	A11
D5	C3320	B13
D6	C3330	C11
D7	C3340	C5
D8	74AS08	A9
D9	74AS00	A13
D10	74AS11	C12
D11	74AS20	A10
D12	74AS00	A5
ER1	res270	C12
E0	74FCT573	E11
E1	74AS32	E11
E2	74AS32	E12
E3	74AS30	A12
E4	C3360	D10
E5	C3351	E10
F0	74F74	D13
F1	74F74	D15
F2	74F74	D15
F3	74AS08	D14
F4	74AS10	L10
F5	74AS30	E13
F6	C3371	D13
F7	74F74	E15
F8	74F74	G13
F9	74ALS573	G14
F10	74LS273	G11
F11	74LS273	H12
F12	74F74	E15
F13	74ALS573	G12
F14	74ALS573	H13
F15	74F74	E14
G0	74AS645	D4
G1	74AS645	F4
G2	74AS645	G4
G3	74AS645	H4
G4	74AS574	D5
G5	74AS574	F5
G6	74AS574	G5
G7	74AS574	H5
G8	74AS574	D5
G9	74AS574	F5
G10	74AS574	G5
G11	74AS574	H5
G12	74FCT646	D5
G13	74FCT646	F5
G14	74FCT646	G5
G15	74FCT646	H5
G16	74FCT573	H10
G17	74FCT573	H9
G18	74FCT573	J9
G19	74FCT573	J10
H0	74AS574	H3
H1	74AS574	G3
H2	74AS574	F3
H3	74AS574	D3
H4	74ALS574	C2
H5	74AS573	H4
H6	74AS573	G4
H7	74AS573	F4
H8	74AS573	D4
H9	74AS632	A5
LABEL		O-1
L1	74ALS574	L3
L2	74ALS573	H11
L3	74ALS873	M1
L4	74ALS573	M4
L5	TMM2018D-25	J2
L6	74ALS645	J2
L7	74ALS873	J1
L8	74ALS573	L2
L9	74ALS573	M3
L10	74ALS573	M3
M1	74ALS573	L3
M2	74ALS573	L5
M3	74ALS573	M7
M4	74ALS573	L5

Name	Type	Pos
M5	74ALS573	L2
M6	74ALS573	M4
M7	74ALS573	L1
M8	74ALS573	M2
M9	74ALS573	L5
M10	74ALS873	J5
M11	74ALS645	L6
M12	74ALS645	M5
M13	74ALS573	L6
M14	74ALS573	M5
M15	SSM7188-25	M6
M16	SSM7188-25	M7
M17	SSM7188-25	M5
M18	SSM7188-25	M6
M19	74AS00	M10
N1	74ALS646	D2
N2	74ALS646	F2
N3	74ALS646	D2
N4	74ALS646	F2
N5	74ALS646	G2
N6	74ALS646	H2
N7	74ALS646	D1
N8	74ALS646	F1
N9	74ALS646	G1
N10	74ALS646	H1
N11	74ALS646	D3
N12	74ALS646	F3
PDR1	res10x-1-101	C12
PDR2	res10x-1-101	B9
PDR3	res10x-1-101	L9
PDR4	NOT USED	J14
PDR5	NOT USED	B9
PDR6	NOT USED	A11
PDR7	NOT USED	D8
PDR8	NOT USED	N9
PD1	4148	L15
PD2	4148	L15
PD3	4148	L15
PF1	Micro fuse 0.5A	M15
PF2	Micro fuse 0.5A	L15
PR1	res4k7	M15
PR2	res4k7	M15
PR3	res4k7	L15
PU1	res1k	A6
PU2	res1k	C5
PU3	res1k	C9
PU4	res1k	A12
PU5	res1k	A14
PU6	res1k	D16
PU7	res1k	E16
PU8	res1k	G14
PU9	res1k	K12
PU10	res1k	M9
PU11	res1k	K14
PU12	res150	K14
PU13	res150	A9
PU14	res150	A11
PU15	res150	D8
PU16	res150	M9
PU17	res1k	D8
PU18	res1k	D8
P1	27C512-15	J14
P2	8251A	J15
P3	74ALS645	H14
P4	74ALS574	H15
P5	74ALS574	G15
P6	74LS641-1	H15
P7	74LS641-1	G15
P8	75188	L15
P9	75189A	L15
P10	dipswitch14pin	L14
P11	74AS1004	J14
QD1	red-led	M16
QR1	res150	M15
QR2	res4k7	M15
QR3	res4k7	M15
QR4	res1k	M15
QR5	res1k	N15

Component locations

PCB: 4101 / 68030 | Issue: 0 | Date: 881021

dde

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PRELIMINARY

Name	Type	Pos
QR6	res1k	G12
QR7	res4k7	B6
Q1	74ALS580	B6
Q2	74ALS573	G13
Q3	74ALS574	H12
Q4	74LS148	B8
Q5	74LS353	J13
Q6	74S175	A8
Q7	74S38	M14
Q8	debugswitch	N16
Q9	74S38	G12
Q10	74S38	H13
Q11	74LS14	G3
Q12	74F74	G13
RR1	res10k	F13
R1	C3070	L8
R2	C3080	L8
R3	C3100	L11
R4	C3000	L10
R5	C3090	H10
R6	C3190	J10
R7	74ALS138	L9
R8	74ALS138	L7
R9	74ALS138	G14
R10	74AS21	E13
R11	74AS04	A14
STE1	JUMPER (2x3)	H10
STP1	JUMPER (3x6)	K13
STQ1	JUMPER (1x3)	B6
STR1	JUMPER (1x2)	F13
STT1	JUMPER (2x4)	L12
STT2	JUMPER (2x4)	L12
STT3	JUMPER (2x4)	L12
STT4	JUMPER (2x2)	L12
STT5	JUMPER (1x3)	M12
STT6	JUMPER (2x7)	M14
STT7	JUMPER (2x8)	M14
STT8	JUMPER (1x3)	H10
STZ1	JUMPER (2x2)	F6
STZ2	JUMPER	F6
S1	74LS590	C4
S2	74ALS574	B4
S3	74ALS573	A2
S4	74ALS573	B3
S5	74ALS573	B6
S6	C3110	B2
S7	TMM2018D-25	B4
S8	C3150	B5
S9	C3131	B5
S10	C3140	B5
S11	C3121	C6
S12	74AS04	C7
TC1	10uF/25V (Tantal)	J12
TD1	4148	J12
TR1	res100k	K12
TR2	res1k	K12
TS1	res10x-1-103	G3
T1	OSC-66.667Mhz	M13
T2	osc50M	M12
T3	osc40M	M12
T4	74F74	L13
T5	74F74	L13
T6	74F74	M10
T7	74F74	K14
T8	74AS1004	J13
T9	74AS1004	L11
T10	74S140	M11
T11	74LS390	M11
T12	74LS390	L12
T13	74LS390	L13
T14	74LS393	J13
T15	74LS393	M13
T16	74F74	J12
T17	74LS14	J12
T18	74LS74	K13
T19	74S05	K12
T20	dipswitch	G2
T21	74AS32	K13

Name	Type	Pos
UR1	res1k	J5
US1	res10x-1-103	K4
US2	res10x-1-151	J3
U1	UPXX	J4
U2	PPAX	J4
U3	74AS641	J3
U4	74F74	A6
U5	74F74	A7
U6	dipswitch14pin	K3
U7	hexswitch	K5
U8	74AS32	A6
U9	74AS74	A8
VS1	res10x-1-102	F1
V1	74ALS873	M8
V2	74ALS573	L4
V3	74ALS573	M2
V4	74ALS573	L4
V5	74F74	C5
V6	74ALS574	B1
V7	74ALS645	C1
V8	74ALS645	B2
V9	74ALS645	B3
V10	74ALS645	C2
V11	74ALS645	A1
V12	74ALS573	A2
V13	74AS873	M8
V14	C3181	M8
V15	74AS08	A8
V16	74AS04	C4
WR1	res100	J5
WS1	res10x-1-151	H3
W1	74LS541	H3
W2	74ALS573	C7
W3	C3060	C6
W4	C3170	B9
W5	C3160	C3
W6	74S240	C3
W7	74F74	C8
W8	74F74	C8
W9	74F74	A7
W10	74AS00	C8
W11	74AS08	B8
W12	74AS32	C9
W13	74S38	H11
W14	dipswitch14pin	H2
X1	C3010	L8
X2	C3020	L7
X3	C3032	L9
X4	74F74	M9
X5	74AS02	M9
X6	74AS04	B7
X7	74AS08	B8
YR1	res10k	C6
YR2	res2k2	D14
YR3	res2k2	E14
Y1	MC68882-25	G7
Y2	C3040	G10
Y3	C3050	J11
Y4	74F74	H13
Y5	74AS08	H14
ZR1	res10k	F6
ZR2	res10k	F6
Z1	MC68030RC-33	D8
Z2	74AS04	E12
Z3	74AS08	C5

Name	Type	Pos

Component locations

PCB: 4101 / 68030 | Issue: 0 | Date: 881021

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PRELIMINARY

Name	Type	Pos
A1	74ALS574	A4
A2	74LS461	L5
A3	74LS461	J1
A4	74LS461	L1
A5	74LS461	M1
A6	74LS593	G3
A7	74LS593	K3
A8	74LS593	L3
A9	74LS593	M3
A10	74ALS646	D2
A11	74ALS646	E2
A12	74ALS646	G2
A13	74ALS646	H2
A14	74ALS646	D2
A15	74ALS646	E2
A16	74ALS646	G2
A17	74ALS646	H2
A18	74LS32	G6
A19	74LS08	B2
A20	74LS32	G6
B1	74LS461	J2
B2	74LS461	L2
B3	74LS461	M2
B4	74LS461	J2
B5	74LS461	L2
B6	74LS461	M2
B7	74LS461	J2
B8	74LS461	L2
B9	74LS461	M2
B10	74LS461	J3
B11	74LS461	L3
B12	74LS461	M3
CN1	3M50	C16
CN2	NOT USED	C15
CN3	3M50	C14
CN5	3M34	G16
CONJ1	DIN C96	E1
CONJ2	DIN C96	J1
CONJ3	DIN C96	M1
CONJ4	3M20	K16
CS1	NOT USED	B14
CT1	NOT USED	J14
CT2	NOT USED	J14
C1	74ALS573	K4
C2	74ALS573	L4
C3	74ALS573	M4
C4	74ALS573	K4
C5	74ALS573	L4
C6	74ALS573	M4
C7	74ALS873	L8
C8	74ALS573	M8
C9	74ALS645	M10
C10	74ALS645	M6
C11	74ALS873	L7
C12	74ALS573	M6
C13	74ALS873	L7
C14	74AS573	M5
C15	74LS590	M8
C16	74LS590	M7
C17	74AS573	M5
C18	SDT6116SA35TP	L6
C19	SDT6116SA35TP	L6
C20	74AS32	K10
C21	74AS32	K6
C22	74F74	K10
DQ1	1N4148	K16
DQ2	1N4148	K15
DQ3	1N4148	M15
DS1	NOT USED	C14
DS2	1N4002	D13
DS3	1N4002	C14
DS53	1N4002	C14
D1	74ALS574	L6
D2	74ALS573	L5
D3	74ALS573	K4
D4	74ALS573	L4
D5	74ALS573	M4
D6	74ALS646	D3

Name	Type	Pos
D7	74ALS646	E3
D8	74ALS646	G3
D9	74ALS646	H3
D10	74ALS645	D1
D11	74ALS645	F1
D12	74ALS645	G1
D13	74ALS645	H1
D14	74ALS645	D3
D15	74ALS645	F3
D16	74ALS646	D2
D17	74ALS646	E2
D18	74ALS646	G2
D19	74ALS646	H2
D20	mc68020	H7
D21	74ALS573	M6
D22	74AS04	B6
EC12	220nfdip	E5
EC13	220nfdip	E5
EC14	220nfdip	F5
EC15	220nfdip	F5
EC16	220nfdip	G5
EC17	220nfdip	G5
EC18	220nfdip	H5
EC19	220nfdip	J5
EC20	220nfdip	H5
EC21	220nfdip	G5
EC22	220nfdip	E5
EC23	220nfdip	D5
E1	74LS590	G5
E2	74LS590	G5
E3	74ALS244	K5
E4	74ALS244	K6
E5	74ALS244	K5
E7	74AS280	D5
E8	74AS280	D5
E9	74AS280	F5
E10	74AS280	F5
E11	74AS08	D6
E12	81C256-10	J4
E13	81C256-10	H4
E14	81C256-10	H4
E15	81C256-10	G4
E16	81C256-10	F4
E17	81C256-10	F4
E18	81C256-10	E4
E19	81C256-10	E4
E20	81C256-10	H4
E21	81C256-10	G4
E22	81C256-10	F4
E23	81C256-10	D4
E61	SIL 10-2-330	J5
E62	SIL 10-2-330	J5
E241	SIL 10-2-330	J5
E242	SIL 10-2-330	J5
FRP0	81C1000-12PSZ	C11
FRP1	81C1000-12PSZ	C9
FRP2	81C1000-12PSZ	A11
FRP3	81C1000-12PSZ	A9
FR0	81C1000-12PSZ	C11
FR1	81C1000-12PSZ	C11
FR2	81C1000-12PSZ	C11
FR3	81C1000-12PSZ	C10
FR4	81C1000-12PSZ	C10
FR5	81C1000-12PSZ	C10
FR6	81C1000-12PSZ	C10
FR7	81C1000-12PSZ	C10
FR8	81C1000-12PSZ	C9
FR9	81C1000-12PSZ	C9
FR10	81C1000-12PSZ	C9
FR11	81C1000-12PSZ	C9
FR12	81C1000-12PSZ	C8
FR13	81C1000-12PSZ	C8
FR14	81C1000-12PSZ	C8
FR15	81C1000-12PSZ	C8
FR16	81C1000-12PSZ	A11
FR17	81C1000-12PSZ	A11
FR18	81C1000-12PSZ	A11
FR19	81C1000-12PSZ	A10

Name	Type	Pos
FR20	81C1000-12PSZ	A10
FR21	81C1000-12PSZ	A10
FR22	81C1000-12PSZ	A10
FR23	81C1000-12PSZ	A10
FR24	81C1000-12PSZ	A9
FR25	81C1000-12PSZ	A9
FR26	81C1000-12PSZ	A9
FR27	81C1000-12PSZ	A9
FR28	81C1000-12PSZ	A8
FR29	81C1000-12PSZ	A8
FR30	81C1000-12PSZ	A8
FR31	81C1000-12PSZ	A8
FUSEM	MICROFUSE	L16
FUSEP	MICROFUSE	L15
F1	74AS244	A6
F2	74AS244	C7
F3	74AS244	A7
F4	74AS32	C6
F5	74AS32	A6
F10	74AS08	B6
F11	74AS280	G7
F12	74AS280	G7
F13	74AS280	F7
F14	74AS280	F7
F61	SIL 10-2-330	C8
F62	SIL 10-2-330	C8
F71	SIL 10-2-330	A8
F72	SIL 10-2-330	A8
F81	SIL 10-2-330	C7
F91	SIL 10-2-330	A7
GRP0	81C1000-12PSZ	D11
GRP1	81C1000-12PSZ	D9
GRP2	81C1000-12PSZ	B11
GRP3	81C1000-12PSZ	B9
GR0	81C1000-12PSZ	D11
GR1	81C1000-12PSZ	D11
GR2	81C1000-12PSZ	D11
GR3	81C1000-12PSZ	D10
GR4	81C1000-12PSZ	D10
GR5	81C1000-12PSZ	D10
GR6	81C1000-12PSZ	D10
GR7	81C1000-12PSZ	D10
GR8	81C1000-12PSZ	D9
GR9	81C1000-12PSZ	D9
GR10	81C1000-12PSZ	D9
GR11	81C1000-12PSZ	D9
GR12	81C1000-12PSZ	D8
GR13	81C1000-12PSZ	D8
GR14	81C1000-12PSZ	D8
GR15	81C1000-12PSZ	D8
GR16	81C1000-12PSZ	B11
GR17	81C1000-12PSZ	B11
GR18	81C1000-12PSZ	B11
GR19	81C1000-12PSZ	B10
GR20	81C1000-12PSZ	B10
GR21	81C1000-12PSZ	B10
GR22	81C1000-12PSZ	B10
GR23	81C1000-12PSZ	B10
GR24	81C1000-12PSZ	B9
GR25	81C1000-12PSZ	B9
GR26	81C1000-12PSZ	B9
GR27	81C1000-12PSZ	B9
GR28	81C1000-12PSZ	B8
GR29	81C1000-12PSZ	B8
GR30	81C1000-12PSZ	B8
GR31	81C1000-12PSZ	B8
G1	74AS244	B6
G2	74AS244	D7
G3	74AS244	B7
G4	74AS32	D6
G5	74AS32	C6
G61	SIL 10-2-330	D8
G62	SIL 10-2-330	D8
G71	SIL 10-2-330	B8
G72	SIL 10-2-330	B8
G81	SIL 10-2-330	D7
G91	SIL 10-2-330	B7
H1	UPXX	C1

Component locations

PCB: 4000 / DIOC3 | Issue: 1 | Date: 880112

dansk data elektronik a/s
herlev hovedgade 199. 2730 herlev. tlf. 02-84 50 11

Type: NIOC 1600

Data sheet no.: 9

Revision no.: 0

Date: 860827

General description:

The NIOC 1600 is an intelligent Local Area Network Controller in a SUPERMAX system. The NIOC is built around a MC68000 microprocessor and contains the following IO interfaces:

- Ethernet interface. IEEE 802.3.
- 8 asynchrounous serial RS-232 interfaces.
- Parallel printer interface.
- Service port interface.

Interface to I/O bus:

The NIOC has a standard interface to the common SUPERMAX I/O bus.

Active cycles : Byte read and write.
Word read and write.
Read modify write.

Passive cycles: Byte read and write.
Word read and write.
Double word read and write.
Read modify write.

Ethernet interface.

The NIOC contains the Ethernet transceiver interface. The transceiver cable is connected to a 16 pin flat cable connector CN3.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01		GND	02
03	C-	C+	04
05	TX-	TX+	06
07	GND	GND	08
09	RX-	RX+	10
11	+12 V	GND	12
13	GND		14
15			16

RS-232 Channels.

The serial interface includes the following programmable options:

- Baudrates from 50 to 38400 baud.
- Character length from 5 to 8 bits.
- Odd, even or no parity.
- 1, 1.5 or 2 stop bits.

All RS-232 interface signals are connected to a 60 pin flat cable connector CN1.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01		GND	02
03		GND	04
05	DTR7	DSR7	06
07	CTS7	RTS7	08
09	RXD7	TXD7	10
11			12
13	DTR6	DSR6	14
15	CTS6	RTS6	16
17	RXD6	TXD6	18
19	GND	GND	20
21	GND	+12V	22
23	GND	-12V	24
25	DTR5	DSR5	26
27	CTS5	RTS5	28
29	RXD5	TXD5	30
31	DSR4	DTR4	32
33	RTS4	CTS4	34
35	TXD4	RXD4	36
37	RTS3	DTR3	38
39	TXD3	DSR3	40
41	DSR2	CTS3	42
43	RTS2	RXD3	44
45	TXD0	DTR2	46
47	RXD0	CTS2	48
49	RTS0	RTS1	50
51	CTS0	CTS1	52
53	DSR0	DSR1	54
55	DTR0	DTR1	56
57	TXD1	TXD2	58
59	RXD1	RXD2	60

Parallel Printer Interface.

The NIOC contains an interface to a parallel printer. The interface is located in a 20 pin flat cable connector CN2. Polarity of handshake signals is selected by straps on the NIOC.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	ACK	GND	02
03	DATA(0)	STROBE	04
05	DATA(1)	GND	06
07	DATA(2)	GND	08
09	DATA(3)	GND	10
11	DATA(4)	GND	12
13	DATA(5)	GND	14
15	DATA(6)	GND	16
17	DATA(7)	GND	18
19	BUSY	GND	20

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

The interface to the service port is located in a 20 pin flat cable connector CN0.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	GND		02
03	TXD		04
05	RXD		06
07	RTS		08
09	CTS		10
11	DSR		12
13	GND	DTR	14
15			16
17			18
19			20

Power requirements:

Voltage		Typ. current
+ 5	+-5%	9.0 A
+12	+-5%	0.7 A
-12	+-5%	0.2 A

Physical dimension:

Standard SUPERMAX module.

Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a NIOC module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Straps.
- Pull down resistors for the service port.
- Transceiver cable.
- Flat cables for the serial channels and the parallel printer.
- Firmware.

These items are described in details in the following text.

Unit number/Priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. The address is called the unit number.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot used the same priority. The NIOC module uses one priority. The NIOC module is equiped with a unit number switch, SWU. The switch gives the module a unit number and one priority.

Switch position	Unit number	Priority
0	0x00	00
1	0x01	01
2	0x02	02
3	0x03	03
4	0x04	04
5	0x05	10
6	0x06	11
7	0x07	12
8	0x08	13
9	0x09	14
A	0x0a	20
B	0x0b	21
C	0x0c	22
D	0x0d	23
E	0x0e	24
F	0x0f	30

Pull down resistors for the service port:

Output signals from the service port are open collector signals. These signals must be pulled down to -12v by one and only one module in a Supermax system. When the NIOC is installed in a Supermax system pull down resistors are placed on the basic CPU module in the system. If the NIOC is used outside a Supermax system pull down resistors must be placed in position I9.

Firmware:

The firmware is situated in an EPROMs mounted in position Q1, even bytes, and Q2, odd bytes.

The PROMs contain a test program that is executed after power up reset. After the testprogram has been executed the firmware enables the NIOC to be booted in a Supermax system.

Straps and jumpers:

+ designates factory installed position.

AJ1

Function: Controls polarity of the Acknowledge input from the parallel printer port.

+ PIN 1 connected to PIN 2: Acknowledge is an active high input.

PIN 2 connected to PIN 3: Acknowledge is an active low input.

AJ2

Function: Controls polarity of the Busy input from the parallel printer port.

PIN 1 connected to PIN 2: Busy is an active low input.

+ PIN 2 connected to PIN 3: Busy is an active high input.

AJ3

Function: Controls the size of the PROMs:

PROM type 2764:
PIN 1 connected to PIN 2 and PIN 6 connected to PIN 5.

PROM type 27128:
PIN 1 connected to PIN 2 and PIN 6 connected to PIN 5.

+ PROM type 27256:
PIN 2 connected to PIN 3 and PIN 6 connected to PIN 5.

PROM type 27512:
PIN 2 connected to PIN 3 and PIN 5 connected to PIN 4.

AJ4

Function: Controls the baud rate of the service port.

+ PIN 1 connected to PIN 14: 9600 baud
PIN 2 connected to PIN 13: 4800 baud
PIN 3 connected to PIN 12: 2400 baud
PIN 4 connected to PIN 11: 1200 baud
PIN 5 connected to PIN 10: 600 baud
PIN 6 connected to PIN 9 : 300 baud

AJ5

Function: Controls the time between timer interrupts.

PIN 1 connected to PIN 14: 5 ms
+ PIN 2 connected to PIN 13: 10 ms
PIN 3 connected to PIN 12: 20 ms
PIN 4 connected to PIN 11: 40 ms
PIN 5 connected to PIN 10: 80 ms

AJ6

Function: Controls polarity of the Strobe signal in the parallel printer interface.

+ PIN 1 connected to PIN 2: Strobe is an active low pulse.

PIN 2 connected to PIN 3: Strobe is an active high pulse.

AJ7

Function: Controls the reset signal to the NIOC.

PIN 1 connected to PIN 2: The RESET is generated on the NIOC itself by power up.

+ PIN 2 connected to PIN 3: The RESET signal is taken from the IO bus.

AJ8

Function: Controls the BUS CLOCK signal to the NIOC.

PIN 1 connected to PIN 2: The BUS CLOCK is driven by the NIOC itself. The NIOC does not drive the BUS CLOCK line in the IO bus.

+ PIN 2 connected to PIN 3: The BUS CLOCK on the NIOC is driven by the BUS CLOCK line in the IO bus.

Indicator Leds:

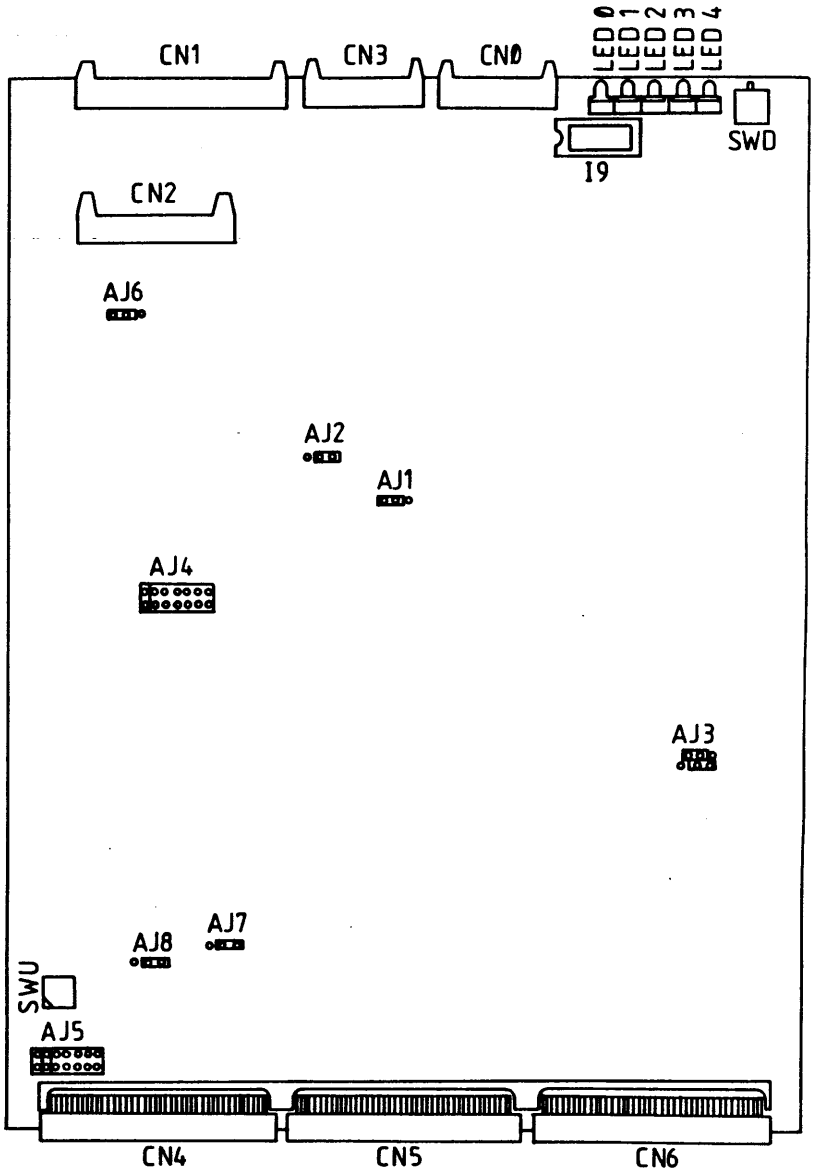
LED0: Indicates activity of the LAN.

LED1: Parity error in memory. Even byte.

LED2: Parity error in memory odd byte.

LED3: The 68000 is in the HALT state.

LED4: The NIOC has activated the error in unit line.


LED0
LED1
LED2
LED3
LED4
CN1
CN3
CN0
SWD
I9
CN2
AJ6
AJ2
AJ1
AJ4
AJ3
AJ7
AJ8
SWU
AJ5
CN4
CN5
CN6

SECTION 1.1

Supermax Technical Data Sheet

Type: NIOC 3600

Data sheet no.: 15

Revision no.: 0

Date: 870622

General description:

The NIOC 3600 is an intelligent Local Area Network Controller in a SUPERMAX system. The pcb can be used either as a NIOC or as a SIOC2 depending on the components in the board, all straps and capabilities denoted by brackets relates to the SIOC2 version of the board. The NIOC is built around a MC68000 microprocessor and contains the following IO interfaces:

- Ethernet interface. IEEE 802.3.
(- External i/O bus for serial RS-232 interfaces.)
(- Parallel printer interface.)
- Service port interface.

Interface to I/O bus:

The NIOC has a standard interface to the common SUPERMAX I/O bus.

Active cycles : Byte read and write.
Word read and write.
Read modify write.

Passive cycles: Byte read and write.
Word read and write.
Double word read and write.
Read modify write.

Ethernet interface.

The NIOC contains the Ethernet transceiver interface. The transceiver cable is connected to a 16 pin flat cable connector CN3.
Signals denoted GNDS can be strapped to ground by AJ0.
Signals denoted term are just terminated otherwise they are not used.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01		GNDS	02
03	C-	C+	04
05	TX-	TX+	06
07	GNDS	GNDS	08
09	RX-	RX+	10
11	+12 V	GND	12
13	GND	term	14
15	term	GNDS	16

(EXTERNAL BUS SERIAL CHANNELS.)

The serial interface includes the following programmable options:

- Baudrates from 50 to 38400 baud.
- Character length from 5 to 8 bits.
- Odd, even or no parity.
- 1, 1.5 or 2 stop bits.

All RS-232 interface boards are connected to a 50 pin flat cable connector CN1.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	GND	D0	02
03	GND	D1	04
05	GND	D2	06
07	GNS	D3	08
09	GND	D4	10
11	GND	D5	12
13	GND	D6	14
15	GND	D7	16
17	GND	A10	18
19	GND	A9	20
21	GND	A8	22
23	GND	A7	24
25	GND	A6	26
27	GND	A5	28
29	GND	A4	30
31	GND	A3	32
33	GND	A2	34
35	GND	A1	36
37	GND	A0	38
39	GND	FINT1	40
41	GND	FINT0	42
43	GND	FAS	44
45	GND	FW	46
47	GND	CSD	48
49	GND	RTS1	50

(Parallel Printer Interface.)

The SIOC2 contains an interface to a parallel printer. The interface is located in a 26 pin flat cable connector CN2. Polarity of handshake signals is selected by straps on the SIOC2.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	DS	GND	02
03	DATA(0)	GND	04
05	DATA(1)	GND	06
07	DATA(2)	GND	08
09	DATA(3)	GND	10
11	DATA(4)	PSENSE	12
13	DATA(5)	GND	14
15	DATA(6)	GND	16
17	DATA(7)	GND	18
19	ACK	GND	20
21	BUSY	GND	22
23	CALL(PE)		24
25	SLCT		26

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

The interface to the service port is located in a 20 pin flat cable connector CN0.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	GND		02
03	TXD		04
05	RXD		06
07	RTS		08
09	CTS		10
11	DSR		12
13	GND	DTR	14
15			16
17			18
19			20

Power requirements:

Voltage		Typ. current
+ 5	+-5%	9.0 A
+12	+-5%	0.1 A
-12	+-5%	0.1 A

Physical dimension:

Standard SUPERMAX module.

Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a NIOC module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Straps.
- Pull down resistors for the service port.
- Transceiver cable.
- (- Flat cables for the serial channels and the parallel) printer.
- Firmware.

These items are described in details in the following text.

Unit number/Priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. The address is called the unit number.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot used the same priority. The NIOC module uses one priority. The NIOC module is equiped with a unit number switch, SWU. The switch gives the module a unit number and one priority.

Switch position	Unit number	Priority
0	0x00	00
1	0x01	01
2	0x02	02
3	0x03	03
4	0x04	04
5	0x05	10
6	0x06	11
7	0x07	12
8	0x08	13
9	0x09	14
A	0x0a	20
B	0x0b	21
C	0x0c	22
D	0x0d	23
E	0x0e	24
F	0x0f	30

Pull down resistors for the service port:

Output signals from the service port are open collector signals. These signals must be pulled down to -12v by one and only one module in a Supermax system. When the NIOC is installed in a Supermax system pull down resistors are placed on the basic CPU module in the system. If the NIOC is used outside a Supermax system pull down resistors must be placed in position I9.

Firmware:

The firmware is situated in an EPROMs mounted in position Q1, even bytes, and Q2, odd bytes.

The PROMs contain a test program that is executed after power up reset. After the testprogram has been executed the firmware enables the NIOC to be booted in a Supermax system.

Straps and jumpers:

+ designates factory installed position.

(AJ1)

Function: Controls polarity of the Acknowledge input from the parallel printer port.

+ PIN 1 connected to PIN 2: Acknowledge is an active high input.

PIN 2 connected to PIN 3: Acknowledge is an active low input.

(AJ2)

Function: Controls polarity of the Busy input from the parallel printer port.

PIN 1 connected to PIN 2: Busy is an active low input.

+ PIN 2 connected to PIN 3: Busy is an active high input.

AJ3

Function: Controls the size of the PROMs:

PROM type 2764:
PIN 1 connected to PIN 2 and PIN 6 connected to PIN 5.

PROM type 27128:
PIN 1 connected to PIN 2 and PIN 6 connected to PIN 5.

+ PROM type 27256:
PIN 2 connected to PIN 3 and PIN 6 connected to PIN 5.

PROM type 27512:
PIN 2 connected to PIN 3 and PIN 5 connected to PIN 4.

AJ4

Function: Controls the baud rate of the service port.

+ PIN 1 connected to PIN 14: 9600 baud
PIN 2 connected to PIN 13: 4800 baud
PIN 3 connected to PIN 12: 2400 baud
PIN 4 connected to PIN 11: 1200 baud
PIN 5 connected to PIN 10: 600 baud
PIN 6 connected to PIN 9 : 300 baud

AJ5

Function: Controls the time between timer interrupts.

PIN 1 connected to PIN 14: 5 ms
+ PIN 2 connected to PIN 13: 10 ms
PIN 3 connected to PIN 12: 20 ms
PIN 4 connected to PIN 11: 40 ms
PIN 5 connected to PIN 10: 80 ms

(AJ6)

Function: Controls polarity of the Strobe signal in the parallel printer interface.

+ PIN 1 connected to PIN 2: Strobe is an active low pulse.

PIN 2 connected to PIN 3: Strobe is an active high pulse.

AJ7

Function: Controls the reset signal to the NIOC.

PIN 1 connected to PIN 2: The RESET is generated on the NIOC itself by power up.

+ PIN 2 connected to PIN 3: The RESET signal is taken from the IO bus.

AJ8

Function: Controls the BUS CLOCK signal to the NIOC.

PIN 1 connected to PIN 2: The BUS CLOCK is driven by the NIOC itself. The NIOC does not drive the BUS CLOCK line in the IO bus.

+ PIN 2 connected to PIN 3: The BUS CLOCK on the NIOC is driven by the BUS CLOCK line in the IO bus.

AJ9

Function: Controls the CLOCK signal to the MANCHESTER encoder.

+ PIN 1 connected to PIN 2: The CLOCK is supplied to pin 14 of the manchester encoder.

PIN 2 connected to PIN 3: pin 134 of the manchester encoder is grounded.

AJA

Function: Controls the Manchester encoder.

PIN 1 connected to PIN 2: Pin 13 of the manchester encoder is left floating.

PIN 2 connected to PIN 3: The CLOCK is supplied to pin 13 of the manchester encoder.

AJB

Function: Controls pin 2 of the manchester encoder.

PIN 1 connected to PIN 2: Pin 2 is connected to pin 1 by AC6.

PIN 2 connected to PIN 3: pin 2 is grounded.

(AJC)

Function: Controls the handshake in the external bus.

PIN 1 connected to PIN 2: Timing controlled by external bus.

+ PIN 2 connected to PIN 3: Timing controlled by the SIOC2.

(AJD)

Function: Polarity of write signal (external bus).

+ PIN 1 connected to PIN 2: Internal logic, factory installed.

PIN 2 connected to PIN 3: NA.

(AJE)

Function: Controls enabeling of data drivers (external bus).

PIN 1 connected to PIN 2:

+ PIN 2 connected to PIN 3: Factory installed.

Indicator Leds:

LED0: Indicates activity of the LAN.

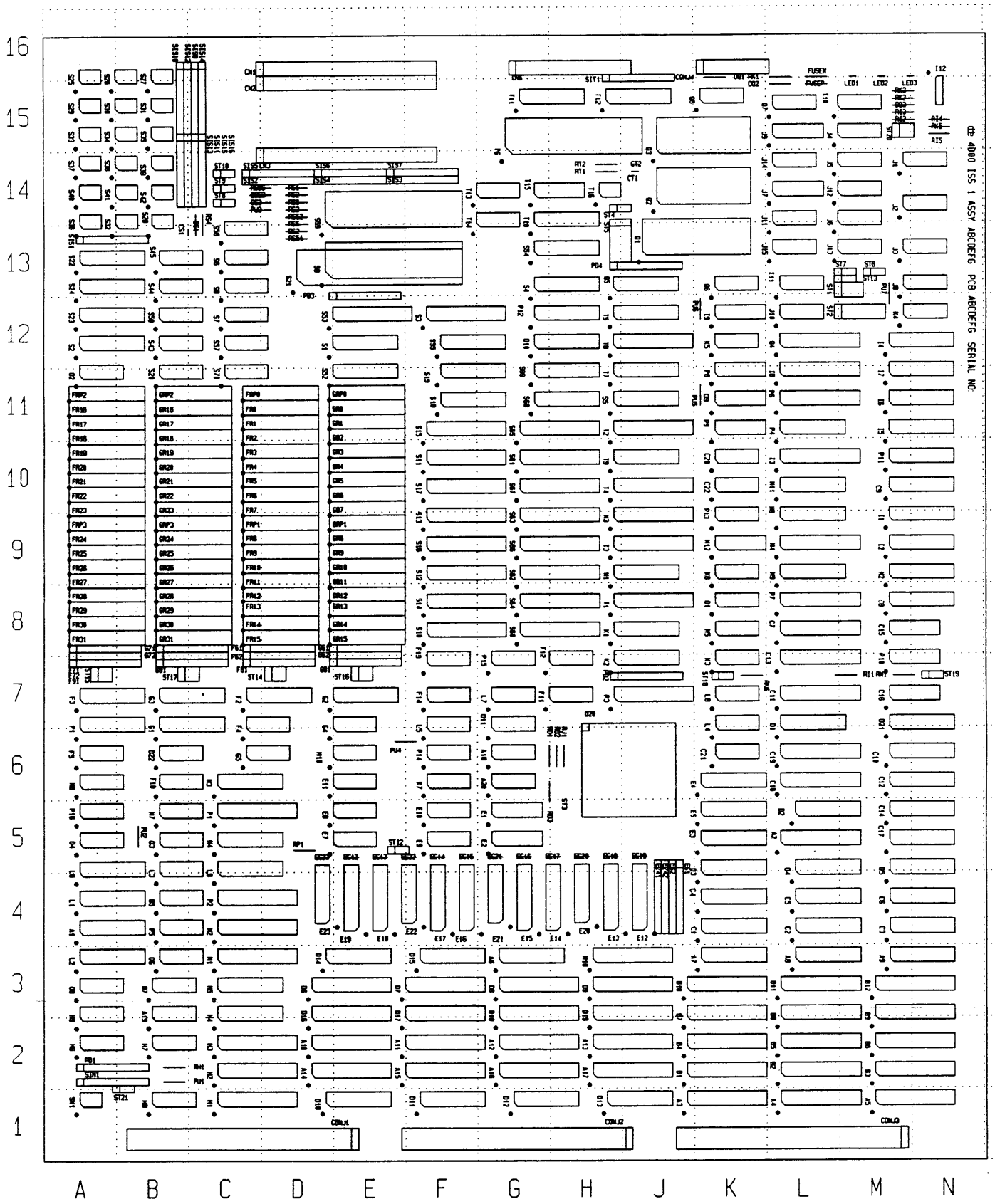
LED1: Parity error in memory. Even byte.

LED2: Parity error in memory odd byte.

LED3: The 68000 is in the HALT state.

LED4: The NIOC has activated the error in unit line.

PRELIMINARY



Component locations

PCB: 4000 / DIOC3	Issue: 1	Date: 880112	dansk data elektronik a/s herlev hovedgade 199. 2730 herlev. tlf. 02-84 50 11

PRELIMINARY

Name	Type	Pos
H2	PPE0	C2
H3	PPF0	C2
H4	74AS641	C2
H5	74AS641	C3
H6	74F74	A2
H7	74F74	B2
H8	74LS14	B1
H9	74AS32	A2
H10	74AS04	D6
I1	74LS642	M9
I2	74LS642	M9
I3	D3040	L10
I4	74ALS574	M12
I5	74ALS573	M11
I6	74AS574	M11
I7	D3370	M11
I8	D3051	L11
I9	74LS163	K12
I10	7438	L15
I11	74LS74	L13
I12	debugswitch	N16
J1	osc.32mHz	M14
J2	osc.40MHz	M14
J3	osc.50MHz	M13
J4	74F74	L15
J5	74F74	L14
J6	74F74	L13
J7	74LS390	L14
J8	74LS393	M13
J9	74LS390	L15
J10	74F74	L12
J11	74AS1004	L13
J12	74AS1004	L14
J13	74AS32	L13
J14	74AS00	L14
J15	74F74	L13
K1	D3090	H8
K2	D3030	H7
K3	74F74	K7
K4	74F74	M12
K5	74F74	K12
K7	74AS20	F6
K8	74AS32	K9
LABEL		O-1
LED1	LEDred	M16
LED2	LEDgreen	M16
LED3	LEDred	M16
L1	D3161	A4
L2	D3170	A3
L3	74F74	B4
L4	74LS74	K6
L5	74F74	F6
L6	74ALS244-1	A4
L7	74AS00	G7
L8	74AS08	K7
L9	D3380	C4
M1	D3070	H9
M2	D3060	M9
M3	D3080	H9
M4	D335140	L9
M5	74F74	K8
M6	74AS32	A6
M7	74AS32	B5
M8	D3300	L9
M9	D3190	L9
M10	D3310	H3
M11	74ALS580	L10
M12	74AS175	K9
N1	D3101	C3
N2	D3111	C4
N3	D3142	C6
N4	74LS541	C5
O1	74AS21	K8
O2	74AS11	A11
O3	74AS08	B5
O4	74F74	A5
O5	74F74	B4
O6	74F74	B3

Name	Type	Pos
O7	74F74	B3
O8	74AS00	A3
O9	74S133	K11
O10	D3360	G12
O11	74F74	G6
PD1	SIL 10-1-101	A2
PD2	SIL 10-1-101	H7
PD3	SIL 10-1-101	D13
PD4	SIL 10-1-101	H13
PU1	1kohm	B2
PU2	1kohm	B5
PU3	1kohm	C14
PU4	1kohm	E6
PU5	1kohm	K11
PU6	1kohm	K13
PU7	1kohm	M13
P1	D3132	C5
P2	D3153	C4
P3	D3180	H7
P4	D3200	L11
P5	74F74	B4
P6	D3330	L11
P7	D3340	L8
P8	74AS138	K11
P9	74AS138	K11
P10	74S139	M7
P11	74LS273	M10
P12	74ALS573	G12
P13	74AS04	K9
P14	74AS08	F6
P15	74AS10	G7
P16		A5
Q1	27C512-15	J13
Q2	SOCKET/EEPROM	J14
Q3	8251A	J14
Q4	D3210	L12
Q5	74ALS645	H13
Q6	74AS32	K13
Q7	75188	L15
Q8	75189	K15
RD1	10kohm	G6
RD2	10kohm	H6
RD3	10kohm	G6
RH1	1kohm	B2
RI1	220ohm	L7
RI2	10kohm	M15
RI3	10kohm	M15
RI4	10kohm	N15
RI5	10kohm	N15
RJ1	1kohm	H6
RK1	150ohm	K16
RK2	150ohm	M15
RK3	150ohm	M15
RK5	10kohm	N15
RK6	10kohm	K7
RM1		M7
RP1	1kohm	D5
RS1	1kohm	D14
RS2	1kohm	D14
RS3	1kohm	D14
RS4	NOT USED	C14
RS5	NOT USED	D14
RS6	Microfuse 1A	D14
RS51	1kohm	D13
RS52	2k7ohm	D14
RS56	Microfuse 1A	C14
RT1	NOT USED	H14
RT2	NOT USED	H14
SIH1	SIL 10-1-103	A2
SIS1	NOT USED	A13
SIS2	SIL 10-4-221/331	C14
SIS3	SIL 10-4-221/331	E14
SIS4	SIL 10-4-221/331	D14
SIS5	SIL 10-4-221/331	C14
SIS6	SIL 10-4-221/331	D14
SIS7	SIL 10-4-221/331	E14
SIS9	NOT USED	C16
SIS10	NOT USED	B16

Name	Type	Pos
SIS11	NOT USED	B15
SIS12	NOT USED	B16
SIS13	NOT USED	B15
SIS14	NOT USED	C16
SIS15	NOT USED	C15
SIS16	NOT USED	C15
SIT1	SIL 10-1-151	H16
ST1	JUMPER (1x2)	L13
ST2	JUMPER (2x7)	L12
ST3	JUMPER (1x2)	H6
ST4	NOT USED	H14
ST5	JUMPER (1x2)	H14
ST6	JUMPER (1x2)	M13
ST7	JUMPER (1x2)	L13
ST8	JUMPER (1x3)	C14
ST9	JUMPER	C14
ST10	JUMPER	C14
ST12	JUMPER	E5
ST13	JUMPER	L13
ST14	JUMPER	D7
ST15	JUMPER	A7
ST16	JUMPER	E7
ST17	JUMPER	B7
ST18		K7
ST19		N7
ST20	JUMPER	M15
ST21	JUMPER	A2
SW1	Hexswitch	A1
S1	D3260	D12
S2	D3250	A12
S3	D3221	F12
S4	D3230	G13
S5	D3240	H11
S6	74AS32	C13
S7	74AS08	C12
S8	74LS14	C13
S9	WD33C93	D13
S10	74ALS646	F8
S11	74ALS646	F10
S12	74ALS646	F9
S13	74ALS646	F9
S14	74ALS646	F8
S15	74ALS646	F11
S16	74ALS646	F9
S17	74ALS646	F10
S18	74ALS573	F11
S19	74ALS645	F11
S20	74AS32	B11
S21	WD33C92	D13
S22	74ALS576	A13
S23	16L8A	A12
S24	16L8A	A13
S25	75176B	A15
S26	75176B	A15
S27	75176B	B15
S28	75176B	B13
S29	75176B	A15
S30	75176B	A15
S31	75176B	B15
S32	75176B	A13
S33	75176B	A15
S34	75176B	A15
S35	75176B	B15
S36	75176B	A13
S37	75176B	A14
S38	75176B	A14
S39	75176B	B14
S40	75176B	A14
S41	75176B	A14
S42	75176B	B14
S43	74F74	B12
S44	7438	B13
S45	74LS08	B13
S52	D3250	D11
S53	D3221	D12
S54	D3230	G13
S55	D3240	F12
S56	74AS32	C13

Component locations

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PRELIMINARY

Name	Type	Pos	Name	Type	Pos	Name	Type	Pos
S57	74AS08	C12						
S58	74LS14	B12						
S59	WD33C93	D13						
S60	74ALS646	G8						
S61	74ALS646	G10						
S62	74ALS646	G9						
S63	74ALS646	G9						
S64	74ALS646	G8						
S65	74ALS646	G11						
S66	74ALS646	G9						
S67	74ALS646	G10						
S68	74ALS573	G11						
S69	74ALS645	G11						
S70	74AS32	C11						
T1	74als646	H8						
T2	74als646	H11						
T3	74als646	H9						
T4	74als646	H10						
T5	74als645	H12						
T6	NS8272	G14						
T7	D3010	H11						
T8	D3290	H12						
T9	D3020	H10						
T10	D3320	G13						
T11	74ls642-1	G15						
T12	74ls540	H15						
T13	7438	F14						
T14	74AS08	F13						
T15	74LS175	G14						
T16	X9103	H14						

Component locations

PCB: 4000 / DIOC3 | Issue: 1 | Date: 880112

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SUPERMAX technical data sheet.
Module: SIOC 0300

Type: SIOC 0300

Data sheet no.: 1

Revision no.: 0

Date: 851008

General description:

The SIOC is the intelligent Serial IO Controller in a SUPERMAX system. The SIOC is built around a microprocessor and contains the following interfaces:

- 6 asynchronous RS-232 channels.
- 2 asynchronous RS-232 or RS-422 channels.
- Parallel printer port.

Interface to I/O bus:

The SIOC has a standard interface to the common SUPERMAX I/O bus. The local memory bus is not used.

Active cycles : Byte read and write.

Passive cycles: Byte read and write.
Word read and write.
Read modify write.

Interface to peripheral equipment:

Seriel Channels:

The seriel interface includes the following programmable options:

- Baudrates from 50 to 19200 baud.
- Character length from 5 to 8 bits.
- Odd, even or no parity.
- 1, 1.5 or 2 stop bits.
- For two channels: Choice of RS-232 or RS-422 interface.

The RS-232 interface signals are all situated in a 60 pin flatcable header.

PIN	SIGNAL	SIGNAL	PIN
01	TXC7	GND	02
03	RXC7	GND	04
05	DTR7	DSR7	06
07	CTS7	RTS7	08
09	RXD7	TXD7	10
11	TXC6	RXC6	12
13	DTR6	DSR6	14
15	CTS6	RTS6	16
17	RXD6	TXD6	18
19	GND	GND	20
21	GND	+12V	22
23	GND	-12V	24
25	DTR5	DSR5	26
27	CTS5	RTS5	28
29	RXD5	TXD5	30
31	DSR4	DTR4	32
33	RTS4	CTS4	34
35	TXD4	RXD4	36
37	RTS3	DTR3	38
39	TXD3	DSR3	40
41	DSR2	CTS3	42
43	RTS2	RXD3	44
45	TXD0	DTR2	46
47	RXD0	CTS2	48
49	RTS0	RTS1	50
51	CTS0	CTS1	52
53	DSR0	DSR1	54
55	DTR0	DTR1	56
57	TXD1	TXD2	58
59	RXD1	RXD2	60

The RS-422 signals and the parallel printer signals are all situated in a 50 pin flatcable header.

PIN	SIGNAL	SIGNAL	PIN
01	I(A)0	C(A)0	02
03	GND	R(A)0	04
05	S(A)0	T(A)0	06
07	GND	GND	08
09	I(B)0	S(B)0	10
11	C(B)0	R(B)0	12
13	ACK	T(B)0	14
15	CD(0)	DS	16
17	CD(1)	GND	18
19	CD(2)	GND	20
21	CD(3)	GND	22
23	CD(4)	GND	24
25	CD(5)	GND	26
27	CD(6)	GND	28
29	CD(7)	GND	30
31	BUSY	R(A)1	32
33	open	GND	34
35	I(A)1	GND	36
37	S(A)1	GND	38
39	S(B)1	GND	40
41	R(B)1	I(B)1	42
43	C(B)1	GND	44
45	T(B)1	GND	46
47	T(A)1	GND	48
49	C(A)1	GND	50

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

Power requirements:

Voltage		Typ. current
+ 5	+-5%	4.6 A
+12	+-5%	0.2 A
-12	+-5%	0.2 A

Physical dimension:

Standard SUPERMAX module.

Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a SIOC module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Straps.
- Pull down resistors for the service port.
- Flat cables for the serial channels and the parallel printer.
- Firmware.

These items are described in details in the following text.

Unit number/Priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. The address is called the unit number. The unit number of the SIOC module is coded in a PAL located in position I2. This PAL is called the unit PAL.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot used the same priority. The SIOC module uses one priority. The priority of the SIOC module are coded in a PAL located in position M1. This PAL is called the priority PAL.

Pull down resistors for the service port:

Output signals from the service port are open collector signals. These signals must be pulled down to -12v by one and only one module in a Supermax system. Pull down resistors are placed in position Q3.

Firmware:

The firmware is situated in an EPROM mounted in position E4.

SBOOT, V. 0100, 830401.

The SIOC with the this firmware will be able to be bootstraped of another module in a Supermax system.

Straps and jumpers:

+ designates factory installed position.

Strap socket 1.

Function: USART interrupt, Rxrdy.

Position: A 2,10
Name : A6

```
                1.
Rxrdy(0)        *       *  RST0
Rxrdy(1)        *       *  RST1
Rxrdy(2)        *       *  RST2
Rxrdy(3)        *       *  RST3
Rxrdy(4)        *       *  RST4
Rxrdy(5)        *       *  RST5
Rxrdy(6)        *       *  RST6
Rxrdy(7)        *       *  RST7
```

Factory installed:

```
                1.
Rxrdy(0)        *       *  RST0
Rxrdy(1)        *       *  RST1
Rxrdy(2)        *       *  RST2
Rxrdy(3)        *       *  RST3
Rxrdy(4)        *       *  RST4
Rxrdy(5)        *       *  RST5
Rxrdy(6)        *       *  RST6
Rxrdy(7)        *       *  RST7
```

Strap socket 2.

Function: USART interrupt, Txrdy.

Position: A 1,10
Name : A7

```
                1.
Txrdy(0)        *       *  RST0
Txrdy(1)        *       *  RST1
Txrdy(2)        *       *  RST2
Txrdy(3)        *       *  RST3
Txrdy(4)        *       *  RST4
Txrdy(5)        *       *  RST5
Txrdy(6)        *       *  RST6
Txrdy(7)        *       *  RST7
```

Not installed from factory.

Strap socket 3.

Function: RS-422 Indicator interrupt.

Position: A 1,9
Name : A8

```
        1.
IINT1   *       *  RST7
IINT1   *       *  RST6
IINT2   *       *  RST5
IINT2   *       *  RST4
IINT3   *       *  RST3
IINT3   *       *  RST2
IINT4   *       *  RST1
IINT4   *       *  RST0
```

Not installed from factory.

Strap socket 4.

Function: Possible to connect two swithes. One is able to generate an internal reset pulse and one is able to generate a hardware "TRAP" interrupt to the 8085.

Position: C 4,1.

Factory installed strapsocket:

```
  * *_* * * * * *

  * *_* * * * * *
1.
```

Strap 1.

Function: Baud rate to service port. Connected to both Txclk and Rxclk.

Position: B 7,1

```
* * * *
* * * *
1 2 3 4
```

Jumper	Clock
+ 1	9600 x 16 baud.
2	4800 x 16 baud.
3	2400 x 16 baud.
4	1200 x 16 baud.

Strap 2.

Function: Special option for hardware service.

Position: B 8,3

Under normal circumstances, the jumper must be in position one.

Strap 3.

Function: Polarity of the parallel printer port signal "DATA STROBE".
The data strobe signal is an output signal.
Position: C 3,4
Name : SP2

```
* * *
1 2 3
```

Jumper	Function
1-2	Active high data strobe.
+ 2-3	Active low data strobe.

Strap 4.

Function: Polarity of the parallel printer port signal "BUSY".
The BUSY signal is an input.

Position: C 2,4
Name : SP3

* * *
1 2 3

Jumper	Function
+ 1-2	Active high BUSY signal.
2-3	Active low BUSY signal.

Strap 5.

Function: Polarity of the parallel printer port signal "ACKNOWLEDGE". The ACK signal is an input.
Position: C 2,4
Name : SP1

* * *
1 2 3

Jumper	Function
+ 1-2	Active low ACK signal.
2-3	Active high ACK signal.

Strap 6.

Function: Transmitter clock to USART(6). RS-232-C interface.

Position: B 6,10
Name : SS1

* * *
1 2 3

Jumper	Function
+ 1-2	The SIOC drives the RS-232-C interface signal Txclk with

baud rate counter(2,0).
The clock is an input to USART(6).

2-3 The RS-232-C interface signal Txclk is an input to USART(6).

Strap 7.

Function: Receiver clock to USART(6). RS-232-C interface.

Position: B 6,10
Name : SS2

* * *
1 2 3

Jumper	Function
+ 1-2	The SIOC drives the RS-232-C interface signal Rxclk with baud rate counter(2,0). The clock is an input to USART(6).
2-3	The RS-232-C interface signal Rxclk is an input to USART(6).

Strap 8 and 9.

Function: Receiver/transmitter clock to USART(6). RS-422 interface.

Position: B 6,7
Name : SS3 and SS4.

* * *
1 2 3

Jumper	Function
+ 1-2	The SIOC drives the RS-422 interface signal Signal element timing with baud rate counter(2,0). The clock is an input to USART(6).

2-3 The RS-422 interface signal Signal element timing is an input to USART(6). (Rxclk and Txclk)

Note that SS3 and SS4 jumpers must be in the same position.

Strap 10.

Function: Transmitter clock to USART(7). RS-232-C interface.

Position: B 9,6
Name : ST1

```
* * *
1 2 3
```

Jumper	Function
+ 1-2	The SIOC drives the RS-232-C interface signal Txclk with baud rate counter(2,1). The clock is an input to USART(7).
2-3	The RS-232-C interface signal Txclk is an input to USART(7).

Strap 11.

Function: Receiver clock to USART(7). RS-232-C interface.

Position: B 9,6
Name : ST2

```
* * *
1 2 3
```

Jumper	Function
+ 1-2	The SIOC drives the RS-232-C interface signal Rxclk with baud rate counter(2,1). The clock is an input to USART(7).

2-3 The RS-232-C interface signal Rxclk is an input to USART(7).

Strap 12 and 13.

Function: Receiver/transmitter clock to USART(7). RS-422 interface.

Position: B 6,6
Name : ST3 and ST4.

* * *
1 2 3

Jumper	Function
+ 1-2	The SIOC drives the RS-422 interface signal Signal element timing with baud rate counter(2,1). The clock is an input to USART(7).
2-3	The RS-422 interface signal Signal element timing is an input to USART(7). (Rxclk and Txclk)

Note that ST3 and ST4 jumpers must be in the same position.

Cables and connectors:

The connection between the SIOC module and the peripherals is made with two flat cable connectors.

The headers mounted on the PCB are positioned as follows:

RS-232 interface signals : C 4,8. 60 pin

RS-422 and the parallel printer : C 3,8. 50 pin or 34 pin.

Service port : C 5,3. 20 pin

Indicator Leds:

LED1: On: The boot prom is enabled.
Off: The boot prom is disabled.
Upon power up: On

LED2: On: A time out is pending.
Off: No time out.
Upon power up: Off.

LED3: On: A buserror is received.
Off: No buserror.
Upon power up: Off.

LED4: On: The ERROR line is active. The error line is set by the program or because of a parity error.
Off: No error.
Upon power up: On

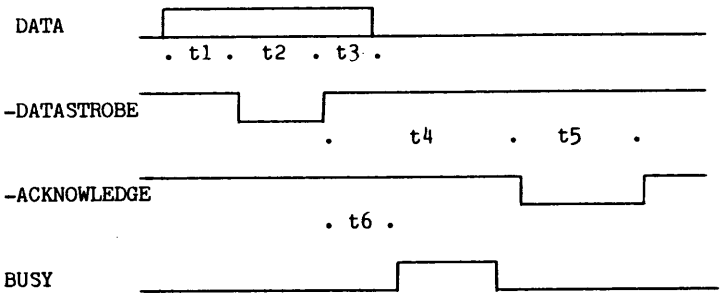
LED5: On: The SIOC has activated the buserror signal.
Off: No error.
Upon power up: Off.

Parallel printer interface specifications:

The parallel port is a Centronics compatible printer interface. The interface is a 8 bit data interface with three control signals. The control signals are:

1. Data strobe. An output from the SIOC.
2. Acknowledge. An input to the SIOC.
3. Busy. An input to the SIOC.

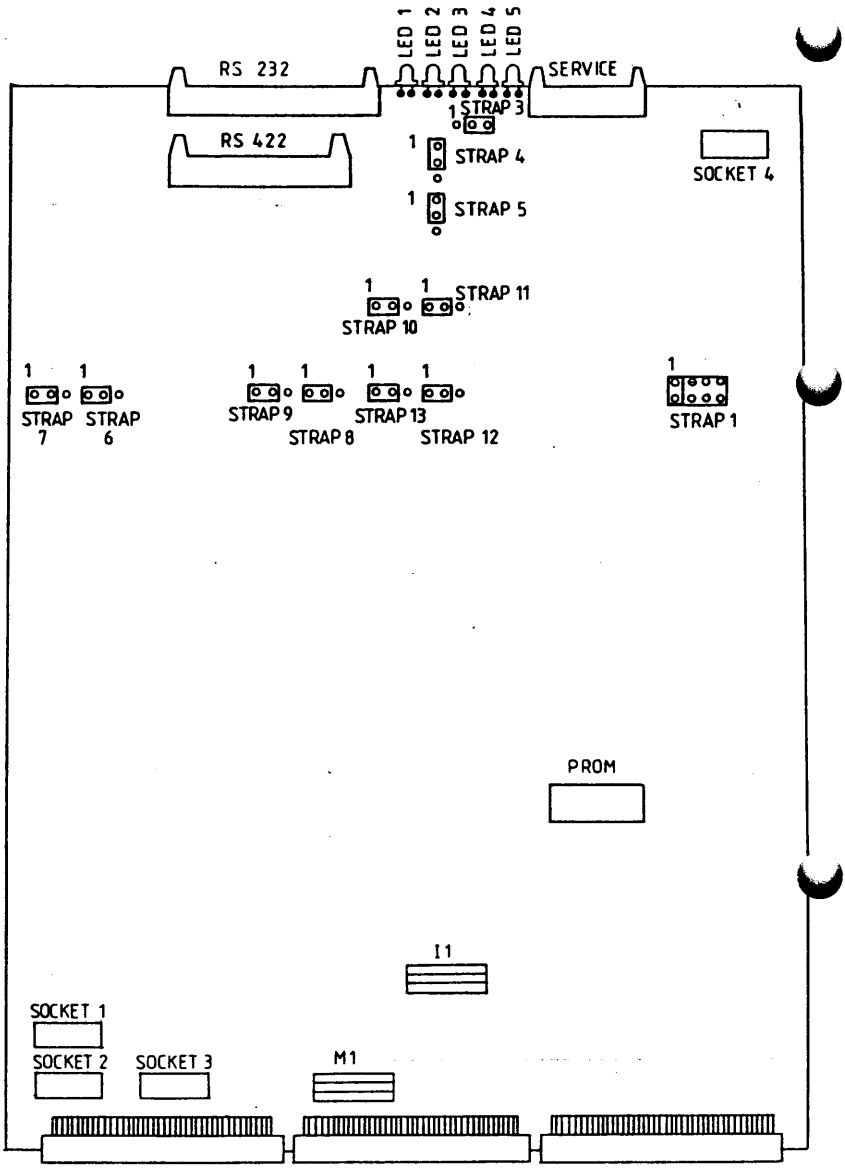
Interface timing:



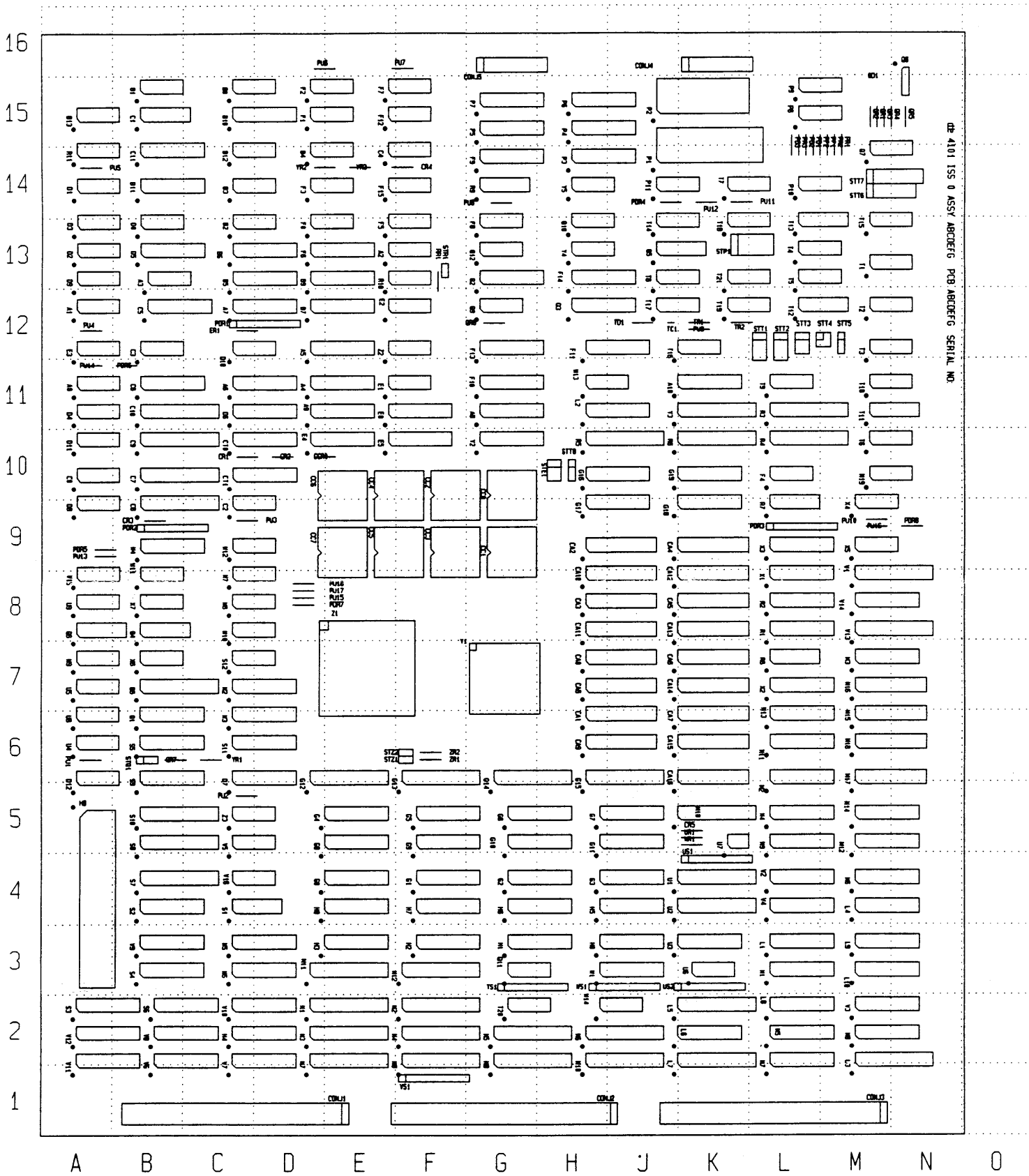
- designates active low signals.

t1: Data stable to datastrobe: min. 1.0 usec.
t2: Datastrobe width : min. 1.0 usec. max. 2.0 usec.
t3: Data hold from datastrobe: min. 1.0 usec.
t4: Datastrobe to acknowledge: min. 0.1 usec.
t5: Acknowledge width : min. 0.1 usec.
t6: Datastrobe to busy : min. 0

SUPERMAX technical data sheet.
Module: SIOC 0300



PRELIMINARY



Component locations

PCB: 4101 / 68030	Issue: 0	Date: 881021	dde	dansk data elektronik a/s herlev hovedgade 199. 2730 herlev. tlf. 02-84 50 11

PRELIMINARY

Name	Type	Pos
+5V		A2
+12V		A3
-12V		A2
AC0		F15
AC1		E15
AC2		B11
AC3		B11
AC4		G7
AC5		B1
AC6		F15
AC7		F15
AJA		G15
AJB		G15
AJC		D11
AJD		B14
AJE		A16
AJ0		G15
AJ1		G9
AJ2		E10
AJ3		L6
AJ4		B8
AJ5		A1
AJ6		C11
AJ7		C2
AJ8		B2
AJ9		H15
AR0		J11
AR1		H11
AR2		J11
AR3		H11
AR4		H11
AR5		J11
AR6		J11
AR7		J11
AR8		H13
AR9		H12
A0		L1
A1		L3
A2		L2
A3		L3
A4		M4
A5		M2
A6		M3
A7		M4
A8		M1
A9		M3
BR0		H11
BR1		J11
BR2		J11
BR3		H11
BR4		H13
BR5		H11
BR6		M15
BR7		C11
BR8		C11
BR9		G9
BR10		C14
BR11		E14
BR12		E14
B0		G3
B1		H6
B2		H4
B3		F5
B4		J3
B5		E6
B6		E4
B7		M5
B8		E1
B9		G1
CN0		K16
CN1		C16
CN2		C14
CN3		G16
CN4		E1
CN5		J1
CN6		M1
CR0		F15
CR1		F15

Name	Type	Pos
CR2		F15
CR3		F15
CR4		F15
CR5		E15
CR6		E15
CR7		E15
CR8		G15
CR9		G15
CR10		F15
CR11		F15
C0		H1
C1		J1
C2		J5
C3		J6
C4		L4
C5		M5
C6		J3
C7		J4
C8		J4
C9		J5
DI0		H15
DI1		H15
DI2		L15
DI3		L16
DI4		K15
DI5		C1
DR0		M11
DR1		M11
DR2		M11
DR3		K11
DR4		K11
DR5		K11
DR6		K11
DR7		K11
DR8		L11
DR9		J11
D0		H2
D1		L4
D2		H4
D3		L5
D4		L5
D5		J8
D6		J8
D7		L8
D8		J7
D9		L10
ER0		M11
ER1		N11
ER2		N11
ER3		L11
ER4		L11
ER5		L11
ER6		L11
ER7		L11
ER8		M11
ER9		K11
E0		L9
E1		J9
E2		L10
E3		M10
E4		J10
E5		M10
E6		L6
E7		A7
E8		C9
E9		A1
FR0		L11
FR1		M11
FR2		K11
FR3		L11
FR4		B2
FR5		B2
FR6		B2
FR7		B2
FR8		C2
FR9		M15
FS1		H15
F0		J15

Name	Type	Pos
F1		J14
F2		J14
F3		J13
F4		J13
F5		J13
F6		J12
F7		J12
F8		J11
F9		B1
GND		A1
GRA		E10
GR0		M15
GR1		H3
GR2		M15
GR3		M15
GR5		M6
GR6		M15
GR7		D3
GR8		C3
GR9		M15
G0		L15
G1		L14
G2		L14
G3		L13
G4		L13
G5		L13
G6		L12
G7		L12
G8		L11
HR0		G7
HR1		E8
HR7		E2
HR8		E3
HR9		E6
H0		K15
H1		K14
H2		K14
H3		K13
H4		K13
H5		K13
H6		K12
H7		K12
H8		K11
IRA		C12
IR0		E6
IR1		F8
IR2		H7
IR3		G6
IR4		E10
IR5		C1
IR6		K15
IR7		B10
IR8		G12
IR9		G8
I0		M15
I1		M14
I2		M14
I3		M13
I4		M13
I5		M13
I6		M12
I7		M12
I8		M11
I9		L15
K0		D2
K1		G2
K2		D1
K3		A3
K4		B2
K5		C2
K6		B3
K7		C1
K8		E2
K9		D3
LED0		L16
LED1		L16
LED2		M16
LED3		M16

Component locations

PCB: NIOC / SIOC | Issue: | Date:

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PRELIMINARY

Name	Type	Pos
LED4		M16
L0		G3
L1		D3
L2		B4
L3		D5
L4		G4
L5		E3
L6		B3
L7		A3
L8		C4
L9		D6
M0		C7
M1		A8
M2		L7
M3		J7
M4		L8
M5		L7
M6		B8
M7		B8
M8		A6
M9		E8
NY0		F15
NY1		F15
N0		B6
N1		B7
N2		D5
N3		C6
N4		A5
N5		B6
N6		A4
N7		C5
N8		C5
N9		A5
O0		B4
O1		B5
O2		B5
O3		E4
O4		D4
O5		D9
O6		E8
O7		D8
O8		D7
O9		D8
PUA		F7
PU1		C6
PU2		B2
PU3		A4
PU4		A6
PU5		A7
PU6		E9
PU7		G7
PU8		A9
PU9		B8
PU10		C8
PU11		C12
PU12		D11
P0		C9
P1		D7
P2		C7
P3		C6
P4		C8
P5		D6
P6		J2
P7		L9
P8		M9
P9		L6
Q0		L7
Q1		L8
Q2		L6
Q3		J15
Q4		K15
Q5		L9
Q6		G4
Q7		H6
Q8		G6
Q9		D4
R0		H7
R1		L7

Name	Type	Pos
R2		J6
R3		E7
R4		E6
R5		G6
R6		C3
R7		C3
R8		A11
R9		A10
R10		D10
R11		B10
R12		C10
SI0		H15
SI1		H15
SI2		H15
SI3		D11
SI4		A12
SI9		D14
SI10		A15
SI11		C14
SI12		D15
SI13		C16
SI14		E15
SI15		A15
SWD		M16
SWU		A2
S0		A8
S1		A9
S2		A4
S3		A9
S4		A6
S5		A7
S6		B7
S7		C8
S8		B9
TR1		A11
TR2		B11
TR3		A12
TR4		B12
TR5		C12
TR6		C12
TR7		C12
TR8		D11
TR9		B12
TTR1		B11
TTR2		B11
TTR3		B11
T0		D9
T1		B13
T2		A13
T3		C13
T4		C10
T5		C11
T6		C12
T7		C12
T8		B12
T9		B12
T10		C13
T11		D11
T12		D12
T13		D12
T14		D13
T15		A12
T16		D13
T17		D13
T18		A13
T19		A13
T20		A14
T21		A12
T22		A15
T23		A15
T24		C13
U2		E7
U3		B10
U4		H3
U5		H3
U6		C4
U7		H10
U8		E3

Name	Type	Pos
U9		M6
W0		H15
W1		H14
W2		H14
W3		H13
W4		H13
W5		H13
W6		H12
W7		H12
W8		H11
W9		H11
XA		E13
XB		G13
XC		E12
XD		G12
XE		D10
XF		E13
XG		G13
XH		E12
X0		E9
X1		E13
X2		G13
X3		J9
X4		J10
X5		G10
X6		G10
X7		E11
X8		G11
X9		H9
YA		G7
YB		E9
YC		G7
YD		E10
YE		H8
YF		G9
Y0		E10
Y1		E14
Y2		G15
Y3		G12
Y4		G8
Y5		H8
Y6		B9
Y7		H9
Y8		G9
Y9		H7
ZC		B13
ZD		B13
ZE		B11
ZF		G10
ZG		A14
ZH		A11

Component locations

PCB: NIOC / SIOC | Issue: | Date:

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Type: SIOC2 3600

Data sheet no.: 16

Revision no.: 1

Date: 880311

General description:

The SIOC2 3600 is an intelligent asyncronius peripheral controller in a SUPERMAX system. The pcb can be used either as a NIOC or as a SIOC2 depending on the components in the board, all straps and capabilities denoted by brackets relates to the NIOC version of the board. The SIOC2 is built around a MC68000 microprocessor and contains the following IO interfaces:

(- Ethernet interface. IEEE 802.3.)
- External I/O bus for serial RS-232 interfaces.
- Parallel printer interface.
- Service port interface.

Interface to I/O bus:

The SIOC2 has a standard interface to the common SUPERMAX I/O bus.

Active cycles : Byte read and write.
Word read and write.
Read modify write.

Passive cycles: Byte read and write.
Word read and write.
Double word read and write.
Read modify write.

(Ethernet interface.)

The NIOC contains the Ethernet transceiver interface. The transceiver cable is connected to a 16 pin flat cable connector CN3.
Signals denoted GNDS can be strapped to ground by AJ0.
Signals denoted term are just terminated otherwise they are not used.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01		GNDS	02
03	C-	C+	04
05	TX-	TX+	06
07	GNDS	GNDS	08
09	RX-	RX+	10
11	+12 V	GND	12
13	GND	term	14
15	term	GNDS	16

EXTERNAL BUS SERIAL CHANNELS.

The serial interface includes the following programmable options:

- Baudrates from 50 to 38400 baud.
- Character length from 5 to 8 bits.
- Odd, even or no parity.
- 1, 1.5 or 2 stop bits.

All RS-232 interface boards are connected to a 50 pin flat cable connector CN1.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	GND	D0	02
03	GND	D1	04
05	GND	D2	06
07	GNS	D3	08
09	GND	D4	10
11	GND	D5	12
13	GND	D6	14
15	GND	D7	16
17	GND	A10	18
19	GND	A9	20
21	GND	A8	22
23	GND	A7	24
25	GND	A6	26
27	GND	A5	28
29	GND	A4	30
31	GND	A3	32
33	GND	A2	34
35	GND	A1	36
37	GND	A0	38
39	GND	FINT1	40
41	GND	FINT0	42
43	GND	FAS	44
45	GND	FW	46
47	GND	CSD	48
49	GND	RTS1	50

Parallel Printer Interface.

The SIOC2 contains an interface to a parallel printer. The interface is located in a 26 pin flat cable connector CN2. Polarity of handshake signals is selected by straps on the SIOC2.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	DS	GND	02
03	DATA(0)	GND	04
05	DATA(1)	GND	06
07	DATA(2)	GND	08
09	DATA(3)	GND	10
11	DATA(4)	PSENSE	12
13	DATA(5)	GND	14
15	DATA(6)	GND	16
17	DATA(7)	GND	18
19	ACK	GND	20
21	BUSY	GND	22
23	CALL(PE)		24
25	SLCT		26

Interface to service port:

The interface to the service port is a modified RS 232C interface. All output signals are "open collector" signals and may be wired together with the corresponding output signals from other units i a Supermax system. Pull down resistors are used to pull the signals down to -12 v when not driven by an output.

The interface to the service port is located in a 20 pin flat cable connector CN0.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	GND		02
03	TXD		04
05	RXD		06
07	RTS		08
09	CTS		10
11	DSR		12
13	GND	DTR	14
15			16
17			18
19			20

Power requirements:

Voltage		Typ. current
+ 5	+-5%	9.0 A
+12	+-5%	0.1 A
-12	+-5%	0.1 A

Physical dimension:

Standard SUPERMAX module.

Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a SIOC2 module is installed in a Supermax system the following items must be selected/checked:

- Unit number/Priority.
- Straps.
- Pull down resistors for the service port.
- Transceiver cable.
- Flat cables for the serial channels and the parallel printer.
- Firmware.

These items are described in details in the following text.

Unit number/Priority:

Each intelligent Supermax module connected to the common I/O bus has a unique address. The address is called the unit number.

The arbitration scheme used in the common I/O bus is based on fixed priorities. Two units connected to the the I/O bus cannot used the same priority. The NIOC module uses one priority. The SIOC2 module is equiped with a unit number switch, SWU. The switch gives the module a unit number and one priority.

Switch position	Unit number	Priority
0	0x00	00
1	0x01	01
2	0x02	02
3	0x03	03
4	0x04	04
5	0x05	10
6	0x06	11
7	0x07	12
8	0x08	13
9	0x09	14
A	0x0a	20
B	0x0b	21
C	0x0c	22
D	0x0d	23
E	0x0e	24
F	0x0f	30

Pull down resistors for the service port:

Output signals from the service port are open collector signals. These signals must be pulled down to -12v by one and only one module in a Supermax system. When the NIOC is installed in a Supermax system pull down resistors are placed on the basic CPU module in the system. If the SIOC2 is used outside a Supermax system pull down resistors must be placed in position I9.

Firmware:

The firmware is situated in an EPROMs mounted in position Q1, even bytes, and Q2, odd bytes.

The PROMs contain a test program that is executed after power up reset. After the testprogram has been executed the firmware enables the SIOC2 to be booted in a Supermax system.

Straps and jumpers:

+ designates factory installed position.

AJ1

Function: Controls polarity of the Acknowledge input from the parallel printer port.

+ PIN 1 connected to PIN 2: Acknowledge is an active high input.

PIN 2 connected to PIN 3: Acknowledge is an active low input.

AJ2

Function: Controls polarity of the Busy input from the parallel printer port.

PIN 1 connected to PIN 2: Busy is an active low input.

+ PIN 2 connected to PIN 3: Busy is an active high input.

AJ3

Function: Controls the size of the PROMs:

PROM type 2764:
PIN 1 connected to PIN 2 and PIN 6 connected to PIN 5.

PROM type 27128:
PIN 1 connected to PIN 2 and PIN 6 connected to PIN 5.

+ PROM type 27256:
PIN 2 connected to PIN 3 and PIN 6 connected to PIN 5.

PROM type 27512:
PIN 2 connected to PIN 3 and PIN 5 connected to PIN 4.

AJ4

Function: Controls the baud rate of the service port.

+ PIN 1 connected to PIN 14: 9600 baud
PIN 2 connected to PIN 13: 4800 baud
PIN 3 connected to PIN 12: 2400 baud
PIN 4 connected to PIN 11: 1200 baud
PIN 5 connected to PIN 10: 600 baud
PIN 6 connected to PIN 9 : 300 baud

AJ5

Function: Controls the time between timer interrupts.

PIN 1 connected to PIN 14: 5 ms
+ PIN 2 connected to PIN 13: 10 ms
PIN 3 connected to PIN 12: 20 ms
PIN 4 connected to PIN 11: 40 ms
PIN 5 connected to PIN 10: 80 ms

AJ6

Function: Controls polarity of the Strobe signal in the parallel printer interface.

+ PIN 1 connected to PIN 2: Strobe is an active low pulse.

PIN 2 connected to PIN 3: Strobe is an active high pulse.

AJ7

Function: Controls the reset signal to the SIOC2.

PIN 1 connected to PIN 2: The RESET is generated on the NIOC itself by power up.

+ PIN 2 connected to PIN 3: The RESET signal is taken from the IO bus.

AJ8

Function: Controls the BUS CLOCK signal to the SIOC2.

PIN 1 connected to PIN 2: The BUS CLOCK is driven by the SIOC2 itself. The SIOC2 does not drive the BUS CLOCK line in the IO bus.

+ PIN 2 connected to PIN 3: The BUS CLOCK on the SIOC2 is driven by the BUS CLOCK line in the IO bus.

(AJ9)

Function: Controls the CLOCK signal to the MANCHESTER encoder.

+ PIN 1 connected to PIN 2: The CLOCK is supplied to pin 14 of the manchester encoder.

PIN 2 connected to PIN 3: pin 134 of the manchester encoder is grounded.

(AJA)

Function: Controls the Manchester encoder.

PIN 1 connected to PIN 2: Pin 13 of the manchester encoder is left floating.

PIN 2 connected to PIN 3: The CLOCK is supplied to pin 13 of the manchester encoder.

(AJB)

Function: Controls pin 2 of the manchester encoder.

PIN 1 connected to PIN 2: Pin 2 is connected to pin 1 by AC6.

PIN 2 connected to PIN 3: pin 2 is grounded.

AJC

Function: Controls the handshake in the external bus.

PIN 1 connected to PIN 2: Timing controlled by external bus.

+ PIN 2 connected to PIN 3: Timing controlled by the SIOC2.

AJD

Function: Polarity of write signal (external bus).

+ PIN 1 connected to PIN 2: Internal logic, factory installed.

PIN 2 connected to PIN 3: NA.

AJE

Function: Controls enabeling of data drivers (external bus).

PIN 1 connected to PIN 2:

+ PIN 2 connected to PIN 3: Factory installed.

Indicator Leds:

LED0: Indicates activity of the LAN.

LED1: Parity error in memory. Even byte.

LED2: Parity error in memory odd byte.

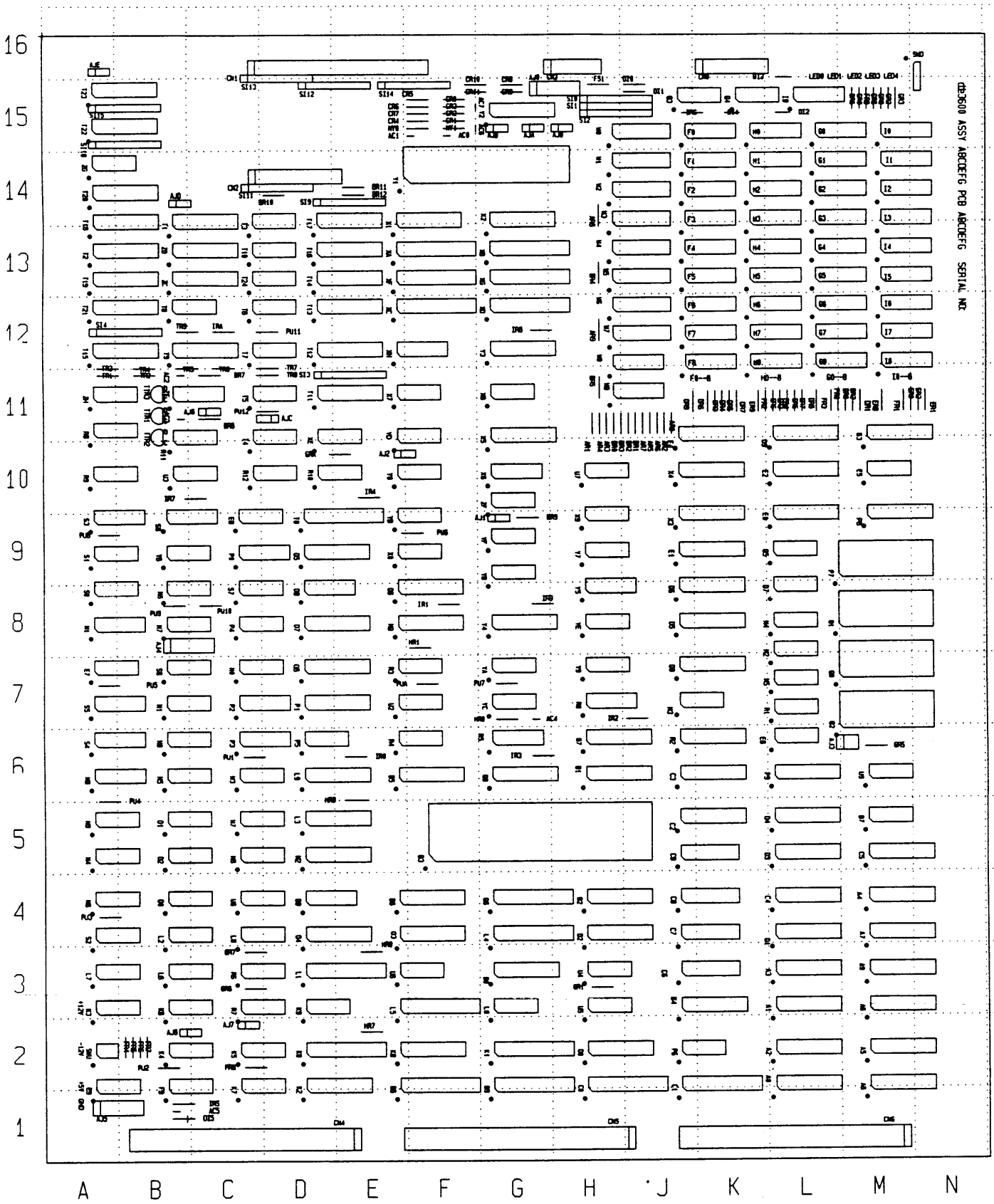
LED3: The 68000 is in the HALT state.

LED4: The SIOC2 has activated the error in unit line.

SIOC2 SUB MODULES.

A SIOC2 sub module is connected to the SIOC2 by the cnl 50 pin flatcable connector.
The 50 pin flatcable contains 11 address, 8 data, interrupt and control signals nescesary to place peripherals outside the supermax cardcage.
Eatch sub module contains eight serial channels, the sub modules place in the external bus address space is decided by a rotary switch, ei the first module should have the switch in position zero, the second in position one. The last module (the module at the end of the cabble) should have terminations resistors for the cabble, three single in line resistor networks with nine 100 ohms resistors to one commen pin.
The flat cabble for the external bus is a shielded cabble, with a maximum lenght of 15 feet.

PRELIMINARY



Component locations				
PCB: NIOC / SIOC	Issue:	Date:	dde	dansk data elektronik a/s herlev hovedgade 199. 2730 herlev. tlf. 02-84 50 11

PRELIMINARY

Name	Type	Pos
A1		E3
A2		E4
A3		E4
A4		C3
A5		C4
A6		A2
A7		A1
A8		B1
A9		C4
A10		A3
A11		B3
A12		A3
A13		B3
A14		B2
A15		C3
B1		H3
B2		H4
B3		E5
B4		F5
B5		F4
B6		F4
B7		H5
B8		H4
B9		J12
B10		G4
CJ1		J16
CJ2		J16
CJ3		J16
CONJ1		E1
CONJ2		J1
CONJ3		M1
CP1		G15
CP2		G15
CQ1		L15
CQ2		L15
CT1		E12
C1		L5
C2		M5
C3		J5
C4		L8
C5		L9
C6		L10
C7		J4
C8		M8
C9		M8
C10		M8
C11		M9
C12		M9
C12A		B12
C12B		B12
C12C		B13
C12D		B13
C12E		D13
C12F		D13
C13		M10
C14		M10
C15		M10
C16		M11
C17		J4
DJ1		A14
DJ2		A14
DJ3		K15
DJ4		K15
DJ5		J15
DQ1		G16
DQ2		G16
DQ3		H16
DQ4		H16
DQ5		H16
D1		M4
D2		M4
D3		L4
D4		L4
D5		G1
D6		H1
D7		G2
D8		H2
E1		L8

Name	Type	Pos
E2		H6
E3		H6
E4		K6
E5		L10
E6		M13
F1		J3
F2		J3
F3		L3
F4		L3
F5		M3
F6		M3
F7		J2
F8		L2
F9		M2
F10		J1
F11		L1
F12		M1
F12V+		A14
F12V-		A14
G1		M12
G2		M11
G3		C5
G4		C6
G5		C8
G6		H12
H1		H10
H2		G10
H3		G9
H4		G11
H5		H10
H6		G8
H7		H9
H8		G10
I1		G3
I2		J8
I3		H3
I4		F3
I5		G4
J1		H14
J2		J14
J3		H15
J4		J15
K1		J10
K2		J10
K3		J9
K4		J8
K5		L11
LABEL		O-1
L1		J11
L2		J11
L3		L11
M1		F1
M2		F2
M3		F3
M4		G3
M5		E3
M6		E2
M7		E1
M8		C1
M9		C2
N1		F8
N2		G6
N3		G6
N4		G13
N5		G5
N6		F6
N7		F6
O1		F9
O2		F8
O3		C9
O4		E6
O5		E6
P1		G14
P2		F14
P3		G15
P4		H13
P5		G14
P6		H14

Name	Type	Pos
Q1		L15
Q2		M15
Q3		M15
Q4		M14
Q5		L14
Q6		L14
Q7		M14
Q8		J13
Q9		J14
Q10		H11
Q11		L13
RB1		K12
RB2		H4
RB3		F4
RB4		H4
RC1		K4
RC2		L11
RC3		L11
RC4		L11
RC5		M6
RC6		M6
RC7		M6
RC8		M6
RC9		M6
RC10		M6
RC11		N6
RC12		N6
RE1		K7
RG1		D9
RH1		G9
RH2		H8
RH3		H9
RH4		G9
RH5		G10
RH6		G9
RH7		G10
RH8		H13
RI1		H4
RI2		D1
RI3		J3
RI4		H3
RI5		F3
RJ1		A15
RJ2		A14
RJ3		H16
RJ4		H16
RJ5		H16
RL1		J12
RM1		E2
RP1		G15
RP2		G15
RQ1		J13
RQ2		L15
RQ3		L15
RQ4		M15
RQ5		M15
RQ6		M16
RQ7		M15
RQ8		G16
RQ9		G16
RQ10		H16
RQ11		H16
RQ12		H16
RS1		D14
RS2		D14
RS3		D14
RS4		D14
RS5		D14
RS6		D14
RS7		E14
RS8		E14
RS9		E14
RT1		E12
RT2		E14
RT3		E14
RT4		E14
RT5		E14
RT6		E14

Component locations

PCB: SIOC | Issue: | Date:

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PRELIMINARY

Name	Type	Pos	Name	Type	Pos	Name	Type	Pos
RT7		E14						
RT8		E14						
RT9		E14						
RT10		E14						
R1		A4						
R2		A13						
R3		A12						
R4		A5						
R5		B13						
R6		B12						
R7		A5						
R8		C13						
R9		C12						
R10		A6						
R11		A7						
R12		B11						
R13		B11						
R14		A8						
R15		A11						
R16		A11						
R17		A9						
R18		A10						
SA1		A2						
SB1		J12						
SC1		M5						
SC2		L8						
SE1		G2						
SE2		L5						
SE3		M5						
SG1		M12						
SG2		M12						
SN1		E3						
SN2		G5						
SN3		F8						
SP1		F14						
SP2		H15						
SP3		H15						
SP4		H15						
SR1		C11						
SR2		C11						
SR3		C11						
SR4		C11						
SR5		C11						
SR6		C11						
SR7		C12						
SR8		C12						
SR9		C12						
SS1		B11						
SS2		A11						
SS3		E11						
SS4		E11						
ST1		F13						
ST2		F13						
ST3		F11						
ST4		F11						
S1		C10						
S2		E8						
S3		E13						
S4		E12						
S5		E11						
S6		E11						
S7		F10						
S8		E8						
S9		E10						
T1		F10						
T2		E9						
T3		F12						
T4		F13						
T5		F11						
T6		F11						
T7		E10						
3M20		K16						
3M50		C15						
3M60		C16						
20MHz		L12						

Component locations

PCB: SIOC | Issue: | Date:

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Type: RAM 0200

Data sheet no.: 4

Revision no.: 0

Date: 851015

General description:

The RAM 0200 is a 1 Mb dynamic RAM module with error correcting code ECC. RAM 0200 is controlled by CPU modules 0100 and 0101. RAM 0200 is organized as four blocks of memory each block 256 kb. The RAM is delivered with 1, 2 or 4 blocks of memory installed.

Interface to CPU modules:

In a Supermax system each CPU has its own private main memory. The main memory of a CPU consists of one or more RAM modules. The RAM modules are connected together with the associated CPU module by the local memory bus. The local memory busses are implemented in the mother board. RAM modules are placed in adjacent slots below their associated CPU module. Each time a memory module is added to the main memory the local memory bus is extended to the next lower slot. The order in which the memory modules are placed is arbitrary.

The RAM module is organized as 256 k double words of four bytes each. A double word consists of two words each 16 bit wide. A 16 bit word is extended with 6 ECC bits.

The CPU module controls the memory modules and takes care of error detection and correction. The CPU module executes the following cycles in memory modules:

Refresh cycle
Word read cycle
Word write cycle
double word read cycle
double word write cycle

The local memory bus is multiplexed between address and data. In the first part of a memory cycle the bus transfers address from the CPU module to the memory modules, and in the second part the bus transfers data between CPU module and memory modules.

Board lay out:

Board lay out is shown on page 5. The numbering of bits in a word is also shown on the drawing. Bit 16 to bit 21 is the error correcting code.

The rows contain the following addresses:

	ADDRESS RANGE (Byte addresses)	
ROW 0	000000-03FFFC	Even word addresses only
ROW 1	000002-03FFFE	Odd word addresses only
ROW 2	040000-07FFFC	Even word addresses only
ROW 3	040002-07FFFE	Odd word addresses only
ROW 4	080000-0BFFFC	Even word addresses only
ROW 5	080002-0BFFFE	Odd word addresses only
ROW 6	0C0000-0FFFFC	Even word addresses only
ROW 7	0C0002-0FFFFE	Odd word addresses only

Power requirements:

Voltage	Typ. current
+ 5 +-5%	1.0 A

Physical dimension:

Standard SUPERMAX module.

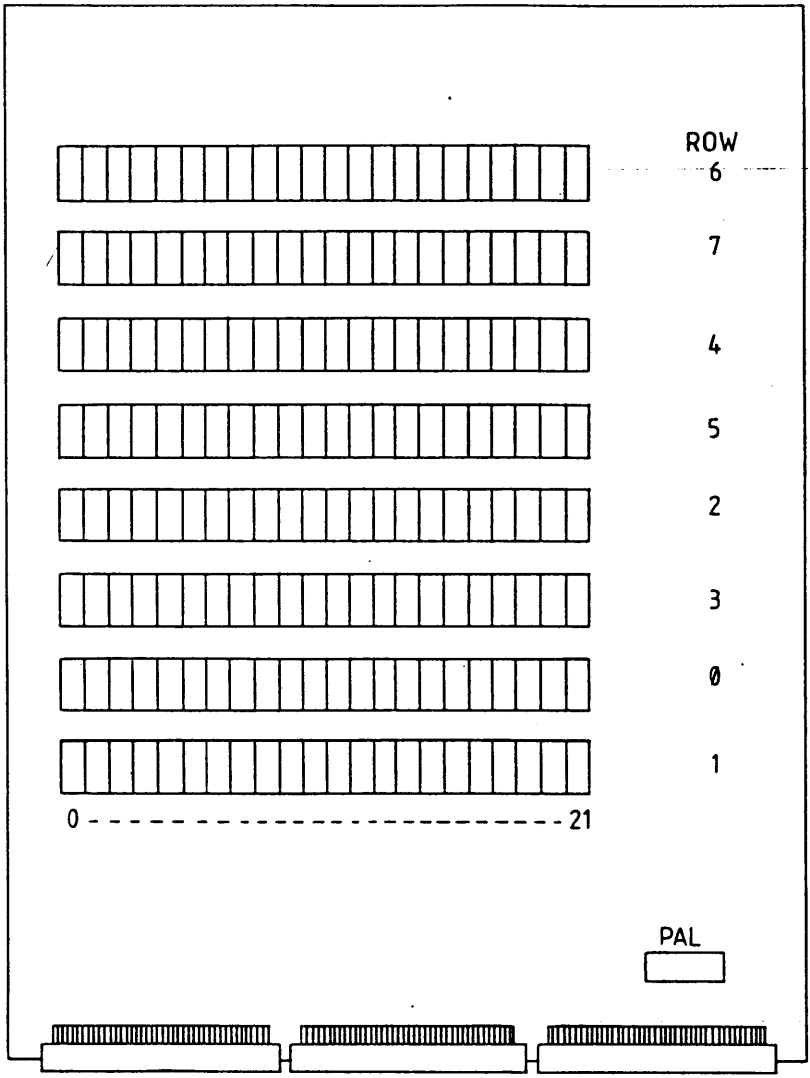
Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

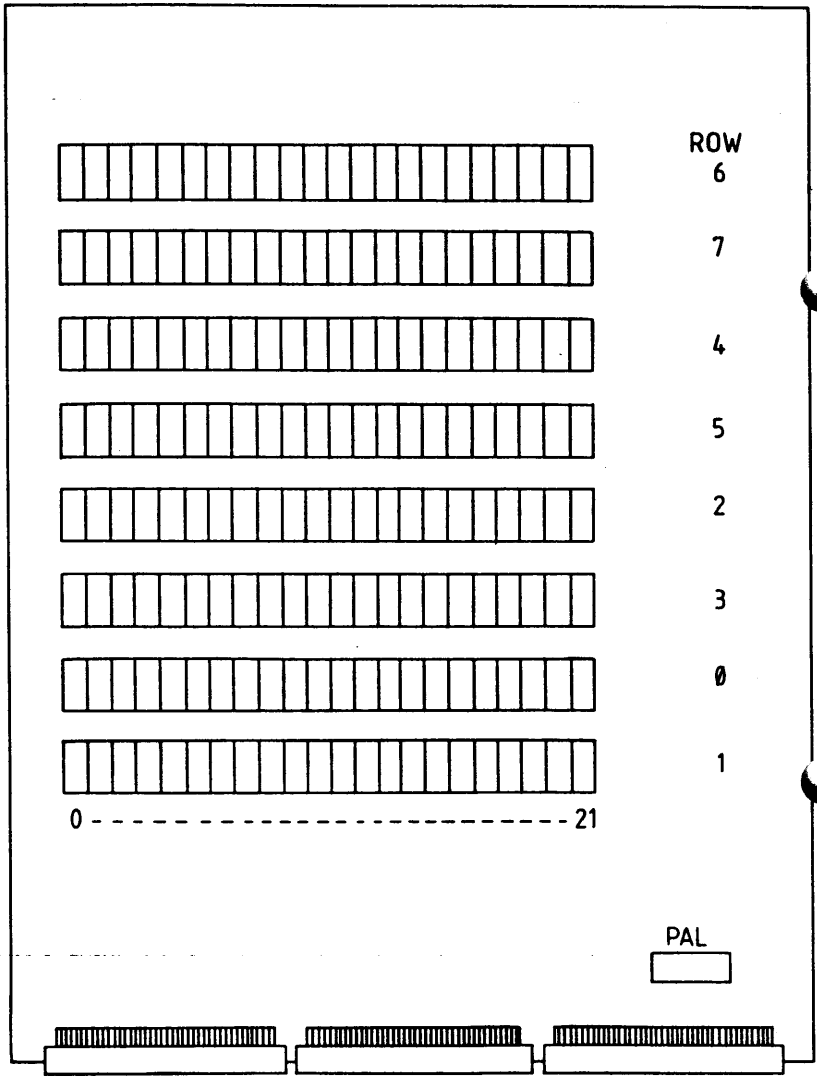
Installation:

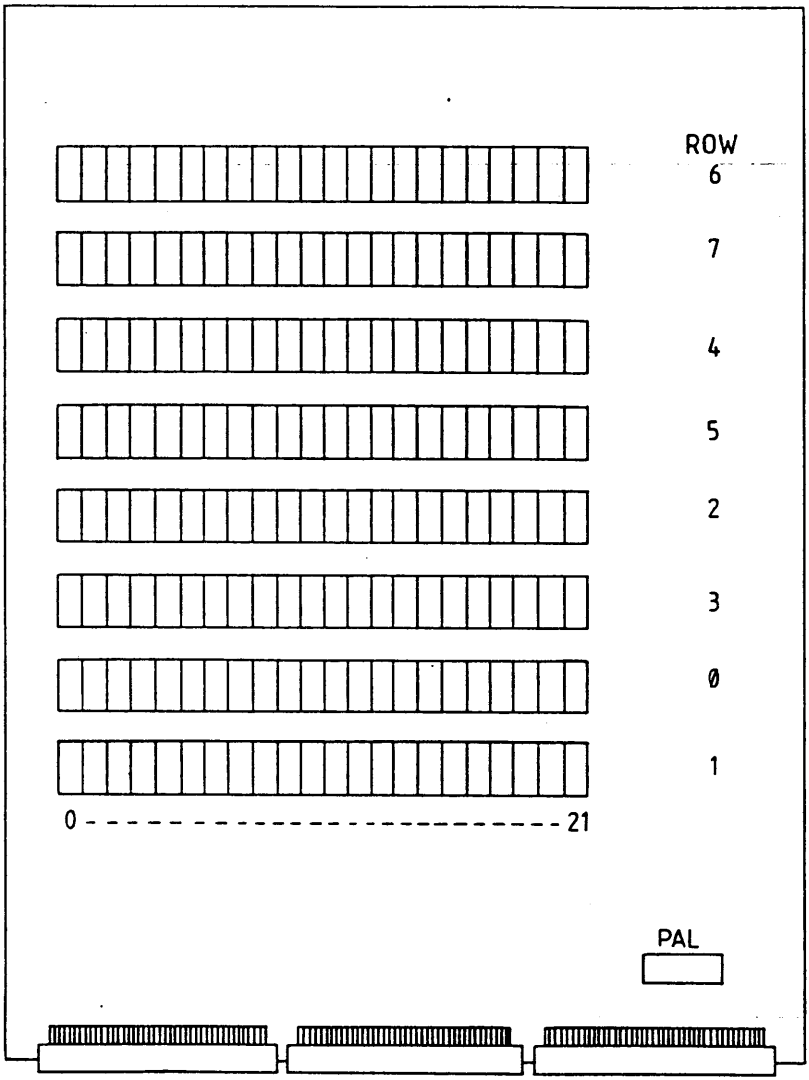
Before a RAM module is installed in a Supermax system the starting address of the module must be selected. The starting address of the module is coded in a PAL together with the amount of memory installed on the module.

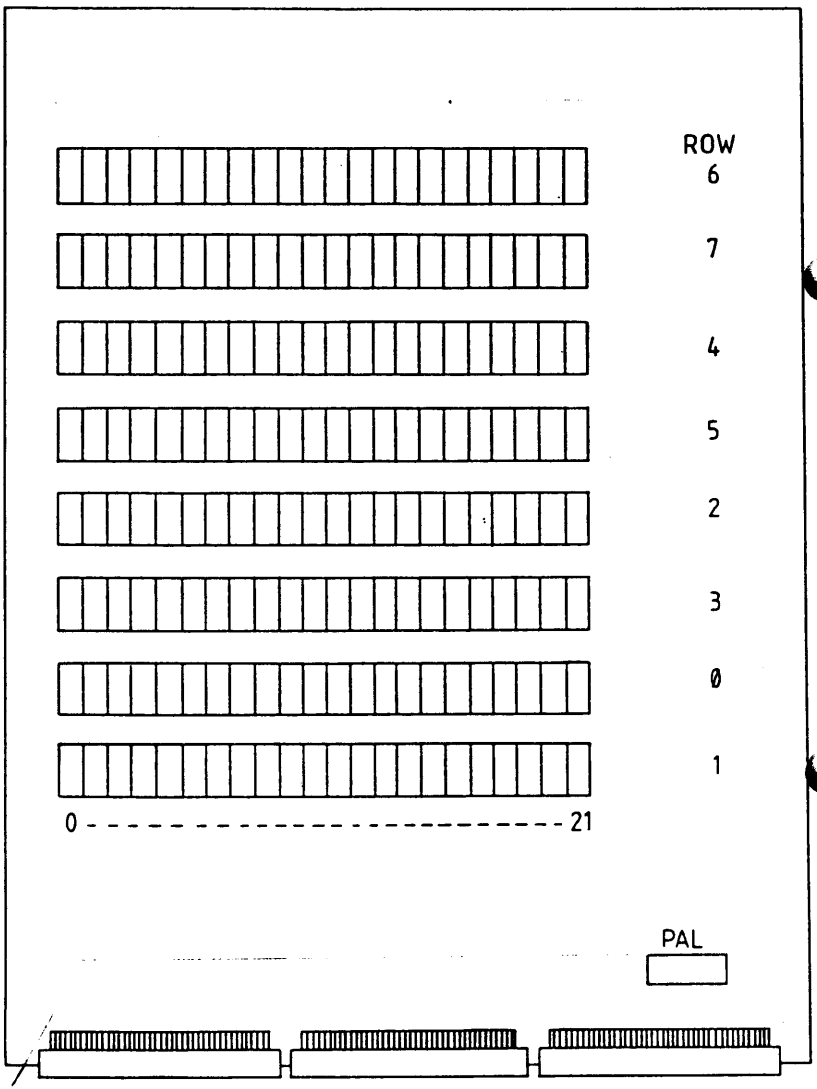
Lables on address PALs

Starting address	Size: 1 Mb	Size: 1/2 Mb
0 Mb	C180	C180H
1 Mb	C181	C181H
2 Mb	C182	C182H
3 Mb	C183	C183H
4 Mb	C184	C184H
5 Mb	C185	C185H
6 Mb	C186	C186H
7 Mb	C187	C187H
8 Mb	C188	C188H
9 Mb	C189	C189H
10 Mb	C18A	C18AH
11 Mb	C18B	C18BH
12 Mb	C18C	C18CH
13 Mb	C18D	C18DH
14 Mb	C18E	C18EH
15 Mb	C18F	C18FH


ROW
6
7
4
5
2
3
0
1
0
21
PAL


ROW
6
7
4
5
2
3
0
1
0
21
PAL


ROW
6
7
4
5
2
3
0
1
0
21
PAL


ROW
6
7
4
5
2
3
0
1
0
21
PAL

SUPERMAX technical data sheet.
Module: RAM 1400

Type: RAM 1400

Data sheet no.: 5

Revision no.: 0

Date: 851015

General description:

The RAM 1400 is a 4 Mb dynamic RAM module with error correcting code ECC. RAM 1400 is controlled by CPU modules 0100 and 0101. RAM 1400 is organized as four blocks of memory each block 1 Mb. The RAM is delivered with 1, 2, 3 or 4 blocks of memory installed.

Interface to CPU modules:

In a Supermax system each CPU has its own private main memory. The main memory of a CPU consists of one or more RAM modules. The RAM modules are connected together with the associated CPU module by the local memory bus. The local memory busses are implemented in the mother board. RAM modules are placed in adjacent slots below their associated CPU module. Each time a memory module is added to the main memory the local memory bus is extended to the next lower slot. The order in which the memory modules are placed is arbitrary. RAM modules type 1400 may be mixed with RAM modules type 0200 to implement the main memory of a CPU.

The RAM module is organized as 1 M double words of four bytes each. A double word consists of two words each 16 bit wide. A 16 bit word is extended with 6 ECC bits.

The CPU module controls the memory modules and takes care of error detection and correction. The CPU module executes the following cycles in memory modules:

Refresh cycle
Word read cycle
Word write cycle
double word read cycle
double word write cycle

The local memory bus is multiplexed between address and data. In the first part of a memory cycle the bus transfers address from the CPU module to the memory modules, and in the second part the bus transfers data between CPU module and memory modules.

Board lay out:

Board lay out is shown on page 5. The numbering of bits in a word is also shown on the drawing. Bit 16 to bit 21 is the error correcting code.

The rows contain the following addresses:

	ADDRESS RANGE (Byte addresses)	
ROW 0	000000-0FFFFC	Even word addresses only
ROW 1	000002-0FFFFE	Odd word addresses only
ROW 2	100000-1FFFFC	Even word addresses only
ROW 3	100002-1FFFFE	Odd word addresses only
ROW 4	200000-2FFFFC	Even word addresses only
ROW 5	200002-2FFFFE	Odd word addresses only
ROW 6	300000-3FFFFC	Even word addresses only
ROW 7	300002-3FFFFE	Odd word addresses only

Power requirements:

Voltage	Typ. current
+ 5 +-5%	2.0 A

Physical dimension:

Standard SUPERMAX module.

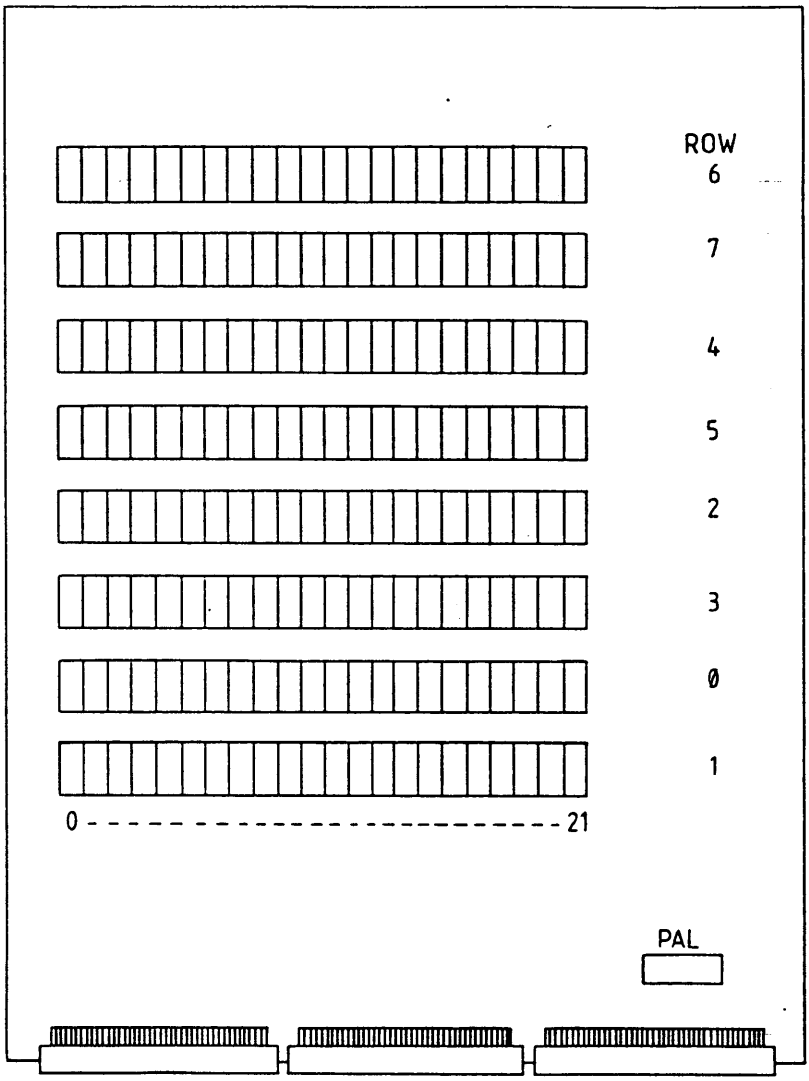
Width : 331 mm.
Depth : 415 mm.
Height: 14 mm.

Installation:

Before a RAM module is installed in a Supermax system the starting address of the module must be selected. The starting address of the module is coded in a PAL together with the amount of memory installed on the module.

Lables on address PALs

Starting address	Size: 1 Mb	Size: 2 Mb	Size: 3 Mb	Size: 4 Mb
0 Mb	M01	M02	M03	M04
4 Mb	M41	M42	M43	M44
8 Mb	M81	M82	M83	M84
12 Mb	MC1	MC2	MC3	MC4


ROW
6
7
4
5
2
3
0
1
0 - 21
PAL

Type: RAM 3000

Data sheet no.: 11

Revision no.: 0

Date: 861101

General description:

The RAM 3000 is a RAM mother module on which up to four RAM daughter modules can be placed. RAM 3000 contains data bus drivers/registers, refresh counter, address decoding logic, and connectors for RAM daughter modules. A data word in RAM 3000 contains 32 data bits. A 32 bit data word is organized as two 16 bit words, each with 6 check bits for the error correcting code, ECC. RAM 3000 is designed for 1 MB, 4 MB, and future 16 MB RAM daughter modules. RAM daughter modules of different sizes may be placed on the same RAM 3000 module. A daughter module signals its size to the mother module which calculates the starting address for the next following daughter module. The maximum amount of RAM on a RAM 3000 module is 16 MB. The maximum amount of RAM with RAM 3000 modules is also 16 MB.

RAM 3000 is controlled by CPU module 0100, 0101 or 3400.

Interface to CPU modules:

In a Supermax system each CPU has its own private main memory. The main memory of a CPU consists of one or more RAM modules. The RAM modules are connected to the associated CPU module by the local memory bus. The local memory bus is implemented in the mother board. RAM modules are placed in adjacent slots below their associated CPU module. Each time a memory module is added to the main memory the local memory bus is extended to the next lower slot.

The CPU module controls the memory modules and takes care of error detection and correction. The CPU module executes the following cycles in memory modules:

Refresh cycle
16 bit read cycle
16 bit write cycle
32 bit read cycle
32 bit write cycle

The local memory bus is multiplexed between address and data. In the first part of a memory cycle the bus transfers address from the CPU module to the memory modules, and in the second part the bus transfers data between the CPU module and the memory modules.

Board layout:

The daughter module board layout is shown on the last page.

When the board is used with CPU module 0100 and 0101 the following RAMs are used:

RAM0 - RAM15 : The first 16 bit word. Data bits D0 through D15.
RAM16 - RAM21 : ECC bits of the first 16 bit word.
RAM22 - RAM37 : The second 16 bit word. Data bits D16 through D23.
RAM38 - RAM43 : ECC bits of the second 16 bit word.

When the board is used with CPU module 3400 the following RAMs are used:

RAM0 - RAM31 : Data bits D0 through D31.
RAM32 - RAM38 : ECC bits.
RAM39 - RAM43 : Not used.

Power requirements:

Voltage	Typ. current
+ 5 Volt +-5%	2.0 A, including RAM daughter modules.

Installation:

The maximum amount of RAM on a RAM 3000 module is 16 MB.

The maximum amount of RAM with RAM 3000 modules is 16 MB.

The starting address of a RAM 3000 module is selected by a strap. Available start adresses are 0, 4, 8 and 12 MB. The strap is located between the bus connector and ICF. The strap is called SW1 and pin 6 is near ICF pin 1.

Four RAM daughter modules can be placed on a RAM 3000 module. The position closest to the motherboard is called position 0. In the following table a "1" indicates that a RAM 3200 daughter modules is installed. A RAM 3200 module holds 1 Mbyte of memory. A "4" indicates that a RAM 3300 daughter module is installed. RAM 3300 holds 4 Mbyte of memory. A "0" indicates that no module is installed.

When the board is strapped to start address 0 Mbyte, the board can be mounted with the following RAM daughter modules:

Position 0:	4	4	4	4
Position 1:	0 or 1	4	4	4
Position 2:	0 or 1	0 or 1	4	4
Position 3:	0 or 1	0 or 1	0 or 1	4

or

Position 0:	1	1	1	1
Position 1:	0	1	1	1
Position 2:	0	0	1	1
Position 3:	0	0	0	1

Pin numbers:

```
Pin 6   * * *
Pin 1   * * *
         SW1
```

Start address: 0 MB, pin 4 connected to 5 and pin 2 connected to 3.

```
      * *_*
Pin 1 * *_*
       SW1
```

When the board is strapped to start address 4 Mbyte, the board can be mounted with the following RAM daughter modules:

Position 0:	4	4
Position 1:	0	4
Position 2:	0	0
Position 3:	0	0

or

Position 0:	1	1	1	1
Position 1:	0	1	1	1
Position 2:	0	0	1	1
Position 3:	0	0	0	1

Pin numbers:

```
Pin 6   * * *
Pin 1   * * *
         SW1
```

Start address: 4 MB, pin 5 connected to 6 and pin 2 connected to 3.

```
      *_* *
Pin 1 * *_*
       SW1
```

When the board is strapped to start address 8 Mbyte, the board can be mounted with the following RAM daughter modules:

Position 0:	4
Position 1:	0
Position 2:	0
Position 3:	0

or

Position 0:	1	1	1	1
Position 1:	0	1	1	1
Position 2:	0	0	1	1
Position 3:	0	0	0	1

Pin numbers:

```
Pin 6   * * *
Pin 1   * * *
         SW1
```

Start address: 8 MB, pin 4 connected to 5 and pin 1 connected to 2.

```
      * *_*
Pin 1 *_* *
```

When the board is strapped to start address 12 Mbyte, the board can be mounted with the following RAM daugther modules:

Position 0:	1	1	1	1
Position 1:	0	1	1	1
Position 2:	0	0	1	1
Position 3:	0	0	0	0

No 4 Mbyte daughter modules.

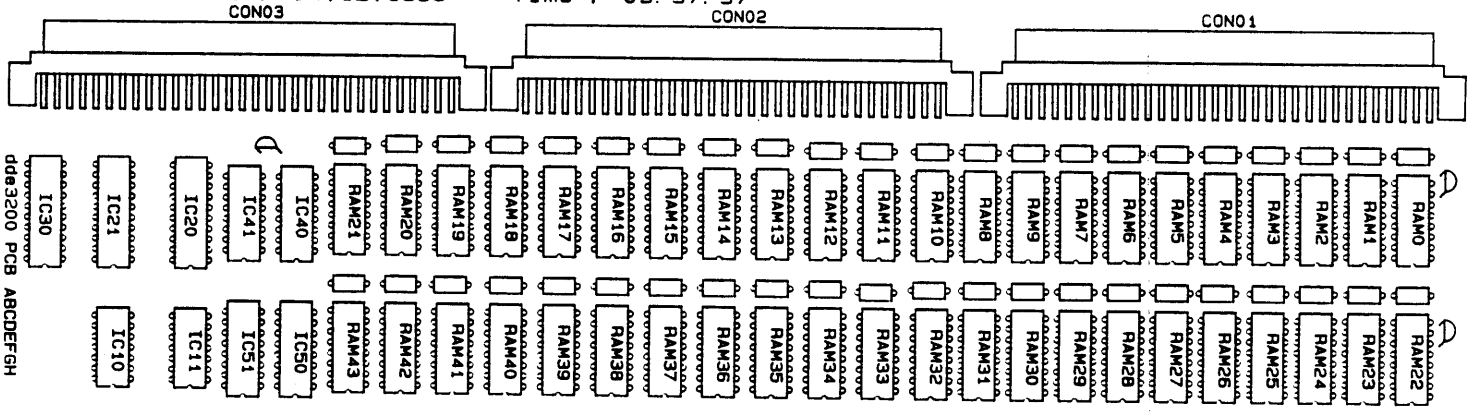
Pin numbers:

```
Pin 6   * * *
Pin 1   * * *
         SW1
```

Start address: 12 MB, pin 5 connected to 6 and
pin 1 connected to 2.

```
        *_* *
Pin 1   *_* *
         SW1
```

DDE3200 Date : 04.12.1986 Time : 09: 57: 57



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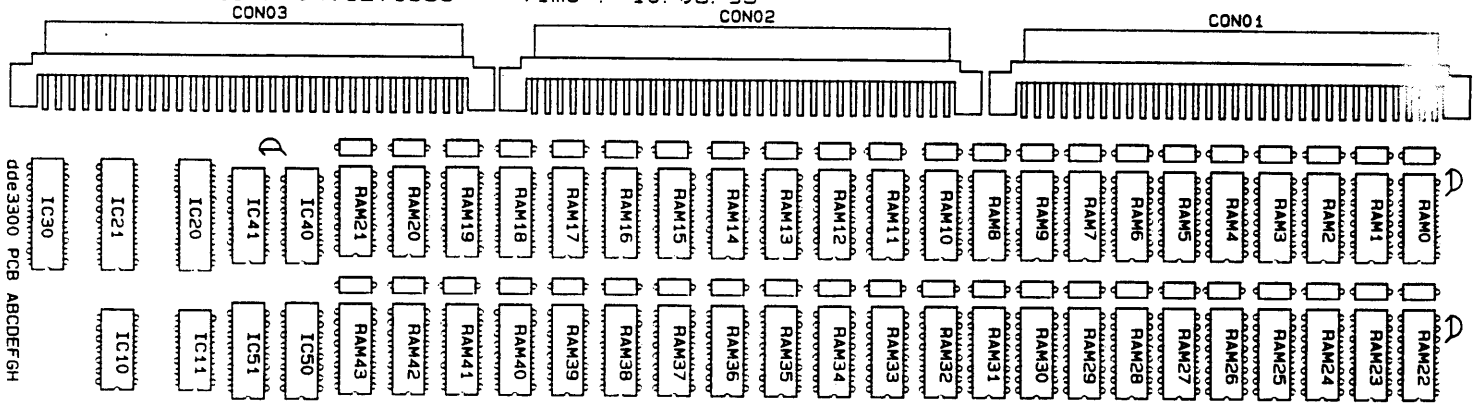
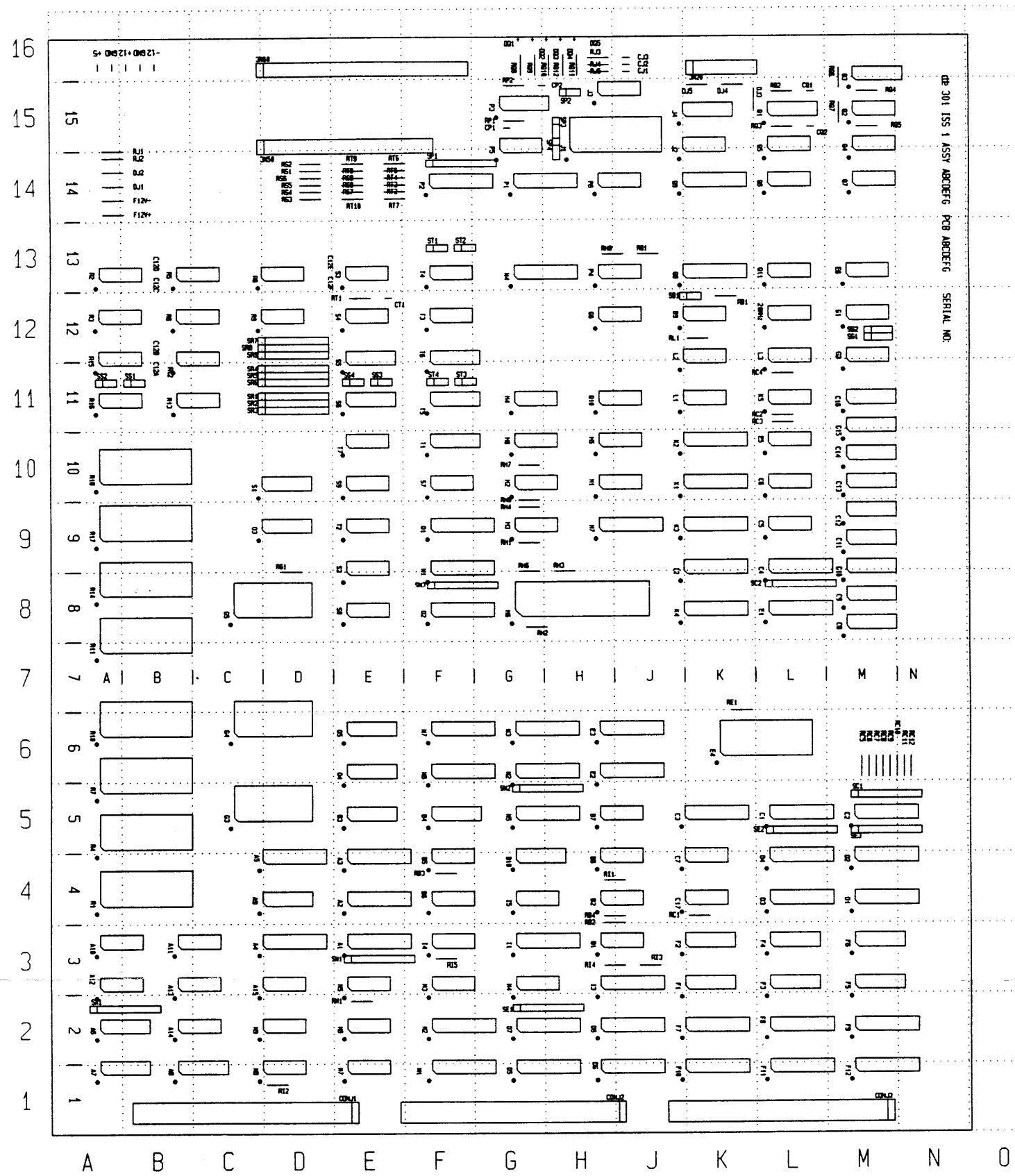


PRELIMINARY



Component locations

PCB: SIOC	Issue:	Date:	dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11

Name	Type	Pos
CG00	74ALS573	G2
CG01	74ALS573	H2
CG02	74ALS573	G2
CG03	74ALS573	H2
CG04	PAL-20L8A	F2
CG05	PAL-16R4A	C2
CG06	PAL-16R4A	E2
CG07	74ALS573	F2
CG08	74ALS138	E2
CG09	NS16081-6	H3
CG10	OSC.6MHz	A2
CG11	7407	C3
CG12	HD63484-8	E3
CG13	74ALS11	A3
CG14	PAL-20R8A	C3
CG17	74ALS138	A3
CG18	74ALS138	B4
CG19	74ALS645	G5
CG20	74ALS645	F4
CG21	74ALS573	G4
CG22	74ALS573	E4
CG23	74ALS573	G4
CG24	74ALS573	F4
CG25	74AS32	C5
CG26	74AS32	B5
CG27	74AS08	A5
CG28	74AS08	A5
CG29	74AS08	A3
CG30	74AS08	B5
CG31	74AS08	C5
CG32	PAL-16R4B	C3
CG33	74ALS573	B3
CG34	74ALS138	J5
CG35	74ALS573	H4
CG36	74ALS573	E4
CG37	74ALS573	F5
CG38	74ALS573	G5
CG39	74S163	B3
CG40	uPD41264-12	A7
CG41	uPD41256-12	A9
CG42	uPD41256-12	E7
CG43	uPD41256-12	E9
CG44	uPD41256-12	C7
CG45	uPD41256-12	C9
CG46	uPD41256-12	G7
CG47	uPD41256-12	G9
CG48	74AS04	A2
CG49	74S163	J5
CG50	uPD41256-12	B7
CG51	uPD41256-12	B9
CG52	uPD41256-12	F7
CG53	uPD41256-12	F9
CG54	uPD41256-12	D7
CG55	uPD41256-12	D9
CG56	uPD41256-12	H7
CG57	uPD41256-12	H9
CG58	74S163	E5
CG59	74S163	C4
CG60	uPD41256-12	B7
CG61	uPD41256-12	B9
CG62	uPD41256-12	F7
CG63	uPD41256-12	F9
CG64	uPD41256-12	D7
CG65	uPD41256-12	D9
CG66	uPD41256-12	H7
CG67	uPD41256-12	H9
CG68	74ALS74	B3
CG69	14P-STRAP	B2
CG70	uPD41256-12	C7
CG71	uPD41256-12	C9

Name	Type	Pos
CG72	uPD41256-12	G7
CG73	uPD41256-12	G9
CG74	uPD41256-12	E7
CG75	uPD41256-12	E9
CG76	uPD41256-12	J7
CG77	uPD41256-12	J9
CG78	74ALS645	H4
CG79	74LS169B	B2
CG80	74LS169B	C2
CG81	PAL-16R8A	C4
CG82	74ALS112	B4
Cbb	10uF/16V-Sol.Al	D2
C1	100nF	G12
C2	150pF	G12
C3	100nF	G12
C4	150pF	G12
C5	100nF	G13
C6	150pF	G13
C7	100nF	G13
C8	150pF	G13
C9	100nF	G14
C10	150pF	G14
C11	100nF	G14
C12	150pF	G14
DECLHI	1N4002	C13
EG0	10H424P	A9
EG1	10H424P	A10
EG2	10H424P	B9
EG3	10H424P	B10
EG4	10H424P	C9
EG5	10H424P	C10
EG6	10H424P	D9
EG7	10H424P	D10
EG8	10H141P	A9
EG9	10H141P	A10
EG10	10H141P	B9
EG11	10H141P	B10
EG12	10H141P	C9
EG13	10H141P	C10
EG14	10H141P	D9
EG15	10H141P	D10
ERb1	SIL-5x82R	A10
ERb2	SIL-5x82R	A11
ERb3	SIL-5x82R	B10
ERb4	SIL-5x82R	B11
ERb5	SIL-5x82R	C10
ERb6	SIL-5x82R	C11
ERb7	SIL-5x82R	E10
ERb8	SIL-5x82R	E11
ERb9	82R	D12
ERb10	SIL-5x82R	F10
ERb11	SIL-5x82R	F11
ERb12	SIL-5x82R	E14
ERb13	SIL-5x82R	E14
ERb14	SIL-5x82R	D14
ERb15	SIL-5x82R	J12
ERb16	SIL-5x82R	J13
ERb17	SIL-5x82R	J12
ERb18	SIL-5x82R	J10
ERb19	82R	F9
ERb20	SIL-5x82R	J9
ERb21	SIL-5x82R	H11
ERb22	SIL-5x82R	C11
ERb23	SIL-5x82R	H12
ERb24	SIL-5x82R	C12
ERb25	SIL-5x82R	A12
ERb28	SIL-5x82R	D12
ERb29	SIL-5x82R	C12
ERb30	SIL-5x82R	B12
ERb31	SIL-5x82R	F14

Name	Type	Pos
ERb35	82R	J11
ERb36	SIL-5x82R	G11
ERb37	82R	D9
ERb38	SIL-5x82R	J10
ERb39	82R	C13
ERb40	560R	F10
ERb41	SIL-5x82R	D13
ERb45	SIL-5x82R	H13
ERb48	560R	B13
ERb51	SIL-5x82R	F11
ERb53	SIL-5x82R	F10
ERe1	560R	F10
ERe2	560R	F10
ERe3	560R	F9
ERe4	560R	E12
ERe5	SIL-5x470R	D11
IC1	74AS04	F10
IC2	10H124P	E10
IC3	10H124P	E9
IC4	10H424P	B12
IC5	10H424P	B12
IC6	10H124P	H12
IC7	MCM422L10	D13
IC8	AM8151DC	E11
IC9	AM8151DC	E12
IC10	AM8151DC	E13
IC11	10H125P	H13
IC12	74ALS541	H13
IC13	OSC.80MHz	A4
IC14	10H124P	D11
IC15	10H136P	C12
IC16	10H125P	A12
IC17	10H113P	C13
IC18	10H136P	B11
IC19	10H141P	C11
IC20	10H103P	C12
IC21	10H424P	J9
IC22	10H136P	J12
IC23	10H104P	J11
IC24	10H103P	J11
IC25	10H103P	J12
IC26	10H131P	D12
IC26-1	10H113P	D12
IC27	10H124P	H10
IC28	10H113P	H11
IC29	10H131P	H11
IC30	10H131P	F11
IC31	10H124P	H9
IC32	10H124P	F9
IC33	10H136P	J10
IC34	10H136P	J9
IC35	10H141P	H9
IC36	74AS08	H12
IC37	10H141P	F9
IC38	74S00	A5
IC39	74ALS32	A12
IC40	10H124P	B13
IC41	10H125P	A11
IC44	10H158P	E11
IC45	10H158P	E9
J1	INT.BUS-96p-DIN	J1
J1.1	INT.BUS-96p-DIN	J1
J2	INT.BUS-96p-DIN	D1
J2.1	INT.BUS-96p-DIN	D1
L1	COIL	H13
L2	COIL	H13
L3	COIL	H13
RCL1	47R	A11
RCL2	47R	B11
RCL3	47R	A11

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Issue	Date
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dde 2600

Component Locations

Parts no

Dwg. no.

2

Type: RAM 3100

Data sheet no.: 10

Revision no.: 0

Date: 861029

General description:

The RAM 3100 is a RAM mother module on which up to four RAM daughter modules can be placed. RAM 3100 contains data bus drivers/registers, refresh counter, address decoding logic, and connectors for RAM daughter modules. A data word in RAM 3100 contains 32 data bits and 7 check bits for the error correcting code, ECC. RAM 3100 is designed for 1 MB, 4 MB, and future 16 MB RAM daughter modules. RAM daughter modules of different sizes may be placed on the same RAM 3100 module. A daughter module signals its size to the mother module which calculates the starting address for the next following daughter module. The starting address of a module must be divisible with the size of the module which is easily achieved by placing the largest modules first. The first RAM daughter module is placed closest to the bus connectors on RAM 3100.

RAM 3100 is controlled by CPU module 3400. RAM 3400 cannot be controlled by CPU modules 0100 and 0101.

Interface to CPU modules:

In a Supermax system each CPU has its own private main memory. The main memory of a CPU consists of one or more RAM modules. The RAM modules are connected to the associated CPU module by the local memory bus. The local memory bus is implemented in

the mother board. RAM modules are placed in adjacent slots below their associated CPU module. Each time a memory module is added to the main memory the local memory bus is extended to the next lower slot. The starting address of RAM module number N is calculated by RAM module N-1 as the starting address of RAM module N-1 plus the sum of the sizes of all daughter modules placed on RAM module N-1. The starting address is transferred on the local memory bus from module N-1 to module N. The starting address for the first memory module, closest to the CPU module, is zero.

The CPU module controls the memory modules and takes care of error detection and correction. The CPU module executes the following cycles in memory modules:

Refresh cycle
32 bit read cycle
32 bit write cycle
nibble mode read cycle

The local memory bus is multiplexed between address and data. In the first part of a memory cycle the bus transfers address from the CPU module to the memory modules, and in the second part the bus transfers data between the CPU module and the memory modules.

Board layout:

The daughter module board layout is shown on the last page.

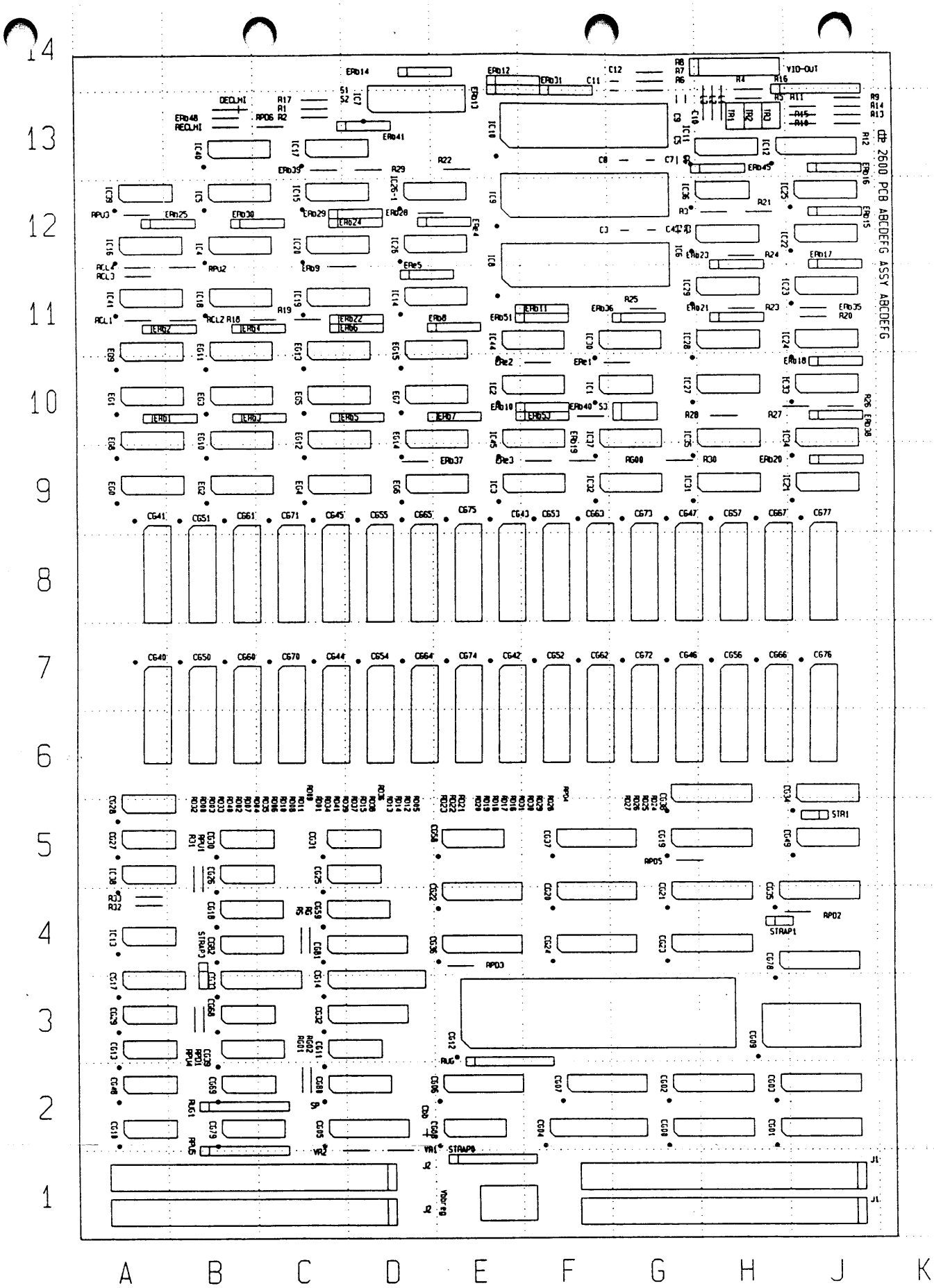
RAM0 - RAM31 : Data bits D0 through D31.
RAM32 - RAM38 : ECC bits.
RAM39 - RAM43 : Not used.

Power requirements:

Voltage	Typ. current
+ 5 Volt +-5%	2.0 A, including RAM daughter modules.

Installation:

The starting address of a RAM 3100 module is calculated by the preceding RAM 3100 modules in a memory system, so there is no need to change address switches, straps or address decoding PALs. If a memory system is implemented with RAM 3100 and RAM daughter modules of different sizes, the RAM daughter modules should be placed in the order of decreasing size, that is with the largest modules first.



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dde 2600

Component-ID

Parts no

Dwg no

Name	Type	Pos
RCL4	47R	A12
RD00	33R	B5
RD01	33R	C5
RD02	33R	B5
RD03	33R	B5
RD04	33R	C5
RD05	33R	D5
RD06	33R	C5
RD07	33R	B5
RD08	33R	C5
RD09	33R	C5
RD10	33R	C5
RD11	33R	C5
RD12	33R	D5
RD13	33R	D5
RD14	33R	D5
RD15	33R	D5
RD16	33R	E5
RD17	33R	E5
RD18	33R	E5
RD19	33R	E5
RD20	33R	E5
RD21	33R	E5
RD22	33R	E5
RD23	33R	E5
RD24	33R	G5
RD25	33R	G5
RD26	33R	G5
RD27	33R	G5
RD28	33R	F5
RD29	33R	F5
RD30	33R	F5
RD31	33R	F5
RD32	33R	B5
RD33	33R	B5
RD34	33R	C5
RD35	33R	C5
RD36	33R	D5
RD37	33R	D5
RD38	33R	D5
RD39	33R	D5
RD40	33R	B6
RD41	33R	C6
RECLHI	1K2	B13
RG	47R	C4
RG00	1K	G9
RG01	270R	C2
RG02	2K7	C3
RPD1	33R	B3
RPD2	33R	J4
RPD3	33R	E4
RPD4	33R	F6
RPD5	33R	H5
RPD6	33R	C13
RPU1	1K	B5
RPU2	1K	B12
RPU3	1K	A12
RPU4	1K	B3
RPU5	SIL-9x3K3	B2
RS	47R	C4
RUG	SIL-9x3K3	E3
RUG1	SIL-9x3K3	B2
R1	Not-mounted	C13
R2	Not-mounted	C13
R3	1K96-1%-MR25	H12
R4	1K96-1%-MR25	H14
R5	1K96-1%-MR25	H13
R6	Not-mounted	G14
R7	Not-mounted	G14
R8	Not-mounted	G14

Name	Type	Pos
R9	68R	J13
R10	68R	J13
R11	68R	J13
R12	68R	J13
R13	68R	J13
R14	68R	J13
R15	68R	J13
R16	SIL-9x150R	H14
R17	560R	C13
R18	560R	B11
R19	560R	C11
R20	560R	J11
R21	560R	H12
R22	560R	E13
R23	560R	H11
R24	560R	H12
R25	560R	G11
R26	560R	J10
R27	560R	J10
R28	560R	H10
R29	560R	D13
R30	560R	G9
R31	1K	B4
R32	33R	A4
R33	33R	A4
SP	STRAP	C2
STRAP0	STRAP	E1
STRAP1	STRAP	H4
STRAP3	STRAP	B4
STR1	STRAP	J5
S1	STRAP	D13
S2	STRAP	D13
S3	STRAP	G10
TR1	TR.POT-500R	H13
TR2	TR.POT-500R	H13
TR3	TR.POT-500R	H13
VID-OUT	20P-HEADER	H14
VR1	301R-1%-MR25	D2
VR2	562R-1%-MR25	C2
Vbbreg	LM337KC	E1
cbb1	100nF-Cer	B11
cbb2	100nF-Cer	A11
cbb3	100nF-Cer	A10
cbb4	100nF-Cer	B10
cbb5	100nF-Cer	C10
cbb6	100nF-Cer	D10
cbb7	100nF-Cer	D11
cbb8	100nF-Cer	C11
cbb9	100nF-Cer	A12
cbb10	100nF-Cer	B12
cbb11	100nF-Cer	C12
cbb12	100nF-Cer	D12
cbb13	100nF-Cer	J10
cbb14	100nF-Cer	J12
cbb15	100nF-Cer	J13
cbb16	100nF-Cer	G12
cbb17	100nF-Cer	J9
cbb18	100nF-Cer	E10
cbb19	100nF-Cer	E11
cbb20	100nF-Cer	F11
cbb21	100nF-Cer	J12
cbb22	100nF-Cer	J10
cbb23	100nF-Cer	G11
cbb24	100nF-Cer	D14
cbb25	100nF-Cer	F14
cbb26	100nF-Cer	E14
cbb27	100nF-Cer	C13
cxx1	10uF/16V-Sol.Al	A2
cxx2	100nF-Cer	A2
cxx3	100nF-Cer	A3

Name	Type	Pos
cxx4	100nF-Cer	A4
cxx5	100nF-Cer	A4
cxx6	100nF-Cer	A5
cxx7	100nF-Cer	A5
cxx8	100nF-Cer	A6
cxx9	100nF-Cer	A7
cxx10	100nF-Cer	A7
cxx12	100nF-Cer	A8
cxx13	100nF-Cer	A9
cxx14	100nF-Cer	A10
cxx15	100nF-Cer	A10
cxx16	100nF-Cer	A11
cxx17	100nF-Cer	A11
cxx18	100nF-Cer	A12
cxx19	100nF-Cer	A13
cxx20	100nF-Cer	A13
cxx23	100nF-Cer	K13
cxx24	100nF-Cer	K13
cxx25	100nF-Cer	K12
cxx26	100nF-Cer	K11
cxx27	100nF-Cer	K11
cxx28	100nF-Cer	K10
cxx29	100nF-Cer	K10
cxx30	100nF-Cer	K9
cxx31	100nF-Cer	K8
cxx33	100nF-Cer	K7
cxx34	100nF-Cer	K7
cxx35	100nF-Cer	K6
cxx36	100nF-Cer	K5
cxx37	100nF-Cer	K5
cxx38	100nF-Cer	K4
cxx39	100nF-Cer	K4
cxx40	100nF-Cer	K3
cxx41	100nF-Cer	K2
cxx42	100nF-Cer	K2
cyy2	100nF-Cer	C9
cyy3	100nF-Cer	D9
cyy4	100nF-Cer	E9
cyy5	100nF-Cer	F9
cyy6	100nF-Cer	G9
cyy7	100nF-Cer	H9
cyy9	100nF-Cer	C10
cyy10	100nF-Cer	D10
cyy11	100nF-Cer	E10
cyy12	100nF-Cer	F10
cyy13	100nF-Cer	G10
cyy14	100nF-Cer	H10
cyy16	100nF-Cer	C10
cyy17	100nF-Cer	D10
cyy18	100nF-Cer	E10
cyy19	100nF-Cer	F10
cyy20	100nF-Cer	G10
cyy21	100nF-Cer	H10
cyy22	100nF-Cer	E12
cyy23	100nF-Cer	C11
cyy24	100nF-Cer	D11
cyy25	100nF-Cer	E11
cyy26	100nF-Cer	F11
cyy27	100nF-Cer	G11
cyy28	100nF-Cer	H11
cyy29	100nF-Cer	E13
cyy30	100nF-Cer	C11
cyy31	100nF-Cer	D11
cyy32	100nF-Cer	H11
cyy33	100nF-Cer	E13
cyy34	100nF-Cer	C12
cyy35	100nF-Cer	D12
cyy36	100nF-Cer	H12
cyy37	100nF-Cer	C13
cyy38	100nF-Cer	D13

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dde 2600

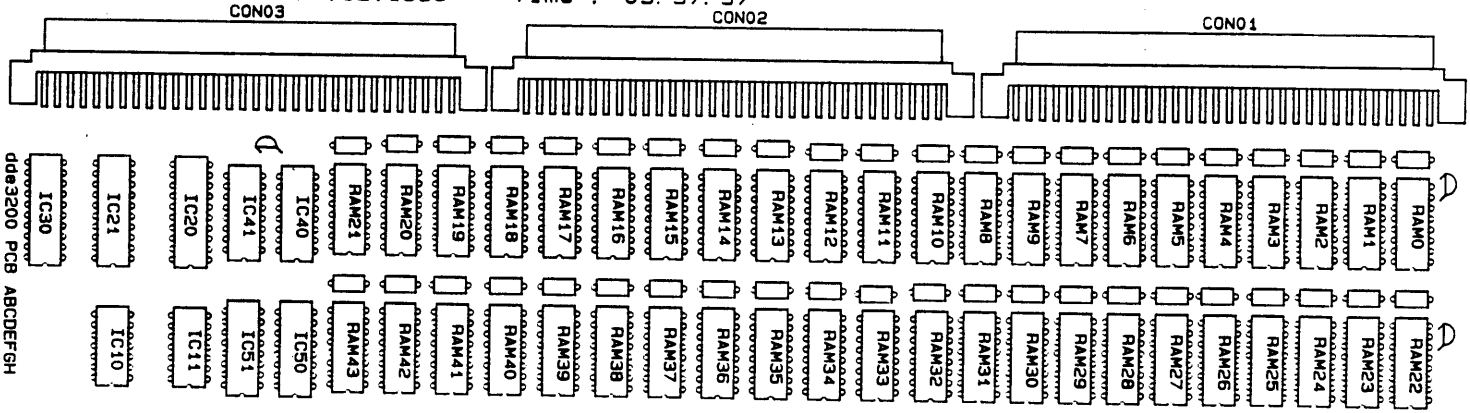
Component Locations

Parts no.

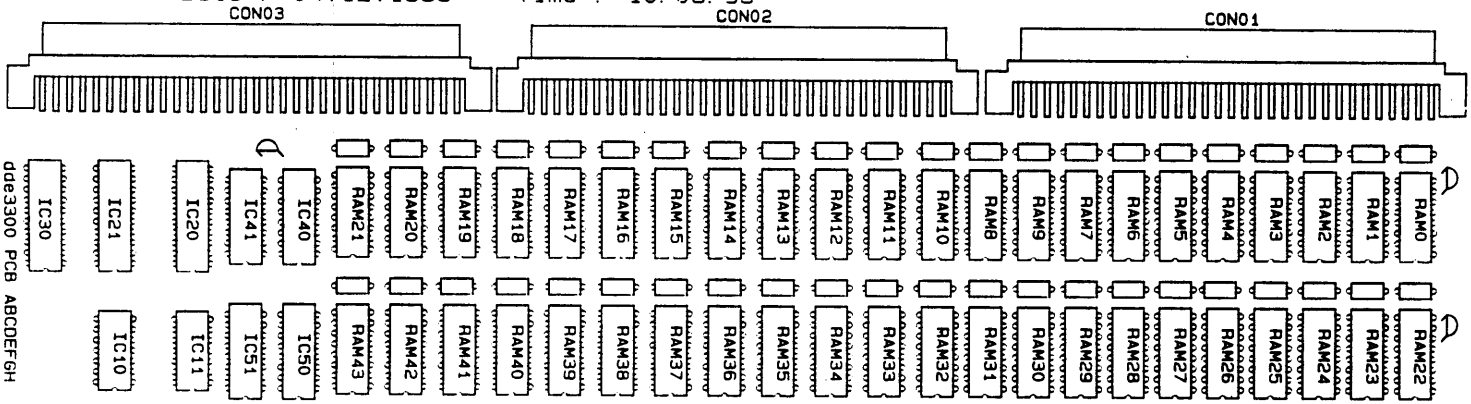
Dwg. no.

3

DDE3200 Date : 04.12.1986 Time : 09: 57: 57



DDE3300 Date : 04.12.1986 Time : 10:08:55



dde3300 PCB ABCDEFGH

Type: RAM module 3200

Data sheet no.: 13

Revision no.: 0

Date: 861201

General description:

The RAM 3200 is a RAM daughter module. The module containes 44 256 kbit nibble mode dynamic RAMs and drivers for address and control signals. The RAM is organized as two words each 22 bits wide including error correcting bits. The total amount of RAM is 1 Mbyte.

1 to 4 RAM 3200 modules fit into RAM mother module 3000 or 3100.

Installation:

A daughter module signals its size to the mother module which calculates the starting address for the next following daughter module. No strapping is needed.

CON01
CON02
CON03
RAM0
RAM1
RAM2
RAM3
RAM4
RAM5
RAM6
RAM7
RAM9
RAM8
RAM10
RAM11
RAM12
RAM13
RAM14
RAM15
RAM16
RAM17
RAM18
RAM19
RAM20
RAM21
RAM22
RAM23
RAM24
RAM25
RAM26
RAM27
RAM28
RAM29
RAM30
RAM31
RAM32
RAM33
RAM34
RAM35
RAM36
RAM37
RAM38
RAM39
RAM40
RAM41
RAM42
RAM43
IC40
IC41
IC20
IC21
IC30
IC50
IC51
IC11
IC10
dde3200 PCB ABCDEFGH
DDE3200
Date : 04.12.1986
Time : 09:57:57

Type: RAM module 3300

Data sheet no.: 14

Revision no.: 0

Date: 861201

General description:

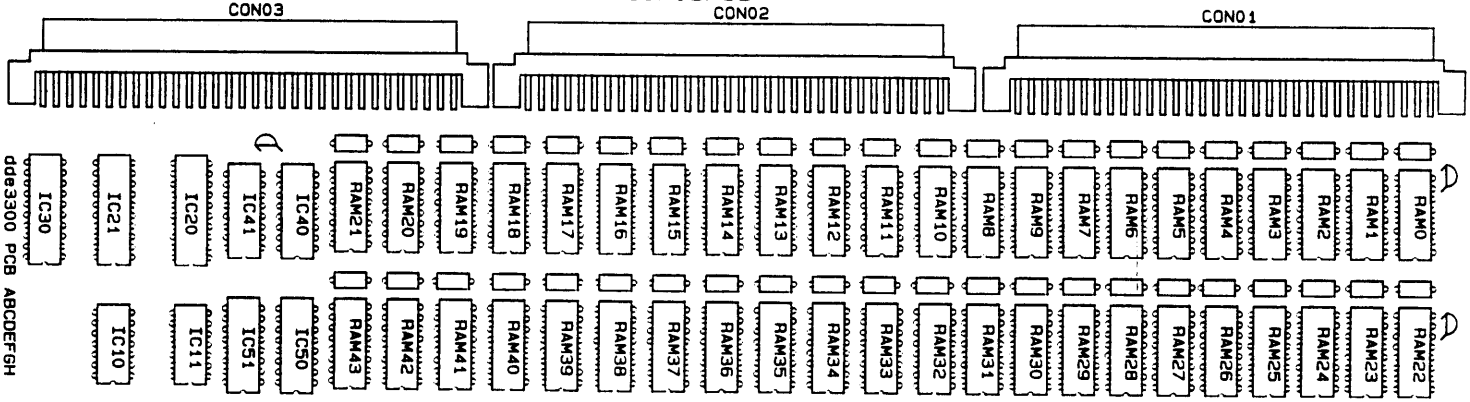
The RAM 3300 is a RAM daughter module. The module containes 44 1 Mbit nibble mode dynamic RAMs and drivers for address and control signals. The RAM is organized as two words each 22 bits wide including error correcting bits. The total amount of RAM is 4 Mbyte.

1 to 4 RAM 3300 modules fit into RAM mother module 3000 or 3100.

Installation:

A daughter module signals its size to the mother module which calculates the starting address for the next following daughter module. No strapping is needed.

DDE3300 Date : 04.12.1986 Time : 10:08:55



SECTION 1.2

Supermax Technical Data Sheet

Supermax Technical Data Sheet

Type:	Memory mother module 4400
Data sheet no:	19
Revision no:	0
Date:	90-05-07

General Description

The memory mother module 4400 is a module on which up to four daughter modules can be placed. The module contains data bus drivers/registers, refresh counter, address decoding logic, and connectors for daughter modules. A data word in the mother module contains 32 data bits and 7 check bits for the error correcting code, ECC.

The mother module is designed for 1 Mb, 4 Mb and 16 Mb daughter modules. Because of the memory layout of mother module 4400, called **Two-way Interleave**, an even number of daughter modules must be mounted. Two consecutive daughter modules must have the same size, and are called a memory block. Two memory blocks of different sizes may be placed on the same mother module. A memory block signals its size to the mother module which calculates the starting address for the next following memory block. The starting address of a memory block must be divisible with the size of the memory block which is easily achieved by placing the largest memory blocks first. The first memory block is placed closest to the bus connectors on mother module 4400.

NOTE: Memory mother module 4400 is controlled by the CPU R3000 module only and must be mounted with at least two daughter modules.

Interface to CPU modules

In a Supermax system each CPU has its own main memory. The main memory of a CPU consists of one or more memory mother modules. The memory mother modules are connected to the CPU module by the local memory bus. The local memory bus is implemented in the mother board. Memory mother modules are placed in adjacent slots below their CPU module. Each time a memory mother module is added to the main memory the local memory bus is extended to the next lower slot.

The CPU module controls the memory modules and takes care of error detection and correction. The CPU module executes the following cycles in memory modules:

Refresh cycle
32 bit read cycle
32 bit write cycle
Read-modify-write cycle
Burst mode read cycle
Burst mode write cycle

The local memory bus is multiplexed between address and data. In the first part of a memory cycle the bus transfers the address from the CPU module to the memory modules, and in the second part the bus transfers the data between the CPU module and the memory modules.

Switches

The starting address for the first memory module, closest to the CPU module, must be zero. Memory mother module 4400 decodes 28 address bits corresponding to 256 Mb. The starting address of a mother module 4400 is set by rotating two 4 bit hexadecimal switches, SW1 and SW2.

SW2 Sets bit (27:24) of the starting address. Corresponds to 16 Mb increments.

SW1 Sets bit (23:20) of the starting address. Corresponds to 1 Mb increments.

Example: SW2 is set to 1 and SW1 is set to 8. The starting address will be 1 × 16 Mb + 8 × 1 Mb, which is 24 Mb.

Power requirements

Voltage	Typical current
+ 5 Volt ±5%	3.0 A. including daughter modules.

Introduktion.

Denne manual beskriver hardwaredelen af Network Terminal Controller´en (NTC) samt giver en programmeringsoversigt. Kredsløbet beskrives i hovedtræk og den detaljerede beskrivelse fremgår af diagrammerne.

NTC´en er opbygget omkring to 8085 processorer, en Seeq 8003 ethernet controller samt en tre-port data buffer-memory. Kortet indeholder al elektronikken til NTC´en (powersupply dog undtaget).

Seeq controlleren implememterer Data Link laget i OSI (Open Systems Interconnect) modellens syv-lags struktur. Der benyttes en CSMA/CD protokol (Carrier Sense Multiple Acces/ Collision Detect). Det nederste lag, Physical Layer, udgøres af et 50 ohm baseband coaxial kabel, hvortil NTC´en forbindes via en transceiverboks og et standard transceiverkabel.

NTC´ens software implementerer OSI modellens Network Layer, Transport Layer samt Session Layer.

NTC´en giver tilkoblingsmulighed til et Lokalnet (Ethernet IEEE 802.3) via de otte RS 232 C (V24) porte.

Network Solutions Via Standards

While computer networks have existed for sometime, proprietary networks from different suppliers could not be used to inter-communicate. The open systems concept was developed to solve this compatibility problem. An open system is built using widely accepted standards. Open systems allow end users to select equipment from a number of suppliers to realize an optimal solution for their application.

As a standard gets widely accepted, manufacturers of VLSI integrated circuits can incorporate the standard into silicon, thereby lowering the overall system cost.

THE ISO MODEL

The International Standard Organization (ISO), in an effort to encourage 'open' networks, developed the Open Systems Interconnect (OSI) reference model. In simple terms, the model logically groups the functions and sets of rules, called protocols, necessary to establish and conduct communication between two or more parties. The model consists of seven functions, often referred to as layers. The OSI model describes the functions of each layer in broad terms, not specific implementations.

This layered model approach affords two key advantages. First, layers allow a clear division of the design task making specifications clean. Second, systems based on a layered architecture are flexible. Flexibility is achieved because each layer functions independently of the layer preceding or after it. Thus, specific layer implementations can be changed easily. For example, layers 1 and 2 of a network can be changed to be either CSMA/CD based (e.g. IEEE 802.3) or token ring based (e.g. IEEE 802.5), without affecting layers 3 through 7.

The layer functions of the OSI model are summarized in Figure 1-1.

The Physical Layer describes the physical media over which the bit stream is to be transmitted. This Layer specifies type of cable (coax, twisted pair, etc.) signal levels, bit rate, data encoding method, modulation method, and method for detecting collisions in contention networks. In short, this Layer describes the actual physical media over which the bit stream is transmitted and the method of transmission, i.e. baseband or broadband.

The Data Link Layer describes the rules for transmitting on the channel (made up of the encoder/decoder, transceiver cable, and transmission medium). Such items as the format of the information (frame) and procedures for gaining control of the channel (access method), transmitting the frame, and releasing the physical media are specified by the Data Link Layer.

The Network Layer controls switching between links in a multihop network. The Network Layer is not necessary for a single LAN system because all stations connected onto a LAN share the same channel. This Layer is critical in gateway, communication server, and dial-up communication applications.

The Transport Layer ensures end-to-end message integrity and provides for the required quality of service for exchanged information. For example, end-to-end acknowledgements and flow control are performed by the Transport Layer.

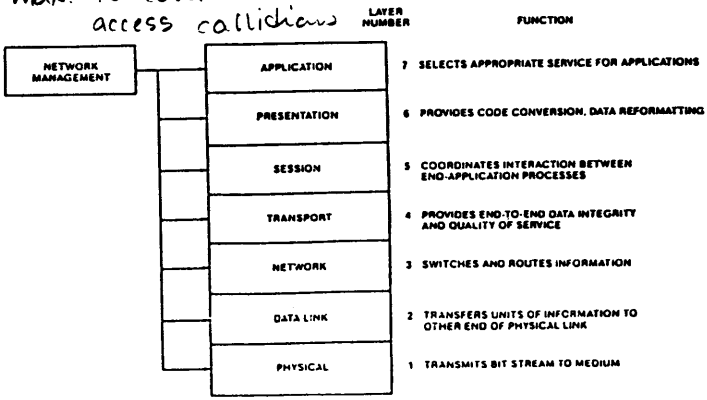
The Session Layer establishes and terminates logical connections between network entities. This Layer is also responsible for the mapping of logical names into network addresses.

The Presentation Layer provides for any necessary translation, format conversion, or code conversion to put the information into a recognizable form.

The Application Layer provides network based services to the end user. Examples of network services are distributed data bases and electronic mail. The Application Layer is not to be confused with the end user application itself.

Network Management is responsible for operation planning, which includes the gathering of operational statistics such as errors and traffic. It is also responsible for network initialization and maintenance (fault isolation). Network Management interfaces to each Layer.

"min of 9,6 µs pause
frame gap" mellem pakke
max. 16 collisions
access collisions



CSMA/CD Overview

Carrier Sense Multiple Access with Collision Detection (CSMA/CD) is a simple and efficient means of determining how a station transmits information over common medium that is shared with other stations. CSMA/CD is the access method used by the IEEE 802.3 standard.

Carrier Sense (CS) means that any station wishing to transmit 'listens' first. When the channel is busy (i.e. some other station is transmitting), the station waits (defers) until the channel is clear before transmitting.

Multiple Access (MA) means that any station wishing to transmit can do so. No central controller is needed to decide who is able to transmit and in what order. The environment in which all stations on the network are peers with equal access is commonly referred to as distributed control.

Collision Detection (CD) means that when the channel is idle (no other station is transmitting), a station can start transmitting. It is possible for two stations to start transmitting simultaneously causing a 'collision.' In the event of a collision, the transmitting stations will continue transmitting for a fixed time to ensure that all transmitting stations detect the collision. This is known as the jamming. After the jam, the stations stop transmitting and wait a random period of time before retrying. The range of random wait times increases with the number of successive collisions such that collisions can be resolved even if a large number of stations are colliding.

IEEE 802.3

Local area networks, LANs, are communication networks extending from several hundred to several thousand feet within a building or other facility. As seen from Figure 1-2, LANs are a means of connecting various types of equipment for the purpose of sharing resources and communicating in a distributed processing environment. Although LANs using a range of speeds (from 2400 bits/sec up to 2 Mbits/sec) exist today, the trend is clearly towards networks between 1 and 10 million bits per second.

IEEE 802.3/Ethernet has gained wide acceptance by both large and small corporations as a high speed (10 Mbps) LAN. The main components of the IEEE 802.3/Ethernet network are as follows:

The cable is a low noise, shielded 50 ohm coaxial cable. Over which information is transmitted at 10 million bits per second. Segments of the cable can be up to 500 meters in length and can be connected into longer network lengths using repeaters, which regenerate the signal.

The transceiver transmits and receives signals on the coaxial cable. In addition, it isolates the node from the channel in case of a failure within the node, and detects electrical interference (called collisions) on the cable. It is connected to the cable using a simple tap and to the station by means of a transceiver cable which consists of four individual twisted pairs and may be up to 50 meters in length.

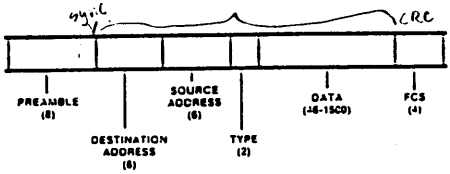
The terminator is a passive device which fits at both ends of each cable segment (or the ends of segments connected by repeaters), providing proper electrical termination (to eliminate reflections).

Finally, the interface provides the connection to the user or the server station and performs the following principle functions:

- Frame assembly/disassembly
- Handling of source and destination addressing
- Detection of physical channel transmission errors
- Network link management
  - — Collision avoidance
  - — Collision handling
- Encoding and decoding of the signal to and from the transceiver.

Frame Format

On an Ethernet communication network, information is transmitted and received in packets or frames. An Ethernet frame consists of a preamble, two address fields, a type field, a data field, and a frame check sequence (FCS). Each field has a specific format which is described in detail below. An Ethernet frame has a minimum length of 64 bytes and a maximum length of 1518 bytes exclusive of the preamble. The Ethernet frame format is shown below.



NOTE:
Field length in bytes in parentheses.

Preamble: The preamble is a 64-bit field consisting of 62 alternating "1"s and "0"s followed by a "11" End-of-Preamble indicator.

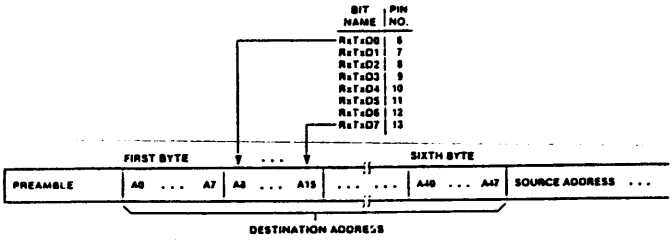
Destination Address: The Destination Address is a 6-byte field containing either a specific Station Address, a Broadcast Address, or a Multicast Address to which this frame is directed.

Source Address: The Source Address is a 6-byte field containing the specific Station Address from which this frame originated.

Type Field: The Type Field consists of two bytes. This field is uninterpreted at the Data Link Layer, and is passed through the EDLC chip to be handled at the Client Layer.

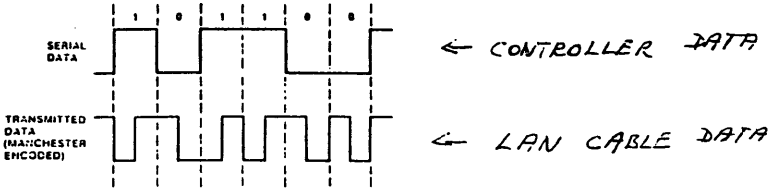
Data Field: The Data Field consists of 46 to 1500 bytes of information which are fully transparent in the sense that any arbitrary sequence of bytes may occur.

Frame Check Sequence: The Frame Check Sequence (FCS) field is a 32-bit cyclic redundancy check (CRC) value computed as a function of the Destination Address Field, Source Address Field, Type Field, and Data Field. The FCS is appended to each transmitted frame, and used at reception to determine if the received frame is valid.



BITS WITHIN A BYTE ARE TRANSMITTED/RECEIVED BIT NO. "0" FIRST THROUGH BIT NO. "7" LAST.

Bit Serialization/Deserialization



Manchester Coding

Funktionel beskrivelse.

Blokdiagrammet for NTC'en er vist på side 9.

Kortet er opbygget omkring to 8085 processorer og en Seeq 8003 ethernet controller, og kan inddeles i fem blokke:

1) Ethernet controller med DMA kredsløb til overførsel af data mellem controller og buffermemory (diagram side 1).

2) Den centrale timing-generering og back-up kontrol (diagram side 2).

3) Tre-port buffermemory med mapping kredsløb for hver port (diagram side 3).

4) CPU 1 m. eget program- og data-lager, serviceport samt FIFO til kommunikation mellem CPU 1 og CPU 2 (diagram side 4).

5) CPU 2 m. eget program- og data-lager samt 8 UART porte (diagram side 5).

Buffermemoryarealet skal kunne accesses fra såvel controller som CPU1 og CPU2, således at controlleren skal kunne opnå en middelaccestid på under 800 nS.

Tilgangen er derfor lavet med to timeslices på 350 nS:

- I den første deles controller RX og TX om acces (RX har højest prioritet, men når først TX er startet, kan RX ikke komme til, før TX er færdig; d.v.s. modtagning af egen transmission supportes ikke).

- I den anden timeslice deles CPU1 og CPU2 om acces, således at CPU1 har første prioritet.

Bufferen har tre uafhængige porte, en for controller RX/TX, en for CPU1 samt en for CPU2. Selve memoryarealet er 40 k hhv. 80

k bytes afhængigt af, om der benyttes 1 k eller 2 k bufferstørrelse, d.v.s. der er 40 buffere til rådighed (kan evt. udvides til 64 buffere, når der anvendes 1 k bufferstørrelse).

Ved hjælp af mapping kredsløbet kan en vilkårlig af disse buffere mappes ind på den ønskede adresse i portvinduet. Således kan en hel buffer flyttes ved ændring af en enkelt byte i mapping-listen.

CPU1 har et vindue på 8 k ind til bufferarealet, CPU2 ser 32 k og controlleren ser en RX- samt TX-buffer ad gangen.

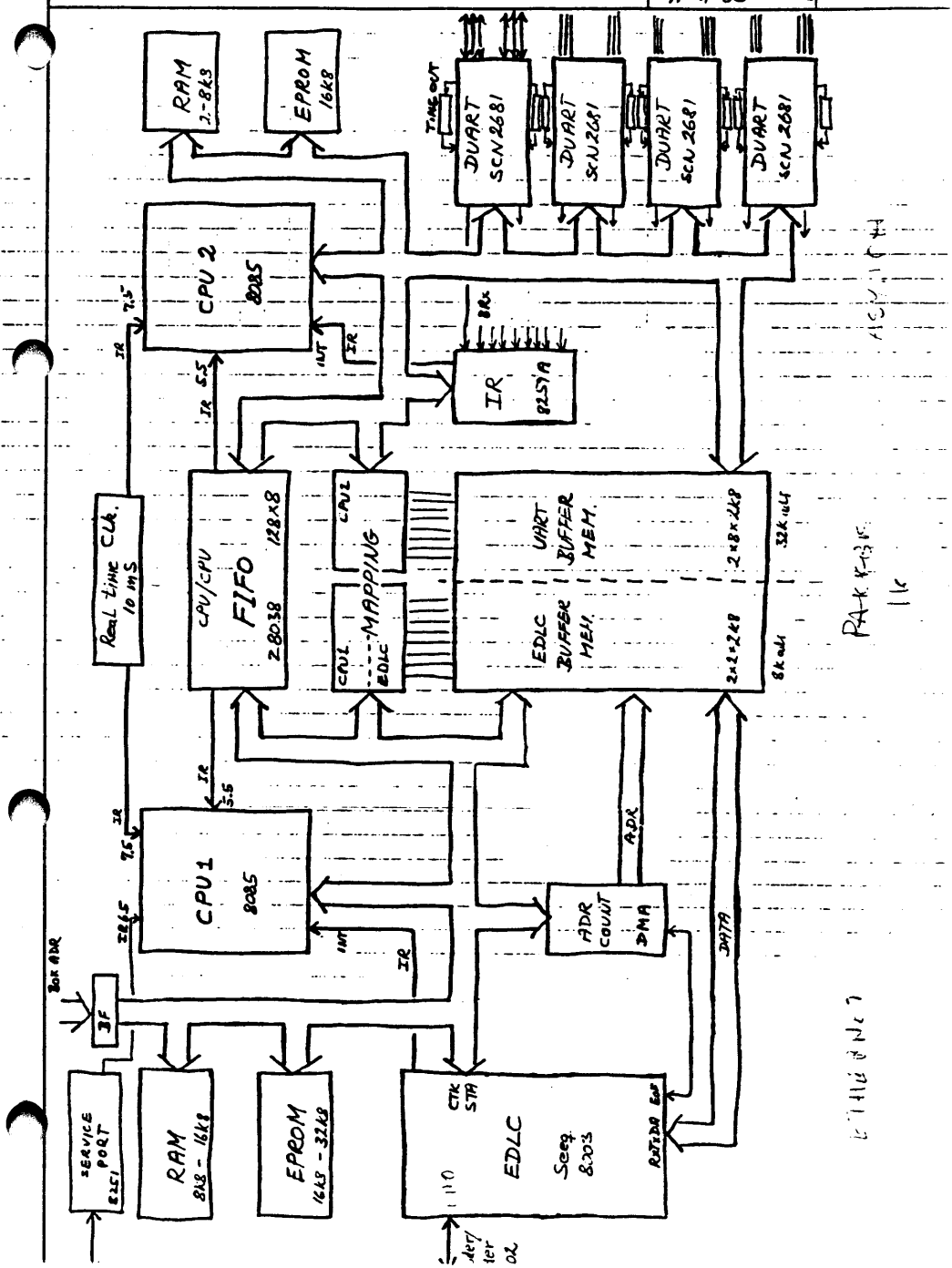
CPU1 tager sig af styring af controller kreds, bufferallokering, øvre netværksprotokol, serviceport samt videregiver meddelelser til CPU2.

CPU2 betjener de otte asynkrone brugerporte.

Kommunikationen mellem de to CPU´er foregår via en FIFO; det er dog også muligt at anvende en fælles, fast indmappet buffer (udnyttes i testprogrammet).

dansk data elektronik a/s

BLOK DIAGRAM:	NTC	Initialeridato 19-9-83	Side 9
		Revideret 11-11-83 24-11-83 30-4-85	Projekt



STRAP SETTINGS PÅ ETHERBOARD:

S1: .* *
1 2
Reset til SIA. (Er normalt ikke forbundet).

S2: .* *
1 2
Indsætter wait-state for controller kreds.
Forbindes, hvis EDLC = Seeq 8001.

S3: .* * *
1 2 3
Valg af EPROM eller RAM for IC 19.
Anbragt ved IC 19.
Forbindes: 1 - 2 for EPROM;
2 - 3 for RAM.

S4: .* * *
1 2 3
Valg af EPROM eller RAM for IC 20.
Anbragt ved IC 20.
Forbindes: 1 - 2 for EPROM;
2 - 3 for RAM.

S5: .* * *
1 2 3
Valg af 2764 eller 27128 for IC 19.
Anbragt ved IC 19; (Se også S7/S8).
Forbindes: 1 - 2 for 2764;
2 - 3 for 27128.

S6: .* * *
1 2 3
Valg af 2764 eller 27128 for IC 20.
Anbragt ved IC 20; (Se også S7/S8).
Forbindes: 1 - 2 for 2764;
2 - 3 for 27128.

S7: .* * *
1 2 3
Valg af 2764 eller 27128 for IC 20.
Anbragt ved IC 13; (Se også S5/S6).
Forbindes: 1 - 2 for 2764;
2 - 3 for 27128.

S8: .* * *
1 2 3
Valg af 2764 eller 27128 for IC 19.
Anbragt ved IC 13; (Se også S5/S6).
Forbindes: 1 - 2 for 2764;
2 - 3 for 27128.

S9: .* * *
1 2 3

Valg af 2764 eller 27128 for IC B9.
Anbragt ved IC B9; (Se også S19).
Forbindes: 1 - 2 for 2764;
2 - 3 for 27128.

S10: .* * *
1 2 3

Valg af EPROM eller RAM for IC B9.
Anbragt ved IC B9.
Forbindes: 1 - 2 for EPROM;
2 - 3 for RAM.

S11: .* * * * * *
1 2 3 4 5 6

Valg af antal clock-cycles
for timeout på port 0.

Antal:	Forbindelse:
32	1 - 2
64	1 - 3
128	1 - 4
256	1 - 5
512	1 - 6

S12: .* * * * * *
1 2 3 4 5 6

Valg af antal clock-cycles
for timeout på port 1.

Antal:	Forbindelse:
32	1 - 2
64	1 - 3
128	1 - 4
256	1 - 5
512	1 - 6

S13: .* * * * * *
1 2 3 4 5 6

Valg af antal clock-cycles
for timeout på port 2.

Antal:	Forbindelse:
32	1 - 2
64	1 - 3
128	1 - 4
256	1 - 5
512	1 - 6

S14: .* * * * * * Valg af antal clock-cycles
1 2 3 4 5 6 for timeout på port 3.

Antal:	Forbindelse:
32	1 - 2
64	1 - 3
128	1 - 4
256	1 - 5
512	1 - 6

S15: .* * * * * * Valg af antal clock-cycles
1 2 3 4 5 6 for timeout på port 4.

Antal:	Forbindelse:
32	1 - 2
64	1 - 3
128	1 - 4
256	1 - 5
512	1 - 6

S16: .* * * * * * Valg af antal clock-cycles
1 2 3 4 5 6 for timeout på port 5.

Antal:	Forbindelse:
32	1 - 2
64	1 - 3
128	1 - 4
256	1 - 5
512	1 - 6

S17: .* * * * * * Valg af antal clock-cycles
1 2 3 4 5 6 for timeout på port 6.

Antal:	Forbindelse:
32	1 - 2
64	1 - 3
128	1 - 4
256	1 - 5
512	1 - 6

S18: .* * * * * * Valg af antal clock-cycles
1 2 3 4 5 6 for timeout på port 7.

Antal:	Forbindelse:
32	1 - 2
64	1 - 3
128	1 - 4
256	1 - 5
512	1 - 6

S19: .* * * Valg af 2764 eller 27128 for IC B9.
1 2 3 Anbragt ved IC B3; (Se også S9).
Forbindes: 1 - 2 for 2764;
2 - 3 for 27128.

S20: .* * * Valg af bufferstørrelse 1k8/2k8.
1 2 3 Anbragt ved IC B3.
Forbindes: 1 - 2 for 1k8;
2 - 3 for 2k8.

S21: .* * * Valg af bufferstørrelse 1k8/2k8.
1 2 3 Anbragt ved IC 76.
Forbindes: 1 - 2 for 2k8;
2 - 3 for 1k8.

NB: Se MAP settings ang. buffer nr.

S22: .* * * Valg af CPU 2 RAM størrelse 2k8/8k8.
1 2 3 Anbragt ved IC C0.
Forbindes: 1 - 2 for 8k8;
2 - 3 for 2k8.

S23: .* * Valg af CPU 1 reset fra CPU 2.
1 2 Anbragt ved IC B5.
(C1 udelades, når S23 forbindes).

IC F1: Strapfelt for RTC til CPU1 og CPU2;

```
                1      14
1 mS          .*        *      +5 V
5 mS           *        *      1 mS
10 mS          *        *      5 mS
20 mS          *        *      10 mS
50 mS          *        *      20 mS
til CPU1       *        *      50 mS
GND            *        *      til CPU2
                7       8
```

IC F2: Strapfelt for clock til DUART time-out tællere, kanal 7 - 4;

```
                1      16
N.C.          .*        *      +5 V
1 mS           *        *      1 mS
CLK to 6       *        *      CLK to 4
RxTxC ch6      *        *      RxTxC ch4
1 mS           *        *      1 mS
CLK to 7       *        *      CLK to 5
RxTxC ch7      *        *      RxTxC ch5
GND            *        *      N.C.
                8       9
```

IC F3: Strapfelt for clock til DUART time-out tællere, kanal 3 - 0;

```
                1      16
N.C.          .*        *      +5 V
1 mS           *        *      1 mS
CLK to 2       *        *      CLK to 0
RxTxC ch2      *        *      RxTxC ch0
1 mS           *        *      1 mS
CLK to 3       *        *      CLK to 1
RxTxC ch3      *        *      RxTxC ch1
GND            *        *      N.C.
                8       9
```

IC F4: Strapfelt for Net-interface modstande:

```
                1      16
N.C.          .*        *      +5 V
C+             *        *      C-
Res C+         *        *      Res C-
T+             *        *      T-
Res T+         *        *      Res T-
R+             *        *      R-
Res R+         *        *      Res R-
GND            *        *      N.C.
                8       9
```

NORMALT FORBINDES FØLGENDE STRAPS:

S 1:	---	(Ingen forbindelse)
S 2:	1-2.	1 waitstate
S 3:	1-2.	EPROM
S 4:	1-2.	EPROM
S 5:	2-3.	27128
S 6:	2-3.	27128
S 7:	2-3.	27128
S 8:	2-3.	27128
S 9:	2-3.	27128
S10:	1-2.	EPROM
S11:	1-5.	256 cycles
S12:	1-5.	256 cycles
S13:	1-5.	256 cycles
S14:	1-5.	256 cycles
S15:	1-5.	256 cycles
S16:	1-5.	256 cycles
S17:	1-5.	256 cycles
S18:	1-5.	256 cycles
S19:	2-3.	27128
S20:	1-2.	1k buffer

S21:	2-3.	1k8 buffer
S22:	2-3.	2k8 RAM
S23:	1-2.	CPU1 reset fra CPU2

IC F1:	3-6 og 8-11.
IC F2:	2-3, 5-6, 11-12 og 14-15.
IC F3:	2-3, 5-6, 11-12 og 14-15.
IC F4:	2-3, 4-5, 6-7, 10-11, 12-13 og 14-15.

Desuden gælder følgende for "normaludgaven" af printet:

IC 21 udelades; men sokkel monteres (CPU 1 RAM)

IC 82 udelades; men sokkel monteres (dekoder f buff RAM)

IC 89-90-91-92-93 udelades; sokler monteres (buffer RAM)

IC C0 monteres med 2k8 RAM (CPU 2 RAM)

De tre stk. 96 p EURO-konnektorer udelades;

FØLGENDE POSITIONER MONTERES MED IC-SOKLER:

IC 1	IC 99	IC D2
IC 2	IC A0	IC D3
IC 19	IC A6	IC D4
IC 20	IC B6	IC D5
IC 22	IC B7	IC D6
IC 23	IC B9	IC D7
IC 26	IC C0	IC F1
IC 27	IC C1	IC F2
IC 84	IC C3	IC F3
IC 88	IC C6	IC F4
IC 86	IC C7	IC FB
IC 87	IC C8	IC FD
IC 88	IC C9	IC FE
IC 94	IC D0	
IC 95	IC D1	

Desuden monteres sokler, men ikke kredse i følgende positioner:

IC 21, IC 82, IC 89-90-91-92-93.

Konnektorbeskrivelse:

CN og CE: Stik til Ethernet transceiver;
To parallelforbundne 3M20 konnektorer til hhv. transceiver og serviceport.
Forbindelser:

3M20			Cannon	
1		Shield		
2		Shield	1	
3		C-	9	
4		C+	2	
5		T-	10	
6		T+	3	
7		N.C.	11	
8		N.C.	4	
9		R-	12	
10		R+	5	
11		+12 V (ikke CE)	13	
12		GND	6	
13		N.C.	14	
14	(7)	GND (på CE)	7	N.C.
15	(6)	N.C.	15	N.C.
16	(5)	CTS (på CE)	8	N.C.
17	(4)	RTS (på CE)		
18	(3)	RxD (på CE)		
19	(2)	TxD (på CE)		
20	(1)	N.C.		

Pin 14 til 20 på konnektor CE anvendes desuden som serviceport-konnektor.
Fremtidigt anvendes kun CN til transceiver.

CP: Etherboks port konnektor, RS-232-C signaler (Som 3M60 konnektor på SIOC, men med krydsede signal/kontrol-ledninger):

PIN	SIGNAL	PIN	SIGNAL
01	N.C.	02	GND
03	N.C.	04	GND
05	DSR7	06	DTR7
07	RTS7	08	CTS7
09	TXD7	10	RXD7
11	N.C.	12	N.C.
13	DSR6	14	DTR6
15	RTS6	16	CTS6
17	TXD6	18	RXD6
19	GND	20	GND
21	GND	22	N.C.
23	GND	24	N.C.
25	DSR5	26	DTR5
27	RTS5	28	CTS5
29	TXD5	30	RXD5
31	DTR4	32	DSR4
33	CTS4	34	RTS4
35	RXD4	36	TXD4
37	CTS3	38	DSR3
39	RXD3	40	DTR3
41	DTR2	42	RTS3
43	CTS2	44	TXD3
45	RXD0	46	DSR2
47	TXD0	48	RST2
49	CTS0	50	CTS1
51	RST0	52	RTS1
53	DTR0	54	DTR1
55	DSR0	56	DSR1
57	RXD1	58	RXD2
59	TXD1	60	TXD2

CV: NTC Spændingskonnektor:

1	2	3	4	5
.*	*	*	*	*
GND	+5	-12	+12	NC

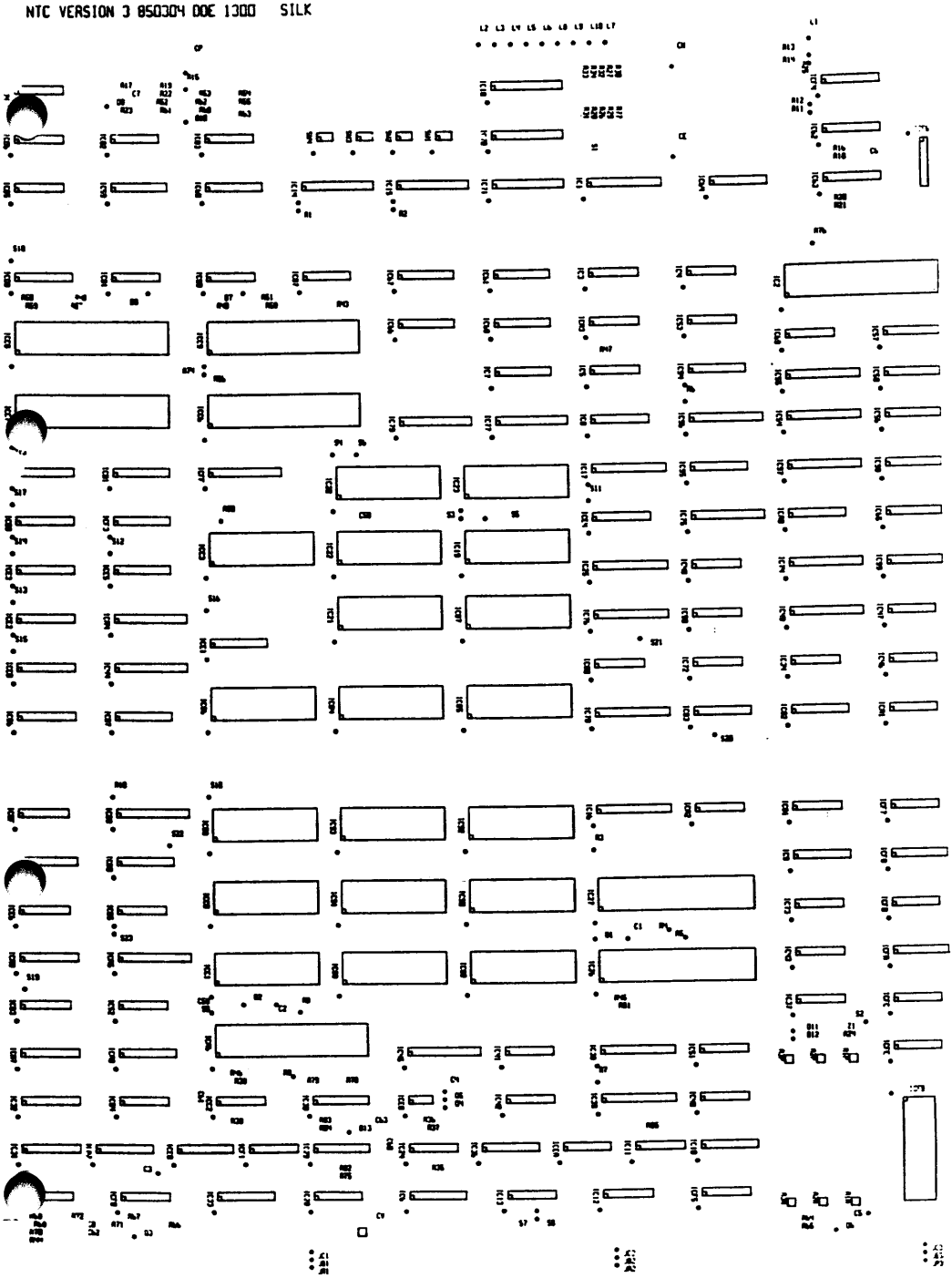
Strømforbrug: +5 V ∝ 6 A max (3 A typ)
+12 V ∝ 1 A max
-12 V ∝ 0.5 A max

Evt. loddes powerledningerne til printet, idet der er aftagelig stikforbindelse på netdelen.

LED indikeringer på NTC:

LED:	NAVN:	Forbundet til:
L1:	POWER	+5 V
L2:	NET ACTIVITY	Carrier Sense
L3:	TRANSMIT	TxEN
L4:	RECEIVE	Rx enabled (RFENDN)
L5:	STATUS 1	CPU1 I/O register
L6:	STATUS 2	CPU2 I/O register
L7:	-	(Monteres ikke)
L8:	ERROR	CPU1 I/O register
L9:	TEST	CPU1 I/O register
L10:	PORT ACTIVITY (Inp)	RxRDY interrupt

NTC VERSION 3 850304 DOE 1300 SILK



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KOMPONENTLISTE FOR NETWORK TERMINAL CONTROLLER:

>>>>>>>>>> FØLGENDE ER EN SUMMERET KOMPONENTLISTE
FOR NTC PRINTET;
EGENTLIG STYKLISTE MED KOMPONENTNUMMERERING
FINDES PÅ SIDE 54.

****

IC'ER:

74ALS00N	4 STK	ALS		
74LS03	1 STK			LS
74ALS08N	2 STK	ALS		
74ALS10N	4 STK	ALS		
74S10N	1 STK		SCHOTTKY	
74ALS11N	2 STK	ALS		
74S11N	1 STK		SCHOTTKY	
74ALS28N	4 STK	ALS		
74ALS32N	6 STK	ALS		
74ALS74N	11 STK	ALS		
74ALS112	5 STK	ALS		
74ALS138N	12 STK	ALS		
74ALS169BN	3 STK	ALS		
74S189A	6 STK		SCHOTTKY	
74LS193N	9 STK			LS
74ALS244N	1 STK	ALS		
74ALS257N	5 STK	ALS		
74LS273N	3 STK			LS
74LS390N	3 STK			LS
74ALS540N	3 STK	ALS		
74ALS541N	10 STK	ALS		
74ALS573N	2 STK	ALS		
74ALS574N	6 STK	ALS		
74ALS580N	1 STK	ALS		
74ALS645N	1 STK	ALS		
HEF 4040 BP	8 STK	LOCMOS		

HEF 4066 BP	2 STK	LOCMOS
HEF 4093 BP	1 STK	LOCMOS
H6900 20 MHZ	1 STK	XTAL OSC
H6500 7,37 MHZ	1 STK	XTAL OSC
AD1403N	1 STK	LINEAR
LM339N	1 STK	LINEAR
75188N	5 STK	LINEAR
75189AN	5 STK	LINEAR
8085A-2	2 STK	
27128-25	3 STK	
HM6264P-15	14 STK	(heraf 6 stk som option)
TC5517APL	1 STK	
2681 DUART	4 STK	
8003 EDLC	1 STK	
8023 SIA	1 STK	
8038 FIO	1 STK	
8251A USART	1 STK	
8259A IRC	1 STK	

ANDRE KOMP.:

MULTILAYER PRINT (4 LAGS), STØRRELSE SOM SIOC	1 stk
CONNECTOR 3M 20 polet	2 stk
CONNECTOR 3M 60 polet	1 stk
CONNECTOR 96 p EURO	3 stk
CONNECTOR Molex 5 polet	1 stk
Hex DIP switch	4 stk
LYSDIODE 3 mm RED	9 stk
DIODE 1N4148	11 stk
DIODE 1N5817	2 stk
ZENER 5V6	1 stk
NiCd 180 mAh	3 stk
MODSTAND 9x1 k	1 stk SIL
MODSTAND 9x3k3	5 stk SIL
MODSTAND 9x10k	13 stk SIL
MODSTAND 39 ohm	4 stk
MODSTAND 47 ohm	3 stk

MODSTAND	150 ohm	10 stk	
MODSTAND	470 ohm	2 stk	
MODSTAND	680 ohm	2 stk	
MODSTAND	1 k	3 stk	
MODSTAND	1k8	2 stk	
MODSTAND	2k2	8 stk	
MODSTAND	2k4	2 stk	
MODSTAND	4k7	1 stk	
MODSTAND	5k6	3 stk	
MODSTAND	10k	8 stk	
MODSTAND	100k	1 stk	
MODSTAND	10k0	4 stk	4e
MODSTAND	750 ohm	1 stk	4e
MODSTAND	61k9	1 stk	4e
KONDS.	10uF/16	5 stk	
KONDS.	10 nF	3 stk	
KONDS.	100 nF	2 stk	
KONDS.	afkobl.	52 stk	

UBENYTTEDE GATES:

IC	4	PIN 3	2 INPUT OR	ALS32
IC	29	PIN 9	FLIP FLOP N.E.	ALS112
IC	A3	PIN 3	2 INPUT NAND	ALS00
IC	B3	PIN 8	2 INPUT AND	ALS08
IC	DF	PIN 6	2 INPUT NAND	ALS00
IC	DF	PIN 8	2 INPUT NAND	ALS00
IC	E7	PIN 9	FLIP FLOP N.E.	ALS112
IC	EA	PIN 8	FLIP FLOP P.E.	ALS74

****

<u>stykliste for</u> NETWORK TERMINAL CONTROLLER:

****

	Navn	Komponent	Pins	Fabrikat
	IC1	8023 SIA	20	Seeq
	IC2	8003 EDLC	40	Seeq
	IC3	SN74ALS74N	14	Texas
	IC4	SN74ALS32N	14	Texas
	IC5	SN74LS03N	14	Texas
	IC6	SN74ALS138N	16	Texas
	IC7	SN74ALS138N	16	Texas
	IC8	SN74ALS138N	16	Texas
	IC9	SN74ALS138N	16	Texas
	IC10	SN74ALS112N	16	Texas
	IC11	SN74S11N	14	Texas
	IC12	SN74S10N	14	Texas
	IC13	SN74ALS08N	14	Texas
	IC14	SN74ALS541N	20	Texas
	IC15	SN74ALS541N	20	Texas
	IC16	SN74ALS541N	20	Texas
	IC17	SN74LS273N	20	Texas
	IC18	SN74LS273N	20	Texas
	IC19	MBM27128-25	28	Fujitsu
	IC20	MBM27128-25	28	Fujitsu
>OPTION	IC21	HM6264PL-15	28	Hitachi
	IC22	HM6264PL-15	28	Hitachi
	IC23	HM6264PL-15	28	Hitachi
	IC24	HEF4066BP	14	Philips
	IC25	SN74ALS573N	20	Texas
	IC26	P8085A-2	40	Intel
	IC27	Z8038	40	Zilog
	IC28	H6900 20 MHZ OSC	14	NEL
	IC29	SN74ALS112N	16	Texas
	IC30	SN74ALS169BN	16	Texas
	IC31	SN74LS390N	16	Texas
	IC32	SN74LS390N	16	Texas
	IC33	SN74LS390N	16	Texas

IC34	SN74ALS74N	14	Texas
IC36	SN74ALS112N	16	Texas
IC37	SN74ALS10N	14	Texas
IC38	SN74ALS541N	20	Texas
IC39	SN74ALS574N	20	Texas
IC40	SN74ALS74N	14	Texas
IC41	SN74ALS74N	14	Texas
IC42	SN74ALS32N	14	Texas
IC43	SN74ALS10N	14	Texas
IC44	SN74ALS541N	20	Texas
IC45	SN74ALS574N	20	Texas
IC46	SN74ALS74N	14	Texas
IC47	SN74ALS74N	14	Texas
IC48	SN74ALS10N	14	Texas
IC49	SN74ALS645N	20	Texas
IC50	SN74ALS28N	14	Texas
IC51	SN74ALS28N	14	Texas
IC52	SN74ALS32N	14	Texas
IC53	SN74ALS11N	14	Texas
IC54	SN74ALS574N	20	Texas
IC55	SN74ALS574N	20	Texas
IC56	SN74LS193N	16	Texas
IC57	SN74LS193N	16	Texas
IC58	SN74LS193N	16	Texas
IC59	SN74LS193N	16	Texas
IC60	SN74LS193N	16	Texas
IC61	SN74LS193N	16	Texas
IC62	SN74LS193N	16	Texas
IC63	SN74LS193N	16	Texas
IC64	SN74LS193N	16	Texas
IC65	SN74ALS257N	16	Texas
IC66	SN74ALS257N	16	Texas
IC67	SN74ALS257N	16	Texas
IC68	SN74ALS257N	16	Texas
IC69	SN74ALS74N	14	Texas
IC70	SN74ALS574N	20	Texas
IC71	SN74ALS574N	20	Texas
IC72	SN74ALS28N	14	Texas
IC73	SN74ALS00N	14	Texas
IC74	SN74ALS541N	20	Texas
IC75	SN74ALS541N	20	Texas

	IC76	SN74ALS244N	20	Texas
	IC77	SN74ALS541N	20	Texas
	IC78	SN74ALS541N	20	Texas
	IC79	SN74ALS541N	20	Texas
	IC80	SN74ALS32N	14	Texas
	IC81	SN74ALS11N	14	Texas
>OPTION	IC82	SN74ALS138N	16	Texas
	IC83	SN74ALS138N	16	Texas
	IC84	HM6264PL-15	28	Hitachi
	IC85	HM6264PL-15	28	Hitachi
	IC86	HM6264PL-15	28	Hitachi
	IC87	HM6264PL-15	28	Hitachi
	IC88	HM6264PL-15	28	Hitachi
>OPTION	IC89	HM6264PL-15	28	Hitachi
>OPTION	IC90	HM6264PL-15	28	Hitachi
>OPTION	IC91	HM6264PL-15	28	Hitachi
>OPTION	IC92	HM6264PL-15	28	Hitachi
>OPTION	IC93	HM6264PL-15	28	Hitachi
	IC94	SN74S189AN	16	Texas
	IC95	SN74S189AN	16	Texas
	IC96	SN74ALS540N	20	Texas
	IC97	SN74ALS580N	20	Texas
	IC98	SN74ALS257N	16	Texas
	IC99	SN74S189AN	16	Texas
	ICA0	SN74S189AN	16	Texas
	ICA1	SN74ALS74N	14	Texas
	ICA2	SN74ALS32N	14	Texas
	ICA3	SN74ALS00N	14	Texas
	ICA4	SN74ALS573N	20	Texas
	ICA5	SN74LS273N	20	Texas
	ICA6	P8085A-2	40	Intel
	ICA7	SN74ALS138N	16	Texas
	ICA8	SN74ALS138N	16	Texas
	ICA9	SN74ALS138N	16	Texas
	ICB0	SN74ALS138N	16	Texas
	ICB1	SN74ALS138N	16	Texas
	ICB2	SN74ALS112N	16	Texas
	ICB3	SN74ALS08N	14	Texas
	ICB4	SN74ALS00N	14	Texas
	ICB5	SN74ALS28N	14	Texas
	ICB6	SN74S189AN	16	Texas

	ICB7		SN74S189AN	16	Texas
	ICB8		SN74ALS540N	20	Texas
	ICB9		MBM27128-25	28	Fujitsu
>OPTION	ICC0		HM6264PL -15	28	Hitachi
		ELLER	TC5517APL (se S22)	24	Toshiba
	ICC1		HM6264PL -15	28	Hitachi
	ICC2		HEF4066BP	14	Philips
	ICC3		P8259A	28	Intel
	ICC6		SCN2681ACIN40	40	Signetics
	ICC7		SCN2681ACIN40	40	Signetics
	ICC8		SCN2681ACIN40	40	Signetics
	ICC9		SCN2681ACIN40	40	Signetics
	ICD0		SN75188N	14	Texas
	ICD1		SN75188N	14	Texas
	ICD2		SN75188N	14	Texas
	ICD3		SN75188N	14	Texas
	ICD4		SN75189AN	14	Texas
	ICD5		SN75189AN	14	Texas
	ICD6		SN75189AN	14	Texas
	ICD7		SN75189AN	14	Texas
	ICD8		HEF4040BP	16	Philips
	ICD9		HEF4040BP	16	Philips
	ICDF		SN74ALS00N	14	Texas
	ICE0		HEF4040BP	16	Philips
	ICE1		HEF4040BP	16	Philips
	ICE2		HEF4040BP	16	Philips
	ICE3		HEF4040BP	16	Philips
	ICE4		HEF4040BP	16	Philips
	ICE5		HEF4040BP	16	Philips
	ICE6		H6500 7,3728 MHZ OSC	14	NEL
	ICE7		SN74ALS112N	16	Texas
	ICE8		AD1403N	8	An. Dev.
	ICE9		LM339N	14	Texas
	ICEA		SN74ALS74N	14	Texas
	ICEB		SN74ALS138N	16	Texas
	ICF0		HEF4093BP	14	Philips
	ICF1		(Strap-sokkel RTC)	14	
	ICF2		(Strap-sokkel TOC)	16	
	ICF3		(Strap-sokkel TOC)	16	
	ICF4		(Strap-sokkel NET)	16	
	ICF5		SN74ALS74N	14	Texas

ICF6	SN74ALS10N		14	Texas
ICF7	SN74ALS74N		14	Texas
ICF8	SN74ALS169BN		16	Texas
ICFA	SN74ALS169BN		16	Texas
ICFB	8251A		28	NEC
ICFC	SN74ALS32N		14	Texas
ICFD	SN75188N		14	Texas
ICFE	SN75189AN		14	Texas
ICFF	SN74ALS540N		20	Texas
Z1	Zener, 5V6 400mW			
D1	Diode 1N4148			
D2	Diode 1N4148			
D3	Diode 1N4148			ORIENTERING
D4	Diode 1N4148			AF
D5	Diode 1N4148	evt.		DIODER
D6	Diode 1N4148	1N4448		AFMÆRKET
D7	Diode 1N4148			MED
D8	Diode 1N4148			GUL PRIK
D9	Diode 1N4148			VED
D10	Diode 1N4148			KATODE.
D11	Diode 1N5817	Schottky		
SE BEM. D12	Diode 1N5817	Schottky		
D13	Diode 1N4148			
L1 til L10	Lysdiode, 3 mm RØD			(L7 monteres ikke)
SE BEM. A1	NiCd Element	180 mAh		Varta 180 RS
SE BEM. A2	NiCd Element	180 mAh		Varta 180 RS
SE BEM. A3	NiCd Element	180 mAh		Varta 180 RS
SW1 til SW4	Hex switch, EECO Micro DIP 230057			
CN (Net)	3M Konnektor 20 pin, dobbeltrække			
CE (Extend)	3M Konnektor 2 pin, dobbeltrække			
CP (Port)	3M Konnektor 60 pin, dobbeltrække			
>OPTION A1-B1-C1	EURO-konnektor, 96 pin			
>OPTION JA2-B2-C2	EURO-konnektor, 96 pin			
>OPTION JA3-B3-C3	EURO-konnektor, 96 pin			
>OPTION CV (Power)	Konnektor 5 pin Molex 2391			

Desuden straps og strap-sokler.

R1	SIL Modstand, 9 modstande 10 k ohm
R2	SIL Modstand, 9 modstande 10 k ohm
R3	SIL Modstand, 9 modstande 10 k ohm
R4	SIL Modstand, 9 modstande 10 k ohm
R5	SIL Modstand, 9 modstande 10 k ohm
R6	SIL Modstand, 9 modstande 10 k ohm
R7	SIL Modstand, 9 modstande 3k3
R8	SIL Modstand, 9 modstande 10 k ohm
R9	SIL Modstand, 9 modstande 10 k ohm
R10	SIL Modstand, 9 modstande 10 k ohm
R11	SIL Modstand, 9 modstande 3k3
R12	SIL Modstand, 9 modstande 3k3
R13	SIL Modstand, 9 modstande 3k3
R14	SIL Modstand, 9 modstande 3k3
R15	SIL Modstand, 9 modstande 1k ohm
R16	Modstand 5k6
R17	Modstand 5k6
R18	Modstand 2k4
R19	Modstand 2k4
R20	Modstand 39 ohm
R21	Modstand 39 ohm
R22	Modstand 39 ohm
R23	Modstand 39 ohm
R24	Modstand 1k ohm
R25	Modstand 150 ohm
R26	Modstand 150 ohm
R27	Modstand 150 ohm
R28	Modstand 150 ohm
R29	Modstand 150 ohm
R30	Modstand 150 ohm
(R31	Modstand 150 ohm Monteres ikke)
R32	Modstand 150 ohm
R33	Modstand 150 ohm
R34	Modstand 150 ohm
R35	Modstand 10 k
R36	Modstand 10 k
R37	Modstand 10 k
R38	Modstand 10 k
R39	Modstand 10 k

R43	Modstand	10 k		
R44	Modstand	10 k		
R45	Modstand	470 ohm		
R46	Modstand	470 ohm		
R47	Modstand	1k		
R48	Modstand	3k3		
R49	Modstand	3k3		
R50	Modstand	3k3		
R51	Modstand	3k3		
R52	Modstand	3k3		
R53	Modstand	3k3		
R54	Modstand	3k3		
R55	Modstand	3k3		
R56	Modstand	2k2		
R57	Modstand	2k2		
R58	Modstand	2k2		
R59	Modstand	2k2		
R60	Modstand	2k2		
R61	Modstand	2k2		
R62	Modstand	2k2		
R63	Modstand	2k2		
R64	Modstand	1k8		
R65	Modstand	1k8		
R66	Modstand	10k		
R67	Modstand	10k0	MR 25	Metalfilm
R68	Modstand	10k0	MR 25	Metalfilm
R69	Modstand	10k0	MR 25	Metalfilm
R70	Modstand	750R	MR 25	Metalfilm
R71	Modstand	10k0	MR 25	Metalfilm
R72	Modstand	61k9	MR 25	Metalfilm
R73	SIL Modstand, 9 modstande 10 k ohm			
R74	SIL Modstand, 9 modstande 10 k ohm			
R75	Modstand	47 ohm		
R76	SIL Modstand, 9 modstande 10 k ohm			
R77	Modstand	1 k ohm		
R78	Modstand	47 ohm		
R79	Modstand	47 ohm		
R80	SIL Modstand, 9 modstande 10 k ohm			
R81	Modstand	680 ohm		
R82	Modstand	680 ohm		
R83	Modstand	100 k ohm		

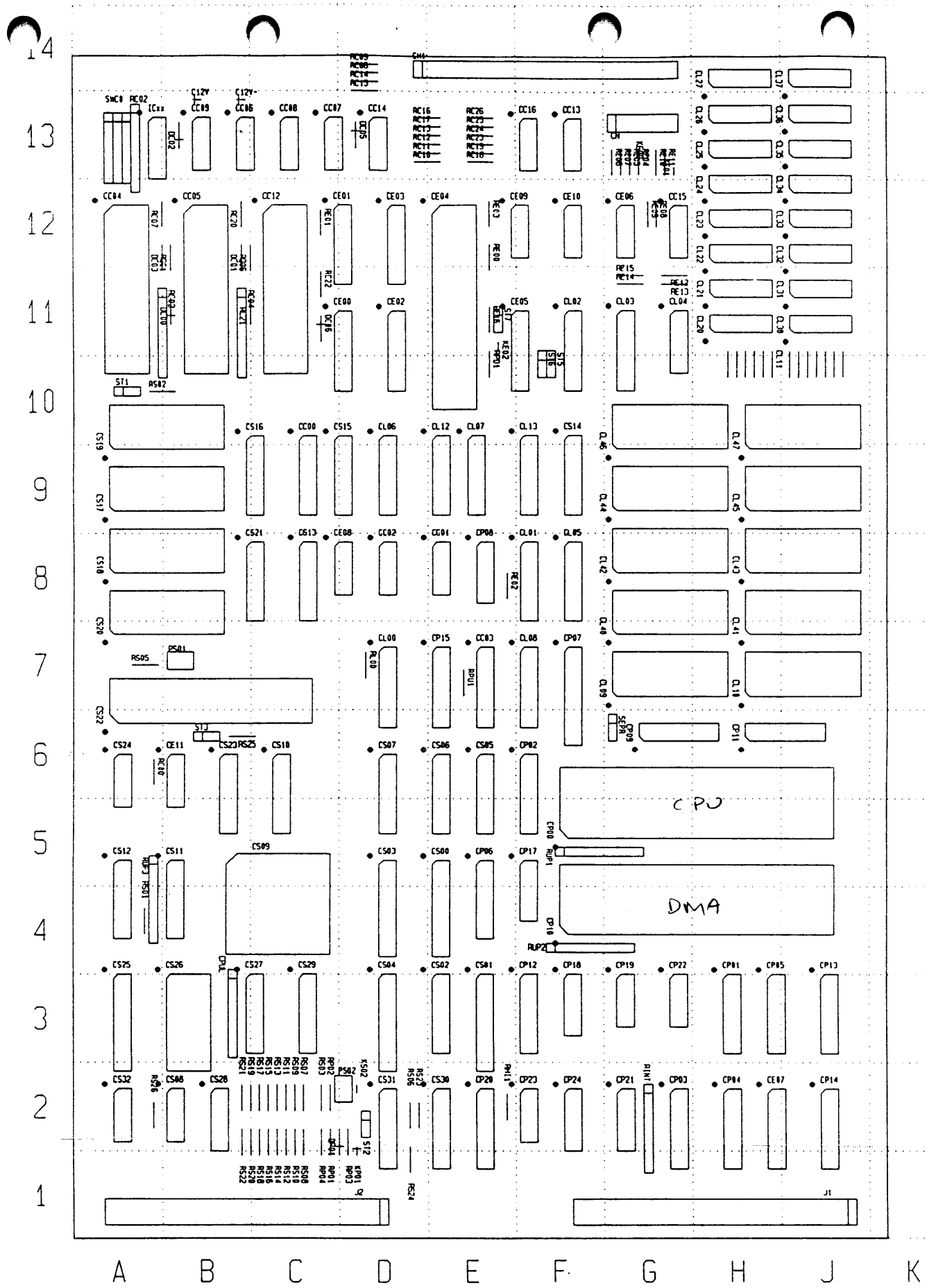
	R84	Modstand 5k6
	R85	Modstand 4k7
>OPTION	C1	(Ellyt 10 uF/16 V Sol.Al. Philips)
		C1 monteres ikke, hvis S23 forbindes.
	C2	Ellyt 10 uF/16 V Sol.Al. Philips
	C3	Ellyt 10 uF/16 V Sol.Al. Philips
	C4	Ellyt 10 uF/16 V Sol.Al. Philips
	C5	Ellyt 10 uF/16 V Sol.Al. Philips
	C6	Konds. 10 nF 2e
	C7	Konds. 10 nF 2e
	C8	Konds. 10 nF 2e
	C9 til C61	Afkobling 100 nF 2e eller 4e
	C62	Konds. 100 nF 2e
	C63	Konds. 100 nF 2e

****

>>>> Bemærkninger:

> NiCd akkumulatorer og D12 monteres <u>ikke</u>
> før det færdige print er testet.
> Tåler ikke loddebadet!!!!!!!!!!!!!!!!!
> <u>D12 monteres til sidst</u>, efter montage
> af akkumulatorer (EVT. FØRST EFTER
> ENDELIG INSTALLATION).
> Efter montage af akkumulatorer må
> printet ikke lægges på ledende underlag.

****



		dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf 02-84 50 11
Issue	Date	dde 2500
0	------	
1	------	
2	861122	Component-ID
3		
4		Parts no
5		Drg no

Name	Type	Pos
+5V	Terminal	E1
+12V	Terminal	E1
-5V	Terminal	E1
-12V	Terminal	E1
CC00	74ALS645	C10
CC01	OSC.7.3728MHz	E8
CC02	74ALS74	D8
CC03	PAL-16R4A	E7
CC04	SCN2681ACIN40	A12
CC05	SCN2681ACIN40	B12
CC06	75189AN	B13
CC07	75188AN	C13
CC08	75189AN	C13
CC09	75188AN	B13
CC12	Z8530APC	C12
CC13	75189AN	F13
CC14	75188AN	D13
CC15	75189AN	G12
CC16	75188AN	F13
CE00	74ALS645	C11
CE01	74ALS645	C12
CE02	74ALS573	D11
CE03	74ALS573	D12
CE04	82586	E12
CE05	8023A	E11
CE06	14P-STRAP	G12
CE07	PAL-16L8A	H2
CE08	74ALS74	C8
CE09	OSC.8MHZ	E12
CE10	OSC.20MHZ	F12
CE11	74ALS74	B6
CH1	60P-HEADER	D14
CL00	74ALS574	D7
CL01	PAL-16R8A	F8
CL02	74AS573	F11
CL03	74AS573	G11
CL04	74LS590	G11
CL05	PAL-16L8A	F8
CL06	74AS645	D10
CL07	74AS645	E10
CL08	PAL-16L8A	F7
CL09	DQ28C64-250	G7
CL10	DQ28C64-250	H7
CL11	33R	H11
CL12	74AS645	E10
CL13	74AS645	F10
CL20	HM50257P-15	H11
CL21	HM50257P-15	H11
CL22	HM50257P-15	H12
CL23	HM50257P-15	H12
CL24	HM50257P-15	H12
CL25	HM50257P-15	H13
CL26	HM50257P-15	H13
CL27	HM50257P-15	H14
CL30	HM50257P-15	J11
CL31	HM50257P-15	J11
CL32	HM50257P-15	J12
CL33	HM50257P-15	J12
CL34	HM50257P-15	J12
CL35	HM50257P-15	J13
CL36	HM50257P-15	J13
CL37	HM50257P-15	J14
CL40	MBM27C512-20	G7
CL41	MBM27C512-20	H7
CL42	MBM27C512-20	G8
CL43	MBM27C512-20	H8
CL44	MBM27C512-20	G9
CL45	MBM27C512-20	H9
CL46	MBM27C512-20	G9
CL47	MBM27C512-20	H9

Name	Type	Pos
CN	16P-HEADER	G13
CPUL	SIL-9x1K5	B4
CP00	MC68000L10	F5
CP01	PAL-16L8A	H4
CP02	PAL-16R8A	F6
CP03	74ALS574	G2
CP04	PAL-16L8A	H2
CP05	74ALS573	H4
CP06	74ALS573	E5
CP07	PAL-20L8A	F7
CP08	74ALS138N	E8
CP09	74ALS573	G6
CP10	MC68450-10	F4
CP11	74ALS573	H6
CP12	74ALS573	F4
CP13	74ALS645	J4
CP14	74ALS645	J2
CP15	PAL-16R4A	E7
CP17	74LS390	F5
CP18	74LS390	F4
CP19	74AS74	G4
CP20	74ALS240	E2
CP21	16P-STRAP	G2
CP22	OSC.20MHZ	G4
CP23	74ALS74	F2
CP24	74LS390	F2
CS00	PAL-GSAS	E5
CS01	PAL-GSAS	E4
CS02	74ALS573	E4
CS03	74ALS646	D5
CS04	74ALS646	D4
CS05	PAL-16L8A	E6
CS06	PAL-16L8A	E6
CS07	PAL-16R8A	D6
CS08	74ALS74	B2
CS09	AM8052-6LC	B5
CS10	74ALS573	C6
CS11	74ALS573	B5
CS12	74ALS573	A5
CS13	74ALS573	C8
CS14	74ALS645	F10
CS15	74ALS645	C10
CS16	74ALS574	B10
CS17	HM6264LP-10	A9
CS18	HM6264LP-10	A8
CS19	HM6264LP-10	A9
CS20	HM6264LP-10	A7
CS21	PAL-16L8A	B8
CS22	AM8152ADC	A6
CS23	16P-STRAP	B6
CS24	14P-STRAP	A6
CS25	PAL-20L8A	A4
CS26	MB8128-10	B4
CS27	74ALS574	B4
CS28	74S158	B2
CS29	74ALS640	C4
CS30	74AS240	E2
CS31	74AS240	D2
CS32	OSC.80MHz	A2
C12V	Capacitor	B13
C12V-	Capacitor	B13
DC00	1N4148	B11
DC01	1N4148	B11
DC02	1N4148	B13
DC03	1N4148	B11
DC05	1N4148	D13
DC06	1N4148	C11
DP01	1N4148	D1
GND	Terminal	E1
GND.1	Terminal	F1

Name	Type	Pos
ICxx	74LS163	A13
J1	96P-DIN	J1
J2	96P-DIN	D1
KE00	10nF	G13
KE01	10nF	G13
KE02	22nF	E11
KP01	68uF/6V3-Sol.Al	D2
KS02	Capacitor	D2
PS01	TR.POT-50R	B7
PS02	TR.POT-500R	D2
RC00	1K	A6
RC01	2K2	B11
RC02	SIL-9x3K3	A13
RC03	SIL-9x3K3	B11
RC04	SIL-9x3K3	B11
RC06	2K2	C11
RC07	3K3	B12
RC08	1K	D14
RC09	1K	D14
RC10	FUSE-0.5A	D13
RC11	FUSE-0.5A	D13
RC12	FUSE-0.5A	D13
RC13	FUSE-0.5A	D13
RC14	1K	D14
RC15	1K	D14
RC16	FUSE-0.5A	D13
RC17	FUSE-0.5A	D13
RC18	FUSE-0.5A	E13
RC19	FUSE-0.5A	E13
RC20	3K3	B12
RC21	10K	C11
RC22	10K	C12
RC23	FUSE-0.5A	E13
RC24	FUSE-0.5A	E13
RC25	Not-Used	E13
RC26	Not-Used	E13
RE00	3K3	E12
RE01	3K3	C12
RE02	3K3	E8
RE03	3K3	E12
RE04	39R	G13
RE05	39R	G13
RE06	5K6	G13
RE07	2K43	G13
RE08	39R	G12
RE09	39R	G12
RE10	2K43	G13
RE11	5K6	G13
RE12	470R	H11
RE13	470R	H11
RE14	470R	G11
RE15	470R	G11
RE16	560R	E11
RHI1	1K	E2
RINT	SIL-9x3K3	G2
RL00	47R	D7
RPD1	pull-dwn	E11
RPU1	1K	E7
RP01	1K	C2
RP02	10K	C2
RP03	47R	D2
RP04	10K	C2
RS01	1K	A4
RS02	47R	A10
RS03	10R	C2
RS05	10R	A7
RS06	4K7	D2
RS07	68R	C2
RS08	Not-Used	C2
RS09	68R	C2

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Component Locations

Parts no.

Dwg. no.

2

Name	Type	Pos
RS10	Not-Used	C2
RS11	68R	C2
RS12	Not-Used	C2
RS13	68R	C2
RS14	Not-Used	C2
RS15	68R	C2
RS16	Not-Used	C2
RS17	68R	C2
RS18	Not-Used	C2
RS19	68R	C2
RS20	Not-Used	C2
RS21	68R	B2
RS22	Not-Used	B2
RS23	100R	D2
RS24	4K7	D2
RS25	1K	C6
RS26	1K2	A2
RUP1	SIL-9x3K3	F5
RUP2	SIL-9x3K3	F4
RUP3	SIL-9x3K3	A5
SEPR	3P-STRAP	G6
ST1	3P-STRAP	A10
ST2	3P-STRAP	D2
ST3	3P-STRAP	B6
ST5	3P-STRAP	F11
ST6	3P-STRAP	F11
ST7	3P-STRAP	E11
SWC0	STRAP	A13
cxx1	10uF/16V-Sol.Al	A2
cxx2	100nF	A2
cxx3	100nF	A3
cxx4	100nF	A4
cxx5	100nF	A4
cxx6	100nF	A5
cxx7	100nF	A5
cxx8	100nF	A6
cxx9	100nF	A7
cxx10	100nF	A7
cxx12	100nF	A8
cxx13	100nF	A9
cxx14	100nF	A10
cxx15	100nF	A10
cxx16	100nF	A11
cxx17	100nF	A11
cxx18	100nF	A12
cxx19	100nF	A13
cxx20	100nF	A13
cxx23	100nF	K13
cxx24	100nF	K13
cxx25	100nF	K12
cxx26	100nF	K11
cxx27	100nF	K11
cxx28	100nF	K10
cxx29	100nF	K10
cxx30	100nF	K9
cxx31	100nF	K8
cxx33	100nF	K7
cxx34	100nF	K7
cxx35	100nF	K6
cxx36	100nF	K5
cxx37	100nF	K5
cxx38	100nF	K4
cxx39	100nF	K4
cxx40	100nF	K3
cxx41	100nF	K2
cxx42	100nF	K2

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Issue	Date
0	------
1	------
2	861122
3	
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Component Locations

Parts no.

Dwg. no.

3

Supermax NTC2

Technical Data

This chapter is a detailed description of the following items:

- Straps and jumpers.
- Switches.
- Connections.
- Serial drivers/receivers.
- Other components.
- Power specifications.
- Physical dimensions.
- Back panel plugs.

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Straps and jumpers

The following tables indicate the use of the various straps and jumpers used in the NTC2. The factory installed position is marked with an '*'.

MC68000 clock frequency		
	1 – 2	8 MHz
*	2 – 3	10 MHz

Table 4-1: Strap ST1

Extern clock or crystal on 82C501		
*	1 – 2	20 MHz extern
	2 – 3	NC. (Crystal)

Table 4-2: Strap ST2

Extern clock or crystal on 82C501		
	1 – 2	20 MHz extern
*	2 – 3	NC. (Crystal)

Table 4-3: Strap ST3

Mode select on 82C501		
*	1 – 2	Ethernet 1.0
	2 – 3	NON standard

Table 4-4: Strap ST4

Parallel printer output select		
*	1 – 2	Controlled by AUX3
	2 – 3	Controlled by on board logic

Table 4-5: Strap ST5

Clock for parallel interface		
	1 – 2	MC68000 clock
*	2 – 3	4 MHz

Table 4-6: Strap ST6

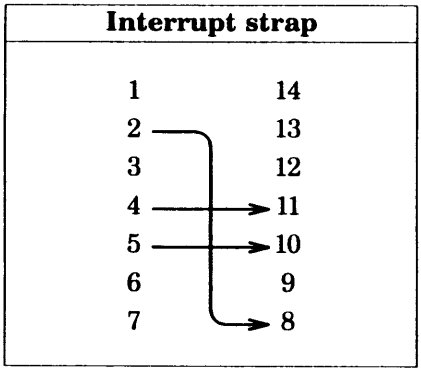

Table 4-7: Strap ISTRAP

Switches

The debug switch **SWD** is connected to interrupt level 7 on the MC68000 and is used to abort program execution for debugging and diagnostic purposes.

Connections

The following connections are made to and from the NTC2.

Power connection		
Pin	**Signal**	**Text**
1	6.3VAC	Input Phase 1 from transformer
2	GND	
3	6.3VAC	Input Phase 2 from transformer
4	6.3VAC	Output Phase 1 to pin 5
5	6.3VAC	Input Phase 1 from pin 4
6	GND	
7	6.3VAC	Input Phase 2 from pin 8
8	6.3VAC	Output Phase 2 to pin 7

Table 4-8: Connector PWR

Ethernet connection			
Pin	**Signal**	**Pin**	**Signal**
1	GND	NC	2
3	C –	C +	4
5	TX-	TX +	6
7	NC	NC	8
9	RX –	RX +	10
11	12V	GND	12
13	←78Ω→		14
15	NC	NC	16

Table 4-9: Connector CN

Serial connection			
Pin	**Signal**	**Pin**	**Signal**
1	PGND	2	NC
3	TxD	4	NC
5	RxD	6	NC
7	RTS	8	NC
9	CTS	10	NC
11	DSR	12	NC
13	GND	14	DTR
15	CD	16	+ 12V
17	– 8V	18	NC
19	NC	20	NC

Table 4-10: Connectors CAN0 – CAN7

Parallel connection			
Pin	**Signal**	**Pin**	**Signal**
1	STROBE	2	AUTOFEED
3	DATA(0)	4	ERROR
5	DATA(1)	6	INIT
7	DATA(2)	8	SELECT IN
9	DATA(3)	10	GND
11	DATA(4)	12	GND
13	DATA(5)	14	GND
15	DATA(6)	16	GND
17	DATA(7)	18	GND
19	ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SELECT	26	NC

Table 4-11: Connector CENTRO

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Serial drivers/receivers

The serial drivers and receivers are mounted in sockets in order to make replacement easier. There is 1 driver chip and 1 receiver chip for each of the 8 channels.

Mnemonic	Channel	Function	Component
U30	0	Driver	14C88 or 75C188
U50	1	Driver	14C88 or 75C188
U31	2	Driver	14C88 or 75C188
U51	3	Driver	14C88 or 75C188
U32	4	Driver	14C88 or 75C188
U52	5	Driver	14C88 or 75C188
U33	6	Driver	14C88 or 75C188
U53	7	Driver	14C88 or 75C188
U40	0	Receiver	14C89 or 75C189
U60	1	Receiver	14C89 or 75C189
U41	2	Receiver	14C89 or 75C189
U61	3	Receiver	14C89 or 75C189
U42	4	Receiver	14C89 or 75C189
U62	5	Receiver	14C89 or 75C189
U43	6	Receiver	14C89 or 75C189
U63	7	Receiver	14C89 or 75C189

Table 4-12: Serial drivers/receivers

Other components

There are a few other *need-to-know* components on the NTC2.

Mnemonic	Function	Component
3AFUSE	Fuse +5 Volt	3 A Picofuse
1AFUSE	Fuse +12 Volt	1 A Picofuse
1AFUSE	Fuse −8 Volt	1 A Picofuse
IC19	EPROM Odd	27C512 – 20 or 27C1001 – 20
IC20	EPROM Even	27C512 – 20 or 27C1001 – 20
IC21	SRAM Odd	MB8464 – 15 or equivalent
IC21A	SRAM Even	MB8464 – 15 or equivalent
IC54	Ethernet address	PROM EP320
L0	Status LED	Red LED
L1	Status LED	Red LED
L2	Status LED	Red LED
L3	Status LED	Red LED
L4	Status LED	Green LED
L5	Status LED	Green LED

Table 4-13: Other components

Power specifications

Input voltage	180 – 264 VAC or 90 – 127 VAC (Strapable)
Frequency	50 (60) Hz
Power consumption	20W
Fuse	1 A (slow blow)

Table 4-14: AC specifications

5 V	1.6 A
12 V	0.5 A
–8 V	0.1 A

Table 4-15: DC specifications

Environment

Temperature	10 – 35 ° C
Humidity	10 – 90 % non condensing

Table 4-16: Environment

Physical dimensions

Length	440 mm
Height	300 mm
Depth	100 mm (including fixing plate)
Weight	6 kg

Table 4-17: Physical dimensions

Back panel plugs

Pin	Signal	Pin	Signal
1	PGND	14	NC
2	TXD	15	NC
3	RXD	16	NC
4	RTS	17	NC
5	CTS	18	NC
6	DSR	19	NC
7	GND	20	DTR
8	CD	21	+12V
9	−8V	22	NC
10	NC	23	NC
11	NC	24	NC
12	NC	25	NC
13	NC		

Table 4-18: RS−232C pin assignments

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Pin	Signal	Pin	Signal
1	STROBE	14	AUTOFEED
2	DATA(0)	15	ERROR
3	DATA(1)	16	INIT
4	DATA(2)	17	SELECT IN
5	DATA(3)	18	GND
6	DATA(4)	19	GND
7	DATA(5)	20	GND
8	DATA(6)	21	GND
9	DATA(7)	22	GND
10	ACK	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SELECT		

Table 4-19: Centronics port pin assignments

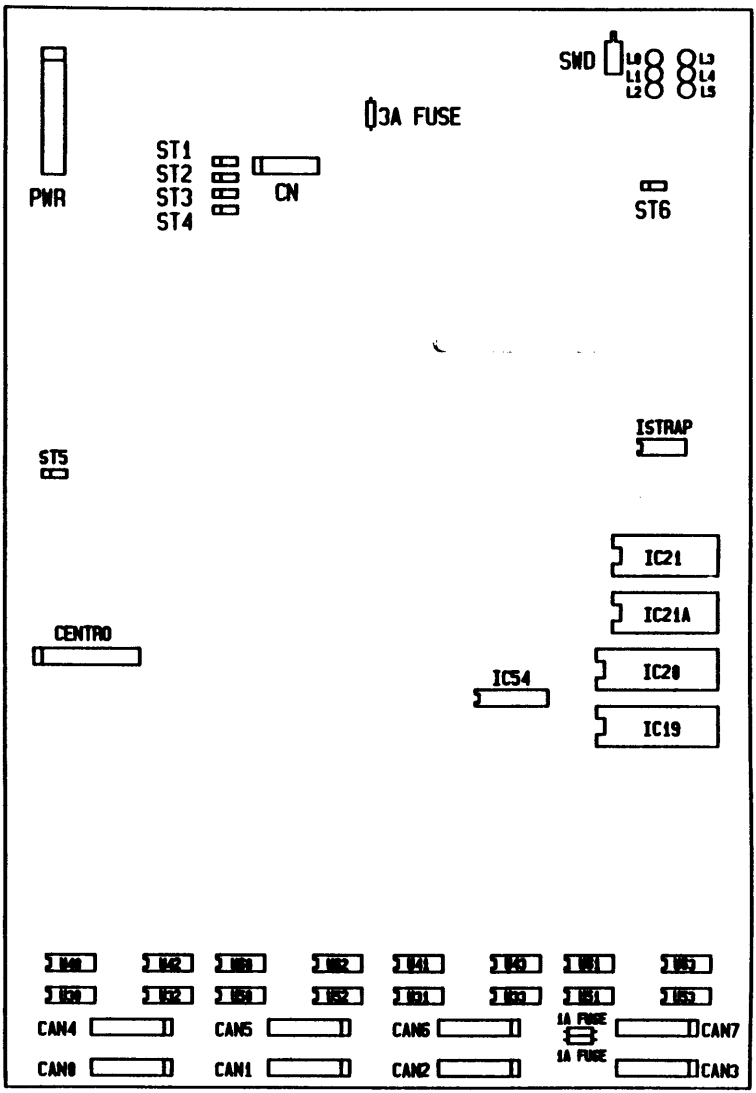


Figure 4-1: Component layout

Type: SGD Alpha board 2500

Data sheet no.:

Revision no.: 1

Date: 882101

2.1.1: General description:

The SGD is an intelligent Graphic Display Controller in a Supermax system. The SGD consists of two boards: A CPU board (alpha board), and a bit mapped graphic board with a graphic co-processor. This technical data sheet describes the SGD 2500 alfa board.

The alpha board contains the CPU, and is built around a MC68000 microprocessor. It also has implemented the following IO interfaces:

- IEEE 802.3 Ethernet interface.
- Serial RS-232 interfaces.
- Service port interface.
- Extension bus.

2.1.2: Ethernet interface:

The alpha board contains a Ethernet transceiver interface. The transceiver cable is connected to a 16 pin flat cable connector CN. Termination and bias to the different signals are provided by CE06 strapping.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	GND	GND	02
03	C-	C+	04
05	TX-	TX+	06
07	GND	GND	08
09	RX-	RX+	10
11	+12 V	GND	12
13	GND	term	14
15	term	GND	16

2.1.3: Serial channals:

The serial interface includes the following programmable options:

- Baud rates from 50 to 38400 baud.
- Character length from 5 to 8 data bits.
- Odd, even or no parity.
- 1, 1.5 or 2 stop bits.

All RS-232 interface ports are connected to a 60 pin flat cable connector CH1.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	TXD1A	RXD1A	02
03	RTS1A	CTS1A	04
05	DSR1A	DTR1A	06
07	GND	GND	08
09	+12V	-12V	10
11	TXD1B	RXD1B	12
13	RTS1B	CTS1B	14
15	GND	DTR1B	16
17	+12V	-12V	18
19	TXD2A	RXD2A	20
21	RTS2A	CTS2A	22
23	DSR2A	DTR2A	24
25	GND	GND	26
27	+12V	-12V	28
29	TXD2B	RXD2B	30
31	RTS2B	CTS2B	32
33	GND	DTR2B	34
35	+12V	-12V	36
37	TXD3A	RXD3A	38
39	RTS3A	CTS3A	40
41	DSR3A	DTR3A	42
43	GND	GND	44
45	TXC3A	RXC3A	46
47	+12V	-12V	48
49	TXD3B	RXD3B	50
51	RTS3B	CTS3B	52
53	DSR3B	DTR3B	54
55	GND	GND	56
57	TXC3B	RXC3B	58
59	+12V	-12V	60

2.1.4: Interface to RS232 channels:

A 60 pin flat cable is run from CH1 to a small back panel, where the six serial channels are split out to six 25 pin connectors. Channel 0 to 3 contain the following signals:

PIN	SIGNAL	SIGNAL	PIN
01	GND	NC	14
02	TXD	NC	15
03	RXD	NC	16
04	RTS	NC	17
05	CTS	NC	18
06	DSR	NC	19
07	GND	DTR	20
08	NC	+12V	21
09	-12V	NC	22
10	NC	NC	23
11	NC	NC	24
12	NC	NC	25
13	NC		

Connector description:

CHANNEL 0-3

PIN	SIGNAL	SIGNAL	PIN
01	GND	NC	14
02	TXD	TXC	15
03	RXD	NC	16
04	RTS	RXC	17
05	CTS	NC	18
06	DSR	NC	19
07	GND	DTR	20
08	NC	+12V	21
09	-12V	NC	22
10	NC	NC	23
11	NC	NC	24
12	NC	NC	25
13	NC		

Connector description:

CHANNEL 4-5

2.1.5: Bus connector: J1

Pin number:	ROW a Signal mnemonic:	ROW b	ROW c
1	BD00	NC	BD08
2	BD01	NC	BD09
3	BD02	NC	BD10
4	BD03	NC	BD11
5	BD04	NC	BD12
6	BD05	NC	BD13
7	BD06	NC	BD14
8	BD07	NC	RESS
9	GND	NC	GND
10	BSYSCLK -	NC	NC
11	GND	NC	BERR- **
12	UDS-	NC	BRESET* (slow)
13	LDS-	NC	NC
14	R-W	NC	NC
15	GND	NC	BA23
16	DTACK-	NC	BA22
17	GND	AM1 **	BA21
18	AS-	AM2 **	BA20
19	NC	AM3 **	BA19
20	BIACK **	GND	BA18
21	NC	NC	BA17
22	NC	NC	BA16
23	AM4 **	GND	BA15
24	BA07	IRQ7-	BA14
25	BA06	IRQ6-	BA13
26	BA05	IRQ5-	BA12
27	BA04	IRQ4-	BA11
28	BA03	IRQ3-	BA10
29	BA02	IRQ2-	BA09
30	BA01	IRQ1-	BA08
31	-12V	NC	+12V
32	+5V	+5V	+5V

Bus connector: J2

Pin number:	ROW a Signal mnemonic:	ROW b	ROW c
1		-5V	GND
2	CAN3	-5V	GND
3	CAN2	-5V	GND
4	CAN1	-5V	GND
5	CAN0	-5V	GND
6	VID2	-5V	GND
7	VID1 **	-5V	GND
8	HSYNC	-5V	GND
9	VSYNC	-5V	GND
10	CAN3-	-5V	GND
11	CAN2-	-5V	GND
12	CAN1-	-5V	GND
13	CAN0-	-5V	GND
14	VID2-	-5V	GND
15	VID1-	-5V	GND
16	HSYNC-	-5V	GND
17	VSYNC-	-5V	GND
18	BCLK2-	-5V	GND
19	BCLK1-	-5V	GND
20	ESYNC-	-5V	GND
21	RSTT	-5V	GND
22	BLANK	-5V	GND
23		-5V	GND
24		-5V	GND
25	RESET-X2-	-5V	GND
26	DCLK	-5V	GND
27	+5V	-5V	GND
28	+5V	-5V	GND
29	+5V	-5V	GND
30	+5V	-5V	GND
31	+5V	-5V	GND
32	+5V	-5V	GND

2.1.6: Power requirements:

Voltage		Typ. current	
+ 5	+-5%	5.0 A	
+12	+-5%	0.4 A	(excl. transceiver)
-12	+-5%	0.1 A	

2.1.7: Physical dimension:

Elongated Double Europa module.

Width : 234 mm.
Depth : 340 mm.
Height: 20 mm.

2.1.8: Installation:

Before the alpha board is used in SGD the following items must be selected/checked:

- Straps.
- Transceiver cable.
- Flat cables for the serial channels.
- Version of firmware.

These items are described in details in the following text.

2.1.9: Firmware:

The firmware is situated in EPROM's mounted in position CL41, CL43, CL45 and CL47 (even bytes); CL40, CL42, CL44 and CL46 (odd bytes).

The EPROM's also contain a test program that is executed after power up reset. After the test program has been executed, the SGD firmware is automatically started and are ready to receive commands.

2.1.10: Straps and jumpers:

+ designates factory installed position.

Strap CE06:

Function: Controls termination of LAN cable.

+ PIN 1 connected to PIN 14: Ethernet drop cable.
+ PIN 2 connected to PIN 12
+ PIN 3 connected to PIN 12
+ PIN 4 connected to PIN 11
+ PIN 5 connected to PIN 10
+ PIN 6 connected to PIN 9
  PIN 7 connected to PIN 8

Strap SEPR:

Function: Controls address input to EPROM memory.
+ PIN 1 connected to PIN 2 : 512kb EPROMs used.
  PIN 2 connected to PIN 3 : 256kb EPROMs used.

Changing the strap position will also require a PAL change.

Strap ST1:

Function: Controls address input to character RAM.

PIN 1 connected to PIN 2 : CA13 connected to pin 26 of CS17, CS18, CS19 and CS20.

Strap ST2:

Function: Controls delay of pixel clock relative to character clock.

+ PIN 1 connected to PIN 2: Maximum delay selected, adjustable by potentiometer PS02.

PIN 2 connected to PIN 3: No delay selected.

Strap ST3:

Function: Controls GREY level for analog screen output.

+ PIN 1 connected to PIN 2

PIN 2 connected to PIN 3

Strap ST5:

Function: Controls the CLOCK signal to the MANCHESTER encoder.

+ PIN 1 connected to PIN 2: The CLOCK is supplied to pin 14 of the manchester encoder.

PIN 2 connected to PIN 3: Pin 14 of the manchester encoder is grounded.

Strap ST6:

Function: Controls the Manchester encoder.

PIN 1 connected to PIN 2: The CLOCK is supplied to pin 13 of the manchester encoder.

PIN 2 connected to PIN 3: Pin 13 of the manchester encoder is left floating.

Strap ST7:

Function: Controls pin 2 of the manchester encoder.

PIN 1 connected to PIN 2: Pin 2 is grounded.

PIN 2 connected to PIN 3: Pin 2 is connected to pin 1 by KE02

Strap SWC0:

Function: Software select strap and extra baud rate select.
(Applies only to versions earlier than 1.7)

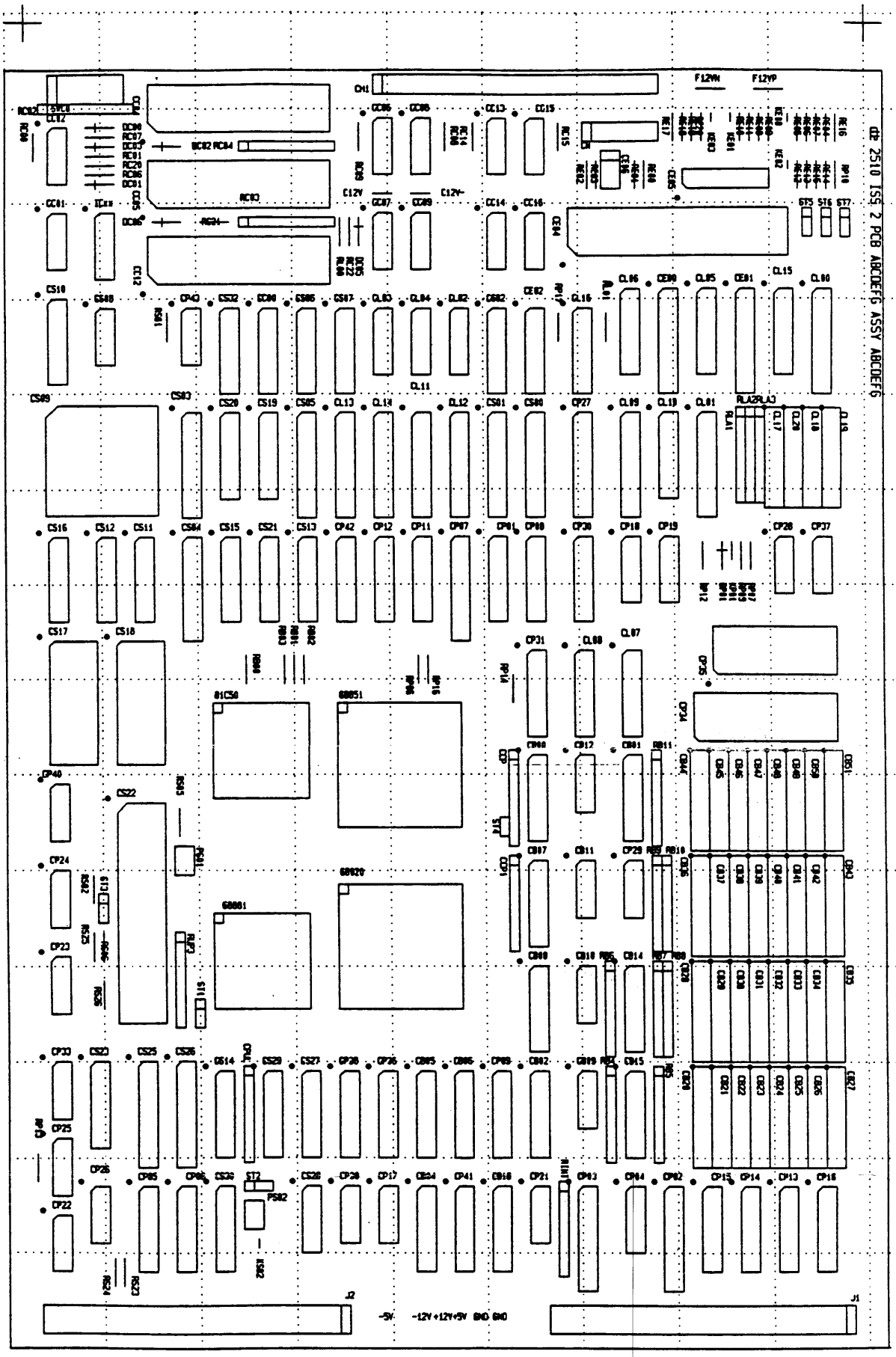
Strappings for SWC0:

```
Monitor timing for      *-* * * * * * *
80 MHz pixel rate:      * * * * * * * *
                       .* * * * * * * *

Monitor timing for      * * * * * * * *
70 MHz pixel rate:      I * * * * * * *
                       .I * * * * * * *

Monitor timing for      * * * * * * * *
64 MHz pixel rate:      * I * * * * * *
                       .* I * * * * * *
```

The next strappings are independant of the abovementioned:

```
                        * * * * * * * *
68020 accelerator       * * * * * * I *
board installed:       .* * * * * * I *

Initialize via printer  * * * * * * * *
port on versions earlier * * * * * * * I
than 1.6:              .* * * * * * * I
```

The symbol I denotes strap position.



Component locations

PCB: 2510 / SGD Alpha	Issue: 2	Date: 880524	dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11

Name	Type	Pos
+5V	terminal	E1
+12V	terminal	E1
-5V	terminal	E1
-5V.1	terminal	E1
-12V	terminal	E1
CB00	16L8D	F7
CB01	16L8B	G7
CB02	16L8B	F3
CB04	16L8A	E2
CB05	16R8B	E3
CB06	16R8B	E3
CB07	16R8B	F6
CB08	16R8B	F5
CB09	74S32	F3
CB10	74S32	F5
CB11	74S32	F6
CB12	74S32	F7
CB14	74S241	G5
CB15	74S241	G3
CB18	74S241	F2
CB20	MB81C4256-12PSZ	H3
CB21	MB81C4256-12PSZ	H3
CB22	MB81C4256-12PSZ	H3
CB23	MB81C4256-12PSZ	H3
CB24	MB81C4256-12PSZ	J3
CB25	MB81C4256-12PSZ	J3
CB26	MB81C4256-12PSZ	J3
CB27	MB81C4256-12PSZ	J3
CB28	MB81C4256-12PSZ	H5
CB29	MB81C4256-12PSZ	H5
CB30	MB81C4256-12PSZ	H5
CB31	MB81C4256-12PSZ	H5
CB32	MB81C4256-12PSZ	J5
CB33	MB81C4256-12PSZ	J5
CB34	MB81C4256-12PSZ	J5
CB35	MB81C4256-12PSZ	J5
CB36	MB81C4256-12PSZ	H6
CB37	MB81C4256-12PSZ	H6
CB38	MB81C4256-12PSZ	H6
CB39	MB81C4256-12PSZ	H6
CB40	MB81C4256-12PSZ	J6
CB41	MB81C4256-12PSZ	J6
CB42	MB81C4256-12PSZ	J6
CB43	MB81C4256-12PSZ	J6
CB44	MB81C4256-12PSZ	H7
CB45	MB81C4256-12PSZ	H7
CB46	MB81C4256-12PSZ	H7
CB47	MB81C4256-12PSZ	H7
CB48	MB81C4256-12PSZ	J7
CB49	MB81C4256-12PSZ	J7
CB50	MB81C4256-12PSZ	J7
CB51	MB81C4256-12PSZ	J7
CCP	10-1-102	F7
CCP1	10-1-102	F6
CC00	74ALS645	C11
CC01	OSC.7M3728HZ	A12
CC02	74S74	A13
CC04	2681	B13
CC05	2681	B12
CC06	75189	D13
CC07	75188	D12
CC08	75189	E13
CC09	75188	E12
CC12	8530	B12
CC13	75189	F13
CC14	75188	F12
CC15	75189	F13
CC16	75188	F12
CE00	74ALS646	G12
CE01	74ALS646	H12
CE02	16R4A	F11
CE04	82586	F12
CE05	8023A	H13
CE06	STRAP	G13
CH1	Serial-I/O	D14
CL00	20R8A	J12
CL01	20R6A	H10
CL02	74S138	E11

Name	Type	Pos
CL03	74S139	D11
CL04	74S151	E11
CL05	74AS573	H12
CL06	74AS573	G12
CL07	74AS573	G8
CL08	74AS573	F8
CL09	20L8A	G10
CL10	74AS573	G10
CL11	74ALS646	E10
CL12	74ALS646	E10
CL13	74ALS646	D10
CL14	74ALS646	D10
CL15	74ALS645	J12
CL16	16R4A	F11
CL17	MB81C4256-12PSZ	J10
CL18	MB81C4256-12PSZ	J10
CL19	MB81C4256-12PSZ	J10
CL20	MB81C4256-12PSZ	J10
CN	LAN-I/O	G13
CPUL	10-1-152	C3
CP01	16L8D	F9
CP02	20L8A	G2
CP03	20R8A	F2
CP04	74LS148	G2
CP05	74ALS645	B2
CP06	74ALS645	B2
CP07	20L8A	E9
CP08	16L8A	F9
CP09	74AS573	F3
CP11	74AS573	E9
CP12	74AS573	D9
CP13	74ALS645	J2
CP14	74ALS645	H2
CP15	74ALS645	H2
CP16	74ALS645	J2
CP17	74LS393	D2
CP18	74LS390	G9
CP19	74LS390	G9
CP21	STRAP	F2
CP22	STRAP	A2
CP23	OSC.50MHZ	A5
CP24	OSC.40MHZ	A6
CP25	74S74	A3
CP26	74S00	A2
CP27	20L8A	F10
CP28	74LS14	J9
CP29	74LS07	G6
CP30	16L8A	F9
CP31	16R6D	F8
CP33	74AS1004	A4
CP34	271001	H7
CP35	~~2764~~ D2 28C67	H8
CP36	16L8B	D3
CP37	74LS393	J9
CP38	16R8B	D3
CP39	74S260	D2
CP40	OSC.16MHZ	A6
CP41	16L8A	E2
CP42	74AS573	D9
CP43	74S10	B11
CS00	20R8A	F10
CS01	20R8A	F10
CS02	16L8A	F11
CS03	74ALS646	B10
CS04	74ALS646	B9
CS05	20L8A	D10
CS06	16R8A	D11
CS07	74AS574	D11
CS08	74S74	A11
CS09	8052	A10
CS10	74ALS574	A12
CS11	74ALS574	B9
CS12	74ALS573	A9
CS13	74ALS573	D9
CS14	74ALS645	C3
CS15	74ALS645	C9
CS16	74ALS574	A9
CS17	SRAM32KX8-10	A8

Name	Type	Pos
CS18	SRAM32KX8-10	B8
CS19	74ALS645	C10
CS20	74ALS645	C10
CS21	16L8A	C9
CS22	8052A	B6
CS23	16R4A	A4
CS25	20L8A	B4
CS26	HM6116ASP-10	B4
CS27	74AS574	D3
CS28	74S158	D2
CS29	74ALS640	C3
CS30	74S240	C2
CS32	16R4A	C11
C12V	10uF-TANTAL	E13
C12V-	10uF-TANTAL	E13
DC00	1N4148	A13
DC01	1N4148	A13
DC02	1N4148	B13
DC03	1N4148	A13
DC05	1N4148	D12
DC06	1N4148	B12
DP01	1N4148	H9
F12VN	FUSE-1.5A	H14
F12VP	FUSE-1.5A	H14
GND	terminal	E1
GND.1	terminal	F1
ICxx	74ALS163	A12
J1	BUS-96p-DIN	J1
J2	BUS-96p-DIN	D1
KE00	10nF-CERAMIC	J14
KE01	10nF-CERAMIC	H14
KE02	10nF-CERAMIC	J13
KE03	10nF-CERAMIC	H14
KP01	10uF-TANTAL	H9
KS02	10nF-CERAMIC	C2
PS01	trim	B6
PS02	TRIM-500R	C2
RB4	10-2-330	G3
RB5	10-2-330	G3
RB6	10-2-330	G5
RB7	10-2-330	G5
RB8	10-2-330	G5
RB9	10-2-330	G6
RB00	330R	C8
RB01	330R	D8
RB02	33R	D7
RB03	470R	C8
RB10	10-2-330	G6
RB11	10-2-330	G7
RC00	1KR	A13
RC01	2K2R	A13
RC02	10-1-332	A14
RC03	10-1-332	C12
RC04	10-1-332	C13
RC06	2K2R	A13
RC07	3K3R	B13
RC08	1K0R	E13
RC09	1K0R	D13
RC14	1K0R	E13
RC15	1K0R	F13
RC20	3K3R	B13
RC21	10KR	C12
RC22	10KR	D12
RE00	3K3R	G13
RE01	3K3R	G13
RE02	3K3R	G13
RE03	3K3R	G13
RE04	39R0	J14
RE05	39R0	J14
RE06	5K6R	J14
RE07	2K43R	J13
RE08	39R0	H14
RE09	39R0	J14
RE10	2K43R	H13
RE11	5K6R	H14
RE12	470R	J13
RE13	470R	J13
RE14	470R	J13

Component locations

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Name	Type	Pos
RE15	470R	J13
RE16	560R	J14
RE17	39R0	H14
RE18	39R0	H14
RE19	2K43R	H13
RE20	5K6R	H14
RINT	10-1-332	F2
RLA1	10-2-470	H10
RLA2	10-2-470	H10
RLA3	10-2-470	H10
RL00	33R	D12
RL01	470R	G11
RP06	1KR	E8
RP07	5K6R	H9
RP09	27KR	H9
RP10	470R	J13
RP12	33R	H9
RP13	470R	A2
RP14	470R	F8
RP16	1KR	E8
RP17	470R	F11
RS01	470R	B11
RS02	33R	A6
RS05	10R	B6
RS06	100R	B5
RS23	1KR	B2
RS24	100R	B2
RS25	1KR	A5
RS26	1KR	B4
RUP3	10-1-332	B5
ST1	STRAP	C4
ST2	STRAP	C2
ST3	STRAP	B5
ST4	STRAP	F6
ST5	STRAP	J12
ST6	STRAP	J12
ST7	STRAP	J12
SWC0	switch	A14
81C50	MB81C50	C7
68020	68020	D5
68851	68851	D7
68881	68881	C5

Name	Type	Pos

Name	Type	Pos

Component locations

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Type: SGD 2510

Data sheet no.: SGD

Revision no.: 1

Date: 880812

General description:

The SGD 2510 is an intelligent Graphical Display Controller in a SUPERMAX system. The SGD consist of two boards a CPU board and a bit mapped graphics board with on board graphical processor This technical data sheet is only concerned with the CPU board. The CPU board is built around a MC68020 microprocessor and contains the following IO interfaces:

- Ethernet interface. IEEE 802.3.
- serial RS-232 interfaces.)
- Service port interface.
- Extension bus.

SERIAL CHANNELS.

The serial interface includes the following programmable options:

- Baud rates from 50 to 38400 baud.
- Character length from 5 to 8 bits.
- Odd, even or no parity.
- 1, 1.5 or 2 stop bits.

All RS-232 interface boards are connected to a 60 pin flat cable connector CH1.

Ethernet interface.

The SGD contains the Ethernet transceiver interface. The transceiver cable is connected to a 16 pin flat cable connector CN.
Extra ground can be provided by strapping CE06 to accomodate IEEE 802.3.

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01		GNDS	02
03	C-	C+	04
05	TX-	TX+	06
07	GNDS	GNDS	08
09	RX-	RX+	10
11	+12 V	GND	12
13	GND	term	14
15	term	GNDS	16

Ei signals designated GNDS can be strapped to ground by CE06.
Signals designated term are only terminated not used.

Interface to RS232 channels.

A 60 pin flat cable is led from CH1 to a small back print where the six serial channels are split up on 6 25 pin connectors. Channel 0 to 3 contain the following signals.

Connector description: CHANNEL 0-3

PIN	SIGNAL	SIGNAL	PIN
01	GND	NC	14
02	TXD	NC	15
03	RXD	NC	16
04	RTS	NC	17
05	CTS	NC	18
06	DSR	NC	19
07	GND	DTR	20
08	NC	+12V	21
09	-12V	NC	22
10	NC	NC	23
11	NC	NC	24
12	NC	NC	25
13	NC		

Connector description: CHANNEL 4-5

PIN	SIGNAL	SIGNAL	PIN
01	GND	NC	14
02	TXD	TXC	15
03	RXD	NC	16
04	RTS	RXC	17
05	CTS	NC	18
06	DSR	NC	19
07	GND	DTR	20
08	NC	+12V	21
09	-12V	NC	22
10	NC	NC	23
11	NC	NC	24
12	NC	NC	25
13	NC		

Cable description:

PIN	SIGNAL	SIGNAL	PIN
01	TXD1A	RXD1A	02
03	RTS1A	CTS1A	04
05	DSR1A	DTR1A	06
07	GND	GND	08
09	+12V	-12V	10
11	TXD1B	RXD1B	12
13	RTS1B	CTS1B	14
15	GND	DTR1B	16
17	+12V	-12V	18
19	TXD2A	RXD2A	20
21	RTS2A	CTS2A	22
23	DSR2A	DTR2A	24
25	GND	GND	26
27	+12V	-12V	28
29	TXD2B	RXD2B	30
31	RTS2B	CTS2B	32
33	GND	DTR2B	34
35	+12V	-12V	36
37	TXD3A	RXD3A	38
39	RTS3A	CTS3A	40
41	DSR3A	DTR3A	42
43	GND	GND	44
45	TXC3A	RXC3A	46
47	+12V	-12V	48
49	TXD3B	RXD3B	50
51	RTS3B	CTS3B	52
53	DSR3B	DTR3B	54
55	GND	GND	56
57	TXC3B	RXC3B	58
59	+12V	-12V	60

Firmware:

The firmware is situated in EPROM mounted in position CP34.

The PROM contain a test program that is executed after power up reset. After the test program has been executed the firmware are ready to receive commands.

Straps and jumpers:

+ designates factory installed position.

CE06

Function: Controls ground connections of LAN cable.

PIN 1 connected to PIN 2 drop cable pin 1 grounded.
PIN 3 connected to PIN 4 drop cable pin 11 grounded.
PIN 5 connected to PIN 6 drop cable pin 4 grounded.
PIN 7 connected to PIN 8 drop cable pin 8 grounded.

ST1

Function: Controls rw input to cache comparator.

PIN 1 connected to PIN 2 : read and write accesses are seperately cached.
+ PIN 2 connected to PIN 3 : read and write accesses are cached together.

ST2

Function: Controls delay of pixel clock versus character clock.

+ PIN 1 connected to PIN 2: Maximum delay selected, adjustable at potentiometer PS02.
PIN 2 connected to PIN 3: No delay selected.

Power requirements:

Voltage		Typ. current
+ 5	+-5%	7.0 A
+12	+-5%	0.1 A
-12	+-5%	0.1 A

Physical dimension:

Elongated Double Europa module.

Width : 234 mm.
Depth : 340 mm.
Height: 20 mm.

Installation:

Before a SGD module is used in a Supermax system the following items must be selected/checked:

- Straps.
- Transceiver cable.
- Flat cables for the serial channels.
- Firmware.

These items are described in details in the following text.

SWC0

Function: Software select strap and extra baud rate select.

there are eight straps in sw with pin 1,2 and 3.
strap 0 and 1 work in conjunction

0	PIN 2 not connected	
		Selection of 80MHZ monitor initialization
1	PIN 2 not connected	
0	PIN 2 connected to pin 1	
		Selection of 64MHZ monitor initialization
1	PIN 2 not connected	
0	PIN 2 not connected	
		Selection of 70MHZ monitor initialization
1	PIN 2 connected to pin 1	
2	currently not used	
3	currently not used	
4	currently not used	
5	currently not used	
6	currently not used	
7		

ST3

Function: Controls GREY level for analog screen output.

+ PIN 1 connected to PIN 2

PIN 2 connected to PIN 3

ST4

Function: Controls CDIS signal to 68020.

PIN 1 connected to PIN 2 internal cache disabled.

ST5

Function: Controls the CLOCK signal to the MANCHESTER encoder.

+ PIN 1 connected to PIN 2: The CLOCK is supplied to pin 14 of the manchester encoder.

PIN 2 connected to PIN 3: pin 14 of the manchester encoder is grounded.

ST6

Function: Controls the Manchester encoder.

PIN 1 connected to PIN 2: The CLOCK is supplied to pin 13 of the manchester encoder.

PIN 2 connected to PIN 3: Pin 13 of the manchester encoder is left floating.

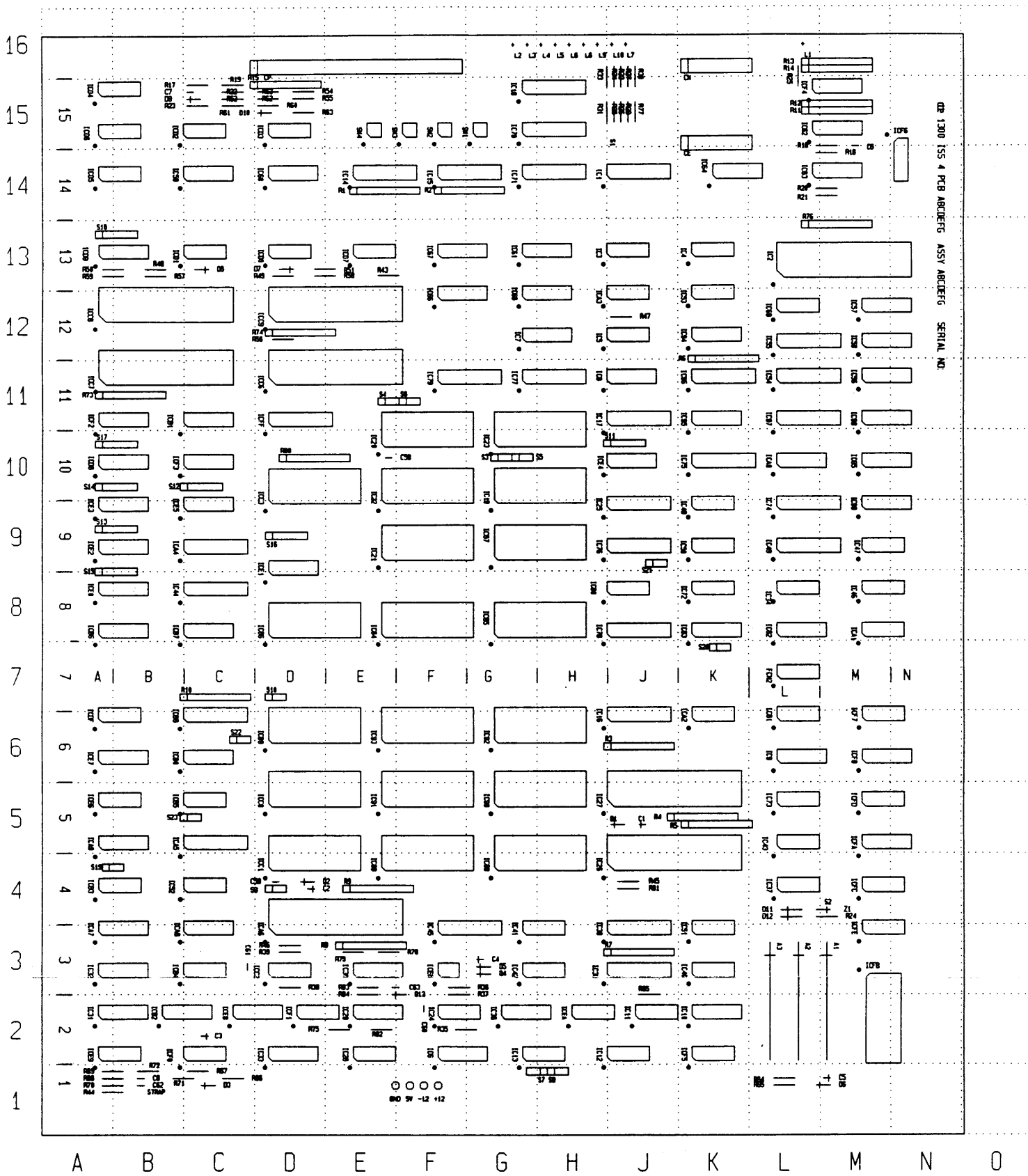
ST7

Function: Controls pin 2 of the manchester encoder.

PIN 1 connected to PIN 2 pin 2 is grounded.

PIN 2 connected to PIN 3: Pin 2 is connected to pin 1 by KE02

PRELIMINARY



Component locations

PCB: NTC	Issue:	Date:	dde	dansk data elektronik a/s herlev hovedgade 199. 2730 herlev. tlf. 02-84 50 11

PRELIMINARY

Name	Type	Pos
+12		F1
-12		F1
A1		M3
A2		L3
A3		L3
CE		K15
CN		K16
CP		C16
C1		J5
C2		D4
C3		C2
C4		G3
C5		M1
C6		M15
C7		B15
C8		B1
C58		E10
C59		D4
C60		F2
C61		C3
C62		B1
C63		E3
D1		H5
D2		D4
D3		C1
D4		G3
D5		G3
D6		L1
D7		D13
D8		C13
D9		B15
D10		C15
D11		L4
D12		L4
D13		E3
FCN2		L7
GND		E1
ICA0		L10
ICA1		M8
ICA2		K6
ICA3		H12
ICA4		B9
ICA5		B5
ICA6		D3
ICA7		A3
ICA8		B3
ICA9		A5
ICB0		B6
ICB1		B11
ICB2		B2
ICB3		A4
ICB4		B3
ICB5		B5
ICB6		A8
ICB7		B8
ICB8		B6
ICB9		D6
ICC0		D5
ICC1		D4
ICC2		D3
ICC3		D9
ICC6		D11
ICC7		A11
ICC8		A12
ICC9		D12
ICDF		A6
ICD0		D13
ICD1		B13
ICD2		B15
ICD3		D15
ICD4		A15
ICD5		A14
ICD6		A15
ICD7		E13
ICD8		A10
ICD9		A13
ICEA		H2
ICEB		C2

Name	Type	Pos
ICE0		A8
ICE1		D8
ICE2		A9
ICE3		A9
ICE4		H10
ICE5		B9
ICE6		A5
ICE7		A6
ICE8		F3
ICE9		A2
ICFA		M5
ICFB		M3
ICFC		M4
ICFD		M5
ICFE		M3
ICFF		D11
ICF0		B2
ICF1		D2
ICF2		A11
ICF3		B10
ICF4		L15
ICF5		K2
ICF6		M15
ICF7		M6
ICF8		M6
IC1		H14
IC2		L13
IC3		H13
IC4		K13
IC5		H12
IC6		F2
IC7		G12
IC8		H11
IC9		L6
IC10		K2
IC11		J2
IC12		H2
IC13		G2
IC14		E14
IC15		F14
IC16		H6
IC17		H11
IC18		G15
IC19		G9
IC20		E10
IC21		E9
IC22		E9
IC23		G10
IC24		F2
IC25		H9
IC26		H4
IC27		H5
IC28		E2
IC29		E2
IC30		E3
IC31		A2
IC32		A3
IC33		D2
IC34		L8
IC36		G2
IC37		L4
IC38		H3
IC39		H3
IC40		K3
IC41		G3
IC42		G3
IC43		L5
IC44		B8
IC45		F3
IC46		M8
IC47		M9
IC48		K9
IC49		L9
IC50		K9
IC51		K3
IC52		B4
IC53		K12
IC54		L11

Name	Type	Pos
IC55		L12
IC56		M11
IC57		M12
IC58		M12
IC59		B14
IC60		D14
IC61		G13
IC62		L15
IC63		L14
IC64		K14
IC65		M10
IC66		F12
IC67		F13
IC68		G12
IC69		L12
IC70		G15
IC71		G14
IC72		K8
IC73		L5
IC74		L9
IC75		K10
IC76		H9
IC77		G11
IC78		H8
IC79		F11
IC80		H8
IC81		L6
IC82		L8
IC83		K8
IC84		E8
IC85		G8
IC86		D8
IC87		G9
IC88		G4
IC89		E4
IC90		G5
IC91		E5
IC92		G6
IC93		E6
IC94		K12
IC95		K11
IC96		K11
IC97		L11
IC98		M11
IC99		M9
LABEL		O-1
LAYID		N11
L1		L16
L2		G16
L3		G16
L4		H16
L5		H16
L6		H16
L7		J16
L8		H16
L9		H16
L10		J16
R1		E14
R2		F14
R3		H6
R4		J5
R5		K5
R6		K12
R7		H3
R8		E3
R9		E4
R10		B7
R11		L15
R12		L15
R13		L16
R14		L16
R15		C15
R16		L15
R17		B15
R18		L14
R19		C15
R20		L14
R21		L14

Component locations

PCB: NTC

Issue:

Date:

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PRELIMINARY

Name	Type	Pos	Name	Type	Pos	Name	Type	Pos
R22		C15	S13		A9			
R23		B15	S14		A10			
R24		M4	S15		A9			
R25		L16	S16		D9			
R26		J15	S17		A10			
R27		J16	S18		A13			
R28		J15	S19		A4			
R29		J15	S20		K7			
R30		J16	S21		J9			
R31		H15	S22		C6			
R32		J16	S23		B5			
R33		H16	Z1		M4			
R34		J16	5V		F1			
R35		G2						
R36		G3						
R37		F3						
R38		D3						
R39		D3						
R43		E13						
R44		B1						
R45		J4						
R46		D3						
R47		H12						
R48		B13						
R49		D13						
R50		B13						
R51		E13						
R52		C15						
R53		C15						
R54		D15						
R55		D15						
R56		D12						
R57		B13						
R58		D13						
R59		A13						
R60		C15						
R61		C15						
R62		D15						
R63		D15						
R64		L1						
R65		L1						
R66		C1						
R67		C1						
R68		A1						
R69		B1						
R70		B1						
R71		C1						
R72		B1						
R73		A11						
R74		D12						
R75		E2						
R76		L13						
R77		J15						
R78		E3						
R79		E3						
R80		D10						
R81		J4						
R82		E2						
R83		E3						
R84		E3						
R85		J3						
STRAP		B1						
SW1		G15						
SW2		F15						
SW3		F15						
SW4		E15						
S1		H15						
S2		L4						
S3		G10						
S4		E11						
S5		G10						
S6		F11						
S7		H1						
S8		H1						
S9		D4						
S10		D7						
S11		H10						
S12		B10						

Component locations

PCB: NTC

Issue:

Date:

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Type: SGD Graphic Board 2600

Data sheet no.:

Revision no.: 1

Date: 871125

2.2: General description:

The Graphic Board contains the following elements:

- Graphic controller
- Frame buffer memory
- RGB colour palettes
- Crosshair control
- Local zoom
- Alpha overlay
- Optional math slave processor

The graphic board in the SGD is implemented using the Hitachi HD63484 ACRTC, 64k by 4 bits VideoDRAM's, and AmD's Am8151 8 bit Graphic Color Palettes as the key components.

The board contains a frame buffer memory of 1 M bytes VRAM (where each pixel is 8 bits wide), three 8 bit palettes (R, G, and B) with D/A converters, and hardware for crosshair, local zoom, and alpha overlay.

The frame buffer is seen as 512 k words of 16 bits from the graphic controller. On the serial (display) side of the frame buffer, data are read out 32 bits once every fourth pixel clock. The word is then converted to ECL levels and serialized into 8 bits for every pixelclock. These bits are then used to address the palettes.

Maximum resolution is 1024 by 1024 pixel's of 8 bits, 256 simultaneous colours from a palette of 16 million colours.

All datasignals to and from the board are latched. This is necessary as the graphic controller does not end its cycles syncronously to the CPU.

The video timing can be adapted to various monitors by selecting an appropriate pixel frequency crystal oscillator and change the settings of those registers in the controller that influences the video timing (firmware change). The pixel frequency should be in the range of 60 to 80 MHz.

As the ACRTC only provides information for the crosshair position with a resolution of one character clock, the position by pixel within the character cell must be generated by hardware. The dot position is output in the attribute word from the ACRTC and latched each frame.
The crosshair may have one of 8 colours as specified in the attribute word.

VSYNC from the alphaboard is resyncronized before it is presented to the ACRTC. The ACRTC then generates the timing (hsync, vsync and blanking) for the monitor.

The -2 volt reference voltage for all the ECL signal termination resistors is generated internally on the board.

2.2.1: Interface to bus:

Bus connector J1: Signal names:

Pin nr.	Row a	Row b	Row c
1	BD00	NC	BD08
2	BD01	NC	BD09
3	BD02	NC	BD10
4	BD03	NC	BD11
5	BD04	NC	BD12
6	BD05	NC	BD13
7	BD06	NC	BD14
8	BD07	NC	BD15
9	GND	NC	GND
10	*	DREQ-	RES
11	GND	DONE-	*
12	UDS-	NC	*
13	LDS-	NC	NC
14	R-W	NC	NC
15	GND	NC	BA23
16	DTACK-	*	BA22
17	GND	*	BA21
18	AS-	*	BA20
19	GND	*	BA19
20	*	GND	BA18
21	NC	NC	BA17
22	NC	NC	BA16
23	*	GND	BA15
24	BA07	IRQ7-	BA14
25	BA06	IRQ6-	BA13
26	BA05	IRQ5-	BA12
27	BA04	IRQ4-	BA11
28	BA03	IRQ3-	BA10
29	BA02	IRQ2-	BA09
30	BA01	IRQ1-	BA08
31	*	*	*

32	+5V	+5V	+5V

*) Signal may be present, but is not used on graphic board.

Bus connector J2: Signal names:

Pin nr.	Row a	Row b	Row c
1	NC	*	GND
2	CAN3	*	GND
3	CAN2	*	GND
4	CAN1	*	GND
5	CAN0	*	GND
6	*	*	GND
7	*	*	GND
8	*	*	GND
9	*	*	GND
10	*	*	GND
11	*	*	GND
12	*	*	GND
13	*	*	GND
14	*	*	GND
15	*	*	GND
16	*	*	GND
17	VSYNC-	*	GND
18	*	*	GND
19	BCLK1-	*	GND
20	*	*	GND
21	*	*	GND
22	*	*	GND
23	*	*	GND
24	NC	*	GND
25	*	*	GND
26	DCLK	*	GND
27	+5V	-5V	GND

28	+5V	-5V	GND
29	+5V	-5V	GND
30	+5V	-5V	GND
31	+5V	-5V	GND
32	+5V	-5V	GND

*) Signal may be present, but is not used on graphic board.

2.2.2: Interface to monitor:

The video monitor interface signals are situated in a 20 pin flatcable header.
The cable is twisted pair flatcable.

PIN	SIGNAL	COLOUR	DESCRIPTION:	COAX:
01	TSYN-	BROWN	TTL H+V SYNC (ACTIVE LOW)	
02	GND	L. BROWN		
03	B OUT	RED	ANALOG BLUE (75 OHM)	***
04	GND	L. BROWN		
05	G OUT	ORANGE	ANALOG GREEN (75 OHM)	***
06	GND	L. BROWN		
07	R OUT	YELLOW	ANALOG RED (75 OHM)	***
08	GND	L. BROWN		
09	TH	GREEN	TTL HALF-INTENSITY	
10	GND	L. BROWN		
11	THSYN-	BLUE	TTL HSYNC (ACTIVE LOW)	***
12	GND	L. BROWN		
13	TVSYN-	PURPLE	TTL VSYNC (ACTIVE LOW)	***
14	GND	L. BROWN		
15	TB	GRAY	TTL BLUE (OPTION)	
16	GND	L. BROWN		
17	TG	WHITE	TTL GREEN (OPTION)	
18	GND	L. BROWN		
19	TR	BLACK	TTL RED (OPTION)	
20	GND	L. BROWN		

WHEN USING A TTL MONITOR, R16 SHOULD BE CHANGED FROM 150 OHM PULL-DOWN TO 10K PULL-UP.

2.2.3: Physical dimensions:

Elongated Double Europe Card module.

Width: 234 mm.
Lenght: 340 mm.
Height: 20 mm.

2.2.4: Power Requirements:

Voltage	Typ. current
+ 5 V +-5%	2.2 A
- 5.2 V +-5%	5.3 A
+12 V	not used
-12 V	not used

2.2.5: Straps and pals:

+ designates factory installed position.

STRAPO:

Function: ACRTC interrupt level.
STRAPO is located between Vbbreg and CG08.

```
STRAPO:   .* * * * * * * * * *
           1 2 3 4 5 6 7 8 9 10
```

Jumper between pin 1 and pin 2: ACRTC int. to CPU int.req 7
Jumper between pin 1 and pin 3: ACRTC int. to CPU int.req 6
Jumper between pin 1 and pin 4: ACRTC int. to CPU int.req 5

+ Jumper between pin 1 and pin 5: ACRTC int. to CPU int.req 4
  Jumper between pin 1 and pin 6: ACRTC int. to CPU int.req 3
  Jumper between pin 1 and pin 7: ACRTC int. to CPU int.req 2
  Jumper between pin 1 and pin 8: ACRTC int. to CPU int.req 1
  Pin 9 and pin 10 is not connected.

STRAP1:

Function: Memory bank organisation; present board only supports one organisation as mentioned below.
STRAP1 is located between CG35 and CG78.

```
STRAP1:   .* *-*
           1 2 3
```

  Jumper between pin 1 and pin 2: (not supported)
+ Jumper between pin 2 and pin 3: 1 M bytes Frame Buffer

SP:

Function: Palette adr. latch option; present board only supports normal palette addressing.
SP is located between CG80 and CG05.

```
SP:       .*-*
           1 2
```

+ Jumper between pin 1 and pin 2: Normal palette mode.

STRAP3:

Function:

Function: Memory bank organisation; present board only supports one organisation corresponding to no strap connection.
STRAP3 is located between CG17 and CG33.

```
STRAP3:   .* * *
           1 2 3
```

No connections should be made on STRAP3.

CG69:

Function: Graphic start position coarse adjust and alpha sync adjust.
CG69 is located between CG39 and CG79.

lsb	CG39-3	.* 1		14 *	GND	CG39:	
	CG39-4	* 2	CG69	13 *	GND	Graphic start	
	CG39-5	* 3		12 *	GND	CG79:	
msb	CG39-6	* 4		11 *	GND	Sync. adj.	
lsb	CG79-3	* 5		10 *	N.C.		
	CG79-4	* 6		9 *	CG79-5		
	GND	* 7		8 *	CG79-6	msb	

Factory installed strap: Connections between 1,2,3,12,13,14 and between 5,6,7,8,9.

STR1:

Function: Memory bank organisation; present board only supports one organisation corresponding to the shown connection.
STR1 is located between CG34 and CG49.

```
STRAP1:   .*-* *                    1 - 2
           1 2 3
```

Jumper between pin 1 and pin 2: (not supported)
+ Jumper between pin 2 and pin 3: 1 M bytes Frame Buffer

S3:

Function: Graphic start fine adjust.
S3 ic located between IC1 and IC32.

```
S3:      * * * * *
        .* * * * *
         1 3 5 7 9
```

Jumper between pin 1 and pin 2: delay of 4 pixel clock
Jumper between pin 3 and pin 4: delay of 3 pixel clock
Jumper between pin 5 and pin 6: delay of 2 pixel clock
Jumper between pin 7 and pin 8: delay of 1 pixel clock
+ Jumper between pin 9 and pin 10: no additional delay

Pals:

CG04 (20L8):	Addr. decode for graphic board.
CG05 (16R4):	DTACK generation and select signals.
CG06 (16R4):	Math chip control signals (not used).
CG14 (20R8):	DRAM control for frame memory.
CG32 (16R4):	Control for attr. latch and addr. mux.
CG81 (16R8):	Blanking resyncronizing.

Type: SGD Backpanel

Data sheet no.:

Revision no.: 1

Date: 882101

2.4: General description:

2.4.1: Backpanel:

The panel contains six DB25 connectors used for printer/debug port, tablet/mouse, keyboard, host serial connection, and two aux connections. The panel also has one DB15 connector for an ethernet transceiver cable. The DB9 connector is not used in the present version of the SGD.
The panel is connected to the alpha board through a flatcable:

60 pin flatcable:

The 60 pin flatcable connector is used for the interconnection to the alpha board. All the serial communication signals and the +/- 12 V connections are routed via this flatcable. Refer to the technical data sheet for the alpha board for pin assignment for this connector.

The six RS-232 interface ports (DB25) each have the signals:

PIN	SIGNAL
1	Protective GND
2	TxD

3	RxD
4	RTS
5	CTS
6	DSR
7	GND
8	nc
9	-12 V (fuse 0.5 A)
10	nc
11	nc
12	nc
13	nc
14	nc
15	nc (TxC on aux ports)
16	nc
17	nc (RxC on aux ports)
18	nc
19	nc
20	DTR
21	+12 V (fuse 0.5 A)
22	nc
23	nc
24	nc
25	nc

The Ethernet transceiver cable connector (DB15) carries the signals:

PIN	SIGNAL	
1	GND	(collision pair shield)
2	CD+	(collision detect +)
3	DO+	(transmit pair +)
4	GND	(receive pair shield)
5	DI+	(receive pair +)

6	GND	(12 V RETURN)
7	NC	
8	GND	(optional shield)
9	CD-	(collision detect -)
10	DO-	(transmit pair -)
11	GND	(transmit pair shield)
12	DI-	(receive pair -)
13	+12 V	(power to transceiver)
14	GND	(power pair shield)
15	NC	

Shell is protective GND

On the rear side of the cabinet are also a power connector and a fuse, a power outlet for the monitor, an auxilary power outlet and five coax connectors for monitor signals (see: "interface to monitor" in graphic board technical data sheet).

SECTION 2.0

DDE Data Sheet for Hard Disks

DDE Data Sheet for Winchester Disk Drives. WD 1 REV. 0

MANUFACTURER: ATASI TYPE: 3046

FORM FACTOR: 5.25 inch.

ENVIRONMENT:

Electrical Interface: ST 506.

Power requirements:
+5 VDC +- 5 pct., 1.0 Amp typ.
+12 VDC +- 5 pct., 2.5 Amp typ. Starting current 4.5 A typ.

Operating temperature range: 10 to 50 deg. celsius.

CAPACITY:

Unformatted capacity: 46.3 Mb

Number of cylinders: 645

Number of heads: 7

ACCESS TIMES:

Track to track: 3.0 ms
Average: 30.0 ms
Maximum: 60.0 ms

Write precompensation from cylinder: 320
Reduced write current from cylinder: not used.

HEAD MOVE MECHANISM: track following servo.

Delay between step pulses buffered mode: Min. 2.5 us. Max. 500 us.
Delay between step pulses non buffered mode: Min. 3 ms.

HEAD LOCK MECHANISM: Automatic.

LOCATION OF STRAPS AND CONNECTORS:

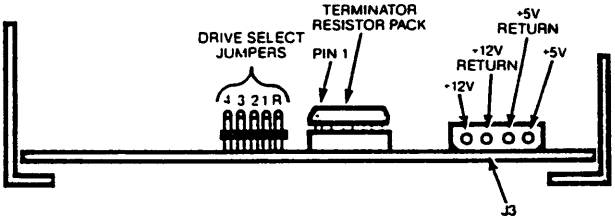


Figure 7 SELECT JUMPER, TERMINATOR AND J3 LOCATIONS

SECTION 5 — PHYSICAL INTERFACE

The interface between the disk drive and the host controller consists of four connections:

J1 — CONTROL SIGNALS

J2 — READ/WRITE SIGNALS

J3 — DC POWER

J4 — FRAME GROUND

(see Figure 14 for connector locations).

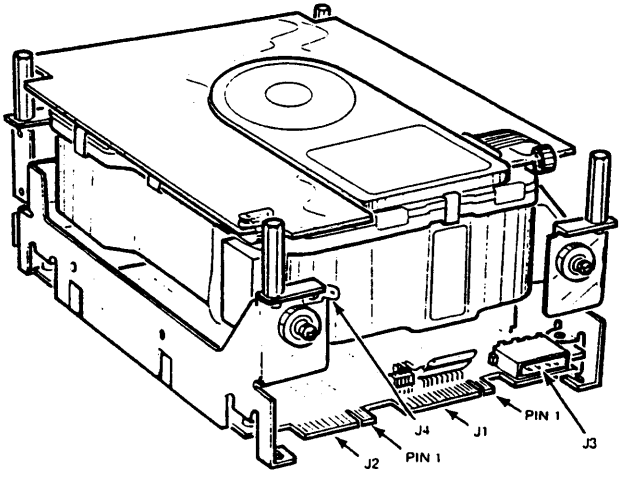


Figure 14 CONNECTOR LOCATIONS

DDE Data Sheet for Winchester Disk Drives. WD 2 REV. 0

MANUFACTURER: HITACHI TYPE: DK511-5

FORM FACTOR: 5.25 inch.

ENVIRONMENT:

Electrical Interface: ST 506.

Power requirements:
+5 VDC +- 5 pct., 2.0 Amp typ.
+12 VDC +-10 pct., 2.5 Amp typ. Starting current 5.0 A typ.

Operating temperature range: 5 to 45 deg. celsius.

CAPACITY:

Unformatted capacity: 51.0 Mb

Number of cylinders: 699

Number of heads: 7

ACCESS TIMES:

Track to track: 8.0 ms
Average: 30.0 ms
Maximum: 55.0 ms

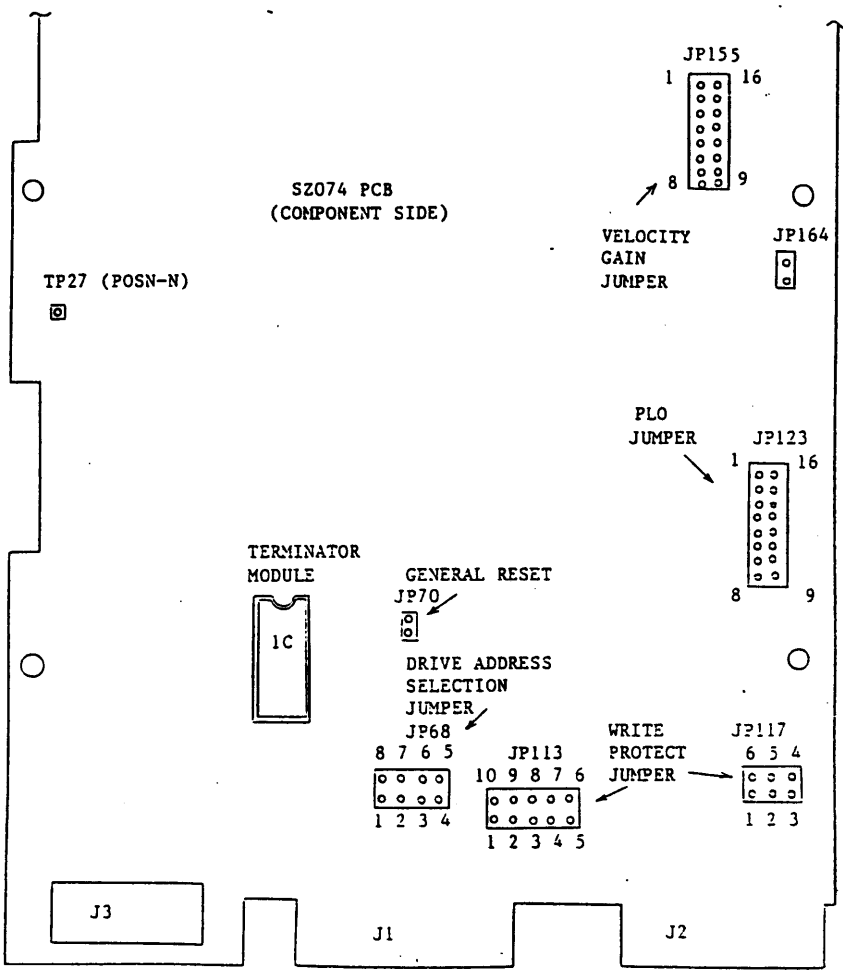
Write precompensation from cylinder: 256
Reduced write current from cylinder: not used.

HEAD MOVE MECHANISM: track following servo.

Delay between step pulses: Min. 0.3 us. Max. 100 us.

HEAD LOCK MECHANISM: None.

LOCATION OF STRAPS AND CONNECTORS:



J1: COMMAND CABLE. 34 PINS.
J2: DATA CABLE. 20 PINS.
J3: POWER CABLE.

1C: TERMINATOR MODULE.
If multiple drives are connected in daisy chain mode, only the last drive must be terminated.

JP68: Drive address selection jumper.

drive address 0:	pin 1 connected to pin 8
drive address 1:	pin 2 connected to pin 7
drive address 2:	pin 3 connected to pin 6
drive address 3:	pin 4 connected to pin 5

JP70: General RESET: Not installed.

JP113: Write protect: Jumper between pin 2 and pin 9.

JP117: Write protect: Jumper between pin 2 and pin 3.

JP164: Not installed.

JP123: Ajustment of PLO free running frequency: DO NOT CHANGE.

JP155: Ajustment of velocity gain: DO NOT CHANGE.

DDE Data Sheet for Winchester Disk Drives. WD 3 REV. 0

MANUFACTURER: HITACHI TYPE: DK511-8

FORM FACTOR: 5.25 inch.

ENVIRONMENT:

Electrical Interface: ST 506.

Power requirements:
+5 VDC +- 5 pct., 2.0 Amp typ.
+12 VDC +- 5 pct., 2.5 Amp typ. Starting current 5.0 A typ.

Operating temperature range: 5 to 45 deg. celsius.

CAPACITY:

Unformatted capacity: 85.7 Mb

Number of cylinders: 823

Number of heads: 10

ACCESS TIMES:

Track to track: 6.0 ms
Average: 25.0 ms
Maximum: 45.0 ms

Write precompensation from cylinder: not specified.
Reduced write current from cylinder: not used.

HEAD MOVE MECHANISM: track following servo.

Delay between step pulses: Min. 0.3 us. Max. 100 us.

HEAD LOCK MECHANISM: None.

LOCATION OF STRAPS AND CONNECTORS:

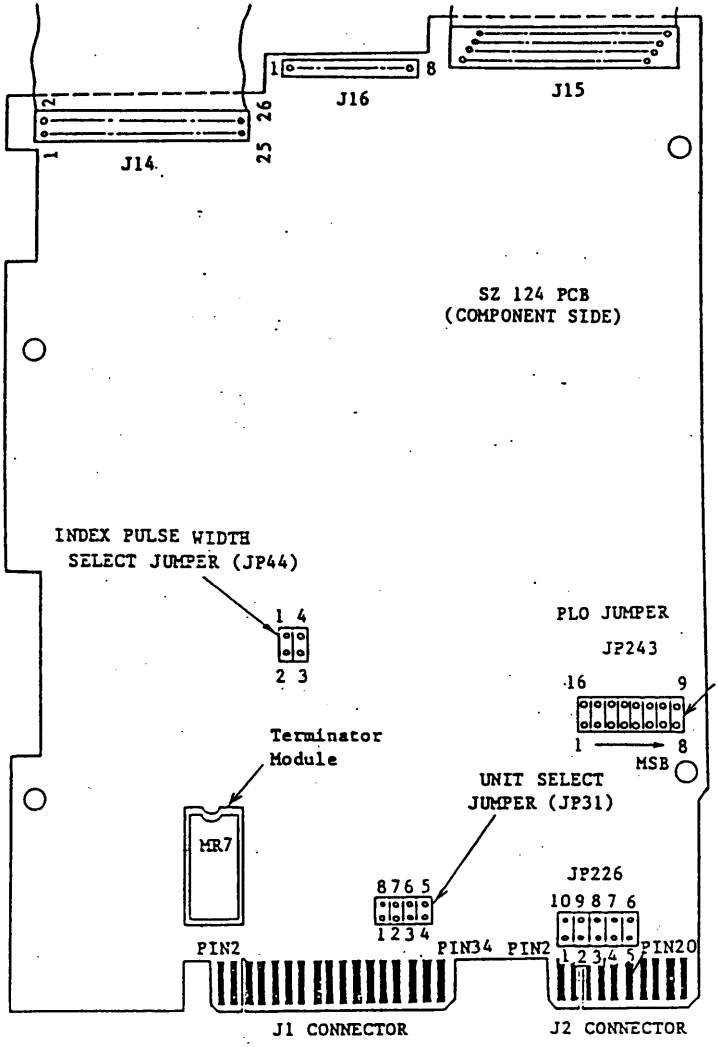


Fig. 1 DK511-8 JUMPERS ON SZ124 PCB

NOTE. The other jumpers unless stated setting-up method in this manual must not be removed.

J1: COMMAND CABLE. 34 PINS.
J2: DATA CABLE. 20 PINS.

MR7: TERMINATOR MODULE.
If multiple drives are connected in daisy chain mode, only the last drive must be terminated.

JP31: Drive address selection jumper.

drive address 0:	pin 2 connected to pin 7
drive address 1:	pin 3 connected to pin 6
drive address 2:	pin 4 connected to pin 5
drive address 3:	pin 1 connected to pin 8

JP44: Index pulse with: Jumper between pin 1 and pin 2.

JP226: Write protect: Jumper between pin 8 and pin 9.
Jumper between pin 5 and pin 6.

JP243: Ajustment of PLO free running frequency: DO NOT CHANGE.

DDE Data Sheet for Winchester Disk Drives. WD10 REV. 0

MANUFACTURER: MAXTOR TYPE: XT-3280

FORM FACTOR: 5.25"

ENVIRONMENT:

Electrical Interface: SCSI

Power requirements:
+5 VDC +- 5 pct., 1.7 Amp typ.
+12 VDC +- 5 pct., 1.8 Amp max. Starting current 4.5 A max.

Power dissipation: 30 W typ. 35 W max.

Operating temperature range: 10 to 45 deg. celsius.

Maximum temperature gradient: 10 deg. celsius/hour.

Operating humidity: 8 pct. - 95 pct. no condensation.

CAPACITY:

Unformatted capacity: 286 Mb

Number of cylinders: 1224

Number of data heads: 15

ACCESS TIMES (including settling time):

Track to track: 4.0 ms

Average: 30.0 ms

Maximum: 54.0 ms

HEAD MOVE MECHANISM:

Rotary voice coil controlled by track following servo.

HEAD LOCK MECHANISM:

Upon spin down the positioner is retracted and locked and the spindel is stopped using dynamic braking.

CONNECTORS:

J1: SCSI connector.

J2: Power connector.

Pin 1: +12 VDC.
Pin 2: +12 Return.
Pin 3: + 5 Return.
Pin 4: + 5 VDC.

+ designates factory installed position.

CONTROLLER ID:

Controller ID is set by three straps: JP 83, JP 84, JP 85.

ID	JP 85	JP 84	JP 83
0 +	out	out	out
1	out	out	in
2	out	in	out
3	out	in	in
4	in	out	out
5	in	out	in
6	in	in	out
7	in	in	in

TERMINATOR RESISTORS:

Interface terminator packs RN83, RN82, and RN81 provide proper termination for the interface lines. When more than one disk drive are connected to the SCSI cable the last disk drive and only the last disk drive on the cable must have terminators installed.

SPINDEL MOTOR JUMPER, JP 44:

+ When JP 44 is installed, the spindel motor will start as soon as power is applied.

When JP 44 is removed, the spindel motor will start after a delay time when power is applied. The delay time is 13 seconds multiplied by the the controller ID.

BUS PARITY CHECK, JP 86:

If JP 86 is not installed, the disk drive does not generate or check parity on the SCSI cable.

+ If JP 86 is installed, the disk drive generates and checks parity on the SCSI cable.

DRIVE TYPE, JP 87:

If JP 87 is installed the drive reports its type as XT-3170.

+ If JP 87 is not installed the drive reports its size as XT-3280.

BUS TERMINATOR POWER JUMPERS JP 81, JP 82:

+ If JP 81 is installed the terminator power comes from the disk drive.

If JP 82 is installed the terminator power comes from the SCSI interface.

Write Data Jumper JP 21:

Must be installed.

Write Unsafe Enable Jumper JP 43:

Must be installed.

Off-track Write Disable Jumper JP 41:

Must be installed.

Write Protect Jumper JP 42:

When JP 42 is installed, data cannot be written on the drive.

CAUTION:

Mounting screw lengths must be chosen such that no more then .125" of the screw is available to enter the frame mounting hole.

Torque applied to mounting screws must be between 9 inch*pounds and 12 inch*pounds. (1 - 1.3 Nm).

DDE Data Sheet for Winchester Disks

Manufacturer: Micropolis	**Sheet number: WD 16 rev. 0**
Type: 1680 Series	**Form Factor: 5¼" Half-Height**

Environment.

Electrical Interface: SCSI.

DC Power Requirements							
Voltage	Start-up		Idle		Seeking		Ripple
	Avg.	Peak	Avg.	Peak	Avg.	Peak	(maximum)
+5V ±5% maximum	1.0A	1.1A	1.0A	1.1	1.0A	1.1A	2%
+12 ±5% typical	1.40A	2.00A	0.80A	1.10	0.90A	2.10A	2%
maximum	2.00A	2.20A	1.10A	1.40	1.20A	2.50A	

Average power dissipation: 15 W.

Operating temperature range: 10 to 50 deg. celsius.

Storage temperature range: -40 to 65 deg. celsius.

Maximum temperature gradient: 24 deg. celsius/hour.

Operating humidity : 10 to 90 %. no condensation.

General Performance Specifications.

Seek time (including settling time)

Track-to-track: 4 msec.
Average: 14 msec.
One-Third Strike (maximum): 15 msec.
Maximum: 30 msec.

Rotational Latency Average 8.33 msec.

Media transfer rate 15Mhz.
Transfer rate at interface 1.6 Mbyte/s. (maximum)

General Functional Specifications.

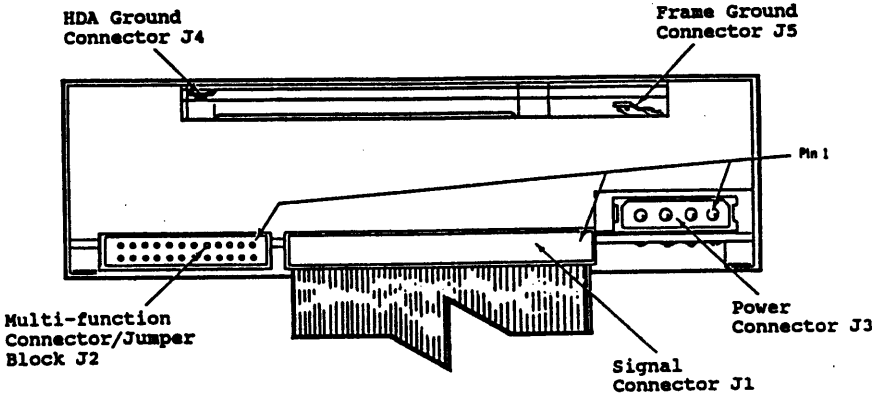
cylinders: 1780
heads: 7
Unformatted capacity 389 Mbytes

The positioner automatically retracts and losks, in a data-free landing zone, on spin-down.

Mounting.

Recommemded orientation is vertical on either side, or horizontal with the device electronics board down.

Connectors.



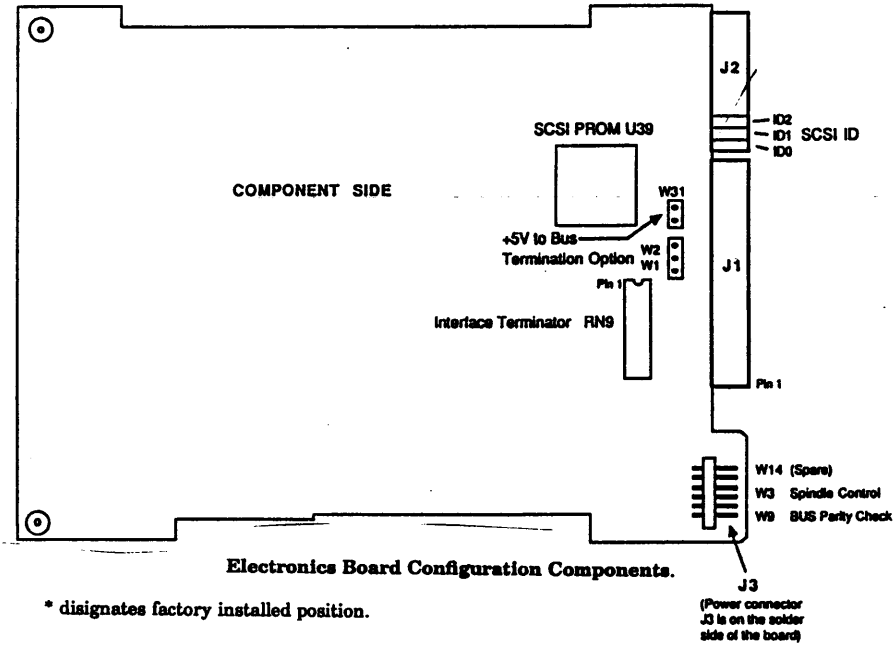
Power and Interface Connections.

J1: SCSI connector

J2: Multi-function connector

J3: Power connector
Pin 1: +12 VDC
Pin 2: +12 Return
Pin 3: +5 Return
Pin 4: +5 VDC

Configuration options.



Electronics Board Configuration Components.

* disignates factory installed position.

SCSI controller ID			
SCSI ID	ID2	ID1	ID0
ID0	-	-	-
ID1	-	-	x
ID2	-	x	-
ID3	-	x	x
ID4	x	-	-
ID5	x	-	x
ID6	x	x	-
ID7	x	x	x

SCSI jumpers is located in J2, ID0 pin1-2, ID1 pin 3-4, ID2 pin 5-6.

Terminator resistors.

Interface terminator pack RN9 provide termination for the interface lines. When more than one disk drive are connected to the SCSI cable the last disk drive and only the last disk drive on the cable must have terminator installed.

BUS termination power.

A jumper must be installed at W1 or W2 to select the source of power to the termination.
* When a jumper is installed in W1, the drive provides terminator power.
When a jumper is installed in W2, terminator power is provided by the host system via interface cable J1 pin 26.

When a jumper is installed at both W2 and W31, the drive provides terminator power to its own terminators, and also to the SCSI cable J1 pin 26. * Not installed.

BUS parity check.

When a jumper is installed at W9, the disk drive does not generate or check parity on the SCSI cable.
* When a jumper is not installed at W9, the disk drive generates and checks parity on the SCSI cable.

Spindle control.

When a jumper is installed at W3 the disk drive must wait for a Start motor command to start the spindle motor.
* When a jumper is not installed in W3, the drive starts the spindle motor at power up.

Documentation.

Publications available from Micropolis:

Product Description Micropolis 1680 Series.
Tecnical Manual Micropolis 1680 Series.

DDE Data Sheet for Winchester Disks

Manufacturer: Micropolis	**Sheet number: WD 15 rev. 0**
Type: 1670 Series	**Form Factor: 5¼" Half-Height**

Environment.

Electrical Interface: SCSI.

DC Power Requirements							
Voltage	Start-up		Idle		Seeking		Ripple
	Avg.	Peak	Avg.	Peak	Avg.	Peak	(maximum)
+5V ±5% maximum	2.3A	2.3A	2.3A	2.3	2.3A	2.3A	2%
+12 ±5%							2%
typical	1.75A	2.00A	0.60A	0.90	0.90A	1.80A	
maximum	2.00A	2.00A	0.88A	1.00	1.10A	2.00A	

Average power dissipation: 22 W.

Operating temperature range: 10 to 50 deg. celsius.

Storage temperature range: -40 to 65 deg. celsius.

Maximum temperature gradient: 24 deg. celsius/hour.

Operating humidity : 10 to 90 %. no condensation.

General Performance Specifications.

Seek time (including settling time)

Track-to-track: 4 msec.
Average: 16 msec.
One-Third Strike (maximum): 18 msec.
Maximum: 37 msec.

Rotational Latency Average 8.33 msec.

Media transfer rate 10Mhz.
Transfer rate at interface 1.6 Mbyte/s. (maximum)

General Functional Specifications.

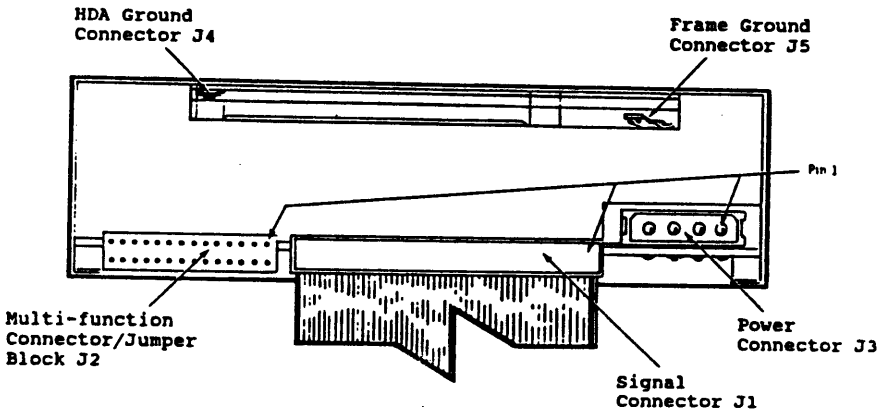
cylinders: 1245
heads: 7
Unformatted capacity 182 Mbytes

The positioner automatically retracts and losks, in a data-free landing zone, on spin-down.

Mounting.

Recommemded orientation is vertical on either side, or horizontal with the device electronics board down.

Connectors.



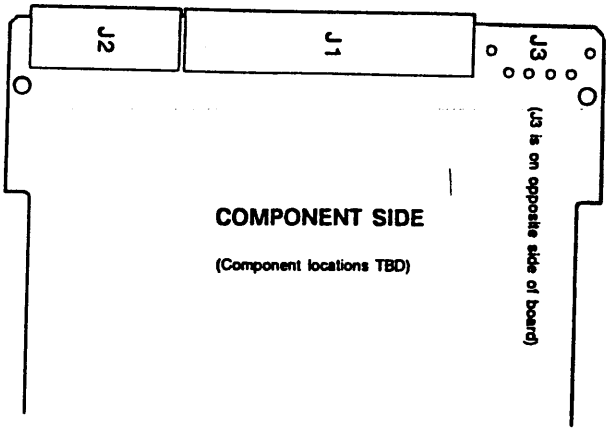
Power and Interface Connections.

J1: SCSI connector

J2: Multi-function connector

J3: Power connector
Pin 1: +12 VDC
Pin 2: +12 Return
Pin 3: +5 Return
Pin 4: +5 VDC

Configuration options.



Electronics Board Configuration Components.

* disignates factory installed position.

SCSI controller ID			
SCSI ID	ID2	ID1	ID0
ID0	-	-	-
ID1	-	-	x
ID2	-	x	-
ID3	-	x	x
ID4	x	-	-
ID5	x	-	x
ID6	x	x	-
ID7	x	x	x

SCSI jumpers is located in J2, ID0 pin1-2, ID1 pin 3-4, ID2 pin 5-6.

Terminator resistors.

Interface terminator pack RN9 provide termination for the interface lines. When more than one disk drive are connected to the SCSI cable the last disk drive and only the last disk drive on the cable must have terminator installed.

BUS termination power.

A jumper must be installed at W1 or W2 to select the source of power to the termination.
* When a jumper is installed in W1, the drive provides terminator power.
When a jumper is installed in W2, terminator power is provided by the host system via interface cable J1 pin 26.

BUS parity check.

When a jumper is installed at W9, the disk drive does not generate or check parity on the SCSI cable.
* When a jumper is not installed at W9, the disk drive generates and checks parity on the SCSI cable.

Spindle control.

When a jumper is installed at W3 the disk drive must wait for a Start motor command to start the spindle motor.
* When a jumper is not installed in W3, the drive starts the spindle motor at power up.

Documentation.

Publications available from Micropolis:

Product Description Micropolis 1670 Series.
Tecnical Manual Micropolis 1670 Series.

DDE Data Sheet for Winchester Disks

Manufacturer: Micropolis	**Sheet number: WD 14 rev. 0**
Type: 1580 Series	**Form Factor: 5¼"**

Environment.

Electrical Interface: SCSI.

DC Power Requirements							
Voltage	Start-up		Idle		Seeking		Ripple
	Avg.	Peak	Avg.	Peak	Avg.	Peak	(maximum)
+5V ±5% maximum	2.0A	2.0A	2.0A	2.0	2.0A	2.0A	2%
+12 ±5% typical	4.25A	4.25A	1.80A	1.90	2.25A	3.10A	2%
maximum	4.35A	4.35A	2.00A	2.10	2.45A	3.30A	

Average power dissipation: 33 W.

Operating temperature range: 10 to 50 deg. celsius.

Storage temperature range: -40 to 65 deg. celsius.

Maximum temperature gradient: 24 deg. celsius/hour.

Operating humidity : 10 to 90 %. no condensation.

General Performance Specifications.

Seek time (including settling time)

Track-to-track: 4 msec.
Average: 16 msec.
One-Third Strike (maximum): 17 msec.
Maximum: 35 msec.

Rotational Latency Average 8.33 msec.

Media transfer rate 15Mhz.
Transfer rate at interface 1.6 Mbyte/s. (maximum)

General Functional Specifications.

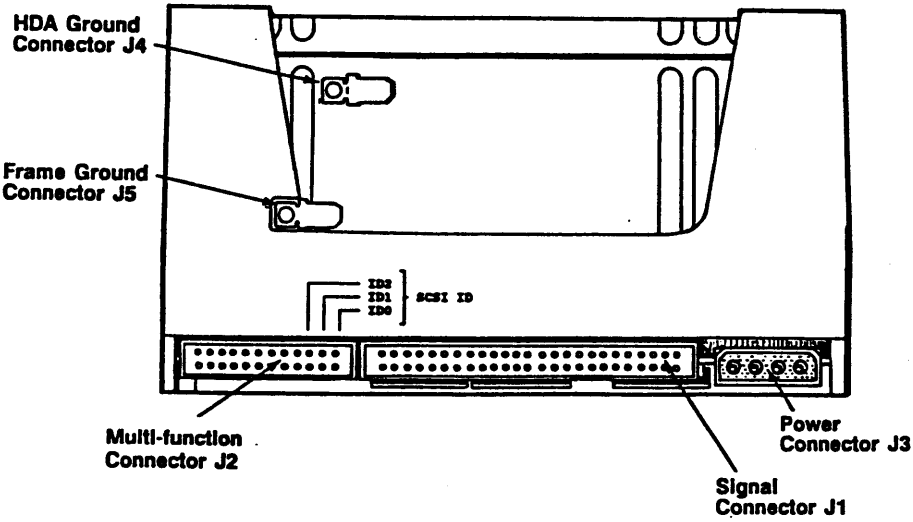
cylinders: 1632
heads: 15
Unformatted capacity 765 Mbytes

The positioner automatically retracts and losks, in a data-free landing zone, on spin-down.

Mounting.

Recommemded orientation is vertical on either side, or horizontal with the device electronics board down.

Connectors.



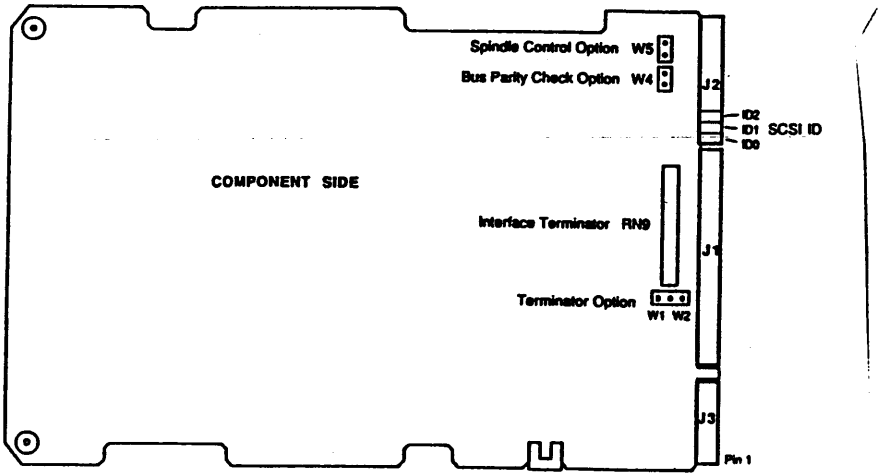
Power and Interface Connections.

J1: SCSI connector

J2: Multi-function connector

J3: Power connector
Pin 1: +12 VDC
Pin 2: +12 Return
Pin 3: +5 Return
Pin 4: +5 VDC

Configuration options.



Electronics Board Configuration Components.

* disignates factory installed position.

SCSI controller ID			
SCSI ID	ID2	ID1	ID0
ID0	-	-	-
ID1	-	-	x
ID2	-	x	-
ID3	-	x	x
ID4	x	-	-
ID5	x	-	x
ID6	x	x	-
ID7	x	x	x

Terminator resistors.

Interface terminator pack RN9 provide termination for the interface lines. When more than one disk drive are connected to the SCSI cable the last disk drive and only the last disk drive on the cable must have terminator installed.

BUS termination power.

A jumper must be installed at W1 or W2 to select the source of power to the termination.
* When a jumper is installed in W1, the drive provides terminator power.
When a jumper is installed in W2, terminator power is provided by the host system via interface cable J1 pin 26.

BUS parity check.

When a jumper is installed at W4, the disk drive does not generate or check parity on the SCSI cable.
* When a jumper is not installed at W4, the disk drive generates and checks parity on the SCSI cable.

Spindle control.

When a jumper is installed at W5 the disk drive must wait for a Start motor command to start the spindle motor.
* When a jumper is not installed in W5, the drive starts the spindle motor at power up.

Documentation.

Publications available from Micropolis:

Product Description Micropolis 1580 Series.
Tecnical Manual Micropolis 1580 Series.

DDE Data Sheet for Winchester Disk Drives. WD 13 REV. 0

MANUFACTURER: MICROPOLIS TYPE: 1373

FORM FACTOR: 5.25"

ENVIRONMENT:

Electrical Interface: SCSI

Power requirements:
+5 VDC +- 5 pct., 2.0 Amp max.
+12 VDC +- 5 pct., 3.3 Amp max. Starting current 4.35 A max.

Average power dissipation: 38 W.

Operating temperature range: 10 to 50 deg. celsius.

Maximum temperature gradient: 24 deg. celsius/hour.

Operating humidity: 10 pct. - 90 pct. no condensation.

CAPACITY:

Unformatted capacity: 85 Mb

NNumber of cylinders: 1016

Number of heads: 4

ACCESS TIMES (including settling time):

Track to track: 5.0 ms

Average: 23.0 ms

One-Third stroke: 25.0 ms

Maximum: 50.0 ms

HEAD MOVE MECHANISM:

Rotary voice coil controlled by track following servo.

HEAD LOCK MECHANISM:

Upon spin down the positioner is retracted and locked and the spindel motor brake is applied.

CONNECTORS:

J1: SCSI connector.

J2: Multi function connector.

J3: Power connector.

Pin 1: +12 VDC.
Pin 2: +12 Return.
Pin 3: + 5 Return.
Pin 4: + 5 VDC.

J4: Head Disk Assembly ground connector.

J5: Outer Frame ground connector.

+ disignates factory installed position.

CONTROLLER ID:

The controller ID is set by three straps in J2.

Strap between pin 1 and pin 2 in J2: ID0
Strap between pin 3 and pin 4 in J2: ID1
Strap between pin 5 and pin 6 in J2: ID2

ID	ID2	ID1	ID0
0 +	out	out	out
1	out	out	in
2	out	in	out
3	out	in	in
4	in	out	out
5	in	out	in
6	in	in	out
7	in	in	in

TERMINATOR RESISTORS:

Interface terminator packs RN1, RN7, and RN8 provide proper termination for the interface lines. When more than one disk drive are connected to the SCSI cable the last disk drive and only the last disk drive on the cable must have terminators installed.

SPINDEL CONTROL OPTION:

If J2 pin 7 is connected to J2 pin 8, the disk drive will wait for a Start Spindle Command to start the spindle motor.

+ If J2 pin 7 and J2 pin 8 are not connected, the disk drive starts the spindle motor at power up.

BUS PARITY CHECK:

If J2 pin 9 and J2 pin 10 are connected, the disk drive does not generate or check parity on the SCSI cable.

+ If J2 pin 9 and J2 pin 10 are not connected, the disk drive generates and checks parity on the SCSI cable.

BUS TERMINATION POWER:

A jumper must be installed at W1 or W2 to select the source of power to the terminator packs RN1, RN7, and RN8.

+ When the jumper is installed at W1, the disk drive provides terminator power.

When the jumper is installed at W2, terminator power is provided by the host system via interface cable J1 pin 26.

Note: The maximum torque applied to mounting screws must not exceed 10 inch*lbs. (1.1 Nm).

DDE Data Sheet for Winchester Disks

Manufacturer: Micropolis	**Sheet number: WD 12 rev. 1**
Type: 1570 Series	**Form Factor: 5¼"**

Environment.

Electrical Interface: SCSI.

DC Power Requirements							
Voltage	Start-up		Idle		Seeking		Ripple
	Avg.	Peak	Avg.	Peak	Avg.	Peak	(maximum)
+5V ±5% maximum	2.0A	2.0A	2.0A	2.0	2.0A	2.0A	2%
+12 ±5% typical	4.25A	4.25A	1.80A	1.90	2.25A	3.10A	2%
maximum	4.35A	4.35A	2.00A	2.10	2.45A	3.30A	

Average power dissipation: 38 W.

Operating temperature range: 10 to 50 deg. celsius.

Storage temperature range: -40 to 65 deg. celsius.

Maximum temperature gradient: 24 deg. celsius/hour.

Operating humidity : 10 to 90 %. no condensation.

General Performance Specifications.

Seek time (including settling time)

Track-to-track: 4 msec.
Average: 18 msec.
One-Third Strike (maximum): 19 msec.
Maximum: 40 msec.

Rotational Latency Average 8.33 msec.

Media transfer rate 10Mhz.
Transfer rate at interface 1.6 Mbyte/s. (maximum)

General Functional Specifications.

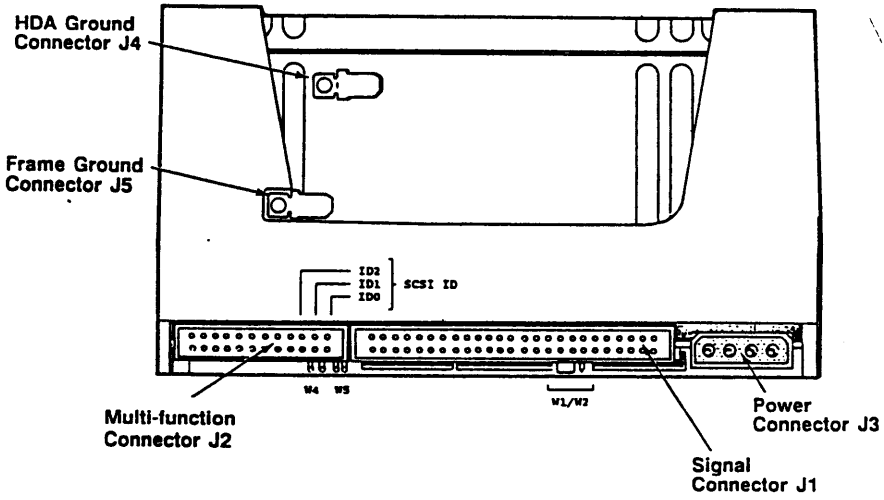
cylinders: 1224
heads: 15
Unformatted capacity 382 Mbytes

The positioner automatically retracts and losks, in a data-free landing zone, on spin-down.

Mounting.

Recommemded orientation is vertical on either side, or horizontal with the device electronics board down.

Connectors.



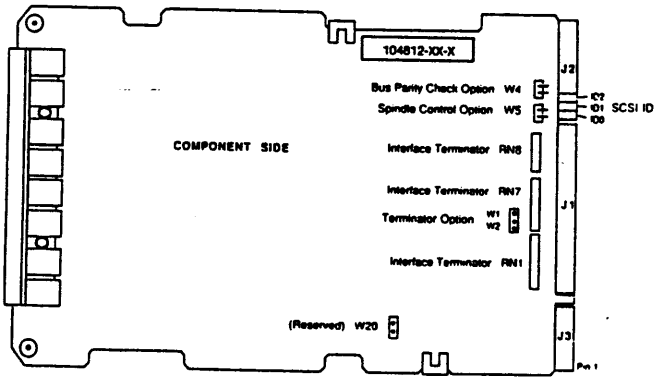
Power and Interface Connections.

J1: SCSI connector

J2: Multi-function connector

J3: Power connector
Pin 1: +12 VDC
Pin 2: +12 Return
Pin 3: +5 Return
Pin 4: +5 VDC

Configuration options.



Electronics Board Configuration Components.

* disignates factory installed position.

SCSI controller ID			
SCSI ID	ID2	ID1	ID0
ID0	-	-	-
ID1	-	-	x
ID2	-	x	-
ID3	-	x	x
ID4	x	-	-
ID5	x	-	x
ID6	x	x	-
ID7	x	x	x

Terminator resistors.

Interface terminator packs RN1, RN7, and RN8 provide termination for the interface lines. When more than one disk drive are connected to the SCSI cable the last disk drive and only the last disk drive on the cable must have terminators installed.
Please note that the orientation of the terminators differs on different versions of the board. Pin 1 is marked on the board.

BUS termination power.

A jumper must be installed at W1 or W2 to select the source of power to the termination.
* When a jumper is installed in W1, the drive provides terminator power.
When a jumper is installed in W2, terminator power is provided by the host system via interface cable J1 pin 26.

BUS parity check.

When a jumper is installed at W4, the disk drive does not generate or check parity on the SCSI cable.
* When a jumper is not installed at W4, the disk drive generates and checks parity on the SCSI cable.

Spindle control.

When a jumper is installed at W5 the disk drive must wait for a Start motor command to start the spindle motor.
* When a jumper is not installed in W5, the drive starts the spindle motor at power up.

Documentation.

Publications available from Micropolis:

Product Description Micropolis 1570 Series.
Tecnical Manual Micropolis 1570 Series.

DDE Data Sheet for Winchester Disk Drives. WD 9 REV. 0

MANUFACTURER: MICROPOLIS TYPE: 1375

FORM FACTOR: 5.25"

ENVIRONMENT:

Electrical Interface: SCSI

Power requirements:
+5 VDC +- 5 pct., 2.0 Amp max.
+12 VDC +- 5 pct., 3.3 Amp max. Starting current 4.35 A max.

Average power dissipation: 38 W.

Operating temperature range: 10 to 50 deg. celsius.

Maximum temperature gradient: 24 deg. celsius/hour.

Operating humidity: 10 pct. - 90 pct. no condensation.

CAPACITY:

Unformatted capacity: 170 Mb

Number of cylinders: 1016

Number of heads: 8

ACCESS TIMES (including settling time):

Track to track: 5.0 ms

Average: 23.0 ms

One-Third stroke: 25.0 ms

Maximum: 50.0 ms

HEAD MOVE MECHANISM:

Rotary voice coil controlled by track following servo.

HEAD LOCK MECHANISM:

Upon spin down the positioner is retracted and locked and the spindel motor brake is applied.

CONNECTORS:

J1: SCSI connector.

J2: Multi function connector.

J3: Power connector.

Pin 1: +12 VDC.
Pin 2: +12 Return.
Pin 3: + 5 Return.
Pin 4: + 5 VDC.

J4: Head Disk Assembly ground connector.

J5: Outer Frame ground connector.

+ disignates factory installed position.

CONTROLLER ID:

The controller ID is set by three straps in J2.

Strap between pin 1 and pin 2 in J2: IDO
Strap between pin 3 and pin 4 in J2: ID1
Strap between pin 5 and pin 6 in J2: ID2

ID	ID2	ID1	IDO
0 +	out	out	out
1	out	out	in
2	out	in	out
3	out	in	in
4	in	out	out
5	in	out	in
6	in	in	out
7	in	in	in

TERMINATOR RESISTORS:

Interface terminator packs RN1, RN7, and RN8 provide proper termination for the interface lines. When more than one disk drive are connected to the SCSI cable the last disk drive and only the last disk drive on the cable must have terminators installed.

SPINDEL CONTROL OPTION:

If J2 pin 7 is connected to J2 pin 8, the disk drive will wait for a Start Spindle Command to start the spindle motor.

+ If J2 pin 7 and J2 pin 8 are not connected, the disk drive starts the spindle motor at power up.

BUS PARITY CHECK:

If J2 pin 9 and J2 pin 10 are connected, the disk drive does not generate or check parity on the SCSI cable.

+ If J2 pin 9 and J2 pin 10 are not connected, the disk drive generates and checks parity on the SCSI cable.

BUS TERMINATION POWER:

A jumper must be installed at W1 or W2 to select the source of power to the terminator packs RN1, RN7, and RN8.

+ When the jumper is installed at W1, the disk drive provides terminator power.

When the jumper is installed at W2, terminator power is provided by the host system via interface cable J1 pin 26.

Note: The maximum torque applied to mounting screws must not exceed 10 inch*lbs. (1.1 Nm).

DDE Data Sheet for Winchester Disk Drives. WD 5 REV. 0

MANUFACTURER: MICROPOLIS TYPE: 1325

FORM FACTOR: 5.25 inch.

ENVIRONMENT:

Electrical Interface: ST 506.

Power requirements:
+5 VDC +- 5 pct., 0.9 Amp average.
+12 VDC +- 5 pct., 3.3 Amp average. Peak current 3.9 A.

Operating temperature range: 10 to 46 deg. celsius.

Thermal Shock: max. 24 deg. celcius/hour.

This gradient should not be exceeded when moving drive from storage to operation.

CAPACITY:

Unformatted capacity: 85.3 Mb

Number of cylinders: 1024

Number of heads: 8

Maximum number of defective tracks: 85

ACCESS TIMES (including settling time):

Track to track: 6.0 ms
Average: 28.0 ms
Maximum: 62.0 ms

Write precompensation must NOT be used.

Reduced write current from cylinder: not used.

HEAD MOVE MECHANISM: track following servo. Rotary voice coil.

Delay between step pulses: 2 us to 200 us or > 1ms.

Step periods exceeding 20 us will extend access times.

HEAD LOCK MECHANISM: Automatic.

LOCATION OF AND CONNECTORS: Figure 3-1.

J1: COMMAND CABLE. 34 PINS.
J2: DATA CABLE. 20 PINS.
J3: DC POWER INPUT.
J4: FRAME GROUND.

LOCATION OF STRAPS: Figure 3-2.

RN1: TERMINATOR MODULE.

If multiple drives are connected in daisy chain mode, only the last drive must be terminated.

J6: Drive address selection jumper. SHUNT BLOCK Figure 6-1.

DS4 installed: Drive address 4.
DS3 installed: Drive address 3.
DS2 installed: Drive address 2.
DS1 installed: Drive address 1.

Only one connection must be installed.

W2: installed.
W1: Not installed

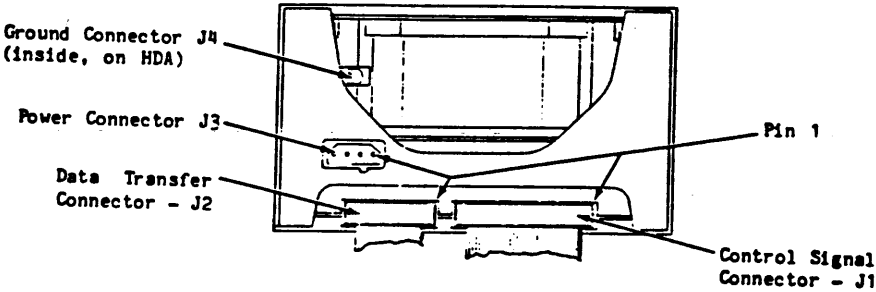
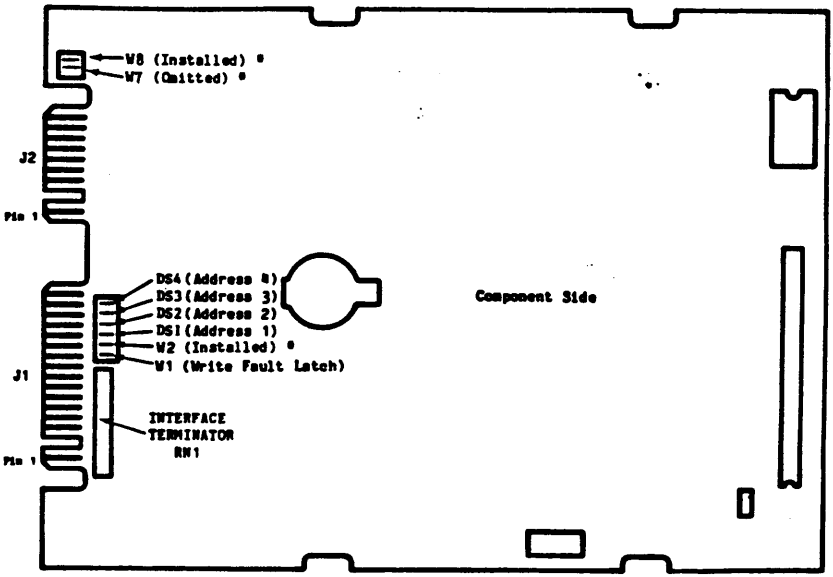


Figure 3-1. Power and Interface Connections



* Options. See Maintenance Manual Micropolis No. 101420.

Figure 3-2. Drive-Address Jumpers and Interface Terminator

DDE Data Sheet for Winchester Disk Drives. WD 7 REV. 0

MANUFACTURER: NEC TYPE: D5126

FORM FACTOR: 5.25"

ENVIRONMENT:

Electrical Interface: ST 506

Power requirements:
+5 VDC +- 5 pct., 1.0 Amp max.
+12 VDC +- 5 pct., 1.8 Amp max. Starting current 2.5 A max.

Temperature range: 5 to 50 deg. celsius.

Humidity: 8 pct. - 80 pct. no condensation.

CAPACITY:

Unformatted capacity: 25.6 Mb

Number of cylinders: 615

Number of heads: 4

ACCESS TIMES (including settling time):

Track to track: 18.0 ms

Average: 85.0 ms

Maximum: 215.0 ms

Write precompensation from cylinder: 128
Reduced write current from cylinder: not used.

HEAD MOVE MECHANISM: Stepper motor.

Delay between step pulses buffered mode: Min. 3 us. Max. 200 us.

Delay between step pulses non buffered mode: Min. 3 ms.

HEAD LOCK MECHANISM: Automatic.

Before power off, for transportation, it is recommended that the controller commands the drive to seek to cylinder 664.

SWITCHES:

Disk drive number:
DIP switch located in position 02:

SWITCH NUMBER :	1	2	3	4	5	6	7	8
drive number 1:	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
SWITCH NUMBER :	1	2	3	4	5	6	7	8
drive number 2:	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
SWITCH NUMBER :	1	2	3	4	5	6	7	8
drive number 3:	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
SWITCH NUMBER :	1	2	3	4	5	6	7	8
drive number 4:	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF

TERMINATOR RESISTORS:

Terminator resistors are switched on/off by a DIP switch located in position 2D. When the switches are ON the terminator resistors are connected to the disk drive. When more than one disk drive are connected to a controller in daisy chain only the last disk drive in the chain must have the terminator resistors connected.

DDE Data Sheet for Winchester Disk Drives. WD 6 REV. 0

MANUFACTURER: NEC TYPE: D2257

FORM FACTOR: 8"

ENVIRONMENT:

Electrical Interface: SMD

Power requirements:
+5 VDC +- 5 pct., 4.0 Amp typ.
-12 VDC +- 5 pct., 1.0 Amp typ.
+24 VDC +-10 pct., 3.0 Amp typ. Starting current 5.5 Amp.

Temperature range: 5 to 40 deg. celsius.

Relative humidity: 20 pct. - 80 pct without condensation.

CAPACITY:

Unformatted capacity: 167.7 Mb

Number of cylinders: 1024

Number of heads: 8

ACCESS TIMES:

Track to track: 5.0 ms

Average: 20.0 ms

Maximum: 40.0 ms

HEAD MOVE MECHANISM: Track following servo. Rotary actuator.

HEAD LOCK MECHANISM: MANUAL.

SWITCHES:

INSTALLATION MODE DIP SWITCH. Position 14A.

BIT(1:4): Binary coded unit number. BIT(1): MSB. BIT(4): LSB.
BIT(5): Address mode switch.
BIT(6): Servo offset control
BIT(7): Motor start delay.
BIT(8): Motor start mode.

	Bit no.	1	2	3	4	5	6	7	8
DDE factory setting:		0	0	0	0	0	0	0	0

If two disk drives are connected to the same controller, switch setting on the second disk drive must be changed to:

	Bit no.	1	2	3	4	5	6	7	8
		0	0	0	1	0	0	1	0

Do not change bit 5, 6, and 8.

CONTROL MODE DIP SWITCH. DO NOT CHANGE. Position 13M.

BIT(1:3): Device type.
BIT(4): AM mode select.
BIT(5): RPS mode select.
BIT(6): FWRF mode select
BIT(7): TAG4 control
BIT(8): Interface control.

	Bit no.	1	2	3	4	5	6	7	8
DDE factory setting:		0	0	0	1	0	0	0	1

SECTOR SELECT SWITCHES. Position 14M.

Bit no.	1 2 3 4 5 6 7 8
DDE factory setting	0 1 0 0 0 0 0 0

This switch setting must be used when ther disk drive is controlled by NEC DS800B

If the disk drive is controlled by XEBEC S1490 the switch setting must be changed to:

Bit no.	1 2 3 4 5 6 7 8
Disk drive number	0 1 1 1 0 0 0 0

TERMINATOR RESISTORS:

Terminator resistors must only be installed in the last disk drive in the daisy chain, when more than one disk drive are connected to the the same controller.

The terminator resistors are four dual-in-line packages palced in positions 17F, 17G, 17H, and 17J close to connector P1 on board G9QSV.

DDE Data Sheet for Winchester Disk Drives. WD 8 REV. 0

MANUFACTURER: PERTEC TYPE: DX332

FORM FACTOR: 8"

ENVIRONMENT:

Electrical Interface: SMD.

Power requirements:
+24 VDC +-10 pct., 4.5 Amp typ. Maximum current 12 Amp.
+24 VDC +-10 pct., 1.0 Amp typ. Maximum current 3 Amp.
+ 5 VDC +- 3 pct., 2.2 Amp typ. Maximum current 3 Amp.
- 5.2 VDC +- 3 pct., 2.9 Amp typ. Maximum current 3 Amp.

Temperature range: 10 to 40 deg. celsius operating.
Relative humidity 10 pct. - 80 pct. operating.
Maximum shipping an storage altitude: 6096 meters.

NOTE: "It is recommended that power be applied to the drive 30 minutes prior to recording of data."

CAPACITY:

Unformatted capacity: 332.4 Mb

Number of cylinders: 1649

Number of heads: 10

ACCESS TIMES:

Track to track: 5 ms

Average: 22 ms

Maximum: 45 ms

HEAD MOVE MECHANISM: track following servo.

HEAD LOCK MECHANISM: Automatic.

SWITCHES:

SW3(1): 1 = disable write
0 = enable write

SW3(2): Not used.

SW3(3:4): Drive type. 0 0 for DX332.

SW3(5:8): Sector clock switches

DDE factory switch setting:

BIT number:	1	2	3	4	5	6	7	8
SW3:	0	0	0	0	0	0	0	1

SW2(1:8): Sector clock switches

DDE factory switch setting:

BIT number:	1	2	3	4	5	6	7	8
SW2:	1	0	1	1	0	0	0	0

SW1(1:8): Not used

DDE factory switch setting:

BIT number:	1	2	3	4	5	6	7	8
SW1:	1	0	0	0	0	0	0	0

0 = switch open
1 = switch closed

DISK DRIVE NUMBER:

DIP switch position U20

BIT(4:1): binary coded unit number. BIT(4) MSB, BIT(1) LSB.

DDE factory switch setting:

BIT number:	1	2	3	4	5	6	7	8
U20:	0	0	0	0	0	0	0	1

TERMINATOR RESISTORS:

Terminator resistors are mounted on a printed circuit board J3 placed in connector J1A2. When two or more disk drives are connected in a daisy chain, only the last disk drive must contain pull up resistors.

DDE Data Sheet for Winchester Disk Drives. WD 11 REV. 1

MANUFACTURER: PRIAM TYPE: 717, 728, 738

FORM FACTOR: 5.25"

ENVIRONMENT:

Electrical Interface: SCSI

Power requirements:
+5 VDC +- 5 pct., 2.1 Amp max.
+12 VDC +- 5 pct., 4.0 Amp max. Starting current 4.5 A max.

Average power dissipation: 38 W.

Operating temperature range: 10 to 50 deg. celsius.

Maximum temperature gradient: 15 deg. celsius/hour.

Operating humidity: 8 pct. - 80 pct. no condensation.

CAPACITY:	717	728	738
Unformatted capacity:	170 Mbyte	280 Mbyte	380 Mbyte
Number of cylinders:	1225	1225	1225
Number of heads:	7	11	15

ACCESS TIMES (including settling time):

Track to track:	5.0 ms
Average (1/3 stroke):	20.0 ms
Maximum:	30.0 ms

HEAD MOVE MECHANISM:

Linear voice coil controlled by track following servo.

HEAD LOCK MECHANISM:

Upon spin down the positioner is retracted and locked and the spindel motor brake is applied.

CONNECTORS:

J1: SCSI connector.

J3: Power connector.

Pin 1: +12 VDC.
Pin 2: +12 Return.
Pin 3: + 5 Return.
Pin 4: + 5 VDC.

J11: Jumper settings.

J14: Frame ground connector.

+ disignates factory installed position.

JUMPER SETTING:

controller ID:

The controller ID is set by three straps in J11.

Strap between pin 1 and pin 2 in J11: ID1
Strap between pin 3 and pin 4 in J11: ID2
Strap between pin 5 and pin 6 in J11: ID4

ID	ID4	ID2	ID1
0 +	out	out	out
1	out	out	in
2	out	in	out
3	out	in	in
4	in	out	out
5	in	out	in
6	in	in	out
7	in	in	in

J11 pin 7-8:

in+ : auto sequence up

J11 pin 9-10

in+ : parity enable

J11 : pin 11-12, 13-14:

out+ : blocksize selected by software.

J11 : pin 15-16

out+ : unit attention enabled

J11 : pin 17-18

output: drive ready (not used)

J11 : pin 19-20

out+ : disable write protect

Jumper W3:

out+: soft scsi bus reset

Jumper W5:

out+: no delay on motor start (this jumper is not mounted on all versions of the controller board)

Jumper W6:

in+: terminator power to j1-26

TERMINATOR RESISTORS:

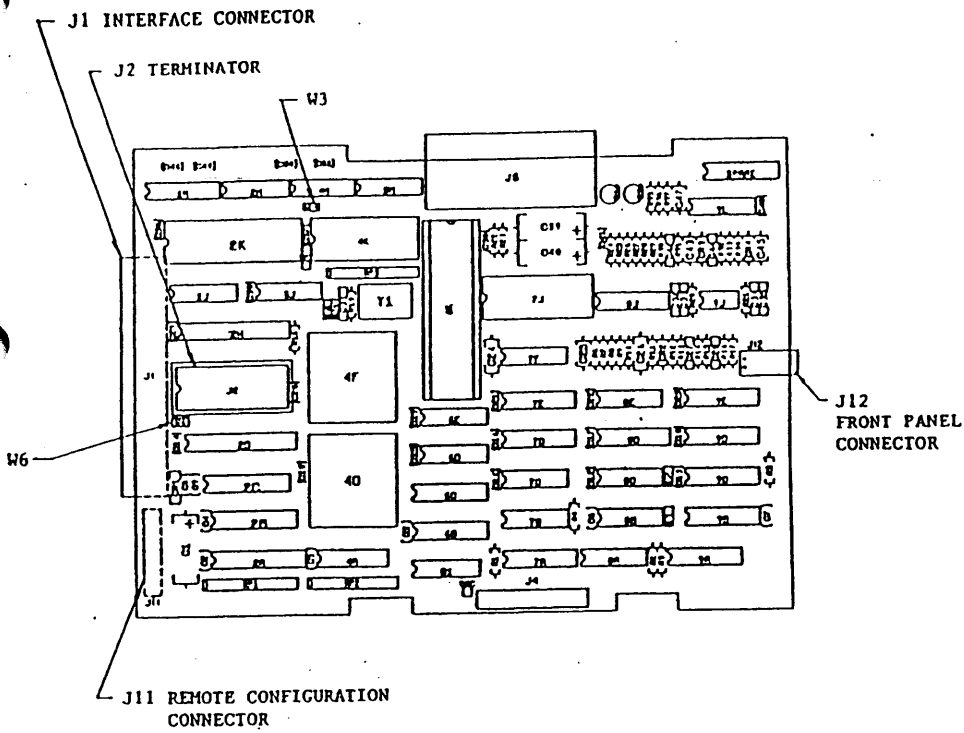
Interface terminator pack J2 provide proper termination for the interface lines. When more than one disk drive are connected to the SCSI cable the last disk drive and only the last disk drive on the cable must have terminators installed.

DOCUMENTATION:

Publications available from PRIAM:

OEM/service manual 717/728/738 winchester disk drives.
P/N 308080

Priam specification models 717, 728, and 738 SCSI interface.
P/N 300971



SCSI interface connector/switch placement

DDE Data Sheet for Winchester Disk Drives. WD 4 REV. 0

MANUFACTURER: VERTEX TYPE: V185

FORM FACTOR: 5.25 inch.

ENVIRONMENT:

Electrical Interface: ST 506.

Power requirements:
+5 VDC +- 5 pct., 1.5 Amp typ.
+12 VDC +-10 pct., 2.8 Amp typ. Starting current 4.5 A typ.

Operating temperature range: 4 to 50 deg. celsius.

CAPACITY:

Unformatted capacity: 85.0 Mb

Number of cylinders: 1166

Number of heads: 7

Maximum number of defective tracks: 85

ACCESS TIMES:

Track to track:	5.0 ms
Average:	30.0 ms
Maximum:	65.0 ms

Write precompensation must NOT be used.

Reduced write current from cylinder: not used.

HEAD MOVE MECHANISM: track following servo. Rotary voice coil.

Delay between step pulses: Min. 5 us.

Step periods exceeding 39 us will extend access times.

HEAD LOCK MECHANISM: Automatic.

LOCATION OF STRAPS AND CONNECTORS: Figure 6-1.

J1: COMMAND CABLE. 34 PINS.
J2: DATA CABLE. 20 PINS.
J3: DC POWER INPUT.
J4: FRAME GROUND.

RP1: TERMINATOR MODULE. Figure 11-3.
If multiple drives are connected in daisy chain mode, only the last drive must be terminated.

J6: Drive address selection jumper. SHUNT BLOCK Figure 6-1.

pin 1 - pin 16 open
pin 2 - pin 15 open
pin 3 - pin 14 open
pin 4 - pin 13 open
pin 5 - pin 12 drive address 3 if shorted
pin 6 - pin 11 drive address 2 if shorted
pin 7 - pin 10 drive address 1 if shorted
pin 8 - pin 9 drive address 0 if shorted

Only one connection must be installed.

J12: PCB Option Pads. Figure 6-1.

No connections installed.

6.1 Physical Interface Overview

The electrical interface between the V100 and the host controller is via four connectors:

1. J1—Control signals (multiplexed)
2. J2—Read/write signals (radial)
3. J3—DC power input
4. J4—Frame ground

Refer to Figure 6-1 for connector locations.

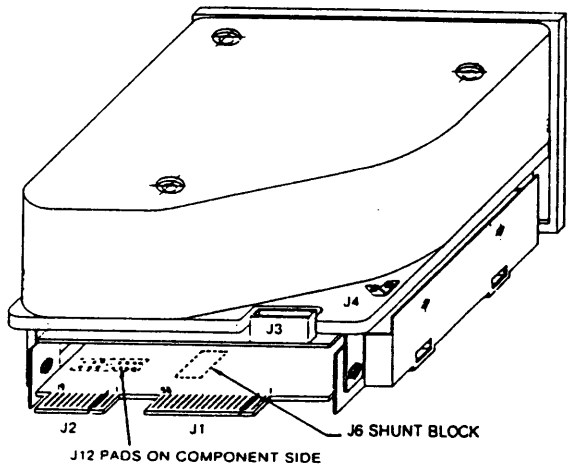


Figure 6-1
Interface Connector Physical Locations

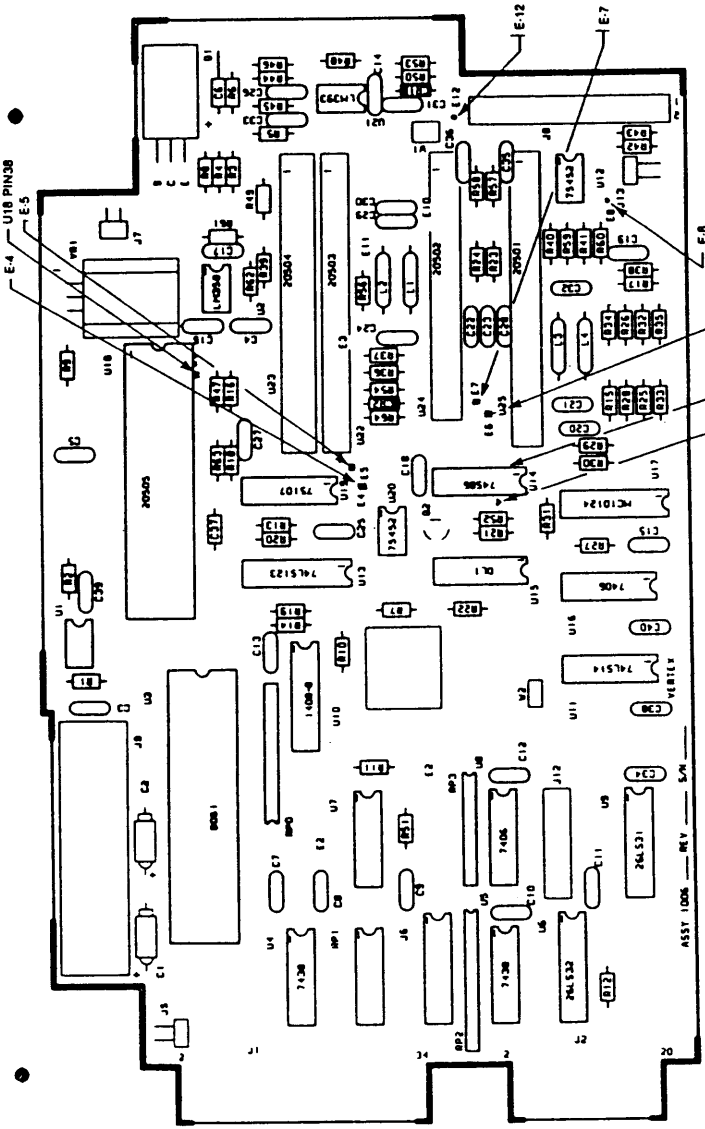


Figure 12-3
M.I.C.2.X Test Point Locations
Data PCB

SECTION 2.1

DDE Data Sheet for Power Supplies

DDE Data Sheet for Power Supplies. PS 12 REV. 0 DATE 880222

MANUFACTURER: Coutant NAME: dde020

TYPE: Switching modular

ENVIRONMENT:

Temperature range: 0 to 70 deg. C in free air.

Output power derating above 50 deg. C. 2.5% / deg. C

AC SPECIFICATIONS:

187-264 V or 99-132 V (strapable)

47-440 Hz

Inrush current: < 18 A peak

DC SPECIFICATIONS:

Modul	Volt	Tolerance	Adjustment	Max. current	Peak. current
	V	+/- %		A	A in 10 sec.
M	5	5	y	20.0	20.0
G	12	5	n	4.0	8.0
G	12	5	n	4.0	8.0
G	12	5	n	4.0	8.0
G	12	5	n	4.0	8.0

EFFICIENCY:

70 - 85 %

NOTES:

No minimum load on any module
Maximum output power is 300 W.

DDE Data Sheet for Power Supplies. PS 9 REV. 0 DATE 860609

MANUFACTURER: Coutant NAME: dde019

TYPE: Switching modular ML 150

ENVIRONMENT:

Temperature range: 0 to 70 deg. C in free air.

Output power derating above 50 deg. C. 2.5% / deg. C

AC SPECIFICATIONS:

187-264 V or 99-132 V (strapable)

47-440 Hz

Inrush current: < 18 A peak

DC SPECIFICATIONS:

Modul	Volt V	Tolerance +/- %	Adjustment	Max. current A	Peak. current A in 10 sec.
M	5	5	y	20.0	
L	-5.2	5	y	10.0	
C	12	5	n	3.0	
C	-12	5	n	3.0	

EFFICIENCY:

70 - 85 %

NOTES:

No minimum load on any module
Maximum output power is 150 W.

DDE Data Sheet for Power Supplies. PS 8 REV. 0 DATE 860117

MANUFACTURER: Coutant NAME: dde018

TYPE: Switching modular

ENVIRONMENT:

Temperature range: 0 to 70 deg. C in free air.

Output power derating above 50 deg. C. 2.5% / deg. C

AC SPECIFICATIONS:

187-264 V or 99-132 V (strapable)

47-440 Hz

Inrush current: < 18 A peak

DC SPECIFICATIONS:

Modul	Volt V	Tolerance +/- %	Adjustment	Max. current A	Peak. current A in 10 sec.
L	5	5	y	10.0	
L	-5.2	5	y	10.0	
S	24	5	n	5.0	16.0
S	24	5	n	5.0	16.0
G	-24	5	n	3.0	8.0
G	12	5	n	4.0	8.0
G	-12	5	n	3.0	8.0

EFFICIENCY:

70 - 85 %

NOTES:

No minimum load on any module
Maximum output power is 400 W.

DDE Data Sheet for Power Supplies. PS 7 REV. 0 DATE 851218

MANUFACTURER: Coutant NAME: dde017

TYPE: Switching modular

ENVIRONMENT:

Temperature range: 0 to 70 deg. C in free air.

Output power derating above 50 deg. C. 2.5% / deg. C

AC SPECIFICATIONS:

187-264 V or 99-132 V (strapable)

47-440 Hz

Inrush current: < 18 A peak

DC SPECIFICATIONS:

Modul	Volt	Tolerance	Adjustment	Max. current	Peak. current
	V	+/- %		A	A in 10 sec.
M	5	5	y	20.0	20.0
G	12	5	n	4.0	8.0
G	12	5	n	4.0	8.0
G	12	5	n	4.0	8.0
G	24	5	n	4.0	8.0

EFFICIENCY:

70 - 85 %

NOTES:

No minimum load on any module
Maximum output power is 300 W.

DDE Data Sheet for Power Supplies. PS 6 REV. 0 DATE 851218

MANUFACTURER: Coutant NAME: dde016

TYPE: Switching modular

ENVIRONMENT:

Temperature range: 0 to 70 deg. C in free air.

Output power derating above 50 deg. C. 2.5% / deg. C

AC SPECIFICATIONS:

187-264 V or 99-132 V (strapable)

47-440 Hz

Inrush current: < 18 A peak

DC SPECIFICATIONS:

Modul	Volt V	Tolerance +/- %	Adjustment	Max. current A	Peak. current A in 10 sec.
X	+ 5	5	y	40.0	-
M	+ 5	5	y	20.0	-
S	+12	5	n	8.0	16.0
BT	+24	2	n	1.0	-
BT	-12	2	n	0.5	-

EFFICIENCY:

70 - 85 %

NOTES:

No minimum load on any module.
X and M modules connected in parallel in order to get 60 A on +5V.
This connection must NOT be removed.
Maximum power is 400 W when fan is mounted.

DDE Data Sheet for Power Supplies. PS 5 REV. 0 DATE 851218

MANUFACTURER: Coutant NAME: dde014

TYPE: Switching modular

ENVIRONMENT:

Temperature range: 0 to 70 deg. C in free air.

Output power derating above 50 deg. C. 2.5% / deg. C

AC SPECIFICATIONS:

187-264 V or 99-132 V (strapable)

47-440 Hz

Inrush current: < 18 A peak

DC SPECIFICATIONS:

Modul	Volt V	Tolerance +/- %	Adjustment	Max. current A	Peak. current A in 10 sec.
X	+ 5	5	y	40.0	-
S	+12	5	n	8.0	16.0
BT	+24	2	n	1.0	-
BT	-12	2	n	0.5	-

EFFICIENCY:

70 - 85 %

NOTES:

No minimum load on any module
Maximum power is 330 W when fan is mounted.

DDE Data Sheet for Power Supplies. PS 4 REV. 0 DATE 851218

MANUFACTURER: Coutant NAME: dde013

TYPE: Switching modular

ENVIRONMENT:

Temperature range: 0 to 70 deg. C in free air.

Output power derating above 50 deg. C. 2.5% / deg. C

AC SPECIFICATIONS:

187-264 V or 99-132 V (strapable)

47-440 Hz

Inrush current: < 18 A peak

DC SPECIFICATIONS:

Modul	Volt V	Tolerance +/- %	Adjustment	Max. current A	Peak. current A in 10 sec.
X	+ 5	5	y	40.0	-
G	+12	5	n	4.0	8.0
G	+12	5	n	4.0	8.0
BT	+24	2	n	1.0	-
BT	-12	2	n	0.5	-

EFFICIENCY:

70 - 85 %

NOTES:

No minimum load on any module
Maximum power is 330 W when fan is mounted.

DDE Data Sheet for Power Supplies. PS 3 REV. 0 DATE 851218

MANUFACTURER: Coutant NAME: dde009

TYPE: Switching modular

ENVIRONMENT:

Temperature range: 0 to 70 deg. C in free air.

Output power derating above 50 deg. C. 2.5% / deg. C

AC SPECIFICATIONS:

187-264 V or 99-132 V (strapable)

47-440 Hz

Inrush current: < 18 A peak

DC SPECIFICATIONS:

Modul	Volt	Tolerance	Adjustment	Max. current	Peak. current
	V	+/- %		A	A in 10 sec.
M	5	5	y	20.0	-
G	12	5	n	4.0	8.0
G	12	5	n	4.0	8.0
S	24	5	n	8.0	16.0
C	5	5	n	3.0	-

EFFICIENCY:

70 - 85 %

NOTES:

No minimum load on any module
Maximum output power is 400 W when fan is mounted.

DDE Data Sheet for Power Supplies. PS 2 REV. 0 DATE 851218

MANUFACTURER: Coutant NAME: dde006

TYPE: Switching modular

ENVIRONMENT:

Temperature range: 0 to 70 deg. C in free air.

Output power derating above 50 deg. C. 2.5% / deg. C

AC SPECIFICATIONS:

187-264 V or 99-132 V (strapable)

47-440 Hz

Inrush current: < 18 A peak

DC SPECIFICATIONS:

Modul	Volt V	Tolerance +/- %	Adjustment	Max. current A	Peak. current A in 10 sec.
M	5	5	y	20.0	20.0
G	12	5	n	4.0	8.0
G	12	5	n	4.0	8.0
G	24	5	n	4.0	8.0

EFFICIENCY:

70 - 85 %

NOTES:

No minimum load on any module
Maximum output power is 300 W.

DDE Data Sheet for Power Supplies. PS 1 REV. 0 DATE 851218

MANUFACTURER: Coutant NAME: dde001

TYPE: Switching

ENVIRONMENT:

Temperature range: 0 to 70 deg. C in free air.

Output power derating above 50 deg. C. 1.0% / deg. C

AC SPECIFICATIONS:

166-264 V or 85-132 V (strapable)

47-63 Hz

Inrush current: < 30 A peak

DC SPECIFICATIONS:

Modul	Volt	Tolerance	Adjustment	Min. current	Max. current
	V	+/- %		A	A
-	5	0.5	y	10.0	100.0
-	12	0.5	y	0.0	13.0
-	12	0.5	y	0.0	5.0
-	24	0.5	y	0.0	7.0
-	5	0.5	y	0.0	2.5

EFFICIENCY:

> 65 %

NOTES:

All outputs protected

Max. output power 850W.

DDE Data Sheet for Power Supplies. PS10.

Revision 0 **Date 870601**

Name: No-Break System 1000VA

Manufacturer: SILCON A/S, Denmark.

Type: Uninterruptable Power Supply (UPS)

Mains input

Voltage	220 VAC ± 10%
Frequency	50 Hz ± 5%
Efficiency at rated load	typ. 82%
Power factor at nominal conditions	0.93
Input current	sinusoidal
Max. current with discharged battery	9 ARMS
External fuse	16 A

Output

Voltage, static	220 VAC ± 2%
Distortion, at linear load	<5%
Voltage, dynamic for 100% load change	± 5%
Recovery time	<20ms
Frequency locked to mains	
Output power at load P.F. 0.7 lag to 0.9 lead	1000 VA
Output current limited to	4.5 ARMS
Over current 50% for 30 sec. on mains operation	
Short circuit proof	
System shut down for:	
I_{peak} > 3 x max. IRMS for > 30 sec. I peak 13.5 A	
V_{batt} < 39 VDC	
V_{out} > 245 VAC	
High temperature	

Charger

Current limit	6 ADC
Charge voltage, adjustable	54-57 VDC

Battery operation

Battery voltage for rated output	40.8-57.6 VDC
Battery current at 48 VDC, full load	28 ADC
Battery current at 40.8 VDC, full load	33 ADC
Output frequency	50 Hz ± 0.5%
Efficiency at rated load	typ. 75%
Battery MCB (magnetic circuit breaker)	35 A
Inv. shut down for V_{batt} outside	39-60 VDC
Change to battery operation for:	
V_{mains} outside specification	
f_{mains} outside specification	
Overload	

General data

Ambient temperature	-10/+40 °C
RFI according to	VDE0875-N
Acoustic noise	appr. 50 dB(A)
Dimensions H x W x D	695x200x795 mm
Weight	appr. 75 kg

LED indicators

Mains operation	green
Battery operation	yellow
Overload	red
Output voltage	green

Alarm for battery operation and overload:
Acoustic alarm
Potential free contact

DDE Data Sheet for Power Supplies. PS 11.

Revision 0 **Date 870601**

Name: No-Break System 2000VA

Manufacturer: SILCON A/S, Denmark.

Type: Uninterruptable Power Supply (UPS)

Mains input

Voltage	220 VAC ± 10%
Frequency	50 Hz ± 5%
Efficiency at rated load	typ. 83%
Power factor at nominal conditions	0.93
Input current	sinusoidal
Max. current with discharged battery	18.5 ARMS
External fuse	20 A

Output

Voltage, static	220 VAC ± 2%
Distortion, at linear load	<5%
Voltage, dynamic for 100% load change	± 5%
Recovery time	<20ms
Frequency locked to mains	
Output power at load P.F. 0.7 lag to 0.9 lead	2 kVA
Output current limited to	9.1 ARMS
Over current 50% for 30 sec. on mains operation	
Short circuit proof	
System shut down for:	
I_{peak} > 3 x max. IRMS for > 30 sec. I peak 27 A	
V_{batt} < 39 VDC	
V_{out} > 245 VAC	
High temperature	

Charger

Current limit	12 ADC
Charge voltage, adjustable	54-57 VDC

Battery operation

Battery voltage for rated output	40.8-57.6 VDC
Battery current at 48 VDC, full load	56 ADC
Battery current at 40.8 VDC, full load	66 ADC
Output frequency	50 Hz ± 0.5%
Efficiency at rated load	typ. 76%
Battery MCB (magnetic circuit breaker)	75 A
Inv. shut down for V_{batt} outside	39-60 VDC
Change to battery operation for:	
V_{mains} outside specification	
f_{mains} outside specification	
Overload	

General data

Ambient temperature	-10/+40 °C
RFI according to	VDE0875-N
Acoustic noise	appr. 50 dB(A)
Dimensions H x W x D	695x200x795 mm
Weight	appr. 105 kg

LED indicators

Mains operation	green
Battery operation	yellow
Overload	red
Output voltage	green

Alarm for battery operation and overload:
Acoustic alarm
Potential free contact

SECTION 2.2

DDE Data Sheet for Streaming Tape Cartrigde Drive

DDE Data Sheet for Streaming Tape Cartridge Drive SD3 REV. 0

MANUFACTURER: ARCHIVE TYPE: 2060L and 2150L

GENERAL DRIVE DESCRIPTION:

The VIPER is a streaming 1/4" tape cartridge drive.The VIPER contains a embedded controller in a half-high package.
The VIPER 2060 stores 45 megabytes on 9 tracks, using a DC300 cartridge.
The VIPER 2150 stores 125 Mbyte on 15 tracks, or 150 Mbyte on 18 tracks, using a DC600 cartridge.

FORM FACTOR: 5.25"

ENVIRONMENT:

Electrical Interface: QIC-02

Power requirements:
+5 VDC +- 5 pct., 0.7 Amp
+12 VDC +-10 pct., 0.2 Amp motor not running.
0.8 Amp typ motor running max. 1.5 amp
2.5 Amp tape start surge(up to 300ms)

Power dissipation: 20.0 W typical
35.0 W max.

Operating temperature range: 5 to 45 deg. celsius.

Maximum temperature gradient: ----------

Operating humidity: 20 pct. - 80 pct. non-condensing.

DATA FORMAT AND MEDIA:

2060L:	QUALIFIED TAPE	FUNCTION	
	3M DC600A	read/write	QIC-24
	3M DC300XLP	read/write	QIC-24
2150L:	QUALIFIED TAPE	FUNCTION	
	3M DC600XTD	read/write	QIC-150
		read/write	QIC-120
		read	QIC-24
	3M DC600A	read/write	QIC-120
		read	QIC-24
	3M DC300XLP	read	QIC-24

PREVENTIVE MAINTENANCE:

The only preventive maintenance required for the VIPER is that the head and sensor holes must be kept clean.

The recording head should be cleaned after each initial pass with a new tape.
The recording head should be cleaned after every 8 hours of read/write activity.
The sensor openings and cartridge cavity should be cleaned whenever dirt or dust becom visible.

Information about cleaning procedure is available in the product manual.

CONNECTORS AND STRAPS:

1: QIC-02 connector.

2: Power connector.

Pin 1: +12 VDC.
Pin 2: +12 Return.
Pin 3: + 5 Return.
Pin 4: + 5 VDC.

Factory strapping: no straps installed

DOCUMENTATION:

Publications available from ARCHIVE:

Product manual QIC02 models 2060L and 2150L
Manual part number 21494-001.

DDE Data Sheet for Streaming Tape Cartridge Drive SD2 REV. 0

MANUFACTURER: TANDBERG TYPE: TDC 3319

GENERAL DRIVE DESCRIPTION:

The TDC 3319 is a streaming 1/4" tape cartridge drive comprising the TDC 3309 (basic drive) and the TDC 3350 MK-II (intelligent formatter). It records and reads serially on 9 tracks, and can store 45 Mbytes on a 450-foot cartridge.

FORM FACTOR: 5.25"

ENVIRONMENT:

Electrical Interface:

formatter to DIOC: QIC-02

drive to formatter: QIC-36

Power requirements:
+5 VDC +- 5 pct., 1.9 Amp
+12 VDC +-10 pct., 0.3 Amp motor not running.
1.0 Amp typ motor running max. 1.4 amp

Power dissipation: 12.5 W motor not running
21.5 W typical, motor running

Operating temperature range: 5 to 40 deg. celsius.

Maximum temperature gradient: 6 deg. celsius/hour

Operating humidity: 20 pct. - 80 pct. non-condensing.

DATA FORMAT:

The tape format conforms with the QIC-24 standard for data interchange.

The drive is able to read QIC-11 and QIC-24 tape formats, but it is unable to write other formats than the QIC-24.

MEDIA:

Type of media:

DC300XLP	(450-foot),	certified for 10.000 frpi.
DC600A	(600-foot),	certified for 10.000 frpi.
DC600XTD	(600-foot),	certified for 10.000 frpi.

It is recommmended to use tapes certified for 10.000 frpi.

PREVENTIVE MAINTENANCE:

It is required to clean the read/write head.

Recommemded equipment for head cleaning are:

a) The Tandberg Data 'TDC cleaning cartridge kit'.
b) Isopropyl-alcohol and cotton-tipped swabs, i.e. the 'CK-90' kit from 3M.

The cleaning interval depends on three main factors:

a) How much the drive is used.
b) The quality of the tape.
c) The quality of the enviroment

However, the following can be used as a recommended guideline:

Usage	Clean
8 hours a day	Daily
Daily	Weekly
Weekly	Monthly

Always clean the head immediately after using a new cartridge, and if a large number of rewrite- or reread operations are performed.

CONNECTORS AND STRAPS:

J1: Signal connector formatter board/basic drive.

J2: Power connector.

Pin 1: +12 VDC.
Pin 2: +12 Return.
Pin 3: + 5 Return.
Pin 4: + 5 VDC.

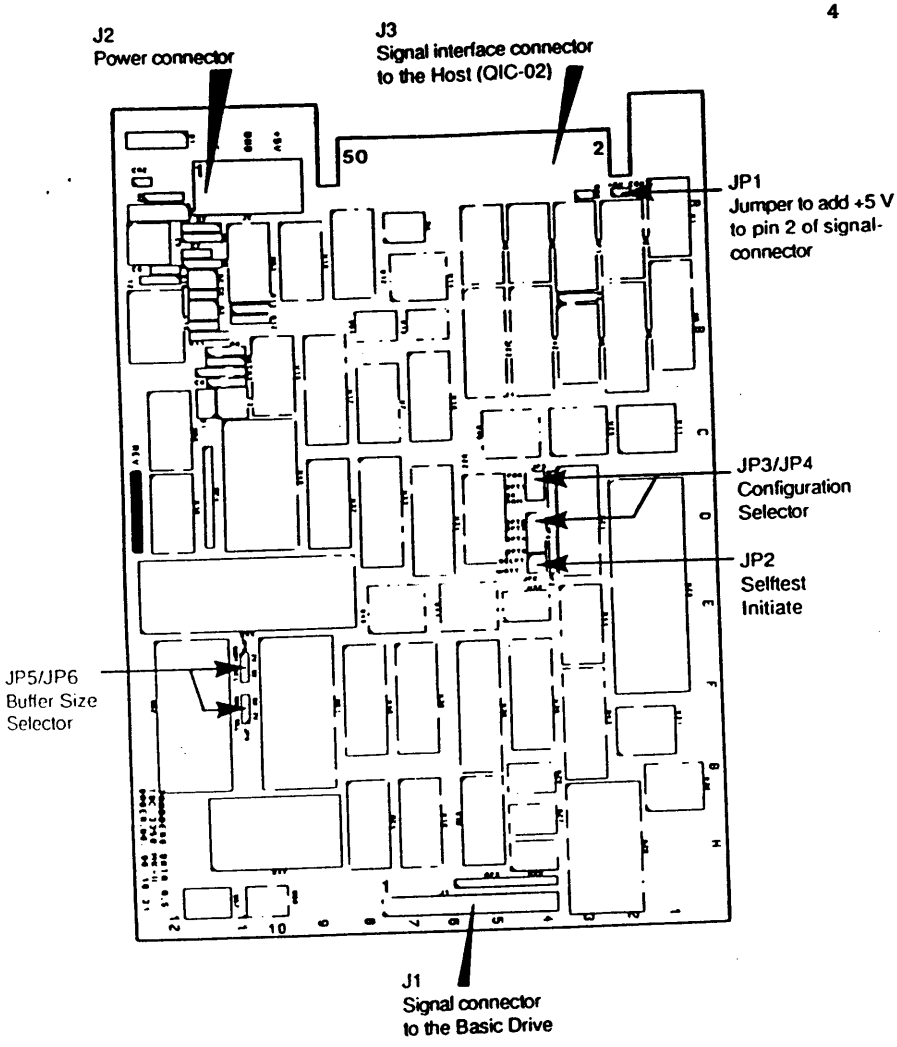
J3: QIC-02 connector to the host.

Factory strapping: no straps installed

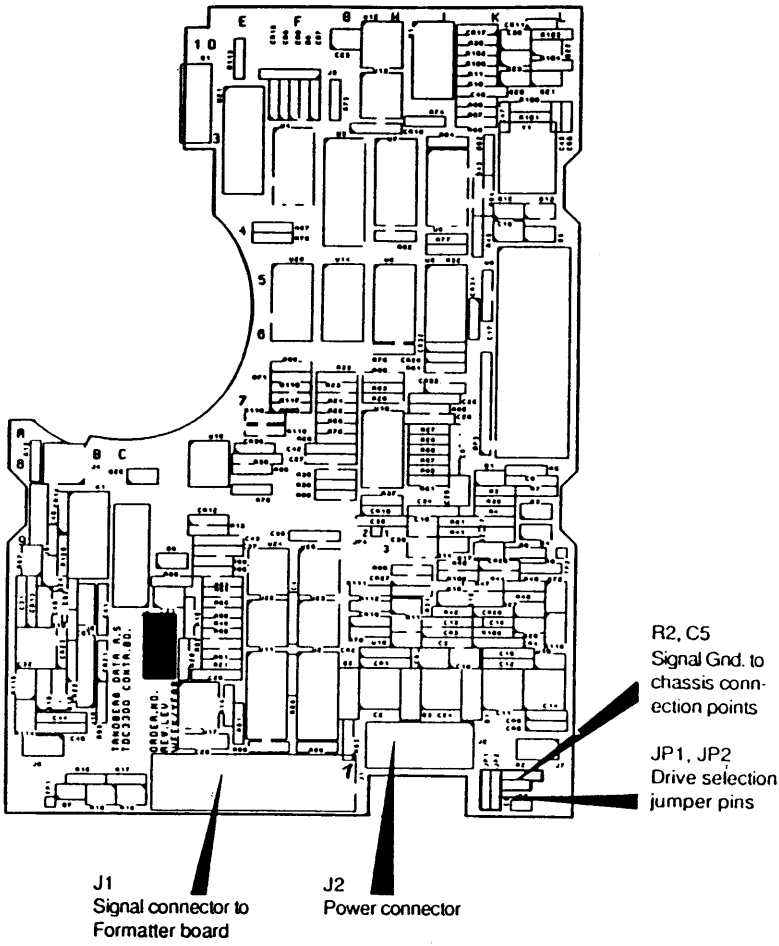
DOCUMENTATION:

Publications available from Tandberg Data:

TDC 3319 Reference Manual
TDC 3319 Maintenance Manual



Location of jumper positions and connectors on the TDC 3309 controller board.



Location of jumper positions and connectors on the TDC 3350 formatter board.

DDE Data Sheet for Streaming Tape Cartridge Drive SD1 REV. 0

MANUFACTURER: TANDBERG TYPE: TDC 3320

GENERAL DRIVE DESCRIPTION:

The TDC 3320 is a streaming 1/4" tape cartridge drive comprising the TDC 3315 (basic drive) and the TDC 3350 MK-II (intelligent formatter). It records and reads serially on 15 tracks, and can store 125 Mbytes on a 600-foot cartridge.

FORM FACTOR: 5.25"

ENVIRONMENT:

Electrical Interface:

formatter to DIOC: QIC-02

drive to formatter: QIC-36

Power requirements:
+5 VDC +- 5 pct., 1.8 Amp
+12 VDC +-10 pct., 0.3 Amp motor not running.
1.0 Amp typ motor running max. 1.4 amp

Power dissipation: 12.6 W motor not running
21.0 W typical, motor running

Operating temperature range: 5 to 40 deg. celsius.

Maximum temperature gradient: 6 deg. celsius/hour

Operating humidity: 20 pct. - 80 pct. non-condensing.

DATA FORMAT:

The tape format conforms with the QIC-120 standard for data interchange.

The drive is able to read QIC-11 and QIC-24 tape formats, but it is unable to write other formats than the QIC-120.

MEDIA:

Type of media:

DC600A (600-foot), certified for 10.000 frpi.
DC600XTD (600-foot), certified for 10.000 frpi.

From other manufacturers than 3M, it is recommended to use only DC600XTD.

PREVENTIVE MAINTENANCE:

It is required to clean the read/write head.

Recommemded equipment for head cleaning are:

a) The Tandberg Data 'TDC cleaning cartridge kit'.
b) Isopropyl-alcohol and cotton-tipped swabs, i.e. the 'CK-90' kit from 3M.

The cleaning interval depends on three main factors:

a) How much the drive is used.
b) The quality of the tape.
c) The quality of the enviroment

However, the following can be used as a recommended guideline:

Usage	Clean
8 hours a day	Daily
Daily	Weekly
Weekly	Monthly

Always clean the head immediately after using a new cartridge, and if a large number of rewrite- or reread operations are performed.

CONNECTORS AND STRAPS:

J1: Signal connector formatter board/basic drive.

J2: Power connector.

Pin 1: +12 VDC.
Pin 2: +12 Return.
Pin 3: + 5 Return.
Pin 4: + 5 VDC.

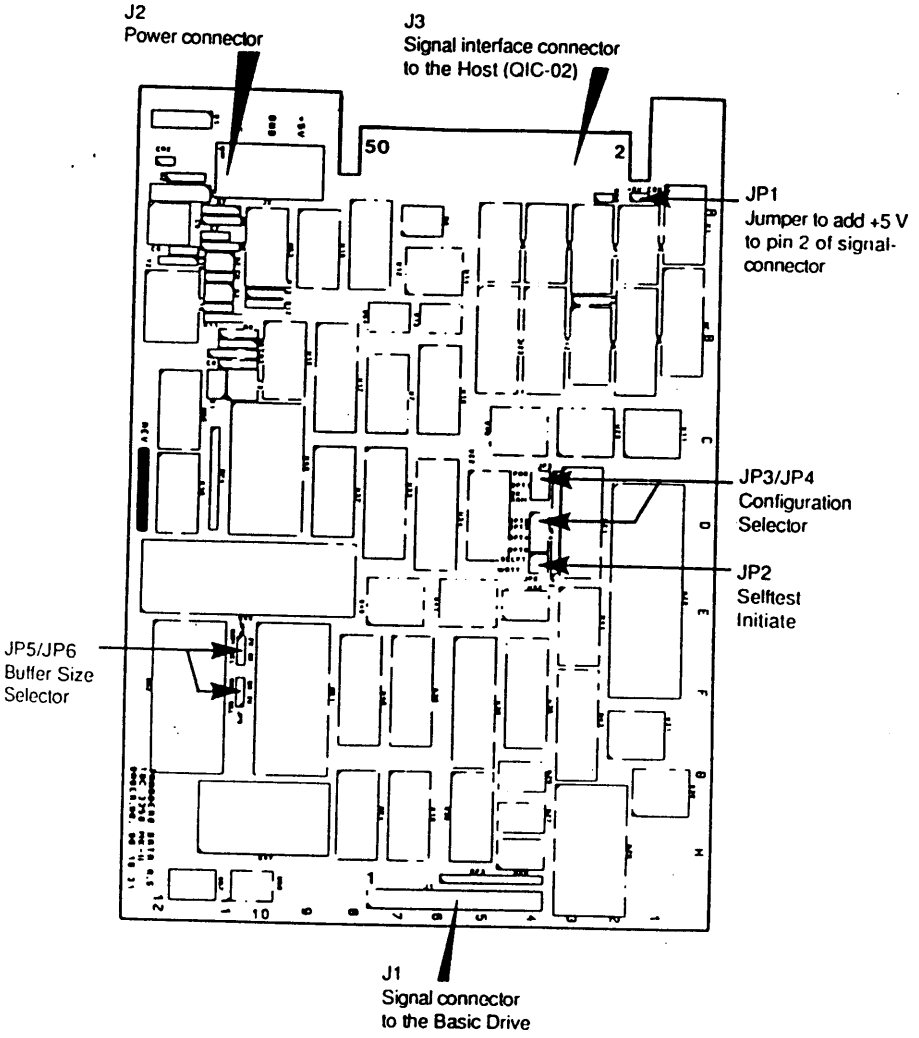
J3: QIC-02 connector to the host.

Factory strapping: no straps installed

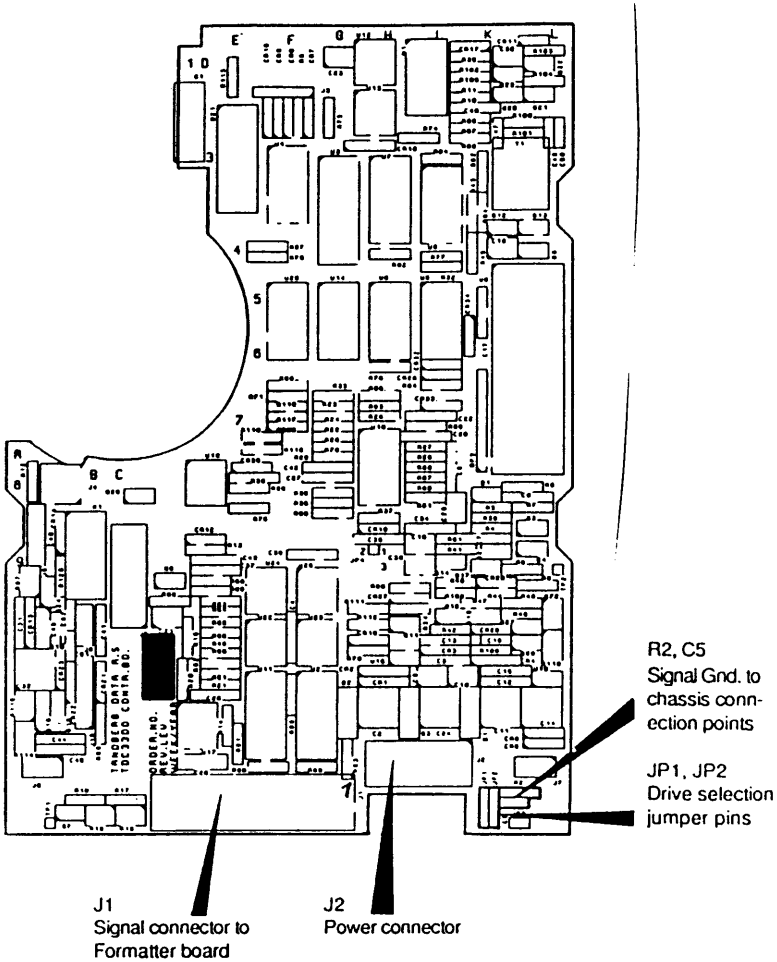
DOCUMENTATION:

Publications available from Tandberg Data:

TDC 3320 Reference Manual
TDC 3320 Maintenance Manual



Location of jumper positions and connectors
on the TDC 3315 controller board.



Location of jumper positions and connectors on the TDC 3350 formatter board.

DDE Data Sheet for Video Tape Cartridge Drive VD1 REV. 0

MANUFACTURER: EXERBYTE TYPE: 8200

GENERAL DRIVE DESCRIPTION:

The EXERBYTE EXB-8200 CTS is a high capacity 8 mm cartridge drive.The drive contains a embedded controller with SCSI interface. It uses helical scan technology, to record on a industry standard 8 mm cartridge.

FORM FACTOR: 5.25"

ENVIRONMENT:

Electrical Interface: SCSI

power requirements:
+5 VDC +- 4 pct., 4.0 Amp max.
+12 VDC +- 4 pct., 1.2 Amp max.

Power dissipation: 20.0 W typical

Operating temperature range: 5 to 40 deg. celsius.

Maximum temperature gradient: 1 c/minute max 10 c/hour

Operating humidity: 20 pct. - 80 pct. non-condensing.

DATA FORMAT AND MEDIA:

Standard 8mm tape cartridge.

Cartridge size	length(ft.)	max formatted capacity (Mbyte)
256	45	250
512	90	500
1024	180	1000
1536	270	1500
2048	360	2000

PREVENTIVE MAINTENANCE:

To be provided.

CONNECTORS AND STRAPS:

1: Power connector.

Pin 1: +12 VDC.
Pin 2: +12 Return.
Pin 3: + 5 Return.
Pin 4: + 5 VDC.

3: SCSI connector.

Straps: SCSI id; factory strapped: ON,ON,ON (id=7)

DOCUMENTATION:

Publications available from EXERBYTE:

Product specifikation EXB-8200 Cartridge Tape Subsystem.
Interface Users Manual.

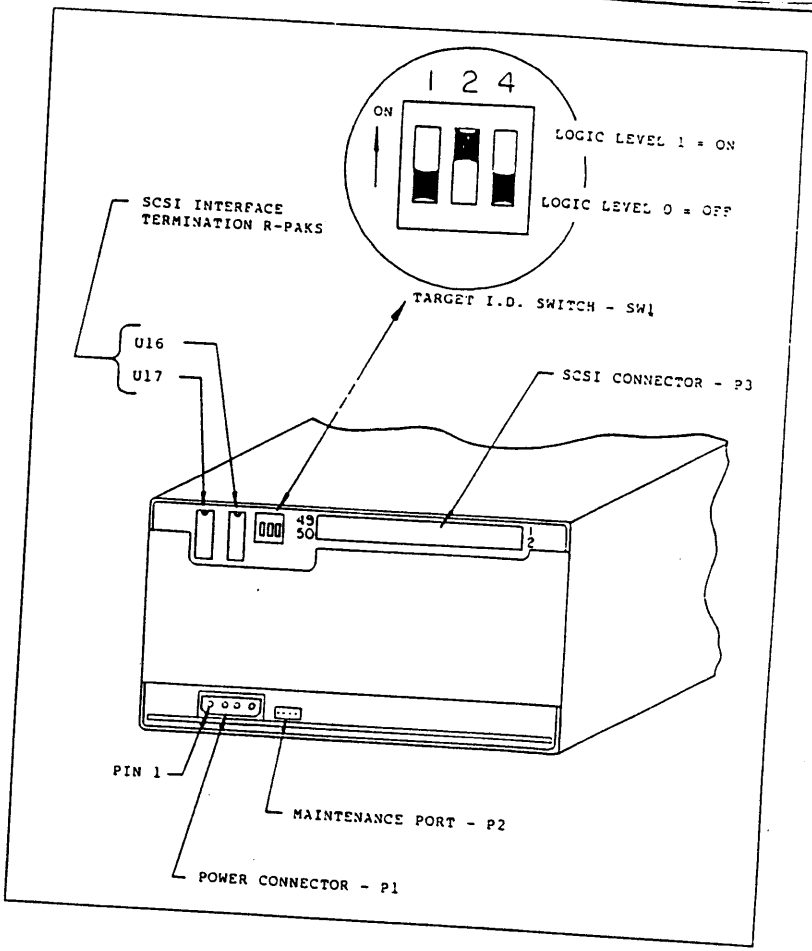


Figure 7-1. Rear Panel Connectors and Controls

Section I

DESCRIPTION

GENERAL DESCRIPTION

This manual describes the Small Computer System Interface (SCSI) installed on the Microstreamer•, CacheTape•, and the GCR CacheTape•. The Cipher SCSI-to-Tape Drive Controller (CSC) incorporates all the components and circuitry on a multi-layered printed wiring board. The two CSC models which are usable on the tape drives specified are:

- o CSC 100 -- Single-Ended Drivers and Receivers
- o CSC 200 -- Differential Drivers and Receivers

The CSC dimensions are:

- o Height - 6.80 inches
- o Width - 16.50 inches
- o Depth - 2.67 inches with non-shielded connector;
  3.0 inches with shielded connector
- o Weight - 7.5 lbs.

The major modules of the CSC are:

- o SCSI Protocol Controller Chip
- o Memory Array Controller
- o 64K Byte Buffer Memory
- o 8085 Microprocessor
- o 2K X 8-Bit Scratch Pad RAM
- o 24K X 8-Bit EPROM
- o 5V Power Supply

The SCSI bus capabilities are:

- o Transfer Rate: 1.5 Mbytes/sec. maximum - asynchronous
- o Organization: 8-Bit Parallel with Parity

Power for the controller is supplied from the tape drive to a switching voltage regulator on the SCSI PWB. The CSC requires no preventive maintenance.

PHYSICAL DESCRIPTION

The CSC assembly (Figure 1-1) is designed to be field-installable (by a technician) onto the rear of the tape drive housing. The SCSI controller is integrated onto a 6.3" X 16" multi-layered printed wiring board. When the CSC enclosure is securely anchored, it hinges open to allow access to the controller PWB and to facilitate interconnecting the CSC to the tape drive interface connectors and the input power connector. There is no operator access to the CSC assembly once installed on the tape drive. Access is restricted to trained maintenance personnel for repair and replacement purposes only.

FUNCTIONAL DESCRIPTION

The CSC provides the required control functions and interface signals to accommodate the operation of Microstreamer, CacheTape and GCR CacheTape on ANSI standard SCSI bus. The two interfaces which the controller provides are the standard Cipher interface and SCSI. The controller will perform standard SCSI tape functions including the COPY command. Its circuitry includes all logic required to operate as a target device when executing the standard tape functions, and as an initiator device when executing the COPY command to another device on the SCSI bus. The microprocessor and associated memory are used to control communication over the SCSI bus, manage the controller buffer memory, queue tape functions, and control the tape interface protocol.

Figure 1-2 is a system block diagram. Data transfer to tape is accomplished by data coming in from the SCSI interface and being temporarily stored in the buffer memory. From the buffer memory data is sent to the tape interface. Reading from the tape occurs by data coming in from the tape interface and being held in the buffer memory. From there, bytes are transferred out to the SCSI interface.

REFERENCE MANUALS

This addendum is designed to be used in conjunction with the technical manuals for Cipher's 1/2" reel-to-reel tape drives:

TAPE DRIVE	MANUAL P/N
F880 Microstreamer	799816-003
M890/M891 CacheTape	799816-006
M990 GCR CacheTape	799891-001

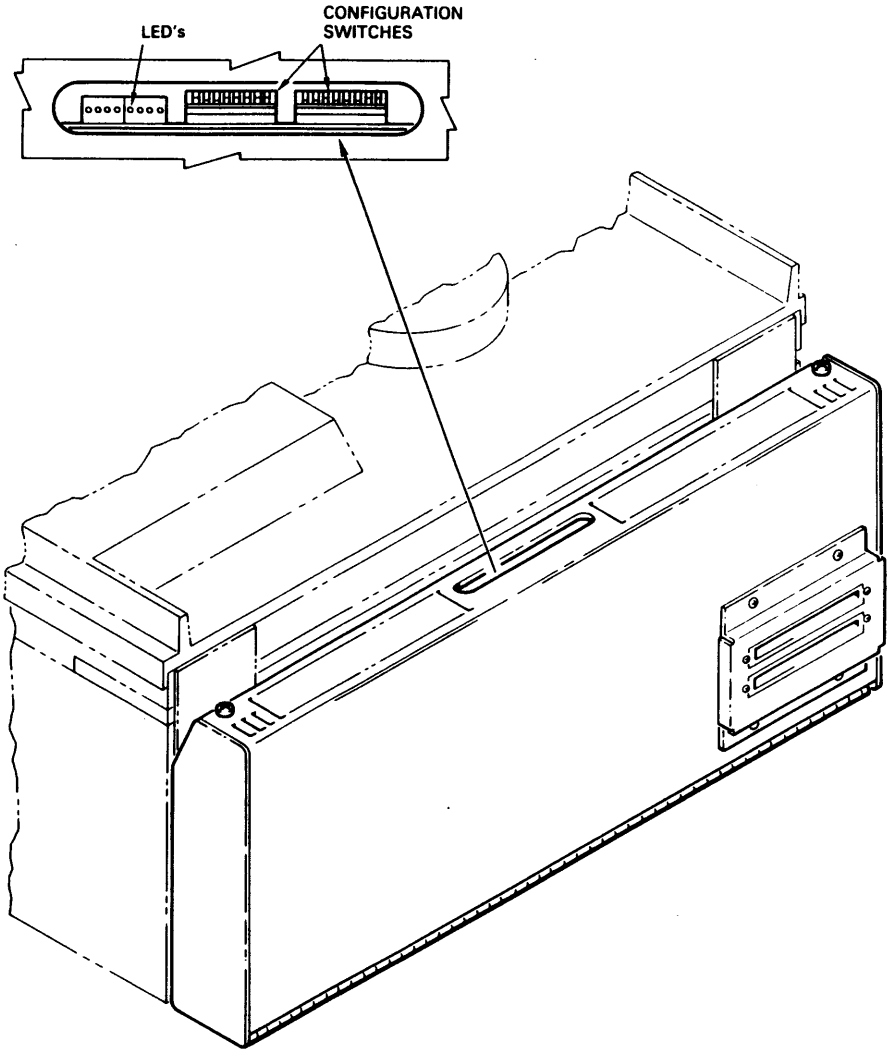


Figure 1-1. SCSI Controller Assembly

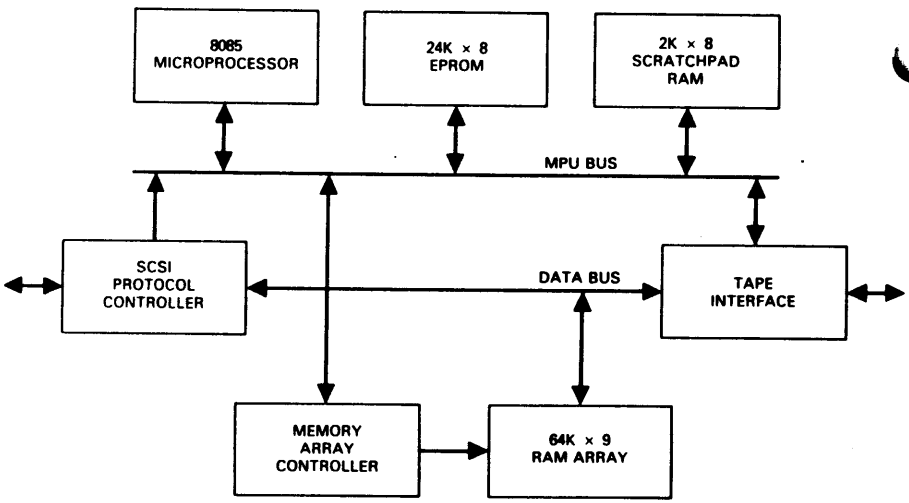


Figure 1-2. System Block Diagram

SECTION II

INSTALLATION, RETROFIT INSTALLATION, SWITCH SETTINGS, AND INTERFACE CONNECTIONS

Notice: If installation is for a retrofit kit, disregard this procedure and refer to retrofit installation instructions, page 2-6.

INSTALLATION

The CSC assembly should be installed by a qualified technician. It is designed to attach on tape drives that are rack-mounted or mounted inside a Cipher enclosure. The CSC enclosure opens to allow access to the controller PWB and to facilitate connecting the CSC to the tape drive interface and the input power. If it is to be installed on a rack-mounted tape drive, the CSC assembly must be attached to the tape drive before installation in the equipment rack. On an enclosed tape drive, the tape drive must be removed from the enclosure before installation can be attempted. The installation of the CSC assembly requires a pair of diagonal pliers, cutters and a phillips screw driver. Refer to Figure 2-1.

To install, proceed as follows:

1. Open the top cover of the tape drive and loosen the two screws on either side of the top plate behind the front panel.

2. Open the top plate by lifting the sides directly behind the front panel. Place the safety pin in the hole provided in the top plate support arm. See Figure 2-1, sheet 1.

3. Disconnect the main harness from the PWB.

4. Locate the small male connector tie-wrapped to the main harness; this is the SCSI power and ground harness. Cut and remove the three tie wraps that secure it to the main harness. See Figure 2-1, sheet 1.

5. Route the SCSI harness to the back of the tape drive. Loosely attach an adhesive backed tie wrap anchor to the SCSI harness. Attach the anchor to the back wall of the chassis as shown in Figure 2-1, sheet 1.

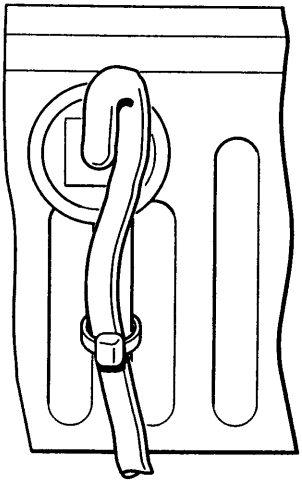
6. Route the male end of the SCSI harness through the large opening in the back of the chassis. Connect the male connector to the female connector of the SCSI power cable. See Figure 2-1, sheet 2.

7. Reconnect the main harness assembly to the PWB.

8. Assemble the mounting screw, bracket, and well nut to the CSC chassis. Install the well nut through the bracket hole on the front side of th CSC from the inside out. Slide the bracket into the front slot, lip down, facing away from the CSC chassis for Microstreamer and CacheTape drives (facing toward the CSC chassis for GCR's), between the well nut and inner hole. Insert the screw through the bracket and into the well nut.

9. Route the power cable through the chassis slot (bottom) of the CSC housing.

10. Hook the CSC assembly onto the back of the tape drive. Route the power cord down the back of the drive. Provide a service loop in the cord and secure the cord with a tie-wrap as shown below.



11. Tighten the well nut, while applying pressure on the bracket, until the CSC assembly is securely fastened to the tape driave chassis.

12. Plug the power cable into J4 on the CSC board. Secure it to the CSC housing with the provided tie wrap anchor.

13. Plug the interface cables to the PWB assembly and to the CSC assembly board. J1 and J2 plug into P1 and P2, respectively. Loop the cable.

14. Close the CSC enclosure and refer to Figure 2-1, sheet 3. Fasten one end of each ground strap to each screw on top of the CSC housing. Tighten the screws.

15. Fasten the other end of each ground strap onto the back of the top plate using one hinge screw on each end of the top plate.

16. Check that the drive passes the power-up tests.

17. Install the drive in rack or enclosure. Remove the window on an enclosure - for I/O cable access - before reinstalling the tape drive unit.

SERVICE ACCESS

Service access to the CSC PWB on a rack-mounted tape drive can be done without removing the drive from the slides. The tape drive must be removed from an enclosure for service.

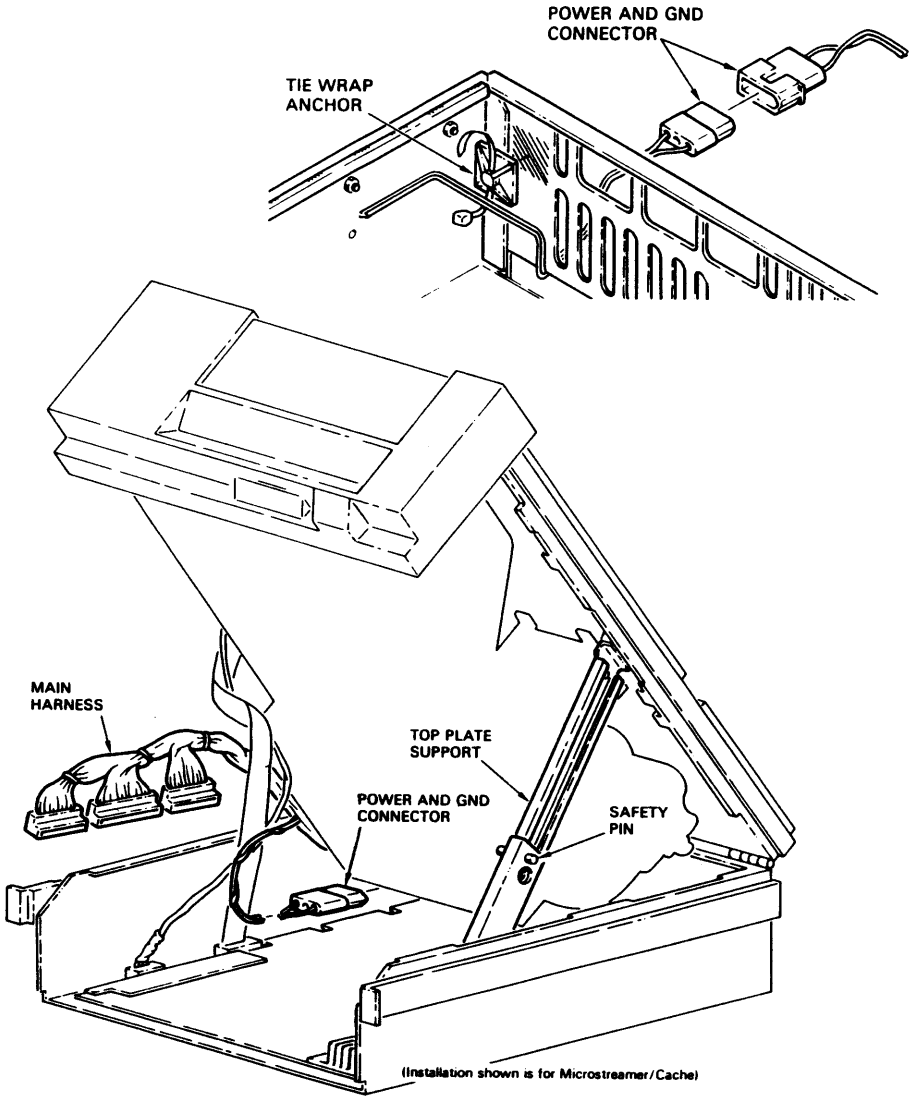


Figure 2-1. CSC Assembly Installation

Sheet 1 of 3

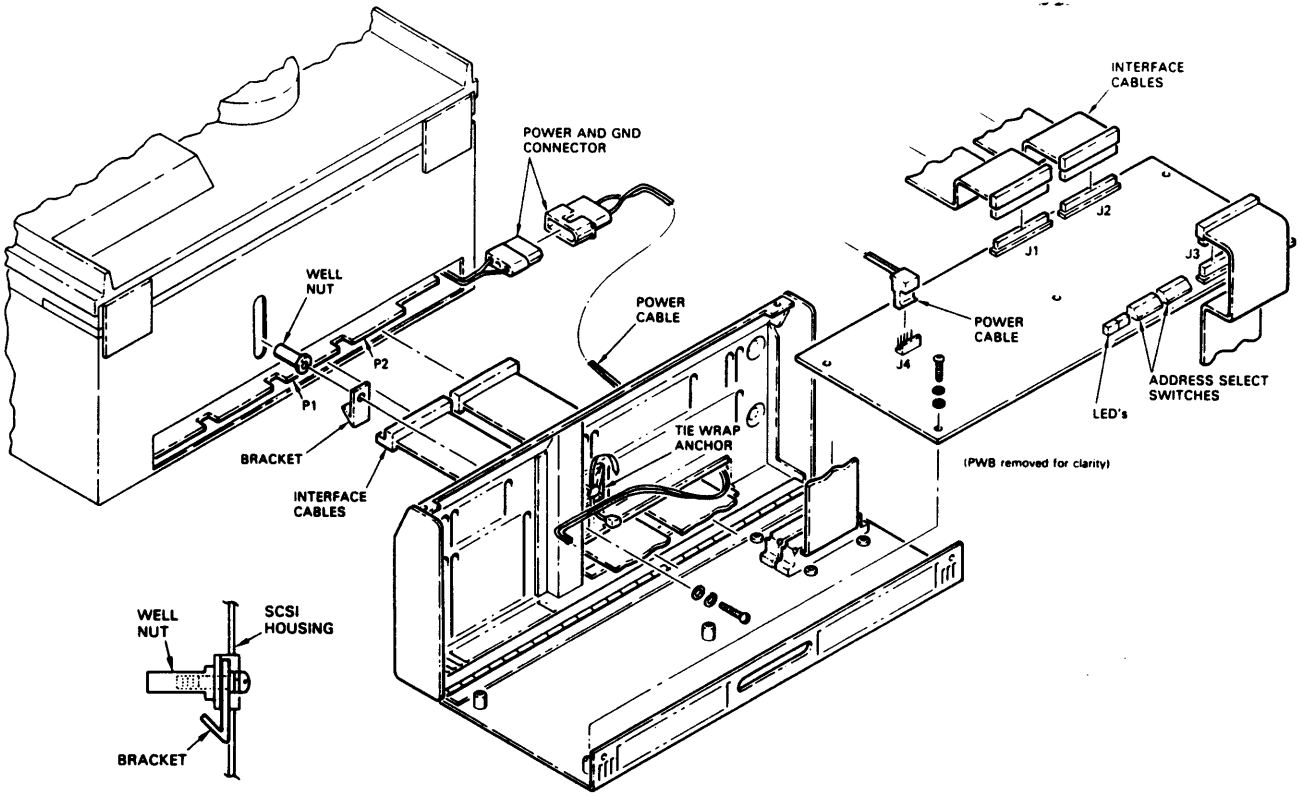


Figure 2-1. CSC Assembly Installation

Sheet 2 of 3

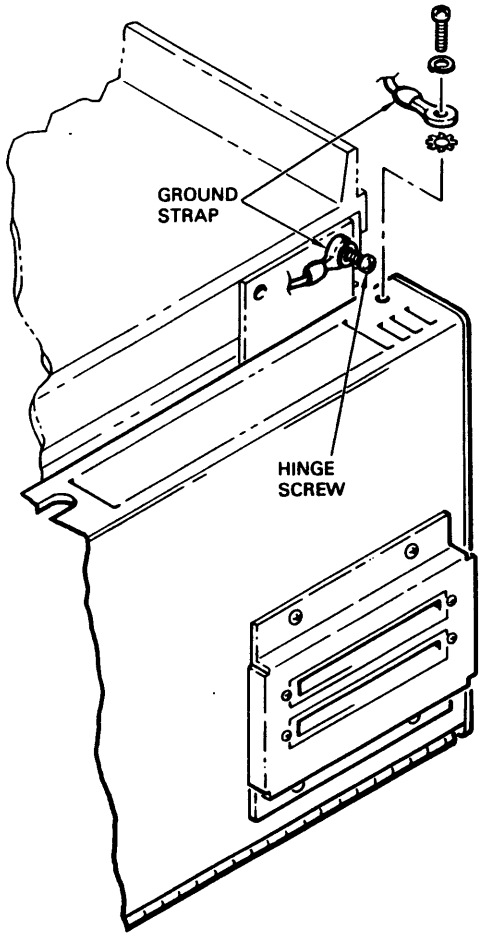


Figure 2-1. CSC Assembly Insatllation

Sheet 3 of 3

INSTALLATION

The CSC assembly should be installed by a qualified technician. It is designed to attach on tape drives that are rack-mounted or mounted inside a Cipher enclosure. The CSC enclosure opens to allow access to the controller PWB and to facilitate connecting the CSC to the tape drive interface and the input power. If it is to be installed on a rack-mounted tape drive, the drive must be fully extended and removed from the rack slides prior to installation. On an enclosed tape drive, the tape drive must be removed from the enclosure before installation can be attempted. The installation of the CSC assembly requires a pair of diagonal pliers, pliers, and a phillips screw driver. Refer to Figure 2-1A.

To install, proceed as follows:

1. Turn power off and remove tape drive power cord from outlet.
2. Place the top cover in the Maintenance Access position. Open top plate by lifting sides directly behind front panel. Place safety pin in hole provided in top plate support arm. See Figure 2-1A, sheet 1.
3. Disconnect cable harness from the PWB.
4. Install line tap connectors to main harness assembly by crimping onto wire as follows (connect to the top board, Sense/Servo board, on the GCR):

MAIN HARNESS	POWER CONNECTIONS
(GCR)	
P1-3	White wire--P2
P1-1	Black wire--P3
Microstreamer/Cache)	
P3-10	White wire--P2
P3-9	Black wire--P3

5. Plug the black and white wires of the SCSI Harness adapter cable into the taps according to step 4.
6. Route the male end of the SCSI Harness through the back of the chassis.
7. Connect the female plug of the SCSI Harness to the male plug.
8. Reconnect main harness assembly to PWB.
9. Power up the tape drive

CAUTION -

CSC 100 only: Connect a voltmeter between pins 1 (gnd) and 5 (voltage) of J4. The value of the input should be +35±6 Vdc for Microstreamer and CacheTape, and +57±6 or +37±5 Vdc for GCR. Turn drive power off before continuing and remove power cord. **Warning** - If voltages don't check correctly, do not reconnect harness. Go back to step 4 and repeat steps 4-9 after turning power off.

10. Close top plate and place power cord on top.

11. Route the power cable through the CSC housing bottom slot and anchor with tie wrap as shown in Figure 2-1A.

12. Hook CSC assembly onto the back of the tape drive housing and tighten the well nut.

13. Plug power cable to J4 on the CSC board.

14. Plug interface cables to PWB assembly and to CSC assembly board. J1 and J2 plug into P1 and P2, respectively. Loop the cable.

15. Close CSC enclosure and refer to Figure 2-1A, sheet 3. Fasten one end of each ground strap to both screws located on top of enclosure and tighten the screws.

16. Fasten the other end of each ground strap onto the back of the top plate by loosening one hinge screw located on each end of the top plate. Retighten the screws

17. Turn drive on and check that drive powers up correctly.

18. Power drive off and reinstall in rack or enclosure. Remove the window on an enclosed Microstreamer for I/O cable access, before reinstalling the tape drive unit.

SERVICE ACCESS

Service access to the CSC PWB on a rack-mounted tape drive can be done without removing the drive from the slides. The tape drive must be removed from an enclosure for service.

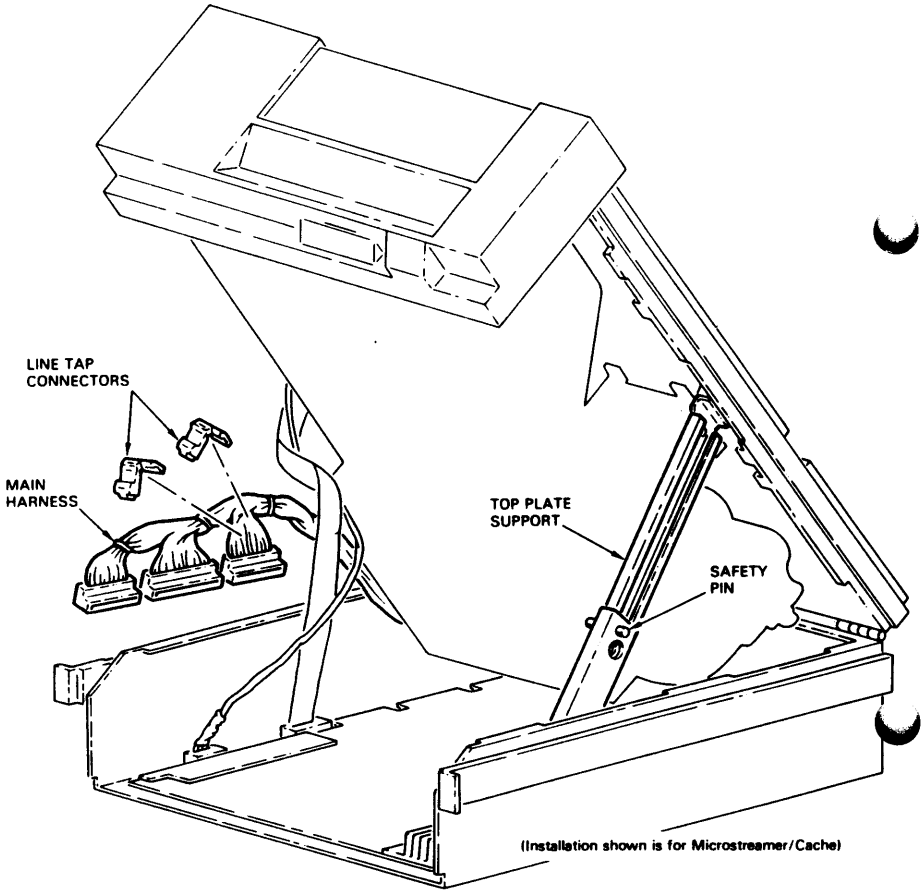


Figure 2-1a. CSC Retrofit Assembly Installation
Sheet 1 of 4

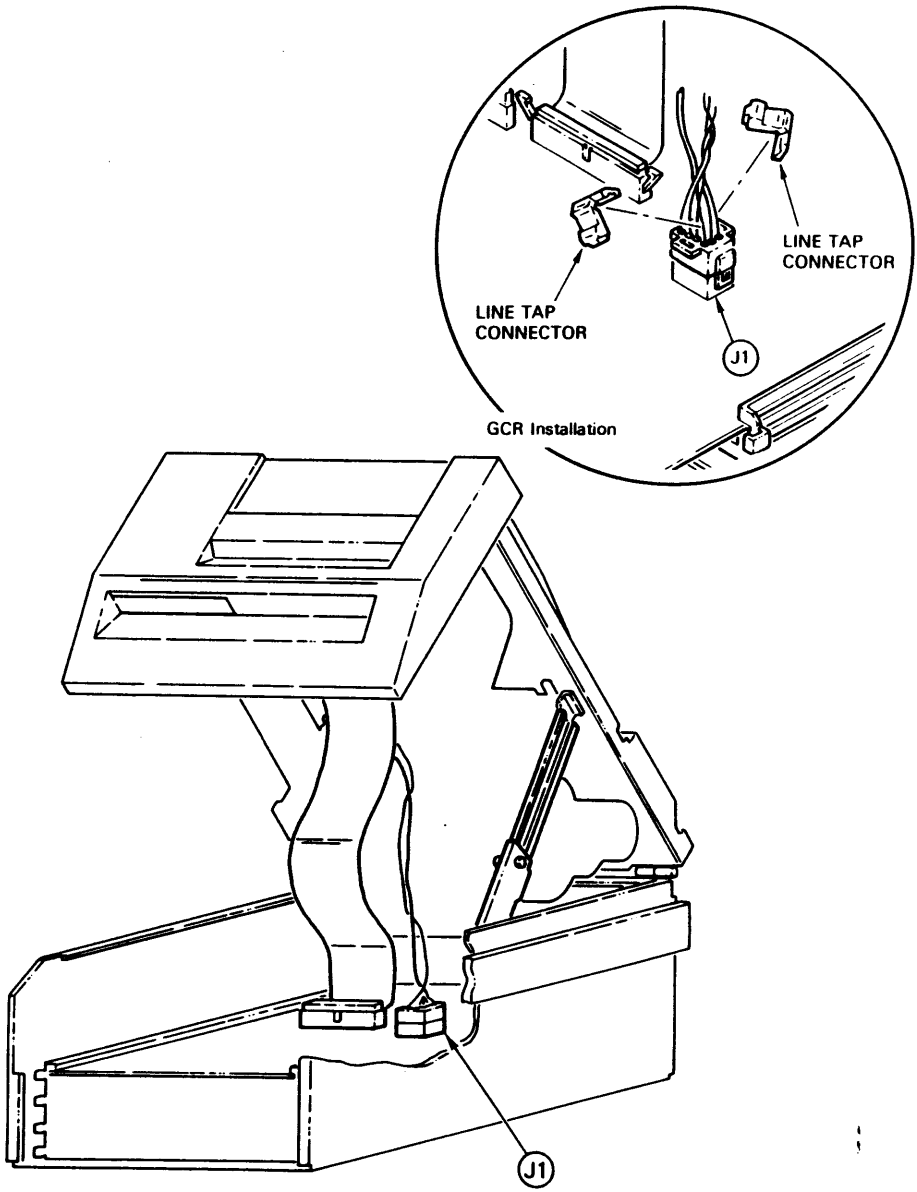


Figure 2-1a. CSC Retrofit Assembly Installation, Sheet 2 of 4

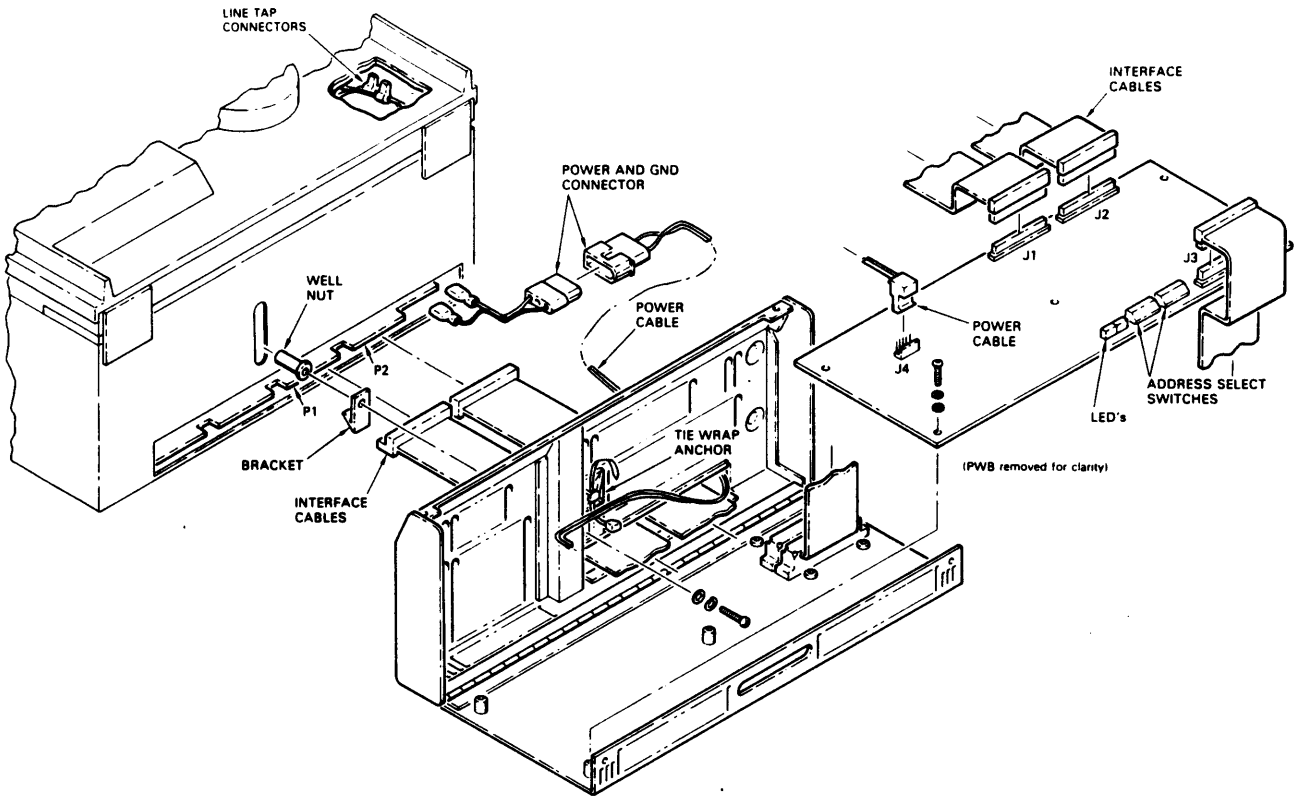


Figure 2-1a. CSC Retrofit Assembly Installation

Sheet 3 of 4

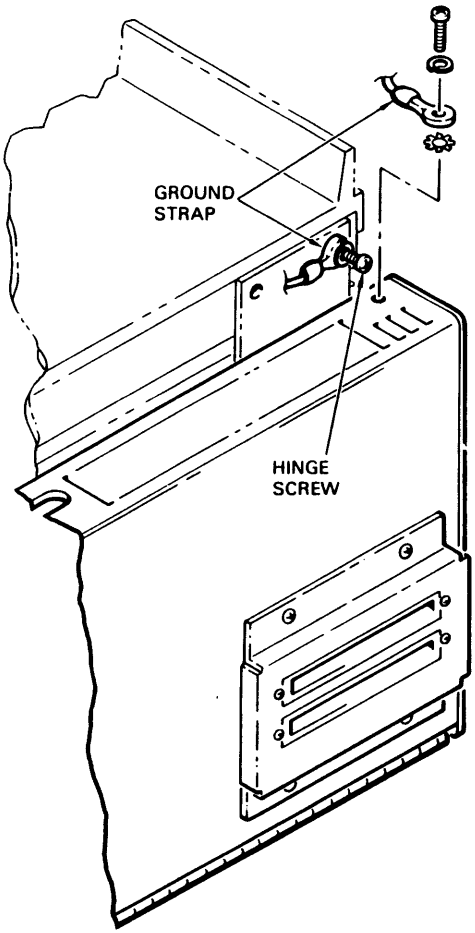


Figure 2-1a. CSC Retrofit Assembly Installation
Sheet 4 of 4

SCSI ID SWITCHES

A DIP switch is used to select the SCSI ID as shown on Table 2-1. Note: Refer to the silkscreen on the board for these switches.

	2	1	0	SCSI ID
	Open	Open	Open	0
	Open	Open	Closed	1
	Open	Closed	Open	2
*	Open	Closed	Closed	3
	Closed	Open	Open	4
	Closed	Open	Closed	5
	Closed	Closed	Open	6
	Closed	Closed	Closed	7

Table 2-1. SCSI ID

Silkscreen position S, between 0 and C of switch position 4 is the hardware reset switch; its normal operating position is open. Toggle this to reset the board. Switches 5 through 7 are not used and should be closed.

CONFIGURATION SWITCHES

The switches, labeled 0 through 7, and their functions are listed in Table 2-2.

SWITCH		POSITION		FUNCTION
SW1		0	1	
	*	Closed	Closed	1 Unit available on controller
		Open	Closed	2 Units available on controller
		Closed	Open	3 Units available on controller
		Open	Open	4 Units available on controller
		2	3	
	*	Closed	Closed	Normal
		Open	Closed	Loop on power-up routines
		Closed	Open	Loop on RAM data dump
		Open	Open	Allow execution after power-up failure
		4	5	
		Closed	Closed	880
		Open	Closed	890/891
		Closed	Open	990 (up to 32K data blocks; data recoverable after fatal drive error)
		Open	Open	990 (up to 64K data blocks; data not recoverable after fatal drive error)
6				
	*	Closed		Parity checked
		Open		Non-parity checked
7				
	*	Closed		Arbitrating Model
		Open		Non-arbitrating Model

Table 2-2. Configuration Switches

* Factory settings

CSC 100 ONLY

There are a number of jumpers on the CSC 100 PWB. Only jumper W7 can be altered. An installed jumper causes the controller to issue a hard reset of the SCSI bus at power-up. A hard reset is not issued if the jumber is removed.

CSC 200 ONLY

The CSC 200 has two DIP switches not found on the CSC 100, at locations 5A and 6T. All switches at 5A should be closed. They are for test purposes only. All switches at 6T except 4 and 5 should be closed. The following table provides the function of switches 4 and 5.

POSITION		FUNCTION
4	5	
Closed	Open	*Hard reset of SCSI bus issued at power-up.
Open	Closed	No hard reset of SCSI bus issued at power-up.

* Factory Setting

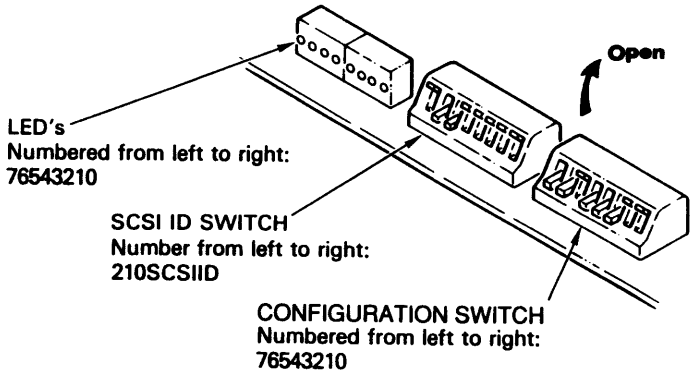


Figure 2-2. Controller Board Switches

INTERFACE CONNECTIONS

SCSI controllers are daisy-chained together using a common cable. A minimum conductor size of 28 AWG is used to minimize noise effects and ensure proper distribution of terminator power. For both models, a 50-conductor flat cable or 25 twisted-pair cable is used. Shielded or non-shielded cable connectors are available.

The CSC 100 can use terminator power supplied by the SCSI bus in the event the drive and interface are at the end of the bus and not turned on.

Figure 2-3 shows the termination scheme for CSC 100 and CSC 200. For CSC 100, the ribbon cable connecting the peripherals in a daisy-chained manner is limited to 6.0 meters. All SCSI signals in the cable are terminated at each end by 220/330 Ohm termination resistors. The CSC 200 is recommended for SCSI connections exceeding 6.0 meters and ranging up to 15.0 meters, primarily for interconnection outside of a cabinet. All SCSI bus signals consist of two lines denoted (+)signal and (-)signal. Each differential pair must be terminated at each end of the SCSI bus with 330 Ohms to +5V, 330 Ohms to ground, and 150 Ohms between the signal pairs. Terminations are made by inserting terminators into the sockets: on the CSC 100 PWB at locations 2A and 2B and on the CSC 200 at locations 2A, 2H, and 3G. Only two devices at each physical end of the bus require terminators; if the controller is not at either physical end of the bus, remove the terminators.

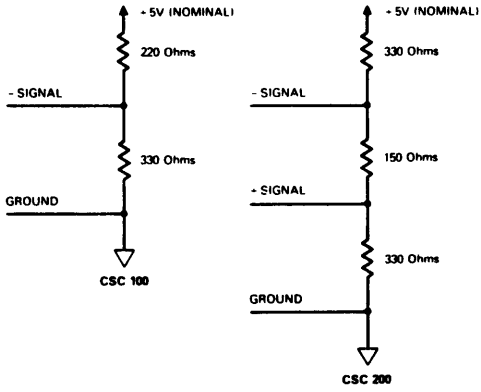


Figure 2-3. SCSI Bus Signal Termination

SCSI Bus Terminator Power. The controller supplies terminator power through a diode to its socketed SCSI bus terminators. This power is also supplied to SCSI bus connection J3 pin 26 for powering a terminator on the opposite end of the bus. This provides for signal integrity if that device loses internal power. Additionally, external terminator power into the controller can be provided through a diode in SCSI bus connector J3 pin 26.

Connectors. Two 50-pin connectors, J1 and J2, are provided to connect the controller to the tape drive. Also mounted on this board is a 50-pin connector, J3, which is provided to connect the CSC 100 to the SCSI bus in a daisy-chain configuration. For the model CSC 200, two 50-pin connectors, J3 and J4, are provided for daisy-chaining.

Pin Assignments. The signals, mnemonics and pin assignments for connectors J1 and J2 are presented in Table 2-3. See Section III for command definitions. Table 2-4 shows the single-ended pin assignments for ANSI unshielded and Alternative 1 shielded connectors. Table 2-5 shows the single-ended pin assignments for ANSI Alternative 2 shielded connectors. Table 2-6 shows the differential pin assignments for ANSI unshielded and Alternative 1 shielded connectors, Table 2-7 for Alternative 2 shielded connectors.

Connector	Signal Pin	Signal
J1 Controller to Tape Drive	2	Formatter Busy (IFBY)
	4	Last Word (ILWD)
	6	Write Data 4 (IW4)
	8	Initiate Command (IGO)
	10	Write Data O (IWO)
	12	Write Data 1 (IW1)
	14	---
	16	---
	18	Reverse (IREV)
	20	Rewind (IREW)
	22	Write Data Parity (IWP)
	24	Write Data 7 (IW7)
	26	Write Data 3 (IW3)
	28	Write Data 6 (IW6)
	30	Write Data 2 (IW2)
	32	Write Data 5 (IW5)
	34	Write (IWRT)
	36	---
	38	Edit (IEDIT)
	40	Erase (IERASE)
	42	Write File Mark (IWFM)
	44	---
	46	Transport Address 0 (ITAD0)
	48	Read Data 2 (IRD2)
	50	Read Data 3 (IRD3)
J2 Controller to Tape Drive	1	Read Data Parity (IRDP)
	2	Read Data 0 (IRD0)
	3	Read Data 1 (IRD1)
	4	Load Point (ILDP)
	6	Read Data 4 (IRD4)
	8	Read Data 7 (IRD7)
	10	Read Data 6 (IRD6)
	12	Hard Error (IHER)
	14	File Mark (IFMK)
	16	Identification (IIDENT)
	18	Formatter Enable (IFEN)
	20	Read Data 5 (IRD5)
	22	End of Tape (IEOT)
	24	Rewind/Unload (IRWU)
	26	---
	28	Ready (IRDY)

Table 2-3. Interface Connections, Controller to Tape Drive

Connector	Signal Pin	Signal
J2 Controller to Tape Drive	30	Rewinding (IRWD)
	32	File Protected (IFPT)
	34	Read Strobe (IRSTR)
	36	Write Strobe (IWSTR)
	38	Data Busy (IDBY)
	40	High Speed Status (ISPEED)
	42	Corrected Error (ICER)
	44	On Line (IONL)
	46	Transport Address (ITAD1)
	48	Formatter Address (IFAD)
	50	Select Speed (IHISP)

NOTE: All other pins on J1 and J2 are grounded.

Table 2-3. Interface Connections, Controller to Tape Drive (Cont'd.)

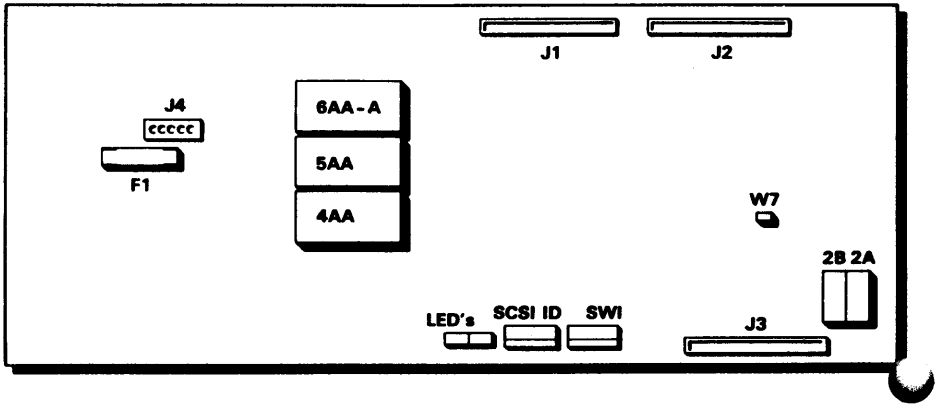


Figure 2-4. CSC PWB Component Locations

Signal Pin	Signal
2	-DB0
4	-DB1
6	-DB2
8	-DB3
10	-DB4
12	-DB5
14	-DB6
16	-DB7
18	-DBP
20	Ground
22	Ground
24	Ground
26	Terminator Power
28	Ground
30	Ground
32	-ATN
34	Ground
36	-BSY
38	-ACK
40	-RST
42	-MSG
44	-SEL
46	-C/D
48	-REQ
50	-I/O

All odd-numbered pins except 25 are connected to ground. Pin 25 left open.

Table 2-4. Model CSC 100 Connector J3 Pin Assignments.

Signal	Pin Number
-DB (0)	26
-DB (1)	27
-DB (2)	28
-DB (3)	29
-DB (4)	30
-DB (5)	31
-DB (6)	32
-DB (7)	33
-DB (P)	34
GROUND	35
GROUND	36
GROUND	37
TERMPWR	38
GROUND	39
GROUND	40
-ATN	41
GROUND	42
-BSY	43
-ACK	44
-RST	45
-MSG	46
-SEL	47
-C/D	48
-REQ	49
-I/0	50

Pins 1-12 and 14-25 are connected to ground. Pin 13 left open.

Table 2-5. Model CSC 100 Connector J3 Pin Assignments (Alternative 2).

Signal Name	Pin Number		Signal Name
SHIELD GROUND	1	2	GROUND
+DB (0)	3	4	-DB (0)
+DB (1)	5	6	-DB (1)
+DB (2)	7	8	-DB (2)
+DB (3)	9	10	-DB (3)
+DB (4)	11	12	-DB (4)
+DB (5)	13	14	-DB (5)
+DB (6)	15	16	-DB (6)
+DB (7)	17	18	-DB (7)
+DB (P)	19	20	-DB (P)
DIFFSENS	21	22	GROUND
GROUND	23	24	GROUND
TERMPWR	25	26	TERMPWR
GROUND	27	28	GROUND
+ATN	29	30	-ATN
GROUND	31	32	GROUND
+BSY	33	34	-BSY
+ACK	35	36	-ACK
+RST	37	38	-RST
+MSG	39	40	-MSG
+SEL	41	42	-SEL
+C/D	43	44	-C/D
+REQ	45	46	-REQ
+I/O	47	48	-I/O
GROUND	49	50	GROUND

Table 2-6. Model CSC 200 Connector J3 Pin Assignments.

Signal Name	Pin Number		Signal Name
SHIELD GROUND	1	26	GROUND
+DB (0)	2	27	-DB (0)
+DB (1)	3	28	-DB (1)
+DB (2)	4	29	-DB (2)
+DB (3)	5	30	-DB (3)
+DB (4)	6	31	-DB (4)
+DB (5)	7	32	-DB (5)
+DB (6)	8	33	-DB (6)
+DB (7)	9	34	-DB (7)
+DB (P)	10	35	-DB (P)
DIFFSENS	11	36	GROUND
GROUND	12	37	GROUND
TERMPWR	13	38	TERMPWR
GROUND	14	39	GROUND
+ATN	15	40	-ATN
GROUND	16	41	GROUND
+BSY	17	42	-BSY
+ACK	18	43	-ACK
+RST	19	44	-RST
+MSG	20	45	-MSG
+SEL	21	46	-SEL
+C/D	22	47	-C/D
+REQ	23	48	-REQ
+I/O	24	49	-I/O
GROUND	25	50	GROUND

Table 2-7. Model CSC 200 Connector J3 Pin Assignments (Alternative 2).