M6809SET100(D2)
OCTOBER 1982

EXORSET USER'S GUIDE

Second Edition

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual is concerned primarily with the hardware features of EXORset and the firmware Monitor, EXORbug. Other manuals included in the standard configurations M6809SET33 and M6809SET100, deal with disk operation (XDOS), M6809 Assembly Language, CRT Editor and BASICM interpretive Compiler. This manual can be used to familiarize the user with the keyboard and back panel controls, as well as gaining an overview of the system architecture before proceeding into software development.

The EXORset is made up of 8 distinct functional units :

-- The EXORset Main Controller Board.
-- The CRT (9" or 12").
-- The dual mini-floppy assembly.
-- The Floppy Disk Controller board.
-- The ASCII keyboard and function keys assembly.
-- The power supply unit.
-- The enclosure. assembly.

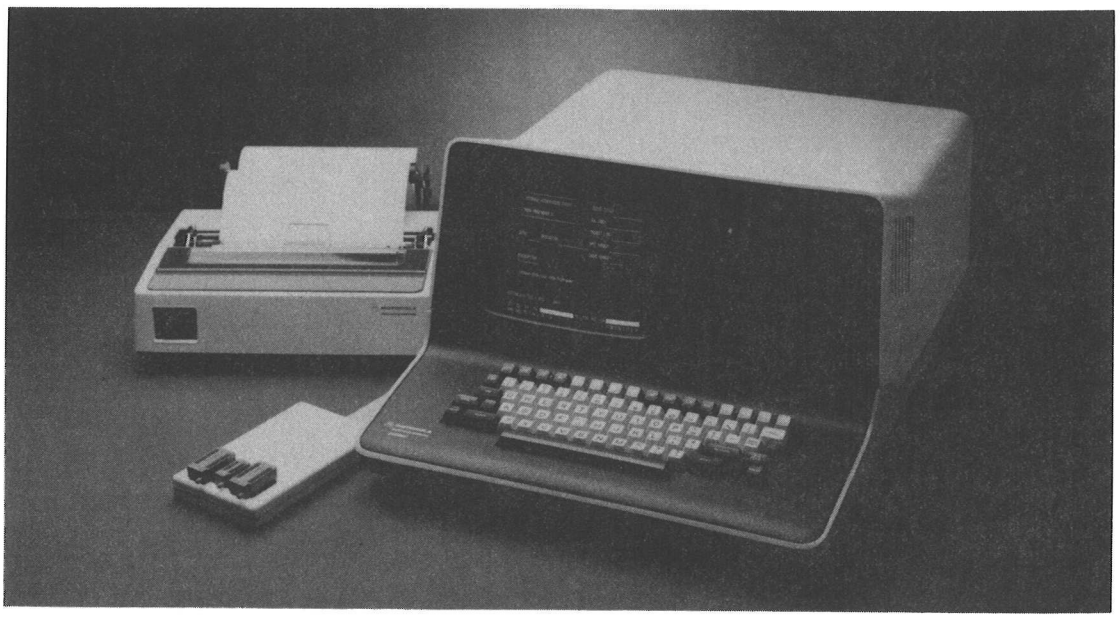


Figure 1-1 Typical EXORset 33 System

1.2 EQUIPMENT SUPPLIED

The EXORset 100 includes the functional units listed in paragraph 1.1. a software and documentation pack is supplied with the following utilities:

-- BASICM Interpretive Compiler
-- XDOS Disk Operating System
-- M6809 Macro Assembler and Linking Loader
-- CRT Editor
-- PLOT Tiny Graphics Package

1.3 OPTIONAL EQUIPMENT

A number of separately available modules can be used to expand the system capabilities. These include M68SETCOMPK a software package for file transfer between EXORciser and EXORset, M68SETMM12 a Listener/Talker/Controller Module for interfacing with an IEEE 488 Bus, M68SETPASCL a Pascal compiler and M68SETDSK3 an adapter kit for interfacing with the 1 or 2MB external floppy disk storage units M68DSK3-2 and M68SFDU2102E. PROM Programming capability can be added using M68PP4. The M68PRT100N2 is an 80 cps, 80/132 column compact matrix printer with semigraphic capability. The unit includes tractor feed and cabeling for immediate connection to the EXORset back panel.

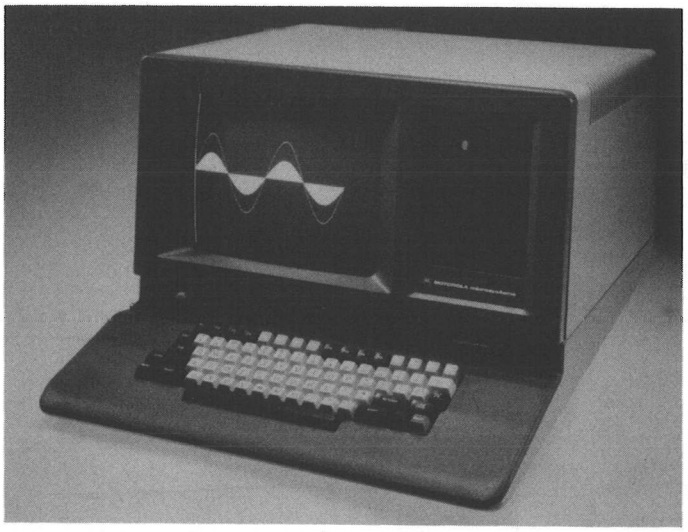


Figure 1-2 Typical EXORset 100 System

CHAPTER 2

INSTALLATION INSTRUCTIONS AND INTERCONNECTION CONSIDERATIONS

2.1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, and interconnection instructions for the EXORset. The EXORset is normally configured for standalone operation. If the unit is to be operated in standalone mode the user should, after unpacking and inspection, refer immediately to Chapter 3 of this manual. If however the EXORset is to be used in conjuction with other equipment, or with Motorola's Micromodule Family, the information provided in this chapter allows the unit to be installed as required using the available connectors and jumper options.

2.2 UNPACKING INSTRUCTIONS

Unpack the EXORset from its shipping carton and, referring to the packing list, verify that all of the items are present, including any of the options that may have been ordered. Save the packing materials for storing or reshipping of the system. If the shipping carton is damaged upon receipt, request that the carrier's agent be present while the system is being unpacked and inspected.

2.3 INSPECTION

The EXORset should be inspected upon receipt for broken, damaged, or missing parts or any other physical or electrical damage.

Before first applying power to the system, check that all connectors are properly inserted (power, keyboard, floppy-disk, CRT) as well as the floppy-disk Controller Module and the optional modules, if any.

2.4 CONNECTOR PIN ASSIGNMENT TABLES

Tables 2-1 to 2-13 list the pin assignments of the various connectors located on the EXORset boards and subassemblies. Refer to Chapter 6 for the location diagrams showing the position of connectors and jumper fields on the boards.

EXORset Main Controller Board :

CONNECTOR	TYPE	NAME	TABLE
J1A	50-pin Card-Edge	ASCII Keyboard	Table 2-1
J1B	23-pin Flex-Tail	ASCII Keyboard	Table 2-1
J2A	20-pin Card-Edge	Function keys	Table 2-2
J2B	8-pin Flex-Tail	Function keys	Table 2-2
J3	20-pin Card-Edge	Serial I/O	Table 2-3
J4	50-pin Card-Edge	Printer	Table 2-4
J5	20-pin	PTM	Table 2-5
J6	Cinch	Video Output	Table 2-6
J7	3-pin	Light Pen	Table 2-7
J8	5-pin	CRT Monitor	Table 2-8
J9	2x43-pin	EXORbus	Table 2-9
J10	2x43-pin	EXORbus	Table 2-9
J11	2x43-pin	EXORbus	Table 2-9
J12	2x43-pin	EXORbus	Table 2-9
J13	10-pin	Power	Table 2-10

EXORset Mini-Floppy Disk Controller Board :

CONNECTOR	TYPE	NAME	TABLE
P2	34-pin Card-Edge	Disk Interface	Table 2-12
P1	2x43-pin	EXORbus	Table 2-9

Mini-Floppy Disk Drive :

CONNECTOR	TYPE	NAME	TABLE
J1(BASF)	34-pin Card-Edge	Disk Interface	Table 2-12
J2(BASF)	4-pin	Power	Table 2-11

Video Display :

CONNECTOR	TYPE	NAME	TABLE
P2	10-pin Card-Edge	CRT Input	Table 2-13

Keyboard Assembly :

CONNECTOR	TYPE	NAME	TABLE
ASCII	23-pin Flex-Tail or 50-pin Card-Edge	ASCII Output	Table 2-1
FUNCT	8-pin Flex-Tail or 20-pin Card-Edge	Function Keys	Table 2-2

Back Panel Assembly:

The back panel of the EXORset is mounted with operator controls for power-on, reset, brightness and with connectors for Serial Port (J3), Printer port (J4) and Composite Video Output(J6). Provision is made for mounting 6 optional I/O connectors. As-supplied, the optional connector mountings are covered by a metal shield, which can be removed by unfastening four screws. The optional connectors on the back panel can attached via cable to card edge connectors on the EXORset Main Board or on any Micromodule installed on the EXORbus expansion slots.

Connector Mounting Location. (Refer to figure 2-1)

A: 40-pin parallel row male connector such as 3M 3324 for:
- Analog interfacing
- PROM Programmer IV connection
- EXORdisk III connection
- Other applications

B: 50-pin parallel row female connector such as UECL for:
- Parallel Interfacing
- Other Applications

C: IEC bus connector #1, 24-pin parallel row female, suitable for IEEE 488 bus connection with locker screws.

D: Connector for serial interfacing as described in the RS232C and V24 standards. Female, dual row, 25 pin. (Cannon or Amphenol type connector)

E: Serial Connector like D.

F:IEC bus connector #2 like C.

G: 50-Pin Cannon Connector (like J4).

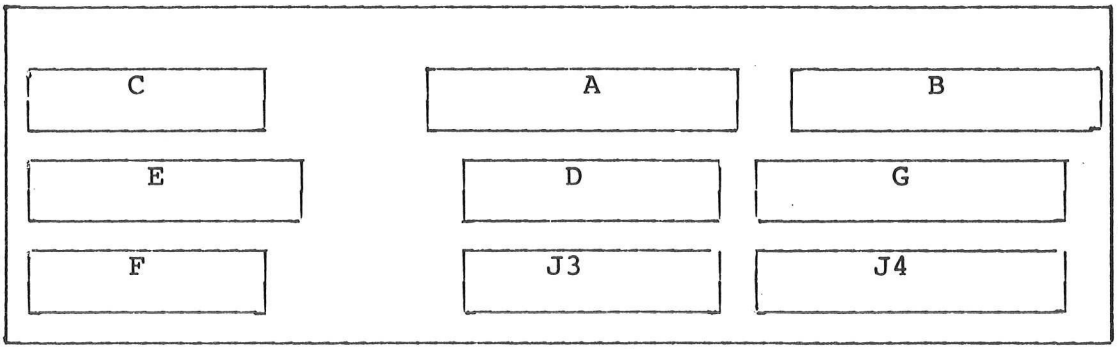


Figure 2-1 Back Panel Connector Locations

Table 2-1 ASCII Keyboard Connector Pin Assignments
(J1,Keyboard Assembly)

FLEX-TAIL J1B PIN	CARD-EDGE J1A PIN	NAME
1	45	Row 0
2	43	Row 2
3	41	Row 4
4	39	GND for ctrl keys (column 8)
5	37	RPT (Row F)
6	35	Row 6
7	33	CTRL (Row E)
8	31	Row 7
9	29	SHIFT (Row I)
10	27	SHIFT LOCK (Row J) (not used)
11	25	Column 0
12	23	Column 1
13	21	Column 2
14	19	Column 3
15	17	Column 4
16	15	Column 5
17	13	Column 6
18	11	Column 7
19	9	NUM PAD (Row G) (not used)
20	7	U/C (Row H)
21	5	Row 5
22	3	Row 3
23	1	Row 1

MATING CONNECTOR :
Flex-Tail : 23-pin Rect. Male 5-825437-0 or equivalent
Card-edge : 3M 3415-0001 or equivalent.

Table 2-2 Function Keys Connector Pin Assignments
(J2,Keyboard Assembly)

FLEX-TAIL J2B PIN	CARD-EDGE J2A PIN	NAME
1	15	Row A
2	13	Row C
3	11	Row B
4	9	Row D
5	7	Column A
6	5	Column B
7	3	Column D
8	1	Column C
MATING CONNECTOR : Flex-Tail : 8-pin Rect. Male AMP 5-825437-0 or equivalent Card-Edge : 3M 3461-0001 or equivalent.		

Table 2-3 Serial I/O (J3)

J3 on BACK PANEL:	J3 on PC CONNECTOR	PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1		1	GND	GROUND
14		2	DTR-	DATA TERMINAL READY low
2		3	TxDATA+	TRANSMITTED DATA - The line through which the terminal sends data to the modem.
15		4	TxDATA-	TRANSMITTED DATA low
3		5	RxDATA+	RECEIVED DATA - The line through which the modem sends data to the terminal.
16		6	RxDATA-	RECEIVED DATA low
4		7	RTS+	REQUEST TO SEND - The line through which the terminal requests permission to transmit data to the modem.
17		8	RTS-	REQUEST TO SEND low
5		9	CTS+	CLEAR TO SEND - The line through which the modem acknowledges the acceptance of a terminal request to send data.
18		10	CTS-	CLEAR TO SEND low
6		11	DSR+	DATA SET READY - The line through which the modem indicates its on-line, in-service, or active status.
19		12	DSR-	DATA SET READY low
7		13	GND	GROUND
20		14	DTR+	DATA TERMINAL READY - The line through which the terminal indicates its on-line, in-service, or active status.
8		15	DCD+	CARRIER DETECT - The line through which the modem indicates that its interfacing communications channel is in an acceptable active state.
21		16	DCD-	CARRIER DETECT low

17	RDCLK+	RECEIVE CLOCK - The line to be used to clock in and syncronize data into the terminal.
18	RDCLK-	RECEIVE CLOCK low
19	TDCLK+	TRANSMIT CLOCK - The line to be used to clock in and synchronize data into the modem
20	TDCLK-	TRANSMIT CLOCK low

MATING CONNECTOR :
3M 3461-0001 or equivalent.

Conversion of pin numbers: 25-Pin Cannon Plug (on back panel) to 20-pin Card Edge connector on main board.

Cannon	Card Edge		Cannon	Card Edge
1	1		14	2
2	3		15	4
3	5		16	6
4	7		17	8
5	9		18	10
6	11		19	12
7	13		20	14
8	15		21	16
9	17		22	18
10	19		23	20
11	-		24	-
12	-		25	-
13	-			

Refer to Section 2.6 for a description of the configuration jumpers for J3.

Table 2-4 Parallel I/O Connector Pin Assignments (J4)

BACK PANEL

	PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1	1	INPUT	INPUT PRIME - A low-level output signal which clears the printer buffer and initializes the logic. (Not used by all printers).
2	3	GND	GROUND - Printer interface ground.
3	5	FAULT	FAULT - A low-level input signal that indicates a printer fault condition such as paper empty, light detect, or a desselect condition. (Not used by all printers).
4	7	GND	GROUND - Same as pin 3.
5	9	PB7	PERIPHERAL DATA LINE (PB7) - Free.
6	11	PB6	PERIPHERAL DATA LINE (PB6) - Free.
7	13	PB5	PERIPHERAL DATA LINE (PB5) - Free.
8	15	PB4	PERIPHERAL DATA LINE (PB4) - Free.
9	17	PB3	PERIPHERAL DATA LINE (PB3) - Free.
10	19	BUSY	BUSY - An input signal indicating that the printer cannot receive data.
11	21	OUT-PP	OUT OF PAPER - A high-level input indicating the printer is out of paper.
12	23	SEL	SELECT - A high-level input signal indicating that the printer is selected.
13	25	PD8	PERIPHERAL DATA LINE (PD8) - Output data to printer from PA7 of PIA.
14	27	PD7	PERIPHERAL DATA LINE (PD7) - Same as pin 25 except bit A6.
15	29	PD6	PERIPHERAL DATA LINE (PD6) - Same as pin 25 except bit A5.
16	31	PD5	PERIPHERAL DATA LINE (PD5) - Same as pin 25 except bit A4.
17	33	PD4	PERIPHERAL DATA LINE (PD4) - Same as pin 25 except bit A3.
18	35	PD3	PERIPHERAL DATA LINE (PD3) - Same as pin 25 except bit A2.
19	37	PD2	PERIPHERAL DATA LINE (PD2) - Same as pin 25

			except bit A1.
20	39	PD1	PERIPHERAL DATA LINE (PD1) - Same as pin 25 except bit A0.
21	41	GND	GROUND - Same as pin 3.
22	43	DATASTB	DATA STROBE - A 1.0 microsecond output pulse used to clock data from the MPU to the printer logic.
23	45	GND	GROUND - Same as pin 3.
24	47	ACKNLG	ACKNOWLEDGE - A low-level input pulse indicating the input of a character into memory or the end of a functional operation.
25	49	GND	GROUND - Same as pin 3.

All even numbers (2-50) : GROUND.

MATING CONNECTOR :
3M 3415-0001 or equivalent.

Card-Edge to Back Panel Connector - Pin Conversion

1	1	26	38
2	26	27	14
3	2	28	39
4	27	29	15
5	3	30	40
6	28	31	16
7	4	32	41
8	29	33	17
9	5	34	42
10	30	35	18
11	6	36	43
12	31	37	19
13	7	38	44
14	32	39	20
15	8	40	45
16	33	41	21
17	9	42	46
18	34	43	22
19	10	44	47
20	35	45	23
21	11	46	48
22	36	47	24
23	12	48	49
24	37	49	25
25	13	50	50

Table 2-5 Timer Interface Signals (J5)

PIN		SIGNAL NAME AND DESCRIPTION
1	G1	GATE INPUT 1 - Low level asyncronous TTL compatible input signal as trigger or clock gating to Timer.
	O1	TIMER OUTPUT 1 -High level output from PTM
	C1	CLOCK INPUT 1 - Low level asyncronous TTL voltage level input signal used to decrement Timer.
	G2	GATE INPUT 2 - Same as J5-1.
9	O2	TIMER OUTPUT 2 - Same as J5-3.
11	C2	CLOCK INPUT 2 - Same as J5-5.
13	G3	GATE INPUT 3 - Same as J5-1.
15	O3	TIMER OUTPUT 3 - Same as J5-3.
17	C3	CLOCK INPUT 3 - Same as J5-5,
2,4, 6,8, 10, 12,14, 16,18, 19,20	GND	GROUND

Table 2-6 Composite Video Connector Pin Assignments(J6)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1	VID	VIDEO OUT - Composite video out
2	GND	GROUND

Table 2-7 Light Pen Connector Pin Assignments(J7)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1	+5v	
2	LPSTB	Light Pen Strobe (input to U100)
3	GND	Ground Jumper connection 2-3 = no light pen

Table 2-8 Video Display Connector Pin Assignments (J8)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1		Composite Video signal Out (TTL-Level)
2	GND	Ground
3	HSYNC	Horizontal Sync.
4	VSYNC	Vertical Sync.
5	Key	

Table 2-9 EXORbus Connector (J9,J10,J11,J12)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
A	+5 Vdc	+5 Vdc POWER - Used for the system logic circuits and available to the user for prototype module requirements (10 amps tot. max).
B	+5 Vdc	+5 Vdc POWER - Same as above.
C	+5 Vdc	+5 Vdc POWER - Same as above.
D	IRQ	INTERRUPT REQUEST - A low level sensitive input signal to the MPU used to request generation of an MPU interrupt sequence. This signal is latched every cycle during Q high, but will not be received by the MPU until the following bus cycle. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin executing the interrupt sequence.
E	NMI	NON-MASKABLE INTERRUPT - A low going edge sensitive input signal to the MPU used to request generation of a MPU non-maskable interrupt sequence. When sampled low one cycle after being sampled high (samples taken every cycle during Q high), an NMI will be triggered. The MPU will recognize the signal on the following bus cycle and begin a non-maskable interrupt sequence at that time, regardless of the logic state of the Interrupt Mask Bit in the MPU Condition Code Register.
F	VMA	VALID MEMORY ADDRESS - A high level TTL

		compatible signal produced by the MPU module and used to indicate that a valid memory address is present on the address bus.
H	GND	Ground. (Not used)
J	E	ENABLE - Clock signal generated by the clock circuitry on the EXORset Main Controller Board. E is similar to phase 2 clock in 6800 systems. Data is placed on the bus during E.
K	GND	GROUND - Power ground for +/- 12 Vdc.
L	MEMCLK	MEMORY CLOCK - Ungated, TTL level clock signal, in phase with E.
M	-12Vdc	-12 Vdc POWER - Used for system logic and available to the user for custom designed prototype modules (1.0 A max).
N	BUSREQ	An active low signal used to request access to the system bus. Alow on this line will cause the MPU Module to three-state (off or high impedance state) the data,address and R/W lines. A BUSGNT signal (pin 15) wiil also be generated at this time. (Not used)
P	BA	BUS AVAILABLE - This signal, decoded with Bus Status (BS) indicates the MPU state : BA BS 0 0 Normal 0 1 Interrupt Acknowledge 1 0 Sync. Acknowledge 1 1 Halt or Bus Grant
R	MEMRDY	MEMORY READY
S	LIC	LAST INSTRUCTION CYCLE (Not used)
T	+12Vdc	+12 Vdc POWER - Used for the system logic and available to the user for custom designed prototype modules (5.0 A max).
U	STANDBY	STANDBY POWER - Not used in the EXORset.
V	PWRFAIL	POWER FAIL - Not used in the EXORset
W	PARITY	PARITY ERROR - Not used in the EXORset.
X	GND	GROUND
Y	GND	GROUND
Z	GND	GROUND
Anot	FIRQ	FAST INTERRUPT - A low level sensitive input to the MPU used to request generation of an MPU fast interrupt sequence. The MPU will wait until it completes the instruction being

		executed before it recognizes the request. At that time, if the fast interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin executing the fast interrupt sequence.
Bnot	GND	GROUND
Cnot	---	USER DEFINED
Dnot	---	USER DEFINED
Enot	---	USER DEFINED
Fnot	---	USER DEFINED
Hnot	D3not	DATA (bit 3) - One of 8 bi-directional data lines used to provide a two-way data transfer between the MPU and all other plug-in modules within the system. The data bus drivers on the other modules are in their off or high impedance state except when selected during a memory read or write operation.
Jnot	D7not	DATA (bit 7) - Same as D3not on pin Hnot.
Knot	D2not	DATA (bit 2) - Same as D3not on pin Hnot.
Lnot	D6not	DATA (bit 6) - Same as D3not on pin Hnot.
Mnot	A14	ADDRESS (bit 14) - One of the 16 address lines from the MPU that permits the MPU to select any addressable memory location within the EXORset.
Nnot	A13	ADDRESS (bit 13) - Same as A14 above.
Pnot	A10	ADDRESS (bit 10) - Same as A14 above.
Rnot	A9	ADDRESS (bit 9) - Same as A14 above.
Snot	A6	ADDRESS (bit 6) - Same as A14 above.
Tnot	A5	ADDRESS (bit 5) - Same as A14 above.
Unot	A2	ADDRESS (bit 2) - Same as A14 above.
Vnot	A1	ADDRESS (bit 1) - Same as A14 above.
Wnot	GND	GROUND
Xnot	GND	GROUND
Ynot	GND	GROUND
1	+5 Vdc	+5 Vdc POWER - Used for the system logic circuits and available to the user for prototype module requirements (10 A total max).

2	+5 Vdc	+5 Vdc POWER - Same as above.
3	+5 Vdc	+5 Vdc POWER - Same as above.
4	HALT	HALT - A normally high level signal used to halt the MPU. Alow level on the HALT input causes the MPU to halt at the end of the present instruction, and remain halted indefinitely intil the HALT pin is driven high.
5	RESET	RESET - This buffered input signal to the MPU is used to restart the EXORset when power is initially applied. Restart occurs on the low-to-high transition of the RESTART signal. If the RESTART pushbutton switch, located on the Main Controller Board, is depressed while the system is operating, the low-to-high transition of the RESET signal will cause the MPU to execute the EXORbug restart routine or the restart routine indicated by the user.
6	R/W	READ/WRITE - This signal is generated by the MPU and indicates to the other modules contained within the system that the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Additionally, when the MPU is halted, this signal will be in the read state.
7	Qout	Qout - A quadrature clock signal generated by the MPU which leads the E (enable) signal. Addresses from the MPU will be guaranteed valid with the leading edge of Q. It has a phase shift of 90 deg. compared to the E signal.
8	GND	GROUND - Power ground for +/-12Vdc.
9	GND	GROUND - Power ground for +/-12Vdc.
10	VUA	VALID USER'S (ALTERNATE MAP) ADDRESS - This signal, when high, allows additional module(s) to respond in address map 2 .
11	-12Vdc	-12Vdc POWER - Used for the system logic circuits and available to the user for custom designed prototypes modules (1.0 A max).
12	REFREQ	REFRESH REQUEST - When low, this input signal to the MPU Module initiates a memory refresh cycle of the dynamic memory modules. The memory clock signal will continue to run to allow memory refreshing. (Not used)
13	REFGNT	REFRESH GRANT - (Not used)
14	DEBUG	DEBUG - Not used in the EXORset.

15	BUSGNT	THREE-STATE GRANT - This signal is generated in response to a low level BUSREQ. When high this signal indicates that the MPU is not in control of the bus. (Not used)
	+12Vdc	+12Vdc POWER - Used for the system logic circuits and available to the user for prototype module requirements.
17	STANDBY	STANDBY POWER - Not used in the EXORset.
18	CLK	CLOCK - Not used in the EXORset.
19	VXA	VALID EXECUTIVE ADDRESS - A high level signal generated in place of the VUA when EXORbug is addressing the executive portion of the memory map. Additionally all peripheral modules must be set to respond to VXA if the user wants to operate those modules in the Executive portion of the map.
20	GND	GROUND
21	GND	GROUND
22	GND	GROUND
23	BS	BUS STATUS - This signal, decoded with Bus Available (BA) indicates the MPU state : BA BS 0 0 Normal 0 1 Interrupt Acknowledge 1 0 Sync. Acknowledge 1 1 Halt or Bus Grant
24	GND	GROUND
25	---	USER DEFINED - This signal line may be used for custom modules.
26	---	USER DEFINED - Same as above.
27	---	USER DEFINED - Same as above.
28	---	USER DEFINED - Same as above.
29	D1not	DATA (bit 1) - Same as D3not on pin Hnot.
30	D5not	DATA (bit 5) - Same as above.
31	D0not	DATA (bit 0) - Same as above.
32	D4not	DATA (bit 4) - Same as above.
33	A15	ADDRESS (bit 15) - Same as A14 on pin Mnot.
34	A12	ADDRESS (bit 12) - Same as above.
35	A11	ADDRESS (bit 11) - Same as above.

36	A8	ADDRESS (bit 8) - Same as above.
37	A7	ADDRESS (bit 7) - Same as above.
38	A4	ADDRESS (bit 4) - Same as above.
39	A3	ADDRESS (bit 3) - Same as above.
40	A0	ADDRESS (bit 0) - Same as above.
41	GND	GROUND
42	GND	GROUND
43	GND	GROUND

Table 2-10 Main Controller Board Power Connector (J13)

PIN	SIGNAL	WIRE COLOR
1	+5 Vdc	Red
2	+5 Vdc	Red
3	+5 Vdc sense	Red
4	+12 Vdc return	Orange
5	+5 Vdc sense return	Black
6	-12 Vdc return	Green
7	+5 Vdc return	Black
8	-12 Vdc	Blue
9	+5 Vdc return	Black
10	+12 Vdc	Red / White
MATING CONNECTOR : AMP 1-480285-0 or equivalent.		

Table 2-11 Mini-Disk Drive Power Connector Pin Assignments
J5(BASF)

PIN	SIGNAL
1	+12 V
2	GND
3	Free
4	+5 V
MATING CONNECTOR : AMP 1-480424-0 with pins 60619-1 or equivalent.	

Table 2-12 Mini-Floppy Disk Drive Signal Connector Pin Assignments J1(BASF)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
2	HDL	HEAD LOAD - This logic low level output signal is used to position the flexible diskette against the recording head.
4	---	NOT USED -
6	RDY	READY - This logic low level signal (generated by the disk drive electronics) is used to indicate that the flexible diskette is inserted correctly into the disk drive, and that the dc voltage levels and disk speed is correct.
8	IDX	INDEX - A logic low level signal from the disk drive used to indicate the beginning of a track. This pulse occurs once per revolution of the diskette (200 ms period).
10	SEL0	SELECT 0 - This logic low level signal is used to select drive 0.
12	SEL1	SELECT 1 - Same as pin 10, except for drive 1.
14	SEL2	SELECT 2 - Same as pin 10, except for drive 2 (not used in the EXORset).
16	MOT	MOTOR ON - This logic low signal is used to turn the drive(s) motor(s) on.
18	DIR	DIRECTION - This signal is used in conjunction with the STEP signal to move the R/W head from track to track. When this signal is a logic low level, the R/W head is moved to the lower numbered tracks (out). When this signal is a logic high level, the head moves to the higher numbered tracks (in). This signal must remain in the desired logic state during the duration of the STEP signal.
20	STP	STEP - This signal is used in conjunction with the DIRECTION signal to move the R/W head from track to track. A logic low level pulse causes the head to be moved one track (step) in the direction indicated by the DIRECTION signal.
22	WDT	WRITE DATA - This signal consists of logic low level pulses representing data to be recorded on the flexible diskette. Write current reverses direction on the leading edge of each pulse.

24	WGT	WRITE GATE - A logic low level signal used to enable recording of data on the flexible diskette. When this signal is a logic high level, reading data from the flexible disk is enabled.
26	TRZ	TRACK 0 - Logic low level signal used to indicate when the R/W head is positioned over track 0.
28	WPT	WRITE PROTECT - A logic low signal indicating that the diskette is write protected (write protect notch of the diskette left open).
30	RDT	READ DATA - Unseparated "Raw Data" (clock and data) read from the diskette.
32	---	NOT USED -
34	---	NOT USED -
All odd pins (1-33) : GROUND		
MATING CONNECTOR : 3M 3463-0001 or equivalent.		

Table 2-13 Video Display Connector Pin Assignments (P2)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1	GND	GROUND - Video Signal Return
2	RB	REMOTE BRIGHTNESS - 200 Kohm pot.terminal 1
3	RB	REMOTE BRIGHTNESS - 200 Kohm pot.terminal 2
4	RB	REMOTE BRIGHTNESS - 200 Kohm pot.cursor
5	--	Not Used
6	TTLH	TTL HSYNC. IN - Not used
7	+12v	Power in
8	VID	Composite Video in.
9	TTLV	TTL VSYNC. In - Not used
10	GND	GROUND +12v Power Return
MATING CONNECTOR : AMP 583299-1 or equivalent		

(This table refers to 9" monitor units. The pin assignments for 12" units are described in Appendix B).

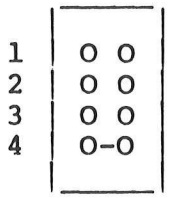
2.5 JUMPER CONNECTIONS

This Section lists the jumper connections of the Main Controller Board in numeric sequence from K1 through K23. The location of each jumper can be seen in the Component Location Diagram (Section 6). The jumper fields KA,KB,KC & KD (Serial I/O Configuration) are described in Section 2.6. The diagrams show the as-delivered jumper connections for each field. Where no connection is shown, the unit is supplied without jumper connections in that field.

2.5.1 EXORset Main Controller Board Jumper Options

2.5.1.1 K1: Timer Gate Enable

This jumper field allows the user to tie the three timer inputs (G1, G2, G3) to ground, enabling the three timers in the PTM. The as-delivered configuration is with timers 2 and 3 disabled and timer 1 enabled with cycle count.



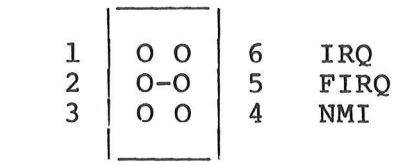
- 8 - Enable timer 1 gate
- 7 - Enable timer 2 gate
- 6 - Enable timer 3 gate
- 5 - Enable timer 1 gate (cycle count)

Options 1-8 and 4-5 are mutually exclusive.

PIN	SIGNAL	FUNCTION
1-3		Ground
4		Cycle Count
5	G1	Timer 1
6	G2	Timer 2
7	G3	Timer 3
8	G1	Timer 1

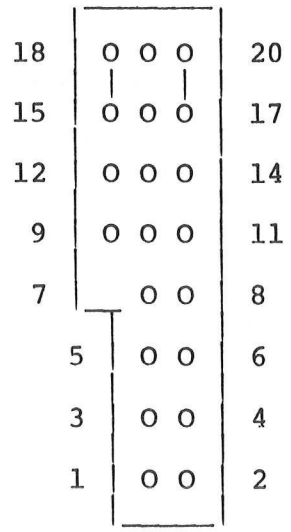
2.5.1.2 K2: PTM Interrupt Request Priority

The PTM can generate an IRQ to the MPU. This can be assigned on K2 to one of three priorities: IRQ, FIRQ or NMI. The as-delivered version is for the PTM to generate a FIRQ.



2.5.1.3 K3: PTM Timer Source and Interrupt

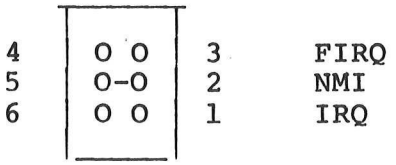
K3 consists of 12 possible jumpers which can be considered in two groups: the first four are for the timer source clock selection, and the remaining eight are for timer interrupt selection. The as-delivered configuration is with no external timer source and with the NMI and FIRQ outputs of the timers disabled.



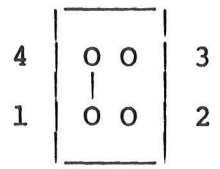
CONNECTION		FUNCTION
1-2	C3	1.27 MHz input (FIRQ)
3-4	C3	Receiver Clock input (FIRQ)
5-6	C2	Receiver Clock input (FIRQ)
7-8	C1	Receiver Clock input (FIRQ)
9-10	O1	Timer 1 Output to interrupt (NMI)
10-11	O1	Timer 1 Output to interrupt (FIRQ)
12-13	O2	Timer 2 Output to interrupt (NMI)
13-14	O2	Timer 2 Output to interrupt (FIRQ)
15-16	O3	Timer 3 Output to interrupt (NMI)
16-17	O3	Timer 3 Output to interrupt (FIRQ)
18-19	GND	Interrupt Disable (NMI)
19-20	GND	Interrupt Disable (FIRQ)

2.5.1.3 K4: ACIA/SSDA Interrupt Request Priority

The user has the option of using the IRQ from the ACIA/ SSDA to generate an IRQ, a FIRQ or an NMI to the MPU. In the as-delivered configuration the ACIA/SSDA IRQ generates an NMI.



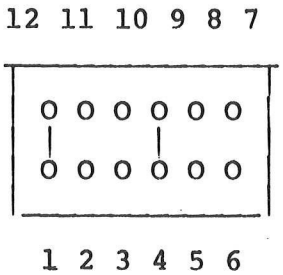
2.5.1.5 K5: Internal or External RCLK



CONNECTION	FUNCTION
1-4	Internal Clock
2-3	External Clock

2.5.1.6 K6: INTERRUPT PIA 1

This jumper field is used to connect either the normal interrupt IRQ, the fast interrupt FIRQ or non-maskable interrupt NMI to the two sides of the PIA. Either interrupt (or none) may be connected to each side of the PIA independently. As delivered, the NMI is connected to both sides.

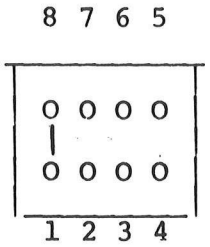


CONNECTION	FUNCTION
1-12	NMI A-Side
2-11	FIRQ A-Side
3-10	IRQ A-Side
4-9	NMI B-Side
5-8	FIRQ B-Side
6-7	IRQ B-Side

K7 not assigned

2.5.1.7 K8: Baud Rate Selection

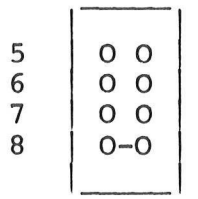
Baud rate selection for the serial I/O interface is user-selected at K8. The as-delivered baud rate is 9600 baud.



Jumper in = L
No Jumper = H

CONNECTION				FUNCTION
4-5	3-6	2-7	1-8	Baud Rate
L	L	L	L	50
L	L	L	H	75
L	L	H	L	110
L	L	H	H	134,5
L	H	L	L	150
L	H	L	H	300
L	H	H	L	600
L	H	H	H	1200
H	L	L	L	1800
H	L	L	H	2000
H	L	H	L	2400
H	L	H	H	3600
H	H	L	L	4800
H	H	L	H	7200
H	H	H	L	9600
H	H	H	H	19200

2.5.1.8 K9: Dynamic RAM Power Source Select



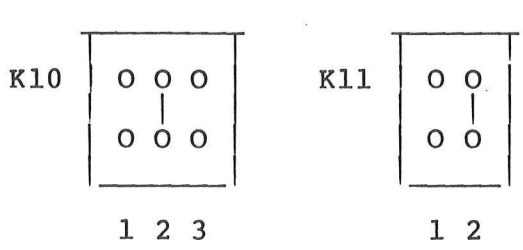
}Dynamic RAM with 3 voltages(MCM4116)

Dynamic RAM with 1 voltage (Intel 2118)

PIN	SIGNAL
1	+5v
2	-5v
3	+5v
4	+12v
5	RAM Socket pin 8
6	RAM Socket pin 9
7	RAM Socket pin 1
8	RAM Socket pin 8

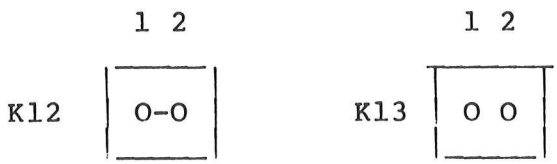
2.5.1.9 K10/K11: EPROM U46-U47-U48 Power Source Select.

(Requires different address decoder PROMs U50,U51)



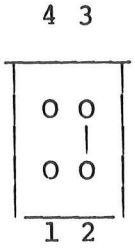
CONNECTION		FUNCTION
K10 1-6	K11 2-3	2K EPROM MCM2716
K10 2-5	K11 2-3	4K EPROM INT2732/HN462732/MBM2732
K10 1-6	K11 1-4	4K EPROM MCM2532
K10 3-4	K11 1-4	8K EPROM MCM68764

2.5.1.10 K12/K13: Locate U46 in Primary or Secondary Map



CONNECTION	FUNCTION
K12 Jumper in, K13 No Jumper	Dyn. RAM ($C000-$DFFF) enabled. U46 in secondary map.
K12 No Jumper, K13 Jumper in	Dyn. RAM ($C000-$DFFF) disabled U46 in primary Map.

2.5.1.11 K14: Relocate Graphics RAM Area.

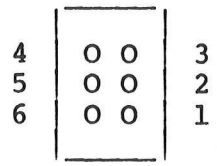


L= Jumper in, H= No Jumper

CONNECTION		FUNCTION
1-4	2-3	Graphics RAM Area
L	L	$0000-$3FFF
H	L	$4000-$7FFF
L	H	$8000-$8FFF

K15 not assigned

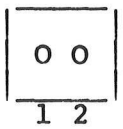
2.5.1.12 K16: CRT and Map Initialization Options.



No Jumper=H Jumper in=L

CONNECTION			FUNCTION
1-6	2-5	3-4	
H	H	H	80 Characters/Line 50 Hz.
H	L	H	80 Characters/Line 60 Hz.
L	H	H	40 Characters/Line 50 Hz.
L	L	H	40 Characters/Line 60 Hz.
X	X	H	MAP 1
X	X	L	MAP 2

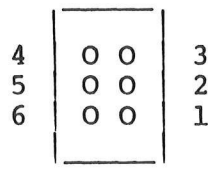
2.5.1.13 K17: Power on PLL



No Jumper = Connection to voltage regulator U119 (MC78L05)

Jumper in = Connection to power supply.
Voltage Regulator U119 out.

2.5.1.14 K18: Keyboard Encoder Nationality Options



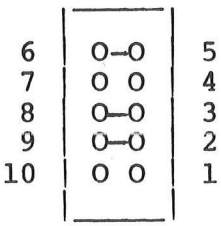
Jumper in = H, No Jumper = L

CONNECTION			LANGUAGE
1-6	2-5	3-4	
H	H	H	English
H	L	L	Spanish
L	H	H	German
L	H	L	Swedish
L	L	H	Norwegian/Danish
L	L	L	French

K19 not assigned.

2.5.1.15 K20: ACIA/SSDA Select

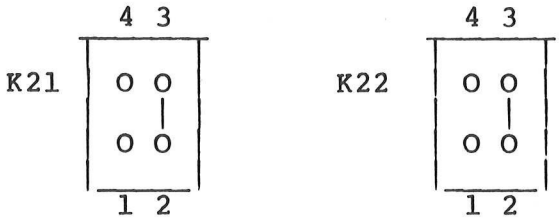
The EXORset Main Controller Board is shipped supplied with an MC6850 ACIA and K20 is configured for this chip. The user has the option of supporting syncronous serial communications by replacing the MC6850 ACIA with an MC6852 SSDA. For either configuration, the user has the selection of RS232C, RS422 and RS423 signal interfaces. Additionally, for either configuration, the necessary send and receive clocks may be transmitted or received.



CONNECTION			FUNCTION
2-9	3-8	5-6	ACIA
4-7	1-10		SSDA

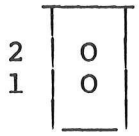
2.5.1.16 K21/K22: EPROM U45 Power Source Select

(Requires different address decoding PROM in U50,U51)



CONNECTION		FUNCTION
K21	K22	
1-4	2-3	2K EPROM MCM2716
2-3	2-3	4K EPROM INT2732/HN462732/MBM2732
1-4	1-4	4K EPROM MCM2532

2.5.1.17 K23: Optional Video Signal on Coax Connector



Jumper in = Comp. Video Signal on coax. card edge connector.

No Jumper = no video signal on coax. connector.

2.5.2 EXORset Mini-Floppy Disk Controller Board Jumper Options

SWA-1 (OUT) IN OUT	Low current signal : to P2 pin 34 (provision for norm. drives) if mini-floppy drives are used
SWA-2 (OUT) IN OUT	Optional drive 3 : SELECT3 signal to P2 pin 4 not connected
SWA-5 SWA-6 (OUT) (IN) IN OUT OUT IN	FDC clock select : 1 MHz clock to FDC (provision for normal drive) 500 KHz clock to FDC (mini-floppy)
SWA-7 SWA-8 (OUT) (IN) IN OUT OUT IN	MEMCLK / E select : MEMCLK signal to FDC / clock divider E signal to clock divider

16K RAM base address select :

SWB-4 (OUT)	SWB-3 (IN)	SWB-2 (IN)	SWB-1 (OUT)	
IN	OUT	IN	OUT	0000
IN	OUT	OUT	IN	4000
OUT	IN	IN	OUT	8000
OUT	IN	OUT	IN	C000

FDC and disk driver base address :

SWC-8 (OUT)	SWC-7 (IN)	SWC-6 (OUT)	SWC-5 (IN)	SWC-4 (OUT)	SWC-3 (IN)	SWC-2 (IN)	SWC-1 (OUT)	
IN	OUT	IN	OUT	IN	OUT	IN	OUT	0000
IN	OUT	IN	OUT	IN	OUT	OUT	IN	1000
IN	OUT	IN	OUT	OUT	IN	IN	OUT	2000
IN	OUT	IN	OUT	OUT	IN	OUT	IN	3000
IN	OUT	OUT	IN	IN	OUT	IN	OUT	4000
IN	OUT	OUT	IN	IN	OUT	OUT	IN	5000
IN	OUT	OUT	IN	OUT	IN	IN	OUT	6000
IN	OUT	OUT	IN	OUT	IN	OUT	IN	7000
OUT	IN	IN	OUT	IN	OUT	IN	OUT	8000
OUT	IN	IN	OUT	IN	OUT	OUT	IN	9000
OUT	IN	IN	OUT	OUT	IN	IN	OUT	A000
OUT	IN	IN	OUT	OUT	IN	OUT	IN	B000
OUT	IN	OUT	IN	IN	OUT	IN	OUT	C000
OUT	IN	OUT	IN	IN	OUT	OUT	IN	D000
OUT	IN	OUT	IN	OUT	IN	IN	OUT	E000
OUT	IN	OUT	IN	OUT	IN	OUT	IN	F000

SWD-1 (OUT)	SWD-2 (IN)	READY select :
IN	OUT	READY generated on-board (for drives without READY signal)
OUT	IN	READY signal from the drive

Map assignment :

SWD-3 (OUT)	SWD-4 (OUT)	SWD-7 (OUT)	SWD-8 (IN)	
IN	OUT	IN	OUT	FDC and disk driver in map 1
IN	OUT	OUT	IN	FDC and disk driver in map 2
OUT	IN	IN	OUT	FDC and disk driver in map 2
OUT	IN	OUT	IN	FDC and disk driver in map 1
OUT	OUT	X	X	FDC and disk driver respond in both maps
X	X	OUT	OUT	FDC and disk driver in map 1 or 2 (depending on SWD-3 and SWD-4)

2.6 USE AS A TERMINAL AND AS A HOST COMPUTER

The user has the option of connecting the EXORset to another device via a connector on the back panel. As-delivered the EXORset is jumper-configured as an RS232C terminal with 9600 baud data transmission rate. A 25-pin cannon plug is mounted on the back panel.

2.6.1 Terminal Mode/ Standalone Mode Keyboard Option

If the EXORset is configured as a terminal (refer to the jumper options in the sections below), it can be switched from standalone mode of operation (off-line) to terminal (or on-line) mode by entering the following command from the keyboard

XCOM

To switch the EXORset from terminal mode (on-line) to standalone mode enter the sequence:

ESC-O

Note that this command only works if it is echoed from the host computer.

2.6.2 KA/KB/KC/KD: Serial I/O Port Configuration

These 72 Jumpers are divided into four rows of 18 columns, KA through KD. Two-position jumper plugs are used to connect the pins. KA-KD are used to configure the EXORset for the desired serial inputs and outputs. The unit can be made compatible with RS232C, RS422 or RS423, as a Modem/Data Set or Data Terminal, or a 20 mA. current loop modem through the Micromodule 11 interface. The MC6850 ACIA may be replaced with a user-supplied MC6852 SSDA. The as-delivered configuration is for RS232C, as a terminal, using an ACIA. The following pages outline the seven standard serial I/O configurations possible . These configurations are intended for use with RS232C and RS449 mechanical interface standard connector assemblies. Care should be taken in making these connections, so as to prevent possible damage to components, since it is possible to short the power supplies.

2.6.3 Higher Noise Immunity Option

In RS232C and RS423 interface applications, all complementary (-) signals which are unused, may be grounded to allow for a twisted pair configuration whose higher noise immunity transmission line characteristics approach that of an RS422 interface. This is done by adding jumpers KA2, KA6, KA8, KA10, KA12, KA14.

2.6.4 Clock Transmission Options

Serial receiver and transmitter clocks may be transferred to and from the EXORset. This is needed in syncronous serial communication applications, when an SSDA is used, but may also be used elsewhere. The jumpers necessary to make available the clock signals are shown below.

For an RS232C Modem Configuration:

Connector J3 pins 17 & 18 RDCLK+,- (output signal), jumpers KA15, KA16
Connector J3 pins 19 & 20 TDCLK+,- (input signal), jumpers KC17, KD12
Signal Reference: jumper KD2.

For an RS422 Modem Configuration:

Connector J3 pins 17 & 18 RDCLK+,- (output signal), jumpers KB15, KB16
Connector J3 pins 19 & 20 TDCLK+,- (input signal), jumpers KC17, KC18
Line termination is provided by optional resistor (typically 100 ohms at 1/4 W) for long distance transmission or high noise environments.

For an RS423 Modem Configuration

Connector J3 pins 17 & 18 RDCLK+,- (output signal), jumpers KA15,KA16
Connector J3 pins 19 & 20 TDCLK+,- (input signal), jumpers KC17, KD12
Signal reference jumper KD1.
NOTE: If terminal clock receivers are unable to withstand +/- 15 vdc on their inputs, then add the optional resistors (2K or 3.3K ohms).

For an RS232C Terminal Configuration

Connector J3 pins 19 & 20 TDCLK+,- (output signal), jumpers KA17, KA18
Connector J3 pins 17 & 18 RDCLK+,- (input signal), jumpers KC15, KC16
Signal reference jumper KD2.
Output slew rate control is provided at optional capacitor C7 (typically 330 pF) for long distance transmission or high noise environments.

For an RS422 Terminal configuration

Connector J3 pins 19 & 20 TDCLK+,- (output signal), jumpers KB17, KB18

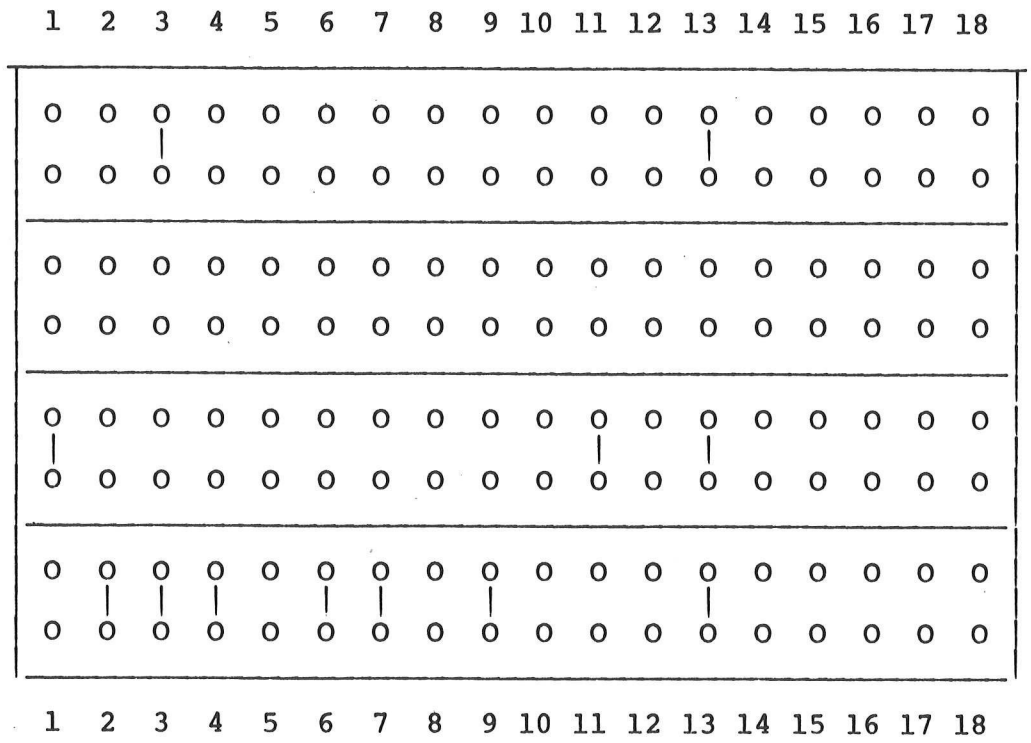
Connector J3 pins 17 & 18 RDCLK+,- (input signal), jumpers KC15, KC16
Line termination is provided by optional resistor R1 (typically 100 ohms at 1/4W) for long distance transmission or high noise environments.

For an RS423 Terminal Configuration:

Connector J3 pins 19 & 20 TDCLK+,- (output signal), jumpers KA17, KA18
Connector J3 pins 17 & 18 RDCLK+,- (input signal), jumpers KC15,KC16
Signal Reference Jumper KD1

NOTE: If modem clock receivers are unable to withstand +/- 15vdc on their inputs, then add the optional resistors (2K or 3.3K ohms).

2.6.5 Jumper Configuration for EXORset as an RS232C Modem/Data Set



	J3 PINS	SIGNALS	JUMPERS
INPUT:	14	DTR	KC11,KD4
	3	TxDATA	KC1,KD3
OUTPUT:	15	DCD	KA13,KC13, KD13
	11	DSR	KD9
	9	CTS	KD7
	5	RxDATA	KA3

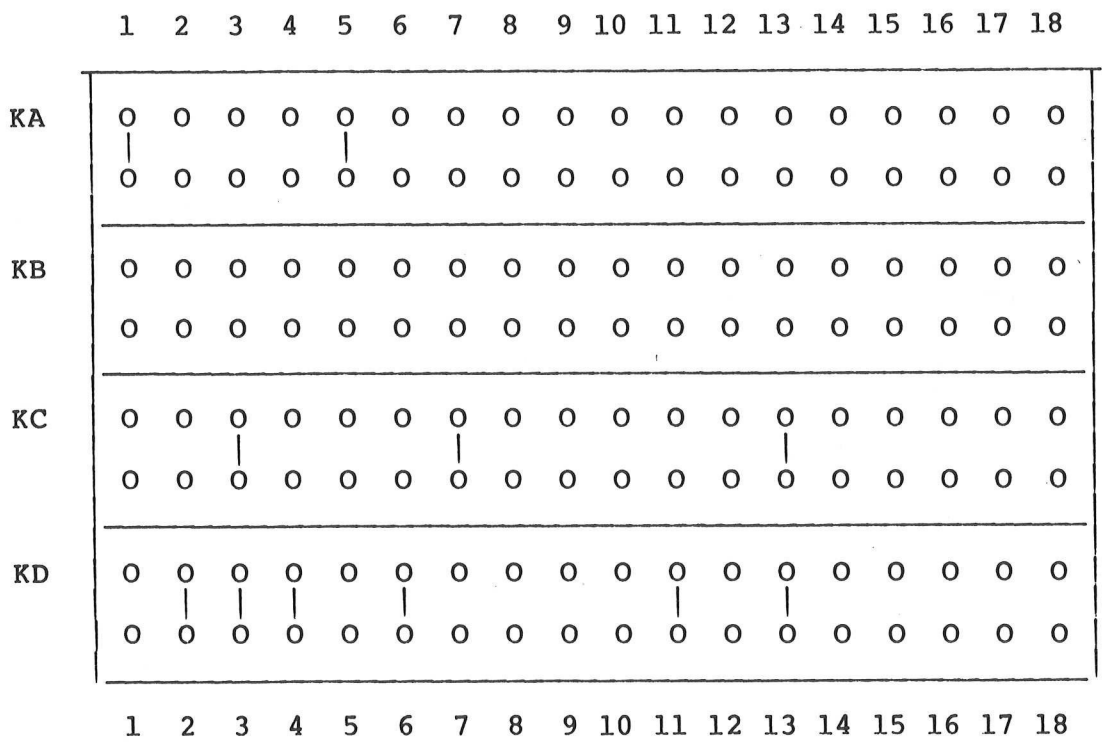
* Signal Reference Jumpers: KD2, KD6

* Unused signals on J3: RTS,RDCLK,TDCLK, all complementary(-) signals; pins 7,17,19,2,4,6,8,10,12,16,18,20.

* Ground on J3 pins 1 and 13.

* Output slew rate control provided at optional capacitors: C9, C10, C11 (typically 330pF) for long distance transmission or high noise environments.

2.6.6 Jumper Configuration for EXORset as an RS232C Terminal



	J3 PINS	SIGNALS	JUMPERS
INPUT:	15	DCD*	KC13,KD13
	9	CTS	KC7,KD4
	5	RxDATA	KC3,KD3
OUTPUT:	14	DTR	KD11
	7	RTS	KA5
	3	TxDATA	KA1

*NOTE: If modem does not supply DCD signal then add jumper KA13

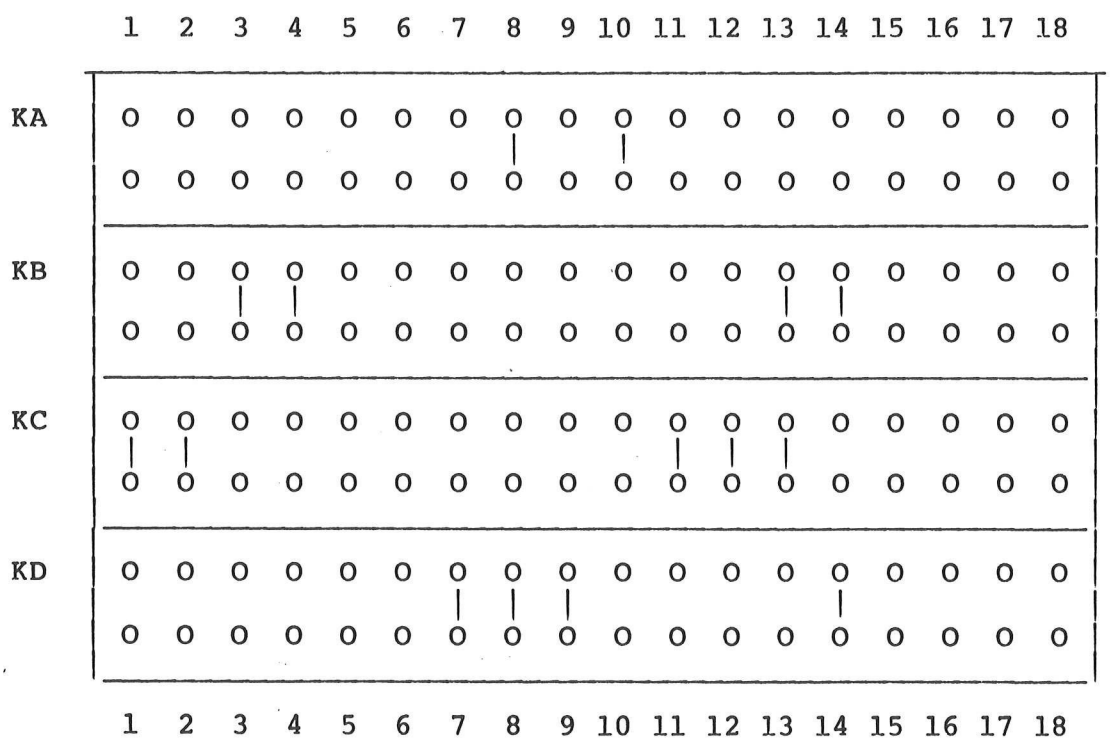
* Signal Reference Jumpers: KD2, KD6

* Unused signals on J3: DSR,RDCLK,TDCLK, all complementary(-) signals; pins 11,17,19,2,4,6,8,10,12,16,18,20.

* Ground on J3 pins 1 and 13.

* Output slew rate control provided at optional capacitors: C9, C10, C11(typically 330pF)for long distance transmission or high noise environments.

2.6.7 Jumper Configuration as an ACIA RS422 Modem/Data Set



	J3 PINS	SIGNALS	JUMPER
INPUT:	14	DTR+	KC11
	2	DTR-	KC12
	3	TxDATA+	KC1
	4	TxDATA-	KC2
OUTPUT:	15,16	DCD+,-	KB13,KB14, KC13,KD14
	11,12	DSR+,-	KD9,KA10
	9,10	CTS+,-	KD7,KA8
	5,6	RxDATA +,-	KB3,KB4

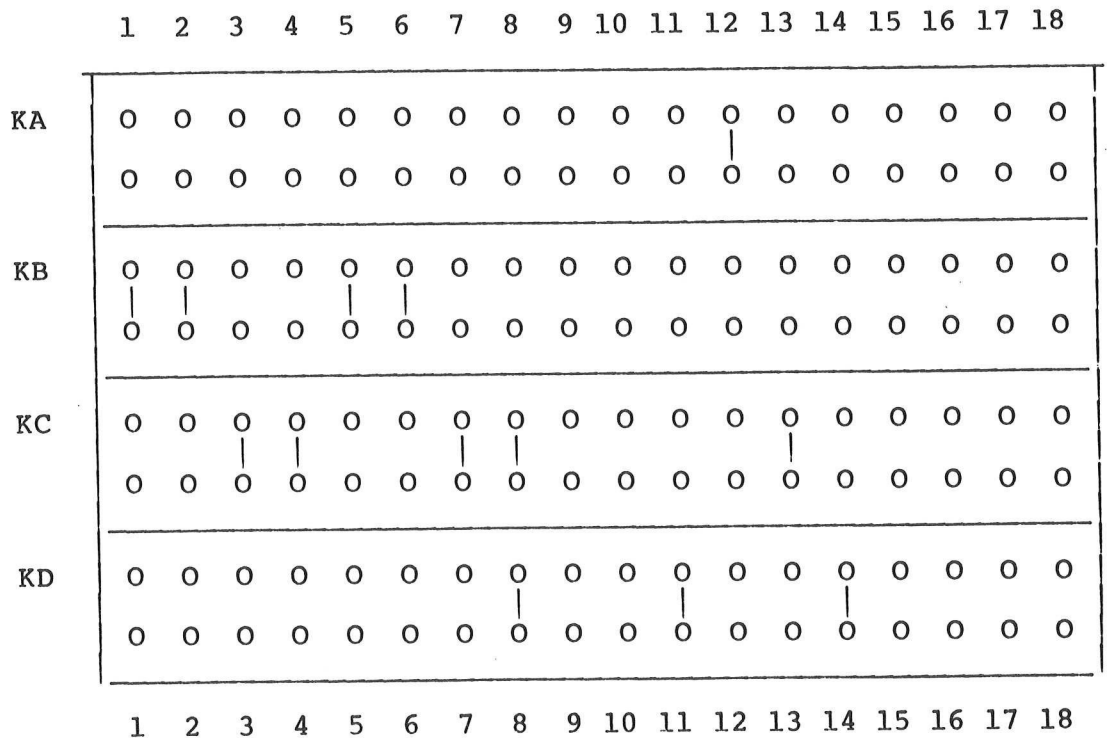
* Signal Reference Jumpers: KD8

* Unused signals on J3: RTS+,-,RDCLK+,-,TDCLK,+,-; pins 7,8,17,18,19,20.

* Ground on J3 pins 1 and 13.

* Line termination provided by optional resistors R16, R17, R18 (typically 100 ohms at 1/4 W) for long distance transmissions or high noise environments.

2.6.8 Jumper Configuration for EXORset as an ACIA RS422 Terminal



	J3 PINS	SIGNALS	JUMPER
INPUT:	15,16 9,10 5,6	DCD+,-* CTS+,- RxDATA +,-	KC13,KD14 KC7,KC8 KC3,KC4
OUTPUT:	14,2 7,8 3,4	DTR+,- RTS+,- TxDATA	KD11,KD12 KB5,KB6 KB1,KB2

*NOTE: If modem does not provide DCD signal, then add jumpers KB13, KB14.

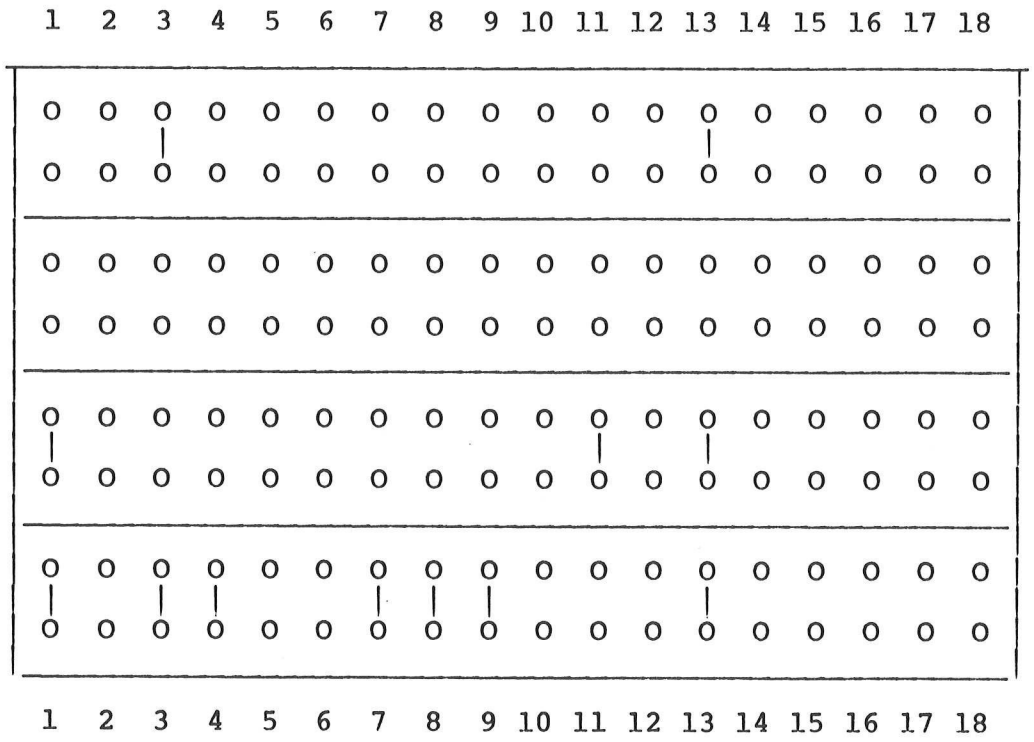
* Signal Reference Jumper: KD8

* Unused signals on J3: DSR+,- ,RDCLK+,-,TDCLK+,-; pins 11,12,17,18,19,20.

* Ground on J3 pins 1 and 13.

* Line termination provided by optional resistors R16,R17, R18 (typically 100 ohms at 1/4W) for long distance transmission or high noise environments.

2.6.9
Jumper Configuration as an ACIA RS423 Modem/Data Set



	J3 PINS	SIGNALS	JUMPER
INPUT:	14	DTR	KC11,KD4
	3	TxDATA	KC1,KD3
OUTPUT:	15	DCD	KA13,KC13, KD13
	11	DSR	KD9
	9	CTS	KD7
	5	RxDATA	KA3

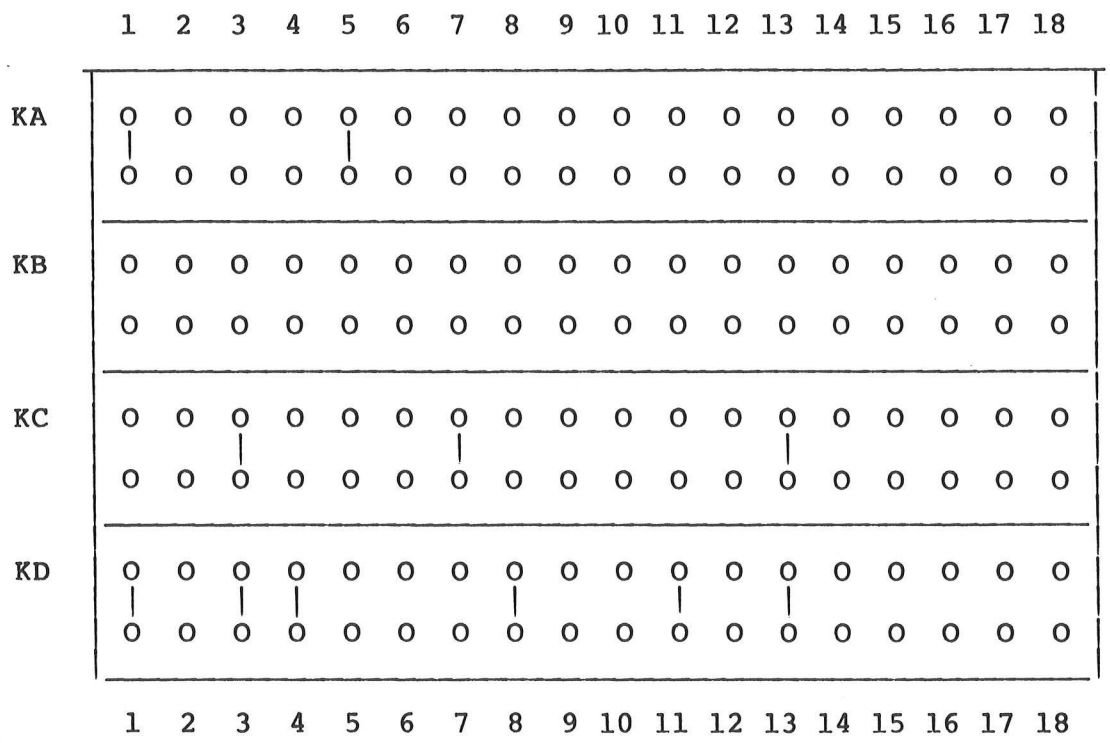
* Signal Reference Matrix Jumpers: KD8, KD1

* Unused signals on J3: RTS,RDCLK,TDCLK, all complementary(-) signals; pins 7,17,19,2,4,6,8,10,12,16,18,20.

* Ground on J3 pins 1 and 13.

* If the terminal being connected has receivers which cannot withstand +/-5vdc on their inputs (unlike MC3486), then optional resistors R11, R12, R19 (typically 2K ohms) and R10, R13, R20 (typically 3.3K ohms) should be added.

2.6.10
Jumper Configuration for EXORset as an ACIA RS423 Terminal



	J3 PINS	SIGNALS	JUMPERS
INPUT:	15	DCD*	KC13,KD13
	9	CTS	KC7,KD4
	5	RxDATA	KC3,KD3
OUTPUT:	14	DTR	KD11
	7	RTS	KA5
	3	TxDATA	KA1

*NOTE: If modem does not provide DCD signal then add jumper KA13.

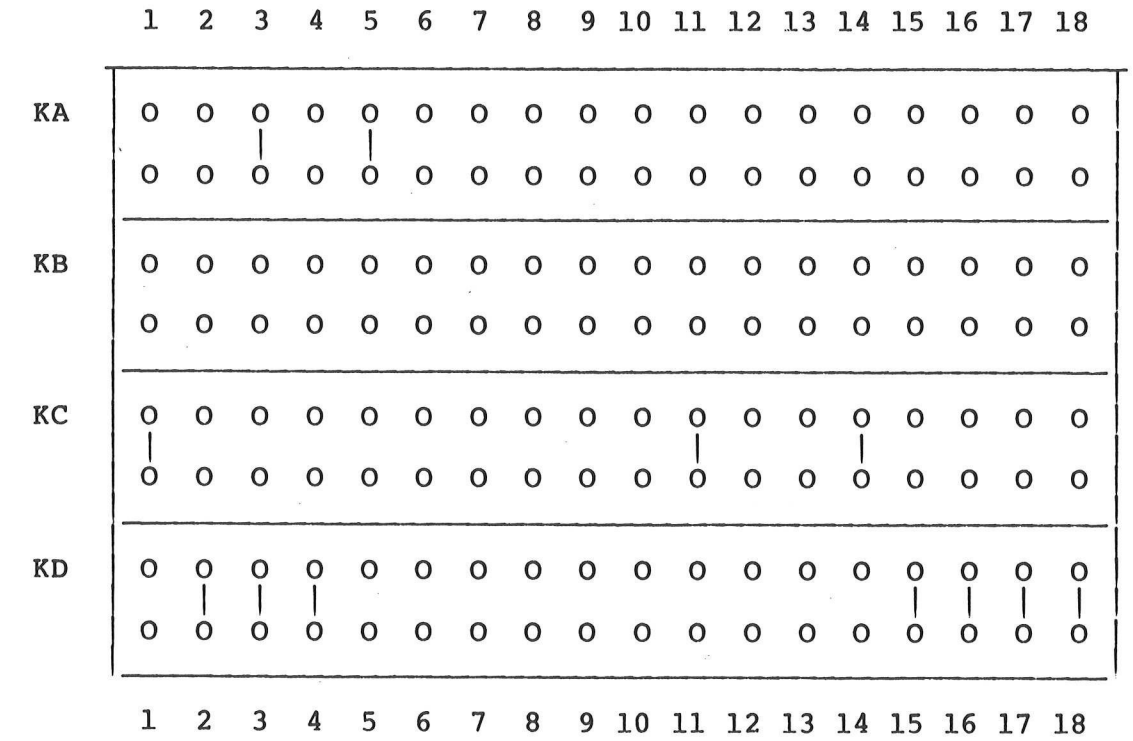
* Signal Reference Jumpers: KD8, KD1

* Unused signals on J3: DSR,RDCLK,TDCLK, all complementary(-) signals; pins 11,17,19,2,4,6,8,10,12,16,18,20.

* Ground on J3 pins 1 and 13.

* NOTE: If modem being connected has receivers which cannot withstand +/-5vdc on their inputs (unlike MC3486), then optional resistors R11, R12, R19 (typically 2K ohms) and R10, R13, R20 (typically 3.3K ohms) should be added.

2.6.11 Jumper Configuration for EXORset as an ACIA 20-mA Current Loop Modem with Micromodule 11



	J3 PINS	SIGNALS	JUMPERS
INPUT:	14	DTR	KC11,KD4
	3	TxDATA	KC1,KD3
OUTPUT:	20	+12V	KA18
	19,17	GND	KD17,KD15
	18	-12v	K16
	16	+5v	KC14
	7	Reader Control	KA5
	5	RxDATA	KA3

* Signal Reference Matrix Jumpers: KD2

* Unused signals on J3: DCD,DSR,CTS, all complementary(-) signals (except DCD, RDCLK,TDCLK; pins 9,11,15,2,4,6,8, 10,12.

* Ground on J3 pins 1 and 13.

2.7 INTERFACING MODULES ON THE EXORbus

The EXORset is provided with four EXORbus (EXORciser/Micromodule Compatible) slots which makes it possible to evaluate I/O routines for fairly complex systems, to interface a wide variety of types of external equipment or simply to expand the memory capacity with a RAM or ROM module. Three EXORbus slots are always available, one is normally occupied by the Floppy Disk Controller. For example, one or a combination of the following modules can be used:

MEX6820	Universal PIA-Controlled I/O (4 8-bit Parallel Ports, 8 Interrupt lines).
MEX6850	ACIA I/O (1 RS232C or TTY Port),110-9600 Baud
M68MM07	Quad ACIA/SSDA (4 RS232C/RS422/RS423/20mA Current Loop Ports) Selectable Baud Rate.
M68MM11	RS-232C to TTY Adapter
M68MM12	IEEE 488 GPIB Listener/Talker Controller. Includes Software.
M68MM13	Digital Interface Module
M68MM05	A/D,D/A Module
M68MM15	A/D,D/A Module
MEX6816-1HR	16K Byte Hidden Refresh RAM
M68MM04	16K ROM Expansion Module
M68MM14	Arithmetic Processing Unit

The list is not limited to this, and it is also to be noted that EXORset has a PTM, ACIA and PIA and numerous EROM sockets which can be used to emulate M68MM19 and/or M68MM04. There are two main aspects to interfacing Micromodules on the EXORset main board: the first aspect is the mechanical installation of the modules and any relevant connectors and cables. The second aspect is the address map modifications required to integrate the module into the system in a way best suited to the user's requirements. This may require reprogramming the address decoder PROMS using the optional PROM Programmer IV module M68PP4. The address map should be defined first, since, if the standard address decoding is not used the address decoder PROMs will have to be replaced and this will require access to the main board. Also the module base address should be selected by installing a jumper on the Micromodule. Some modules can be installed directly without reprogramming the standard address PROMs.

IMPORTANT NOTE: Dynamic RAM Modules without Hidden Refresh cannot be used in the EXORset. (The E Clock Signal cannot be stretched).

2.7.1 ADDRESS MAP CONSIDERATIONS

The various memory blocks and I/O devices are decoded using fusible-link PROM's. By reprogramming these PROM's, any configuration of RAM, E/ROM, I/O devices can be redefined, in 256-byte increments. The maximum available address space is 56K bytes in each map. The upper 8K address range is reserved for the system. Tables 5-1 and 5-2 in Chapter 5 show the address decode PROM contents corresponding to the EXORset standard memory map. (Refer also to Figure 5-6). Refer to sections 2.5.1.9 - 2.1.5.12 for a description OF jumper fields K12 - K16 which also affect the configuration of the memory map.
Micromodules with VUA enabling will respond in Map 2 and if they can select VXA, they will be in map 1.

As can be seen in Figure 5-6, the EXORset (with standard address decoding) has space at EC10 to EF00 for added I/O devices. example.

2.7.1.1 Address Map Example 1: M68MM12 in EXORset

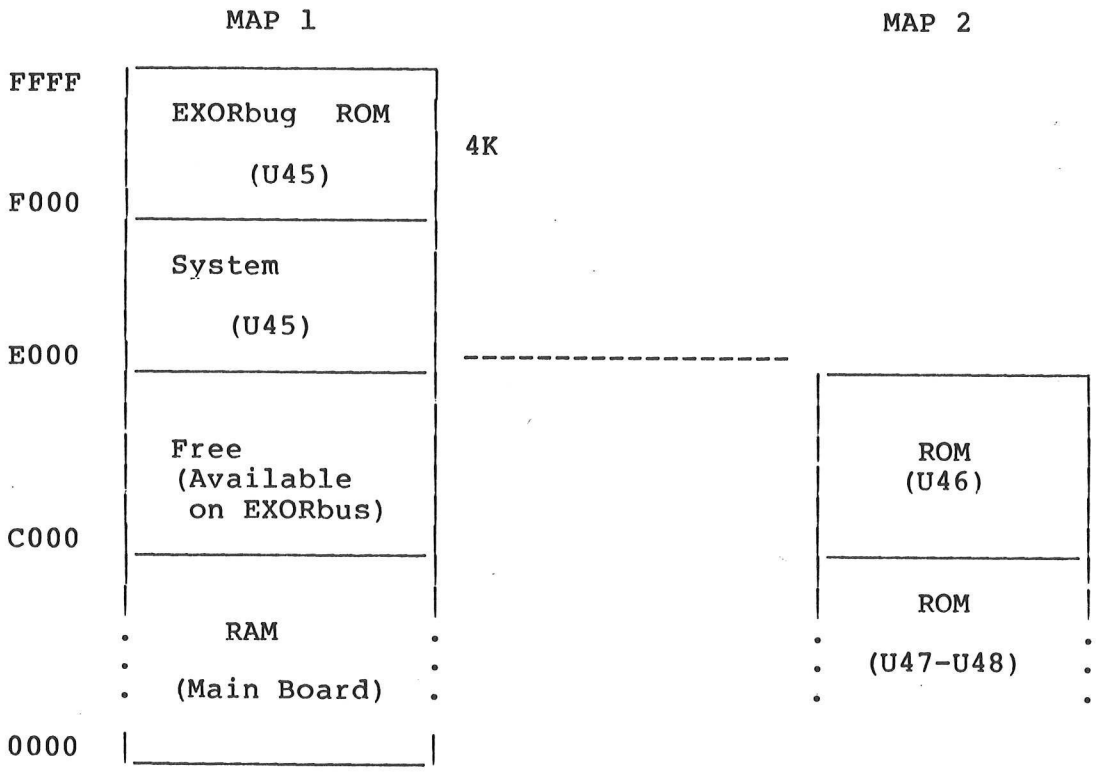


Figure 2-2 Address Map Example

In this example it has been decided to install a M68MM12 IEEE GPIB 488 bus controller in the EXORbus connector. In this

case the module is required to respond in MAP 1. As-delivered, MAP 1 is already fully occupied with physical memory devices. The wish is to locate the on board memory (ROMs) on the M68MM12 at base address C000. This requires that the upper 8K of dynamic RAM on the EXORset be disabled, this results in addresses C000 to DFFF becoming available on the EXORbus expansion connectors. (C000-C800 are required by the M68MM12).
This is achieved installing a HM7641 programmed as in Table 2-14.

Table 2-14 Address Decoder Example

	08	07	06	05	04	03	02	01	PROM ADDR	DEC ADDR	SELECTS
MAP1	1	1	1	1	1	1	0	0	1F0-1FF	F000-FFFF	
	1	1	1	1	1	1	1	0	1EF	EF00-EFFF	
	1	1	1	1	1	1	1	1	1E0-1EE	E000-EEFF	
	1	1	1	1	1	1	1	1	1C0-1DF	C000-DFFF	Free to User
	1	1	1	0	1	1	1	0	180-1BF	8000-BFFF	U12-U26 (Even)
	1	1	1	1	0	1	1	0	140-17F	4000-7FFF	U29-U43 (Odd)
	1	1	1	1	1	0	1	0	100-13F	0000-3FFF	U28-U42 (Even)
MAP2	1	1	1	1	1	1	0	0	0F0-0FF	F000-FFFF	
	1	1	1	1	1	1	1	0	0EF	EF00-EFFF	
	1	1	1	1	1	1	1	1	0E0-0EE	E000-EEFF	
	1	1	1	1	1	1	0	0	0B0-0DF	B000-DFFF	U46 (4K EPROM)
	1	1	1	0	1	1	1	0	080-0AF	8000-AFFF	U12-U26 (Even)
	1	1	1	1	0	1	1	0	040-07F	4000-7FFF	U29-U43 (Odd)
	1	1	1	1	1	0	1	0	000-03F	0000-3FFF	U28-U42 (Even)

This ROM should be installed in U51, Jumper K12 should be installed and Jumper K13 removed. The M68MM12 Base address should be configured to C000 as described in the M68MM12 User's Guide. The software running on the M68MM12 board should be origined at $C000, this requires reprogramming the EPROMs.

2.7.1.2 Address Map Example 2: M68MM07

This module is an example of integration into the address map without altering the address decoding PROMs on the EXORset Main Board. The user must assign the addresses of the I/O port to the area reserved for user-defined I/O devices in the address map. (See Figure 5-6) This is done by means of jumper options described in the M68MM07 User's Guide. For example: select $EC20 as base address, as this is compatible to the EXORset software M68SETCOMPK used to interface EXORciser and EXORset.

2.7.2 Module Installation.

Once the address map considerations have been resolved and all of the follow steps have been completed (where

necessary):

- Address Decoding Modified
- Map Jumper Options installed
- Module Base Address Jumpers
- Micromodule Firmware Re-ORGed

The module can be installed in the EXORbus connector with the component side facing the EXORset Back Panel. If cables and connectors are required this can be mounted on the back panel as described in section 2.4. (Refer to Figure 2-1) If the user uses interrupts th following should be considered: The I/O modules have provision to connect IRQ; but if FIRQ or NMI were to be required, it will be necessary to install a jumper on the module.

When using interrupts for I/O, it will be necessarv to set up a user vector table with second level interrupts, and to change the ATOP vector as described in paragraph 4.4.

When emulating certain system configurations, it may be necessary to change the interrupt connections for EXORset ACIA or PIA1. These are determined by jumpers on K4 and K6 which are normally jumpered to NMI to allow the EXORbug commands of XCOM ,DWLD and DUMP to work properly. The jumper setting can be altered to switch to either NMI,IRQ or FIRQ. IRQ or FIRQ would be used in a typical system.

NOTE

The user is cautioned to be careful about trying to solder to the gold-plated fingers of the connector, since the solder may run all over the contact unless properly done. The board should be oriented with the connector up and only a very little solder used.

CHAPTER 3

OPERATION

3.1 INTRODUCTION

Information in this chapter is intended to familiarize the user with the location and function of the EXORset controls. Directives to control the operation of the EXORset, control or modify the format of displayed data may be entered directly from the keyboard or via the serial interface. These directives are detailed in this chapter.

3.2 BACK PANEL CONTROLS

The RESET pushbutton is located on the back panel of the EXORset. The RESET switch is used to reinitialize and restart the system. The RESET signal reinitializes also the keyboard encoder microprocessor and desselects the mini-floppy drives. The RESET switch initiates a warm-start sequence. The action of the warm-start is the same as the one provided at system power-on, except that the display and the CRT controller are not initialized. If the pressing of the RESET switch does not regain proper display operation, the command "ESC-F" (see Table 3-1) must be entered to reinitialize the display.

The power on/off switch and the CRT brightness control knob are also located on the back panel (see Figure 3-1).

3.3 KEYBOARD CONTROLS

Table 3-1 lists the "ESCAPE" sequences (ESC key followed by the character corresponding to the desired command), the commands, and the special keys used to control the various modes of operation.

Table 3-1 Operation Controls

ESCAPE SEQUENCES :	
ESC-B	Background change toggle.
ESC-C	Erase from cursor position.
ESC-E	Erase screen.
ESC-F	Display format toggle : 80 characters per line by 22 lines or 40 characters per line by 16 lines
ESC-G	Bell.
ESC-H	Cursor left one column.
ESC-K	Erase line where the cursor rests.
ESC-L	Cursor home.
ESC-N	Cursor right one column.
ESC-O	Return from the terminal mode to the stand-alone mode of operation.
ESC-S	Alphanumeric mode on.
ESC-T	Alphanumeric mode off.
ESC-U	Cursor up one line.
ESC-V	Cursor down one line.
ESC-Y	Graphic mode on.
ESC-Z	Graphic mode off.
OPERATION COMMANDS :	
TMAP	Address map toggle. EXORbug monitor displays a "." when the EXORset operates in map 1, and a ":" when the EXORset operates in map 2 (see CHAPTER 5 for the map 1 / map 2 definition).
XCOM	Switch to the terminal mode of operation.

SPECIAL KEYS :	
U/C	UPPER CASE - Upper case / Lower case characters toggle.
RPT	REPEAT - This key depressed together with any other key will cause the character to be repeated at a rate of about 15 Hz.
BRK	BREAK - The BRK key is used to ABORT (exit from) a program in the stand-alone mode of operation. The control returns to EXORbug and prints the contents of the MPU registers. IF THE BREAK KEY HAS BEEN DEPRESSED ONLY ONCE, the aborted program can be re-entered by typing the EXORbug command : ;P This feature is specially important if the BREAK key has been depressed unintentionally !

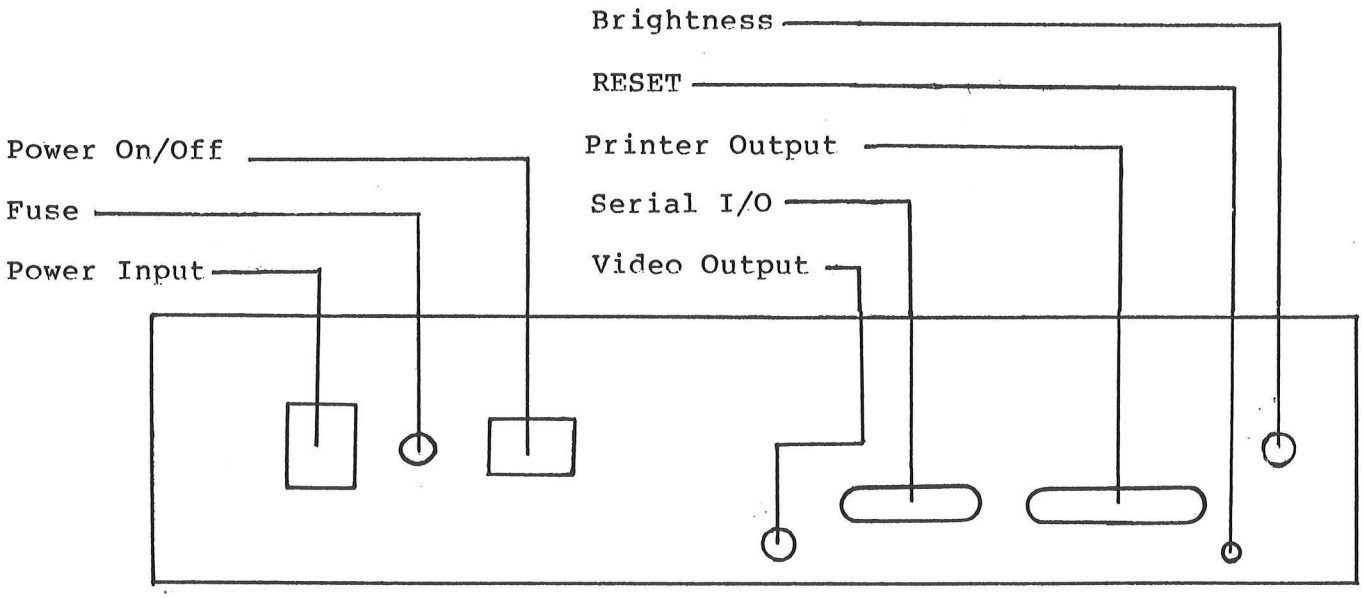


Figure 3-1 EXORset Back Panel Controls

3.4 MINI-FLOPPY DISK OPERATION

There are no front panel controls on the mini-disk drive. Proper loading of the mini-disk is vital to the operation of the mini-disk and drive. Depress the front door in the middle to open the drive. Insert the mini-disk with label toward the door. Insure that the mini-disk is fully inserted before closing the door. It is important that the mini-disk be handled and stored properly. A damaged or contaminated mini-disk can impair or prevent recovery of data and can result in damage to the read/write head. In order to assure trouble-free operation and enhance the service life of the mini-disk, the following procedure for handling should be observed :

--- Return the mini-disk to the protective jacket when not in use.

--- Store the mini-disk vertically; do not stack.

--- Avoid exposing the mini-disk to any magnetizing force in excess of 50 oersted. (Note : the 50 oersted level of magnetizing force is reached at a distance of approximately 76 mm (3 inches) from a typical source, e.g. motors, generators, transformers).

--- Do not store the mini-disk in direct sunlight; warping could result.

--- Do not use a lead pencil or ballpoint pen to write on the label; use a felt tip pen and mark lightly on the label.

--- Clean mini-floppy drives R/W head using a special cleaning diskette every 2 months.

3.5 OPERATOR TEST PROCEDURE AND SELF-TEST

The basic operation of the EXORset can be validated by an operator- monitored series of checks and tests.

3.5.1 Operation Checks

When the EXORset is powered up, and after about a 10-second, the screen should be blank, with the following message apearing in the upper left-hand corner of the screen :

```
.EXORBUG j.k
```

where j.k is the monitor version and revision number.

The display format and address map in which the EXORset initializes after the first power-on depends of the state of the jumpers SW18 (see CHAPTER 2, paragraph 2.5). With all SW18 jumpers left open (default condition), the EXORset initializes with 80 characters per line, 22 lines, upper case characters, white characters on black background, graphic mode off and address map 1.

Various characters can now be entered to check the character entry and display. Note that the EXORset is under EXORbug control, therefore no more than 19 characters can be entered on one line.

The user can now exercise all ESCAPE sequences, control commands, and special keys described in Table 3-1. Note that the ESC-O sequence can only be exercised when the EXORset is connected to a host computer via the RS-232C link.

When the graphic mode is switched on after the first power-on, the display shows the indeterminate (random) contents of the graphic memory. The graphic memory can be initialized by using the EXORbug "I" command :

```
.55;I
BEG ADDR XXXX 4000
END ADDR YYYY 7FFF
```

where 55 is the pattern to be written into the graphic memory (any other byte can also be chosen) and 4000, 7FFF are the lower and upper addresses of the graphic memory.

3.5.2 Self-Test Package

A self test package allows the user to verify system performance, detect internal failures, and aid troubleshooting.

Of course, to run the self-test routines requires some parts of the E/ROM, RAM and a good portion of the processor itself be operating properly. Furthermore, if the diskette diagnostic is to be run, the system must be able to perform basic read/write operations.

3.5.3.1 System Requirements

The diagnostic is designed to run with the following minimum requirements :

- EXORbug system monitor
- The resident disk driver firmware
  (if the diskette is to be tested)
- RAM memory at locations 0000 through 00FF.
- The self-test programm (Supplied on minidiskette 82SETUTIL)

3.5.3.2 Test descriptions

The diagnostic can be E/ROM or disk resident. In the case of E/ROM resident test program, the operator enters the program by typing the EXORbug command nnnn;G. The self-test program is position-independent, therefore nnnn corresponds to the first location of the E/ROM socket used.

If the program is disk resident, it can be loaded and executed via the XDOS command SELFTEST. If the user wants to relocate the program prior execution, the XDOS command LOAD SELFTEST.CM should be used, followed by the EXORbug "MV" (move) command. (Alternatively, the XDOS DUMP command can be used to alter the file´s RIB).

Example :

```
=LOAD SELFTEST.CM
.MV
BEG xxxx 3000
END yyyy 3FFF
DEST zzzz uuuu
.
```

where 3000 and 3FFF are the beginning and ending addresses of the SELFTEST program after loading and uuuu the destination (relocation) address. To execute the program, enter the command : uuuu;G.

In response to the prompt (*), one of seven following tests may be run :

A. Memory CRC check

This test, based upon the cyclic redundancy check, permits to read and characterize the contents of a memory range by giving a unique signature. One can determine if an E/ROM or a loaded program matches with a known good one.

In response to the prompt, the operator must issue a "C" and then enter the starting and ending addresses of the memory range he wants to test.

Example :

```
*
C> CRC CHECK

BEG 1000
END 1FFF
CRC 2D4A

*
```

B. Memory diagnostic

This test permits to identify a bad RAM location. It is divided into three different tests :

- Walking address test
- Bit pattern test
- Walking bit test

The walking address test stores the most significant 8 bits of memory address in the even addressed byte and the least significant 8 bits of memory address in the odd addressed byte. The walking address test then verifies that all addresses are stored in the proper memory locations.

The bit pattern test stores a bit pattern into each memory location and then verifies the actual memory contents. The test is performed for each of the following hex patterns: FF, AA, 55, 00.

The walking bit test first clears all memory locations. One single bit is then set and shifted throughout the memory. After each shift, the bit uniqueness is tested by reading all others bits (which should remain zero).

In response to the prompt, the operator must issue an "M" and then enter the starting and ending addresses of the memory range to be tested. If an error occurs during the test, the wrong location address, the required correct value and the actual value are displayed.

Example :

```
*
M> RAM CHECK

BEG 1000
END 1FFF

 1-WALKING ADD TEST

 2-BIT PATT TEST (FF,AA,55,00)
10F0 FF 23
10F4 AA 18

 3-WALKING BIT TEST

*
```

C. Keyboard test

This test insures that all the keys transmit the correct ASCII code.
In response to the prompt, the operator must issue a "K". The ASCII characters are displayed on the console. The operator must enter the displayed set of characters in any order. They will be deleted as soon as a match occurs.

Example :

```
*
K> KEYBOARD CHECK

TYPE :ABCDEF
```

if the operator enters D, the following will be displayed on the same line :

```
TYPE :ABC EF

*
```

D. Diskette diagnostics

There are five tests which may be run on a selective basis or continuously.

CAUTION : REMOVE XDOS DISKETTE AND INSERT SCRATCH DISKETTE(S) INTO THE DRIVE(S) BEFORE EXECUTING DESTRUCTIVE TESTS ! Note also that unless stated otherwise, only one side of the diskette is tested. (For future enhancement).

D.1 Write/Read test (destructive)

Beginning with track #0, sector #1 of the selected drive, pseudo-random data is written/read one sector at a time until all the sectors have been tested. The same process applies to the alternate drive if it is selected. If a verify error occurs, the error message E@ followed by the drive, track and sector number will be displayed.

D.2 Read for CRC (non-destructive)

Starting with track #0, sector #1 of the selected drive, all the sectors are read for CRC only. If selected, the alternate drive will then be tested. If an error occurs, the drive, track and sector numbers are displayed.

D.3 Worse case track/sector access (non-destructive)

This test is used to insure track position reliability under worse case application. Beginning at track #0 sector #1, 10 sectors are read for CRC. Then the last 10 sectors of the last track are read for CRC. This process is repeated for

the next 10 sectors in both directions, until all the sectors have been tested. The alternate drive is then checked if it was selected.
10 sectors are read to insure track overflow. Any error will be displayed as drive, track and sector number .

D.4 Worse case data pattern (destructive)

Beginning with track #0, sector #1 of the first selected drive, all the sectors are written with a worse case bit pattern (4DB2). They are then read back to check their CRC. This is then repeated for the alternate drive if it was selected. Any error will be displayed as drive, track and sector number .

D.5 Sector/drive uniqueness (destructive)

Each contiguous sector is written with its own sector and drive unit number. The head is restored and each sector is read to insure uniqueness. The read partial sector is used to read 8 bytes only. If a uniqueness error occurs, it will display an EA followed by drive, track and sector number. If more than 8 bytes are read, the error code will be EB.

In response to the prompt, the operator issues a "D". The five possible tests are displayed, numbered from 1 to 5. The operator should first select the drive to be tested (0, 1 or Both). The operator must then answer the question "Do you want to run all the tests ?" with a Y or N. A "Y" answer will run all the tests, one after each other, continuously looping until the break key is depressed. An "N" answer permits the operator to choose a specific test by entering the corresponding test number. After its completion, another test may be chosen or control may be returned to another EXORset test.

Example :

```
*
D> DISK CHECK

 1-W/R TEST (DEST)
 2-READ FOR CRC (NON-DEST)
 3-WST CASE TK/ST ACCESS (NON-DEST)
 4-WST CASE DATA PATTERN (DEST)
 5-SCT DRIVE UNIQUENESS (DEST)

WHICH DRIVE (0,1,B) ? 0
ALL THE TESTS (Y/N) ? N

TEST # 1-W/R TEST (DEST)

ANOTHER TEST (Y/N) ? N

*
```

E. ACIA diagnostic

This diagnostic permits to check the send and receive functions of the ACIA. The only requirement is to connect the send and receive line together. The full ASCII character set is sent. After a character is sent, a check is done to verify that this character was correctly transmitted and received. If an error occurs, a message such as "TX-TIMEOUT", "RX-TIMEOUT", or the required correct character and the actual character are displayed.

To run the test, the operator must issue an "A" in response to the prompt.

Example :

```
*
A> ACIA CHECK

TX-TIMEOUT  if a transmit timeout occurs
RX-TIMEOUT  if a receive timeout occurs
3E 3D       if sent and received data do not match

*
```

F. CRT diagnostic

This diagnostic is a visual check of the alphanumeric, graphic, character generation, cursor positioning, background change, and 40 to 80 character toggle functions.
To run the test, the operator must issue a "V" in response to the prompt.Then the following sequence will be executed :

--- A draughtboard-like pattern must fill the screen for about 5 seconds (´graphic on´ test).

--- A set of ´#´ characters must then be superimposed for about the same time (´graphic & alphanumeric on´ test).

--- The draughtboard-like pattern must disappear leaving the ´#´ pattern displayed alone for about 5 seconds (´alphanumeric on´ test).

--- The screen will be erased and the full printable ASCII character set must be displayed, the same character filling a full line. The ASCII character set will then be displayed with 40 characters per line and the background changed (80 to 40 characters toggle, character generator, background change test).

--- Next, the cursor moves around the screen, the first time 80 columns horizontal and 22 lines vertical and next 40 columns horizontal and 16 lines vertical. The cursor should not blink during this test (cursor test).

At the end of the CRT check the prompt is issued and the cursor must blink again.

G. BURN-IN test

This test performs memory and diskette tests continuously until the break key is depressed.
The errors, if any, are accumulated and displayed on the CRT along with the test being currently executed and the pass number. Both drives are tested, starting with drive 1. The memory diagnostic is performed by default from the end of the test program to $BFFF if the test program was loaded from a diskette and from $100 to $BFFF if the test program resides on E/ROM. The default starting and / or ending addresses may be altered by the user if necessary.

CAUTION : INSERT A SCRATCH DISKETTE IN EACH DRIVE BEFORE EXECUTING THE TEST.

To run the burn-in test, the operator must enter a "B" in response to the prompt. The default RAM test starting and ending addresses are displayed. The operator enters a RETURN if the default address is to be used, or the desired new value followed by RETURN if he wants to alter the default value(s). The following will then be displayed (example) :

```
B> BURN-IN CHECK                                       PASS # 0011


                          DISK    ERRORS
                          --------------

E1    E2    E3    E4    E5    E6    E7    E8    E9    E@    EA    EB

0004                    0024                          0006        014F


                          MEMORY  ERRORS
                          --------------
                               02BC


1-W/R TEST [DEST]
_
```

Disk error messages description :

E1 through E9 : see Table 5-15.
EA, EB, and E@ : see paragraph D.1 and D.5 above.

CHAPTER 4

EXORbug MONITOR

Information in this chapter is intended to familiarize the user of the EXORset with the various functions offered by the EXORbug monitor program. It provides detailed description of the commands, subroutines and entry points that are available to perform system development, evaluation and debugging.

4.1 EXORbug COMMANDS

In addition to the EXbug 2 compatible commands, the EXORbug monitor offers a new set of functions that greatly extend program development and debugging capability of the EXORset over existing systems.

There are five groups of commands :

1. Four-character commands followed by a carriage return
2. Two-character commands followed by a carriage return
3. Single character commands following a semicolon or dollar sign
4. Memory change commands
5. Control commands

The four-character commands allow a program to exchange programs with an EXORciser, invoke the disk operating system, display memory blocks, select the memory map, and switch to terminal mode. The user may add four-character commands to the standard set.

Two-character and single character commands control program debug functions, allow to move memory blocks within the EXORset memory and to insert ASCII character strings.

Memory change commands allow memory locations to be examined and changed.

Control commands are used to switch the EXORset from terminal to local mode (on-line/off-line) , erase the display, control cursor movements, to control the alphanumeric and graphic displays, select the display format (80/40 characters per line) and to abort or suspend command execution. A summary of EXORbug commands is found in Table 4-1.

Any command may be entered while EXORbug is displaying one of its prompts (. or :). The two prompts are used to indicate to the user which is the currently selected memory

map. A "." indicates first map, while a ":" indicates second map.

EXORbug accepts both upper and lower case characters. All values entered are assumed to be hexadecimal. If an invalid command or a non-hexadecimal value is entered, EXORbug responds by displaying WHAT ?, ringing the bell, and then issuing another prompt.

Control-X can be used at any time (at command level) to delete the current entry and cause another prompt to be displayed.

When entering hexadecimal values, only the last four digits are taken into account. If less than four digits are entered, leading zeroes are assumed.

Table 4-1 EXORbug Commands

COMMAND	FUNCTION	PAGE
PRNT	Display memory block in HEX & ASCII	04-04
DUMP	Dump memory block to EXORciser memory	04-05
DWLD	Download an EXORciser memory block	04-05
LINK	Download an EXORciser disk file	04-06
XDOS	Invoke the disk operating system	04-09
TMAP	Toggle memory map	04-09
XCOM	Switch to terminal mode	04-09
RA	Display/change target A accumulator	04-10
RB	" " B accumulator	04-10
RC	" " C register	04-10
RD	" " D register (A,B accumulator pair).	04-10
RP	Display/change target Direct Page register.	04-11 04-11
RL	Display/change target Location counter (program counter).	04-11
RS	Display/change target Hardware Stack pointer.	04-11
RU	" " User stack pointer	04-11
RX	" " X index register	04-11
RY	" " Y index register	04-11
RR	Display all registers	04-10
SM	Select memory location for display trace function and breakpoints.	04-11
SP	Select display speed	04-13
MV	Move memory block	04-13
IS	Insert ASCII string to memory	04-13
EV	Extend breakpoints to WRITE condition	04-12
TC	Enable track change of memory location	04-12
DT	Disable track change of memory location	04-12
nnnn;G	Go to the target program at the specified address.	04-18
;G	Go to the target program through the	04-17

	user RESTART vector.	
nn;I	Initialize memory block with the specified bit pattern.	04-21
;M or $M	Specify the memory search address range and mask.	04-20
nnnn;N	Trace nnnn instructions	04-19
;N	Trace one instruction	04-19
;P	Proceed with program execution	04-19
nnnn;P	Same as ;P but skip nnnn breakpoints	04-19
$T	Enable trace to ending address function	04-16
;T	Disable trace to ending address function	04-17
nnnn;V	Set breakpoint at address nnnn	04-14
;V or $V	Display breakpoints	04-16
nnnn;U	Remove breakpoint at address nnnn	04-16
;U	Remove all breakpoints	04-16
nnnn;W	Search memory for nnnn (1 or 2 bytes)	04-20
;Z	Line printer ON/OFF	04-21
nnnn/	Open location nnnn for memory change function and display contents.	04-22
followed by :		
[nn]LF	Open next memory location, display address & contents on next line.	04-22
[nn]SPACE	Open next memory location, display contents on same line.	04-22
[nn]COMMA	Open next memory location, no display	04-22
[nn]UA	Open previous memory location, display address & contents on next line.	04-23
[nn]SLASH	Reopen current memory location, display address & contents on next line.	04-23
'CHARACTER	Insert one ASCII character	04-22
nnnn;O	Calculate short relative offset to nnnn	04-23
nnnn;L	Calculate long relative offset to nnnn	04-23
[nn]CR	Terminate memory change function	04-22
CTRL-W	Suspend command execution	04-02
CTRL-X	Abort current command or entry	04-02
ESC-B	Display background change	04-25
ESC-C	Clear display from cursor	04-25
ESC-E	Erase screen	04-25
ESC-F	Display format toggle (40/80 characters)	04-24
ESC-G	Sound bell	04-25
ESC-H	Cursor to previous location	04-24
ESC-K	Kill line from cursor	04-25
ESC-L	Cursor home	04-25
ESC-N	Cursor to next location	04-25
ESC-O	Return to stand-alone mode of operation	04-25
ESC-S	Alphanumeric display ON	04-24
ESC-T	Alphanumeric display OFF	04-24
ESC-U	Cursor up one line	04-25
ESC-V	Cursor down one line	04-25
ESC-Y	Graphic display ON	04-24
ESC-Z	Graphic display OFF	04-24

Note : Brackets indicate optional entries

4.1.1 Four-Character Commands

The four-character commands are activated by entering the appropriate four characters followed by a carriage return (CR) on the system keyboard. The four-character commands are described as follows .

PRNT This command displays the specified portion of memory in both hexadecimal and ASCII form.

After the user has entered PRNT followed by a CR, EXORbug responds by displaying BEG nnnn. nnnn is the last beginning address entered. Note that nnnn is initialized to 0000 on system turn-on. If the displayed beginning address is correct, the user should enter a CR. To change the beginning address, the user has to enter the new address followed by a CR. (The command can be aborted at any time by entering a Control-X).

If an incorrect address is entered, the correct address may be entered directly on the same line before the CR is entered. Up to 19 hexadecimal characters can be entered before the CR. Only the last four characters will be used as the address.

If less than four hexadecimal characters have been entered, the unspecified most significant digits are assumed to be zero. For example, entering E CR gives an address of $000E.

After the beginning address has been successfully entered, EXORbug displays END nnnn (where nnnn is the current ending address). Here the user has the same options for entering an ending address as described for the beginning address.

If the entered ending address is less than the beginning address, EXORbug will request the beginning and ending address again. If the ending address is greater than or equal to the beginning addresses, EXORbug will display the requested portion of memory.

The display format depends on whether the EXORset is operating in 40 or 80 characters per line mode.

In 80 characters/line mode, the display format is the one shown in Figure 4-1. Every ten lines,a byte position header, showing the address of every byte within a line is displayed for better visualisation. In 40 characters/line mode, every line generated by PRNT is truncated and appears on two consecutive display lines. In addition, no byte position header is generated.

While memory is being displayed, entering Control-W will cause the display to be suspended at the end of the current line until another character is entered. Entering Control-X will abort the PRNT command at the end of the current line.

```
.PRNT
BEG 0000 1000
END 0000 1050
     00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
1000 7E F2 AE 7E F0 45 7E F0 6F 7E F0 D5 7E F0 D9 7E  ~r.~pE~po~pU~pY~
1010 F0 88 7E F1 18 7E F2 2A 7E F0 B3 7E F0 AF 7E F0  p.~q.~r*~p3~p/~p
1020 AD 7E F0 3A 7E F0 2D 7E F0 2F 7E F0 B1 8D F2 A6  -~p:~p-~p/~p1.r&
1030 00 81 04 27 37 8D E1 08 20 F5 86 0D 8D DA 86 0A  ...'7.a. u...Z..
1040 8D D6 4F 20 D3 CE FB 99 8D E3 CE FF 0A BD F6 04  .VO SN{..cN..=v.
1050 25 F3 CE FB 9E 8D D6 CE FF 0C BD F6 04 25 F3 CE  %sN{..VN..=v.%sN
.
```

Figure 4-1 PRNT Example

DUMP The DUMP command transfers a memory block to the memory of an EXORciser attached to the RS-232 serial interface on connector J3.

The transmission format used by the DUMP command is the same as the EXbug PNCH command and is compatible with the EXORciser LOAD command.

Before entering the DUMP command, the user must insure that the EXORciser is in the main EXbug control loop and that the RS-232 interface is set-up for 2400 BAUD operation. If these conditions are not met, EXORbug is unable to transfer data to the EXORciser.

The procedure for the DUMP command is exactly the same as the one described for the PNCH command.

DWLD The DWLD command downloads an EXORciser memory-resident program to the EXORset memory.

The transfer is made via RS-232 serial interface (connector J3). As for the DUMP command, the EXORciser must be under EXbug control and the RS-232 interface operating at 2400 BAUD.

After entering the DWLD command, EXORbug sends automatically the PNCH command to the EXORciser. The EXORciser will then request the beginning and ending addresses, and the header information through the EXORset display and keyboard (the

EXORset operating as terminal). For detailed procedure description refer to the corresponding EXORciser User´s Guide.

Note that if the user makes an error causing the EXORciser to abort the PNCH command and issue its prompt (*), the PNCH command has to be reinitialized manually.

Once the beginning and ending addresses, and the header information have been entered successfully, the EXORciser starts its punch sequence and the EXORset starts automatically to load the transferred data. During data transfer, EXORbug checks for checksum errors and memory errors as described for the LOAD command. Once the data transfer is completed, EXORbug issues a prompt.

Note that when using an EXORciser equiped with an EXbug 2, the user must enter DWLD followed by two (2) carriage returns. Note also that EXbug 1.2 will not return automatically to its main control loop after a DWLD operation is performed.

LINK The LINK command allows an EXORciser disk file to be loaded into the EXORset memory. The EXORset must be correctly connected to the EXORciser via the parallel link described in Figure 4.3, that must be implemented at address $ED00. After entering the LINK command followed by a CR, the user must initiate the data transfer on the EXORciser using the MDOS COPY command as described in Figure 4-2.

```
EXBUG 1.2 MAID
*E800;G
MDOS 03.00
=COPY FILE.SF:DV,#UD;D=LINK
```

Figure 4-2 LINK Example

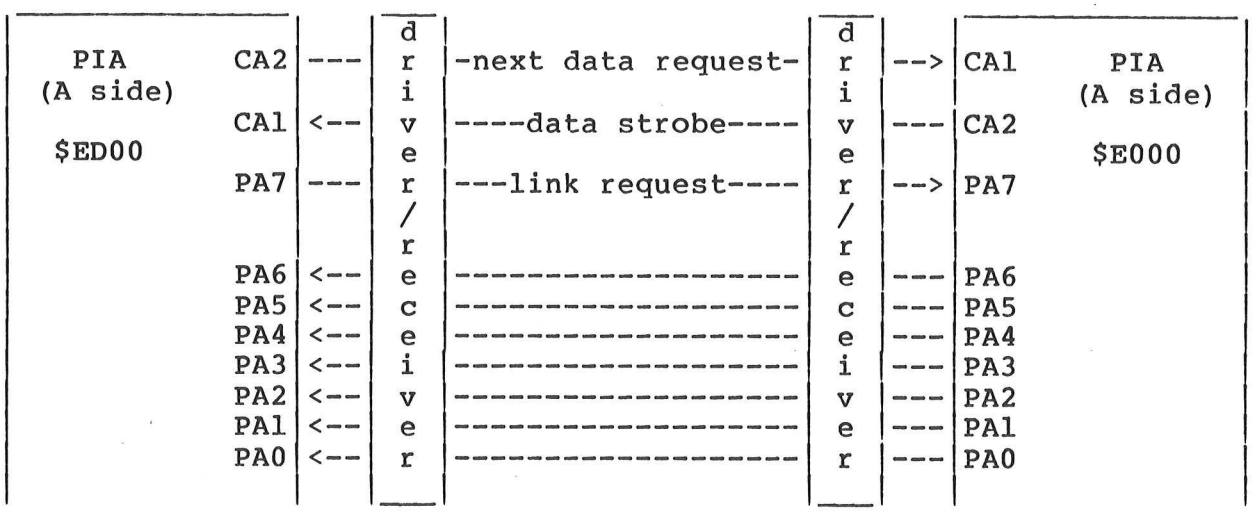
FILE is the name of the file to be transferred. SF is its suffix and DV is its logical drive number.

The program LINK is used to perform the transfer on the EXORciser side of the link, and must reside in a file called LINK. The program LINK is listed below.

```
 OPT LIST
 NAM LINK
 TTL DUMP MDOS FILE TO THE EXORSET MEMORY
 OPT LLEN=120
 SPC 1
* THIS PROGRAM DUMPS A DISKETTE FILE TO THE EXORSET
* VIA A PIA LOCATED AT BASE ADDRESS $E000
 SPC 1
* INTERFACE SIGNALS :
```

```
 SPC 1
* PA0-PA6 : 7-BIT BYTE TO SEND OUT
* PA7     : EXORSET REQUEST (ACTIVE HIGH)
* CA2     : STROBE TO EXORSET (POSITIVE PULSE)
* CA1     : "NEXT" REQUEST FROM EXORSET (NEG TRANSITION)
 SPC 3
 ORG $3000
 SPC 2
* CONTROL DESCRIPTOR BLOCK
*
EX$CDB FDB 0 IOCB ADDRESS
 FDB EX$DRV SOFTWARE DRIVER ADDRESS
EX.PIA FDB $E000 PIA BASE ADDRESS
 FCB DD$RES+DD$OUT+DD$FMC
 FCB VD$NFF
EX.SVX FDB 0 TEMPORARY
EX.TMO FDB 0 TEMPORARY
 SPC 2
EX$DRV EQU *
 SPC 1
 CLC TURN DEVICE ON
 BRA RETURN
 SPC 1
 CLC
 BRA RETURN TURN DEVICE OFF
 SPC 1
 JSR INITR DEVICE INIT
 SPC 1
 CLC
 BRA RETURN DEVICE TERMINATION
 SPC 1
 BSR PUTCH OUTPUT BYTE TO EXORSET
 BCC RETURN
 SPC 1
DNRDY LDAA #I$NRDY DEVICE NOT READY: SET ERROR STATUS
 TSX EXORSET NOT READY OR TIMEOUT
 LDX ,X GET ADDR OF FDB FOLLOWING JSR
 LDX ,X GET CONTENTS OF FDB
 LDX ,X GET ADDRESS OF IOCB
 SPC 1
 STA A IOCSTA,X
*
RETURN TSX RETURN TO CALLER
 LDX ,X GET ADDRESS OF FDB FOLLOWING JSR
 INS ADJUST STACK FOR RETURN
 INS
 JMP 2,X JUMP TO ADDRESS FOLLOWING FDB
 SPC 1
*
INITR LDX EX.PIA
 CLR 1,X RESET CTRL REG
 LDA A #$7F ALL LINES OUTPUTS EXCEPT PA7
 STA A ,X
 LDA A #$34 INIT CTRL
 STA A 1,X
 LDAA 0,X DEVICE READY ?
 BMI DRDY YES, OK
 INS NO, GO OUTPUT ERROR MESSAGE
 INS
 SEC
```

```
 BRA DNRDY
DRDY RTS
 SPC 2
* OUTPUT ONE BYTE
 SPC 1
PUTCH LDX EX.PIA
 CMPB #$D CARRIAGE RETURN ?
 BEQ CONT YES, ACCEPT
 CMPB #$20 CONTROL CHARACTER ?
 BHI CONT NO, GO OUTPUT
 CLC IGNORE CONTROL CHARACTERS
 RTS
CONT PSHB SAVE CHARACTER
 CLR EX.TMO INITIALIZE TIME OUT
 CLR EX.TMO+1
 LDAB 1,X FETCH EVENTUAL EXORSET BYTE REQUEST
 LDA A ,X IS PA7 HIGH ?
 BMI WAITN EXORSET LOAD STILL ACTIVE, GO WAIT BYTE REQUEST
TMER PULB DROP CHARACTER
 SEC ERROR, EXORSET INACTIVE, DEVICE NOT READY
 BRA PUTC4
 SPC 1
WAITN1 LDAB 1,X
 DEC EX.TMO+1
 BNE WAITN
 DEC EX.TMO
 BEQ TMER TIME OUT, GO SET ERROR FLAG
WAITN TSTB WAIT EXORSET REQUEST
 BPL WAITN1
 PULB RETRIEVE CHARACTER
 STA B ,X SEND BYTE
 LDA A #$3C STROBE DATA
 STA A 1,X
 LDA A #$34
 STA A 1,X
 SPC 1
FINE CLC
 SPC 1
PUTC4 LDA A ,X RESET FLAG
 LDX EX.SVX
 RTS
 END
```



Note : Line drivers/receivers are optional

Figure 4.3 Link Parallel Interface

XDOS The XDOS command is used to envoke the disk operating system.

The control is first transferred to the diskette controller which will initialize the drive electronics and then proceed to read the bootblock into memory. Once the bootblock is loaded, control is transferred to it. The bootblock will then attempt to load into memory the remainder of the resident operating system. If no error is detected (see the XDOS User's Guide for a description of error messages), XDOS will display a sign-on message and is ready for use.

TMAP This command allows to switch from one set of address decoding pattern to the other in the system address decoding PROMs.
The function of these PROMs as well as the available addressing maps are described in paragraph 5.2.4 of this manual. Note that with the original EXORset address decoding PROMs, the two memory pages in which the EXORbug monitor and its peripherals reside ($E000 through $FFFF) are not affected by the TMAP command.

XCOM The XCOM command switches the EXORset in the terminal mode of operation.

4.1.2 Two-Character Commands

The two-character commands are activated by entering the appropriate two characters followed by a CR. Two-character commands fall into three groups : register display and change, breakpoint control, and miscellaneous functions.

4.1.2.1 Register Display and Change

These commands allow the user to display and change the M6809 register values that are used while executing the program under test. There is one command that displays all the register values, while individual commands are used to display and change each register. In addition there is a command to select a memory location for display along with the microprocessor registers during breakpoints or trace operations.

RR This command displays all target registers as shown in Figure 4-4.

The mnemonics L, S, U, Y, X, DP, B, A, and C designate the location (program) counter, hardware stack pointer, user stack pointer, Y index register , X index register, direct page register, B accumulator, A accumulator, and condition code register, respectively.

RA This command displays the target A accumulator value (nn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RB This command displays the target B accumulator value (nn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RC This command displays the target condition code register value (nn) . The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RD This command displays the target D register (A,B accumulator pair) value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RL This command displays the target location counter value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RP This command displays the target direct page register value (nn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RS This command displays the target hardware stack pointer value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RU This command displays the target user stack pointer value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RX This command displays the target X index register value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

RY This command displays the target Y index register value (nnnn). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

SM This command allows the user to select a single memory location for display along with the MPU registers during a breakpoint or trace operation.

After the user has entered the SM command, EXORbug displays the address of the memory location being currently selected for display. The default value is 0000. When the address is set to 0000, no memory location is selected. The memory location 0000 can therefore never be selected for display. The user may keep the address unchanged by entering a CR, or enter a new address followed by a CR. An example of SM command utilisation is shown in Figure 4-4.

4.1.2.2 Breakpoint Control

Set, remove and display breakpoints, are functions that are performed by single-character commands (see paragraph 4.1.3). The two-character commands allow the user to extend existing breakpoints to the WRITE condition, to track the

changes of one user defined memory location, and to disable the track change function.

EV This command allows all existing breakpoints to be extended to the WRITE condition. This means that a given breakpoint is active when, and only when, the MC6809 writes data at the corresponding address. This is the case during execution of instructions such as a STA nnnn, where nnnn is a breakpoint address.

On entering the EV command, EXORbug will display "Y/N ?" and wait for a user input. If a Y is entered the extended breakpoint function is enabled. If a N is entered, it is disabled.

TC This command enables the track change-of-memory-location function and to specify the address on which it should operate.

After the user has entered the TC command, EXORbug will display the last memory address that had been entered in a previous TC command (0000 if TC is called for the first time). If the displayed address is correct, the user enters a CR, otherwise it can be modified by entering a new value followed by a CR.

During execution of the target program, whenever the MC6809 references the selected memory location AND modifies its contents, EXORbug will display :

CELL nnnn JUST CHANGED TO mm

where nnnn is the selected memory address and mm is the new contents. The complete microprocessor status, after execution of the instruction that modified the selected memory location, will be displayed on the next line. Execution of the target program will be stopped and a prompt issued to allow the user to enter commands.

As long as the track change-of-memory-location function is enabled, eventual breakpoints are disabled.

During a trace sequence (be it a trace nnnn instructions or a trace to end address), the track change-of-memory-location is disabled.

DT The DT command disables the track change-of-memory-location function. Breakpoints that had eventually been set prior to the TC command, are enabled again. Note that if the TC command had been enabled at the same address than an existing breakpoint, the corresponding breakpoint will be removed by the DT command as it

would be removed by selecting a new address by a another TC command.

4.1.2.3 Miscellaneous Commands

These commands select display speed, move a memory block within the EXORset memory, insert ASCII character strings into memory.

SP This command displays the current delay value used for displaying characters on system CRT. The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR.

The delay value is initialized at system turn-on to 0000 (maximum speed), which corresponds approximately to 600 characters/second. A value of, for example, 300 will slow down the display to about 120 characters/second.

MV This command moves the content of the specified memory block to the specified destination.

After the user has entered the MV command, EXORbug requests beginning and ending addresses as described for the PRNT command. Once the beginning and ending addresses have been entered successfully, EXORbug will request the destination address by displaying DEST nnnn, where nnnn is the last destination address entered (initialized to 0000 at system turn-on). The value may be left unchanged by entering a CR, or modified by entering a new value followed by a CR. The destination address cannot be in the beginning-ending address range. If this should be the case, EXORbug requests new beginning, ending, and destination addresses.

If an overlapping move has to be performed, the user should proceed in two steps : first move the memory block to some safe area, and then, move this area to the final destination. This procedure is mandatory to prevent data of being overwritten by the move before being moved.

As data is being moved, EXORbug checks that memory changes correctly. If an attempt is made to move data to a non-RAM or defective RAM area, EXORbug will display "NO CHNG" and abort the command.

IS This command allows ASCII character strings to be inserted directly from the system keyboard to the specified memory area.

After entering the IS command, EXORbug will request the beginning address at which the string should be inserted. The displayed address can be left unchanged by entering a CR, or modified by entering a new address followed by a CR.

All characters following the CR will be inserted in contiguous memory locations starting at the specified beginning address, until a Control-D (EOT) is entered. The EOT character (04) is the last one to be inserted. As every character is inserted into memory, EXORbug checks if memory changes correctly. If a memory location does not change properly, EXORbug will display "NO CHNG" and abort the command.

The ASCII character string that has been inserted using the IS command, being terminated by EOT, is ready to be displayed by the XPDATA or XPDAT1 subroutines (see paragraph 4.3).

4.1.3 Single-Character Commands

The single-character commands control debug functions. These commands are always preceded by a semicolon (;) or a dollar sign ($). Single-character commands fall into various groups : program execution control, program execution, memory search, and miscellaneous functions.

4.1.3.1 Program Execution Control

These commands control the execution of the target program. They allow the user to set, display, and remove breakpoints; enable or disable the Trace to Ending address mode.

Set a breakpoint

FORMAT : addr;V

This command permits the user to specify a breakpoint. A maximum of 4096 breakpoints can be entered. All breakpoints must reside in the same 4K memory page.

The hardware breakpoints concept of the EXORset, allows breakpoints to be set in RAM or ROM and on any byte of an instruction (even on a memory location referenced by an instruction).

During execution of the target program, the

breakpoints are activated. When a breakpoint is encountered, execution of the program is halted to permit visual check, or other performance analysis of the processor's program registers. The breakpoint sequence is :

- The user designates the breakpoint locations using the addr;V command. Since the breakpoints use interrupts (NMI), they should only be applied in portions of the target program where the stack pointer is pointing to a valid stack area. Should a breakpoint be encountered with the stack pointer (SP) pointing to a non-valid area, EXORbug will display the "BAD SP" message.

- The user initiates the target program execution through the use of the program execution commands (;G, addr;G, ;P, or nnnn;P). Note that breakpoints are not enabled during trace operations.

- When a breakpoint is encountered, control is returned to EXORbug and the processor registers as well as the optional memory location selected by the SM command are displayed as shown in Figure 4-4.

```
.100/00 86,33,B7,2,0,4C,20,102;O FA
 0107  00 FA
.SM 0000 200
.102;V
.RR
L-0000 S-E6FF U-0000 Y-0000 X-0000 DP-00 B-00 A-00 C-D0
.100;G
L-0105 S-E6FF U-0000 Y-0000 X-0000 DP-00 B-00 A-33 C-D0 M-33
.2;P
L-0105 S-E6FF U-0000 Y-0000 X-0000 DP-00 B-00 A-35 C-D0 M-35
.
```

Figure 4-4 Breakpoint Example

NOTE

- When an abort occurs, the breakpoints are NOT removed. During a restart sequence, all breakpoints are removed.

- When a breakpoint is encountered, the processor normally returns control to EXORbug after execution of the instruction on which a breakpoint is set. However, if a breakpoint is set on the

first byte of an instruction preceded by an instruction that uses the look-ahead feature of the MC6809 (like most single byte instructions), control will be returned to EXORbug before execution of the instruction on which the breakpoint is set. The displayed location counter value should be checked to determine where user's program execution has been stopped.

Display the breakpoint addresses

FORMAT : ;V or $V

This command displays the addresses at which breakpoints are set. If no breakpoints have been set (or if they have been removed), EXORbug will display "NO BKPT".

Remove a specified breakpoint

FORMAT : addr;U

This command removes the breakpoint at address addr. If no breakpoint is set at the specified address, EXORbug displays "NO BKPT".

Remove all breakpoints

FORMAT : ;U

This command removes all the breakpoints. If no breakpoint is set, EXORbug displays "NO BKPT".

Specify and enable the trace-to-ending address

FORMAT : $T nnnn [addr] CR

This command enables the trace-to-ending address function, displays the current ending address (nnnn) and allows the user to change it. Once enabled , the trace-to-ending address is initiated by starting program execution with the ;P command. EXORbug will trace the target program, instruction by instruction, until the trace program counter is equal to the ending address. Therefore, the ending address should be set on the first byte of an instruction.

During the trace, entering Control-W will cause the trace to pause until some other character is entered. Entering Control-X will

abort the trace and return control to EXORbug.

Once enabled, the trace-to-ending address remains active until it is disabled or an abort or restart occurs.

Since the trace operation uses an NMI (and the stack), tracing should not be used unless the stack pointer is pointing to a valid stack area.

CWAI instructions cannot be traced because the trace NMI would cause the CWAI to continue and not wait for the user interrupt.

Disable the trace-to-ending address

FORMAT : ;T

This command disables the trace-to-ending address function.

4.1.3.2 Program Execution

These commands permit the user to execute the target program. The various program execution commands permit starting the target program through the restart vector or at a specified address, proceeding with program execution, and tracing one or more instructions.

Start the target program through the restart vector

FORMAT : ;G

This command starts the target program through the user restart vector. The restart vector is obtained from the user's top of memory specified at addresses $E72E and $E72F (see the start-up procedures section.) Therefore, when using ;G, the top of memory address should be set up appropriately otherwise EXORbug will display the "NO VECTORS" message.

This command cannot be used to initiate a trace-to-ending address function. If the trace-to-ending address mode is enabled when the command is entered, EXORbug will display WHAT ?, sound the bell, and issue another prompt.

The values of the target registers are taken except for the direct page register which is cleared and the I and F masks in the condition code register which are set to emulate an effective restart sequence.

The user should ensure that the stack pointer is pointing to a valid stack area before any debug functions, such as breakpoints or track change of memory location, are encountered in the target program. This can be accomplished by specifying the stack pointer value using the RS command before the ;G command, or by executing an LDS instruction at the beginning of the target program.

Start the target program at a specified address

FORMAT : addr;G

This command starts the target program at the specified address. The processor registers will be loaded from the target registers which contain the last values obtained by EXORbug (during the last breakpoint or trace operation). The values of the target registers can be changed using the register change commands (see paragraph 4.1.2.1). During system turn-on, the target stack pointer is initialized to $E703, the target direct page register is cleared and the I and F masks in the target condition code register are set. All other target registers are cleared.

The user should ensure that the stack pointer is pointing to a valid stack area before any debug functions, such as breakpoints or track change of memory location, are encountered in the target program. This can be accomplished by specifying the stack pointer value using the RS command before entering the addr;G command, or by executing an LDS instruction at the beginning of the target program.

The addr;G command cannot be used to initiate a trace-to-ending address function. If the trace-to-ending address is enabled when this command is entered, EXORbug will display WHAT ?, sound the bell, and issue another prompt.

NOTE

- Some EXORbug routines make use of direct addressing with a direct page register value not equal to 00. Aborting may cause the target direct page register to be set to the EXORbug value. Therefore, if the user program uses direct addressing, it is a good practice to check the target register values before entering the addr;G command.

Proceed with target program execution

FORMAT : [value];P

This command resumes target program execution using the target register values. The value (if entered) specifies the number of breakpoint locations to be passed before a breakpoint returns control to EXORbug. Figure 4-4 shows an example of ;P command utilisation.

A pass value will not be accepted if no breakpoint is set and EXORbug will display "NO BKPT". If a pass value is entered and the track change of memory location is active, EXORbug will display WHAT ?, sound the bell, and issue another prompt.

The value;P command cannot be used to initiate a trace -to-ending address function. Even if the trace-to-ending address is enabled, entering value;P will not cause the target program to be traced.

However, the ;P command can be used to initiate a trace-to-ending address function if a pass value is not entered.

Breakpoints are not active during a trace-to-ending address function.

Trace the next instruction

FORMAT : [value];N

This command traces the next instruction(s). If a value is entered, it specifies the number of instructions to be traced. After each instruction is executed, the registers (and optional memory location) are displayed.

If multiple instructions are traced, entering Control-W will cause the trace to stop until some other character is entered. Entering Control-X will cause the trace to abort.

Since the trace function uses NMI, CWAI instructions should not be traced because CWAI instructions will not wait for the user interrupt, but will continue due to the NMI.

Because the trace NMI uses the stack, tracing should only be done in portions of the target program where the stack pointer is pointing to a valid stack area.

4.1.3.3 Memory Search

These commands control the memory search function. Commands are included to establish the search address range and comparison mask and to initialize the memory search.

Specify search address range and comparison mask

FORMAT : ;M or $M

This command first requests the search address range as described in the PRNT command. Memory will be searched from the beginning address specified through the ending address.

After a valid address range is entered, EXORbug requests the search comparison mask in the following manner :

MASK=nnnn [value] CR

nnnn is the hexadecimal representation of the current mask. If the current mask is correct, the user may enter a CR. Otherwise, a new value followed by a CR can be entered.

The search command (value;W) allowing searches of single or double bytes, the search mask has to be, respectively, a single or double byte.

The mask specifies which bits are to be checked against the search value. For example, a mask of $FFFF would compare each bit (during a double byte search), while a mask of $01 would compare only bit 0, the least significant bit (during a single byte search). All bit positions for which the search mask contains a 0 are don't cares.

Search for single or double byte

FORMAT : value;W

This command searches memory over the specified beginning-ending address range for a match with the value entered. The value entered, can be a single or double byte. Only those bit positions set to one in the last comparison mask entered, are compared during the search.

The same beginning and ending address parameters are used for the PRNT, DUMP, IS, I, and the M commands. Therefore, if one of these commands is entered after the M command but before

the W command, the beginning and ending addresses specified for the last such command entered will be used as the search range.

If the value entered for the ;W command is a single byte and if the most significant half of the current mask is not 0, EXORbug will request a new mask to ensure that the user is willing to perform a double byte search. If the user does not modify the mask, a double byte search (where the least significant byte of the search value is the value entered and the most significant byte is 0) will be performed.

If the current mask has a value of 0000 (which means that all bits of the search value are don't cares), EXORbug will request a new mask.

When the memory search finds a match, the address of the match is displayed. Entering Control-W while the search is being performed, causes the search command to wait until some other character is entered. Entering Control-X, causes the search to abort and control to be returned to the EXORbug command level.

4.1.3.4 Miscellaneous

These commands allow the user to initialize memory with a specific bit pattern and to control the line printer operation.

Initialize memory to a specific bit pattern

FORMAT : byte;I

This command initializes random access memory to the specified byte value. After the command is entered, EXORbug requests the beginning and ending addresses of the memory region to be initialized. The beginning and ending addresses are entered as described in the PRNT command.

After valid beginning and ending addresses have been entered, the memory is initialized. The byte value entered is stored in each memory location, starting at the beginning address through the ending address.

As each memory location is initialized, EXORbug reads it back to ensure memory changes properly. Should a memory location not change correctly, EXORbug displays "NO CHNG" and aborts the ;I command.

Enable/disable copy of output to the line printer

FORMAT : ;Z nn [byte]

This command displays the status of the ZFLAG which controls the line printer interface. When the nn value (ZFLAG) is 0, the line printer is not activated and data is only displayed on the system CRT. The nn=0 status is a default condition following a power-up or restart. When the nn value is non-zero (1), the line printer is activated and the CRT output data is also sent to the line printer. The printer output is not paged, but continuous. To select output to the line printer, a "byte" value of 1 must be entered.

User program output, directed through the various EXORbug subroutines, will also be directed to the line printer if the ZFLAG has a value of 1. Note that the ZFLAG is kept in location $E729 and can be modified by program.

4.1.4 Memory Change

The Memory Change function permits the user to examine and change individual memory locations, and to calculate offsets for relative addressing mode instructions. To invoke the Memory Change function, the user enters :

addr/

After the user enters the slash, EXORbug displays a space followed by the contents of the specified memory location in hexadecimal, and then another space. If the contents are to be changed, the user enters a new value in hexadecimal, or an apostroph (') followed by a single character to insert an ASCII character. Next, the user enters one of the following terminators to close the current memory location :

Carriage Return -This ends the Memory Change function and returns control to the EXORbug command level. EXORbug prompts the user.

Line Feed -This causes the next sequential memory location to be opened for memory change. Its address and contents are displayed on the next display line.

Space -This causes the next sequential memory location to be opened for memory change. The contents of the opened location is displayed on the same display line.

Comma -This causes the next sequential memory

location to be opened for memory change. No display is performed.

Up Arrow -This causes the previous sequential memory location to be opened for memory change. Its address and contents are displayed on the next display line.

Slash -This causes the current memory location to be reopened for memory change. Its address and contents are displayed on the next display line.

If an attempt is made to change memory, but the memory does not change properly, EXORbug will issue the "NO CHNG" message, sound the bell, and prompt the user.

The Memory Change function can also be used to calculate the required offset for relative addressing instructions with the addr;O or addr;L commands. To calculate a relative offset, first open the memory location that is to contain the offset or the first byte of the offset in the case of a long branch. (e.g. the second byte of a branch instruction.) Next the destination address is entered, followed by a semicolon and the letter O for a short branch offset, letter L for a long branch offset.

The Memory Change function will indicate that the destination address is out of range by displaying "OUT OF RANGE". If the destination address is in range, the correct offset will be displayed. In both cases, the address and contents of the current location will be redisplayed on the next display line, permitting the user to easily modify it or request another offset calculation.

4.1.5 Control Commands

This paragraph describes the various control commands that can be entered from the system keyboard. All control commands are escape sequences and require two keystrokes. The format for an escape sequence, is the escape code (ESC key) followed by a valid escape character. The valid escape characters are listed in Table 4-1.

The required escape sequences can also be generated by a user program instead of being entered on the keyboard. The escape code ($1B) followed by the selected escape character can be sent to EXORbug via the XOUTCH, XPDATA and XPDAT1 subroutines described in paragraph 4.3.

The various control commands fall into three groups :

- Display control
- Screen control and cursor movements
- Miscellaneous

4.1.5.1 Display Control Commands

The commands in this group allow the user to switch the alphanumeric and graphic displays on and off, and to change the display format.

ESC S — This command is used to enable the alphanumeric display. The display format and the alphanumeric display memory are not modified by this command.

ESC T — This command disables the alphanumeric display. The screen image is not lost and can be visualized using the ESC S command.

However, all operations performed while the alphanumeric display is switched off will modify the display memory affecting the image obtained with the next ESC S command.

ESC Y — This command is used to enable the graphic display. If the display format being currently selected is 80 characters/line, the ESC Y will switch automatically to 40 characters/line and erase the alphanumeric display.

Memory locations $4000 through $7FFF are used as graphic display memory.

ESC Z — This command is used to disable the graphic display.

ESC F — This command switches the display format. The two available display formats are : 80 characters/22 lines and 40 characters/16 lines.

The graphic display is operational only in the 40 character/line format. Therefore, when switching from 40 to 80 character format, the graphic display is disabled. In addition, the ESC F command erases the alphanumeric display (and EXORbug 1.1 version displays the header information).

4.1.5.2 Screen control and cursor movement commands

The commands in this group allow the whole or portions of the alphanumeric display to be erased and the cursor to be moved in any direction.

ESC H — This command moves the alphanumeric display cursor one place to the left (back space).

ESC N This command moves the cursor to the next display location (to the right).

ESC U This command moves the cursor up one line.

ESC V This command moves the cursor down one line.

ESC L This command moves the cursor home (to the first position in the first display line).

ESC K This command kills a line from the current cursor position.

ESC C This command clears the display from the current cursor position.

ESC E This command erases the whole display and moves the cursor home.

4.1.5.3 Miscellaneous Commands

The commands in this group allow the user to switch back to the stand-alone mode of operation, sound the system bell and to invert the display background.

ESC O This command allows to return from the terminal mode of operation to the stand-alone (local) mode of operation.

Note that if a valid escape sequence is received from the serial link, it will be executed by EXORbug. This means that the EXORset can be switched from on-line to local mode of operation by the attached peripheral (i.e an EXORciser).

ESC G This command sounds the system bell.

ESC B This command is used to invert the display background. All visual characters displayed after the ESC B command has been entered, will be displayed with inverted background until another ESC B command is entered.

4.2 ADDING EXORbug COMMANDS

The user has the ability to add as many four character commands as desired. The only limiting factor is memory size. In order to implement this feature, the user must have a table of his commands and the actual commands stored in

memory, and must have told EXORbug where his command table resides. The user command table format must be as follows :

```
Example :  CTBEG   EQU *          Command table beginning
-------            FCC /CMD1/     Four character command
                   FDB CMD1E      Entry address of command
                   FCC /CMD2/     Four character command
                   FDB CMD2E      Entry address of command
                    .  .            .
                    .  .            .
                    .  .            .
                    .  .            .
                   FCC /CMDN/     Four character command
                   FDB CMDNE      Entry address of command
           CTBEND  EQU *          Command table end
```

Once the user's command table is stored in memory, EXORbug must be informed of its location by having the beginning address of the table (the value of CTBEG in the above example) put at locations $E730 and $E731; while the ending address of the table (the value of CTBEND in the above example) is put at locations $E732 and $E733. In both of these cases, the addresses are loaded into memory in the order of most significant byte first followed by the least significant byte.

If the command table and commands are loaded from a tape, the tape may contain an object code that will properly initialize these locations. This object code may be generated by the ORG and FDB statements in the source program. For the above example, the source code required to generate the proper object code to initialize these locations would be :

```
Example : ORG $E730
          FDB CTBEG,CTBEND
```

Note that an ORG statment or END statment would be required after the two source lines shown above, so that the object code would not be produced at locations $E734 and beyond.

Pressing the ABORT button will not modify locations $E730 through $E733. However, pressing the RESTART button will cause these locations to be restored to the EXORbug values. These locations will also be restored to the EXORbug values when power is first applied. Thus, following a RESTART, the user must restore the beginning and ending addresses of his command table (if required) in memory locations $E730 through $E733. If the user does not wish to add commands, no operation is needed.

On entry to the user command, the stack pointer will be pointing at $E7F9 ; the X register will contain the starting address of the user command routine; the other registers are undefined.

4.3 EXORbug SUBROUTINES AND ENTRY POINTS

This paragraph lists and describes the various subroutines and entry points in EXORbug that are available to the user. Any user program running in the EXORset memory may call the described routines or entry points.

Table 4-2 lists the available routines with their corresponding entry addresses.

The first set of routines as well as their entry addresses are compatible with EXbug 1 and 2. Except as stated in the descriptions, all of these are subroutines, end with an RTS, and should only be called by BSR, LBSR, or JSR instructions. Control will be returned to the instruction after the calling BSR, LBSR or JSR, provided the stack pointer and stack memory area are correctly implemented.

Some routines that involve input from the keyboard will wait (in a loop) until the character(s) is(are) input before returning to the calling program. Unless indicated otherwise, routines that output to the display are affected by the SP command and by the ;Z command. That is, output through these routines will be slowed down if SP has not the default value (0000), and will be sent to the line printer, as well as the display, if the Z option is on. The SP value is held in memory locations $E736 and $E737, and can be modified by the user program. The same comment is valid for the ZFLAG at location $E729.

Table 4-2 EXORbug Routines

ENTRY ADDR	NAME	FUNCTION	PAGE
F000	PWRUP	ENTER EXORbug FROM RESTART	04-28
F003	XBEGEN	INPUT BEG & END ADDRESSES	04-28
F006	XCBCDH	CONVERT HEX TO BCD	04-28
F009	XCHEXL	CONVERT MS HALF TO HEX (ASCII)	04-29
F00C	XCHEXR	CONVERT LS HALF TO HEX (ASCII)	04-29
F00F	XINADD	INPUT HEX ADDR INDIRECT (X)	04-29
F012	XINCH	INPUT ONE CHARACTER	04-30
F015	XINCHN	INPUT ONE CHARACTER	04-30
F018	XOUTCH	OUTPUT ONE CHARACTER	04-30
F01B	XOUT2H	DISPLAY 2 HEX CHAR (X)	04-30
F01E	XOUT4H	DISPLAY 4 HEX CHAR (X)	04-31
F021	XPCRLF	DISPLAY CR,LF	04-31
F024	XPDATA	DISPLAY CR,LF,DATA STRING	04-31
F027	XPDAT1	DISPLAY DATA STRING	04-32
F02A	XPSPAC	DISPLAY SPACE	04-32
F02D	XORBUG	EXORbug ENTRY POINT	04-32
F030	XLDA	CROSS MAP LOAD	04-32
F033	XSTA	CROSS MAP STORE	04-33
F036	XTOGL	MAP SWITCHING	04-33
F039	ZAPBKP	REMOVE BREAKPOINTS	04-33
F042	PRINT	OUTPUT 1 CHAR TO LINE PRINTER	04-33
F045	CHKBK	CHECK BREAK	04-34

Table 4-3 Useful EXORbug RAM locations

ADDR	NAME	FUNCTION
E703	STACK	END OF DEFAULT 36 BYTE USER STACK
E704	L4080	DISPLAY LINE LENGTH (40/80 CHARS.)
E705	LCOUNT	CURSOR POSITION LINE COUNT
E706	RCOUNT	CURSOR POSITION ROW COUNT
E707	LCNTMX	MAX. NUMBER OF DISPLAY LINES
E708	RCNTMX	MAX. NUMBER OF DISPLAY ROWS
E714	NECHO	NO ECHO FLAG FOR DISPLAY
E71B/1C	BEGA	BEGINNING ADDRESS
E71D/1E	ENDA	ENDING ADDRESS
E722	BACKGD	DISPLAY BACKGROUND INVERSION FLAG
E729	ZFLAG	LINE PRINTER ON/OFF FLAG
E72E/2F	ATOP	TOP OF USER VECTOR TABLE ADDRESS
E730/31	CTBEG	USER COMMAND TABLE BEG. ADDRESS
E732/33	CTBEND	USER COMMAND TABLE END. ADDRESS
E736/37	SP	DISPLAY SPEED PARAMETER

Name: PWRUP - Power-up and restart entry

Function: Configure EXORbug and its peripherals from a restart or power-up condition.

Call: JMP PWRUP

Output: EXORbug parameters are initialized along with the EXORbug peripheral devices. The EXORbug start-up message is displayed. Note that control is not returned to the calling program, but is given to the EXORbug command input routine.

* * * * *

Name: XBEGEN -Input start and end addresses

Function: Requests input of beginning and ending addresses as defined in the PRNT command. Verifies that inputs are hexadecimal characters. Verifies that the entered ending address is larger than the beginning address.

Call: JSR XBEGEN or (BSR or LBSR)

Output: BEGA ($E71B/$E71C) 16 Bit Beginning address
ENDA ($E71D/$E71E) 16 Bit Ending address

A, B, and X registers are modified.

* * * * *

Name: XCBCDH - Convert an hexadecimal character to a binary number.

Function: Verifies that the input is a hexadecimal digit character. Converts the character in Acc A to a 4-bit binary number with high order 4 bits equal to zero. Sets N (negative)

condition code for non-hexadecimal characters.

Call: JSR XCBCDH

Input: Character to convert must be in Acc A

Output: If hexadecimal character input, Acc A contains the 4-bit binary number represented by the input character and the N condition code is cleared. If non-hexadecimal character input, Acc A contains the character input and the N condition code is set. The B, X and Y registers are preserved.

* * * * *

Name: XCHEXL - Convert binary value to Hex

Function: Converts the most significant 4 bits of Acc A to an ASCII coded hexadecimal digit character.

Call: JSR XCHEXL

Input: Acc A contains the byte to be converted

Output: An ASCII coded hexadecimal digit character in ACC A. The B, X and Y registers are preserved.

* * * * *

Name: XCHEXR - Convert least significant binary value to Hex.

Function: Convert the least significant 4 bits of Acc A to an ASCII coded hexadecimal digit character.

Call: JSR XCHEXR

Input: Acc a contains the byte to be converted

Output: An ASCII coded hexadecimal digit character in ACC A. The B, X and Y registers are preserved.

* * * * *

Name: XINADD - Input an hexadecimal address.

Function: Convert up to 4 input hexadecimal characters to a 16-bit binary number.

Call: JSR XINADD

Input: X index register contains address where to store the result

Output: Most significant 8 bits of resultant 16-bit address will be stored into the memory location pointed at by the X index register. The least significant bits will be stored

into the next higher memory location. Acc A will contain the last character input.Acc B will contain the number of input characters. X and Y index registers are unchanged. The subroutine returns to the calling program when an invalid character, or the fifth hexadecimal digit is entered.

* * * * *

Name: XINCH - Input one character

Function: Wait for and accept input of one character from the system keyboard and echo character to the display if required.

Call: JSR XINCH

Input: There is a "no echo" flag NECHO at address $E714. It must be set non-zero before each call to XINCH for each character that is not to be echoed to the display (and line printer if the Z option is on).

Output: Acc A contains the 8-bit input character as received from the system keyboard. XINCH clears NECHO if it was non-zero. The B, X and Y registers are preserved.

* * * * *

Name: XINCHN - Same as XINCH

* * * * *

Name: XOUTCH - Output character

Function: Output one character with required speed fill.

Call: JSR XOUTCH

Input: Acc A contains the character to output to the system display (and to the line printer if the Z option is on).

Output: Acc A contains character output. The B, X and Y registers are unchanged.

* * * * *

Name: XOUT2H - Output two hexadecimal characters and a space

Function: Converts the contents of an 8-bit binary byte to two hexadecimal charcetrs and output them followed by a space character to the system display

Call: JSR XOUT2H

Input: X index register contains the address of the byte to be converted and output.

Output: Acc A contains the last character output. The X index register is incremented by one. The B and Y registers are preserved.

* * * * *

Name: XOUT4H - Output 4 hexadecimal characters and a space.

Function: Convert the contents of two consecutive 8-bit binary bytes to four hexadecimal characters and output them followed by a space character to the system display.

Call: JSR XOUT4H

Input: X index register contains address of the first byte to be converted and output.

Output: Acc A contains the last character output. The X index register is incremented by two. Other registers are preserved.

* * * * *

Name: XPCRLF - Display CR/LF

Function: Output a carriage return and a line feed to the system display with required speed fill.

Call: JSR XPCRLF

Output: Acc A is modified. Other registers are preserved.

* * * * *

Name: XPDATA - Display CR/LF/Data string

Function: Output a carriage return, a line feed, and the user specified string of characters to the system display

Call: JSR XPDATA

Input: X index register will contain the starting address of user data string to output. Output string must be terminated by an EOT (04) character.

Output: X index register will contain the address of the EOT character. Acc A will contain the EOT character. Other registers are preserved.

* * * * *

Name: XPDAT1 - Display Data string

Function: Output a user specified string of characters.

Call: JSR XPDAT1

Input: X index register contains the starting address of the user data string to output. The output string is terminated by an EOT (04) character.

Output: X index register will contain the address of the EOT character. Acc A will contain the EOT character. Other registers are preserved.

* * * * *

Name: XPSPAC - Display space

Function: Output a space character to the system display.

Call: JSR XPSPAC

Output: Acc A will contain the space character. Other registers are preserved.

* * * * *

Name: XORBUG - Reenter EXORbug

Function: Entry point for user programs to re-enter EXORbug.

Call: JMP XORBUG

Output: Control is not returned to the calling program.

* * * * *

Name: XLDA - Cross map load

Function: Loads the A accumulator with the data pointed at by the X index register. The data is fetched from the other memory map.

Call: JSR XLDA

Input: X index register is the data pointer

Output: A accumulator holds data. All other registers are preserved.

Caution: The system stack must be common to both maps.

* * * * *

Name: XSTA - Cross map store

Function: Stores the content of the A accumulator in the location pointed at by the X index register. The destination is in the other memory map.

Call: JSR XSTA

Input: A accumulator holds data to be stored
X index register is the data pointer

Caution: The system stack must be common to both maps.

* * * * *

Name: XTOGL - Memory map switching

Function: Switches from one memory map to the other.

Call: JSR XTOGL

Caution: The system stack must be common to both maps.

* * * * *

Name: ZAPBKP - Remove breakpoints

Function: Clears the breakpoint RAM and disables breakpoints.

Call: JSR ZAPBKP

Output: A, B, X, and Y registers are modified.

* * * * *

Name: PRINT - Print one character on the line printer

Function: Outputs the character held in A accumulator to the line printer.

Call: JSR PRINT

Input: A accumulator helds the character to be printed.

Output: All registers exept Condition Code register are preserved.

If the printer is not selected or out of paper, then the

Carry bit in the Condition Code register is set on return.

* * * * *

Name: CHKBK - Check break

Function: Gets a character from the keyboard (if any) and checks if it is a break (Control-P) or a Control-W. If a Control-P is received, the routine returns with the Carry set. If a Control-W is received, the routine waits for the next keyboard entry. All other characters cause the routine to return with a cleared Carry.

Call: JSR CHKBK

Output: All registers saved except CC which has the Carry, set if a Control-P is received, cleared otherwise.

* * * * *

4.4 USE OF INTERRUPT VECTORS

EXORbug provides for the interrupt features of the 6809 to be available to the user without restricting EXORbug's use of them. This capability is referred to as the second level interrupt feature. The EXORbug use of the interrupt is the first level and has the highest priority. EXORbug gains control first, then decides if user processing at the second level is specified. The second level vectors (user's vectors) are located indirectly : the address contained in locations $E72E and $E72F points to the last byte of the second level restart vector. This location is referred to symbolically as "ATOP". The other vectors are in the normal order, as illustrated in Figure 4-5. EXORbug tests if ATOP is initialized by the user and has a non-zero value before passing control onto the second level interrupt service routine.

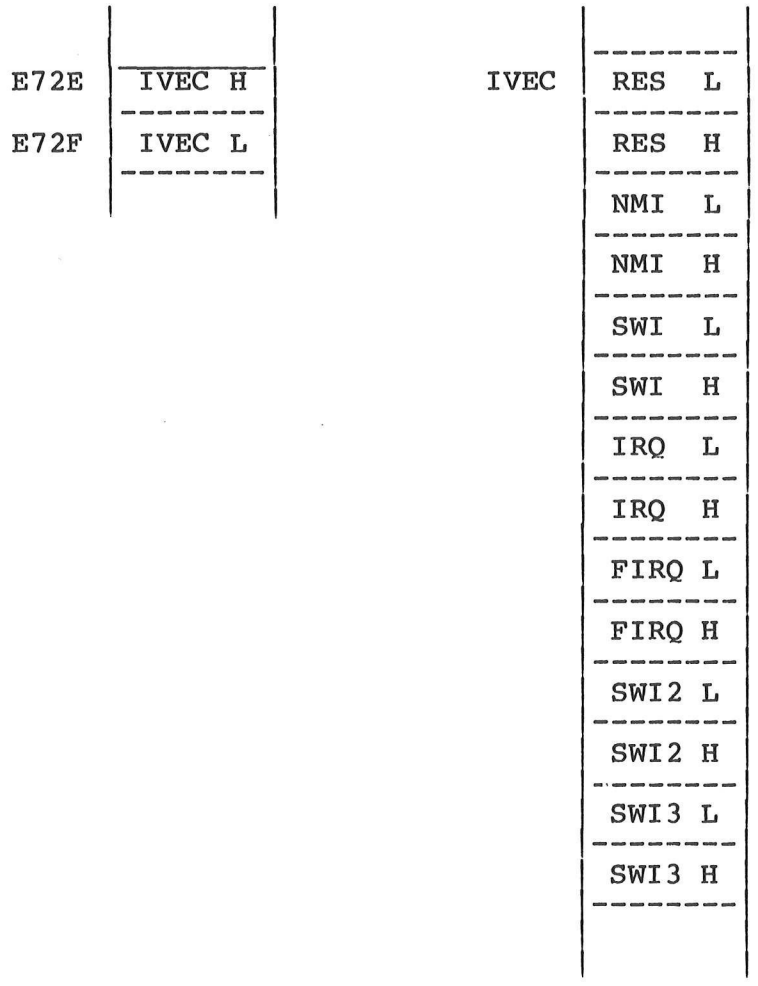


Figure 4-5 Second Level Interrupt Vectors

CHAPTER 5

THEORY OF OPERATION

5.1 INTRODUCTION

This chapter summarizes the EXORset system specifications and describes the operation of the EXORset Main Controller Board and Mini-Floppy Disk Controller Board. A simplified block diagram is presented in Figure 5-1.

5.2 SPECIFICATIONS

The specifications of the various functional units are identified in the following paragraphs.

5.2.1 Main Controller Board Specifications

Power requirements (max)	5V/6A, +12V/1A, -12V/1A
Operating temperature	0 to 50 deg.C
Processor	MC6809
Word size	
Data	8 bits
Address	16 bits
Instructions	8,16,24,32 bits
Instructions	59 instruction mnemonics
Addressing modes	10
Clock cycle time	1 microsecond
Baud rates	50 - 19200 (programmable)
Memory size	56K bytes of RAM and 24K bytes of E/ROM available to user.
Serial interface	
Syncronous or asyncronous	RS-232C,RS422,RS423 & Current Loop
Physical Characteristics	
Dimensions (WxD)	248 mm x 470 mm
Board thickness	1.6 mm

Parallel interface	50-pin card edge
Serial interface	20-pin card edge
CRT	Composite Video or Seperate Sync.
Light Pen Interface	3-pin
Keyboard	ASCII : flex-tail,23-pin or card edge, 50-pin Funct.keys : flex-tail,8-pin or card edge, 20-pin
Timer I/O	20-pin

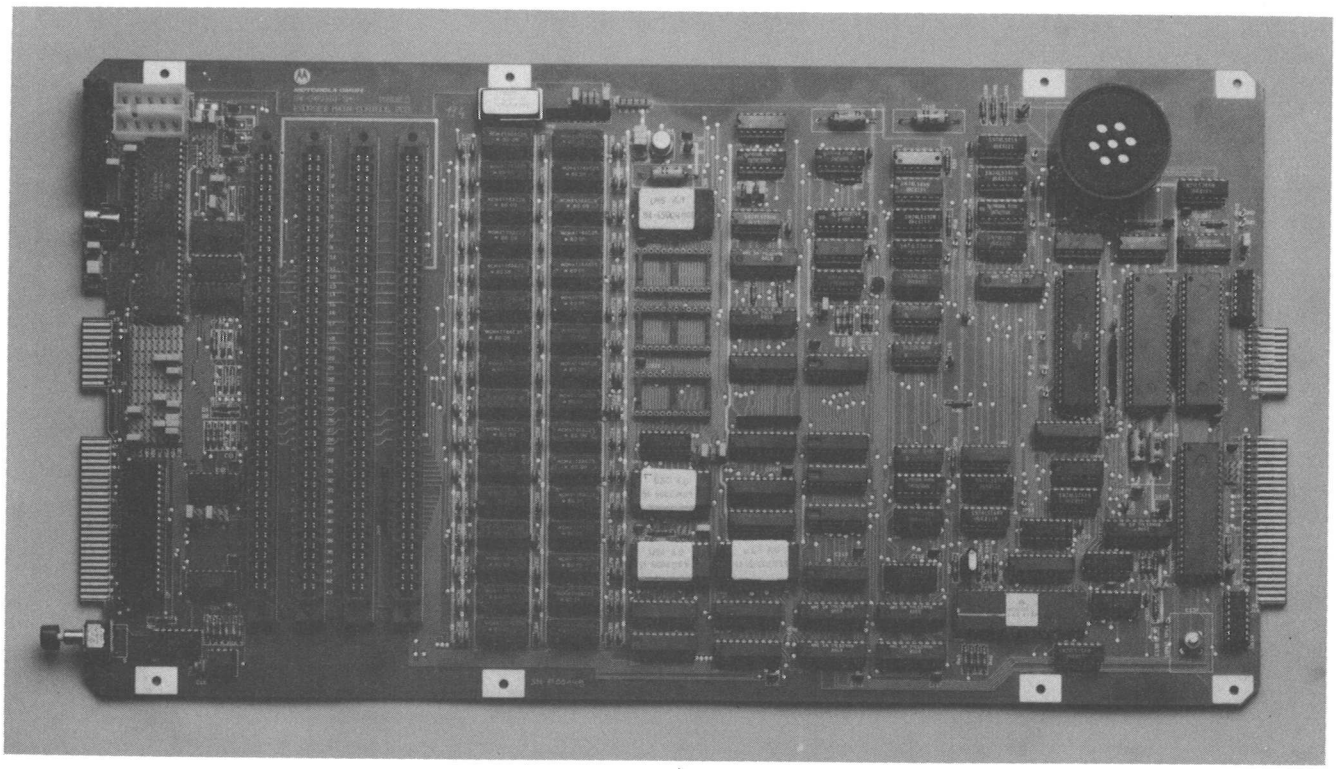


Figure 5-1 Main Controller Board

5.2.2 Floppy Disk Controller Board Specifications

Power requirements (max)	5V/0.8A, +12V/0.2A, -12V/0.15A
Operating temperature	0 to 50 deg.C
Memory size	16K bytes of RAM (not used), 1K bytes of E/ROM (disk driver)
Interface	
Output	TTL open collector
Input	220/330 ohm line terminations
Physical characteristics	
Dimensions (WxD)	248 x 146 mm
Board thickness	1.6 mm
Connector	34-pin card edge connector

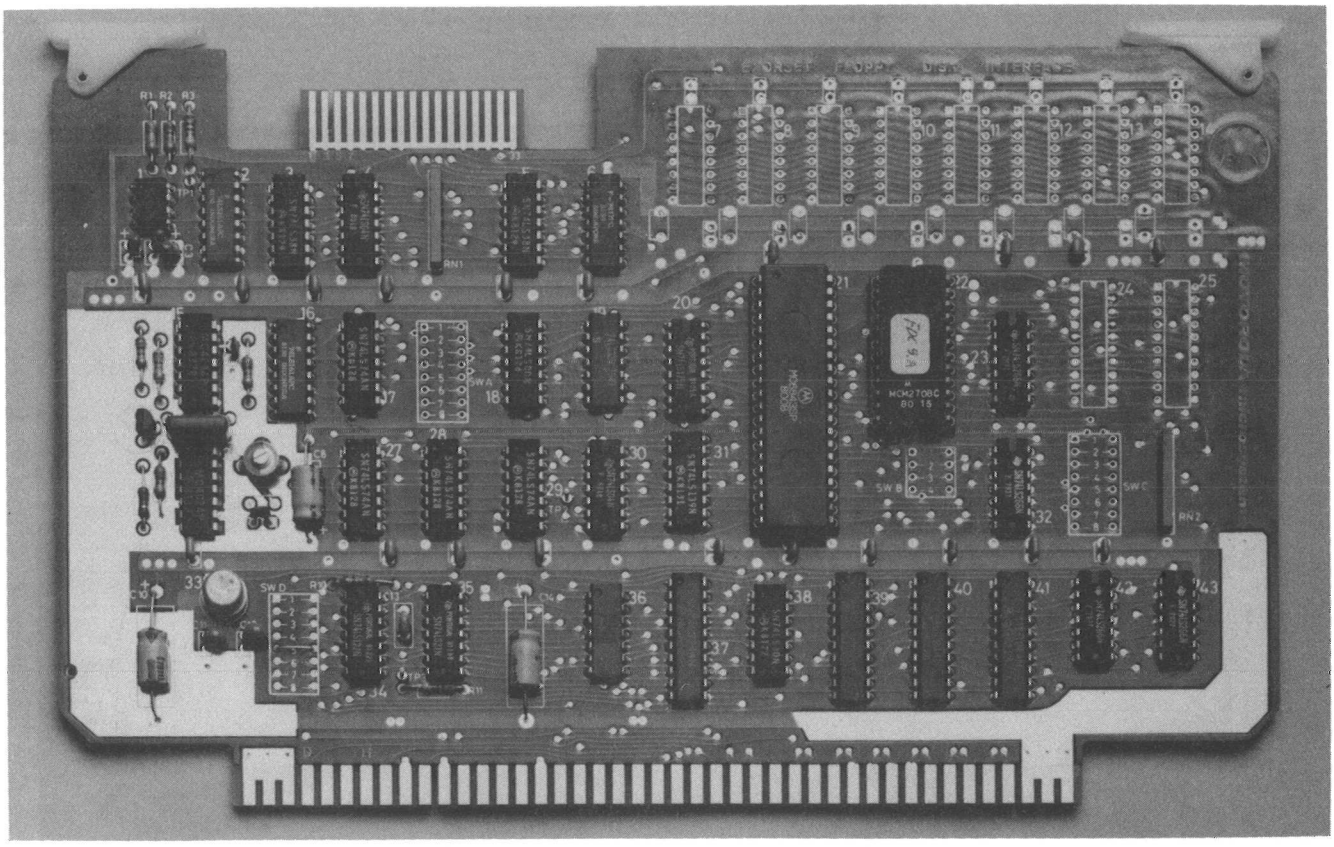


Figure 5-2 Floppy Disk Controller Board

5.2.3 Video Display Specifications

Cathode Ray Tube	9 inches measured diagonally (22.8 cm) - 44 sq.inch viewing area (28.4 sq.cm) - 90 deg. deflection angle - integral implosion protection - P4 (white) or P31 (green) phosphor.
Power input	12 Vdc at 900 milliamperes
Input signals	Composite video , 0.5 to 2.5 V composite P/P , negative sync , input impedance : 75 ohms
Video response	Within 3dB , 10 Hz to 12 MHz
Pulse rise time	20 V rise in 40 nanoseconds
Resolution	650 lines at center , 500 lines at corners
Distorsion/lin.	Less than 2% , measured with standard EIA ball chart and dot pattern
High voltage	9.5 kV at 50 microamp.beam current
Horiz.blanking	11.0 microseconds min (includes retrace and delay)
Scanning freq.	Horiz. 15,750 +/- 500 Hz Vert. 50 / 60 Hz
Controls	Brightness, vertical linearity, horizontal size, raster centering, vertical hold, horizontal hold
Dimensions	7.25 inches high (18.4 cm) - 9.50 inches wide (24.1 cm) - 9.48 inches deep (24.1 cm)
Weight	Net 8 lbs (3.6 kg)
Environment	Operating temperature 0 to 55 deg.C - Storage temp. -40 to +65 deg.C - Operating altitude 10,000 ft max.(3048 m) - Humidity 10% to 90% relative, non-condensing - Approved under spec. 478 (Electronic Data Processing Equipment Components) - Designed to comply with applicable DHEW rules on X-radiation

(This table refers to 9" monitor units. The 12" monitor specifications are described in Appendix B).

5.2.4 Mini-floppy Disk Drive Specifications

Type	BASF 6106 or 6108
Storage capacity	
Formatted	81,920 or 163,840 bytes / disk 40 or 80 tracks / disk 2,048 bytes / track 16 sectors / track 128 bytes / sector
Access time	
Latency	200 ms max / 100 ms average
Track to track	12 ms
Average	240 ms
Settling time	50 ms max
Head load time	35 ms max
Rotational speed	300 RPM
Recording density	2768 BPI (inside track)
Flux density	5536 FCI
Track density	48 TPI
Track radius	57.15 mm (2.25 in) (track 0) 36.5125 mm (1.4375 in) (track 39)
Encoding method	FM
Media requirements	BASF 5.25-2 or equivalent
Environment	
Operating temp.	10 to 50 deg C
Relative humidity	20 to 80 %
Power requirements	+5 Vdc / 0.5 A max, max 50 mVpp ripple +12 Vdc / 0.6 A max, max 100 mVpp ripple Drive motor start current 1.4 A max, 1.2 A typ.for 50 ms Head load start current 0.7 A for 50 ms
Power dissipation	10.5 W operating 4.0 W stand-by (motor off) 8.0 W motor on and desselect
Mechanical dimensions	
Width	146.1 mm (5.75 in.)
Height	53.5 mm (2.11 in.) drive, 82.5 mm (3.25 in.) front panel
Depth	190.0 mm (7.48 in.)
Weight	1.4 kg

5.2.5 Keyboard Specifications

ASCII keys number	61
Output	8 x 8 + 6 x 1 matrix
Function keys number	16
Output	4 x 4 matrix
Contacts	screened mylar technology or mechanical
"On" resistance	< 200 ohms
Physical dimensions	417 x 160 mm max (outline dim.)

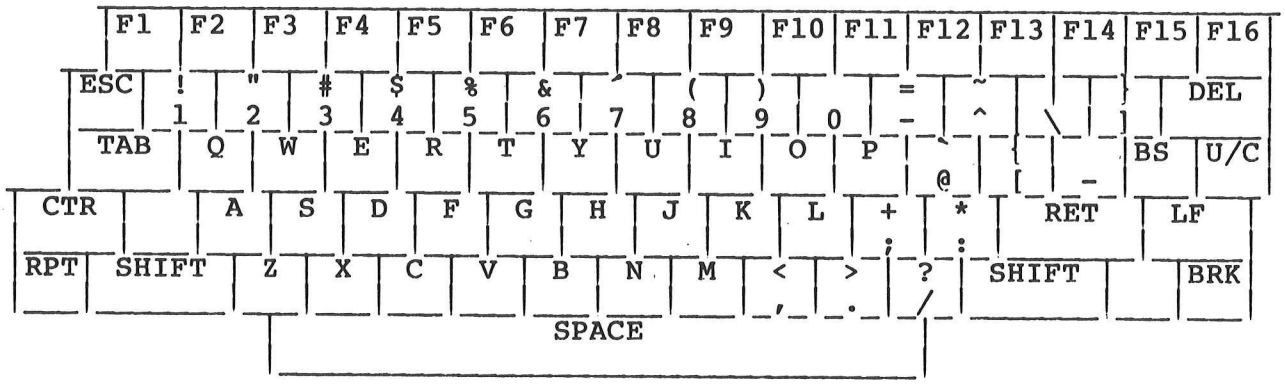


Figure 5-3 Keyboard Assembly

5.2.6 Power Supply Specifications

Refer to Appendix D for the power supply specifications.

5.2.7 Enclosure Specifications

Material	Polyurethane, fire retardant	
Dimensions	EXORset 33	EXORset 100
Width	465.0 mm (18.3 in.)	500.0 mm (19.6 in.)
Height	280.0 mm (11.0 in.)	340.0 mm (13.3 in.)
Length	640 mm (25.2 in.)	655 mm (25.8 in.)

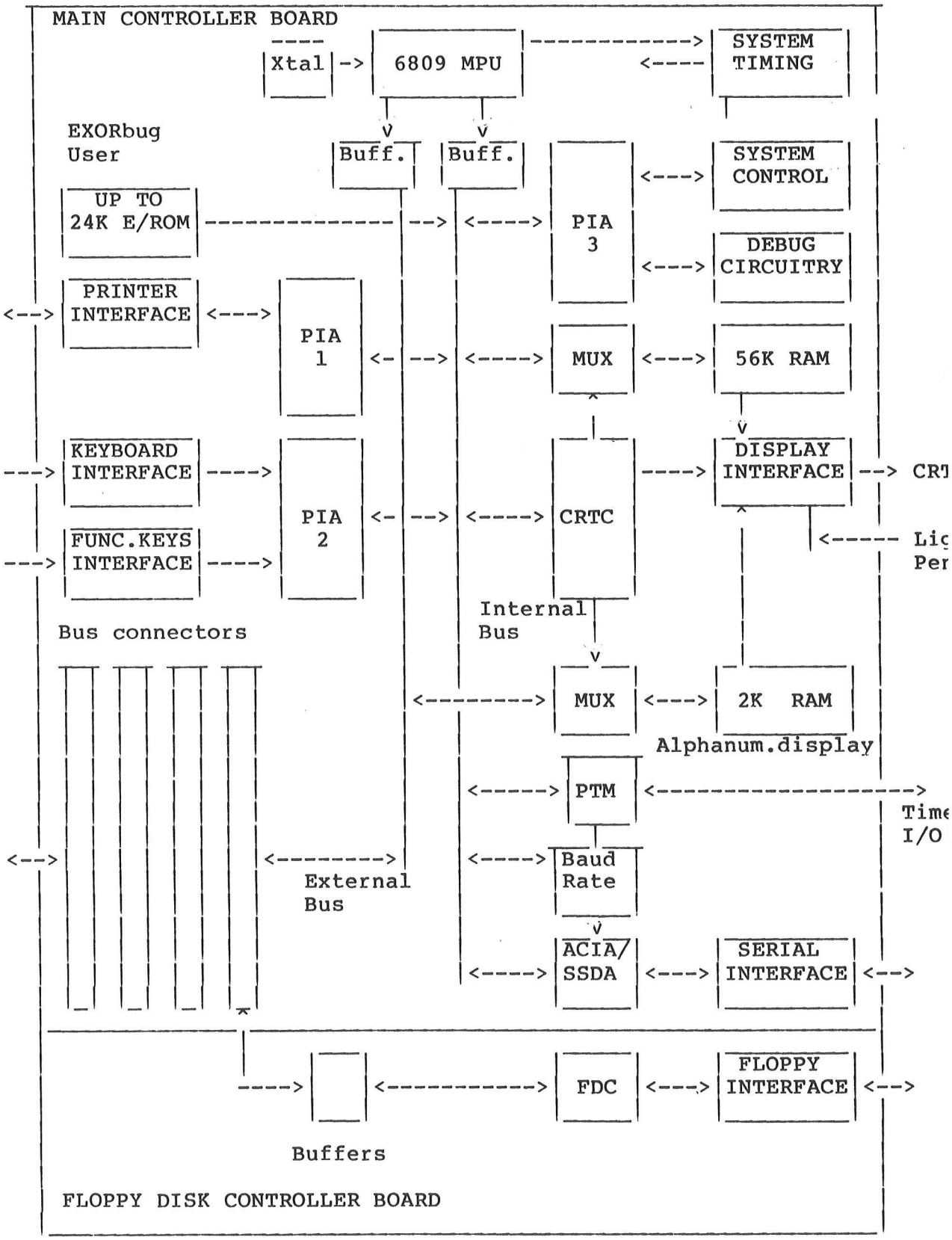


Figure 5-4 EXORset Block Diagram

5.3 MAIN CONTROLLER BOARD

5.3.1 System RESET

An MC1455 (U1) timing device, operated as a monostable multivibrator (one-shot) functions as a restart circuit that generates a low-level RESET signal (approximately 500 ms duration) after power is initially applied to the system. A valid RESET signal (one whose duration is > 8 MPU clock periods) causes the MPU to begin to execute an initialization routine. The RESET signal clears all registers in the PIAs to logic zero (low) so that the PIAs may be configured during system initialization. The RESET signal pre-sets the PTM latches and counters to their maximum count values, disables the counter clocks, clears the status register interrupt flags, and sets the control register internal reset bit which holds all timers in their pre-set state. The RESET signal also restarts the MC3870 Keyboard Encoder Microprocessor. In addition, a debounced RESET switch provides a system reset function. A separate power reset signal (PWRRES) is generated only when power is first applied to the system. This signal is not affected by the RESET switch. PWRRES is used to pre-set the upper case / lower case flip-flop (U106) and the cycle counter flip-flop (U107).

5.3.2 System Timing

One single clock generator generates all signals needed for the MPU, memories, I/O devices, CRT controller and display circuitry. The MPU clock is synchronized with the CRT controller character clock. This allows the use of the same RAM by the CRTC and the MPU in a multiplexed mode without contention (see Figure 5-1). The advantage of this method is that the CRT display refresh is completely transparent to the MPU. Furthermore, dynamic RAM refresh is inherently provided simply by the continuous reading of data by the CRTC.

The MC6809 MPU on-chip oscillator is used as the master clock for the system. A 4 MHz crystal is connected to the EXtal and Xtal inputs of the MPU. The MC6809 Eout (1 MHz) output feeds a phase-lock loop circuitry which generates a 16 MHz signal, the highest frequency of the timing chain. The timing circuitry provides the dot and CRTC clocks, the Row Address Strobe (RAS) and the Column Address Strobe (CAS) for the dynamic RAM, the latch enables, as well as the data bus buffers control signals used to multiplex the RAM access, MPUDR and CRTCDR.

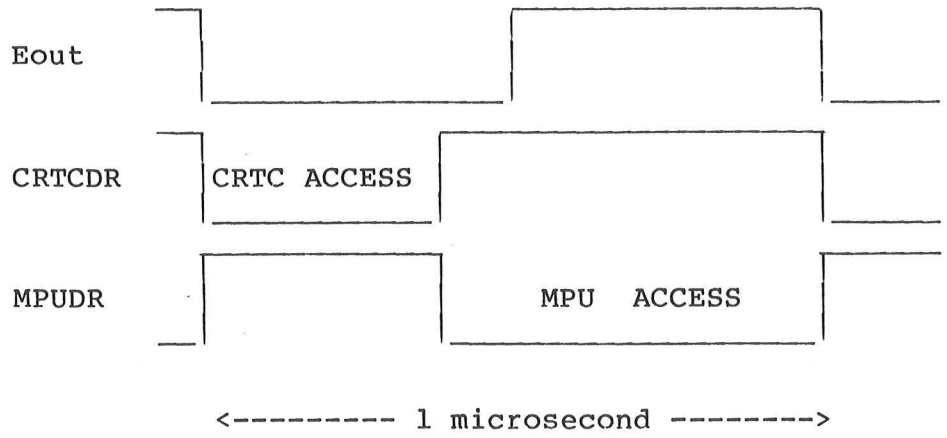


Figure 5-5 Multiplexed Memory Access

5.3.3 MPU and Bus Buffers

The MPU data lines are buffered, using a 74LS640 device (U105). The resulting inverted data bus is available at the Expansion Bus connectors for external boards. A second 74LS640 device (U101) provides the buffered true data bus for all internal devices. The INTADR' signal, generated by the address decoding circuitry, instructs the data bus buffers to turn on when a device located on the Main Controller Board is selected.

Three 74LS244 devices (U75, U89, U111) buffer the MPU address lines.
The address lines for the Expansion Bus Connectors are buffers with bidirectional 741S645's. The direction is controlled by the Bus Grant Signal.

5.3.4 Address Map and Address Decoder Circuits

The EXORset Address Map is shown in Figure 5-3. The upper 8K address range is reserved for the system. The the dynamic RAM on the main board is assigned addresses 0000-DFFF. The RAM area on the Floppy Disk Controller is not used.

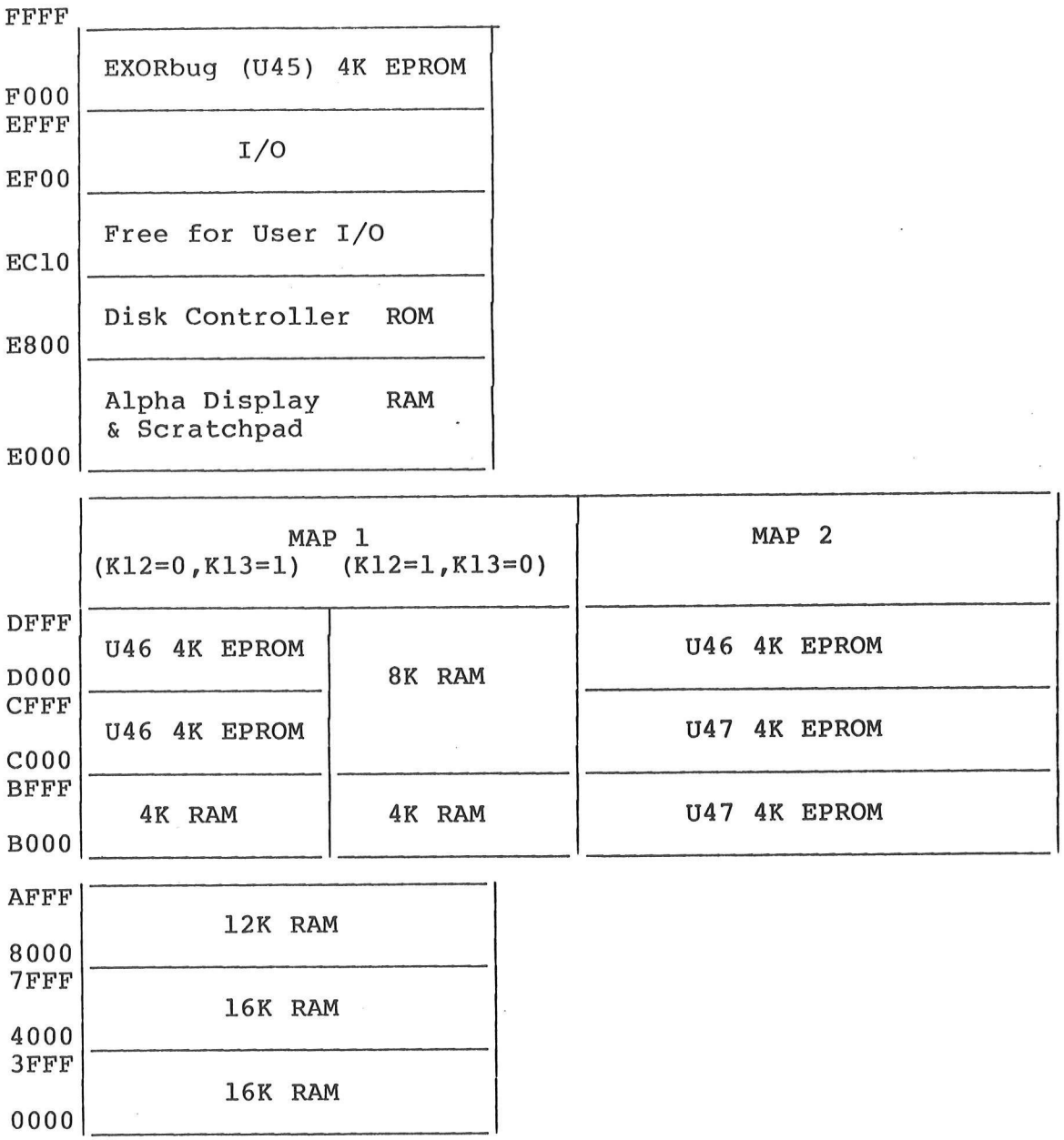


Figure 5-6 EXORset Address Map

The address decoder circuit consists of 2 pre-patterned PROMs :

1 x MCM 7641 - 512 x 8 - tri-state (U50)
1 x MCM 7641 - 512 x 8 - tri-state (U51)

The PROMs decode the addresses AA8 through AA15. The smallest possible decoded address range is therefore 256 bytes. Each PROM contains two independent patterns which can be selected by means of the PROM address A8. This line is connected to the PIA3 (U109) PB0 line. This makes it possible to switch from one map to an alternate map under operator control. Tables 5-1 and 5-2 and show the PROM outputs as programmed in the standard EXORset.

U50 outputs O3 through O8 and U51 outputs O3 through O6 are used to select the various devices on the Main Controller Board (active low signals).

U51 outputs O1 and O2 are used as control signals :

--- INTADR (Internal Address) is low when a device located on the Main Controller Board is decoded. This signal, together with R/W´ and ROMREAD, is used to control the data bus buffers (U101).

--- ROMREAD is low when a E/ROM device located on the Main Controller Board is decoded. This signal, together with R/W´ and INTADR prevents the data buffers from turning on if an attempt is made to write into an E/ROM device.

A 74LS138 (U49) device is used for address decoding of the I/O devices. Each output decodes a 32 byte address range, from a base address defined by the PROM U50 O6 output. Each decoder output selects one I/O device, as shown in Table 5-3. The first address of each 32 bytes block is used as base address for the corresponding I/O device.

Table 5-1 Address Decode PROM U50 Outputs

4K x 8 EPROMS

U50	O8	O7	O6	O5	O4	O3	O2	O1	PROM ADDR.	DEC.ADDR.	SELECTS
MAP1	0	1	1	1	1	1	1	1	1F0-1FF	F000-FFFF	U45
	1	1	0	1	1	1	1	1	1EF	EF00-EFFF	U49
	1	1	1	1	1	1	1	1	1E8-1EE	E800-EEFF	-
	1	1	1	0	1	1	1	1	1E0-1E7	E000-E7FF	U70,U71,U72,U73
	1	1	1	1	1	1	1	1	1D0-1DF	D000-DFFF	U46 (4K EPROM)
	1	1	1	1	1	1	1	1	100-1CF	0000-CFFF	-
MAP2	0	1	1	1	1	1	1	1	0F0-0FF	F000-FFFF	U45
	1	1	0	1	1	1	1	1	0EF	EF00-EFFF	U49
	1	1	1	1	1	1	1	1	0E8-0EE	E800-EEFF	-
	1	1	1	0	1	1	1	1	0E0-0E7	E000-E7FF	U70,U71,U72,U73
	1	0	1	1	1	1	1	1	0D0-0DF	D000-DFFF	U46 (4K EPROM)
	1	1	1	1	0	1	1	1	0C0-0CF	C000-CFFF	U47 (4K EPROM)
	1	1	1	1	1	0	1	1	0B0-0BF	B000-BFFF	U48 (4K EPROM)
	1	1	1	1	1	1	1	1	000-0AF	0000-AFFF	-

8K x 8 EPROMS

U50	O8	O7	O6	O5	O4	O3	O2	O1	PROM ADDR.	DEC.ADDR.	SELECTS
MAP1	0	1	1	1	1	1	1	1	1F0-1FF	F000-FFFF	U45
	1	1	0	1	1	1	1	1	1EF	EF00-EFFF	U49
	1	1	1	1	1	1	1	1	1E8-1EE	E800-EEFF	-
	1	1	1	0	1	1	1	1	1E0-1E7	E000-E7FF	U70,U71,U72,U73
	1	1	1	1	1	1	1	1	1C0-1DF	C000-DFFF	U46 (8K EPROM)
	1	1	1	1	1	1	1	1	100-1BF	0000-BFFF	-
MAP2	0	1	1	1	1	1	1	1	0F0-0FF	F000-FFFF	U45
	1	1	0	1	1	1	1	1	0EF	EF00-EFFF	U49
	1	1	1	1	1	1	1	1	0E8-0EE	E800-EEFF	-
	1	1	1	0	1	1	1	1	0E0-0E7	E000-E7FF	U70,U71,U72,U73
	1	0	1	1	1	1	1	1	0C0-0DF	C000-DFFF	U46 (8K EPROM)
	1	1	1	1	0	1	1	1	0A0-0BF	A000-BFFF	U47 (8K EPROM)
	1	1	1	1	1	0	1	1	080-09F	8000-9FFF	U48 (8K EPROM)
	1	1	1	1	1	1	1	1	000-07F	0000-7FFF	-

2K x 8 EPROMS

U50	O8	O7	O6	O5	O4	O3	O2	O1	PROM ADDR.	DEC.ADDR.	SELECTS
MAP1	0	1	1	1	1	1	1	1	1F0-1FF	F000-FFFF	U45
	1	1	0	1	1	1	1	1	1EF	EF00-EFFF	U49
	1	1	1	1	1	1	1	1	1E8-1EE	E800-EEFF	-
	1	1	1	0	1	1	1	1	1E0-1E7	E000-E7FF	U70,U71,U72,U73
	1	1	1	1	1	1	1	1	1D8-1DF	D800-DFFF	U46 (2K EPROM)
	1	1	1	1	1	1	1	1	100-1CF	0000-D7FF	-
MAP2	0	1	1	1	1	1	1	1	0F0-0FF	F000-FFFF	U45
	1	1	0	1	1	1	1	1	0EF	EF00-EFFF	U49
	1	1	1	1	1	1	1	1	0E8-0EE	E800-EEFF	-
	1	1	1	0	1	1	1	1	0E0-0E7	E000-E7FF	U70,U71,U72,U73
	1	0	1	1	1	1	1	1	0D8-0DF	D800-DFFF	U46 (2K EPROM)
	1	1	1	1	0	1	1	1	0D0-0D7	D000-D7FF	U47 (2K EPROM)
	1	1	1	1	1	0	1	1	0C8-0CF	C800-CFFF	U48 (2K EPROM)
	1	1	1	1	1	1	1	1	000-0C7	0000-C7FF	-

Table 5-2 Address Decode PROM U51 Outputs

U51	O8	O7	O6	O5	O4	O3	O2	O1	PROM ADDR.	DEC.ADDR.	SELECTS
MAP1	1	1	1	1	1	1	0	0	1F0-1FF	F000-FFFF	
	1	1	1	1	1	1	1	0	1EF	EF00-EFFF	
	1	1	1	1	1	1	1	1	1E0-1EE	E000-EEFF	
	1	1	0	1	1	1	1	0	1C0-1DF	C000-DFFF	U13-U27 (Odd)
	1	1	1	0	1	1	1	0	180-1BF	8000-BFFF	U12-U26 (Even)
	1	1	1	1	0	1	1	0	140-17F	4000-7FFF	U29-U43 (Odd)
	1	1	1	1	1	0	1	0	100-13F	0000-3FFF	U28-U42 (Even)
MAP2	1	1	1	1	1	1	0	0	0F0-0FF	F000-FFFF	
	1	1	1	1	1	1	1	0	0EF	EF00-EFFF	
	1	1	1	1	1	1	1	1	0E0-0EE	E000-EEFF	
	1	1	1	1	1	1	0	0	0B0-0DF	B000-DFFF	(4K EPROM)
	1	1	1	0	1	1	1	0	080-0AF	8000-AFFF	U12-U26 (Even)
	1	1	1	1	0	1	1	0	040-07F	4000-7FFF	U29-U43 (Odd)
	1	1	1	1	1	0	1	0	000-03F	0000-3FFF	U28-U42 (Even)
MAP2	1	1	1	1	1	1	0	0	0F0-0FF	F000-FFFF	
	1	1	1	1	1	1	1	0	0EF	EF00-EFFF	
	1	1	1	1	1	1	1	1	0E0-0EE	E000-EEFF	
	1	1	1	1	1	1	0	0	080-0DF	8000-DFFF	(8K EPROM)
	1	1	1	1	0	1	1	0	040-07F	4000-7FFF	U29-U43 (Odd)
	1	1	1	1	1	0	1	0	000-03F	0000-3FFF	U28-U42 (Even)
MAP2	1	1	1	1	1	1	0	0	0F0-0FF	F000-FFFF	
	1	1	1	1	1	1	1	0	0EF	EF00-EFFF	
	1	1	1	1	1	1	1	1	0E0-0EE	E000-EEFF	
	1	1	1	1	1	1	0	0	0C8-0DF	C800-DFFF	(2K EPROM)
	1	1	0	1	1	1	1	0	0C0-0C7	C000-C7FF	U13-U27 (Odd)
	1	1	1	0	1	1	1	0	080-0BF	8000-BFFF	U12-U26 (Even)
	1	1	1	1	0	1	1	0	040-07F	4000-7FFF	U29-U43 (Odd)
	1	1	1	1	1	0	1	0	000-03F	0000-3FFF	U28-U42 (Even)

^ ^
^ INTADR
^
ROMREAD

Table 5-3 I/O Decoder U49 (74LS138) Outputs

O7	O6	O5	O4	O3	O2	O1	O0	DEC.ADDR.	SELECTS DEVICE	
1	1	1	1	1	1	1	1	EFE0-EFFF	not used	
1	1	1	1	1	1	1	1	EFC0-EFDF	not used	
1	1	0	1	1	1	1	1	EFA0-EFBF	PIA3 (control)	U109
1	1	1	0	1	1	1	1	EF80-EF9F	PIA2 (keyb.)	U115
1	1	1	1	0	1	1	1	EF60-EF7F	PIA1 (printer)	U7
1	1	1	1	1	0	1	1	EF40-EF5F	ACIA	U5
1	1	1	1	1	1	0	1	EF20-EF3F	PTM	U1
1	1	1	1	1	1	1	0	EF00-EF1F	CRTC	U100

Note : the first address of the decoded address range is the base address of each I/O device.

The EXORset address decoding PROM's are coded in order to implement a 56K-byte contiguous RAM block in map 1.

5.3.5 RAM Section

Two blocks of 32K bytes of dynamic RAM using MCM4116 devices are included on the Main Controller Board : U12 through U27 (block 0) and U28 through U43 (block 1). The access of the memory is time- multiplexed between the CRTC and the MPU. Table 5-4 shows the addresses generated by the CRTC and the MPU during each portion of one MPU cycle.

Table 5-4 Multiplexed RAM Addresses

ADDRESSES FROM MPU	CRTC		TO RAM
AA13....	MA9	]	
AA12....	MA8	]	
AA11....	MA7	]	COLUMN
AA10....	MA6	]	
AA9	RA3	]	
AA8	RA2	)	
AA7	RA1	)	ROW
AA6	RA0	)	
AA5	MA5	]	COLUMN
AA4	MA4	)	
AA3	MA3	)	ROW
AA2	MA2	)	
AA1	MA1	)	
AA0	MA0	]	COLUMN

The CRTC generates the memory row address and is therefore used as an inherent refresh counter. All of the 128 rows of each memory device are refreshed within 512 microseconds. The CRTC also generates the RAM column address, providing the graphic capability (see paragraph 5.2.7.3).

5.3.6 E/ROM Section

The EXORset Main Controller Board provides 4 sockets for up to 32K bytes of E/ROM devices. However, 1 socket (U45) is supplied already populated with EXORbug monitor firmware on an MCM2732. The three free sockets (U46-U48) provide space for up to 24K bytes of user software on MCM2716, MCM68316 MCM68332 or MCM68364 devices. Refer also to the description of jumper fields K10, K11, K12, K13, K21 and K22 in Chapter 2

and to the address decoding tables 5-1 and 5-2 in this Chapter.

5.3.7 Display Section

5.3.7.1 General Description

The display section consists of the MC6845 CRT Controller, the alphanumeric display and scratchpad RAM, the synchronization logic, the alphanumeric and graphic shift registers, the video mixer and the character generator EPROM.

The 2K-byte alphanumeric display RAM uses 4 x MCM2114 1K x 4 static RAM devices. 1760 bytes (80 characters x 22 lines) are actually used as display memory, leaving 288 bytes free for the system scratchpad.

5.3.7.2 Alphanumeric Display

At the display data rate needed to display 80 characters per line, two characters must be removed from the display memory at each MPU cycle. The display memory is split into two blocks, an "odd" block and an "even" block, and interleaved to appear as an array of 2K x 8 bits to the MPU and 1K of 16 bits to the CRTC. The MPU and the CRTC access the display RAM in a multiplexed mode, as shown in Table 5-5.

Table 5-5 Multiplexed Alphanumeric Display RAM Addresses

ADDRESSES FROM MPU	CRTC	TO RAM
AA10....	MA10	AAA10
AA9	MA9	AAA9
AA8	MA8	AAA8
AA7	MA7	AAA7
AA6	MA6	AAA6
AA5	MA5	AA5
AA4	MA4	AA4
AA3	MA3	AA3
AA2	MA2	AA2
AA1	MA1	AA1

The MPU address line A0 is not used as part of the alphanumeric memory address, but rather is used to gate the chip select into either the even or odd bank of the array. If address line A0 is low, it will select the even bank of memory, when high it will select the odd bank of memory. Two 74LS640's (U60, U59) form a bidirectional bus switch for the data lines. The R/W' line controls the direction of the data transfer. Two 74LS374 (U61, U62) 8-bit latches latch the 16-bit data flowing to the CRT. The output of these latches is three-state and is controlled by the CRTC MA0 line, delayed by one character (=MA0SYNC).

All the timing is derived from the central oscillator. The frequency of this oscillator is at the dot clock rate and is determined by the system parameters. This clock is 16 MHz for a 80 character per line display and 8 MHz for a 40 character per line display. The one or the other clock signal is selected by means of the 74LS157 (U102) multiplexer, controlled by the PIA3 (U109) PB1 line.

Table 5-6 and Table 5-7 show the relationship between the character position on the screen and its actual address in the alphanumeric RAM (offset from the alphanumeric RAM base address). In the standard EXORset the alphanumeric display RAM base address is E000.

Note that in the 40 characters per line format, columns 41 through 64 must be filled with blanks (ASCII $20). (This is automatically done when under EXORbug control). Retrace takes place only after column 64. This display format is necessary to allow the 40 characters alphanumeric and the graphic display to be superimposed.

Table 5-6 Alphanumeric Display Characters Location
(hex offset from alphanumeric RAM base address)
40 characters/line by 16 lines format

	COL1	COL2	COL3	.....	COL40	COL41	COL64
ROW1	00	01	02	.....	27	28 ...	3F
ROW2	40	41	42	.....	67	68 ...	7F
ROW3	80	81	82	.....	A7	A8 ...	BF
.	.	.	.		.	.	.
.	.	.	.		.	.	.
.	.	.	.		.	.	.
.	.	.	.		.	.	.
.	.	.	.		.	.	.
ROW16	3C0	3C1	3C2	.....	3E7	3E8 ...	3FF

<------ DISPLAYED CHARACTERS ------> <-BLANKED->

Table 5-7 Alphanumeric Display Characters Location
(hex offset from alphanumeric RAM base address)
80 characters/line by 22 lines format

	COL1	COL2	COL3	.....	COL80
ROW1	00	01	02	.....	4F
ROW2	50	51	52	.....	9F
ROW3	A0	A1	A2	.....	EF
.	.	.	.		.
.	.	.	.		.
.	.	.	.		.
.	.	.	.		.
.	.	.	.		.
ROW22	690	691	692	.....	6DF

<---------- DISPLAYED CHARACTERS ---------->

5.3.7.3 Graphic Display

The EXORset provides a high resolution full graphic capability, in a raster of 320 dots (40 bytes) by 256 scans.

The CRTC accesses the dynamic RAM cyclically, once per MPU cycle. The RAS signal is generated at each cycle, allowing the dynamic memory refresh to be performed. If a CAS signal is also applied to one of the 16K RAM blocks, the contents of this RAM block will appear on the data outputs. These data are loaded from the inverted data bus into the 74LS165 (U104) shift register. Provided the graphic function is enabled (PIA3 (U109) PB3 line low), the 8-bit word will be shifted out to the CRT, one memory bit controlling one dot in the graphic matrix. Table 5-8 shows the matrix coordinates and the corresponding byte addresses in the graphic memory.

Note that bytes 40 to 63 (columns 321 to 512) should not be displayed and must be filled with blanks (zeroes) by software.

Table 5-8 Graphic Display Matrix
(hex offset from the graphic RAM base address)

	COL1 ... COL8 [BIT7 ... BIT0]	COL9 ... COL16 [BIT7 ... BIT0]	.....	COL313 . COL320 [BIT7 ... BIT0]
ROW1	00	01	.....	27
ROW2	40	41	.....	67
ROW3	80	81	.....	A7
ROW4	C0	C1	.....	E7
.	.	.		.
.	.	.		.
.	.	.		.
.	.	.		.
.	.	.		.
ROW256	3FC0	3FC1	.....	3FE7

5.3.7.4 Video Mixer

The video mixer combines the horizontal sync, vertical sync, and video data. The video data includes the character data, the row and retrace blanking. The video mixer also combines the graphic and alphanumeric data. If both functions are selected together, the graphic output signal is automatically switched to half-intensity, to make the text easily distinguishable from the graphic pattern. The video signal is output to connectors J6 and J8. Connector J8 makes provision for seperate horizontal and vertical signals to be output.

5.3.7.5 Character Generator EPROM

The MCM2708 (U63) allows the user to modify the character set by reprogamming. The charcters are built up on a 5 x 8 matrix with the top row blanked giving effectively a 5 x 7 matrix. Table 5-9 gives the addresses of the character set in the EPROM. Table 5-10 gives the bit pattern of the letter I as a programming example.

Table 5-9 Character Generator EPROM addresses

CHARACTER	ASCII CODE	PROM ADDRESS
NUL	00	00-07
SOH	01	08-0F
STX	02	10-17
ETX	03	18-1F
EOT	04	20-27
ENQ	05	28-2F
ACK	06	30-37
BEL	07	38-3F
BS	08	40-47
HT	09	48-4F
LF	0A	50-57
VT	0B	58-5F
FF	0C	60-67
RETURN	0D	68-6F
SO	0E	70-77
SI	0F	78-7F
DLE	10	80-87
DC1	11	88-8F
DC2	12	90-97
DC3	13	98-9F
DC4	14	A0-A7
NAK	15	A8-AF

SYN	16	B0-B7
ETB	17	B8-BF
CAN	18	C0-C7
EM	19	C8-CF
SUB	1A	D0-D7
ESC	1B	D8-DF
FS	1C	E0-E7
GS	1D	E8-EF
RS	1E	F0-F7
US	1F	F8-FF
SPACE	20	100-107
!	21	108-10F
"	22	110-117
#	23	118-11F
$	24	120-127
%	25	128-12F
&	26	130-137
'	27	138-13F
(	28	140-147
)	29	148-14F
*	2A	150-157
+	2B	158-15F
,	2C	160-167
-	2D	168-16F
.	2E	170-177
/	2F	178-17F
0	30	180-187
1	31	188-18F
2	32	190-197
3	33	198-19F
4	34	1A0-1A7
5	35	1A8-1AF
6	36	1B0-1B7
7	37	1B8-1BF
8	38	1C0-1C7
9	39	1C8-1CF
:	3A	1D0-1D7
;	3B	1D8-1DF
<	3C	1E0-1E7
=	3D	1E8-1EF
>	3E	1F0-1F7
?	3F	1F8-1FF
@	40	200-207
A	41	208-20F
B	42	210-217
C	43	218-21F
D	44	220-227
E	45	228-22F
F	46	230-237
G	47	238-23F
H	48	240-247
I	49	248-24F
J	4A	250-257
K	4B	258-25F
L	4C	260-267
M	4D	268-26F
N	4E	270-277
O	4F	278-27F
P	50	280-287
Q	51	288-28F

R	52	290-297
S	53	298-29F
T	54	2A0-2A7
U	55	2A8-2AF
V	56	2B0-2B7
W	57	2B8-2BF
X	58	2C0-2C7
Y	59	2C8-2CF
Z	5A	2D0-2D7
[	5B	2D8-2DF
\	5C	2E0-2E7
]	5D	2E8-2EF
^	5E	2F0-2F7
	5F	2F8-2FF
`	60	300-307
a	61	308-30F
b	62	310-317
c	63	318-31F
d	64	320-327
e	65	328-32F
f	66	330-337
g	67	338-33F
h	68	340-347
i	69	348-34F
j	6A	350-357
k	6B	358-35F
l	6C	360-367
m	6D	368-36F
n	6E	370-377
o	6F	378-37F
p	70	380-387
q	71	388-38F
r	72	390-397
s	73	398-39F
t	74	3A0-3A7
u	75	3A8-3AF
v	76	3B0-3B7
w	77	3B8-3BF
x	78	3C0-3C7
y	79	3C8-3CF
z	7A	3D0-3D7
{	7B	3D8-3DF
|	7C	3E0-3E7
}	7D	3E8-3EF
~	7E	3F0-3F7
DEL	7F	3F8-3FF

Table 5-10 Character Generator Coding Example

ASCII $49 = I		
PROM ADDRESS	VALUE	
	HEX	BINARY
248	00	00000000
249	0E	00001110
24A	04	00000100
24B	04	00000100
24C	04	00000100
24D	04	00000100
24E	04	00000100
24F	0E	00001110

5.3.7.6 Light Pen Interface

The light pen connector (J7) allows the user to optionally connect a light pen to the EXORset. The pin assignments are described in Table 2-7. The light pen strobe (LPSTR) is input to the MC6845 CRTC (U100). When the light pen detects a beam, the address is stored in the light pen registers R16, R17 of the MC6845. This enables the user to make changes in the display by placing the light pen on the screen next to the character position in which he is interested. The next time the electron beam hits where the light pen is, the CRTC will capture the address (character position) where it occurs. The user can now have his program read the light pen register and make whatever changes are desired. If the light pen response is slow compared to the speed of the processor, the captured address should be offset to determine the actual address.

5.3.8 Keyboard and Keyboard Interface

The keyboard assembly consists of a non-decoded full ASCII key array and a 16-function key array. Figure 5-7 shows the keyboard matrix organization. Refer to Table 2-1 and Table 2-2 for pin assignments.

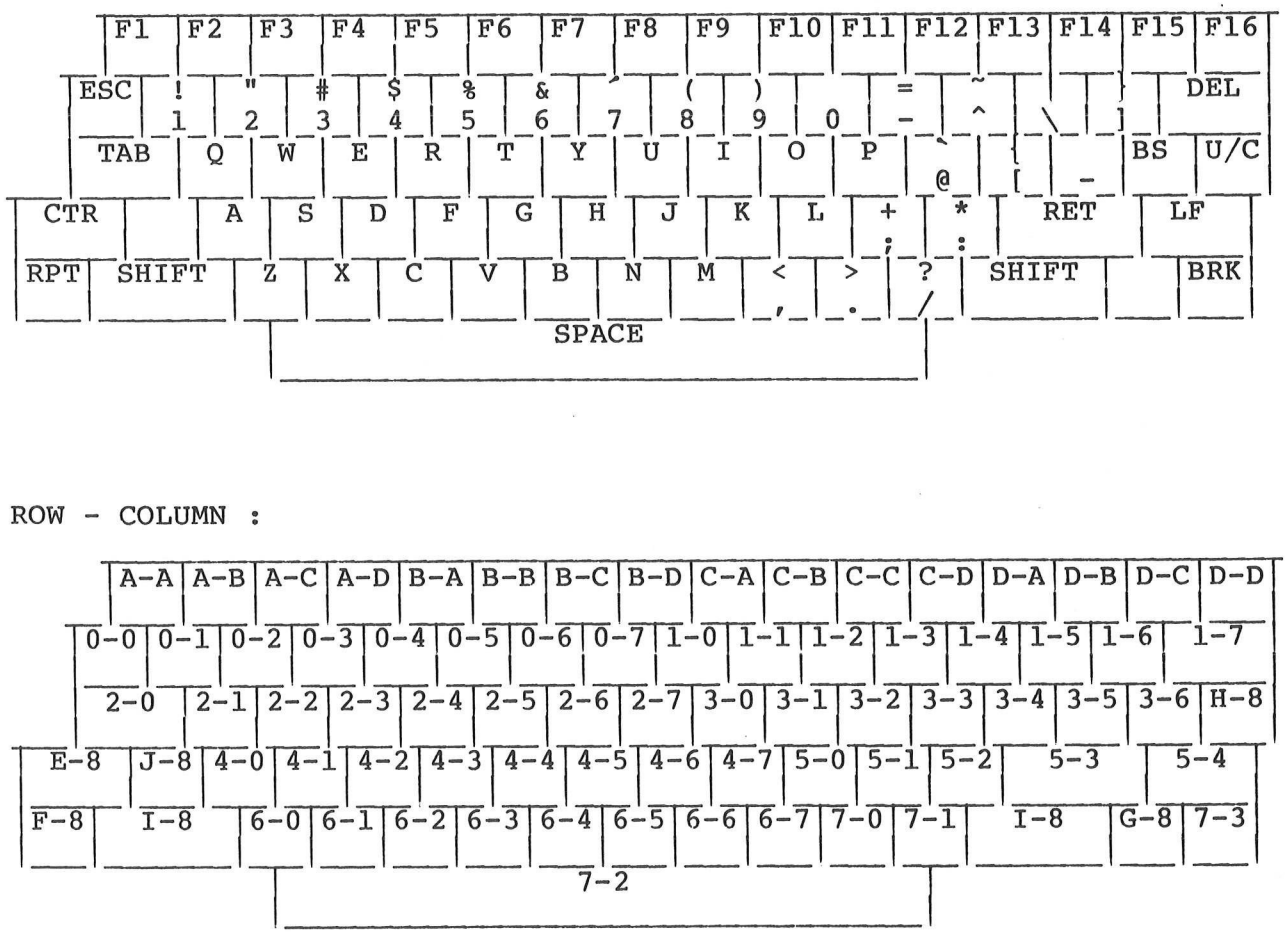


Figure 5-7 Keyboard Matrix Organization

The ASCII matrix outputs are decoded on the Main Controller Board using a specialized one-chip microprocessor. The SC80241P Keyboard Encoder is a pre-programmed MC3870 microprocessor, used to scan a 64 key keyboard. The keyboard is scanned by a 74LS156 open collector 1 of 8 decoder (U118) driven by 3 bits of port 0. The closed keys in the 8 x 8 array are input to port 1, and are debounced and encoded by software. The ASCII code is available at port 4, along with an active low STROBE pulse. The output from port 4 can be restrained if the READY line is held low. An 8-bit FIFO buffers the output until the READY line returns to a high level. In the EXORset, READY is always held high, but PIA2 (U115) PB7 can be used to implement this function, if desired.

The 16-function key matrix outputs are encoded using half a MC6821 PIA (U115, A-side), under application software control (e.g. BASIC-M "ON KEY" statement).

5.3.9 Debug Circuitry

The debug circuitry consists basically of the PIA3 (U109) (A-side), the address comparator (U56), the 4K x 1 MCM66L41 breakpoint memory (U74) and the run-one-instruction counter (U107).

The basic idea of the breakpoint circuitry is to provide a ninth bit in parallel with the system memory. A breakpoint is set by writing a zero into the desired memory location of the breakpoint RAM. When the breakpoint address is encountered during user program execution, the breakpoint RAM outputs a zero, which in turn generates an NMI to the processor. Up to 4K breakpoints may be inserted in a 4K address window (page). The EXORbug monitor controls the breakpoint circuitry through the PIA3 (U109). Lines PA4 through PA7 are set to the high-order address value of the first breakpoint address entered by the operator. These lines ar compared with the address lines A12 through A15. When a match occurs, the comparator output activates the breakpoint RAM. Two lines (PA0 and PA1) are used to write into the breakpoint RAM. One line (PA2) is used to optionally allow breakpoints to be active only during the MPU write cycles.

A hardware trace function is provided that permits a user program to be executed one instruction at a time. The trace is initiated when the system is in an NMI routine from either a previous trace or having run a breakpoint. The user program counter value saved on the stack is pointing to the next user instruction to be executed. Before executing the Return from Interrupt (RTI) instruction, the trace counter is started via PA3 of PIA3. The RTI instruction is then executed, causing the MPU to reload its registers from the stack and begin executing the next user instruction. In the mean time the trace counter is counting machine cycles. The sixteenth cycle after the counter is started will be a fetch of the op-code for the next user instruction (RTI takes 15 cycles to execute). The trace counter detects the fifteenth count and generates a pulse to CA2 of PIA3. After one cycle delay, an NMI is generated to the MPU. The NMI is low at the end of the first cycle of the instruction. This insures that only one instruction is executed. The first task of the NMI service routine is to set PA3 line back high, resetting the trace counter in readiness for the next step.

5.3.10 Serial Interface

The serial interface port (J3) provide an jumper configurable serial I/O interface for RS232C,RS422,RS423 and current loop (using the M68MM11 adapter). The Baud rate is jumper selectable from 50-19600 baud. A detailed description of this interface is given in Section 2.6. and in Table 2-3. Refer also to the descriptions of jumper fields K4, K8 and K20 in Chapter 2.

5.3.11 Parallel Interface

The parallel interface using the PIA1 (U7) provides the interface between the EXORset and a Centronics-Type printer.

Data on the PIA1 peripheral interface lines PA0 through PA7 is output through the drivers and appears at connector J4 as PD (Peripheral Data)1 through PD8. This data is clocked by the DATA STROBE active low output pulse from the PIA1 CA2 line. ACKNLG (Acknowledge) is a low-level signal from the printer to the PIA1 CA1 line indicating that a character has been received. Status signals from the printer are received on PB0, PB1, PB2, CB1 and CB2.

5.4 MINI-FLOPPY DISK CONTROLLER BOARD

5.4.1 Introduction

The Mini-Floppy Disk Controller Board consists of a MC6843 Floppy Disk Controller (FDC), a 1024 x 8-bit E/ROM containing the resident driver firmware program, a drive select circuitry, a 16K bytes RAM block, a three-state bus interface circuitry, and the necessary address decoding logic to permit accessing from the EXORset bus.

The Mini-Floppy Disk Controller Module occupies 17424 address locations, divided as follows :

--- E800 through EBFF are assigned to the Resident Driver Firmware

--- EC00 through EC07 are assigned to the MC6843 FDC

--- EC08 through EC0F are assigned to the drive select latches

--- 8000 through BFFF are assigned to the 16K RAM block

5.4.2 FDC and Data Recovery

The MC6843 FDC (Floppy Disk Controller) (U21) performs all read / write and control operations needed to transfer data to / from the mini-disk drives. Refer to the FDC data sheet for a detailed description of the FDC operation.

A phase locked loop data recovery circuit is used to provide the separated data and clocks needed by the FDC. The PLL data recovery circuit consists of a frequency / phase detector circuit (U15) with filter network, a voltage controlled oscillator (U26), two synchronous 4-bit counters (U2, U16), and five flip-flops (U17, U27, U28). Gate U1 is inserted in the loop only for test purposes. The center frequency of the VCO is normally 4.0 MHz with a lock range of 3.8 to 4.2 MHz. Lockup time will be less than 384 microseconds.

The Raw Data signal from the disk drive unit is a combination of a 250 KHz clock signal and data. This signal is applied to an input flip-flop circuit consisting of two serially connected flip-flops (U17). This circuit generates a negative output pulse with a pulse width equal to one VCO time period (approximately 0.250 microseconds). This negative pulse is used to preset the first reference counter (U16) with a 9 and to set the output of the first data flip-flop to a logic high level.

In the data format used in the disk system, the incoming data stream can have only one consecutive pulse missing. By loading the first reference counter with a 9, it will produce

a positive output transition within 15 VCO pulses (3.750 microseconds), thus generating a clock edge even if the data pulse is missing. This reference counter will also produce a carryout pulse on the 16th VCO pulse (4 microseconds). This pulse is then compared with the carryout output of the second reference counter (U2) by the frequency / phase detector, thus providing a reference for the VCO.

The negative output transitions of the first reference counter are inverted and used to clock the first data flip-flop (U27), causing the output to change to a logic low level. If another data pulse is present in the incoming data stream, then the first data flip-flop is once again set by the input flip-flop circuit. However, if no data is present, then the output of the first data flip-flop will remain at a logic low level until set by a data pulse, which must occur within 64 microseconds of the last data pulse in order to avoid initiating an error message. When the data pulse is set and the first data flip-flop is set, the next output pulse produced by the reference counter causes the second data flip-flop to toggle, producing the NRZ (Non-Return to Zero) data (RDT) required by the FDC.

5.4.3 16K RAM Block

Not used.

5.4.4 Mini-Floppy Drives Selection Circuitry

Data bits D0´ through D4´ are latched into two addressable latches (U20, U29) responding to address EC08 (ambiguous addresses up to EC0F). These five bits are used to select the mini-disk drives and control the drive motors. Table 5-11 shows the function of each bit.

Table 5-11 Mini-Floppy Drives Select Lines

D4´	D3´	D2´ (1)	D1´	D0´	FUNCTION
0	1	X	0	0	Drive 0 selected
0	1	X	0	1	Drive 1 selected
0	1	X	1	0	Drive 2 selected (not used)
0	1	X	1	1	Drive 3 selected (not used)
0	0	X	X	X	All drives desselected
1	0	X	X	X	Drive motors off

X = don´t care
(1) provision for double-sided diskettes

5.4.5 E/ROM Resident Driver Firmware

The Resident Driver Firmware stored in the E/ROM device is used to control all of the Mini-Floppy Disk System hardware operations.

5.4.5.1 Initialization

When the Mini-Floppy Disk System is initially accessed by the user, a defined initialization procedure must be used. When the Mini-Floppy Disk System is used with XDOS, this initialization procedure is automatically performed when the command XDOS is entered by the user. However, if the Mini-Floppy Disk System is used in conjunction with a user designed system, the user must include this initialization procedure in his program. Parameters for the initialization procedure are stored in nine sequential bytes, as described in Table 5-12.

5.4.5.2 Error Messages

The ninth byte (FDSTAT) of the initialization procedure contains a hexadecimal error message (from 30 to 39). If no error occurred during the disk operation, then the carry bit will be reset and the FDSTAT byte will contain the hexadecimal number 30 (ASCII 0) : no error. However, if an error does occur, then the carry bit will be set and the FDSTAT byte will contain a hexadecimal number of 31 to 39 (ASCII 1 to 9) that relates to a specific error message. If an error occurs, any disk operation in progress is halted, and control is returned to the user. Each of the error messages (and their corresponding hexadecimal and ASCII characters) is explained in Table 5-13.

Table 5-12 Initialization Parameters for a User Prepared DOS Program

BYTE	NAME	DEFINITION
0	CURDRV	CURRENT DRIVE - This byte contains the number of the selected drive unit (0 or 1).
1,2	STRSCT	STARTING SECTOR - These two bytes contain the physical sector number of the first sector to be used (starting sector). For single density mini-disks, this starting sector number must be between 0 and 27F (hex), inclusive.
3,4	NUMSCT	NUMBER OF SECTORS - These two bytes contain the number of sectors to be used. This number includes a partial sector read, if one is requested. For single density mini-disks, the sum of the numbers contained in the STRSCT byte and the NUMSCT byte cannot be greater than 280 (hex) when read or write operations are requested.
5	LSCTLN	LAST SECTOR LENGTH - This byte, during read into memory operations, contains the number of bytes to be read from the last sector to be used. This number should be between 1 and 128, since each sector contains 128 bytes. If this number is not between 1 and 128 (inclusively), a CRC error will result when the last sector is read.
6,7	CURADR	CURRENT ADDRESS - These two bytes contain the first address from/to which data is to be read/written during disk read/write operations. The Resident Driver Firmware automatically updates this entry after each sector is read/written. During write test operations, these two bytes contain the address of a one byte data buffer.
8	FDSTAT	FLOPPY DISK STATUS - This byte contains a status indicator returned from the Resident Driver Firmware. If an error occurred during a disk operation, the carry bit will be set on return to the caller, and this byte will contain a number indicating the type of error. If no error occurs, then the carry will be reset and this byte will contain the hexadecimal number 30 (ASCII 0).

Table 5-13 Disk Error Messages

FDSTAT (HEX)	ERROR CODE	DESCRIPTION / POSSIBLE CAUSE
30	E0	NO ERRORS - This status indication is returned when no errors have occurred in the disk operation. On return to the user, the carry bit is cleared.
31	E1	DATA CRC ERROR - This status is returned when the CRC following the data is in error. This error would occur after the sector has been read and, if appropriate, written into memory. The CURADR byte will not be updated for the sector with the error. In multiple sector operations, the equation listed at the end of this table can be used to determine the sector number of the physical sector in which the error occured. Possible causes of this error include miswriting and misreading the data and/or CRC. If the error occurred during WRVERF or RWTEST, the sector should be rewritten. Otherwise, another attempt should be made to read the sector. The Disk Driver will attempt to read the sector 5 times before returning this error.
32	E2	DISK WRITE PROTECTED - This status is returned whenever an attempt is made to write to a diskette that is write protected (the diskette has the write protection tab punched out). Note that during XDOS initialization, certain information is written onto the diskette. The write protection tab must be covered with a piece of opaque tape to allow writing on the diskette.
33	E3	DISK NOT READY - This status is returned when an operation is attempted with a disk that is not ready. Possible causes of the not ready status include the drive unit door is not closed, the diskette is not up to speed, the diskette has been inserted into the drive with the wrong orientation, the drive interface cable is not properly inserted.
34	E4	READ DELETED DATA MARK - This status is returned when an attempt is made to read a sector that is prefaced by a deleted data mark. The sector will not be read into memory or written onto the diskette, and the CURADR

		byte will not be updated for the sector in error. The equation listed at the end of this table can be used to determine the physical sector in error when this error occurs during a multiple sector operation. A possible cause of this status is that a deleted data mark was intentionally written to the sector.
35	E5	TIMEOUT - This status is returned when the track address has not been found after five attempts. Possible causes of this error include attempting to read or write a bad track or sector or an unformatted disk. Reformatting the disk may eliminate this error. This error may also occur as a result of a bad head alignment.
36	E6	INVALID DISK ADDRESS - This error occurs when the sum of the STRSCT and NUMSCT bytes are greater than the number of sectors on the disk. The RESTOR command does not check for this error.
37	E7	SEEK ERROR - This error occurs if a restore is completed incorrectly or track 0 is found before a seek operation is completed. This error may occur during a restore if the drive is not connected to the controller.
38	E8	DATA MARK ERROR - This error occurs if a valid data mark for the sector being read has not been found. This error message occurs before the sector is read, and prevents the sector from being read. The CURADR byte is not updated for the sector in error. The equation provided at the end of this table can be used to determine the number of the physical sector in error, when this error occurs during a multiple sector operation. The Resident Driver Firmware will attempt to read the sector in error five times before returning this error message. Possible causes of this error include misreading and miswriting the disk.
39	E9	ADDRESS MARK CRC ERROR - This error occurs when the CRC of an address mark is incorrect. This error occurs before the sector is read or written, and stops the operation in progress. The CURADR byte is not updated for the sector in error. The equation provided at the end of this table can be used to determine the sector number in error, when this error occurs in a multiple sector operation.

	Possible causes of this error include miswriting the address mark or its CRC when formatting the disk, and misreading the address mark or its CRC. The Resident Driver Firmware will attempt to read the sector in error five times before returning this error message.
EQUATION :	PSNE = STRSCT + NUMSCT - SCTCNT - 1
where :	PSNE is the sector number of the physical sector in error. STRSCT is the contents of the STRSCT byte. NUMSCT is the contents of the NUMSCT byte. SCTCNT is the two byte value contained in locations $B and $C. This value is set equal to the contents of the NUMSCT byte at the beginning of a disk read or write operation, and is then decremented before each sector operation.

5.4.5.3 Resident Driver Firmware Entry Points

Various entry points (addresses) are available to the user to perform specific operations contained within the E/ROM Resident Driver Firmware. These entry points are provided in Table 5-14. This table is divided into three parts : the initialization and error check routines part, the disk operation routines part, and the line printer driver routines part. For all of the firmware entry points described below, the content of the registers is unspecified both upon entry and exit from the subroutine (except where otherwise indicated). Each entry point is accessed by executing a "jump to subroutine" instruction (JSR). The parameters must have been set up in RAM as indicated for each specific function. Upon entry to a disk routine, all MPU registers are saved, as well as the user's top of memory vector. Before returning from a disk routine, all registers and the top of memory vector are restored. If an error occurred, the FDSTAT byte will be changed accordingly, and the carry bit set.

Table 5-14 Resident Driver Firmware Entry Points

NAME	ADDR	FUNCTION
		INITIALIZATION AND ERROR CHECK ROUTINES :
OSLOAD	E800	This entry bootloads the disk operating system, initializes the stack pointer and drive electronics, and restores the head position of drive 0 to track 0. The bootloader and operating system's retrieval information block from sectors 23 and 24 (decimal), respectively, of drive 0 are loaded into memory beginning at location 32 (decimal) (20 hex). Control is then passed to the bootloader by jumping to that location. If a disk error occurs, the error number is printed at the system console and control is returned to EXORbug. No user parameters need to be specified when the Resident Driver Firmware is entered at this entry point. The firmware will initialize all the required parameters.
FDINIT	E822	This subroutine initializes the FDC. No user parameters are required by this subroutine and none are modified by it. This subroutine does not change location FDSTAT or the state of the carry bit.
CHKERR	E853	This subroutine checks for a disk error if called immediately after return from a disk operation by checking the carry flag. The subroutine just returns to the user if no error occurred (carry clear). If an error did occur (carry set), then the subroutine prints an E followed by the contents of FDSTAT (in ASCII) and two spaces at the system console. It then gives control to EXORbug. Other than FDSTAT, no user parameters are required. (If a disk error occurs, the Resident Driver Firmware will load the appropriate data into FDSTAT). CHKERR does not modify any user parameters.
PRNTER	E85A	This subroutine prints an E at the system console followed by the contents of FDSTAT (in ASCII) and two spaces. FDSTAT is the only user parameter required by PRNTER. It does not modify any user parameters.

DISK OPERATION ROUTINES :

READSC	E869	This entry causes the number of sectors (beginning with STRSCT of CURDRV) to be read from the NUMSCT byte into memory beginning at CURADR. The CURADR byte is updated to the next address to be written to after each sector is read. This entry point initializes the LSCTLN byte to 128 (decimal) so that all of the last sector read will be written to memory. This routine does not change CURDRV, STRSCT, or NUMSCT.
READPS	E86D	This entry causes the number of sectors (beginning with STRSCT of CURDRV) to be read into memory beginning at CURADR. The CURADR byte is updated to the next address to be written to after each sector is read. This entry point does not change LSCTLN, so that only a portion of the last sector read may be written to memory. This routine does not change CURDRV, STRSCT, NUMSCT, or LSCTLN.
RDCRC	E86F	This entry causes NUMSCT sectors beginning with STRSCT of CURDRV to be read to check their CRC's. The sectors are not written to memory. This routine does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.
RWTEST	E872	This entry point causes the data at CURADR and CURADR+1 to be written to bytes of NUMSCT sectors beginning with STRSCT of CURDRV. After all of the sectors have been written, they are read back to check their CRC's. This routine does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.
RESTOR	E875	This entry point causes the head of CURDRV to be restored to track 0. The drive must be ready or restore will return an error. RESTOR does not verify that STRSCT and NUMSCT are valid. RESTOR is used to position the drive's head at known track before using the drive. (The OSLOAD routine restores drive 0). RESTOR does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.
SEEK	E878	This entry point causes the head of CURDRV to be positioned at the track containing STRSCT. This routine does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.
WRTEST	E87B	This entry point causes the byte of data pointed to by the address in CURADR and CURADR+1 to be written to bytes of NUMSCT sectors beginning with STRSCT of CURDRV. This routine does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.

WRDDAM	E87E	This entry point causes a deleted data address mark to be written to NUMSCT sectors beginning with STRSCT of CURDRV. This routine does not change CURDRV, STRSCT, NUMSCT, LSCTLN, or CURADR.
WRVERF	E881	This entry point causes NUMSCT sectors beginning with STRSCT of CURDRV to be written from memory beginning at CURADR. CURADR is updated to the address of the next byte to be read from after each sector has been written. After all of the sectors have been written, they are read back and their CRC's are verified as in RDCRC. This routine does not change CURDRV, STRSCT, NUMSCT, or LSCTLN.
WRITSC	E884	This entry point causes NUMSCT sectors beginning with STRSCT of CURDRV to be written from memory beginning at CURADR. CURADR is updated to the address of the next byte to be read from after each sector has been written. This routine does not change CURDRV, STRSCT, NUMSCT, or LSCTLN.
		LINE PRINTER ROUTINES : ----------
LPINIT	EBC0	This entry point exists only to keep MDOS III compatibility. In MDOS III systems, this subroutine initializes the PIA interfacing with the line printer from a reset condition. In the EXORset, this is done by the EXORbug monitor at RESTART. Therefore LPINIT returns only to the caller program.
LIST	EBCC	This subroutine sends the contents of the A accumulator to the line printer. If a printer error occurred, carry is set on return to the caller. The LIST routine detects the paper empty and printer not selected conditions as printer errors.
LDATA	EBE4	This subroutine sends a character string pointed to by the index register X and terminated by a 04 to the line printer.
LDATA1	EBF2	This subroutine performs the same as LDATA except that this subroutine does not print a carriage return and line feed prior to string. It also uses LIST to send characters to the printer.

5.3.5.4 Disk Mini-Diagnostic Routines

The interactive disk test program included in the disk driver E/ROM is described in CHAPTER 3, paragraph 3.5.2. A Disk Mini-Diagnostic (DMD) routine is also available in the E/ROM resident firmware. This routine permits the user to easily execute any disk function a single time and print the status or to continuously execute disk functions and keep an error count in a RAM location. The locations used by the DMD are listed (by name) in Table 5-15. Both single execution operations and continuous operations are described in the following steps.

1. Single Execution Operation

   In order to execute a disk function one time, set up the locations of CURDRV, STRSCT, NUMSCT, LSCTLN, and LDADDR as required for the function. Next, put the entry point address of the function into EXADDR and a non-zero value in ONECON. Then, by typing the EXORbug command EB98;G, the FDC will be initialized, CURDRV will be restored, and the disk function specified by EXADDR will be executed one time on CURDRV. Upon completion of the disk function or detection of an error, the status is printed at the console (the letter E followed by a single digit 0 to 9), and control is returned to EXORbug. Before starting the DMD, the stack pointer S should be set to a valid area by using the EXORbug command RS. (The EXORbug stack pointer value is acceptable).

   Example :

```
.0/xx 00 (LF)     Current drive 0
0001 xx 02 (LF)   Starting sector 200
0002 xx 00 (LF)
0003 xx 00 (LF)   Number of sectors 1
0004 xx 01 (LF)
0005 xx 40 (CR)   Last sector length 40
.20/ xx 01 (LF)   Buffer address 100
0021 xx 00 (LF)
0022 xx E8 (LF)   Read partial sector
0023 xx 6D (LF)
0024 xx FF (CR)   Execute routine once
.EB98;G E0        Execute ; no error
.
```

2. Continuous Execution Operation

In order to continuously execute a disk function, set up locations CURDRV, STRSCT, NUMSCT, LSCTLN and LDADDR as required for the function. Next, put the entry point address of the function into EXADDR and a zero into ONECON. Then, by typing either EB98;G (to start DMD at TOP) or EB90;G (to start DMD at CLRTOP, clear the two byte counters), the FDC will be initialized, CURDRV will be restored, and the disk function specified by EXADDR will be continuously executed on CURDRV until one of the two byte counters is incremented to 0. When a counter reaches 0, an E followed by an indication of the last disk status will be printed at the console, and control will be returned to EXORbug. The user can also cause DMD to stop on the first error of a given type by initializing the corresponding counter to FFFF and entering DMD at TOP.

Table 5-15 Disk Mini-Diagnostic Routines

NAME	ADDR	DEFINITION
CURDRV	00	Same as for normal disk operations.
STRSCT	01	Same as for normal disk operations.
NUMSCT	03	Same as for normal disk operations.
LSCTLN	05	Same as for normal disk operations.
CURADR	06	Set up by DMD from LDADDR before each execution of the requested disk function.
FDSTAT	08	Same as for normal disk operations.
LDADDR	20	These two bytes must be set up by the user with the data he would normally put at CURADR, DMD will update CURADR to LDADDR before each execution of the requested disk function.
EXADDR	22	These two bytes contain the address of the entry point of the disk function (READSC, WRVERF, etc.) to be executed by DMD.
ONECON	24	This byte contains a flag that indicates if the disk function is to be executed once or continuously. If the byte is zero, the disk function will be executed continuously. If the byte is non-zero, the disk function will be executed once.
	60-73	This area contains one two-byte counter for each possible status return from 0 to 9. For example, 60 and 61 contain a two-byte count of the 0 status returns, 62 and 63 contain a two-byte count of the 1 status returns, etc.
CLRTOP	EB90	This location is the entry address of DMD and clears the status counters.
TOP	EB98	This location is the entry address of DMD without clearing the status counters.

5.4.5.4 Recording Format

The format of the data recorded on the diskette is similar to the IBM 3740 format. Data is recorded on the diskette using frequency modulation techniques (each bit recorded on the diskette has an associated clock bit recorded with it). These clock and data bits (if present) are interleaved. By definition, a Bit Cell is the period between the leading edge of one clock bit and the leading edge of the next clock bit. (Thus, the Bit Cell is one clock bit and one data bit if the data bit is present).

When referring to serial data being written to or read from the disk drive, a byte is defined as eight consecutive Bit Cells. The most significant Bit Cell is defined as Bit Cell 0, and the least significant Bit Cell is defined as Bit Cell 7. During a write operation, Bit Cell 0 of each byte is transferred to the diskette first, with Bit Cell 7 being transferred last. Correspondingly, the most significant byte is transferred last. During read operations, Bit Cell 0 of each byte will be read from the diskette first, with Bit Cell 7 last. As with writing, the most significant byte will also be read from the diskette first.

The Mini-Floppy Drives are capable of recording up to 40 tracks of data. The tracks are numbered 0 to 39. Each track is made available to the recording head by moving the head with a stepper motor and carriage assembly controlled by the FDC. The diskette is rotated by the drive motor at a speed of 300 rpm. Table 5-16 shows the mini-disk track format, and Table 5-17 is the track / physical sector number conversion table.

Table 5-16 Mini-Disk Soft Sector Format

PHYSICAL START/END	PATTERN	NAME	
INDEX	80 x FF	Index gap.	x 1 (3)
	6 x 00	Sync bytes	x 16 (4)
	1 x FE (1) C7 (2)	Address mark	
	TRK	Track number	
	1 x 00		
	SEC	Sector number	
	1 x 00		
	2 x CRC	Address CRC (**)	
	11 x FF	Identifier gap	
	6 x 00	Sync bytes	
	1 x FB (1)(*) C7 (2)	Data mark	
	128 x DATA	Data	
	2 x CRC	Data CRC (**)	
	27 x FF	Data gap	
	37 x FF	Track gap	x 1 (5)
INDEX			

(1) Data pattern
(2) Clock pattern
(3) This field is written once at start of each track
(4) This field is repeated 16 times (one for each sector)
(5) This field is written once at the end of each track
(*) Deleted data mark : F8
(**) CRC polynomial : X^16 + X^12 + X^5 + 1

Table 5-17 Track / Physical Sector Conversion Table

Single-Sided Disks

TRACK		PSN	TRACK		PSN
DEC	HEX	HEX	DEC	HEX	HEX
00	00	000	20	14	140
01	01	010	21	15	150
02	02	020	22	16	160
03	03	030	23	17	170
04	04	040	24	18	180
05	05	050	25	19	190
06	06	060	26	1A	1A0
07	07	070	27	1B	1B0
08	08	080	28	1C	1C0
09	09	090	29	1D	1D0
10	0A	0A0	30	1E	1E0
11	0B	0B0	31	1F	1F0
12	0C	0C0	32	20	200
13	0D	0D0	33	21	210
14	0E	0E0	34	22	220
15	0F	0F0	35	23	230
16	10	100	36	24	240
17	11	110	37	25	250
18	12	120	38	26	260
19	13	130	39	27	270

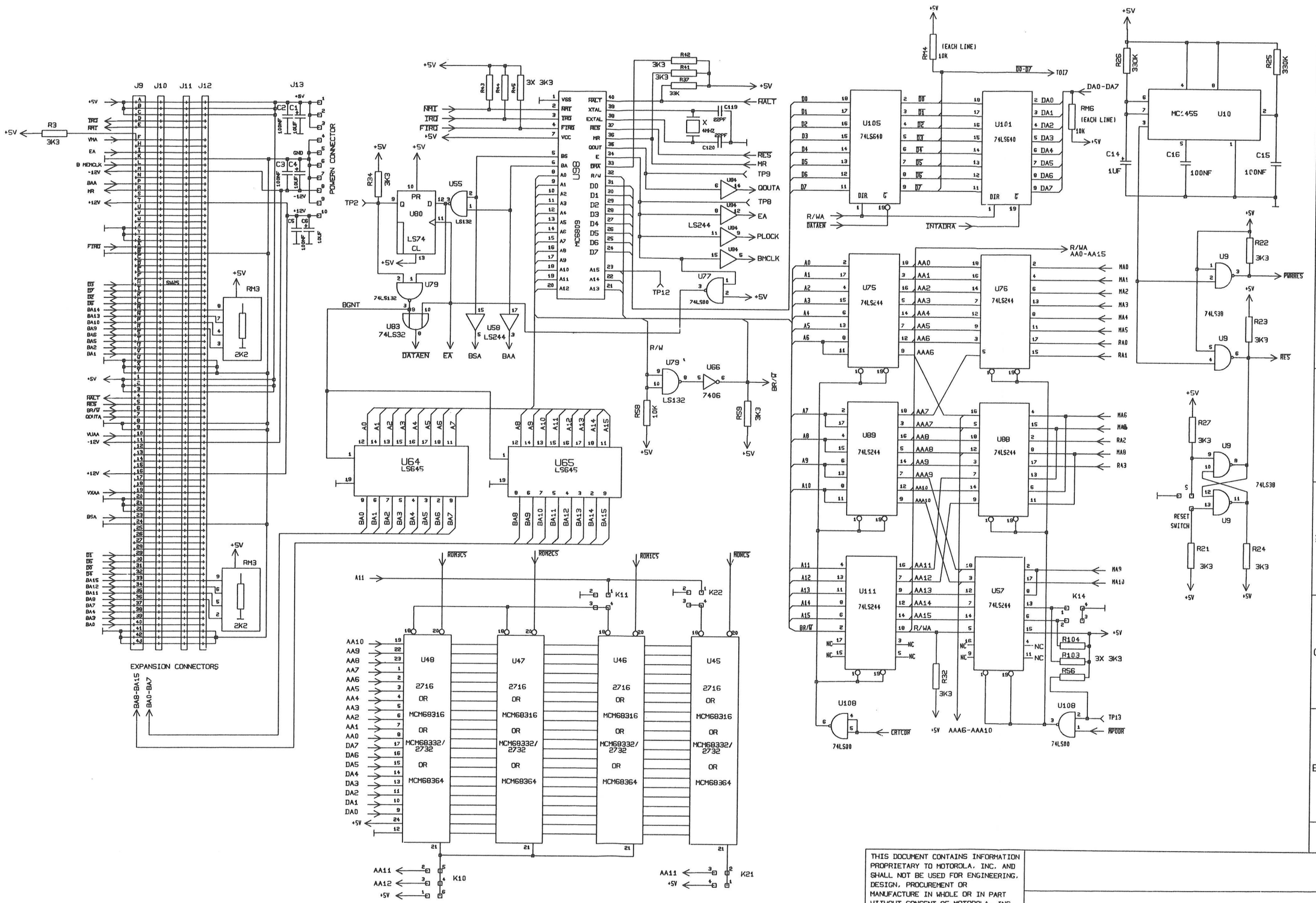
Double-Sided Disks

TRACK		PSN		TRACK		PSN	
DEC	HEX	SFC0	SFC1	DEC	HEX	SFC0	SFC1
00	00	000	010	20	14	280	290
01	01	020	030	21	15	2A0	2B0
02	02	040	050	22	16	2C0	2D0
03	03	060	070	23	17	2E0	2F0
04	04	080	090	24	18	300	310
05	05	0A0	0B0	25	19	320	330
06	06	0C0	0D0	26	1A	340	350
07	07	0E0	0F0	27	1B	360	370
08	08	100	110	28	1C	380	390
09	09	120	130	29	1D	3A0	3B0
10	0A	140	150	30	1E	3C0	3D0
11	0B	160	170	31	1F	3E0	3F0
12	0C	180	190	32	20	400	410
13	0D	1A0	1B0	33	21	420	430
14	0E	1C0	1D0	34	22	440	450
15	0F	1E0	1F0	35	23	460	470
16	10	200	210	36	24	480	490
17	11	220	230	37	25	5A0	5B0
18	12	240	250	38	26	5C0	5D0
19	13	260	270	39	27	5E0	5F0

CHAPTER 6

DEVICE LOCATION AND SCHEMATICS

This chapter contains the component location diagrams and schematics of the EXORset Main Controller Board and Mini-Floppy Disk Controller Board. Component location diagrams and schematics of the video display monitor, the mini-floppy drives, and the power supply are in their respective maintenance manuals (see APPENDIX A, B, and C).

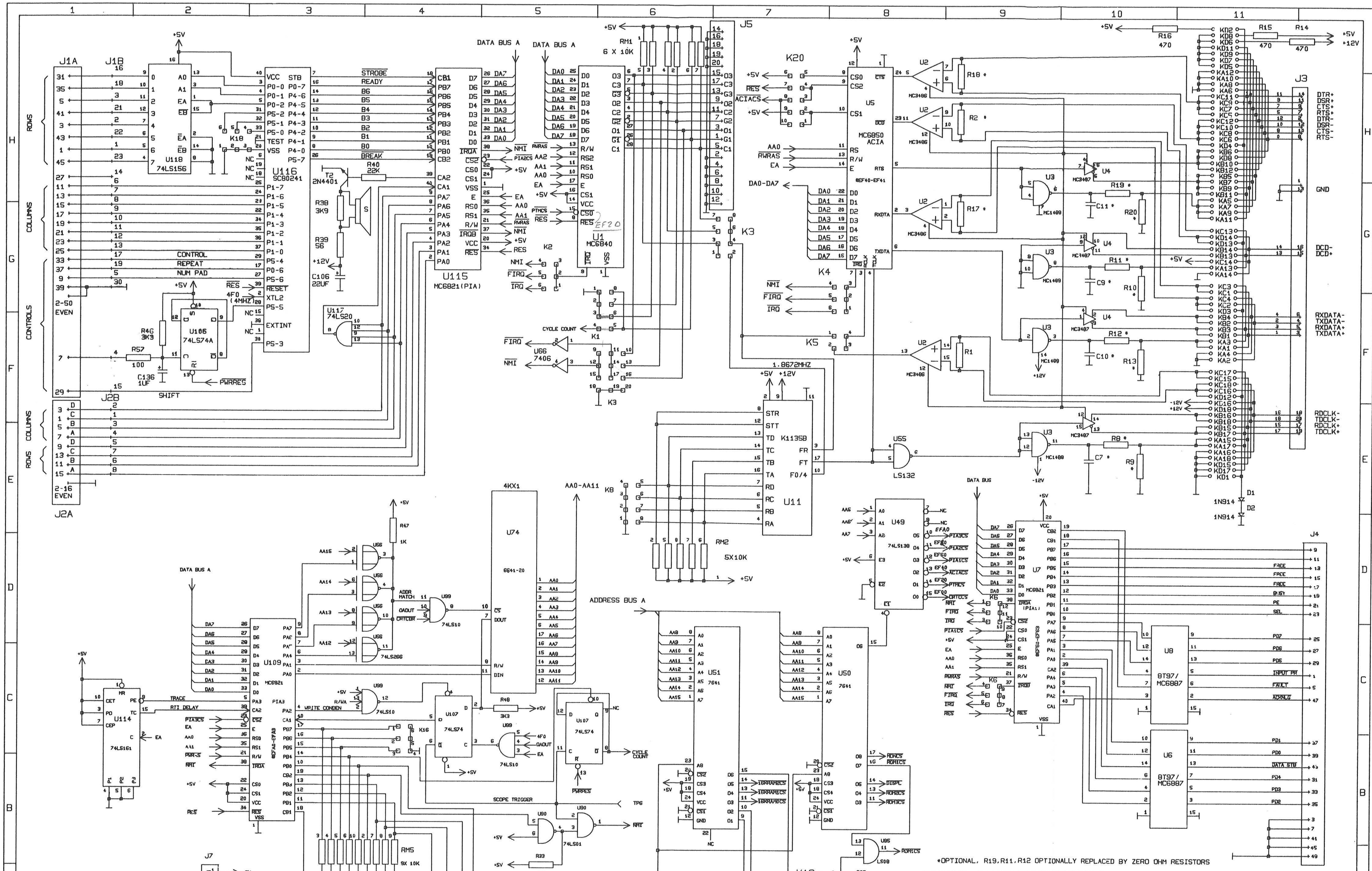


DRAWN BY: BASU CAD	DATE:
CHECKED BY: M. Schulz	4.5.82
ENGINEER: M. Schulz	4.5.82
MANAGER: Nyäch	4.5.82

EXORSET MAIN CONTROLLER BOARD

DRAWING NO. 63CG3003M ISSUE 'C' SHEET: 1/3

CAD-BASU GMBH MUNCHEN



*OPTIONAL, R19,R11,R12 OPTIONALLY REPLACED BY ZERO OHM RESISTORS

DRAWN BY.	BASU CAD	DATE.
CHECKED BY.	M. Schaefer	4.5.82
ENGINEER.	M. Schaefer	4.5.82
MANAGER.	[signature]	4.5.82

EXORSET MAIN CONTROLLER BOARD

DRAWING NO. 63CG3003M ISSUE 'C'

SHEET 2/3

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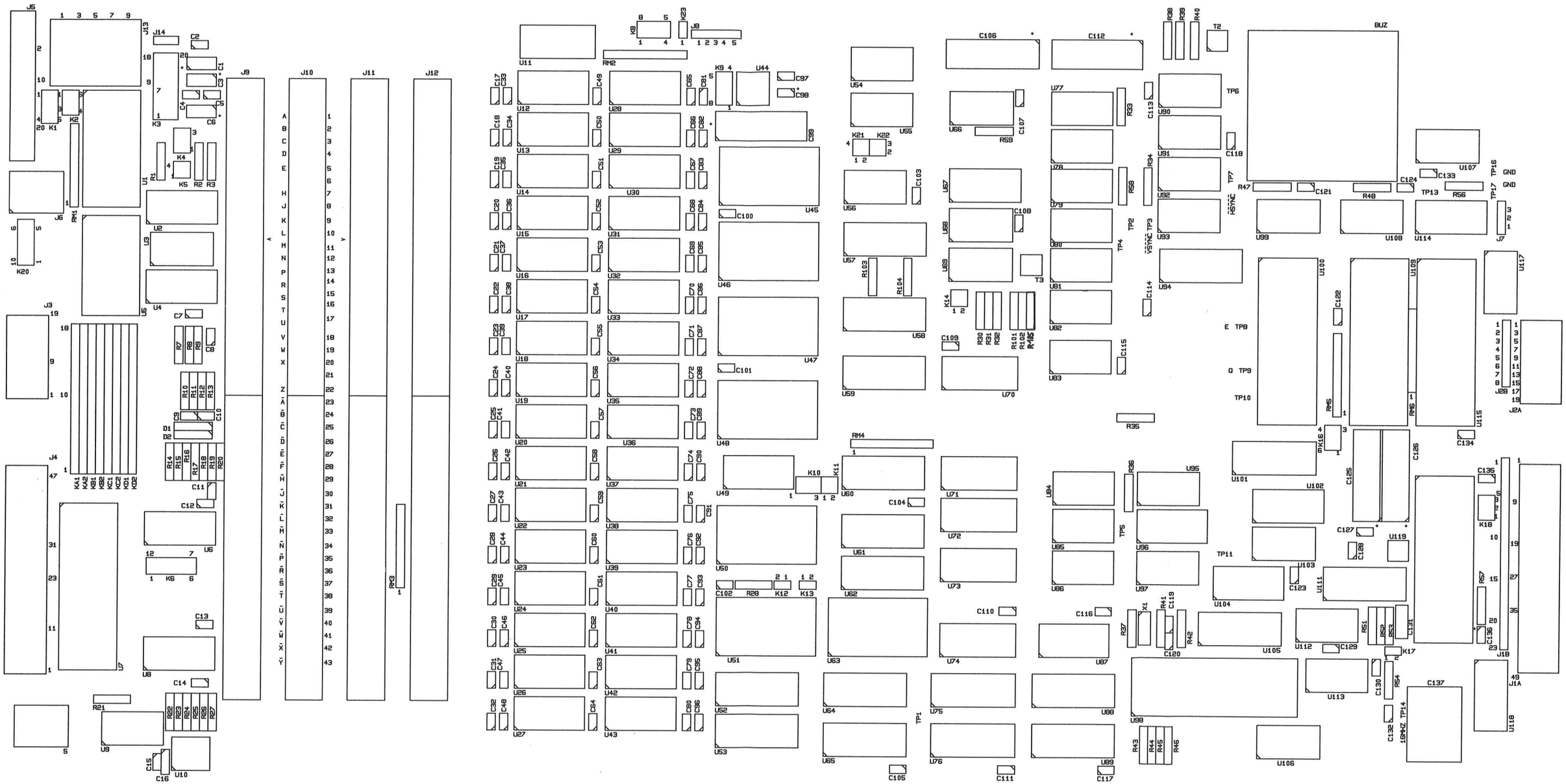
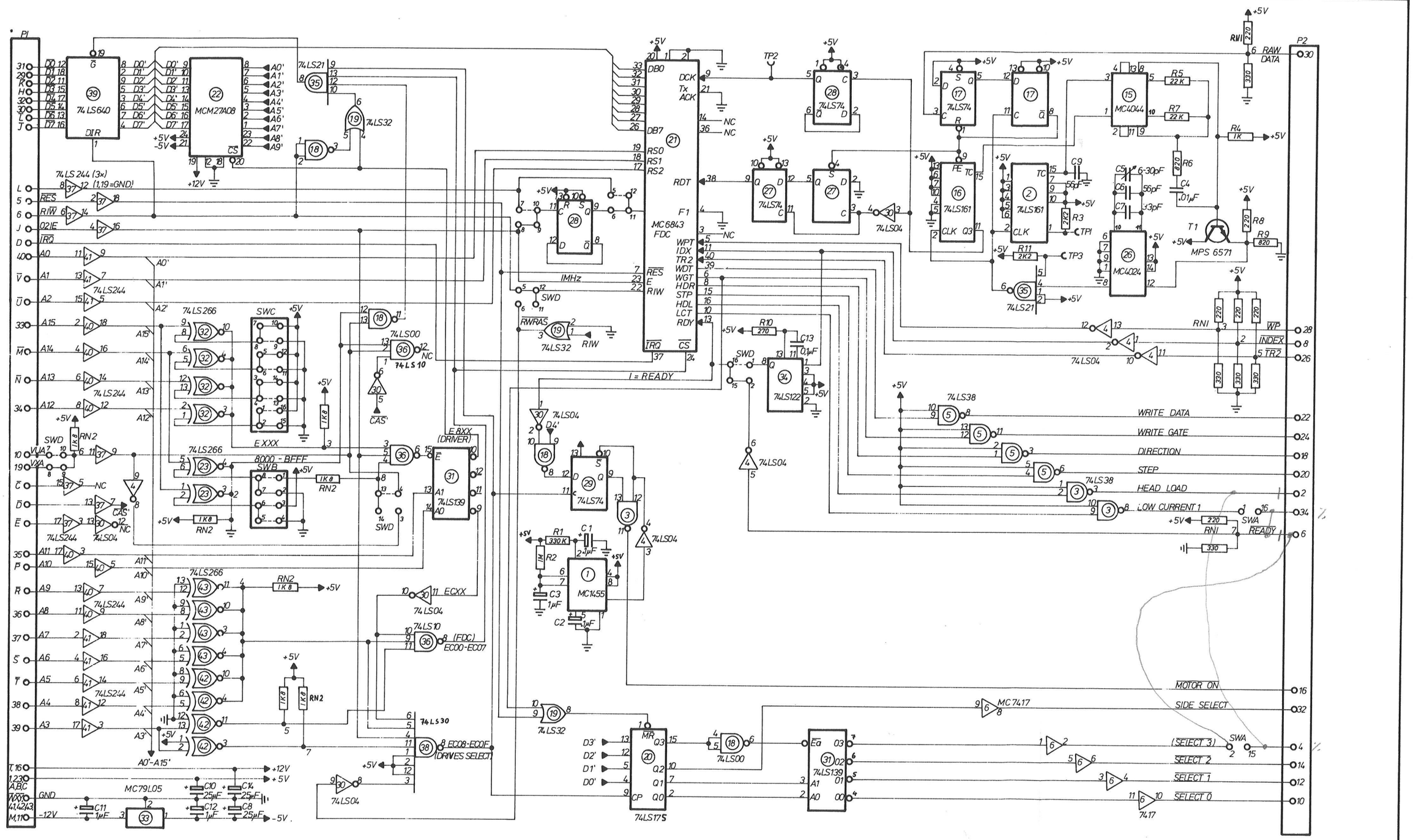
DRAWN BY. BASU CAD DATE.	EXORSET MAIN CONTROLLER BOARD
CHECKED BY. M. Shaft 4.5.82	
ENGINEER. M. Shaft 4.5.82	DRAWING NO. 63CG3003M ISSUE 'C' SHEET 3/3
MANAGER. [illegible] 4.5.82	

* OPTIONAL

** VALUE DEPENDING ON MONITOR TYPE



Component Location: EXORset Main Controller Board



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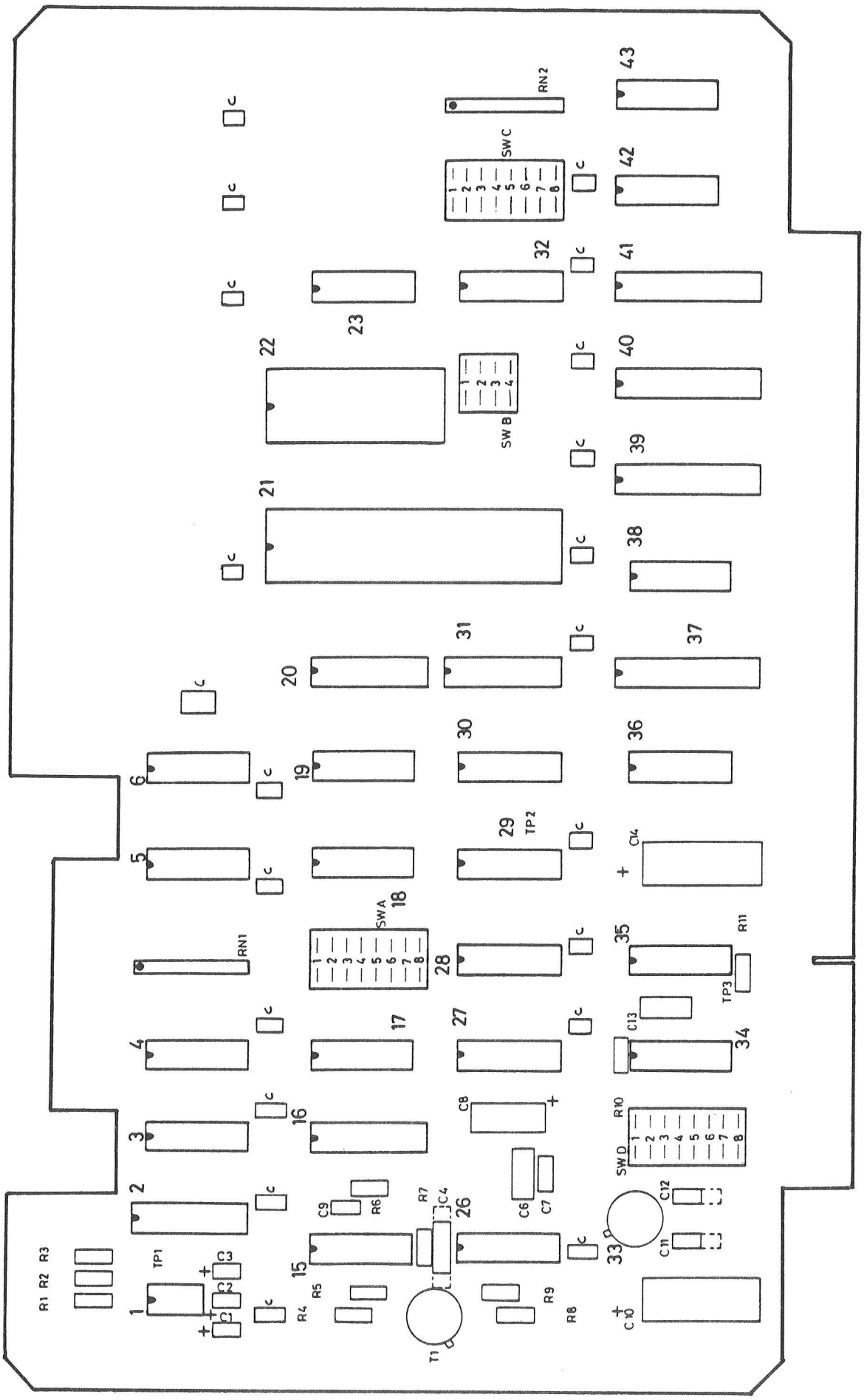
DIMENSIONS: MM (INCHES)			
SCALE: ·/·		TITLE: Floppy disk Controller Module	
REMOVE ALL BURRS AND SHARP EDGES — SURFACE QUALITY IN MICROMETER	DRAWN BY: Thurner / 6 — DATE: Mai '82		
TOLERANCE: 2 PLACE DEC.= ± HOLES ± 3 PLACE DEC.= ± ANGLES ±	CHECKED BY: M. Schaefer — 13.5.82	DRAWING NO. 63CG1216B	ISSUE 'C' — SHEET: 1 OF: 1
BM:	ENGINEER: M. Schaefer — 13.5.82		
	MANAGER: Lejeune — 13.5.82		



Component Location: EXORset Mini-Disk Controller Board

CHAPTER 7

PARTS LIST

This chapter provides the parts list for the EXORset Main Controller Board and Mini-Floppy Disk Controller Board. The list reflects the latest issue of hardware at the time of printing.

E06 SINGLE LEVEL BILL OF MATERIAL EXPLOSION

M6809SET100 12" CRT,XRSET 100
DISPLAY LEVEL IS ITEM FAMILY
DRAWING 53AW7703B61A 0

SC	B/M	PC	COMPONENT	QUANTITY	U/M	DATE	TYP	COMPONENT DESCRIPTION
EA	010	01	01-G2032M02	1.000000	EACH	02/26/82	MAK	FINAL ASSY,EXORSET 100
FA	020	01	M68WNTYPKG-E	1.000000	EACH	03/04/82	MAK	WARRANTY PACKAGE - EUROPE
FA	030	01	30-G9302M02	1.000000	EACH	02/26/82	MAK	POWER CORD
FA	035	01	67-G2046B02	1.000000	EACH	05/04/82	MAK	EXORSET 33/100 SOFTWARE
FA	040	01	56-G9208M01	1.000000	EACH	05/04/82	BUY	PLASTIC BAG
FL	040	01	M68EXORSET/D1	1.000000	EACH	05/07/82	BUY	EXORSET LITERATURE PKG

*XEX3102

E06 SINGLE LEVEL BILL OF MATERIAL EXPLOSION

01-G2032M02 FINAL ASSY,EXORSET 100

DISPLAY LEVEL IS ITEM FAMILY

DRAWING 01-G2032M02 0

SC	B/M	PC	COMPONENT	QUANTITY	U/M	DATE	TYP	COMPONENT DESCRIPTION
EA	010	01	15-G4044M01	1.000000	EACH	05/07/82	BUY	BOTTOM,EXORSET 100
FA	020	01	15-G4042M01	1.000000	EACH	05/07/82	BUY	KEYBOARD PANEL,EXORSET100
FA	030	01	15-G4043M01	1.000000	EACH	05/07/82	BUY	FRONT PANEL,EXORSET100
FA	040	01	15-G2036M01	1.000000	EACH	05/07/82	BUY	COVER,HOOD SET 100
FA	050	01	01-G4040M01	1.000000	EACH	05/07/82	BUY	SWTCH P/S ,SET 100/33
FA	060	01	01-G3003M01	1.000000	EACH	05/07/82	MAK	ASY,MAIN CNTR.SET100 TSTD
FA	070	01	01NW9804B93	1.000000	EACH	05/07/82	BUY	KEYBOARD, UNDECODED
FA	080	01	01-G2006M02	1.000000	EACH	05/07/82	MAK	MONITOR ASSY,EXORSET 100
FA	090	01	01NW9804C19	2.000000	EACH	05/10/82	BUY	DISK DRIVE W/SML FRNT PNL
FA	100	01	01-G1216B04	1.000000	EACH	05/07/82	MAK	PWB ASY,FDC SET100
FA	110	01	01-G2035M01	1.000000	EACH	05/07/82	MAK	BACK PANEL ASSY SET 100
FA	120	01	30-G2034M01	1.000000	EACH	05/07/82	BUY	CABLE HARNESS SET100/MAIN
FA	130	01	30-G9302M03	1.000000	EACH	05/07/82	BUY	FLAT CABLE,DSK DRV TO CNT
FA	140	01	30-G2040M01	1.000000	EACH	05/07/82	BUY	FLOP.DRV,ADAPT CBL SET100
FA	145	01	75NW9402A18	4.000000	EACH	05/10/82	MAK	FOOT,RUBBER 4MM HOLE

* MORE *

FA1500142-G9401M01

```
 E06     SINGLE LEVEL BILL OF MATERIAL EXPLOSION
 01-G2032M02            FINAL ASSY,EXORSET 100
DISPLAY LEVEL IS ITEM        FAMILY
 DRAWING 01-G2032M02       0
SC B/M PC COMPONENT          QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
FA 150 01 42-G9401M01        1.000000 EACH 05/07/82 BUY TIE,CABLE 2.5X1X100
FA 160 01 07-G4046M01        1.000000 EACH 05/07/82 BUY GAUZE FILTER SET100 /LONG
FA 170 01 07-G4046M02        1.000000 EACH 05/07/82 BUY GAUZE FILTER SET100/SHORT
FA 180 01 07-G4047M01        1.000000 EACH 05/07/82 BUY BRCKT,POTENTIOMETR SET100
FA 190 01 75-G4048M01        1.000000 EACH 05/12/82 BUY TAPE,RUBBR,SLF-ADHSV,SQAR
FA 200 01 75-G4049M01        1.000000 EACH 05/12/82 BUY TAPE,RUBBR,SLF-ADHSV,OVAL
FA 210 01 18NW9603A41        1.000000 EACH 05/07/82 BUY RES VAR 100K OHM 10%
FA 220 01 02NW9006A46        1.000000 EACH 05/12/82 BUY NUT,HEX-POT M10 X 0.75
FA 230 01 36NW9506A19        1.000000 EACH 05/07/82 BUY KNOB UPRITE RND 13X6 GRAY
FA 240 01 38NW9404C05        1.000000 EACH 05/07/82 BUY CAP,KNOB 13MM GRAY
FA 250 01 04SW999D009        12.00000 EACH 05/07/82 BUY WSHR,FLT 4.3X0.8 SCYI
FA 260 01 04SW998D005        15.00000 EACH 05/07/82 BUY WSHR,LKIT,J4  X0.5SCYI
FA 270 01 04NW9005A38        6.000000 EACH 05/07/82 BUY WASHER,NYLON M4X9X.8 (MM)
FA 280 01 03SW994D408        13.00000 EACH 05/07/82 BUY SCR,PHFIL,M4.0X0.7X8 SBLO
FA 290 01 03SW994D414        8.000000 EACH 05/12/82 BUY SCR,PHFIL,M4  X0.7X14SBLO
       * MORE *
FA3000103SW994D420

 E06     SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 01-G2032M02            FINAL ASSY,EXORSET 100
DISPLAY LEVEL IS ITEM        FAMILY
DRAWING 01-G2032M02       0
SC B/M PC COMPONENT          QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
FA 300 01 03SW994D420        4.000000 EACH 05/12/82 BUY SCR,PHFIL,M4  X0.7X20SBLO
FA 310 01 03SW994D320        4.000000 EACH 05/12/82 BUY SCR,PHFIL,M3  X0.5X20SBLO
FA 320 01 04SW998D004        4.000000 EACH 05/07/82 BUY WSHR,LKIT,J3  X0.4SCYI
FA 330 01 04NW9005A40        4.000000 EACH 05/12/82 BUY WASHER FLAT M3 9.0 X 0.8
FA 340 01 02SW990D004        1.000000 EACH 05/07/82 BUY NUT,HX M4  X0.7 X3.2 SCYI
FA 350 01 42NW9401A92        3.000000 EACH 05/12/82 BUY FSTNR,FLAT CABLE SLF ADHS
FA 360 01 54-G4053M01        1.000000 EACH 05/13/82 BUY LABEL,UNIT NUMBER

*MSGERM2
```

E06 SINGLE LEVEL BILL OF MATERIAL EXPLOSION

01-G3003M01 ASY,MAIN CNTR.SET100 TSTD
DISPLAY LEVEL IS ITEM FAMILY
DRAWING 01-G3003M01 0

SC	B/M	PC	COMPONENT	QUANTITY	U/M	DATE	TYP	COMPONENT DESCRIPTION
EA	010	01	01-G3003M11	1.000000	EACH	08/25/81	MAK	ASY,XSET MAIN CNTR.BD.UNT
FA	020	02	51-G5004M01	1.000000	EACH	09/30/81	MAK	IC.PRG.EXBUG1.4
FA	030	01	51-G5002M03	1.000000	EACH	09/30/81	MAK	IC.PRG.CHAR-GEN.U63
FA	040	01	51-G5000M04	1.000000	EACH	09/30/81	MAK	IC.PRG.ADDR.DEC U50
FA	050	01	51-G5000M05	1.000000	EACH	09/30/81	MAK	IC.PRG.ADDR.DEC U51
FA	060	01	06SW-124A53	1.000000	EACH	05/08/82	MAK	RES,FILM 1/4W,5%,1.5K OHM

```
 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION
 01-G3003M11              ASY,XSET MAIN CNTR.BD.UNT
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING
SC B/M PC COMPONENT          QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 010 01 84-G8003M01        1.000000 EACH 11/19/81 BUY PCB,EXORSET 5 MAIN CNTRLR
FA 020 01 06SW-124A19        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,56    OHM
FA 021 01 06SW-124A25        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,100   OHM
FA 022 01 06SW-124A29        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,150   OHM
FA 023 01 06SW-124A37        2.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,330   OHM
FA 024 01 06SW-124A45        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,680   OHM
FA 025 01 06SW-124A47        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,820   OHM
FA 026 01 06SW-124A49        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,1.0K  OHM
FA 027 01 06SW-124A61        27.00000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,3.3K  OHM
FA 028 01 06SW-124A41        3.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,470   OHM
FA 029 01 06SW-124A73        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,10K   OHM
FA 030 01 06SW-124A81        3.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,22K   OHM
FA 032 01 06SW-124B10        2.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,330K  OHM
FA 040 01 51NW9626A45        1.000000 EACH 11/19/81 BUY RES NT 10P SIP 9-2.2K
FA 045 01 51NW9626A37        5.000000 EACH 11/19/81 BUY RES NT 10P SIP 9-10K
       * MORE *
FA0500121-G9632M03
```


```
 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 01-G3003M11              ASY,XSET MAIN CNTR.BD.UNT
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING
SC B/M PC COMPONENT          QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 010 01 84-G8003M01        1.000000 EACH 11/19/81 BUY PCB,EXORSET 5 MAIN CNTRLR
FA 020 01 06SW-124A19        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,56    OHM
FA 021 01 06SW-124A25        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,100   OHM
FA 022 01 06SW-124A29        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,150   OHM
FA 023 01 06SW-124A37        2.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,330   OHM
FA 024 01 06SW-124A45        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,680   OHM
FA 025 01 06SW-124A47        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,820   OHM
FA 026 01 06SW-124A49        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,1.0K  OHM
FA 027 01 06SW-124A61        27.00000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,3.3K  OHM
FA 028 01 06SW-124A41        3.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,470   OHM
FA 029 01 06SW-124A73        1.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,10K   OHM
FA 030 01 06SW-124A81        3.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,22K   OHM
FA 032 01 06SW-124B10        2.000000 EACH 11/19/81 BUY RES,FILM 1/4W,5%,330K  OHM
FA 040 01 51NW9626A45        1.000000 EACH 11/19/81 BUY RES NT 10P SIP 9-2.2K
FA 045 01 51NW9626A37        5.000000 EACH 11/19/81 BUY RES NT 10P SIP 9-10K
       * MORE *
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FA0500121-G9632M03
E06 SINGLE LEVEL BILL OF MATERIAL EXPLOSION
01-G3003M11 ASY,XSET MAIN CNTR.BD.UNT
DISPLAY LEVEL IS ITEM FAMILY
DRAWING

SC	B/M	PC	COMPONENT	QUANTITY	U/M	DATE	TYP	COMPONENT DESCRIPTION
FA	050	01	21-G9632M03	2.000000	EACH	11/19/81	BUY	CAP, CER. 22 PF 2.5 MM
FA	051	01	21NW9604A06	2.000000	EACH	01/28/82	BUY	CAP,FXD-CER,.01MF 50V 10%
FA	052	01	21NW9702A09	115.0000	EACH	03/03/82	BUY	CAP,CER0.1UF 50VDC LL.110
FA	054	01	21-G9632M02	1.000000	EACH	11/19/81	BUY	CAP, CER. 0.1 UF 5 MM
FA	055	01	23NW9618A29	3.000000	EACH	11/19/81	BUY	CAP,SOL TANT 1.0MF 35V
FA	056	01	23NW9618A31	3.000000	EACH	11/19/81	BUY	CAP,SOL TANT 10.0MF 35V
FA	057	01	23NW9618A21	5.000000	EACH	11/19/81	BUY	CAP,ELEC 25UF 25V
FA	059	01	20-G9628M01	1.000000	EACH	11/19/81	BUY	CAP, CER. TRIM 6-30 PF
FA	060	01	51NW9615D81	1.000000	EACH	11/19/81	BUY	IC MC6840P 28 PIN
FA	061	01	51NW9615B94	1.000000	EACH	11/19/81	BUY	IC ACIA MC6850P,24 PINS
FA	062	01	51NW9615B27	3.000000	EACH	11/19/81	BUY	IC MC6821P 40 PIN
FA	063	01	51NW9615F28	1.000000	EACH	03/26/82	BUY	IC,HD46505SP,40PIN
FA	064	01	51NW9615G83	1.000000	EACH	11/19/81	BUY	IC SC80241P 40 PIN PLSTC
FA	065	01	51NW9615F86	1.000000	EACH	11/19/81	BUY	IC MC6809P 40P
FA	066	01	51NW9615B65	1.000000	EACH	11/19/81	BUY	IC MC1455P1 8 PIN

* MORE *

FA0670151NW9615B71
E06 SINGLE LEVEL BILL OF MATERIAL EXPLOSION
01-G3003M11 ASY,XSET MAIN CNTR.BD.UNT
DISPLAY LEVEL IS ITEM FAMILY
DRAWING

SC	B/M	PC	COMPONENT	QUANTITY	U/M	DATE	TYP	COMPONENT DESCRIPTION
FA	067	01	51NW9615B71	2.000000	EACH	11/19/81	BUY	IC HEX BUFFER 8T97 16 PIN
FA	068	01	51NW9615B29	1.000000	EACH	11/19/81	BUY	IC MC1488L 14 PIN
FA	069	01	51NW9615A28	1.000000	EACH	11/19/81	BUY	IC MC4024P 14 PIN
FA	070	01	51NW9615B31	1.000000	EACH	11/19/81	BUY	IC MC4044P 14 PIN
FA	071	01	51NW9615F37	1.000000	EACH	11/19/81	BUY	IC ZILOG Z6104-4 18 PIN
FA	072	01	51NW9615F47	4.000000	EACH	11/19/81	BUY	IC MCM2114-20 18 PIN
FA	073	01	51NW9615E37	32.00000	EACH	11/19/81	BUY	IC MCM4116BP-20 16 PIN,
FA	074	01	51NW9615E91	3.000000	EACH	11/19/81	BUY	IC SN74LS00N 14 PIN
FA	075	01	51NW9615F62	1.000000	EACH	11/19/81	BUY	IC SN74LS01N 14 PIN
FA	076	01	51NW9615C20	2.000000	EACH	11/19/81	BUY	IC SN74LS02N 14 PIN
FA	077	01	51NW9615C21	1.000000	EACH	11/19/81	BUY	IC SN74LS04N 14 PIN
FA	078	01	51NW9615C22	1.000000	EACH	11/19/81	BUY	IC SN74LS08N 14 PIN
FA	079	01	51NW9615E88	2.000000	EACH	11/19/81	BUY	IC SN74LS10N 14PIN
FA	080	01	51NW9615E93	1.000000	EACH	11/19/81	BUY	IC SN74LS14N 14 PIN
FA	081	01	51NW9615F05	1.000000	EACH	11/19/81	BUY	IC SN74LS20N POS 14PIN

* MORE *

FA0820151NW9615C23
E06 SINGLE LEVEL BILL OF MATERIAL EXPLOSION
01-G3003M11 ASY,XSET MAIN CNTR.BD.UNT
DISPLAY LEVEL IS ITEM FAMILY
DRAWING

SC	B/M	PC	COMPONENT	QUANTITY	U/M	DATE	TYP	COMPONENT DESCRIPTION
FA	097	01	51NW9615E94	1.000000	EACH	11/19/81	BUY	IC SN74LS279N 16 PIN PLS
FA	098	01	51NW9615E99	2.000000	EACH	11/19/81	BUY	IC SN74LS374N 20 PIN
FA	099	01	51NW9615F63	4.000000	EACH	11/19/81	BUY	IC SN74LS640N 20 PIN
FA	100	01	51NW9615A36	1.000000	EACH	11/19/81	BUY	IC MC7406P 14 PIN
FA	101	01	51NW9615H11	2.000000	EACH	11/19/81	BUY	IC SN74LS645N 20 PN PLST
FA	102	01	51NW9615F60	1.000000	EACH	11/19/81	BUY	IC MC3486P 16 PIN
FA	103	01	51NW9615F61	1.000000	EACH	11/19/81	BUY	IC MC3487P 16 PIN
FA	104	01	51NW9615F01	1.000000	EACH	11/19/81	BUY	IC SN74LS86N 14 PIN
FA	110	01	51NW9615D12	1.000000	EACH	11/19/81	BUY	IC MC78L05CP 3 PIN
FA	111	01	51NW9615G78	1.000000	EACH	11/19/81	BUY	NA*IC,79L05ACG 3PIN MTL
FA	112	01	48NW9616A03	2.000000	EACH	11/19/81	BUY	DIODE,SIL.1N4148/1N914
FA	114	01	51NW9615G14	1.000000	EACH	11/19/81	BUY	IC,*K1135B*MOT* 18 PIN
FA	115	01	48NW9610A14	1.000000	EACH	11/19/81	BUY	TRANS NPN 2N3904 SW HI SP
FA	116	01	48NW9610A01	1.000000	EACH	11/19/81	BUY	TRANS NPN 2N4401 CASE 29
FA	120	01	09NW9811A02	32.00000	EACH	11/19/81	BUY	SKT,IC DIL 14P LO PROFILE

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FA1210109NW9811A04
 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION
 01-G3003M11             ASY,XSET MAIN CNTR.BD.UNT
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING
SC B/M PC COMPONENT          QUANTITY U/M    DATE    TYP COMPONENT DESCRIPTION
FA 121 01 09NW9811A04        44.00000 EACH 11/19/81 BUY SKT,IC DIL 16P LO PROFILE
FA 122 01 09NW9811A09        6.000000 EACH 11/19/81 BUY SKT,IC DIL 18P LO PROFILE
FA 123 01 09NW9811A15        8.000000 EACH 11/19/81 BUY SKT,IC DIL 24P LO PROFILE
FA 124 01 09NW9811A21        1.000000 EACH 11/19/81 BUY SKT,IC DIL 28P LO PROFILE
FA 125 01 09NW9811A22        6.000000 EACH 11/19/81 BUY SKT,IC DIL 40P LO PROFILE
FA 126 01 09NW9811A27        18.00000 EACH 11/19/81 BUY SKT,IC DIL 20P LO PROFILE
FA 127 01 09NW9811A33        1.000000 EACH 02/03/82 BUY SKT,IC DIL 8P  LO PROFILE
FA 140 01 48NW9606A22        1.000000 EACH 11/19/81 BUY XTAL,4MHZ,HC-18W CASE
FA 141 01 29-G9805M01        13.00000 EACH 11/19/81 BUY PIN, TEST POINT
FA 143 01 28NW9802A72        4.000000 EACH 11/19/81 BUY CONN 86 PIN .156C SAEPKG
FA 144 01 80NW9619A43        1.000000 EACH 11/19/81 BUY ALARM,AUDIO/CONTIN-WARBLE
FA 145 01 29NW9805B17        36.00000 EACH 11/19/81 BUY JUMPER,SHORTING INSULATED
FA 150 01 28NW9802D01        4.000000 EACH 11/19/81 BUY HEADER,DBL ROW 2 PIN
FA 151 01 28NW9802D04        1.000000 EACH 11/19/81 BUY HEADER,3 POS SINGLE LINE
FA 152 01 28NW9802D56        1.000000 EACH 11/19/81 BUY HDR,SNGL ROW 4PIN .100CNT
       * MORE *
FA1530128NW9802D57
 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION
 01-G3003M11             ASY,XSET MAIN CNTR.BD.UNT
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING
SC B/M PC COMPONENT          QUANTITY U/M    DATE    TYP COMPONENT DESCRIPTION
FA 153 01 28NW9802D57        1.000000 EACH 11/19/81 BUY HDR,SNGL ROW 5PIN .100CNT
FA 154 01 28NW9802C29        2.000000 EACH 11/19/81 BUY HEADER,DBL ROW STR PCB 4P
FA 155 01 28NW9802B21        4.000000 EACH 11/19/81 BUY HEADER,DBL ROW POST 6PIN
FA 156 01 28NW9802C43        4.000000 EACH 11/19/81 BUY HEADER,DBL ROW 8 PIN
FA 157 01 28NW9802C52        2.000000 EACH 11/19/81 BUY HEADER,DBL ROW 10 PIN
FA 158 01 28NW9802C63        1.000000 EACH 11/19/81 BUY HEADER,DBL RW 12PN .100CR
FA 159 01 28NW9802B34        1.000000 EACH 11/19/81 BUY HEADER DBL ROW POST 16PIN
FA 160 01 28NW9802C86        4.000000 EACH 11/19/81 BUY HDR,DBL ROW 36 PN .100CNT
FA 170 01 28NW9802B35        1.000000 EACH 11/19/81 BUY CONN PC BD HEADER 10 PIN
FA 171 01 28NW9802E12        1.000000 EACH 11/19/81 BUY CONN,RECT-MALE 8 PIN
FA 172 01 28NW9802E13        1.000000 EACH 01/28/82 BUY CONN,RECT-MALE 23 PIN
FA 174 01 28NW9802E36        1.000000 EACH 03/18/82 BUY HEADER,3 PIN UNPROTECTED
FA 180 01 14NW9416A01        1.000000 EACH 12/09/81 BUY PAD MNTG NYL TO-5 T/W

*MSGERM1
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 E06     SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 51-G5004M01              IC.PRG.EXBUG1.4
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING 51-G5004M           0
SC B/M PC COMPONENT           QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 010 01 51-G9615M05         1.000000 EACH 09/29/81 BUY EPROM 4K X 8 EPROM
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*MSGERM2

 E06     SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 51-G5002M03              IC.PRG.CHAR-GEN.U63
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING 51-G5002M           0
SC B/M PC COMPONENT           QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 010 01 51NW9615C73         1.000000 EACH 09/29/81 BUY IC C2708 24 PIN
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*MSGERM2

 E06     SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 51-G5000M04              IC.PRG.ADDR.DEC U50
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING 51-G5000M           0
SC B/M PC COMPONENT           QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 010 01 51NW9615G80         1.000000 EACH 09/29/81 BUY IC,MCM7641DC 24 PIN PLSTC
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*MSGERM2

 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 51-G5000M05              IC.PRG.ADDR.DEC U51
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING 51-G5000M          0
SC B/M PC COMPONENT          QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 010 01 51NW9615G80        1.000000 EACH 09/29/81 BUY IC,MCM7641DC 24 PIN PLSTC
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*MSGERM2
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*MSGERM2

 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 01-G1216B04              PWB ASY,FDC SET100
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING 01-G1216B04         0
SC B/M PC COMPONENT            QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 010 01 01-G1216B13          1.000000 EACH 01/28/82 BUY PWB ASY,FDC SET100  UNTST
FA 020 01 51-G5002M05          1.000000 EACH 12/23/81 MAK IC PRG FDC 9.C SET 33/100
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*MSGERM2

 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 01-G1216B13              PWB ASY,FDC SET100  UNTST
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING 01-G1216B13         0
SC B/M PC COMPONENT            QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 005 01 84-G6216B01          1.000000 EACH 03/02/82 BUY PWB - FDC
FA 010 01 06SW-124A33          1.000000 EACH 11/16/81 BUY RES,FILM 1/4W,5%,220   OHM
FA 020 01 06SW-124A35          1.000000 EACH 11/16/81 BUY RES,FILM 1/4W,5%,270   OHM
FA 030 01 06SW-124A47          2.000000 EACH 11/16/81 BUY RES,FILM 1/4W,5%,820   OHM
FA 040 01 06SW-124A49          1.000000 EACH 11/16/81 BUY RES,FILM 1/4W,5%,1.0K  OHM
FA 050 01 06SW-124A57          2.000000 EACH 11/16/81 BUY RES,FILM 1/4W,5%,2.2K  OHM
FA 060 01 06SW-124A81          2.000000 EACH 11/16/81 BUY RES,FILM 1/4W,5%,22K   OHM
FA 070 01 06SW-124B10          1.000000 EACH 11/16/81 BUY RES,FILM 1/4W,5%,330K  OHM
FA 080 01 06SW-124B22          1.000000 EACH 11/16/81 BUY RES,FILM 1/4W,5%,1.0M  OHM
FA 085 01 08-G9703M03          1.000000 EACH 03/12/82 BUY CAP,FXD FLM 0.01 UF
FA 100 01 09NW9811A15         1.000000 EACH 11/16/81 BUY SKT,IC DIL 24P LO PROFILE
FA 110 01 09NW9811A22         1.000000 EACH 11/16/81 BUY SKT,IC DIL 40P LO PROFILE
FA 115 01 14NW9416A01         1.000000 EACH 11/16/81 BUY PAD MNTG NYL TO-5 T/W
FA 120 01 20-G9628M01          1.000000 EACH 11/16/81 BUY CAP, CER. TRIM 6-30 PF
FA 130 01 21NW9702A09          1.000000 EACH 11/20/81 BUY CAP,CER0.1UF 50VDC LL.110
        * MORE *
FA1400121-G9632M01
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 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 01-G1216B13            PWB ASY,FDC SET100  UNTST
DISPLAY LEVEL IS ITEM       FAMILY
DRAWING 01-G1216B13       0
SC B/M PC COMPONENT          QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
FA 140 01 21-G9632M01        20.00000 EACH 11/20/81 BUY CAP, CER. 0.01 UF 2.5 MM
FA 150 01 21-G9632M04        2.000000 EACH 03/12/82 BUY CAP, CER. 56 PF 2.5 MM
FA 160 01 23NW9618A29        3.000000 EACH 11/16/81 BUY CAP,SOL TANT 1.0MF 35V
FA 170 01 23NW9618A33        3.000000 EACH 11/16/81 BUY CAP,22MF , 25V
FA 180 01 23-G9618M01        2.000000 EACH 03/12/82 BUY CAP, ELECT 0.1 UF
FA 190 01 29-G9805M01        3.000000 EACH 11/16/81 BUY PIN, TEST POINT
FA 200 01 48NW9610A21        1.000000 EACH 11/16/81 BUY TRANS NPN MPS6571
FA 210 01 51NW9615A28        1.000000 EACH 11/16/81 BUY IC MC4024P 14 PIN
FA 220 01 51NW9615B31        1.000000 EACH 11/16/81 BUY IC MC4044P 14 PIN
FA 230 01 51NW9615B65        1.000000 EACH 11/16/81 BUY IC MC1455P1 8 PIN
FA 240 01 51NW9615C21        2.000000 EACH 11/16/81 BUY IC SN74LS04N 14 PIN
FA 250 01 51NW9615C23        1.000000 EACH 11/16/81 BUY IC SN74LS30N 14 PIN
FA 260 01 51NW9615C24        1.000000 EACH 11/16/81 BUY IC SN74LS32N 14 PIN
FA 270 01 51NW9615C25        4.000000 EACH 11/16/81 BUY IC SN74LS74N 14 PIN
FA 280 01 51NW9615C28        2.000000 EACH 11/16/81 BUY IC SN74LS161N  16 PIN
       * MORE *
FA2900151NW9615C70

 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 01-G1216B13            PWB ASY,FDC SET100  UNTST
DISPLAY LEVEL IS ITEM       FAMILY
DRAWING 01-G1216B13       0
SC B/M PC COMPONENT          QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
FA 290 01 51NW9615C70        1.000000 EACH 11/16/81 BUY IC SN74LS139N MOT 16 PIN
FA 300 01 51NW9615C75        1.000000 EACH 11/16/81 BUY IC SN7417N 14 PIN
FA 310 01 51NW9615E88        1.000000 EACH 11/16/81 BUY IC SN74LS10N 14PIN
FA 320 01 51NW9615E91        1.000000 EACH 11/16/81 BUY IC SN74LS00N 14 PIN
FA 330 01 51NW9615E92        1.000000 EACH 11/16/81 BUY IC SN74LS122N 14 PIN
FA 340 01 51NW9615F02        3.000000 EACH 11/20/81 BUY IC 74LS244N SIG 20 PIN
FA 350 01 51NW9615F09        4.000000 EACH 11/16/81 BUY IC SN74LS266J 14 PIN
FA 360 01 51NW9615F16        1.000000 EACH 11/16/81 BUY IC SN74LS175N  16 PIN
FA 370 01 51NW9615F35        1.000000 EACH 11/16/81 BUY IC DM74LS21N 14 PIN
FA 380 01 51NW9615F63        1.000000 EACH 11/16/81 BUY IC SN74LS640N 20 PIN
FA 390 01 51NW9615G38        2.000000 EACH 04/02/82 BUY IC SN74LS38N 14 PIN PLSTC
FA 392 01 51NW9615F26        1.000000 EACH 11/16/81 BUY IC HD46503SP 40 PIN
FA 400 01 51NW9615G78        1.000000 EACH 11/16/81 BUY NA*IC,79L05ACG 3PIN MTL
FA 410 01 51-G9626M01        1.000000 EACH 03/12/82 BUY NTWRK,RES 7/1.8K SIL 8PIN
FA 420 01 51-G9626M02        1.000000 EACH 03/12/82 BUY NTWK,RES 6-220/330 SIP 8P
       * MORE *
FA4300155NW9403A05

 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 01-G1216B13            PWB ASY,FDC SET100  UNTST
DISPLAY LEVEL IS ITEM       FAMILY
DRAWING 01-G1216B13       0
SC B/M PC COMPONENT          QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
FA 430 01 55NW9403A05        2.000000 EACH 11/16/81 BUY EJCTR CRD .062THK/ WHITE
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*MSGERM2

 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 01-G2006M02              MONITOR ASSY,EXORSET 100
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING 01-G2006M02         0
SC B/M PC COMPONENT            QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 010 01 01NW9804C18          1.000000 EACH 12/16/81 BUY MONITOR CRT 12IN 115/230V
FA 020 01 15-G4037M01          1.000000 EACH 12/02/81 BUY SHROUD,EXORSET 100
FA 030 01 21NW9702A09          1.000000 EACH 05/07/82 BUY CAP,CER0.1UF 50VDC LL.110
FA 040 01 28NW9802E37          1.000000 EACH 03/01/82 BUY HEADER ASSEMBLY,3-PIN PWB
FA 050 01 06SW-124A81          1.000000 EACH 05/07/82 BUY RES,FILM 1/4W,5%,22K  OHM
FA 060 01 30-G2038M01          1.000000 EACH 05/07/82 BUY BRIGHTNS CNTRL CBL SET100
FA 065 01 30-G2042M01          1.000000 EACH 05/08/82 BUY VIDEO CBL ASSY SET100
FA 068 01 42-G9401M01          1.000000 EACH 05/08/82 BUY TIE,CABLE 2.5X1X100
FA 070 01 03NW9004B30          2.000000 EACH 05/12/82 BUY SCR,HX HD SF/TP M4.2 X 13
FA 080 01 04SW999D009          2.000000 EACH 05/07/82 BUY WSHR,FLT 4.3X0.8 SCYI



*MSGERM2

 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION

 01-G2035M01              BACK PANEL ASSY SET 100
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING 01-G2035M           0
SC B/M PC COMPONENT            QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 010 01 64-G4039M01          1.000000 EACH 12/04/81 BUY BACK PANEL,EXORSET 100
FA 020 01 15-G4020M01          1.000000 EACH 02/16/82 BUY COVER,BCK PNL,ALUM BLACK
FA 030 01 07CW4077B01          1.000000 EACH 12/04/81 BUY FRAME,FAN FILTER
FA 040 01 91CW4062B01          1.000000 EACH 12/04/81 BUY FILTER,FAN
FA 050 01 59NW9807A30          1.000000 EACH 12/04/81 BUY FAN,115V/50HZ/20W/160 CMH
FA 055 01 30-G2039M01          1.000000 EACH 05/08/82 BUY FAN EARTH CABLE SET100
FA 060 01 75NW9402A17          3.000000 EACH 05/08/82 BUY SHOCK,MNT RUBBER - FAN
FA 070 01 43NW9002A94          3.000000 EACH 05/08/82 BUY INSERT,BRASS-FAN
FA 075 01 07-G4045M01          1.000000 EACH 05/08/82 BUY ADH TAPE FILT.FAN  SET100
FA 080 01 30-G2029M01          1.000000 EACH 12/04/81 BUY CBL ASY,25POL,SET33
FA 090 01 30-G2028M01          1.000000 EACH 12/04/81 BUY CBL ASY,50POL,SET33
FA 130 01 40NW9801B05          1.000000 EACH 12/16/81 BUY SW PSH SPDT MOM SOLDER
FA 140 01 02NW9006A43          1.000000 EACH 02/04/82 BUY SW HARDWARE DRESS NUT
FA 145 01 38NW9404C02          1.000000 EACH 02/04/82 BUY SW HARDWARE,RED CAP
FA 147 01 30-G2043M01          1.000000 EACH 05/07/82 BUY FLAT RIBBON CBL RESET SW
        * MORE *
FA1500109NW9803A26
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E06 SINGLE LEVEL BILL OF MATERIAL EXPLOSION

01-G2035M01 BACK PANEL ASSY SET 100
DISPLAY LEVEL IS ITEM FAMILY
DRAWING 01-G2035M O

SC	B/M	PC	COMPONENT	QUANTITY	U/M	DATE	TYP	COMPONENT DESCRIPTION
FA	150	01	09NW9803A26	1.000000	EACH	02/23/82	BUY	CONNECTOR,BNC SOCKET
FA	155	01	43NW9002A97	2.000000	EACH	05/10/82	BUY	WASHER,BNC INSULATION
FA	157	02	28NW9802E29	1.000000	EACH	05/12/82	BUY	CONN,BNC 500HM-UG1094 B/U
FA	160	01	30-G2041M01	1.000000	EACH	05/10/82	BUY	VID CBL TO BNC CON SET100
FA	170	01	38NW9404C01	2.000000	EACH	02/16/82	BUY	CAP,COVER (17.55MM)
FA	200	01	03SW994D308	4.000000	EACH	12/04/81	BUY	SCR,PHFIL,M3 X0.5X8SBLO
FA	210	01	03SW994D312	2.000000	EACH	05/10/82	BUY	SCR,PHFIL,M3 X0.5X12SBLO
FA	220	01	03SW994D408	1.000000	EACH	05/08/82	BUY	SCR,PHFIL,M4.0X0.7X8 SBLO
FA	230	01	03SW994D412	2.000000	EACH	05/08/82	BUY	SCR,PHFIL,M4 X0.7X12SBLO
FA	240	01	02SW990D004	2.000000	EACH	05/08/82	BUY	NUT,HX M4 X0.7 X3.2 SCYI
FA	250	01	04SW998D005	3.000000	EACH	05/10/82	BUY	WSHR,LKIT,J4 X0.5SCYI
FA	260	01	03SW994D316	1.000000	EACH	05/12/82	BUY	SCR,PHFIL,M3 X0.5X16SBLO
FA	270	01	03SW994D325	2.000000	EACH	05/12/82	BUY	SCR,PHFIL,M3 X0.5X25SBLO
FA	280	01	02SW990D002	9.000000	EACH	05/08/82	BUY	NUT,HX M3 X0.5 X2.4 SCYI
FA	290	01	04SW998D004	9.000000	EACH	05/08/82	BUY	WSHR,LKIT,J3 X0.4SCYI

* MORE *
FA3000102NW9006A45

E06 SINGLE LEVEL BILL OF MATERIAL EXPLOSION

01-G2035M01 BACK PANEL ASSY SET 100
DISPLAY LEVEL IS ITEM FAMILY
DRAWING 01-G2035M O

SC	B/M	PC	COMPONENT	QUANTITY	U/M	DATE	TYP	COMPONENT DESCRIPTION
FA	300	01	02NW9006A45	2.000000	EACH	05/12/82	BUY	NUT,DOME M3 BLK DIN 1587
FA	310	01	04NW9005A40	3.000000	EACH	05/12/82	BUY	WASHER FLAT M3 9.0 X 0.8
FA	320	01	04NW9005A39	2.000000	EACH	05/12/82	BUY	WASHER,NYLON M3 7.0 X 0.5
FA	330	01	43NW9002B04	2.000000	EACH	05/08/82	BUY	DISTANCE ROLL NYL M3X3MM

```
 E06     SINGLE LEVEL BILL OF MATERIAL EXPLOSION
 M6809SET33              XRSET WTH 56K RAM,2DS FLP
DISPLAY LEVEL IS ITEM         FAMILY
DRAWING 53AW7702B83A      0
SC B/M PC COMPONENT           QUANTITY U/M    DATE    TYP COMPONENT DESCRIPTION
FA 010 01 01-G2016M01         1.000000 EACH 07/27/81 MAK FINAL ASY XRSET 33 220V
FA 020 01 67-G2046B02         1.000000 EACH 08/03/81 MAK EXORSET 33/100 SOFTWARE
FA 025 01 30-G9302M02         1.000000 EACH 02/03/82 BUY POWER CORD
FA 040 01 M68WNTYPKG-E        1.000000 EACH 07/27/81 BUY WARRANTY PACKAGE - EUROPE
FL 030 01 68-EXORSETE         1.000000 EACH 08/03/81 BUY EXORSET LITERATURE PKJ
*XEK3026
 E06     SINGLE LEVEL BILL OF MATERIAL EXPLOSION
 01-G2016M01             FINAL ASY XRSET 33 220V
DISPLAY LEVEL IS ITEM         FAMILY
DRAWING
SC B/M PC COMPONENT           QUANTITY U/M    DATE    TYP COMPONENT DESCRIPTION
FA 010 01 01-G2020M01         1.000000 EACH 10/28/81 MAK ASY,BOTTOM SET33
FA 015 01 01-G3003M04         1.000000 EACH 03/05/82 BUY ASY MAIN CNT.SET33  TSTD.
FA 020 01 01-G1216B04         1.000000 EACH 03/04/82 MAK PWB ASY,FDC SET100
FA 021 01 03-G9004M03         8.000000 EACH 10/28/81 BUY SCR-METRC DIN7981 2.9X13
FA 030 01 01-G2005M02         1.000000 EACH 03/04/82 MAK CARD GUIDE,4SLOT,SET33
FA 031 01 03-G9004M04         6.000000 EACH 10/28/81 BUY SCR-METRC DIN7981 2.9X22
FA 032 01 04SW998D004         6.000000 EACH 10/28/81 BUY WSHR,LKIT,J3  X0.4SCYI
FA 040 01 01-G2006M01         1.000000 EACH 10/28/81 MAK ASY-MONITOR
FA 050 01 01-G2013M01         1.000000 EACH 10/28/81 MAK FLOPPY ASY FOR SET 33
FA 051 01 07-G4004M01         1.000000 EACH 03/10/82 BUY BRACKET, DISK TOP
FA 052 01 03SW993D308         2.000000 EACH 10/28/81 BUY SCR,PHFIL,M3.0X0.5X8 SCYI
FA 053 01 04-G9005M05         2.000000 EACH 10/28/81 BUY WSHR-PLSTC 2.8 X5.9X 1.5
FA 054 01 04SW999D009         2.000000 EACH 10/28/81 BUY WSHR,FLT 4.3X0.8 SCYI
FA 055 01 03SW993D408         2.000000 EACH 10/28/81 BUY SCR,PHFIL,M4.0X0.7X8 SCYI
FA 056 01 04SW998D005         2.000000 EACH 10/28/81 BUY WSHR,LKIT,J4  X0.5SCYI
        * MORE *
```

```
FA0600101-G2008M01
 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION
 01-G2016M01              FINAL ASY XRSET 33 220V
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING
SC B/M PC COMPONENT          QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
FA 060 01 01-G2008M01        1.000000 EACH 10/28/81 MAK ASY-KEYBOARD
FA 080 01 15-G4015M01        1.000000 EACH 10/28/81 BUY ENCLSR,FRNT PNL,XR30 PNTD
FA 081 01 03-G9004M03        7.000000 EACH 10/28/81 BUY SCR-METRC DIN7981 2.9X13
FA 090 01 15-G4014M01        1.000000 EACH 11/05/81 BUY ENCLSR,TOP, XR30 PNTD
FA 100 01 03SW993D425        4.000000 EACH 10/28/81 BUY SCR,PHFIL,M4.0X0.7X25SCYI
FA 110 01 04-G9005M04        4.000000 EACH 10/28/81 BUY WSHR-PLSTC 4.5 X 9 X 1.2
FA 140 01 13CW4038B01        1.000000 EACH 10/28/81 BUY SHIELD,CRT 9"DIAG NO-GLAR
FA 150 01 11-G9202M03        1.000000 EACH 10/28/81 BUY FOAM CASHION
FA 160 01 54-G9206M01        1.000000 EACH 10/28/81 BUY LABEL, DANGER
FA 170 01 54-G9206M02        1.000000 EACH 10/28/81 BUY LABEL, UNIT NUMBER
FA 180 01 30-G9302M03        1.000000 EACH 10/28/81 BUY FLAT CABLE,DSK DRV TO CNT
FA 190 01 42-G9401M01        5.000000 EACH 10/28/81 BUY TIE,CABLE 2.5X1X100

*MSGERM2
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```
 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION
 01-G2020M01              ASY,BOTTOM SET33
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING 01-G2020M01         0
SC B/M PC COMPONENT            QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
FA 130 01 80-G9619M01          1.000000 EACH 08/24/81 BUY BUZZER, CONTINUOUS 12 VDC
FA 140 01 03-G9004M01          2.000000 EACH 08/24/81 BUY SCR-METRC DIN7981 2.2X6.5
FA 150 01 01-G2017M01          1.000000 EACH 08/24/81 MAK ASY REAR PANEL 'SET33'
FA 160 01 30-G9302M04          1.000000 EACH 08/24/81 BUY CABLE ASY, FAN
*MSGERM2
 E06      SINGLE LEVEL BILL OF MATERIAL EXPLOSION
 01-G2020M01              ASY,BOTTOM SET33
DISPLAY LEVEL IS ITEM          FAMILY
DRAWING 01-G2020M01         0
SC B/M PC COMPONENT            QUANTITY U/M     DATE    TYP COMPONENT DESCRIPTION
EA 010 01 15-G4013M01          1.000000 EACH 08/24/81 BUY ENCLSR,BTTM, XR30 PNTD
FA 020 01 27-G4005M01          1.000000 EACH 08/24/81 BUY CHASSIS, INNER LEFT
FA 030 01 27-G4011M01          1.000000 EACH 08/24/81 BUY CHASSIS, INNER-RIGHT
FA 040 01 03SW993D420          8.000000 EACH 08/24/81 BUY SCR,PHFIL,M4.0X0.7X20SCYI
FA 050 01 04SW998D005          8.000000 EACH 08/24/81 BUY WSHR,LKIT,J4  X0.5SCYI
FA 060 01 04SW999D009          8.000000 EACH 08/24/81 BUY WSHR,FLT 4.3X0.8 SCYI
FA 070 01 30-G2009M02          1.000000 EACH 08/24/81 MAK PWR SUPPLY ASY, EXORSET
FA 080 01 59-G9807M01          1.000000 EACH 08/24/81 BUY FAN 220V 13/12W 50/60 HZ
FA 080 02 59NW9807A30          1.000000 EACH 03/11/82 BUY FAN,115V/50HZ/20W/160 CMH
FA 081 01 75NW9402A17          4.000000 EACH 11/03/81 BUY SHOCK,MNT RUBBER - FAN
FA 082 01 43NW9002A94          2.000000 EACH 11/03/81 BUY INSERT,BRASS-FAN
FA 090 01 03SW993D416          4.000000 EACH 08/24/81 BUY SCR,PHFIL,M4.0X0.7X16SCYI
FA 100 01 04SW998D005          4.000000 EACH 08/24/81 BUY WSHR,LKIT,J4  X0.5SCYI
FA 110 01 04SW999D009          4.000000 EACH 08/24/81 BUY WSHR,FLT 4.3X0.8 SCYI
FA 120 01 05-G9007M01          4.000000 EACH 08/24/81 BUY RIVET-NUT M4
       * MORE *
FA1300180-G9619M01
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APPENDIX A

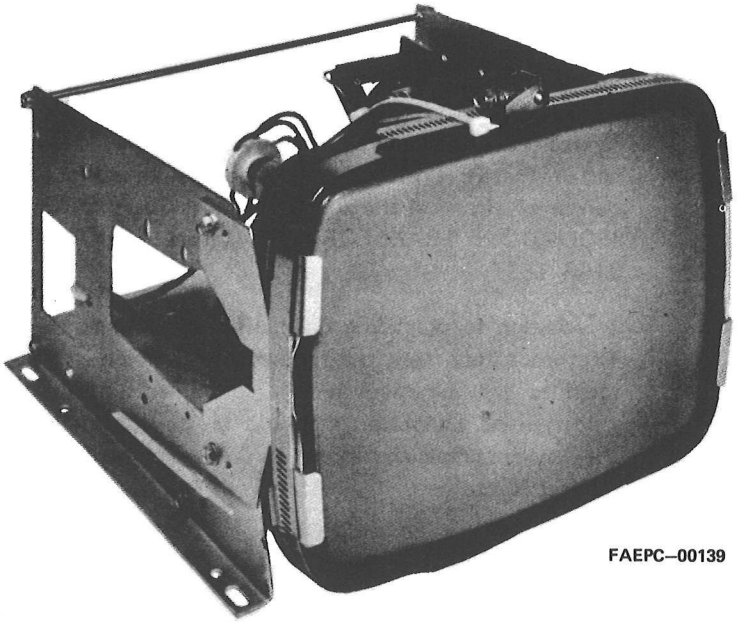
M2000 9" CRT SERVICE MANUAL

MOTOROLA INC.

Service Manual
VP16

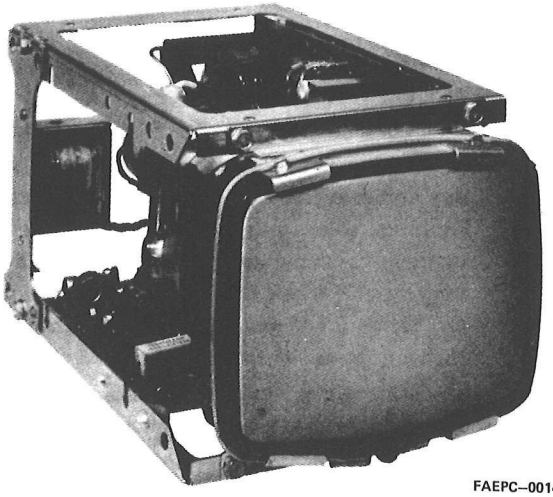
M1000 and M2000 SERIES

(See Table 1)



FAEPC–00139

MODEL M2000 (9"– CRT)



FAEPC–00140

MODEL M1000 (5" – CRT)

TABLE 1

MODEL	SIGNAL INPUT	*CRT SIZE & PHOSPHOR
M1000–100	TTL	5" P4
M1000–155	COMPOSITE	5" P4
M1000–190	DIRECT DRIVE	5" P4
M2000–100	TTL	9" P4
M2000–155	COMPOSITE	9" P4
M2000–355	COMPOSITE	9" P31

*All CRT's are without anti-reflective faceplates.

CAUTION

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

GENERAL INFORMATION

The models described herein are fully transistorized (except CRT) and applicable for displaying alphanumeric characters. All models will accept TTL or composite video inputs depending on jumper positioning. The exception is Model M1000-190 which is designed for direct drive applications only.

NOTE: The Model M2000-100 (TTL) is supplied factory wired as a model M2000-155 (composite video) version. See schematic diagram for jumper locations.

The CRT'S employed are of the magnetic deflection type with integral implosion protection. An operating voltage of 12 volts DC @ 650 mA (typical) is required from an external power supply for the M1000 models. The M2000 models require an external 12 volts DC @ 900 mA (typical).

Input and output connections for these models are made through a 10–pin edge connector on the signal circuit card. Output connections are provided for an optional remote brightness control, except on the Model M1000–190.

Two plug–in etched circuit cards are utilized, a signal circuit card and a deflection circuit card. Components are mounted on the top of the circuit cards and copper foil on the bottom. Schematic reference numbers are printed on the top and bottom of each circuit card to aid in the location and identification of components for servicing. All standard operating/adjustment controls are mounted in a convenient manner on both circuit cards.

MOTOROLA INC.

Display Systems

1299 E. Algonquin Road, Schaumburg, IL. 60196 312/397-8000

VP 16
6/81

PART NO. 68P25253A23–6
PRINTED IN U.S.A.

SAFETY WARNING

CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

1. SAFETY PROCEDURES should be developed by habit so that when the technician is rushed with repair work, he automatically takes precautions.

2. A GOOD PRACTICE, when working on any unit, is to first ground the chassis and to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.

3. Extreme care should be used in HANDLING THE PICTURE TUBE as rough handling may cause it to implode due to atmospheric pressure (14.7 lbs. per sq. in.). Do not nick or scratch glass or subject it to any undue pressure in removal or installation. When handling, safety goggles and heavy gloves should be worn for protection. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode or use a well insulated piece of wire. When servicing or repairing the monitor, if the cathode ray tube is replaced by a type of tube other than that specified under the Motorola Part Number as original equipment in this Service Manual, then avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger of personal injury from unnecessary exposure to X-ray radiation may result.

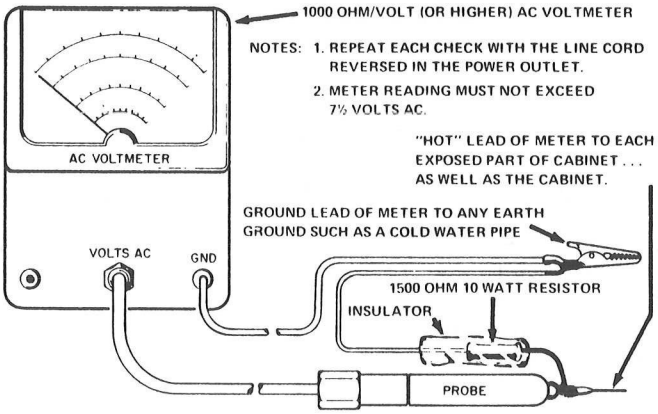
4. An ISOLATION TRANSFORMER should always be used during the servicing of a unit whose chassis is connected to one side of the power line. Use a transformer of adequate power rating as this protects the serviceman from accidents resulting in personal injury from electrical shocks. It will also protect the chassis and its components from being damaged by accidental shorts of the circuitry that may be inadvertently introduced during the service operation.

5. Always REPLACE PROTECTIVE DEVICES, such as fishpaper, isolation resistors and capacitors and shields after working on the unit.

6. If the HIGH VOLTAGE is adjustable, it should always be ADJUSTED to the level recommended by the manufacturer. If the voltage is increased above the normal setting, exposure to unnecessary X-ray radiation could result. High voltage can accurately be measured with a high voltage meter connected from the anode lead to chassis.

7. BEFORE RETURNING A SERVICED UNIT, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER WHEN MAKING THIS TEST.

In addition to practicing the basic and fundamental electrical safety rules, the following test, which is related to the minimum safety requirements of the Underwriters Laboratories should be performed by the service technician before any unit which has been serviced is returned.



Voltmeter Hook-up for Safety Check

A 1000 ohm per volt AC voltmeter is prepared by shunting it with a 1500 ohm, 10 watt resistor. The safety test is made by contacting one meter probe to any portion of the unit exposed to the operator such as the cabinet trim, hardware, controls, knobs, etc., while the other probe is held in contact with a good "earth" ground such as a cold water pipe.

The AC voltage indicated by the meter may not exceed 7½ volts. A reading exceeding 7½ volts indicates that a potentially dangerous leakage path exists between the exposed portion of the unit and "earth" ground. Such a unit represents a potentially serious shock hazard to the operator.

The above test should be repeated with the power plug reversed, when applicable.

NEVER RETURN A MONITOR which does not pass the safety test until the fault has been located and corrected.

ELECTRICAL SPECIFICATIONS *

	MODEL M1000	MODEL M2000
PICTURE TUBE (CRT):	5" measured diagonally (127 mm); 13 sq. in. viewing area (84 sq. cm); 55° deflection angle; P4 phosphor standard	9" measured diagonally (228 mm); 44 sq. in viewing area (284 sq.cm); 90° deflection angle; integral implosion protection; P4 phosphor standard except P31 phosphor in Model M2000-355.
POWER INPUT:	12V DC at 650 mA	12V DC at 900 mA
INPUT SIGNALS:	COMPOSITE VIDEO INPUT: 0.5V to 2.5V composite P/P, sync negative (input impedance: 74 ohms terminated, 12k ohms unterminated), or TTL INPUT: 2.5V to 5.0V P/P, video drive, sync positive at input (input impedance: 75 ohms video termination, >2k ohms vertical and horizontal) DIRECT DRIVE INPUT: 2.5V to 5.0V P/P, video drive, negative vertical sync (190 uSec Min., 400 uSec max.), positive horizontal drive (25 uSec min. to 30 uSec max.). (Input impedance: 75 ohms video termination,>330 ohms horizontal drive,>2k ohms vertical sync.)	
RESOLUTION:	650 lines center, 500 lines corners	
VIDEO RESPONSE:	Within −3 dB,10 Hz to 12 MHz	
LINEARITY:	Within 2% as measured with standard EIA ball chart and dot pattern	
HIGH VOLTAGE:	9.0 kV at 50 uA beam current, nominal	
HORIZONTAL RETRACE TIME:	11.0 uSec maximum	
SCANNING FREQUENCY:	Horizontal: 15,750 Hz ±500 Hz; Vertical: 50/60 Hz	
ENVIRONMENT:	Operating temperature: 0° C to 50° C Storage temperature: −40° C to +65° C Operating altitude: 10,000 feet maximum (3048 meters) Designed to comply with applicable DHEW rules on X-Radiation Designed to enable listing under UL Specification 478	
TYPICAL DIMENSIONS:	4.60" H, 5.12" W, 8.68" D (without power supply) (117 x 130 x 220 mm)	7.25" H, 9.50" W, 9.48" D (184 x 241 x 241 mm)

* Specifications subject to change without notice.

TABLE OF CONTENTS

SERVICE NOTES

CIRCUIT TRACING

Component reference numbers are printed on the top and bottom of the plug-in circuit cards to facilitate circuit tracing. In addition, control names and circuit card terminal numbers are also shown and referenced on the schematic diagrams in this manual.

Transistor elements are identified as follows:

E – emitter, B – base, and C – collector.

COMPONENT REMOVAL

Removing components from an etched circuit card is facilitated by the fact that the circuitry (copper foil) appears on one side of the circuit card only and the component leads are inserted straight through the holes and are not bent or crimped.

It is recommended that a solder extracting gun be used to aid in component removal. An iron with a temperature controlled heating element would be desirable since it would reduce the possibility of damaging the circuit card foil due to overheating.

The nozzle of the solder extracting gun is inserted directly over the component lead and when sufficiently heated, the solder is drawn away leaving the lead free from the copper foil. This method is particularly suitable in removing multi-terminal components.

POWER TRANSISTOR REPLACEMENT

When replacing the "plug-in" transistor, please observe the following precautions:

1. The transistor heat sink is not "captive", which means that the transistor mounting screws also secure the heat sink. When installing the transistor, the heat sink must be held in its proper location.

2. When replacing the plug-in transistor, silicone grease (Motorola Part No. 11M490487) should be applied evenly to the top of the heat sink and bottom of the transistor.

3. The transistor mounting nuts must be tight before applying power to the monitor. This insures proper cooling and electrical connections. NON–COMPLIANCE WITH THESE INSTRUCTIONS CAN RESULT IN FAILURE OF THE TRANSISTOR AND/OR ITS RELATED COMPONENTS.

– NOTE –

Use caution when tightening transistor mounting nuts. If the screw threads are stripped by excessive pressure, a poor electrical and mechanical connection will be made.

CRT REPLACEMENT

Use extreme care in handling the CRT as rough handling may cause it to implode due to high vacuum. Do not nick or scratch glass or subject it to any undue pressure in removal or installation. Use goggles and heavy gloves for protection. In addition, be sure to disconnect the monitor from all external voltage sources.

1. Discharge CRT by shorting 2nd anode to ground; then remove the CRT socket, deflection yoke and 2nd anode lead.

2. Remove CRT from chassis by loosening the one screw that secures the CRT mounting strap or retaining ring.

3. Install new CRT and proceed to horizontal linearity, centering and beam alignment procedures.

HORIZONTAL OSCILLATOR ADJUSTMENT

– NOTE –

Not applicable to Model M1000–190.

Step 1. Turn on monitor and set up for normal operation.

Step 2. Locate the HORIZ. HOLD control, R35, on the Signal circuit card.

Step 3. Begin rotating R35 CCW until the video display is out of horizontal sync. At this point rotate R35 back CW until the video display just locks in horizontally; then stop. Using tape, mark the left–hand edge of the video display (not the raster edge) of the CRT faceplate.

Step 4. Continue rotating R35 CW until the video display is out of horizontal sync again in the opposite direction. At this point rotate R35 back CCW until the video just locks in horizontally; then stop. Mark the left–hand edge of the video display on the CRT faceplate again.

Step 5. Observe the distance between the two marks on the CRT faceplate. The object is to rotate the HORIZ. HOLD control, R35, until the left–hand edge of the video display is centered between the two marks on the CRT faceplate.

VIDEO BIAS ADJUSTMENT

– NOTE –

Not applicable to Model M1000–190.

Step 1. With the monitor operating, rotate the CONTRAST CONTROL, R6,for minimum contrast; then disconnect the input signal(s).

Step 2. Connect a voltmeter across R18 (negative probe toward the collector of Q4).

Step 3. Adjust the VIDEO BIAS control, R14, for a +2.0 $\pm$.05 volt indication.

Step 4. Disconnect the voltmeter.

Step 5. Reconnect the input signal(s) and adjust the CONTRAST control, R6, for desired contrast.

HORIZONTAL LINEARITY ADJUSTMENT

– NOTE–

This adjustment procedure is required only when a CRT and/or deflection yoke have been replaced.

PROCEDURE

Step 1. Disconnect monitor from power supply.

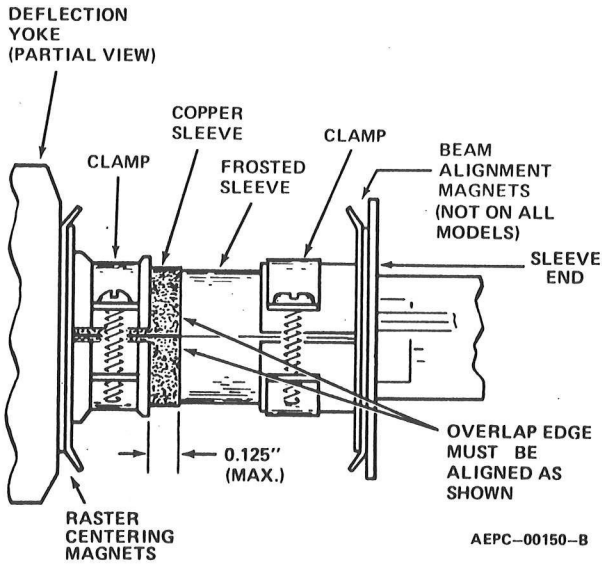


Figure 1. Partial View of CRT Neck/Deflection Yoke for Horiz. Linearity Adjustment

Step 2. (M2000 ONLY) Locate the S–SHAPING transformer, T3, on the deflection circuit card; then rotate its slug down to the bottom. (This action temporarily minimizes the effect of T3 being in the circuit.)

Step 3. (Refer to Figure 1.) Loosen the deflection yoke clamp screw just enough to permit sliding the copper sleeve on the CRT neck back and forth.

Step 4. (Refer to Figure 1.) Position the copper sleeve so that only 1/8" (.125") extends out past the rear lip of the deflection yoke. In addition, be sure that the overlap edge of the copper sleeve is aligned properly and not twisted.

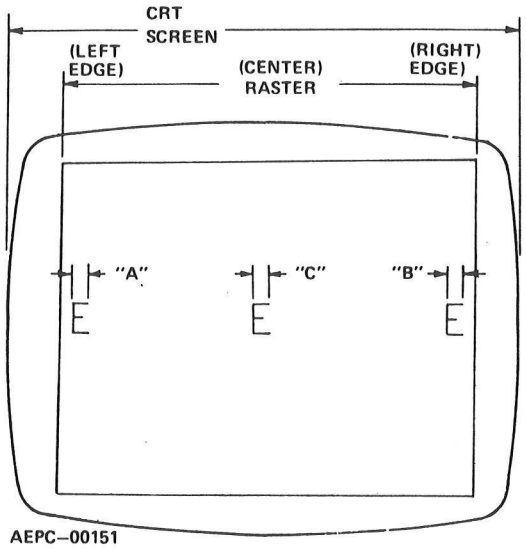


Figure 2. Partial CRT Raster Display of Characters for Adjustment

Step 5. Tighten the clamp screw carefully so as not to disturb the yoke position.

Step 6. Connect the monitor to its power supply and set up for normal operation.

Step 7. (Refer to Figure 2.) Observe the extreme left-hand edge characters (designated "A" in Figure 2). Its width should be equal to the width of the right–hand edge characters (designated "B" in Figure 2). If character "A" is wider than character "B", the copper sleeve is extending out too far. If "A" is narrower than "B", the copper sleeve should be pulled out further. In any event, the copper sleeve may have to be repositioned by trial and error if the 0.125–inch dimension does not provide desired linearity. Continue until the width of character "A" is equal to the width of character "B".

— NOTE —

Steps 8–11 are applicable only for the M2000 monitor.

Step 8. With the M2000 monitor turned on and operating normally, observe the width of the center character (designated "C" in Figure 2). It should be narrower than characters "A" and "B".

Step 9. Connect an oscilloscope (AC coupled) between the blue wire pin (on deflection circuit card) and chassis ground. A parabolic waveform should appear.

Step 10. Begin rotating the slug of T3 upward (away from circuit card) until the amplitude of the waveform is 125 volts P–P. This setting will equalize the width of character "C" to that of characters "A" and "B".

Step 11. Disconnect oscilloscope.

RASTER CENTERING (Figure 1)

– NOTE –

For Model M1000–190 refer to video centering. For models without beam alignment magnets, proceed to Step 2. Raster centering is factory set and should not normally require further adjustment.

Step 1. Position the tabs of the beam alignment magnets such that they are horizontally opposing.

Step 2. Adjust vert. size (R52) and horiz. width (L1) such that all edges of the raster are visible.

Step 3. Position raster centering magnets for best centering of raster.

Step 4. Readjust size to specified dimensions or approximately 3 3/4" wide x 2 5/8" high for M1000 series and 6½" wide x 4" high for M2000 series monitors.

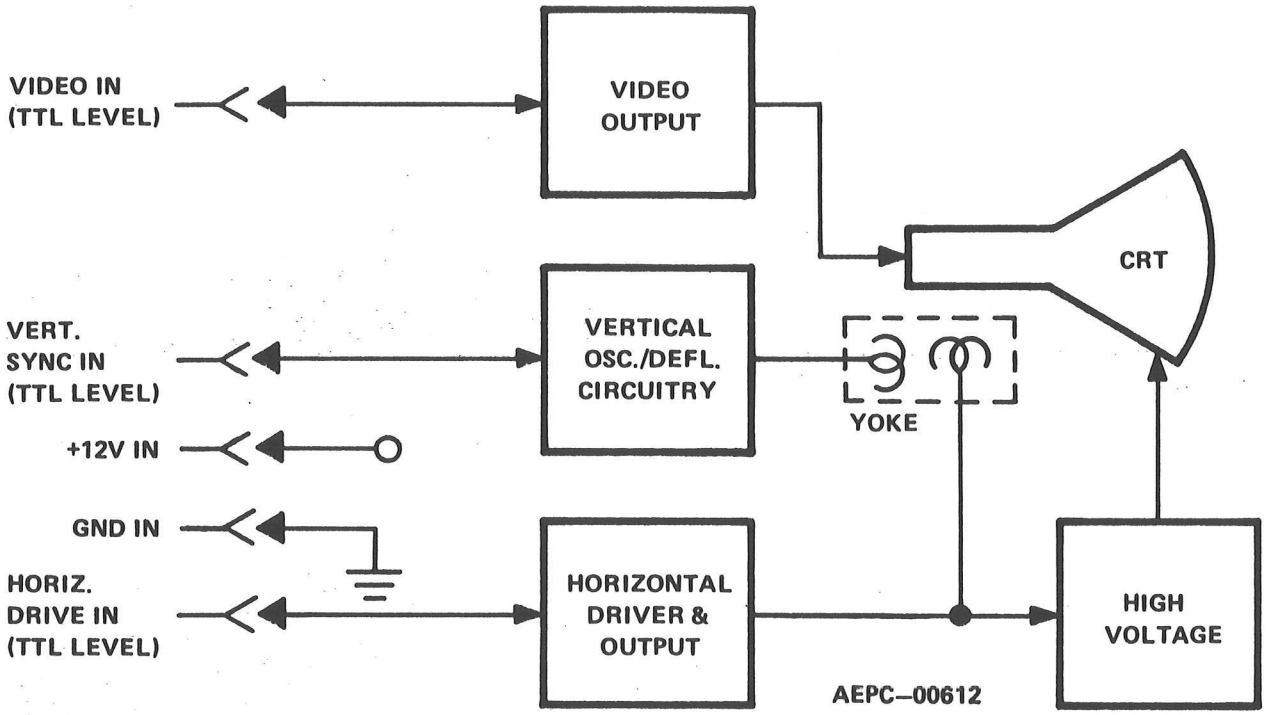
VIDEO CENTERING (For M1000–190 only) (Figure 1)

– NOTE –

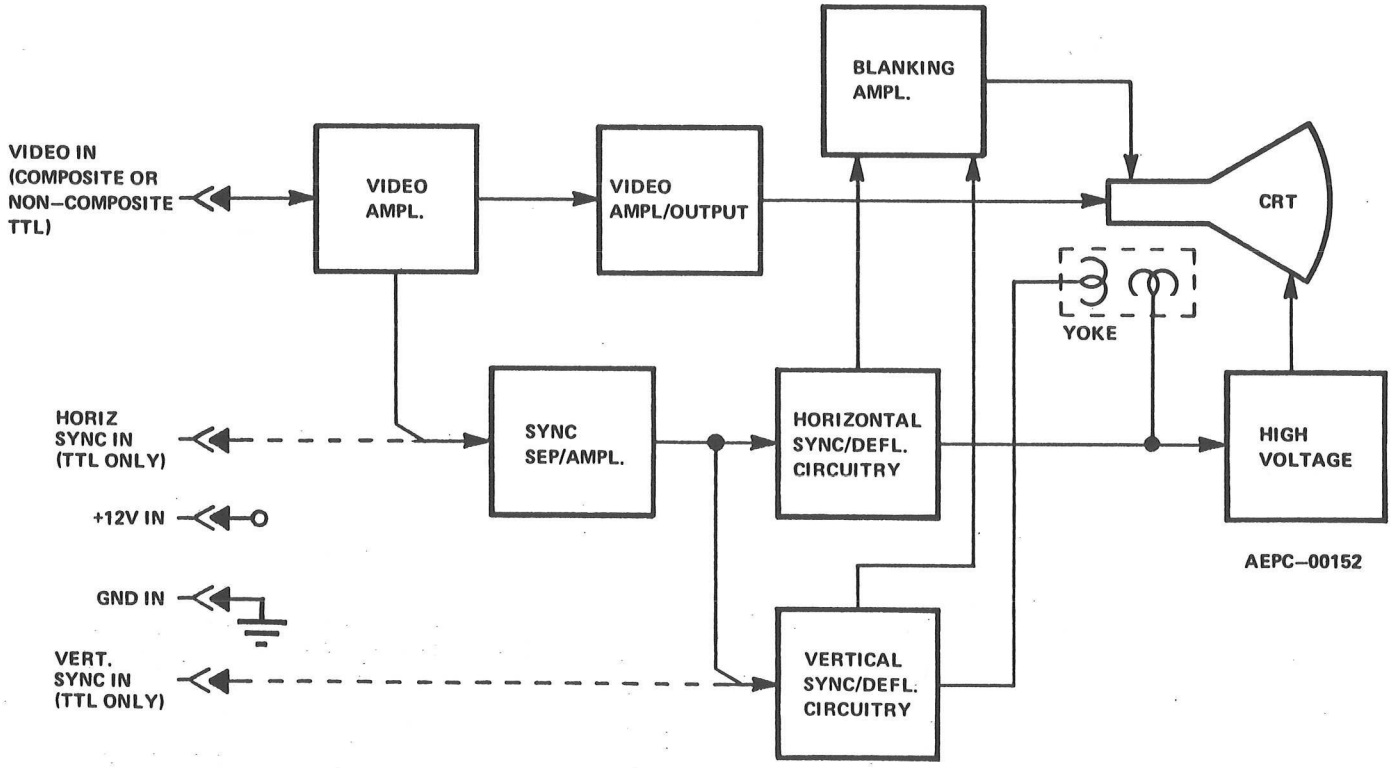
For models without beam alignment rings, proceed to Step 2. Video centering is factory set and should not normally require further adjustment.

Step 1. Position the tabs of the beam alignment magnets such that they are horizontally opposing.

Step 2. Adjust vert. size (R52) and horiz. width (L1) such that all edges of the video are visible.



Block Diagram (Model M1000–190 only)



Block Diagram (All Models except M1000–190)

Step 3. Position raster centering magnets for best centering of video.

Step 4. Readjust size to specified dimensions or approximately 3 3/4" wide x 2 5/8" high for M1000 series and 6 ½" wide x 4" high for M2000 series monitors.

CRT BEAM ALIGNMENT (Figure 1)

For optimum character quality in the corners of the video display, a beam alignment magnet may be used on the monitor CRT. If not used disregard the following procedure.

– NOTE –

Adjustment of the raster centering rings must precede the adjustment of the beam alignment magnet.

PROCEDURE

The beam alignment magnet should be positioned on the neck of the CRT between the deflection yoke and the tube base. The correct location of the rings is approximately over the second grid of the electron gun (Figure 1).

Step 1. Adjust the display brightness for optimum viewing.

Step 2. Adjust the focus voltage for optimum overall focus.

Step 3. Loosen the beam alignment magnet clamping screw just enough to allow the assembly free movement on the CRT neck.

Step 4. While observing the tails on the dots in the corners of the display, rotate the focus rings to minimize the tails.

Step 5. Tighten the clamping screw.

THEORY OF OPERATION

GENERAL

The following circuit description is applicable to monitors using a composite video input signal. For monitors using TTL inputs, the description is basically the same. However, the horizontal and vertical sync pulses are coupled from an external source through separate inputs. In addition, jumpers JU 1 and JU2 will be relocated to the TTL position.

The direct drive model M1000–190 utilizes only output circuitry. The development and processing of the driving signals is performed externally from the monitor and applied to separate inputs similar to the TTL models. Therefore, the following circuit descriptions are also applicable to the direct drive version. (See block diagrams.)

VIDEO AMPLIFIER CIRCUIT (Figure 3.)

The video amplifier consists of four stages that include Q1, Q2, Q3 and Q4. The first stage, Q1, functions as an emitter follower. The low output impedance of this first stage permits use of a low resistance CONTRAST control, R6, which furnishes flat video response over its entire range without the need for compensation. The collector output of Q1 is used to drive the sync separator, Q5. Capacitor C2 provides high frequency roll–off to limit the collector output to the bandwidth required to pass synchronization signals.

Transistors Q2 and Q3 form a direct coupled amplifier with frequency compensation provided by C40 and C41. The output from Q3 is capacitively coupled (C5) to the base of Q4, video output stage. The video bias control, R14, is used to set the quiescent collector current of Q4. Frequency compensation is provided by R17 and C6. The combined action of clamping diode D1 and capacitor C5 provide DC restoration for the video signal.

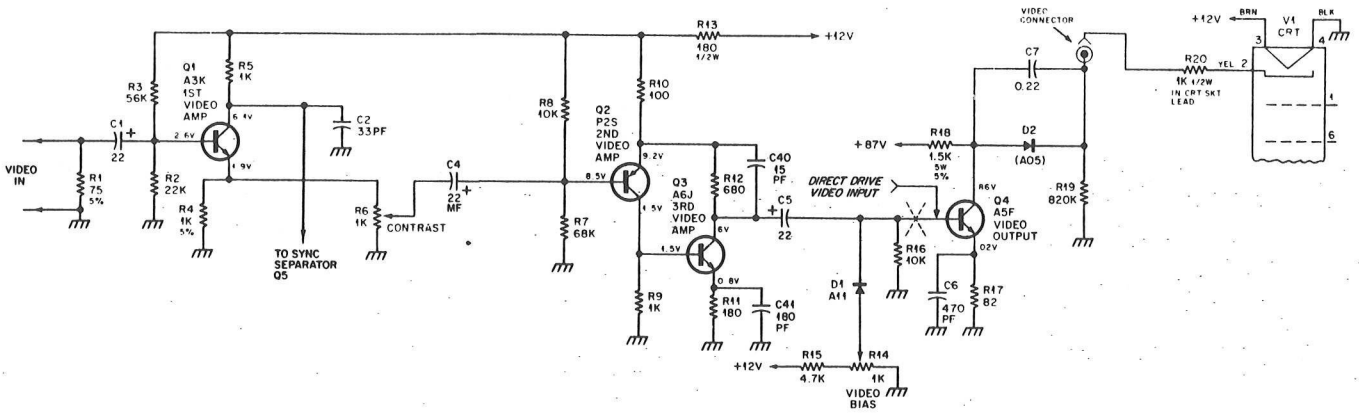


Figure 3. Video Amplifier Circuit

Components C7, D2 and R19 provide CRT beam current limiting. Diode D2 is normally forward–biased; therefore, as Q4 conducts, its collector voltage drops. This causes a larger beam current to flow through R19, which in turn causes its voltage drop to rise. If excessive beam current flows, the voltage developed across R19 becomes greater than the collector voltage of Q4. This action reverse-biases D2, which prevents a further increase in beam current. Capacitor C7 helps couple video to the CRT cathode, pin 2, through R20. Resistor R20 is used to isolate Q4 from transients that may occur as a result of CRT arcing.

SYNC SEPARATOR/AMPLIFIER CIRCUIT

(Reference Figure 4.)

The sync separator employs two stages. Transistor Q5 is the sync separator and Q6 is the sync amplifier. The video input to the sync separator is black positive. Capacitor C3 is charged by the peak base current that flows when the positive peak of the input takes Q5 to saturation. This charge depends on the peak to peak input to Q5 and thus makes the bias for Q5 track the amplitude of the input signal. As a result, Q5 amplifies only the positive peaks of the input signal. The initial bias current through R23 sets the clipping level.

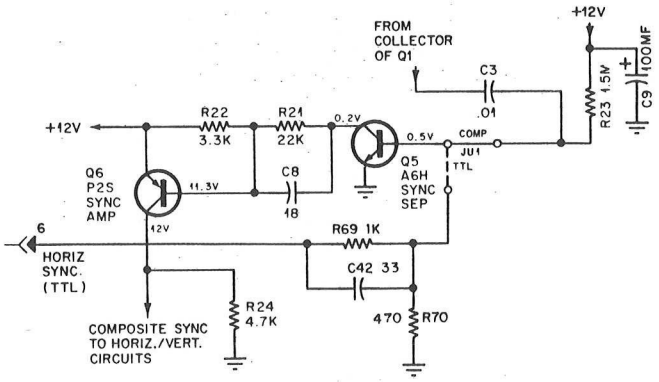


Figure 4. Sync Separator/Amplifier Circuit

PHASE DETECTOR (AFC)

(Reference Figure 5.)

The phase detector control consists of two diodes (D3 & D13) in a keyed clamp circuit. Two inputs are required to generate the required output, one from the sync amplifier, Q6, and one from the horizontal output circuit, Q8. The required output must be of the proper polarity and amplitude to correct phase differences between the input horizontal sync pulses and the horizontal time base. The horizontal output (Q8) collector pulse is integrated into a sawtooth by R28, C13 and R29. During horizontal sync time, both diodes conduct, which shorts C13 to ground. This effectively clamps the sawtooth on C13 to ground at sync time. If the horizontal time base is in phase with the sync (waveform A), the sync pulse will occur when the sawtooth is passing through its AC axis and the net charge on C13 will be zero (waveform B). If the horizontal time base is lagging the sync, the sawtooth on C13 will be clamped to ground at a point negative from the AC axis. This will result in a positive DC charge on C13 (waveform C). This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag. Likewise, if the horizontal time base is leading the sync, the sawtooth on C13 will be clamped at a point positive from its AC axis. This results in a net negative charge on C13, which is the required polarity to slow the horizontal oscillator (waveform D).

Passive components R30, R31 and C16 comprise the phase detector filter. The bandpass of this filter is chosen to provide correction of horizontal oscillator phase without ringing or hunting. Optional capacitor C14 (when present) times the phase detector for correct centering of the picture on the raster.

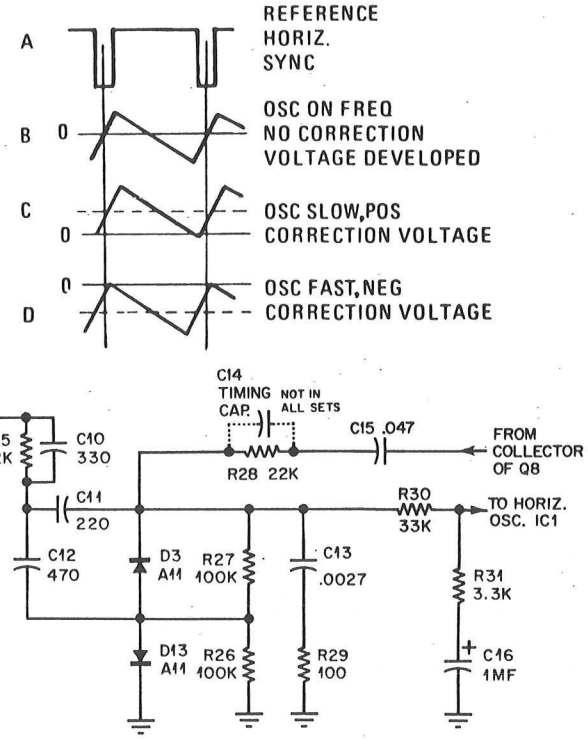


Figure 5. Phase Detector (AFC) Circuit

HORIZONTAL OSCILLATOR AND DRIVER

(Reference Figure 6.)

The horizontal oscillator consists of integrated circuit IC1, which is essentially a voltage controlled oscillator with variable mark–space ratio (duty cycle) and internal voltage reference. The reference voltage is present at pin 6, while resistors R37 and R38 determine the mark–space ratio. The main oscillator timing capacitor is C17, with its charging current derived from three sources: (a) a fixed current from R33, (b) a variable current from R34 and HORIZ. HOLD control R35, (c) and a correcting current from the phase detector (AFC) network through R32. The combination of these three charging currents and C17 determine the horizontal frequency.

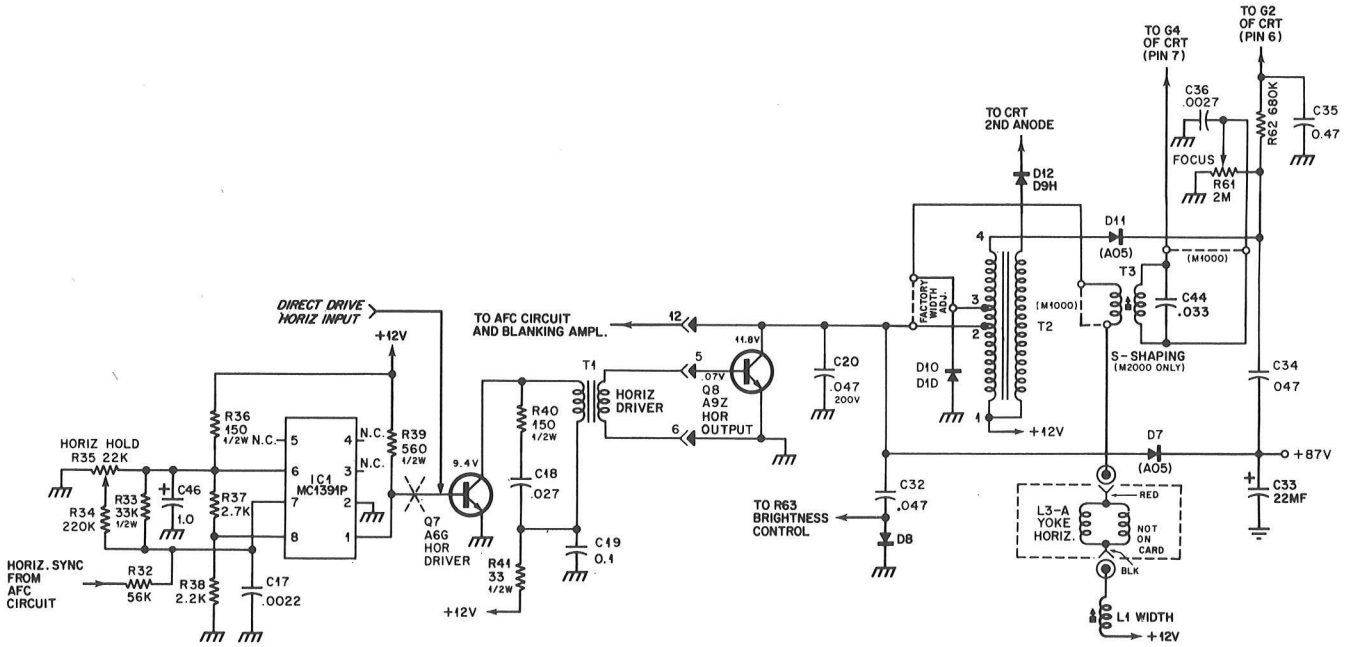


Figure 6. Horizontal Circuit

The output from IC1 (pin 1) is a square wave of proper frequency and duration, which is applied to the base of horizontal driver Q7. The output from Q7 is coupled via the horizontal driver transformer T1 (current step–up) to the base of horizontal output device Q8. Components R41 and C19 provide current limiting, while components R40 and C18 provide transformer damping to suppress ringing in the primary of T2 when Q7 goes into cutoff.

HORIZONTAL OUTPUT
(Reference Figure 6.)

The secondary of T1 provides the required low drive impedance for Q8. Once during each horizontal period, Q8 operates as a switch that connects the supply voltage across the parallel combination of the horizontal deflection yoke (L3–A) and the primary of the high voltage transformer, T2. The required sawtooth deflection current (through the horizontal yoke) is formed by the L–R time constant of the yoke and primary winding of transformer T2. The horizontal retrace pulse charges C33 through D7 to provide +87V.

Momentary transients at the collector of Q8, should they occur, are limited to the voltage on C33 since D7 will conduct if the collector voltage exceeds this value.

The damper diode, D10, conducts during the period between retrace and turn on of Q8. Capacitor C20 is the retrace tuning capacitor. Coil L1 is a series HORIZ. WIDTH control. Components C32 and D8 generate a negative voltage necessary to properly bias the CRT. A copper sleeve on the neck of the CRT shapes the horizontal magnetic field for proper linearity.

Pin 4 of the high voltage transformer, T2, is a boost winding, which together with components D11 and C34, develops a +400 volts for G2 of the CRT. This same +400 volts is also always present on the high side of FOCUS control R61.

— NOTE —

In the M2000 monitor (only), an S–shaping transformer, T3, and capacitor C44 provide additional shaping of the horizontal deflection yoke current for proper linearity.

DYNAMIC FOCUS (M2000 ONLY)
(Reference Figure 6.)

Due to the geometry of a CRT, the electron beam travels a greater distance when deflected to a corner as compared to the distance traveled at the center of the CRT screen. As a result of these various distances traveled, optimum focus can be obtained at only one point. An adequate adjustment can be realized by setting the focus while viewing some point midway between the center of the CRT screen and a corner, thus optimizing the overall screen focus. One of the simplest methods for improvement is to modulate the focus voltage at a horizontal sweep rate. Now optimum focus voltage is made variable on the horizontal axis of the CRT, which compensates for the beam travel along this axis.

In the M2000, the secondary of T3 generates a parabolic voltage, which together with a fixed voltage from the FOCUS control R61, is applied to the focus grid of V1. This system dynamically changes the value of focus voltage from the CRT screen center to screen edge, which will always provide an optimum amount of voltage for best overall focus.

VERTICAL OSCILLATOR, DRIVER AND OUTPUT
(Reference Figure 7.)

Composite sync pulses from the collector of Q6, Sync Ampl., are applied to the double integrating network of R45, C23, R46 and C24. The horizontal component of the sync signal is removed, leaving only the vertical sync pulses. The vertical sync pulses are coupled to the free running ver-

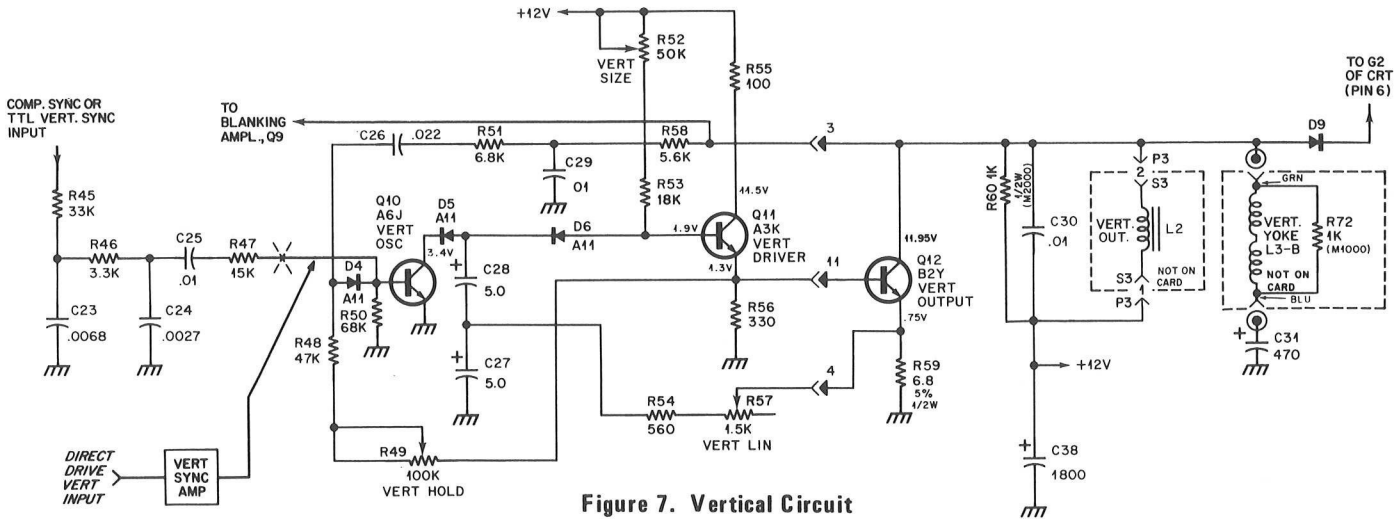
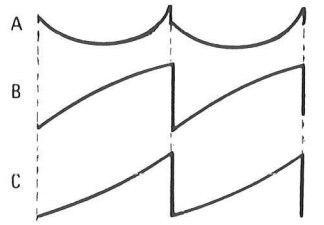


Figure 7. Vertical Circuit



PARABOLA AT JUNCTION OF C27 AND C28

VERTICAL DRIVE WITHOUT VERT PARABOLA ADDED

PARABOLA PULSE AND VERTICAL SAWTOOTH ADDED TOGETHER, WHICH PRODUCES THE REQUIRED VERT DRIVING SIGNAL.

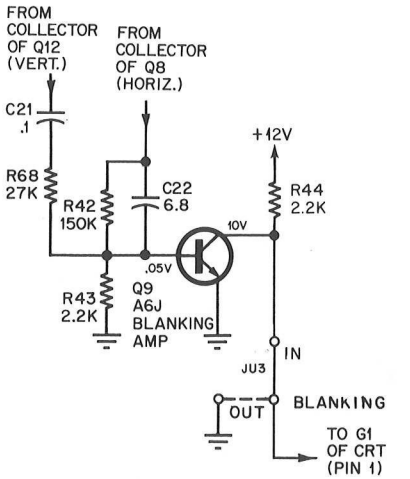


Figure 8. Blanking Amplifier

tical oscillator stage, Q10, by C25 and R47. Transistors Q10 and Q12 are connected as a multivibrator. Transistor Q11 is used as an emitter follower that provides a low impedance drive for the vertical output stage, Q12. The series combination of capacitors C27 and C28 are initially charged to the supply voltage through R53 and the VERT. SIZE control, R52, which generates an exponential ramp of voltage.

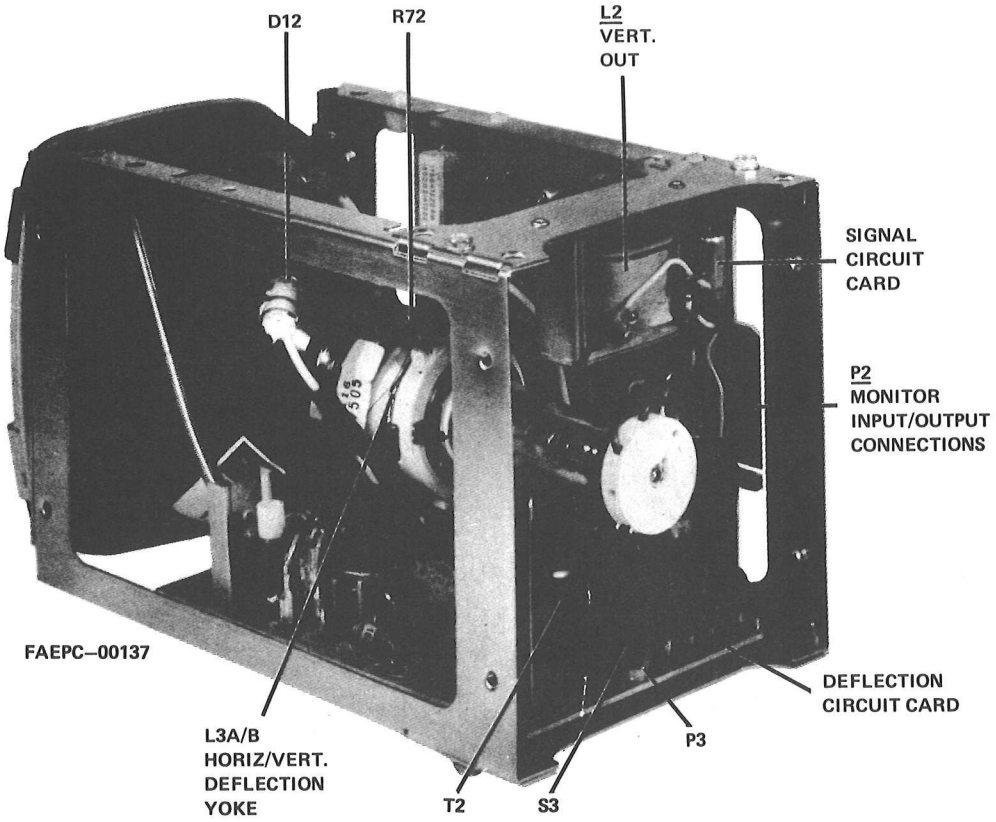
When a positive vertical sync pulse is applied to the base of Q10, it begins conducting, which immediately discharges C27 and C28. This action turns off Q11 and causes a sudden decrease in the collector current of Q12, which also decreases the vertical deflection current through deflection yoke (L3–B) and vertical choke (L2). The resultant rapidly collapsing field in L2 generates a large voltage spike that is used for vertical retrace. Components R58, C29, R51 and C26 shape this spike to ensure that Q10 remains conducting until retrace is carried out to completion. Diode D4 couples the shaped spike to the base of Q10. At this point, Q10 reverts to its non–conducting state and the cycle repeats. The VERT HOLD control, R49, and R48, provide a feedback signal to Q10 to maintain oscillation in the event vertical sycn pulses are not present. Diodes D5 and D6 provide the proper voltage drops to operate Q12 class A.

Vertical linearity is maintained by applying the ramp voltage generated across R59, through R57 (VERT LIN control) and R54, to the junction of C27 and C28. Since this path is resistive, the waveform will be integrated into a parabola by C27 (Waveform A). This results in a predistortion of the ramp waveform (waveform C). (Waveform B illustrates the drive sawtooth without parabola shaping.) Parabolic shaping is necessary to compensate for the nonlinear charging of C27 and C28, and the impedance change occuring in L2 with current. Capacitor C31 serves to remove the DC component of the vertical deflection yoke current. Diode D9 clamps the collector voltage of Q12 to a safe level.

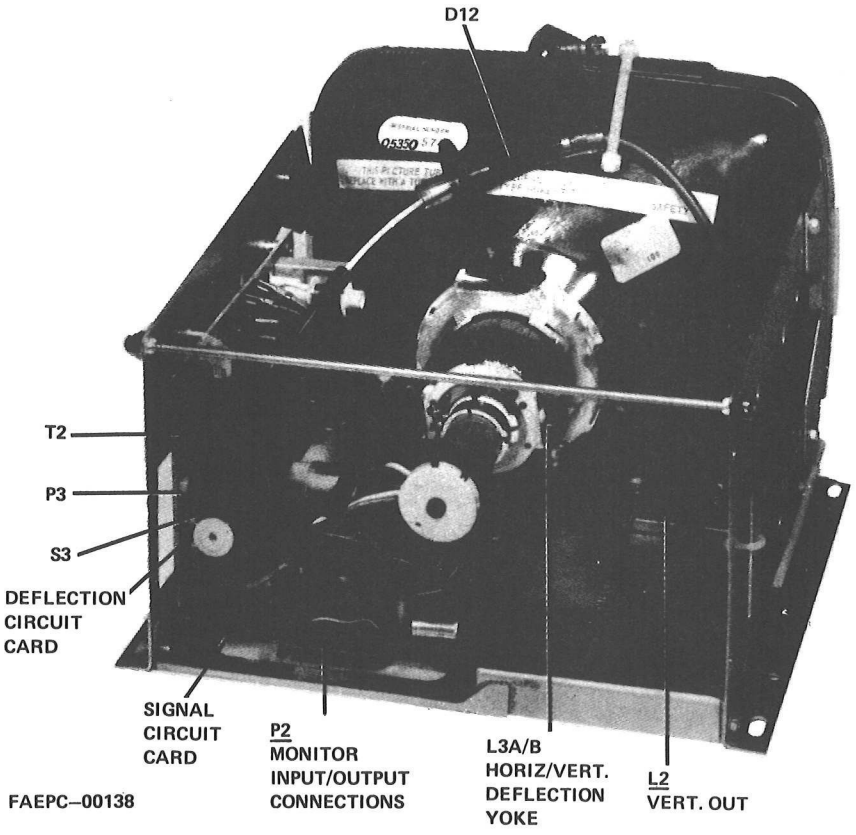
RETRACE BLANKING (NOT ON M1000–190)

(Reference Figure 8.)

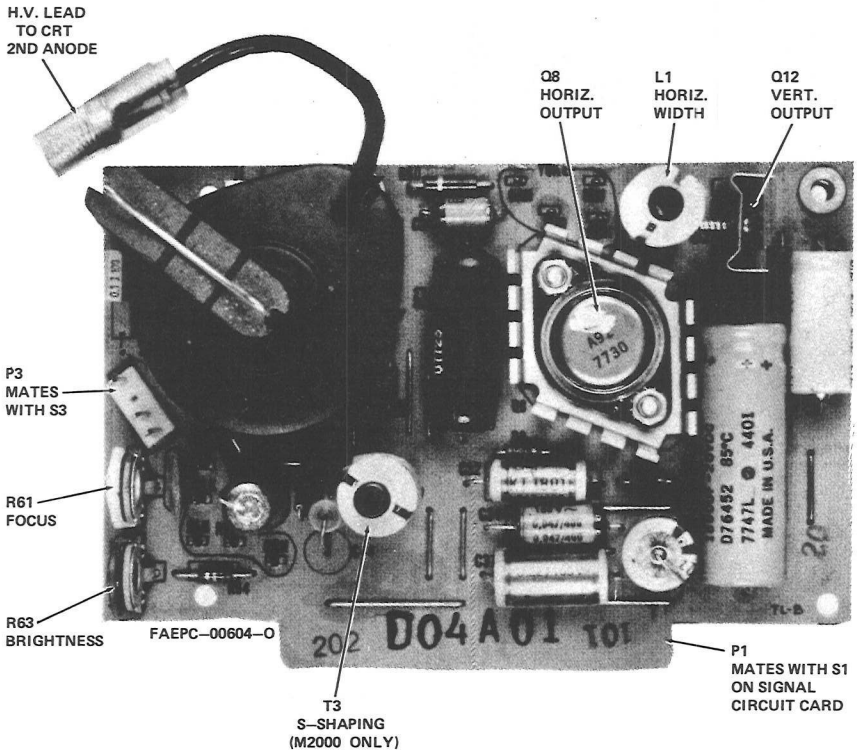
Retrace blanking is provided by negative–going horizontal and vertical rate pulses applied to G1 of the CRT. The collector pulse from the horizontal output stage, Q8, is developed across R43 through R42 and C22. The collector pulse from the vertical output stage, Q12, is differentiated by C21 to remove the sawtooth portion of the waveform. The remaining pulse appears across R43. The mixed vertical and horizontal pulses on R43 are amplified and inverted by the blanking amplifier, Q9, and applied to G1 of the CRT.



Model M1000 — Rear Chassis View

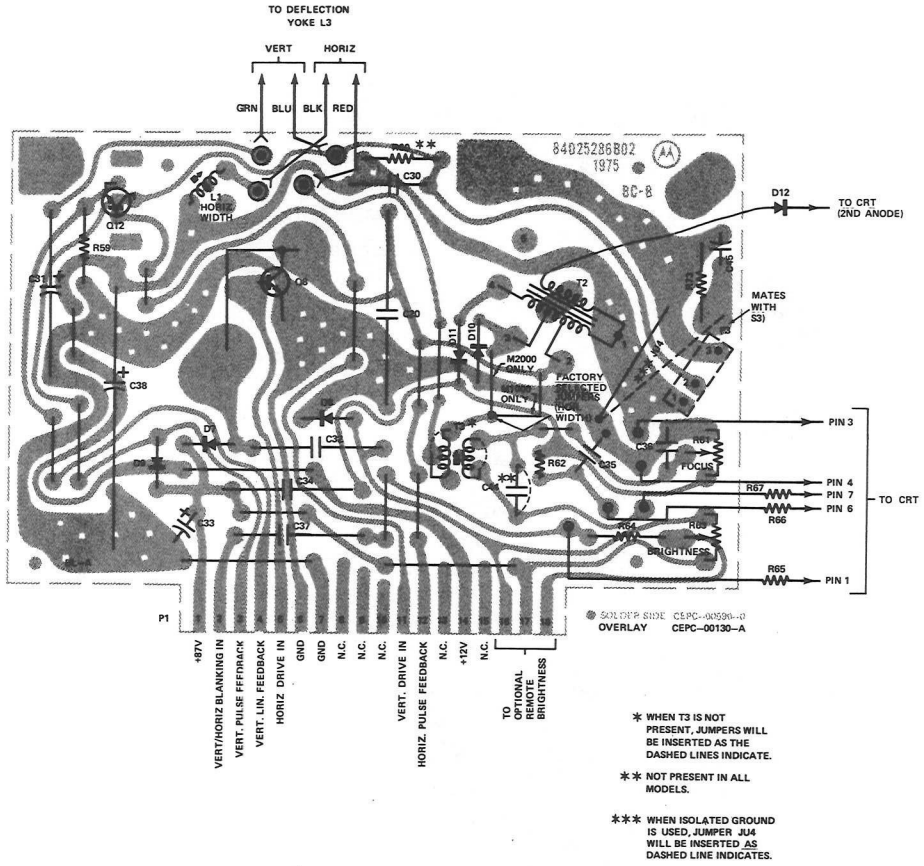


Model M2000 — Rear Chassis View



Deflection Circuit Card — Component Side

—SOLDER SIDE SHOWN—

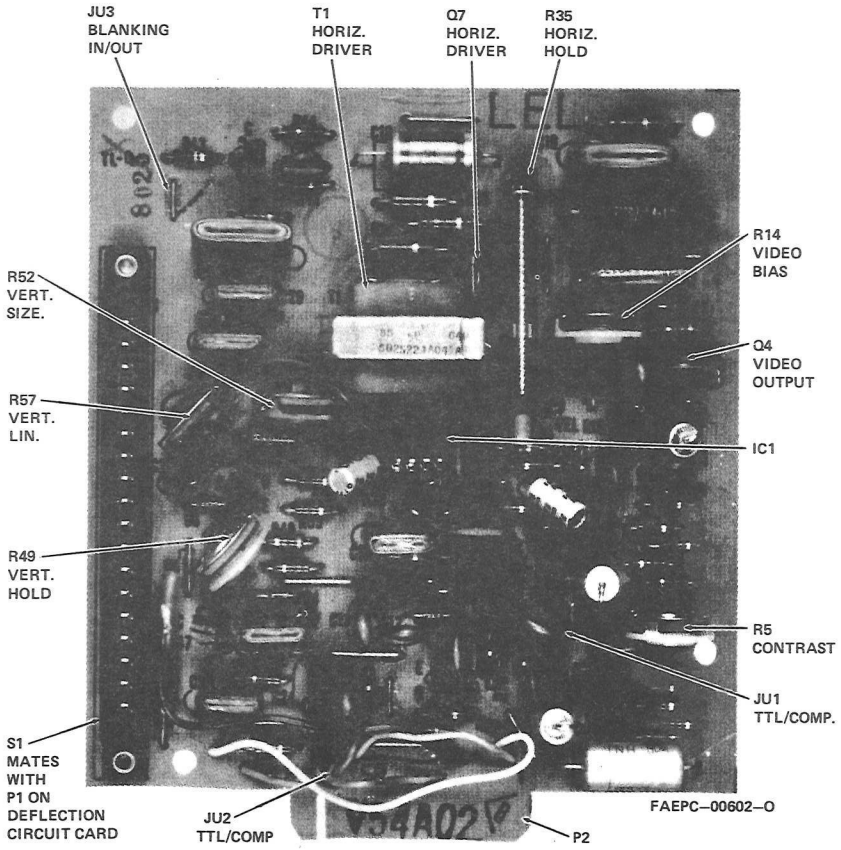


* WHEN T3 IS NOT PRESENT, JUMPERS WILL BE INSERTED AS THE DASHED LINES INDICATE.

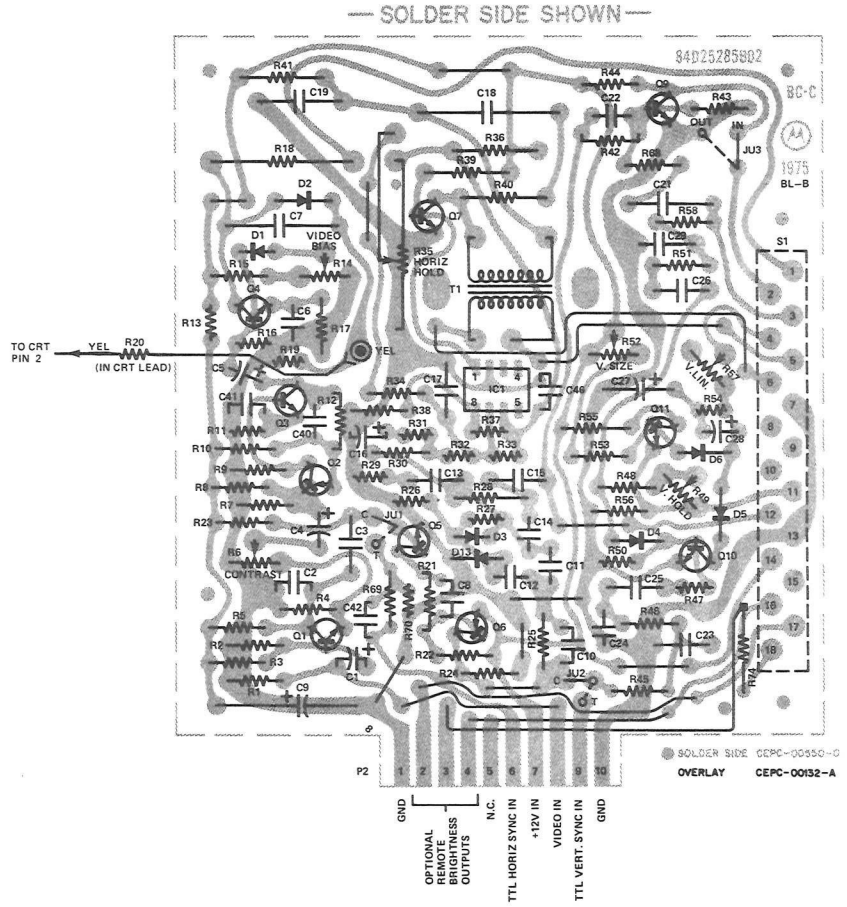
** NOT PRESENT IN ALL MODELS.

*** WHEN ISOLATED GROUND IS USED, JUMPER JU4 WILL BE INSERTED AS DASHED LINE INDICATES.

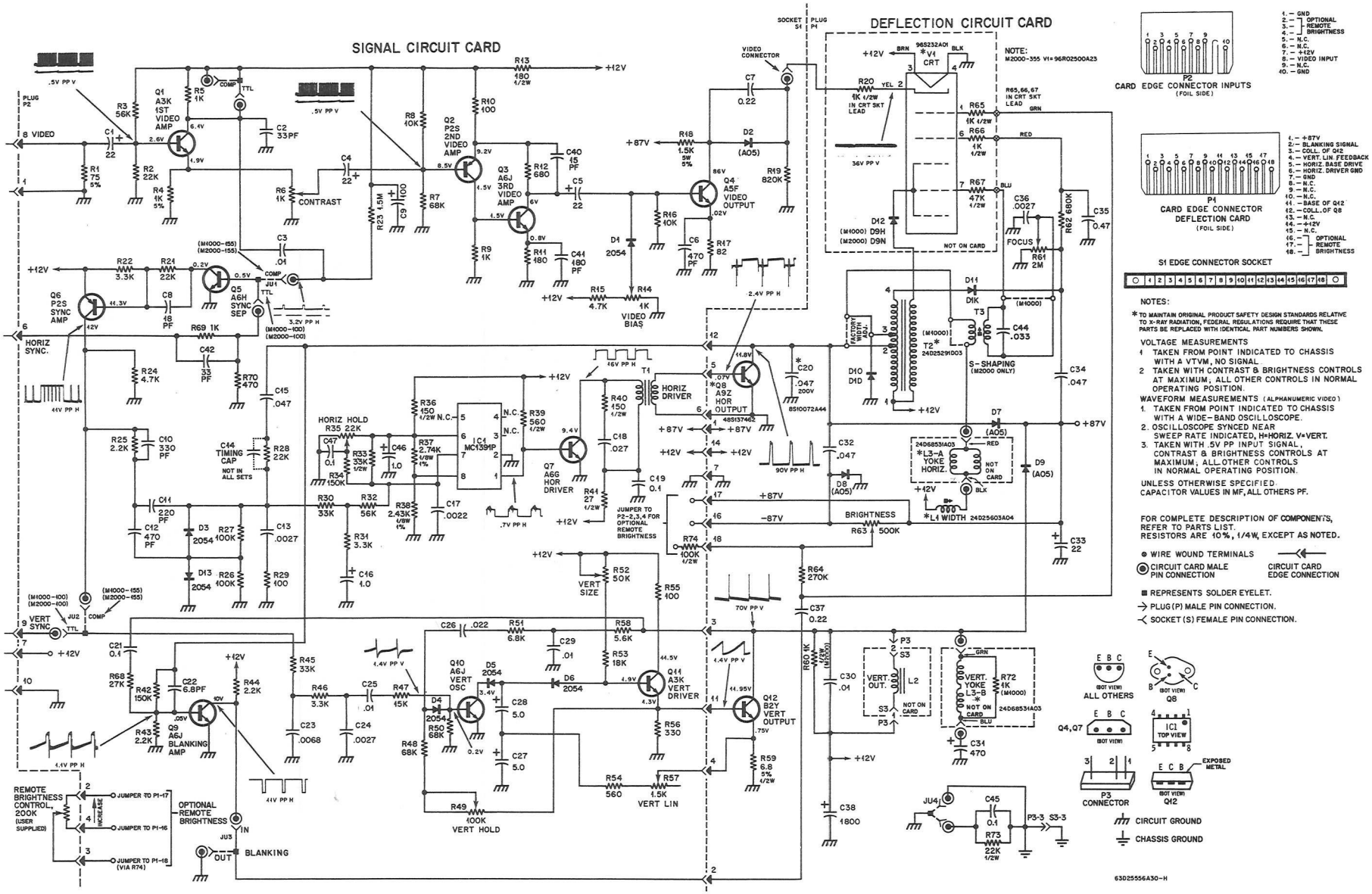
Deflection Circuit Card — Solder Side



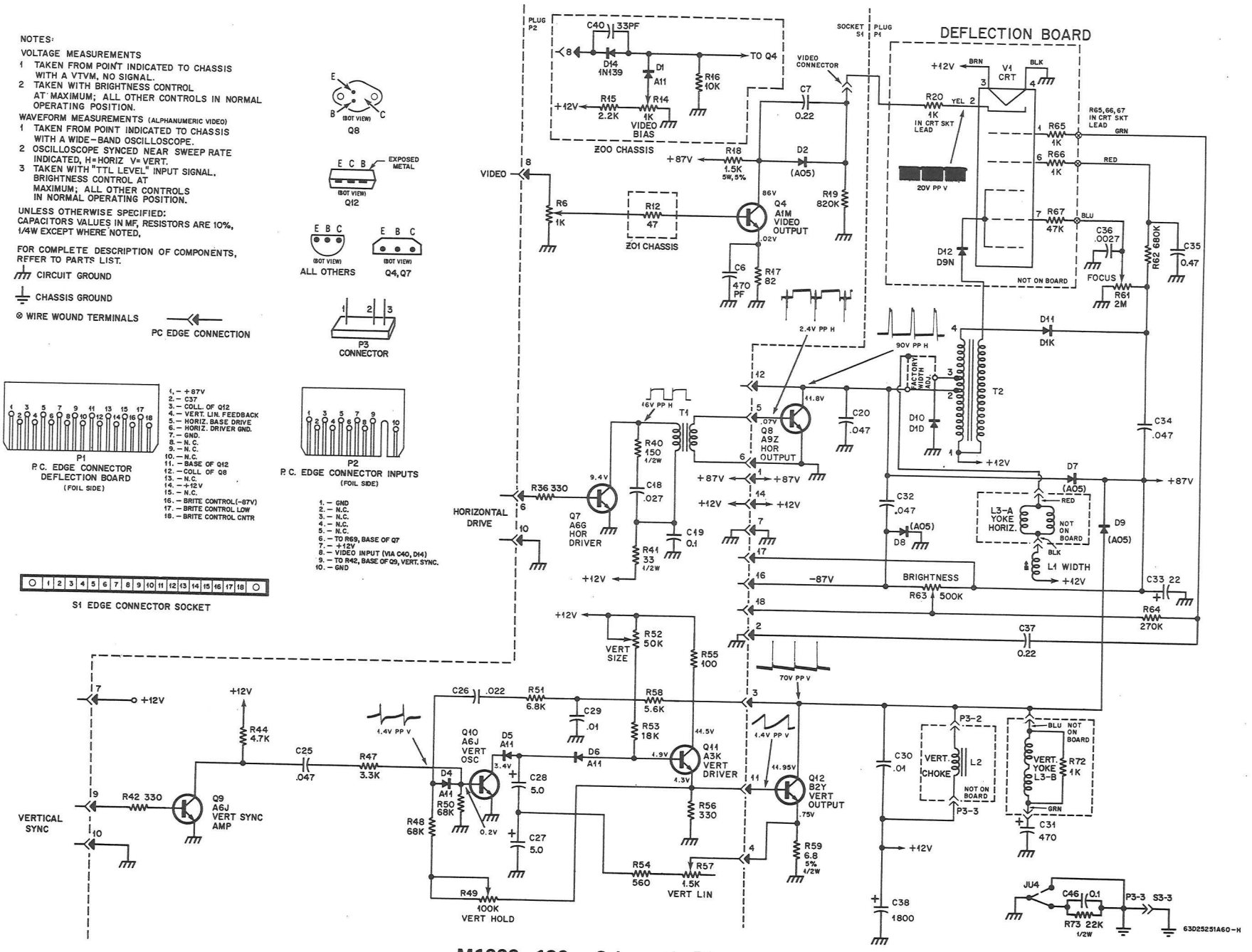
Signal Circuit Card — Component Side (All Models except M1000–190)



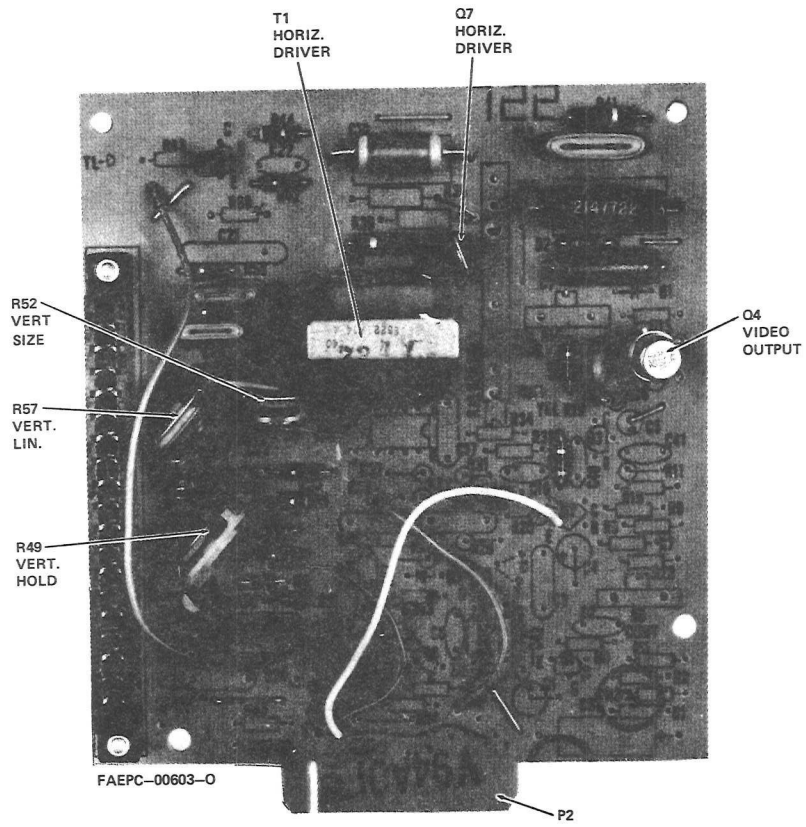
Signal Circuit Card — Solder Side (All Models except M1000–190)



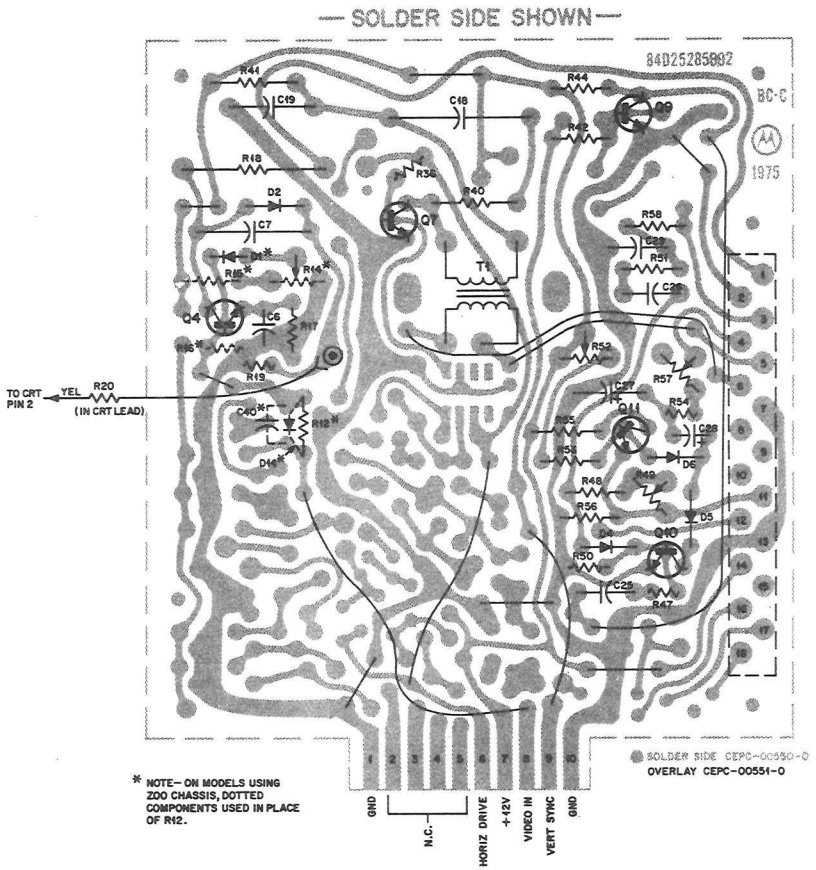
M1000 — 100, 155 and M2000 — 100, 155, 355 — Schematic Diagram



M1000—190 — Schematic Diagram



Signal Circuit Card — Component Side (Model M1000–190)



Signal Circuit Card — Solder Side (Model M1000–190)

REPLACEMENT PARTS LIST

REF. NO.	PART NUMBER	DESCRIPTION
CIRCUIT CARD ASSEMBLIES:		(COMPLETE WITH ALL COMPONENTS)
	84V25013A05	Deflection Circuit Card (Cpt.) (M1000–100, 155)
	84V25551A68	Deflection Circuit Card (Cpt.) (M1000–190)
	84V25014A90	Deflection Circuit Card (Cpt.) (M2000–155, 355)
	84V25013A70	Signal Circuit Card (Cpt.) (All models except M1000–190)
	84V25551A67	Signal Circuit Card (Cpt.) (M1000–190)
CAPACITORS:		(All values are in microfarads unless otherwise noted.)
C1	23S187A26	22, 40V; lytic
C2	21S180C64	33 pF 10%, N750, 100V; Cer. Disc.
C3	8S10191B98	.01 10%, 250V; Polyester
C4, 5	23S187A26	22, 40V; lytic
C6	21S180B53	470 pF 10%, X5F; Cer.Disc
C7	8S10212A91	0.22 10%, 250V; Mtlz Poly
C8	21S180C52	18 pF 5%, NPO; Cer. Disc
C9	23S10255A06	100, 16V; lytic
C10	21S131625	330 pF 10%, X5F; Cer.Disc
C11	21S180B87	220 pF 10%, X5F; Cer.Disc
C12	21S180B53	470 pF 10%, X5F; Cer. Disc
C13	21S180C41	.0027 10%, Z5F; Cer.Disc
C15	8S10191B91	.047 10%, 250V; Polyester
C16	23S10229A32	1.0, 16V; Tant. lytic
C17	8S10299B24	.0022 10%, 400V; Poly Carb
C18	8S10191B88	.027 10%, 400V; Polyester
C19	8S10191C02	0.1 10%, 250V; Polyester
C20	8S10072A44	.047 10%, 200V; Polyester
C21	8S10191C02	0.1 10%, 250V; Polyester
C22	21S180D93	6.8 pF ±0.5 NPO; Cer.Disc
C23	8S10191B97	.0068 10%, 400V; Polyester
C24	21S180C41	.0027 10%, Z5F; Cer. Disc
C25	8S10191B98	.01 10%, 250V; Polyester
C25	8S10191B91	.047 10%, 250V; Polyester (M1000–190 only)
C26	8S10191B89	.022 10%, 250V; Polyester
C27, 28	23S10218A31	5.0, 15V; Tant. lytic
C29	8S10191B98	.01 10%, 250V; Polyester
C30	8S10191A16	.01 10%, 400V; Polyester
C31	23S10255A29	470, 16V; lytic
C32	8S10191B07	.047 10%, 400V; Polyester
C33	23S10255A74	22, 160V; lytic
C34	8S10191B07	.047 10%, 400V; Polyester
C35	8S10212B20	0.47 10%, 400V; Mtlz. Poly.
C36	21S180C41	.0027 10%, Z5F, 500V; Cer.Disc
C37	8S10191A53	0.22 10%, 160V; Polyester
C38	23S10255B83	1800, 16V; lytic
C40	21S180C07	15 pF 10%, N150; Cer.Disc
C40	21S180C82	33 pF 10%, N150; Cer.Disc (M1000–190 only)
C41	21S180B89	180 pF 10%, Z5F 100V; Cer. Disc
C42	21S180C82	33 pF 10%, N150; Cer. Disc
C44	8S10169B71	.033 10%, 400V; Mylar (M2000 only)
C45	8S10212D52	0.1, 100V; Cer. Disc
C46	23S10229A32	1.0, 16V; lytic
C47	21S139640	0.1, +80–20, Z5U, 50V; Cer. Disc
DIODES:		
D1	48R02054A00	Diode, Low Power; 2054
D2	48S191A05	Rectifier, Silicon; 91A05
D3-D6	48R02054A00	Diode, Low Power; 2054
D7-D9	48S191A05	Rectifier, Silicon; 91A05
D10	48S134921	Diode, D1D
D11	48R134978	Rectifier, Silicon; D1K
D12	48S137608	Diode, D9H (M1000 only)
D12	48S137622	Diode, D9N (M2000 only)
D13	48R02054A00	Diode, Low Power; 2054
D14	48S137495	Diode, 1N139 (M1000–190 only)
INTEGRATED CIRCUITS:		
IC1	51S10778A01	MC1391P; T3L
COILS/CHOKES:		
L1	24D25603A03	Coil, Horiz. Width (M1000 only)
L1	24D25603A04	Coil, Horiz. Width (M2000 only)
L2	25D25221A09	Choke, Vert. Out
L3 A/B	24D25290A02	Yoke, Deflection (M1000 only)
L3 A/B	24D68531A03	Yoke, Deflection (M2000 only)
TRANSISTORS:		
Q1	48S134997	1st Video Ampl.; A3K
Q2	48S137127	2nd Video Ampl.; P2S
Q3	48S137172	3rd Video Ampl.; A6J
Q4	48S137093	Video Output; A5F
Q4	48S134919	Video Output; A1M (M1000–190 only)
Q5	48S137171	Sync Sep.; A6H
Q6	48S137127	Sync. Ampl.; P2S
Q7	48S137169	Horiz. Driver; A6G
Q8	48S137462	Horiz. Output; A9Z
Q9	48S137172	Blanking Ampl.; A6J
Q9	48S137172	Vert. Sync; A6J (M1000–190 only)
Q10	48S137172	Vert. Osc.; A6J
Q11	48S134997	Vert. Driver; A3K
Q12	48S137598	Vert. Output; B2Y
RESISTORS/CONTROLS:		
Note:		Only power or special resistors are listed. Use the description when ordering standard values of fixed carbon resistors up to 2 watts.
R6	18D25245A02	Control, Contrast 1k
R14	18D25245A02	Control, Video Bias 1k
R18	17S10731A03	1.5k 5%, 5W; Wire Wound
R35	18C25267B01	Control, Horiz. Hold 22k
R49	18D25245A15	Control, Vert. Hold 100k
R52	18D25245A20	Control, Vert. Size 50k
R57	18D25245A10	Control, Vert. Lin. 1.5k
R61	18D25245A12	Control, Focus 2 Meg.
R63	18D25245A07	Control, Brightness 500k
TRANSFORMERS:		
T1	25D25221A04	Transformer, Horiz. Driver

REPLACEMENT PARTS LIST (Continued)

REF. NO.	PART NUMBER	DESCRIPTION
T2	24D25291E02	Transformer, High Voltage (M1000 only)
T2	24D25291D03	Transformer, High Voltage (M2000 only)
T3	24C25602B01	Transformer, S-Shaping (M2000 only)
MISC. ELECTRICAL PARTS:		
V1	96S10769A01	5"- CRT, Type No.140ANB4 (M1000 only)
V1	96R2500A14	9"-CRT,Type M24-304W/10TS5497A (M2000—155 only)
V1	96R02500A23	9"- CRT (M2000—355 only)
V1	96R02500A22	9"- CRT (M2000—201, M2000—255 only)
MECHANICAL PARTS:		
	14B25751A01	Collar, "C" (CRT Neck)
	42D25298A03	Connector, Anode (M1000 only)
	42D25298A08	Connector, Anode (M2000 only)
S1	9S10768A01	Connector, Receptacle; Header
P3	28S10586A14	Conn., Circuit Card; 3-contacts
	26C25198A03	Heat Sink (for Q8)
	26S10251A08	Heat Sink (for Q12)
S3	15S10183A87	Housing, Recept.; 3-contacts (less contacts)
	39S10184A72	Contact, Recept. (3 req'd.for S3)
	14A25340A01	Insulator, Hi-Voltage Standoff (M2000 only)
	59C25465A02	Magnet, Focus (M2000 only)
	2S10054A36	Nut, Clip-on No.8-18 (M1000 only)
	42C25258A01	Retainer, CRT (M1000 only)
	3S138210	Screw, No. 8-18 x 1-¼" (M1000 only)
	26C25323A01	Shield, Linearity (CRT)
	9D25241A04	Socket, CRT (Incl. leads & resistors R20, R65, R66 & R67)
	41B25268A03	Spring, CRT Aquadag (M1000 only)
	41D65987A01	Spring, Special; CRT Aquadag gnd. (M2000 only)
	42D67027A14	Strap, CRT Mtg.(M2000 only)
	7S10747A02	Support Guide, Circuit Card

APPENDIX B

MDS3000 12" CRT SERVICE MANUAL

MOTOROLA

SERVICE MANUAL

MDS3000, 3003 SERIES (12-INCH)

MDS4000, 4003 SERIES (15-INCH)

CRT DISPLAY MONITORS

StepScan™ MOTOROLA

GENERAL INFORMATION

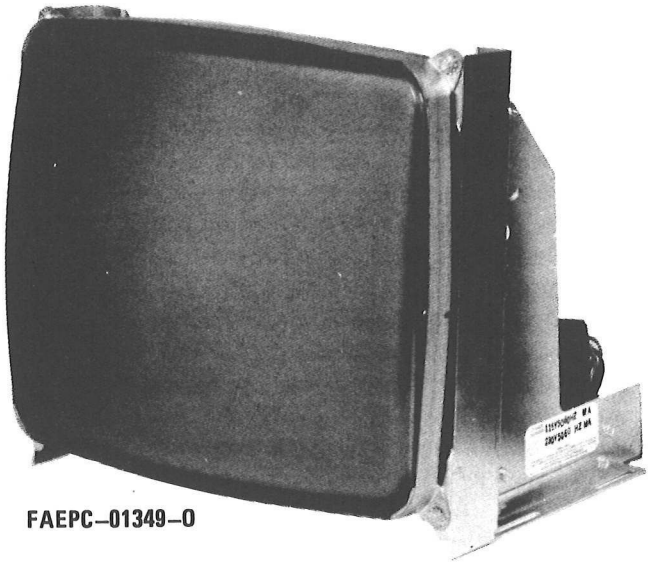
The monitors described herein are fully transistorized (except CRT) and applicable for displaying alphanumeric characters. The MDS3000, MDS3003 series monitors use a 12-inch CRT and the MDS4000, MDS4003 series monitors use a 15-inch CRT. Each monitor accepts a TTL non-composite video, with separate TTL horizontal and vertical sync pulses. Additional inputs include optional TTL StepScan, and/or optional +24VDC to operate the monitor.

A universal power transformer permits operating the monitor from 120, 220 or 240 volts AC, 50/60 Hz. A built-in regulated power supply provides operating voltages of +24V, +13V and +5V.

Input and output connections for the monitor are made through a standard 10-pin edge connector, (or optional 20-pin connector) on the circuit card. Inputs consist of non-composite video, horizontal sync, vertical sync, and signal ground. The optional TTL level StepScan and +24VDC are also connected to the monitor via the 10-pin edge connector. Three pins on the edge connector are also provided for alternate interconnecting of the remote brightness control.

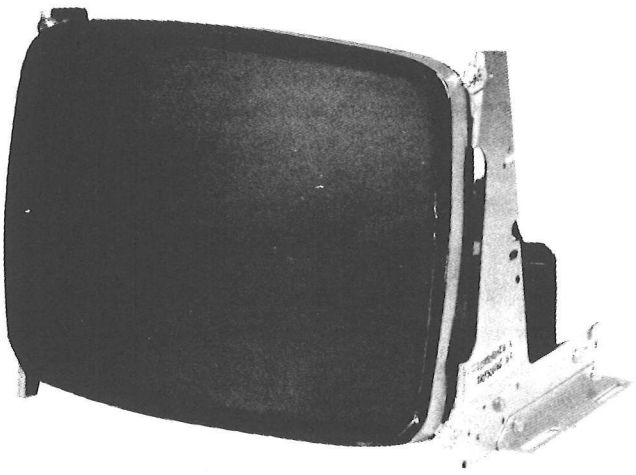
Circuitry consists of two stages for non-composite video amplification, one integrated circuit for vertical sync and deflection processing, five stages for horizontal sync and deflection processing, and a three stage regulated power supply. All models also contain dynamic focusing and spot kill circuitry.

One etched circuit card is utilized, which contains all necessary circuitry. Components are mounted on the top of the circuit card and plated copper foil on the bottom. Schematic reference numbers are printed on the top and bottom of each circuit card to aid in the location and identification of components for servicing. All standard operating/adjustment controls are mounted in a convenient manner on the circuit card.



FAEPC–01349–O

Model MDS4000, MDS4003 Series (15" CRT)



Model MDS3000, MDS3003 Series (12" CRT)

MOTOROLA INC.
Display Systems

1299 E. Algonquin Road, Schaumburg, IL. 60196 (312) 397-8000

MANUAL VP38
1/81

PART NO. 68P25253A82

SAFETY WARNING

CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

1. SAFETY PROCEDURES should be developed by habit so that when the technician is rushed with repair work, he automatically takes precautions.

2. A GOOD PRACTICE, when working on any unit, is to first ground the chassis and to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.

3. Extreme care should be used in HANDLING THE PICTURE TUBE as rough handling may cause it to implode due to atmospheric pressure (14.7 lbs. per sq. in.). Do not nick or scratch glass or subject it to any undue pressure in removal or installation. When handling, safety goggles and heavy gloves should be worn for protection. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode or use a well insulated piece of wire. When servicing or repairing the monitor, if the cathode ray tube is replaced by a type of tube other than that specified under the Motorola Part Number as original equipment in this Service Manual, then avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger of personal injury from unnecessary exposure to X-ray radiation may result.

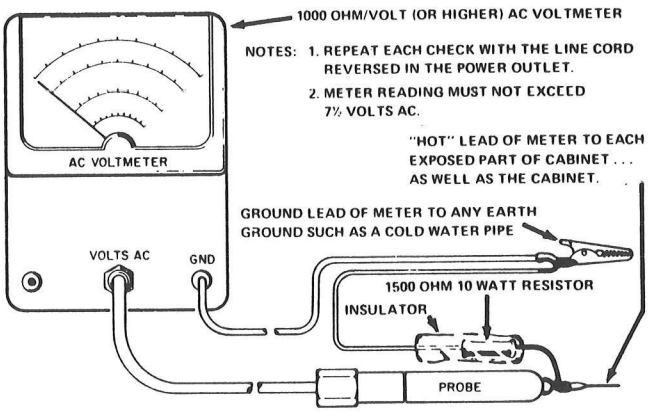
4. An ISOLATION TRANSFORMER should always be used during the servicing of a unit whose chassis is connected to one side of the power line. Use a transformer of adequate power rating as this protects the serviceman from accidents resulting in personal injury from electrical shocks. It will also protect the chassis and its components from being damaged by accidental shorts of the circuitry that may be inadvertently introduced during the service operation.

5. Always REPLACE PROTECTIVE DEVICES, such as fishpaper, isolation resistors and capacitors and shields after working on the unit.

6. If the HIGH VOLTAGE is adjustable, it should always be ADJUSTED to the level recommended by the manufacturer. If the voltage is increased above the normal setting, exposure to unnecessary X-ray radiation could result. High voltage can accurately be measured with a high voltage meter connected from the anode lead to chassis.

7. BEFORE RETURNING A SERVICED UNIT, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER WHEN MAKING THIS TEST.

In addition to practicing the basic and fundamental electrical safety rules, the following test, which is related to the minimum safety requirements of the Underwriters Laboratories should be performed by the service technician before any unit which has been serviced is returned.



Voltmeter Hook-up for Safety Check

A 1000 ohm per volt AC voltmeter is prepared by shunting it with a 1500 ohm, 10 watt resistor. The safety test is made by contacting one meter probe to any portion of the unit exposed to the operator such as the cabinet trim, hardware, controls, knobs, etc., while the other probe is held in contact with a good "earth" ground such as a cold water pipe.

The AC voltage indicated by the meter may not exceed 7½ volts. A reading exceeding 7½ volts indicates that a potentially dangerous leakage path exists between the exposed portion of the unit and "earth" ground. Such a unit represents a potentially serious shock hazard to the operator.

The above test should be repeated with the power plug reversed, when applicable.

NEVER RETURN A MONITOR which does not pass the safety test until the fault has been located and corrected.

Table of Contents

* NOTE: A service schematic diagram and electrical/mechanical parts list for the basic MDS-Series CRT monitors is not included in this manual; instead, it accompanies this manual as a separate sheet, Motorola Part No. 68P25253A84.

For users of unique variations of the MDS-Series CRT monitors, however, order the schematic diagram by its complete model number.

SPECIFICATIONS

DISPLAY

- **MDS3000** – 12" diagonal measure
- **MDS4000** – 15" measured diagonally, 14" diagonal viewable area
- 110^{p} deflection angle
- 3 x 4 aspect ratio
- P4 phosphor standard (other EIA phosphors available)
- T band U.L. implosion protection
- Direct etch and PPG optional
- **Standard Display Size:** (MDS3000) 8.5 x 6.0, (MDS4000) 10.0 x 7.5
- Capable of displaying over 3400 characters.

VIDEO PERFORMANCE

- **Resolution:** 1200 lines center, 950 lines corners (P4 phosphor)
- **Bandwidth:** within 3 dB, 10 Hz to 30 MHz is typical.

PERFORMANCE FEATURES

- **StepScan™:** Stepped vertical scanning option provides an increased capacity display at any horizontal frequency, thus conserving bandwidth and in many cases, eliminating the need for a higher frequency clock for increased performance.
- **Dynamic Focus:** Excellent corner focus is achieved by supplying dynamic voltage to the focus element of the cathode ray tube.

SYNCHRONIZATION

- **Horizontal:** 15.7 kHz $\pm$ 500 Standard; 18.7 kHz $\pm$ 500 optional
- **Vertical:** 47 to 63 Hz
- **Horizontal Blanking:** 11 uSec minimum (for scanning frequency of 15.7 kHz). 10 uSec minimum (at 18.7 kHz). Time includes retrace and delay.
- **Vertical Blanking:** 800 uSec (includes retrace and video delay)

INPUT SIGNALS

- **Horizontal:** 4 to 32 uSec, input TTL compatible, positive-going (negative optional), 4.0V PP $\pm$ 1.5
- **Vertical:** 50 to 1400 uSec, input TTL compatible, positive (negative optional), 4.0V PP $\pm$ 1.5
- **Video:** positive white, input termination 470 ohms $\pm$ 5%, 2.5 - 5.0V PP

  Composite video input with DHHS protection circuit optionally available.

POWER INPUT

- 120/240V AC (105–135), 50/60 Hz, 65VA max.
- 24V DC optional

INTERCONNECT TO CUSTOMER SYSTEM

- 10 pin edge connector standard
- 20 pin ribbon cable optional

CONTROLS

- **Internal:** Horizontal size, horizontal video centering, brightness, focus, vertical hold, vertical size, vertical linearity. (All controls adjustable from top or back of unit).
- **External:** Brightness (as an operator control.
- Optional contrast control available.

GEOMETRY (Pin & Barrel)

- Sides equal less than 1% of height.
- Top and bottom equal less than 1% of width.

LINEARITY

- Character height or width will not vary $\pm$7% from the average character size.
- Adjacent characters will not vary more than 5%.

ENVIRONMENT

- **Operating Temperature:** 0^{o} to $+55^{o}C$
- **Storage Temperature:** $-40^{o}C$ to $+65^{o}C$

  Note: CRT's with bonded etched panels should not be subjected to storage or operating temperatures above $50^{o}C$
- **Operating Altitude:** 10,000 ft. max.

  Designed to comply with DHHS Radiation Performance Standards and U.L. specifications.

*In a continual effort to upgrade our standard products as new technological advances are made, specifications are subject to change without notice.

– NOTE –

This manual is up-to-date and correct as of the printing date.

– CAUTION –

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

SERVICE NOTES

BLOCK/SCHEMATIC DIAGRAMS

Refer to Figure 1 for a functional view of an MDS-Series Display Monitor in block form. It will help in becoming familiar with the overall schematic diagram, which accompanies this manual as a separate service sheet (Motorola Part No. 68P25253A84).

ELECTRICAL/MECHANICAL PARTS LISTS

A complete listing of field replaceable parts in alphanumeric sequence is included on the back of the accompanying schematic diagram.

CIRCUIT TRACING

Component reference numbers are printed on the top and bottom of the circuit card to facilitate circuit tracing. In addition, top (component) and bottom (solder) view drawings are included for convenient viewing of the circuit card. Transistor elements are identified as follows:

E – emitter, B – base, and C – collector

COMPONENT REMOVAL

On the circuit card, component removal requires the use of a "desoldering" iron, carefully applied to prevent lifting of the foil from the circuit card. An iron with a temperature controlled heating element is recommended to reduce the possibility of card damage. Use latest recommended desoldering procedures. The nozzle of the solder extracting gun should be inserted directly over the component lead which is heated only long enough to melt the solder and draw it away. This should leave the component lead free of the circuit card.

POWER TRANSISTOR REPLACEMENT

When replacing transistors Q101 (+24V Reg.) or Q402 (Horiz. Output), use the following information and observe all precautions:

1. There are no plug-in sockets; instead, two (2) screws are soldered from the bottom of the circuit card to protrude up through the circuit card and its bracket. The transistors are secured with two (2) nuts each on the top of the circuit card bracket, which also serves as a heat sink.

2. When replacing a transistor, silicone grease (Motorola Part No. 11M490487) should be applied evenly to the top of the heat sink (circuit card bracket) and bottom of the transistor. In addition, be sure a mica insulator is positioned properly between the transistor and heat sink.

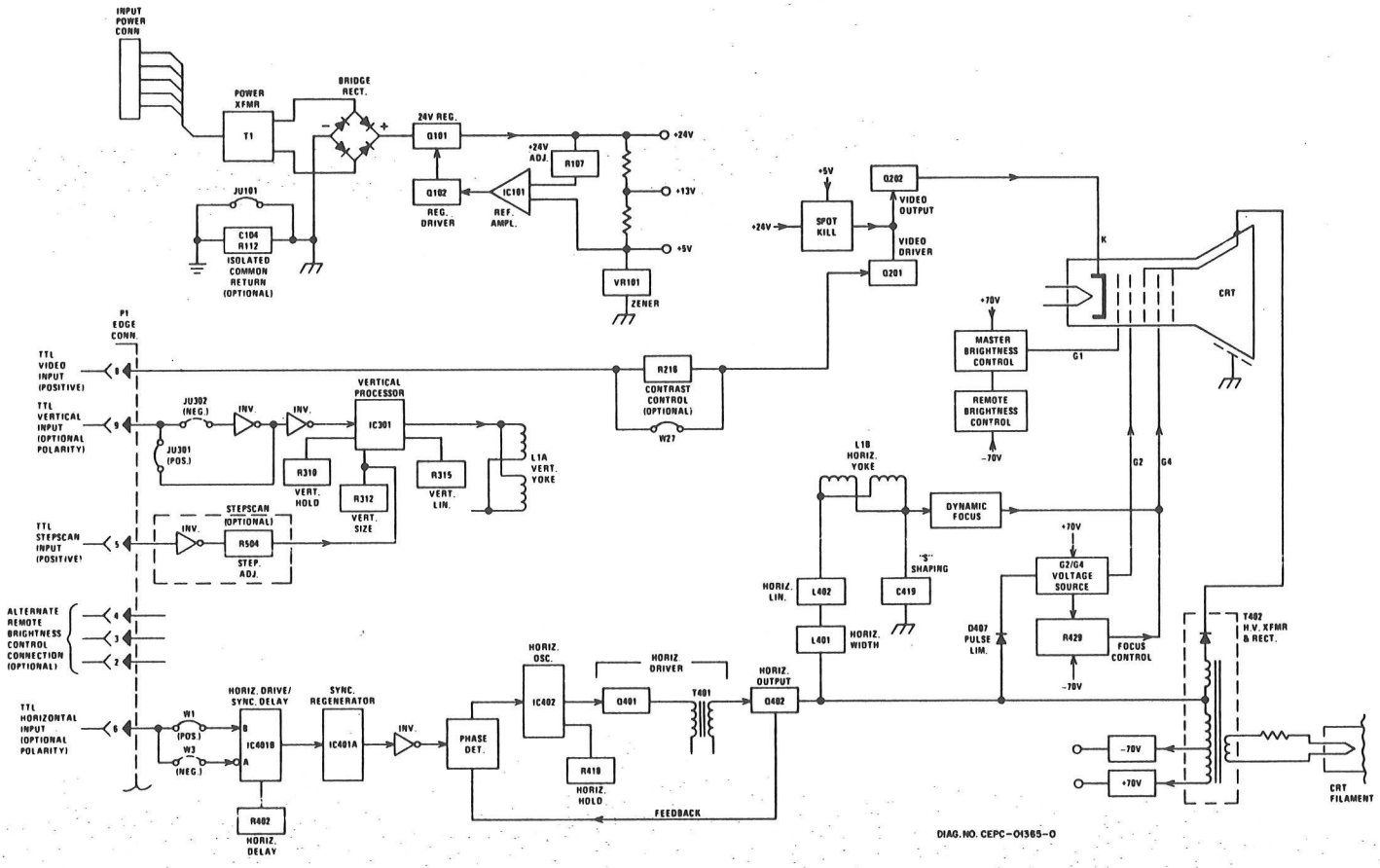


Figure 1. MDS-Series Display Monitor – Functional Block Diagram

3. The transistor mounting nuts must be tight before applying power to the monitor. This insures proper cooling and electrical connections. NON-COMPLIANCE WITH THESE INSTRUCTIONS CAN RESULT IN FAILURE OF THE TRANSISTOR AND/OR ITS RELATED COMPONENTS.

– NOTE –

Use caution when tightening transistor mounting nuts. If the screw or nut threads are stripped by excessive pressure, a poor electrical and mechanical connection will result.

INSTALLATION–MOUNTING SLOT HOLE DIMENSIONS

Figure 2 is a bottom view drawing that clearly illustrates mounting slot hole dimensions. Use it to identify mounting clearances in the final installation.

CRT REPLACEMENT

General

Use extreme care in handling the CRT as rough handling may cause it to implode due to high vacuum pressure.

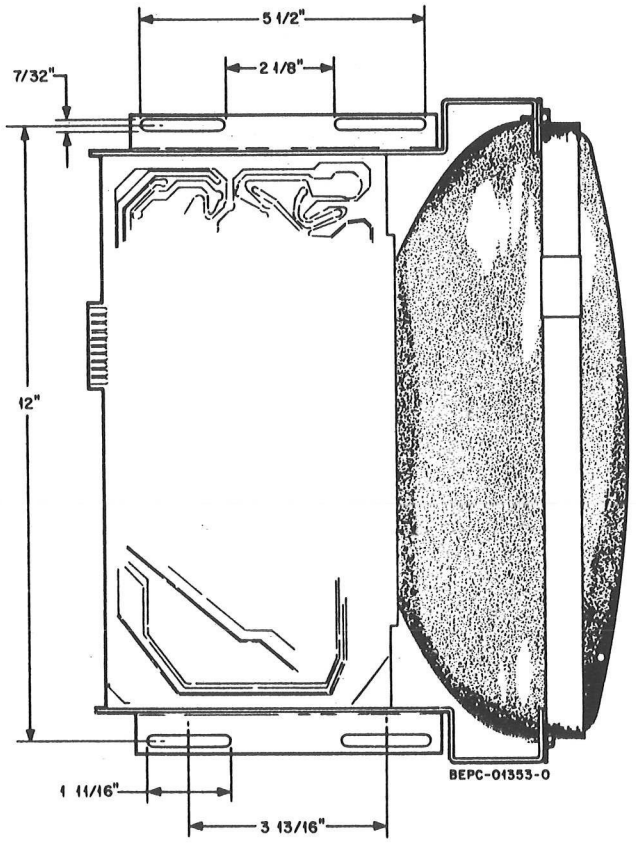


Figure 2. Mounting Slot Hole Dimensions

Do not nick or scratch glass or subject it to any undue pressure in removal or installation. Use goggles and heavy gloves for protection. Also, be sure to disconnect the monitor from all external voltage sources. Refer to Figure 5 for location of the CRT identification label. Information on the label is essential for ordering the correct replacement CRT!

Procedure

Step 1. Connect a grounding strap (first) to the metal chassis for a good earth ground; then discharge CRT by shorting the H.V. 2nd anode to ground.

Step 2. Remove the CRT socket, deflection yoke (loosen clamp screw) and 2nd anode lead.

Step 3. Remove CRT from the front of the chassis by loosening and removing four screws, one at each corner of CRT.

Step 4. Reverse the above steps to re-install the new CRT.

Step 5. After installation perform operational check/adjustment procedures.

SERVICE PHOTOGRAPHS

Figure 3:

Figure 3 shows the rear view of a typical MDS-Series display monitor. Callouts identify the circuit card edge connector (P1) for signal inputs, a six (6) pin power input connector, and a remote brightness control (R213) soldered to the circuit card. Variations to the aforementioned will include a different type of power connector, and the remote brightness control can be interconnected via the circuit card edge connector.

Figure 4:

For convenient access to the component (top) side of the circuit card, reference Figure 4. Callouts accompanying the illustration are self-explanatory.

Figure 5:

For convenient unobstructed troubleshooting of the circuit card, stand the monitor on its side as shown in Figure 5. Notice also in this illustration the location of the CRT identification label. The information on this label is essential for ordering the correct replacement CRT.

Figure 6:

Reference Figure 6 for quick identification and location of adjustable controls, transistors, integrated circuits, etc.

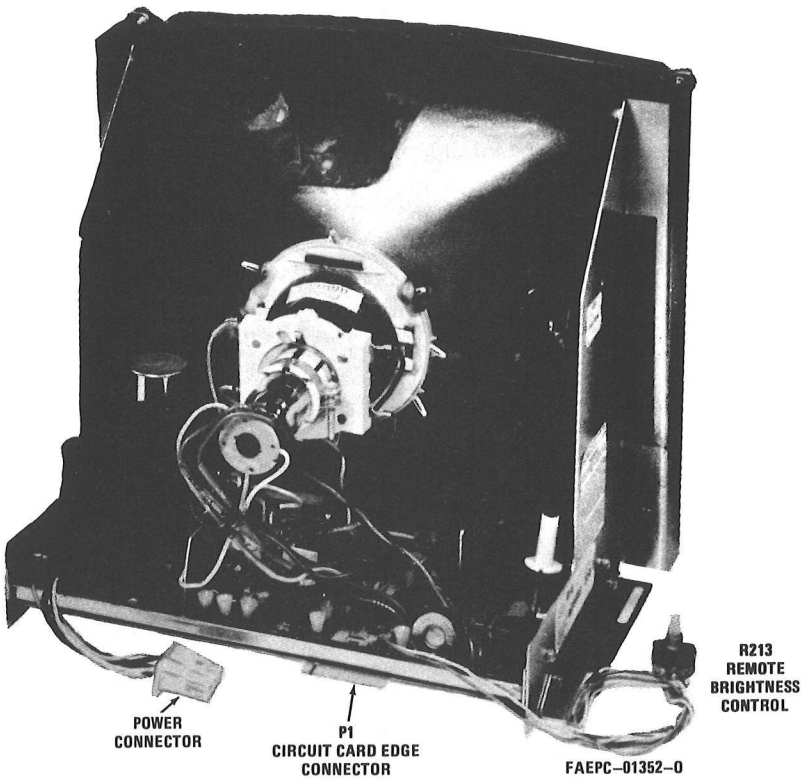


Figure 3. Typical MDS-Series Display Monitor – Rear View

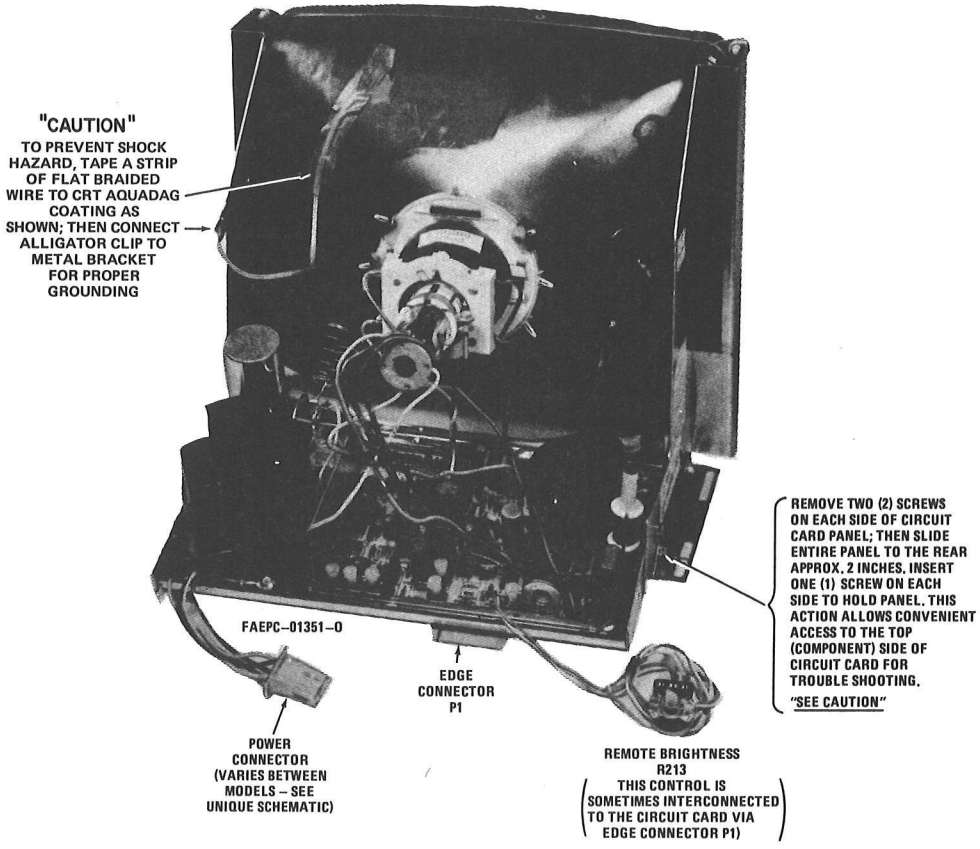


Figure 4. Circuit Card Troubleshooting from Component Side

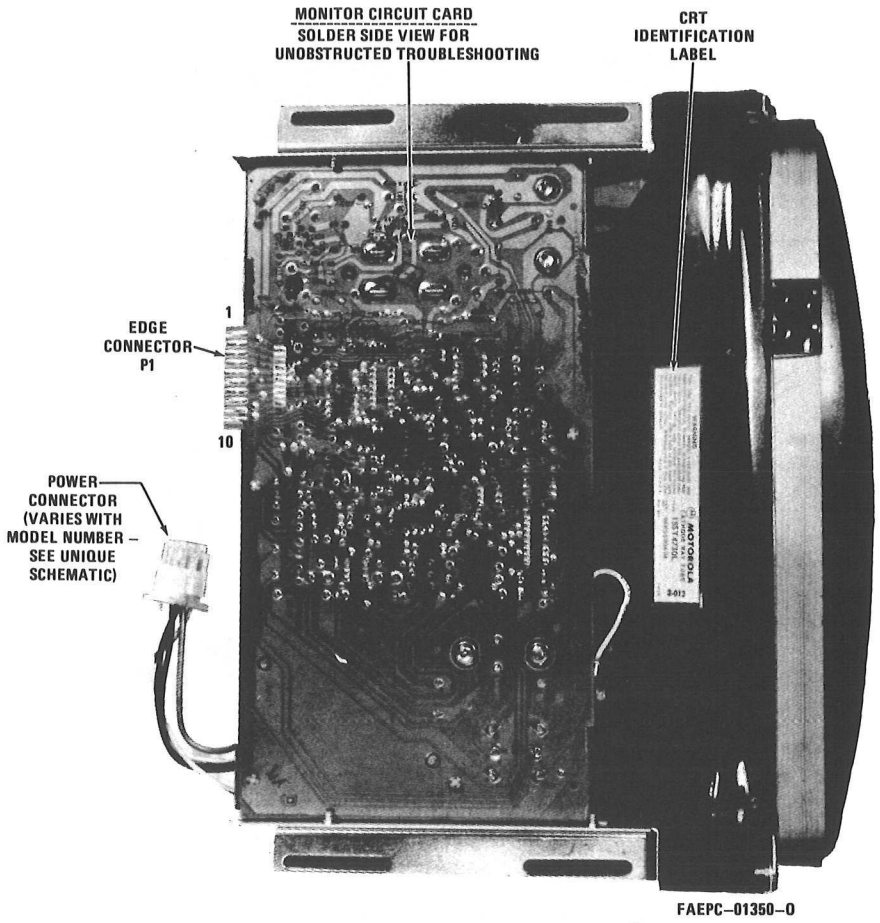


Figure 5. Circuit Card Troubleshooting from Component Side

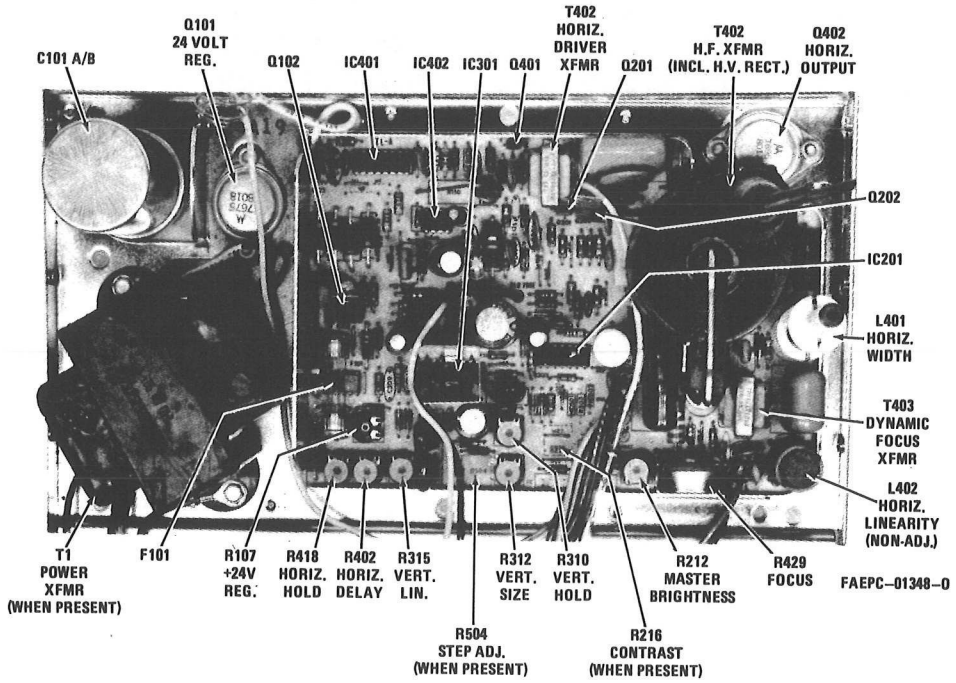


Figure 6. Identification and Location of Circuit Card Components – Adjustable Controls, Transistors, Integrated Circuits, Etc.

OPERATIONAL CHECK/ADJUSTMENT PROCEDURES

GENERAL

The following procedures are provided to check the operation of the monitor and perform simple preinstallation adjustments (if required), or readjust after servicing and component replacement.

When reference is made to adjust to a specific size display (vertically and horizontally), refer to original model specifications for correct dimensions by the monitor model number. This also applies to minimum and maximum tolerances when adjusting for correct CRT geometry, linearity, focus, etc.

– NOTE –

To assist in understanding more of the preceding terminology, refer to a separate Motorola Manual, "Incoming Inspection Guide" (Motorola part number 68P25253A71).

Perform the procedures in the sequence presented, and allow at least five (5) minutes warm-up before adjusting the monitor. In addition, when instructed to disconnect an input signal, do not ground the signal at the circuit card edge connector (P1). This action could damage the signal source generator. Instead, disconnect the signal at its source.

CCW = Counter Clockwise Rotation, CW = Clockwise Rotation. (As viewed from rear of circuit card.)

EQUIPMENT REQUIRED

Variac (0-150 Volts AC)

Precision Digital Voltmeter

Non-Metallic Alignment Tool

Test Signals (Bench test signals must be same amplitude, polarity, and frequency as final installed operating signal source. Refer to original specifications for values by monitor model number.)

The following Motorola gauges are required for performing complete and accurate CRT geometry and linearity alignment. Refer to original model specifications for correct gauges to use.

Linearity Gauge

Slot Gauge

Parallelogram Gauge

ISOLATED GROUND/COMMON RETURN CHECK

– CAUTION –

Do not connect power or signals to monitor.

Procedure No. 1. For monitors with circuit card common return foil isolated from metallic chassis/earth ground. Isolating components are R112 (22K resistor) and C104 (0.1 μF capacitor); jumper JU101 is out.

Step 1. Connect ohmmeter leads between edge connector P1, pin 1, and chassis (earth) ground. Resistance reading should be 22K ohms, $\pm$ 5%.

Step 2. Connect ohmmeter leads between edge connector P1, pin 10, and chassis (earth ground. Resistance reading should be 22k ohms, $\pm$ 5%.

– NOTE –

Step 3 is only for monitors that have their Remote Brightness control (R213) interconnected to the circuit card via edge connector P1, pins 2, 3 and 4.

Step 3. Connect ohmmeter leads between edge connector P1, pin 2, and chassis (earth) ground. Resistance reading should be 22K ohms, $\pm$ 5%.

Procedure No. 2. For monitors with non-isolated circuit card common return foil; whereby, the foil is connected direct to the metallic chassis/earth ground via a (white) wire. (Jumper JU101 is in, while components R112 and C104 are out.)

Step 1. Measure between edge connector pins and chassis (earth) ground as described in Procedure No. 1. Resistance readings should be 0.2 ohms or less.

+24V VOLTAGE REGULATOR CONTROL ADJUSTMENT

Procedure

Step 1. Connect monitor to AC line supply. Adjust supply to 120 volts.

Step 2. Apply signal connector to circuit card edge connector, P1.

Step 3. Adjust Vertical (R310) and Horizontal (R418) Hold controls until display is synced.

Step 4. Connect a DC digital voltmeter or other precision accuracy voltmeter to the collector (case) of the regulator output transistor, Q101.

Step 5. Adjust the +24V Voltage Regulator control, R107, for output of +24 volts $\pm$ 0.5 volts.

Step 6. When adjustment is complete, vary the AC line supply voltage between 105 and 135 volts to check for proper regulator operation. If regulator is operating properly there should be no change in display size.

BRIGHTNESS/CONTRAST ADJUSTMENT

Procedure

Step 1A. Disconnect video signal input (only) at pin 8 of edge connector P1 . . .

or

Step 1B. If monitor is equipped with a Contrast control (R216 on monitor circuit card or customer supplied off-circuit card), rotate to the position that cuts off the video input signal.

Step 2. Rotate Master Brightness control (R212) fully CCW (raster off).

Step 3. Rotate Remote Brightness control (R213) fully CCW (raster off).

Step 4. Rotate Master Brightness control (R212) until the raster just begins to appear on the CRT; then back off slightly to the threshold of raster cutoff.

Step 5A. Reconnect video signal . . .

or

Step 5B. Adjust Contrast control (if present) for desired video display level on CRT.

Step 6. Adjust Remote Brightness control (R213) for desired (overall) brightness level.

HORIZONTAL OSCILLATOR ADJUSTMENT

Procedure

Step 1. Disconnect horizontal sync input (only) at pin 6 of edge connector P1.

Step 2. Adjust Horizontal Hold control (R418) until video display approaches best horizontal sync condition. (Without the horizontal sync input connected, however, the display will never quite lock in.)

– NOTE –

It may be necessary to temporarily increase the raster brightness with the Remote Brightness control (R213) to view the raster edges.

Step 3. Reconnect the horizontal sync signal. (At this point the video display should be in sync.)

Step 4. Adjust the Horizontal Delay control (R402) until the video display is centered horizontally within the raster (as viewed from the left side to the right side of the raster).

HORIZONTAL SIZE ADJUSTMENT

Procedure

Adjust Horizontal Width coil (L401) for specified video width (horizontally).

– NOTE –

To increase width, rotate coil slug CCW (away from circuit card); to decrease width, rotate coil slug CW (toward circuit card).

VERTICAL HOLD ADJUSTMENT

Procedure

If video display is rolling, adjust the Vertical Hold control (R310) until the video display remains locked in.

VERTICAL SIZE/LINEARITY ADJUSTMENT

Procedure No. 1 (Monitors without StepScan)

Step 1. Adjust the Vertical Size control (R312) until the specified size display (vertically) is obtained.

Step 2. (Refer to Figure 7.) Adjust the Vertical Linearity control (R315) until the extreme top and bottom characters (designated "A" and "B") are equal in height to the center characters (designated "C").

Step 3. Readjust the Vertical Size control (R312), if necessary, for specified size display (vertically).

Procedure No. 2 (Monitors with StepScan)

Step 1. With specified StepScan input connected to pin 5 of edge connector P1, rotate the Step Adjust control (R504) for minimum vertical size. (This control will be final adjusted later.)

Step 2. Adjust Vertical Size control (R312) for specified vertical size display – before StepScan is actively applied with Step Adjust control, R504.

Step 3. (Refer to Figure 7.) Adjust the Vertical Linearity control (R315) until the extreme top and bottom characters (designated "A" and "B") are equal in height to the center characters (designated "C").

Step 4. Readjust the Vertical Size control (R312), if necessary, for specified size display (vertically) as described in Step 2.

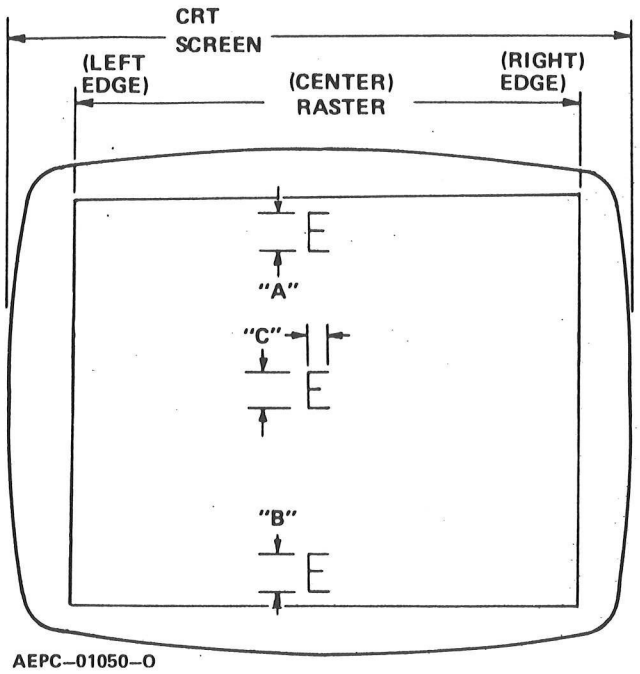


Figure 7. Partial CRT Display of Characters for Vertical Linearity Adjustment

STEPSCAN ADJUSTMENT (Applicable to monitors with StepScan only)

General

StepScan is a unique input signal that is accounted for, and incorporated, when the original video signal format is being developed. As a result, it cannot be connected to just any monitor, even if the monitor has the necessary StepScan circuitry. Check original video signal format specification.

Procedure:

Step 1. Be sure specified positive-going TTL Level StepScan signal is connected to pin 5 of edge connector P1.

Step 2. Rotate the Step Adjust control (R504) through its entire range slowly, and observe that the display size increases vertically.

Step 3A. Adjust the Step Adjust control (R504) for correct vertical size per original model specifications . . .

or

Step 3B. If the StepScan is not required in the final installed application, rotate the Step Adjust control (R504) for minimum vertical size. (See following NOTE.)

– NOTE –

In Step 3B this is applicable only if the StepScan input remains connected to the edge connector from its source. However, if the StepScan source is physically disconnected from pin 5 of the edge connector, pin 5 must be grounded to pin 1 or 10. In either of these conditions, proceed to Step 4.

Step 4. Readjust Vertical Size control (R312) to desired height vertically.

RASTER CENTERING ADJUSTMENT (Applicable only if the CRT and/or deflection yoke have been changed.)

– NOTE –

Depending on the input signal format, the video display on some monitors will be down-centered more than normal within the raster. As a result, an up-centering resistor (R325) is added, which shifts the entire raster (and video display) up. (The shift will vary between 0.1 – 0.4 inches.) This action is necessary to minimize over-adjusting the Centering Magnets to recenter the video display. (Excessive adjustment of the Centering Magnets could cause geometric distortion.)

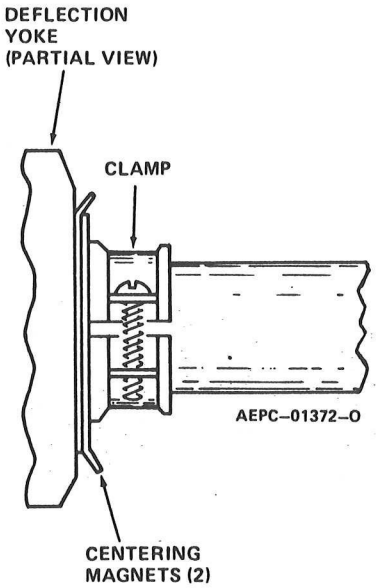


Figure 8. Partial View of CRT Neck/Deflection Yoke – Centering Magnets

General

This procedure should be performed while the monitor is free-standing on a bench, and in the correct sequence (preceding the Raster Geometry Adjustment procedure). Do not readjust after the monitor has been installed in a cabinet or terminal.

Procedure No. 1 (For monitors without up-centering resistor R325.)

Step 1. Turn up the Remote Brightness control (R213) until the four (4) edges of the raster are visible.

Step 2. (Reference Figure 8.) Rotate the two (2) centering magnets (simultaneously) until the raster is centered (horizontally and vertically) within the active phosphor area of the CRT. (Reference Figure 9.)

Step 3. Readjust the Remote Brightness control (R213) for desired (overall) brightness level.

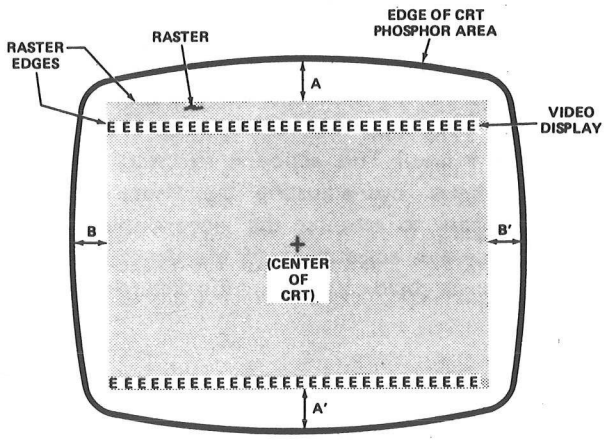


Figure 9. Raster Centering Without Up-Centering Resistor, R325

Procedure No.2 (For monitors with up-centering resistor R325.)

Step 1. Turn up the Remote Brigntness control (R213) until the four (4) edges of the raster are visible.

Step 2. (Reference Figure 8.) Rotate the two (2) centering magnets (simultaneously) until the left and right edges of the raster are centered horizontally, and the top and bottom edges of the video display are centered vertically within the active phosphor area of the CRT. (Reference Figure 10.)

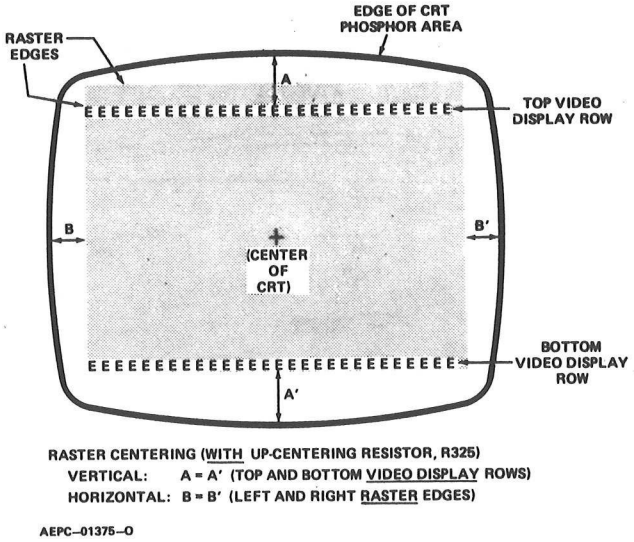


Figure 10. Raster Centering With Up-Centering Resistor, R325

Step 3. Readjust the Remote Brightness control (R213) for desired (overall) brightness level.

– CAUTION –

Remember, do not readjust the centering magnets after performing the CRT Raster Geometry Adjustment procedure that follows, or after final installation. CRT raster geometry will be affected.

RASTER GEOMETRY ADJUSTMENTS

General

This adjustment is normally required only if the yoke and/or CRT have been replaced. Upon completion of the geometry adjustments, there may not be a yoke magnet installed on every yoke mounting pin. Normal installation ranges from one to four yoke magnets per deflection yoke. In addition, keep in mind that there will be some interaction between yoke magnets on the deflection yoke mounting pins. Whereby, as the geometry adjustment proceeds, it may be necessary to remove an earlier positioned magnet from one pin when a new magnet is positioned (or added) on a different pin.

There are two (2) different strength yoke magnets available for correcting CRT geometry. The soft core (or flexible) magnet is the stronger of the two magnets. (Reference Figure 11 to identify their north poles.) Pincushion and trapezoidal correction generally require high strength magnets, and barrel correction requires a lower strength magnet for correction.

– WARNING –

High voltages are present at the deflection yoke and are a potential shock hazard. Exercise caution when performing the following adjustment procedures.

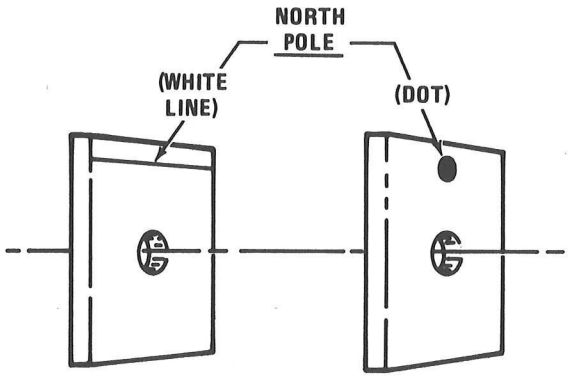


Figure 11. Yoke Magnet North Pole Identification

Pincushion/Barrel Correction (top, bottom and sides) Procedure

Perform this adjustment if the raster exhibits the abnormal effects shown in Figure 13.

Step 1. Push a magnet on the yoke mounting pin as shown in Figure 13. A magnet should be placed only on the pin that corresponds to the affected area.

Step 2. Rotate the magnet to obtain the desired raster, labeled "NORMAL" on Figure 13.

Step 3. If the desired raster cannot be obtained, add a second magnet to the yoke mounting pin. Both magnets must be aligned as shown in Figure 12; then rotated simultaneously.

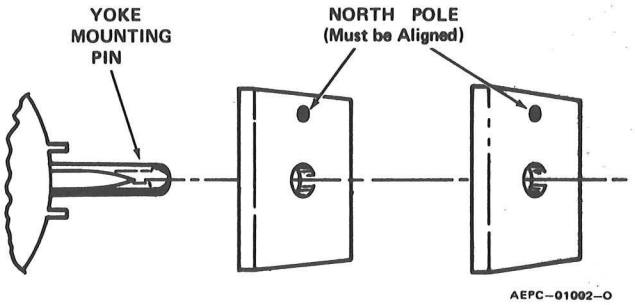


Figure 12. Installing a Second Yoke Magnet

Trapezoidal Correction (corners) Procedure

Perform this adjustment if the raster exhibits the abnormal effects shown in Figure 14.

Step 1. Push a magnet onto the yoke mounting pin as shown in Figure 14. Magnet should be placed only on the pin that corresponds to the affected area.

Step 2. Rotate the magnet to obtain the desired raster, labeled "NORMAL" in Figure 14.

Step 3. If the desired raster cannot be obtained, add a second magnet to the yoke mounting pin. Both magnets must be aligned as shown in Figure 12; then rotated simultaneously.

FOCUS ADJUSTMENT

Procedure

The optimum focus of the display is obtained by adjusting the focus control, R429, for best focus at a point which is near the center and approximately one-third (1/3) down from the top of the display.

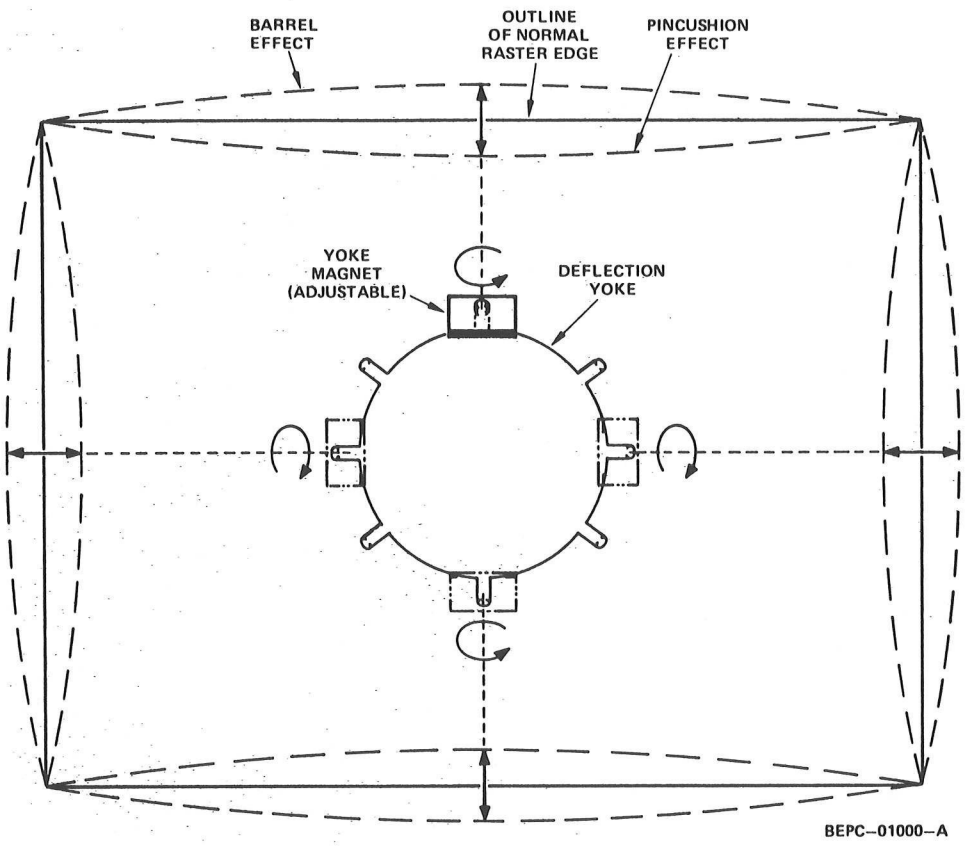


Figure 13. Pincushion/Barrel Effects and Adjustment

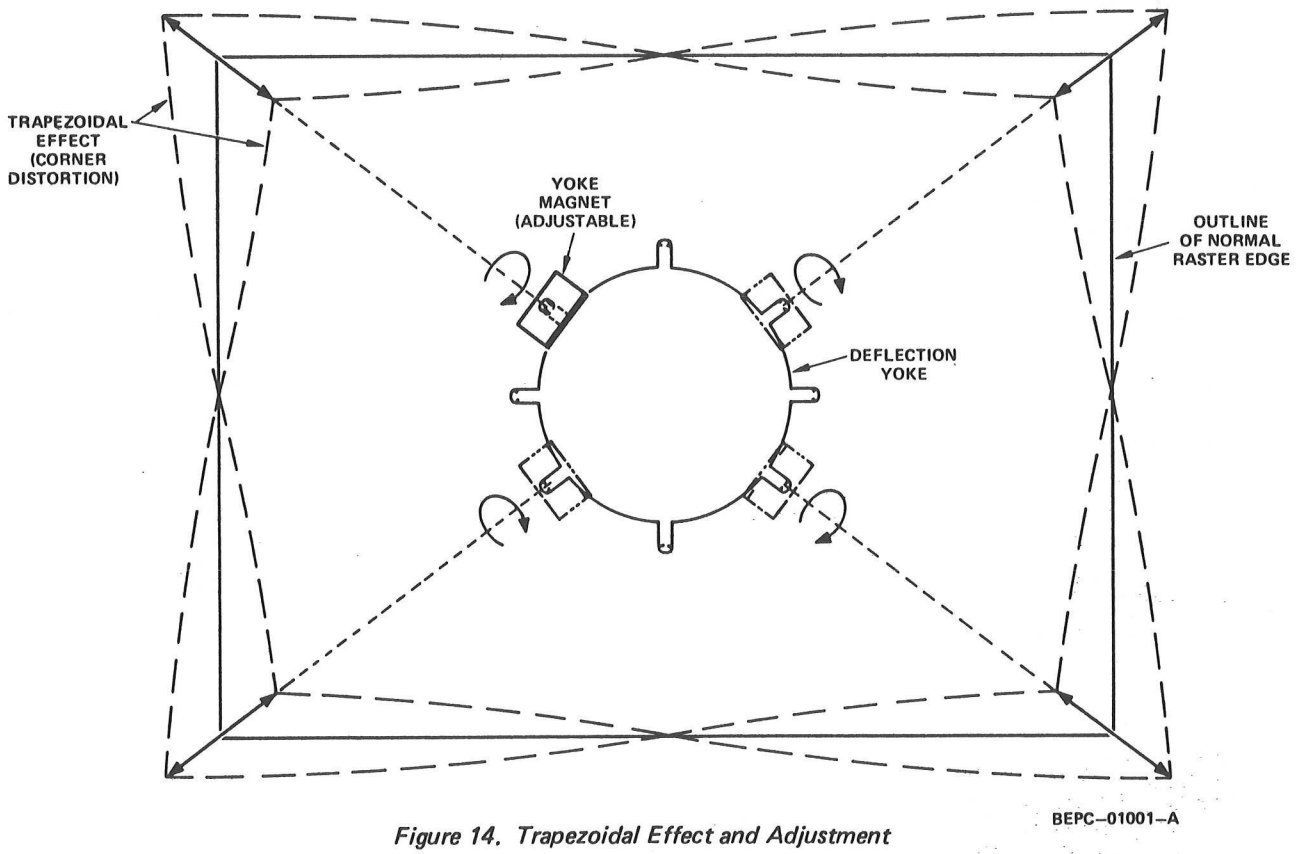


Figure 14. Trapezoidal Effect and Adjustment

THEORY OF OPERATION

POWER SUPPLY (Refer to Figure 15)

The power supply is a transformer operated, full wave, regulated series pass circuit that maintains a constant output voltage with line input variations of ± 12.5%. Depending on how connector S1 is wired, operation from 120, 220 or 240 volts, 50/60 Hz is possible. Integrated circuit IC101 is the reference amplifier, transistor Q102 is the regulated output driver, and Q101 is the series pass transistor.

The output voltage, +24V, appears at the collector of Q101. This voltage is divided between R106, R107 and R109. Resistor R108 limits the range of R107. The voltage appearing on the arm of potentiometer R107 (24V ADJ. control) is the reference input to the inverting input (–) of reference amplifier IC101.

A temperature compensated zener diode, VR101, establishes a fixed reference voltage at the non-inverting input (+) to IC101. Resistors R110 and R111 and diode D105 provide bias current for VR101. The junction of R110 and R111 is the +13V source for the horizontal oscillator, IC402. Regulator VR101 is also the 5 volt source for the monitor circuitry. Operating voltage for IC101 is derived from resistor network R101 and R105.

An increase in output current will cause a decrease in output voltage due to internal supply impedance. This will cause the voltage at the base of Q102 to become more positive via the inverting amplifier IC101. With the base more positive, Q102 will conduct more, increasing its collector current. This increases the base current in Q101. The result is increased output current from Q101, raising the output voltage and maintaining the proper output voltage level.

Electrolytic capacitor C101, section "A", filters the bridge rectifier (D101–D104) output, while section "B" provides additional filtering of the +24V regulator output. Capacitor C103 filters the +5 volt source. R102 is the load resistor for Q102. Resistors R103, R104 bias Q102. Capacitor C102 increases regulation at high frequencies for improved transient response.

VIDEO AMPLIFIER (Refer to Figure 16)

The linear video amplifier consists of two stages, Q201 and Q202, which are connected in a cascode configuration. This common emitter-common base arrangement greatly reduces the effect of Miller capacity (when compared to a conventional single transistor video amplifier/output stage).

A TTL compatible non-composite video signal, approximately 4.0 volts P-P, is DC coupled to the base of Q201 via R202. Resistor R201 provides proper termination for the high frequency input video signal. R203 and C201 provide high frequency compensation to maintain a flat response when Q201 and Q202 conduct. Contrast control R216 (when present) is used to limit the input video signal, which indirectly varies the amplitude of the video drive to the CRT cathode. This action is necessary to provide a contrast function when more than one level of video is applied to the input. Capacitor C208 (when present) provides high frequency compensation for the input video signal.

During a no-signal condition, video driver transistor Q201 is off. At the same time, video output transistor Q202 is base

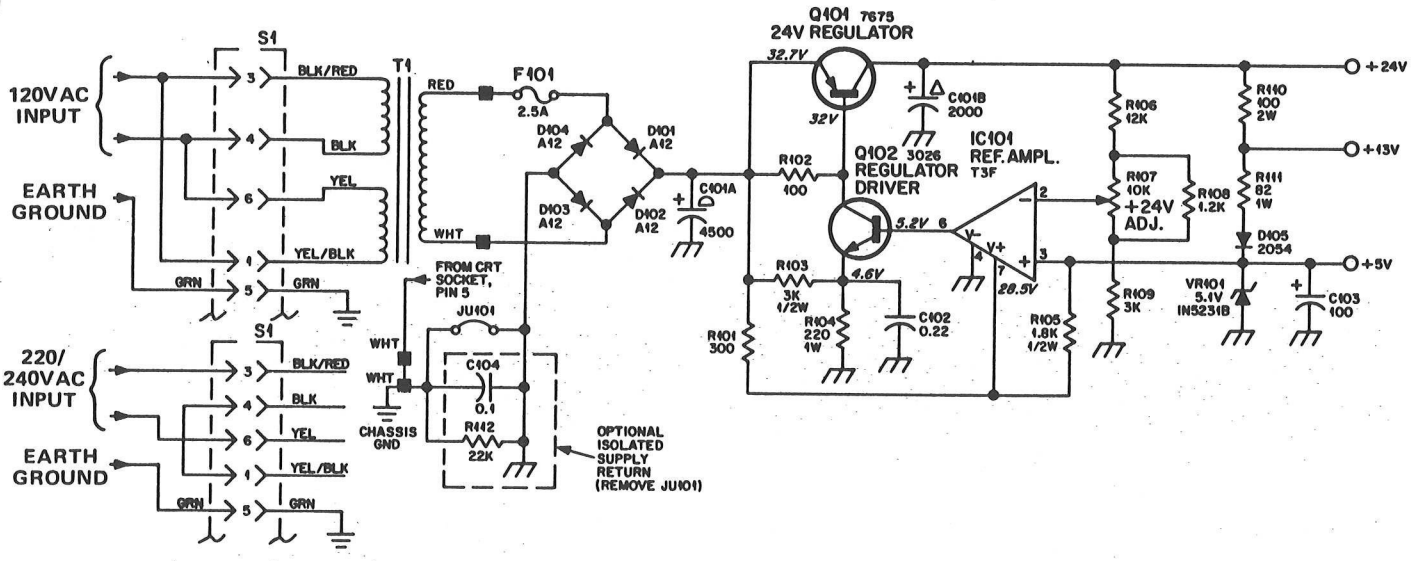


Figure 15. AC Power Input/Regulated Power Supply Output

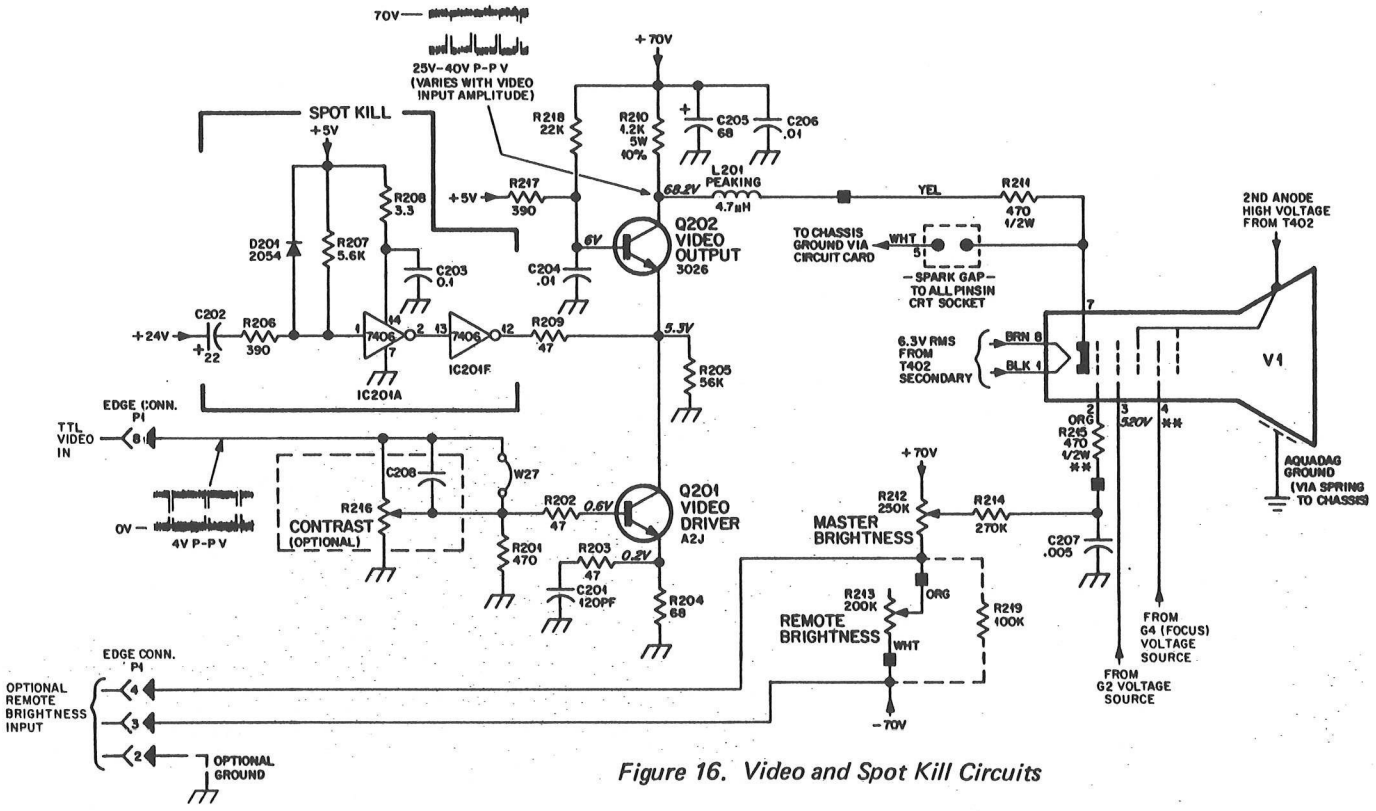


Figure 16. Video and Spot Kill Circuits

biased at 6.0V by R217 and R218. When a video signal is applied to the base of Q201, it turns on, allowing Q202 to conduct. The resultant output is developed across collector load resistor R210 and DC coupled to the CRT cathode via peaking coil L201 and resistor R211. Q202 is protected from CRT arcing by a spark gap built into the CRT socket, and R211 further isolates Q202 from transcients. Capacitor C204 shorts video frequency signals from the base of Q202 to ground. Peaking coil L201 increases the high frequency response of the video amplifier. Capacitor C205 provides filtering of the +70V supply, while C206 is a high frequency AC bypass capacitor to ground.

SPOT KILL (Refer to Figure 16)

When power is removed from the monitor, the horizontal and vertical scans collapse and a bright spot is left that will burn a spot in the phosphor screen unless prevented from doing so.

When the monitor is turned off, the decrease in the 24V supply voltage is coupled through capacitor C202 and resistor R206 to pin 1 of IC201A. This TTL input is normally held in the high state by resistor R207. The falling 24V supply switches IC201A to the low state at pin 1, which is inverted to a high at pin 2 of IC201A; then inverted to a low again by IC201F at pin 12. The open collector output of IC201F, now in the low state (conducting), pulls R209 to ground to become the emitter resistor of Q202. With 6.0 volts on its base, Q202 saturates. The resulting low collector voltage on Q202 is coupled to the CRT cathode causing it to conduct heavily. The large cathode current in the CRT discharges the second anode during scan collapse. The second anode is completely discharged before the scan currents collapse completely so that a spot can not form.

STEPSCAN FUNCTION (Reference Figure 17)

StepScan is useful when it is desired to display more rows of data characters than the existing "alphanumeric video" signal format will permit. A typical display consists of 240 horizontal scan lines which form character rows of data. Between each character row is a desired amount of blank spacing which is made up of horizontal scan lines without video information. By accelerating the vertical deflection between character rows, one (1) horizontal scan line could provide the spacing between rows that would normally be occupies by three (3) horizontal scan lines (see Figure 17). This would reduce the number of blank horizontal scan lines between character rows from three (3) down to one (1). However, the physical spacing between the character rows would not change. Since two (2) horizontal lines are saved between each row, a 24 row format will accumulate 48 unused scan lines. These 48 extra scan lines will reside at the bottom of the display since the CRT still scans a total of 240 horizontal lines. Therefore, the 48 additional lines at the bottom can also be used to display data. This means an additional six (6) rows of characters can be displayed. (For example, 7 lines for char. height plus 1 line for spacing = 8 lines per char. block. 48 unused lines divided by 8 char. block lines = 6 additional rows.)

– NOTE –

StepScan does <u>not</u> actually produce the six (6) additional rows; instead, it simply provides space (and horizontal lines) for them. The six (6) additional rows of video must be designed into the original video signal format during its development.

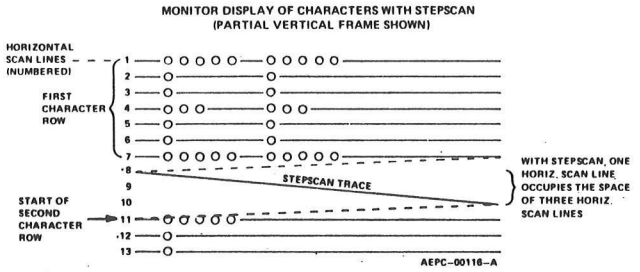


Figure 17. Displaying Characters on a Monitor with StepScan

STEPSCAN CIRCUIT (Refer to Figure 18)

The StepScan circuit requires an external TTL positive-going pulse of approximately 4.0 volts P-P. These pulses are applied to pin 5 of IC201C through the protective network R501, D501 and D502. These pulses switch the TTL input of IC201C from the low state, normally maintained by resistor R502, to the high state. The open collector output of IC201C, pin 6, conducts during these pulses. These current pulses, regulated by control R504, are applied to the height control pin of the vertical processor, IC301. The slope of the output sawtooth current is increased during these pulses to "step" the vertical position to the next character.

The rate at which the vertical processor steps is determined by the repetition rate of the incoming SetpScan pulses. The slope (charge rate) of the stepped portion of the sawtooth is adjustable with the STEP ADJ. control, R504, which varies the spacing between the character rows. With the vertical sawtooth thus modified, the yoke vertical deflection current will be "stepped" during the line between character rows chosen. One additional component associated with StepScan operation is capacitor C307. It increases the response of IC301 internal amplifier output (pin 4) by coupling the leading edge of the StepScan pulses into the amplifier input of IC301 (pin 10).

VERTICAL SCAN (Refer to Figure 18)

Input TTL level pulses pass through resistor R301 and protective diodes D301 and D302 to IC201B or IC201E inputs. The input to IC201B accepts, through jumper JU302, negative vertical sync and the input to IC201E accepts, through jumper JU301, positive vertical sync. R303 holds the input of IC201B low to prevent its output, an open collector, from shorting the input to IC201E when negative sync is not selected.

Output pulses from IC201E (pin 10) are differentiated by capacitor C301 and resistor R306. Diode D303 couples only the negative-going spikes from the differentiator circuit to the sync input of IC301 (pin 8). R307 and R308 provide input current limiting. The sync input (pin 8) performs several functions. It strips away any random noise that may be present on the input line and conditions the vertical pulses for processing. It also converts the input voltage pulses to current to control the internal oscillator. The oscillator generates a non-symetrical square wave with a short duty cycle at the vertical scan frequency (50 to 60 Hz). Components R310, R311 and C304 determine the frequency. This square wave signal is applied to a ramp generator whose slope and amplitude is determined by R312, R313, C305 and C306. The ramp voltage signal is applied to a buffer stage which isolates the ramp generator from the output stages and reduces any loading effect on the previous stages. Components R314, R316 and R315 reshape the ramp voltage to make it extremely linear.

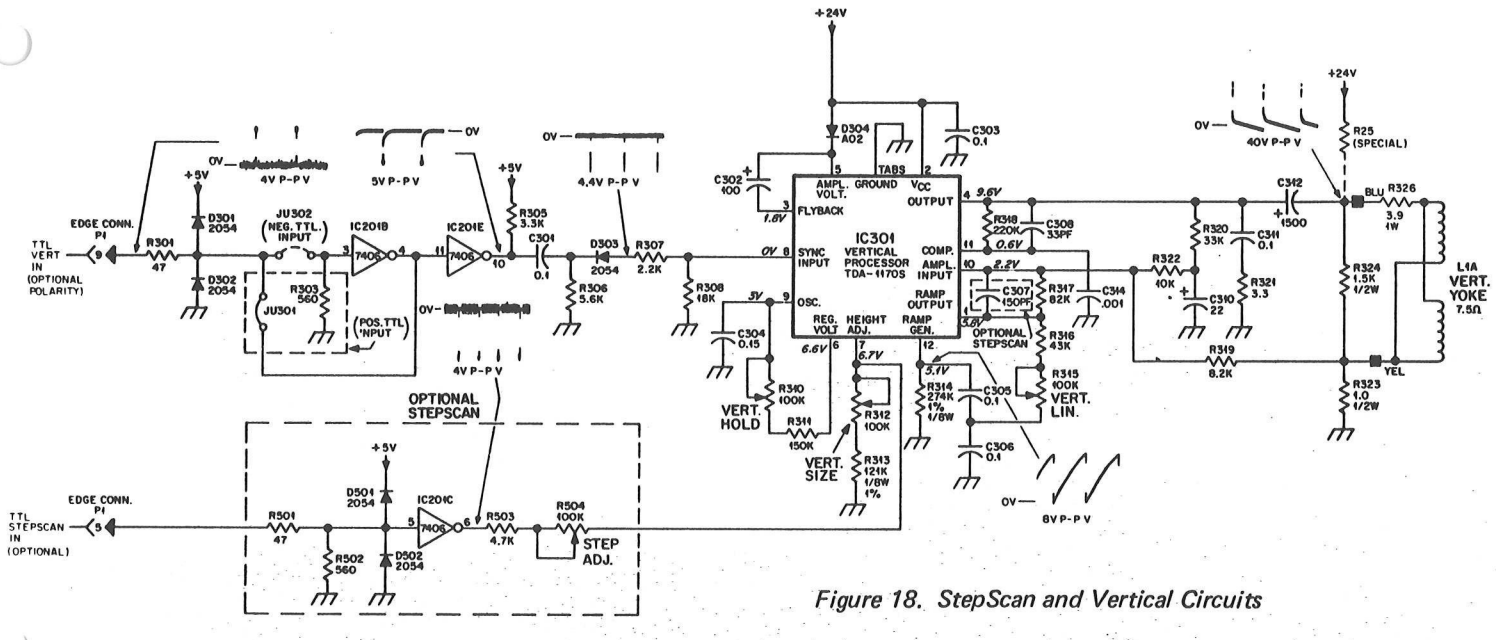


Figure 18. StepScan and Vertical Circuits

The output signal from pin 4 (IC301) drives the vertical deflection coils directly via coupling capacitor C312. Components R321 and C311 provide damping to prevent any oscillations in the output circuit. R320, R322, R319, R318, R323, C310 and C308 provide AC and DC feedback for the output stage to maintain proper gain and linearity. When the scan reaches the bottom of the screen a sync pulse initiates retrace. To insure a quick return to the top of the screen the voltage across the yoke is doubled during retrace to quickly discharge the yoke inductance. This voltage doubling circuit consists of diode D304, capacitor C302 and a transistor network in IC301. Capacitor C314 provides additional (external) compensation for IC301, pin 11. Resistor R325 (when present) is used to up-center the raster and video display.

HORIZONTAL DRIVE/SYNC DELAY AND REGENERATOR (Refer to Figure 19)

TTL horizontal rate sync is coupled to the input of IC401B through the protective network consisting of resistor R401 and diodes D401 andD402. Jumpers W1 or W2 and W3 select positive or negative sync respectively. IC401B is a monostable multivibrator with its time constant being established by resistor R403, HORIZ. DELAY control R402, and capacitor C401. A positive pulse appears at pin 13 of IC401B, the leading edge coincident with the selected leading edge of horizontal sync and the trailing edge determined by the HORIZ. DELAY control, R402.

The falling edge of this pulse triggers IC401A, another monostable multivibrator, whose time constant (established by R406 and C403) regenerate a positive pulse at pin 5 of IC401A. Pulse width at this point is approximately equal to the input sync pulse. This pulse is inverted and increased in amplitude to 24V P-P by IC201D.

PHASE DETECTOR (Refer to Figure 19)

The phase detector consists of two diodes D403 and D404 in a keyed clamp circuit. Its function is to develop a control voltage for synchronizing the horizontal oscillator with the incoming sync pulses. Two inputs are required to generate the required output; one from the horizontal sync regenerator IC401A, and one from the horizontal output circuit, Q402. The required output must be of the proper polarity and amplitude to correct phase differences between the input horizontal sync pulses and the horizontal time base. Each pulse from the collector of the horizontal output, Q402, is integrated into a sawtooth by R411 and C405. Capacitor C406 blocks DC from the collector of Q402. The output transistor of IC201D is normally at cut-off and its collector voltage rests at approximately 24 volts. Since C404 is connected to the output of IC201D, it will charge up to the collector voltage. When a pulse turns on and saturates the output of IC201D, its collector voltage drops to near ground potential. C404 will now discharge, coupling a negative-going sync pulse to the cathodes of D403 and D404. This negative potential is sufficient to forward bias both diodes to conduct and discharge any positive or negative charge on C405 to ground. In other words, it clamps the voltage on capacitor C405 during sync pulse time to approximately zero volts.

Without considering the sync pulses, the sawtooth wave would cause current flow into capacitor C405 when it is negative, and out of C405 when it is positive. Since the sawtooth is symmetrical about its AC axis, the charge and discharge currents of C405 are equal. C405 would therefore average a zero voltage level. A sync pulse (waveform A, Figure 20) clamping the sawtooth as it passes through its AC axis (waveform B, Figure 20), will not affect its positive and negative symmetry. Therefore, the average voltage on C405 would remain zero. However, if the horizontal time base begins to lag, the sync pulse will clamp the sawtooth to ground at a point below its AC axis, resulting in a non-symmetrical charge on C405. This clamping action will cause the sawtooth's AC axis to shift to a point above the

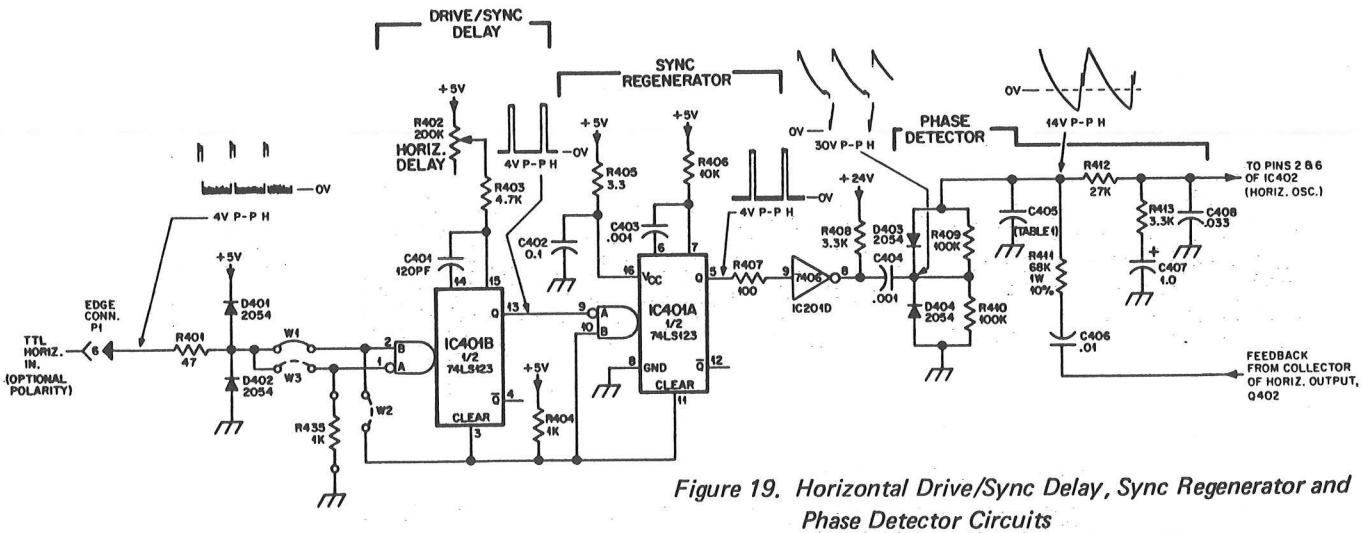


Figure 19. Horizontal Drive/Sync Delay, Sync Regenerator and Phase Detector Circuits

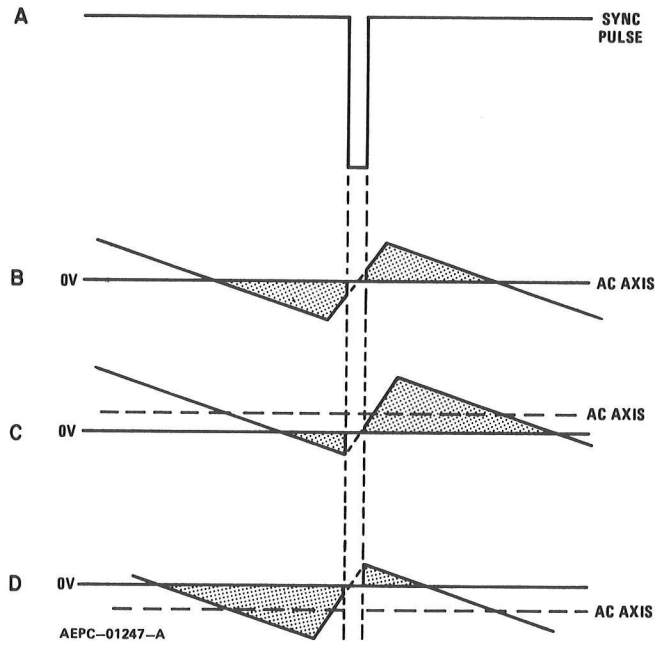


Figure 20. Phase Synchronization Waveforms

ground reference (waveform C, Figure 20). Therefore, most of the sawtooth's waveform is now above ground which will produce a positive voltage on C405. This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag. Likewise, if the horizontal time base is leading the sync pulse, the sawtooth will be clamped to ground at a point above its AC axis. This clamping action will cause the sawtooth's AC axis to shift to a point below the ground reference (waveform D, Figure 20). Now most of the sawtooth's waveform is below ground, which will produce a negative voltage on C405. This is the correct polarity to cause the horizontal oscillator to slow down. The voltage level on C405 is dependent upon which point of the sawtooth is clamped. This also determines how far its AC axis will shift above or below ground.

R412, C407, R413 and C408 comprise the phase detector filter. The bandpass of this filter is designed to provide correction of horizontal oscillator phase without ringing or hunting.

HORIZONTAL OSCILLATOR/DRIVER (Refer to Figure 21)

Integrated circuit timer IC402 operates as an astable square wave oscillator. Its free running frequency is determined by resistors R415, R416, and capacitor C409. The phase detector correction voltage is coupled through resistor R414 to pins 2 and 6 of IC402 to vary the frequency of the oscillator. A second input to IC402, pin 5, allows control of the oscillator free-run frequency by means of R418, HORIZ. HOLD control.

The non-symmetrical output of IC402 (pin 3) is coupled to the horizontal driver transistor, Q401, through C411 and current limiting resistor R419. D405 protects Q401 from reverse base-emitter voltage. Q401 operates as a switch to drive the horizontal output transistor Q402 through transformer T401. T401 is a voltage stepdown transformer to provide a low impedance drive to Q402. R421 is a current limiting resistor for Q401 and C414 is an AC bypass capacitor. R420 and C413 damp the transformer to prevent ringing when Q401 goes into cutoff.

HORIZONTAL OUTPUT (Refer to Figure 21)

The secondary of T401 provides the required low drive impedance for Q402. Components R422 and C415 form a time constant for fast turn-off of Q402. The horizontal output transistor, Q402, is simply a switch that is turned on and off at the horizontal scan rate by the drive signal applied to its base. A sawtooth current through the deflection coils is required to sweep the beam linearly across the CRT screen. The sweep begins at the center of the CRT and sweeps to the right. This happens when Q402 is turned on and its collector voltage drops to near zero. C419 begins discharging through the deflection coils to deflect the beam to the right edge of the CRT. At this time, Q402 cuts off and C419 ceases to supply current to the deflection coils. However, an induced voltage appears across the deflection coil as the magnetic field collapses, and an oscillation occurs between the deflection coils and C416.

During the first half cycle of this oscillation, the induced voltage is felt across the collector of now cut off Q402, C416, and the primary of T402, the flyback transformer. This voltage is stepped up by T402 and rectified to produce the required high voltage that is applied to the 2nd anode of the CRT. The electron beam is also deflected to the left edge of the CRT at this time because the collapsing magnetic field of the deflection coils reverses polarity.

During the second half cycle of the deflection coils/C416 oscillation, the voltage on the collector of still cut off Q402 becomes negative. At this time, camper diode D406 becomes forward biased and begins conduction. The deflection coil current gradually decreases to zero during damper conduction allowing the beam to sweep linearly to the center of the screen.

The horizontal retrace pulse charges C422 through D407 to provide operating voltage for G2 of the CRT. Momentary transients at the colleator of Q402, should they occur, are limited to the voltage on C422 since D407 will conduct if the collector voltage exceeds this value. Coil L402 is a magnetically biased Horiz. Linearity coil that shapes the deflection current for optimum trace linearity. Coil L401 is a series Horiz. Width control. Components R425 and C418, R424 and C417 are damping network components for the Horizontal Linearity (L402) and Width (L401) controls.

The 24 volt supply to the horizontal output is coupled through diode D409 to pin 3 of the transformer, T402. Autoformer action of the transformer boosts the effec-

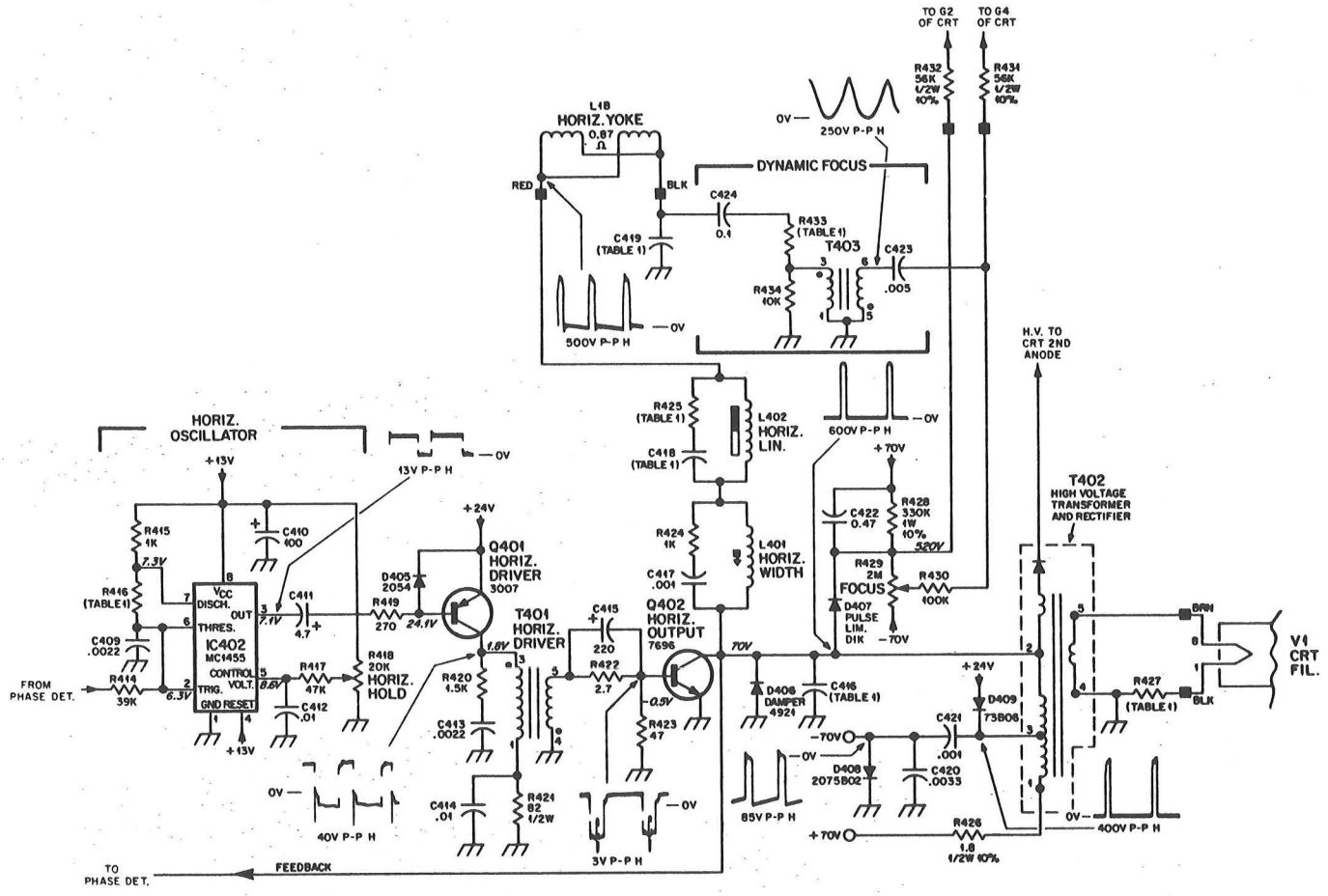
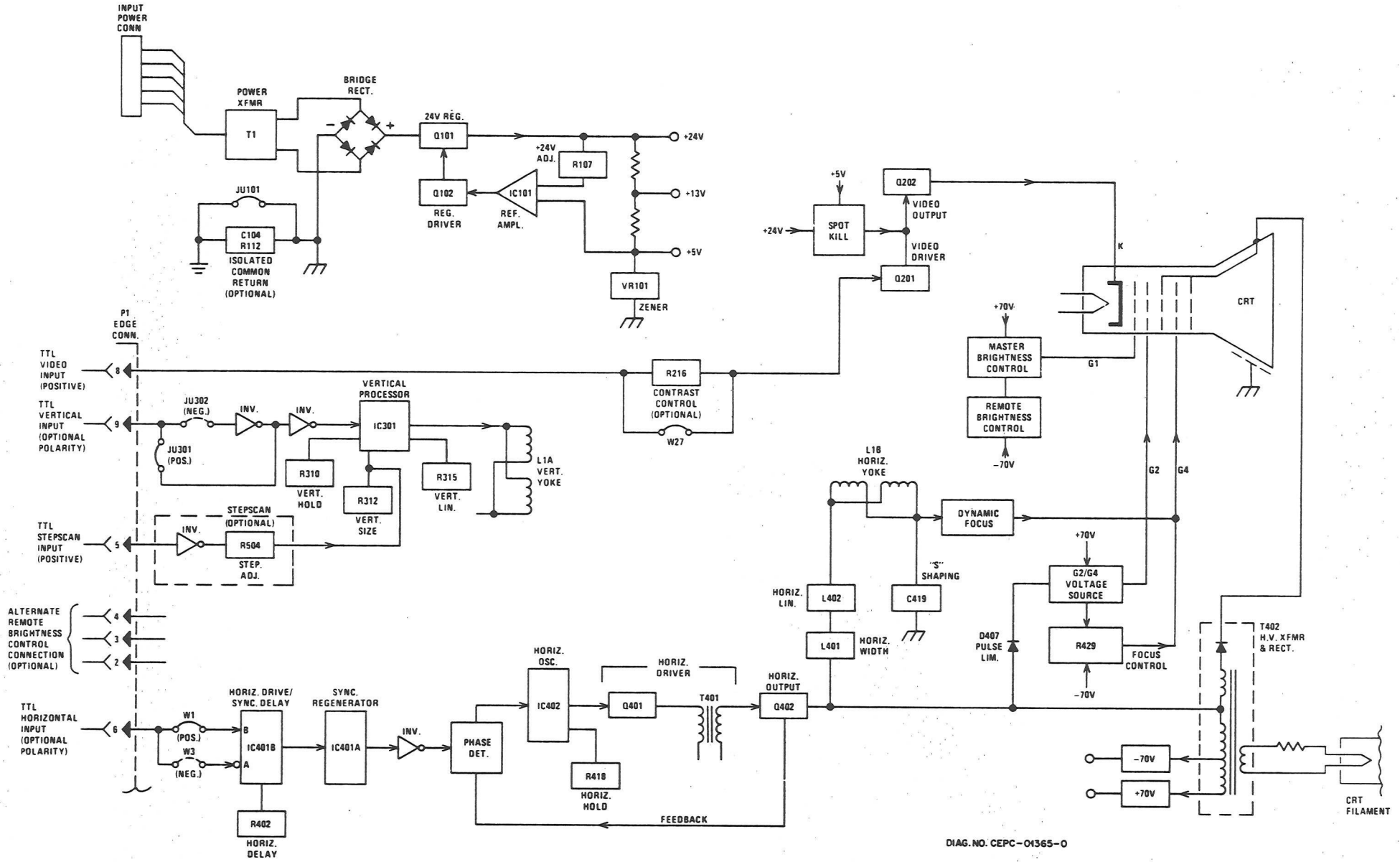


Figure 21. Horizontal Oscillator, Driver and Output Circuits, and Dynamic Focus Circuit

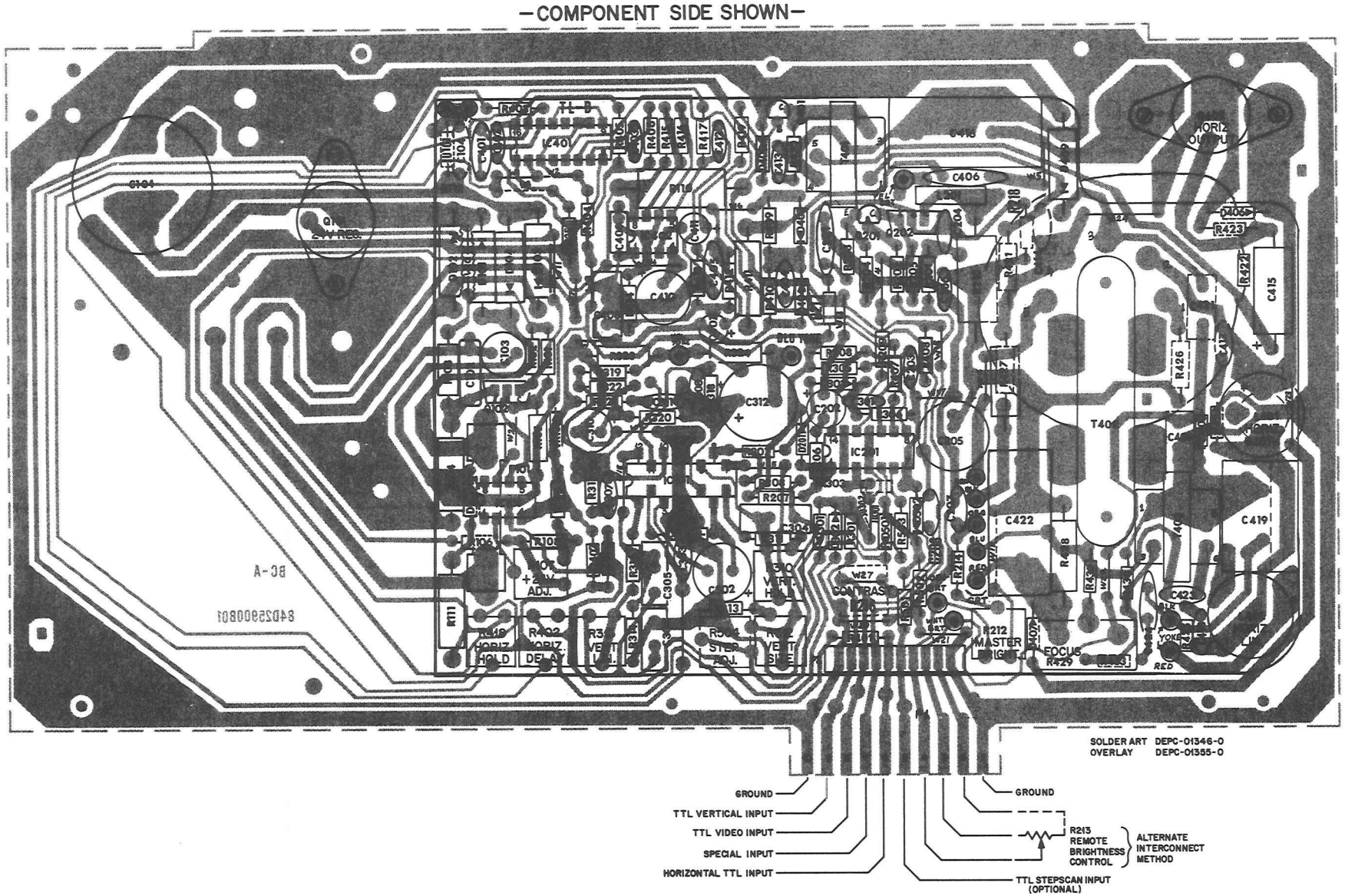
tive supply voltage to the transformer to the 70 volts appearing on pin 1 of T402. This voltage is filtered by C205 and provides the 70 volt source for the chassis. A capacitive divider, C421 and C420, and diode D408 provides a −70 volt supply for the CRT G1 electrode.

DYNAMIC FOCUS (Refer to Figure 21)

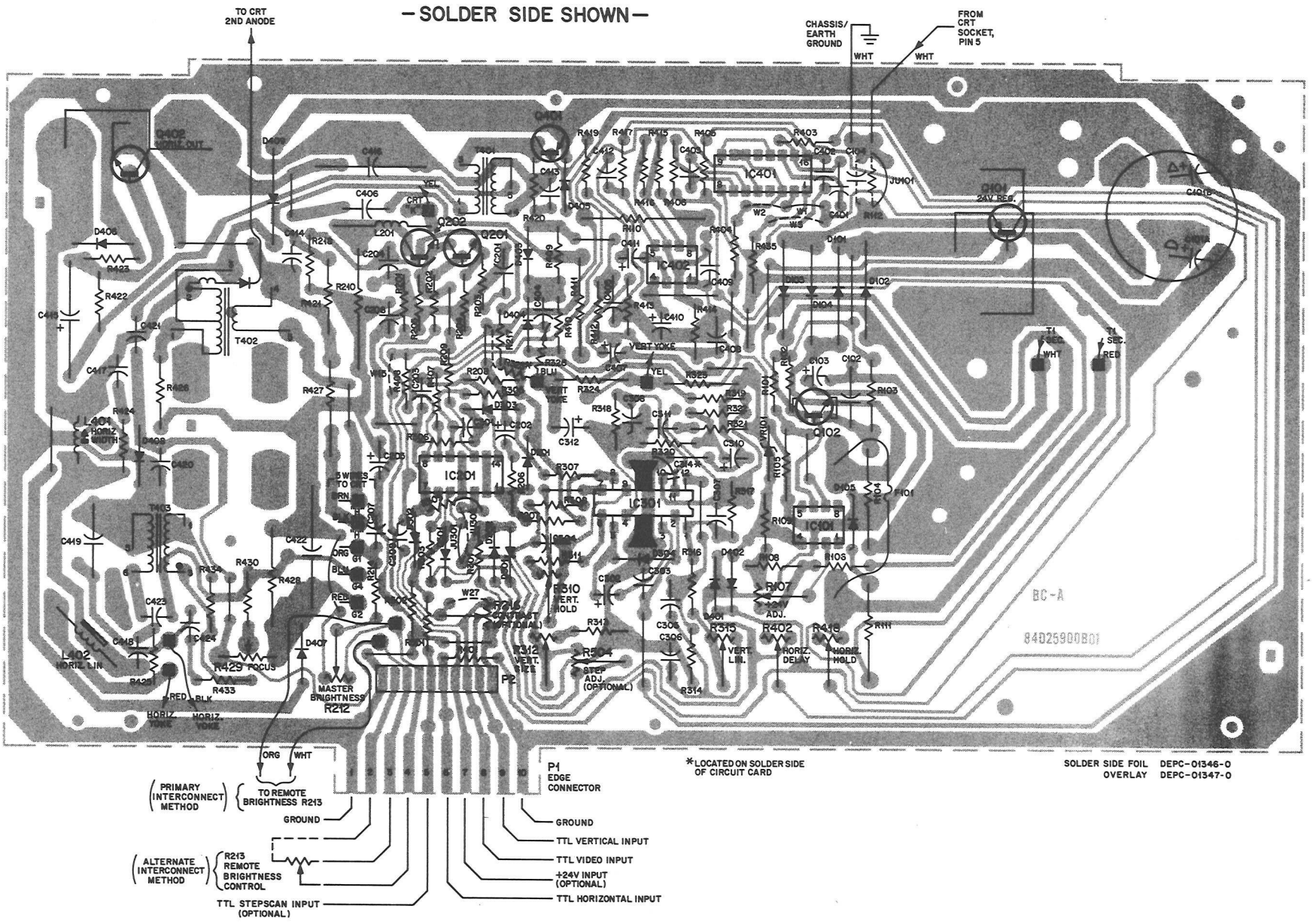
Due to the geometry of a CRT, the electron beam travels a greater distance when deflected to a corner as compared to the distance traveled at the center of the CRT screen. As a result of these various distances traveled, optimum focus can be obtained at only one point. For general applications, an adequate adjustment can be realized by setting the focus while viewing some point mid-way between the center of the CRT screen and a corner, thus optimizing the overall screen focus. When an application requires a tighter specification, one of the simplest methods for improvement is to modulate the focus voltage at a horizontal sweep rate. Now optimum focus voltage is made variable on the horizontal axis of the CRT, which compensates for the beam travel along this axis. The AC component of the focus voltage is developed by stepping up the voltage across capacitor C419 via transformer T403. The linear current ramp in the horizontal yoke winding, L1B, also flows through capacitor C419. The ramp is integrated, the result being a parabolic waveform. This parabola is coupled through capacitor C424 and resistor R433 to the primary of transformer T403. The approximately 250V P-P parabola present at pin 6 of T403 is superimposed on the DC voltage from the FOCUS control, R429, via capacitor C423. This mixed AC and DC voltage results in a waveform of proper phase and amplitude, which is coupled through isolating resistor R431 to the CRT focus anode.



Block Diagram



Circuit Card Layout — Component Side



Circuit Card Layout — Solder Side

MDS SERIES REPLACEMENT PARTS LIST

– NOTE –

When a component requires replacement, it is recommended that only Motorola part numbers be used. This is necessary to ensure optimum performance and reliability from selected components with specific operating characteristics. When a part number is not listed, however, an equivalent may be substituted.

The following parts list represents components for the four (4) basic CRT display models; MDS3000, MDS3003, MDS4000 and MDS4003 Series. For replacement of components that differ in unique CRT display models, compared to the four (4) basic models, order by the unique model number, schematic designator and description.

REF NO.	PART NO.	DESCRIPTION
CIRCUIT CARD ASSEMBLY: (Order by model number only)		
CAPACITORS: (Unless otherwise noted, all capacitor values are in microfarads)		
C101	23R29944A05	4500/50V, 2000/30V; Lytic
C102	8R29967A12	0.22 10%, 50V; Poly
C103	23R29914A21	100, 10V; Lytic
C104	–	0.1 (Optional)
C201	21S180E50	120 pF 5%, NPO, 100V; Cer.
C202	23R29914A77	22, 35V; Lytic
C203	21R29964A05	0.1 +80–20%, Z5U, 100V; Cer.
C204	21S132492	.01 +80–20%, Z5V, 100V; Cer.
C205	23R29944A06	68, 100V; Lytic
C206	21S132492	.01 +80–20%, Z5V, 100V; Cer.
C207	21S180A62	.005 20%, Z5U, 500V; Cer.
C208	–	(Special)
C301	21R29964A05	0.1 +80–20%, Z5U, 100V; Cer.
C302	23R29914B06	100, 50V; Lytic
C303	21R29964A05	0.1 +80–20%, Z5U, 100V; Cer.
C304	8R29967C31	0.15 10%, 100V; Poly
C305,C306	8R29967C29	0.1 10%, 100V; Poly
C307	21S180C17	150 pF 10%, Z5F, 500V; Cer.
C308	21S180B94	33 pF 10%, NPO, 500V; Cer.
C309	(Not Used)	
C310	23R29914A77	22, 35V; Lytic
C311	21R29964A05	0.1 +80–20%, Z5U, 100V; Cer.
C312	23R29914A68	1500, 25V; Lytic
C313	(Not Used)	
C314	21S180B51	.001 10%, X5F, 500V; Cer.
C401	21S180E50	120 pF 5%, NPO, 100V; Cer.
C402	23R29964A05	0.1 +80–20%, Z5U, 100V; Cer.
C403,C404	21S180B51	.001 10%, X5F, 500V; Cer.
C405	21S180C41	.0027 10%, Z5F, 100V; Cer. (MDS3003, 4003 Series)
C405	21S180B71	.0039 20%, Z5F, 100V; Cer. (MDS3000, 4000 Series)
C406	21S180C31	.01 20%, Z5U, 1kV; Cer.
C407	23R10229A32	1.0, 16V; Lytic
C408	8R29967A36	.033 10%, 200V; Poly
C409	21R29964A06	2200 pF 2%, NPO, 100V; Cer.
C410	23R29914A40	100, 16V; Lytic
C411	23R29914A73	4.7, 35V; Lytic
C412	21S180E60	.01 +80–20%, Z5V, 50V; Cer.
C413	21S180C08	.0022 10%, Z5F, 50V; Cer.
C414	21S132492	.01 +80–20%, Z5V, 100V; Cer.
C415	23S10255B81	220, 10V; Lytic
C416	8R29930E45	.0091 5%, 1200V; Poly Carb (MDS4000)
C416	8R29930E46	.01 5%, 1200V; Poly Carb (MDS4003)
C416	8R29930E41	.0068 5%, 1200V; Poly Carb (MDS3000)
C416	8R29930E97	.011 5%, 1200V; Poly Carb (MDS3003)
C417	21S180B51	.001 10%, X5F, 500V; Cer.
C418	21S131625	330 pF 10%, X5F, 500V; Cer. (MDS3003,4000)
C418	21S180E78	270 pF 10%, X5F, 500V; Cer. (MDS3000,4003)
C419	8R29951A07	1.0 10%, 200V; Poly (MDS4000, 4003)
C419	8R29951A06	0.68 10%, 200V; Poly Carb (MDS3000, 3003)
C420	8R29967A31	.0033 10%, 200V; Poly
C421	8R29967A58	.001 10%, 600V; Poly
C422	8R29969A85	0.47 10%, 600V; Mtlz. Poly
C423	21S180A62	.005 20%, Z5U, 500V; Cer.
C424	21R29964A05	0.1 +80–20%, Z5U, 100V; Cer.
C425		(Special)
DIODES:		
D101-D104	48R191A12	Rectifier, Silicon; (91A12)
D105	48R02054A00	Silicon Diode, Gen. Purpose; (2054)
D201	48R02054A00	Silicon Diode, Gen.Purpose (2054)
D301-D303	48R02054A00	Silicon Diode, Gen.Purpose (2054)
D304	48R191A02	Rectifier, Silicon; (91A02)
D401-D405	48R02054A00	Silicon Diode, Gen. Purpose (2054)
D406	48R134921	Silicon Diode, Damper; 800V (4921)
D407	48R134978	Silicon Diode; (D1K)
D408	48R02075B02	Diode, Fast Recovery; 200V (75B02)
D409	48R02073B06	Diode, Fast Recovery; 600V (73B06)
D501,D502	48R02054A00	Silicon Diode, Gen.Purpose;(2054)
FUSES:		
F101	65S129421	2.5 Amp., 250V (120, 220 240VAC Operation)
INTEGRATED CIRCUITS:		
IC101	51R10732A01	IC, Op. Ampl.; T3F
IC201	51R10834A04	IC, 6-Inverter; 7406
IC301	51R06015A00	IC, Vert. Processor; TDA1170S
IC401	51R06621A00	IC, Dual Retrig. Monostable; 74LS123
IC402	51R06332A00	IC, Timing; NE555
COILS:		
L201	24D25601A02	Coil, 4.7 uH; (Peaking)
L401	24D25603A14	Coil, Horiz. Size
L402	24D25600A10	Coil, Horiz. Linearity (MDS4000)
L402	24D25600A13	Coil, Horiz. Linearity (MDS4003)
L402	24D25600A11	Coil, Horiz. Linearity (MDS3000)
L402	24D25600A12	Coil, Horiz. Linearity (MDS3003)
TRANSISTORS:		
Q101	48R137675	PNP; 7675 (24V Reg.)
Q102	48R03026A00	NPN; 3026 (Reg. Driver)
Q201	48R134952	NPN; A2J (Video Driver)
Q202	48R03026A00	NPN; 3026 (Video Output)
Q401	48R03007A00	PNP; 3007 (Horiz. Driver)
Q402	48R137696	NPN; 7696 (Horiz.Output)
RESISTORS/CONTROLS: (Unless otherwise noted, all values are in ohms, 1/4 watt, 5%. Resistors not listed are of the fixed carbon film type, 1/4 or 1/2 watt, 5%, as noted on the schematic.) Abbr; FCF = Fixed Carbon Film, FCC = Fixed Carbon Composition, FMF = Fixed Metal Film, WW = Wirewound		
R104	6S126A33	FCC; 220 5%, 1W
R107	18D25904A05	Control, Var.; 10k (+24V Adj.)
R110	6S127A25	FCC; 100 5%, 2W (Standup Type)
R111	6S126A23	FCC; 82 5%, 1W
R210	17S647132	WW, 1.2k 10%, 5W
R212	18D25904A02	Control, Var.; 250k (Master Brightness)
R213	18D25212A39	Control, Var.; 200k (Remote Brightness)
R214	6S124B08	FCC; 270k
R310	18D25904A04	Control, Var.; 100k (Vert. Hold)
R312	18D25904A12	Control, Var.; 100k (Vert. Size)
R313	6S10621D96	FMF; 121k 1%, 1/8 W
R314	6S10621E31	FMF; 274k 1%, 1/8W
R315	18D25904A04	Control, Var.; 100k (Vert. Lin.)
R323	6S125B70	FCC; 1.0 10%, 1/2W
R326	6–126B59	FCC; 3.9 5%, 1W
R402	18D25904A03	Control, Var.; 200k (Horiz.Delay)
R411	6S124481	FCC; 68k 10%, 1W
R416	6R29891A19	FMF; 15.4k 1%, 1/8W (MDS3003, 4003)
R416	6R29891A26	FMF; 18.2k 1%, 1/8W (MDS3000, 4000)
R418	18D25904A06	Control, Var.; 20k (Horiz.Hold)
R421	6R8259FM12	FMF; 82 1%, 1/2 W
R426	6S125D72	FCC; 1.8 10%, 1/2W
R427	6S10053J05	FCC; 1.0 5%, 1/2W
R428	6S125793	FCC; 330k 10%, 1W
R429	18C25218A14	Control, Var.; 2M (Focus)
R504	18D25904A04	Control, Var.; 100k (Step Adj.)
TRANSFORMERS:		
T401	25D25772A04	Transformer, Horiz. Driver
T402	24D25291A12	Transformer, High Voltage; Incl. H.V. Rect. (MDS4000)
T402	24D25291A13	Transformer, High Voltage; Incl. H.V. Rect. (MDS4003)
T402	24D25291A10	Transformer, High Voltage; Incl. H.V. Rect. (MDS3000)
T402	24D25291A11	Transformer, High Voltage; Incl. H.V. Rect. (MDS3003)
T403	25D25771B05	Transformer, Dynamic Focus
ZENER DIODES:		
VR101	48S10813A06	Diode, Zener; 5.1V (IN5231B)
CHASSIS MOUNTED COMPONENTS:		
L1	24D25687B18	Yoke, Deflection (MDS4000 Series)
L1	24D25687B17	Yoke, Deflection (MDS4003 Series)
L1	24D25687B19	Yoke, Deflection (MDS3000 Series)
L1	24D25687B16	Yoke, Deflection (MDS3003 Series)
S1	15R29982A06	Housing, Recept.; 6-Contact (less contacts)
	39S10184A64	Contact, Recept,; Female (S1 requires 5)
T1	1V25564B27	Transformer, Power (Incl. Conn S1)
T1	25D25239B49	Transformer, Power (Less Conn.S1)

– CRT REPLACEMENT NOTE –

Order replacement CRT's by referring to the CRT Identification Label on the bell of the tube. There will be a manufacturers Type Number, and a Motorola Part Number that begins with a 96 prefix. (An example of the complete Motorola No. would be 96R02500B04.) If the label is not present, or legible, order the replacement CRT by the complete model number; such as MDS4000–100.

MECHANICAL PARTS LIST

REF. NO.	PART NO.	DESCRIPTION
	41B25930A01	Spring, Aquadag
	42B25158C01	Clamp, Deflection
	1V25574A01	Socket, CRT (Incl. leads and resistors)
	14S562353	Insulator, Transistor
	7D25901A01	Bracket, Side; Right-Hand (MDS4000, 4003)
	7D25901A02	Bracket, Side; Left-Hand (MDS4000, 4003)
	7C25902A01	Bracket, Mounting Foot (2 Req'd.)
	7C25826A04	Heat Sink/Support (IC301)
	42S10122A12	Clip, Fuse; F101 (2 Req'd.)
	7D25307C01	Bracket, Side; Right-Hand (MDS3000, 3003)
	7D25307C02	Bracket, Side; Left-Hand (MDS3000, 3003)
	58B25944A01	Adapter, Adjusting Control

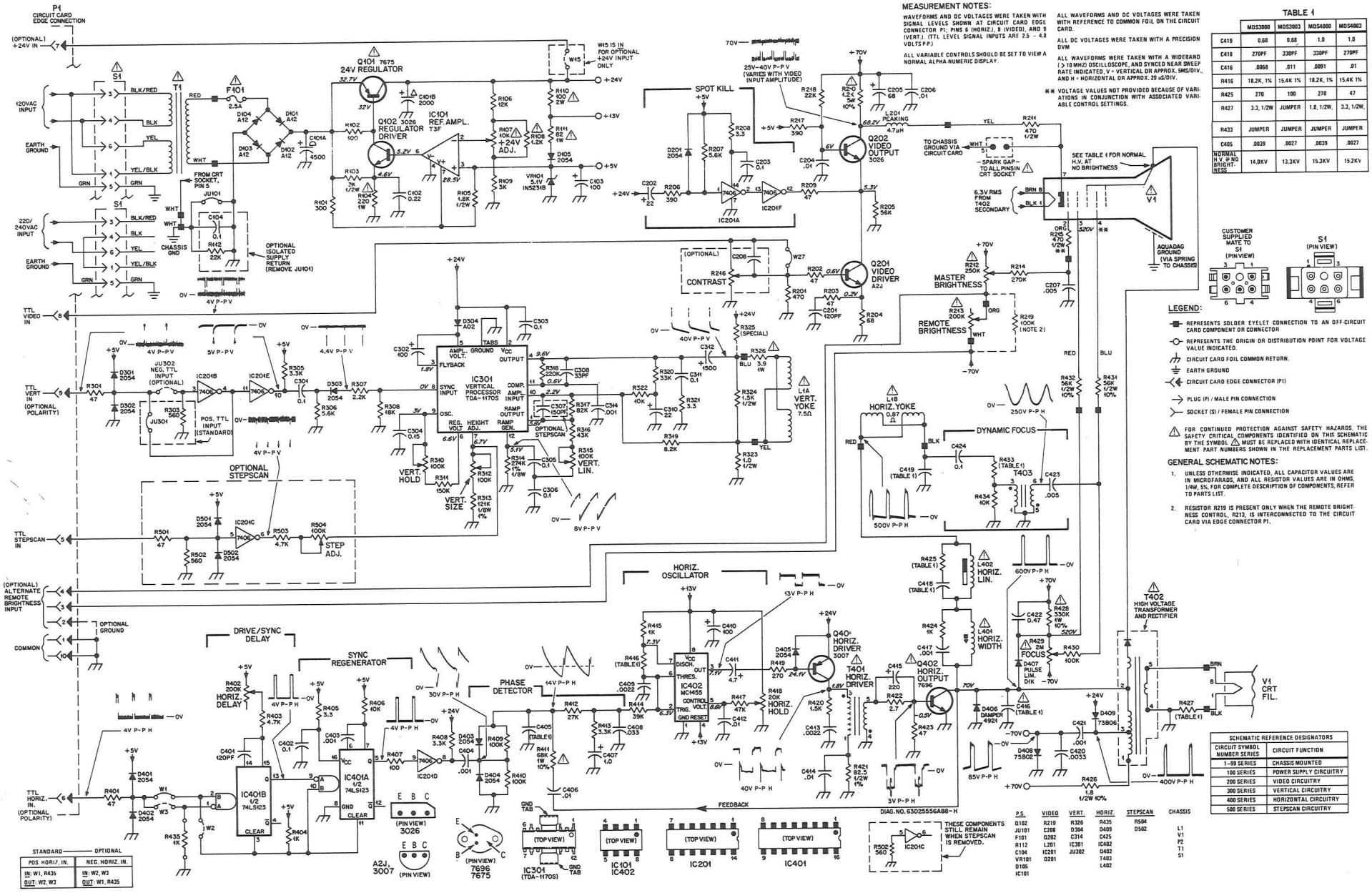
MOTOROLA INC.
Display Systems

1299 E. Algonquin Road, Schaumburg, IL. 60196 (312)397-8000

SCHEMATIC DIAGRAM & ELECTRICAL/MECHANICAL PARTS LIST
MDS3000, 3003 SERIES (12 INCH CRT DISPLAY MONITORS)
MDS4000, 4003 SERIES (15 INCH CRT DISPLAY MONITORS)

RELEASED
1/81

SERVICE SHEET
68P25253A84–O



BASIC MDS SERIES SCHEMATIC DIAGRAM

(Use in conjunction with Service Manual 68P25253A82; VP38)

APPENDIX C

BASF 6106/6108 MINI DISK DRIVE TECHNICAL MANUAL

BASF

6106/6108 LSI

Part N° 80307-050

REVISION	RECORD OF REVISION	REMARKS
01	LSI/K	valid for LSI-version

L I S T O F C O N T E N T S

L I S T O F I L L U S T R A T I O N S

L I S T O F T A B L E S

SECTION I.
INTRODUCTION

1.1. GENERAL

This manual contains descriptive material and procedures useful in installation, operation, maintenance and repair of the BASF Mini Disk Drive Models BASF 6106 and BASF 6108.

1.2. RELATED DOCUMENTATION

Product- and Interface Specification :
BASF 6106/08 : 80 307-046

1.3. DESCRIPTION

The models BASF 6106 and BASF 6108 are very compact random access data storage units, which utilize a 5.25" Flexy Disk as storage medium. The BASF 6106 stores data on one side of the Flexy Disk,the BASF 6108 on both sides.

The Flexy Disk is rotated at 300 RPM yielding a data transfer rate of 125.000 bits per second in single density, and twice as much in double density.

Data capacity on all 40 tracks varies from 81.92 kbytes (BASF 6106, 16 sectors at 128 bytes) to 368.64 kbytes, so increasing capacity more then four times by using the BASF 6108 with 9 sectors of 512 bytes each.

The Mini Disk Drives are equipped with a DC-controlled spindle drive motor, thus no AC-power is needed. Ceramic read/write heads with tunnel erase are used within the BASF 6106/6108 to ensure reliable data recording.

The heads are positioned with a fourphase DC-stepper motor actuator, utilizing a spiral wheel which provides precise location of the read/write head or heads on the track.

In the electronic, a large scale integrated circuit (LSI) in NMOS technique is used,which contains most of the digital control logic of the drive. The LSI increases the reliability of the electronic and decreases the repair time.

Applications for both types of mini disk drives comprise word processing and text editing systems, program storage for mini and micro computers, "intelligent" desktop calculators and the hobby micro computer market.

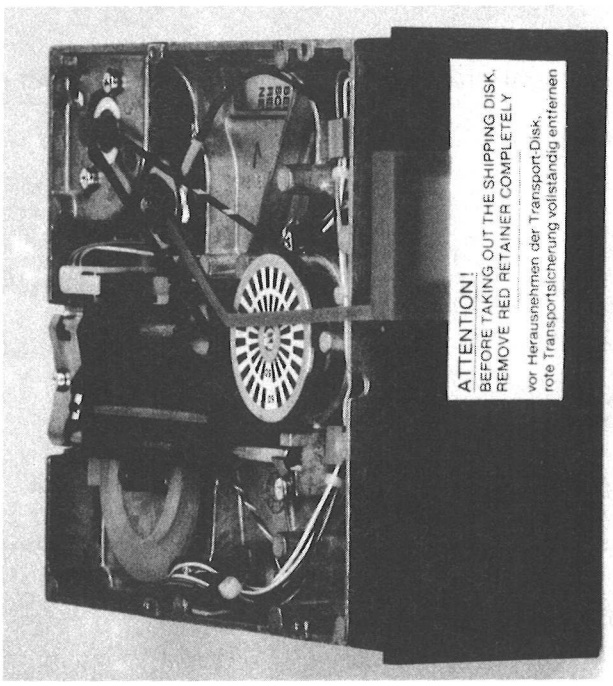


FIGURE 1 - 1 : MODEL BASF 6106/6108 MINI DISK DRIVE

1.4 SPECIFICATION SUMMARY

A comprehensive list of principal specifications for model BASF 6106 and model BASF 6108 is provided in table 1 - 1.

P E R F O R M A N C E S P E C I F I C A T I O N S

CAPACITY	BASF 6106 (single sided)		BASF 6108 (double sided)	
Unformatted	Single Density	Double Density	Single Density	Double Density
per Disk	125 Kbytes	250 Kbytes	250 Kbytes	500 Kbytes
per Surface	125 Kbytes	250 Kbytes	125 Kbytes	250 Kbytes
per Track	3.125 Kbytes	6.250 Kbytes	3.125 Kbytes	6.25 Kbytes
Formatted (16 Sectors/Track)				
per Disk	81.920 Kbytes	163.840 Kbytes	163.840 Kbytes	327.680 Kbytes
per Surface	81.920 Kbytes	163.840 Kbytes	81.920 Kbytes	163.840 Kbytes
per Track	2.048 Kbytes	4.096 Kbytes	2.048 Kbytes	4.096 Kbytes
per Sector	128 bytes	256 bytes	128 bytes	256 bytes
TRANSFER RATE	125 Kbits/s	250 Kbits/s	125 Kbits/s	250 Kbits/s

LATENCY

Maximum	200 ms
Average	100 ms

ACCESS TIME

Track to track positioning	12 ms
Average	240 ms
Settling Time	max. 48 ms
Head Load Time	max. 35 ms
Drive Motor Start Time	max.650 ms

F U N C T I O N A L S P E C I F I C A T I O N S

	BASF 6106		BASF 6108	
	Single Density	Double Density	Single Density	Double Density
Rotational Speed	300 RPM ± 2,5 %	300 RPM ± 2,5 %	300 RPM ± 2,5 %	300 RPM ± 2,5 %
Recording Density (inside Track)	3979 BPRAD (2768 BPI)	7958 BPRAD (5536 BPI)	3979 BPRAD (2768 BPI)	7958 BPRAD (5536 BPI)
Flux Density	7958 FTPRAD (5536 FCI)	7958 FTPRAD (5536 FCI)	7958 FTRAD (5536 FCI)	7958 FTPRAD (5536 FCI)
Track Density	48 TPI	48 TPI	48 TPI	48 TPI
Track Radius Track 00 Track 39	 57,15 mm 36.5125 mm	 57,15 mm 36.5125 mm	 55,03 mm +) 34.3958 mm +)	 55,03 mm +) 34.3958 mm +)
Encoding Method	FM	MFM	FM	MFM
Media Requirements	BASF Flexy Disk 5.25"-1	BASF Flexy Disk 5.25"-1D	BASF Flexy Disk 5.25"-2	BASF Flexy Disk 5.25"-2D

+) On Side 1, Side 0 see 6106
Track radius 1 is 2. 1167 mm
smaller then track radius 0.

TABLE 1 - 1 : SPECIFICATION SUMMARY (continued)

PHYSICAL SPECIFICATIONS

Environmental limits	
Ambient temperature on disk surface (operation)	10° to 50°C (50°F to 120°F)
Relative humidity	20 % to 80 %
Maximum wet bulb	29°C (84°F)
DC-voltage requirements	+ 12 VDC ± 5 % 0,7 A+)
	max. 100 mVpp ripple
	+ 5 VDC ± 5 % 0,5 A
	max. 50 mVpp ripple
	+) additional motor starting current : max. 0.65 A for max. 50 msec
	head load start current 0.7 A for 50 msec
Power dissipation	10.0 Watts operating
	4.0 Watts stand by (motor off)
	7.5 Watts motor on and deselected
Mechanical dimensions:	
Width	146.1 mm (5.75 inch)
Height	53.5 mm (2.11 inch)
Depth	190.0 mm (7.48 inch)
Weight	1.4 kg

RELIABILITY SPECIFICATIONS

MTBF	10 000 POH under typical usage+)
Unit life time	5 years
MTTR	30 minutes
Error rates:	
Soft read errors	1 per 10^8 bits read
Hard read errors	1 per 10^{11} bits read
Seek errors	1 per 10^6 seeks

+) Duty cycle of Spindle Drive Motor: 20 % of POH

MEDIA SPECIFICATIONS

Jacket	133.4 mm (5.25 inch) square
Disk	130.2 mm (5.125 inch) diameter
Center hole	28.58 mm (1.125 inch) diameter

TABLE 1 - 1 : SPECIFICATION SUMMARY

1.5. OPTIONS SUMMARY

The following tables list the options of the BASF 6106 and BASF 6108 mini disk drives.

1.5.1. FACTORY INSTALLED OPTION

Option	Function
Door Lock Solenoid	Locks the front door under control of the users software.

TABLE 1 - 2 : FACTORY INSTALLED OPTION

1.5.2. JUMPER OPTIONS

The following options are selectable by jumpers on the PCB. Refer to table 3 - 10 for jumper option matrix.

Option	Function
RADIAL SELECT	Allows the connection of four mini disk drives to the host system. Each drive has an own address (0,1,2,3) selectable by jumper.
AUTO SELECT	The interface is always enabled (drive is always selected). The SELECT-lines are not used.
HEAD LOAD	Loading of the head can be accomplished in three modes: ● Selected Head Load (INT.SELECT• HEAD LOAD) ● Auto Head Load (INT. SELECT) ● Radial Head Load (HEAD LOAD) The head will be loaded only if the inserted mini disk rotates.
IN USE	Pin 34 of the interface is used as IN USE input signal and controls the door lock solenoid and the activity indicator. If this option is used the disk change option must be disabled.
DOOR LOCK LATCH	Allows locking of the door without maintaining the IN USE signal activated by storing the state of the IN USE-signal into the IN USE-flipflop. To use this option, the IN USE-option must be jumpered.
DISK CHANGE	Notifies the host system that the mini disk has been changed. If this option is used, the IN USE-option must be disabled.
DOOR LOCK	Locking of the door can be accomplished as follows : 1. by the IN USE-signal 2. by the IN USE-FF (DOOR LOCK LATCH) 3. if the drive is selected (SELECT active) 4. if the head is loaded (HEAD LOAD active) 5. if 1. or 2. is true 6. if 1. or 3. is true 7. if 1. or 4. is true 8. if 2. or 3. is true 9. if 2. or 4. is true 10. if 1. or 2. or 3. is true 11. if 1. or 2. or 4. is true
ACTIVITY INDICATOR OPTIONS	The lighting of the activity LED is selectable by jumper to one of the following conditions: - the head is loaded and the drive is ready - the door is locked and the drive is ready - HEAD LOAD is active - the door is locked
WRITE PROTECT OPTION	Allows protection of the mini disk against overwrite if the write protect notch is closed (ECMA, Shugart).
STEPPER MOTOR SWITCHING	The stepper motor is switched on and off together with the drive motor if a jumper is inserted. If the jumper is not inserted, the stepper motor will be enabled as long as power is supplied.

TABLE 1 - 3 : JUMPER SELECTABLE OPTIONS

1.6. RECORDING MEDIA

The BASF mini disk drives use a removable 130 mm (5.25 inch) diameter flexible disk as storage media. Figure 1 - 2 shows construction and dimensions of a typical 5.25" flexy disk. The recommended recording media is :

- for model BASF 6106 mini disk drives :
  single density : BASF 5.25"-1
  double density : BASF 5.25"-1D

- for model BASF 6108 mini disk drives :
  single or double density : BASF 5.25"-2D

The flexy disk is an oxide coated flexible disk enclosed in a protective plastic envelope. The protective envelope contains apertures for head contact , index detection, write protect detection and drive spindle loading.
The write protect notch is used to protect the written data on the flexy disk (see 2.3.14.4. write protect detector).

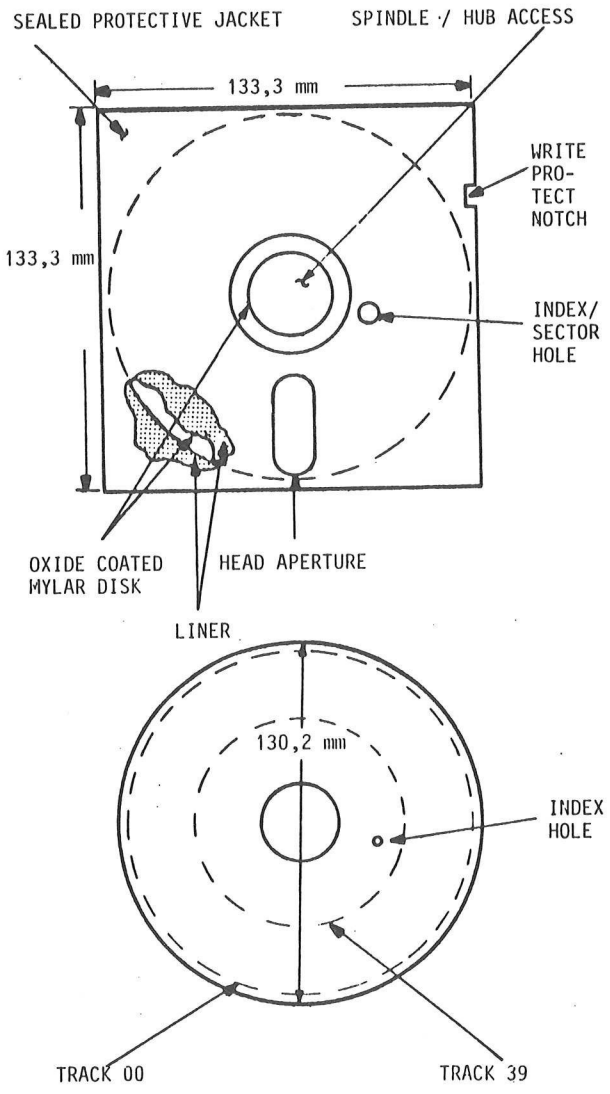


FIGURE 1 - 2 :
FLEXIBLE DISK CONSTRUCTION AND DIMENSIONS

1.7. RECORDING FORMATS

The format of the data recorded on the diskette depends on the host system. There are two encoding schemes used :

- FM - Frequency Modulation
  for single density

- MFM - Modified Frequency Modulation
  for double density

1.7.1. FM-ENCODING

This scheme utilizes clocks to define bit cell times. The presence of a flux reversal between clock pulses is defined as a "one" bit. The absence of a flux reversal between clocks is defined as a "zero" bit.
On the write data and read data interface lines between disk drive and host system, each pulse represents a flux reversal on the diskette.

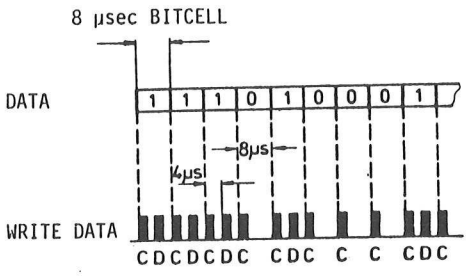


FIGURE 1 - 3 : FM-ENCODING

1.7.2. MFM-ENCODING

A flux transition is always recorded at the center of the bitcell for each "one" data bit. No flux transition is recorded for a "zero" bit, unless it is not followed by another "zero" bit. In this case, the flux transition is provided at the end of the first bit cell.

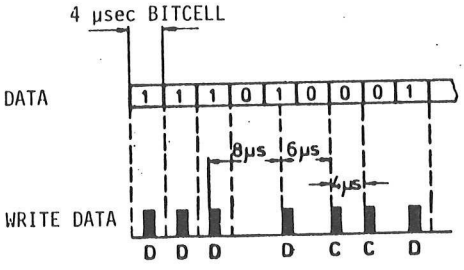


FIGURE 1 - 4 : MFM-ENCODING

1.8. TRACK FORMAT

The tracks of the flexy disk may be formatted in numerous ways, depending on the formatter of the host system used. The BASF mini disk drives write and read hard or soft sectored track formats.

1.8.1. SOFT SECTORED TRACK FORMATS

In a soft sectored track format, the user may record one long record or several smaller records on a track. The most common soft sectored track formats are described in the following chapters.
(The designer should also consider national and international standards for data interchange).

1.8.1.1. SOFT SECTORED TRACK FORMAT FOR SINGLE DENSITY (16 sectors/track à 128 bytes)

This format is shown in figure 1 - 6. It is similar to the IBM-format.
The beginning of a track is indicated by a physical index pulse. Each record is preceded by a unique record identifier. Record identifiers and data fields are separated by gaps. The gaps are necessary to allow updating of a data field without disturbing adjacent fields.

INDEX GAP

This gap starts with the index pulse and is 16 bytes in length. It is not affected by any update write process.

IDENTIFIER GAP

This gap consists of 11 bytes FF and may vary slightly in length after the data field has been updated.

DATA GAP

This gap separates the data field from the following ID-field and is nominally 27 bytes in length. It will vary slightly in length after the data field has been updated.

TRACK GAP

The gap between the last data field and the index pulse is defined as track gap. It varies slightly in length, due to write frequency and disk speed tolerances. It is nominally 101 bytes in length.

ADDRESS MARK (AM)-BYTE

The soft sectored track format needs unique bit patterns to identify the beginning of ID and data fields for synchronizing the deserializer circuit in the host system. The unique bit pattern is called Address Mark (AM). AM-patterns do not contain clock bits in all bit cells (all other data bytes must have clock bits in each bit cell!).

There are three different AM-patterns used :

- ID-AM — in front of an ID-field
- DATA-AM — in front of a data field
- DELETED DATA-AM — in front of a deleted data field

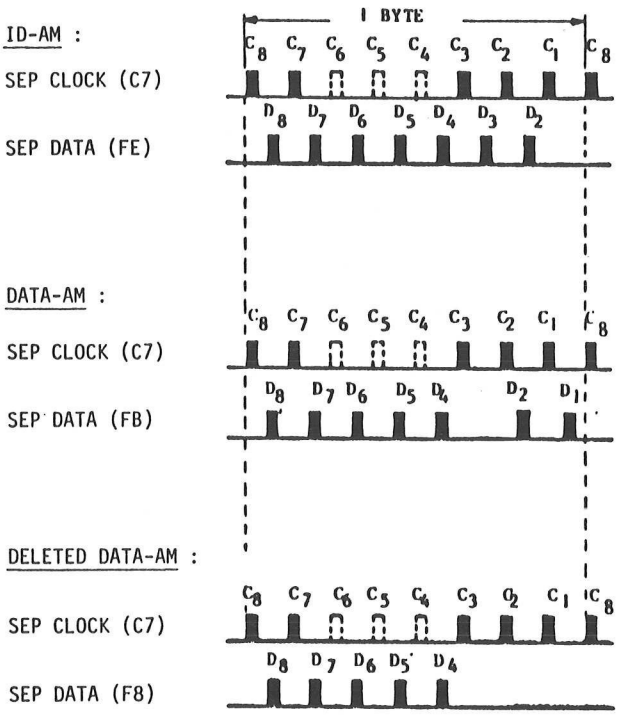


FIGURE 1 - 5 : ADDRESS MARK PATTERNS

SECTOR IDENTIFIER

The sector identifier consists of the identifier mark, the address identifier and the EDC-pattern.

IDENTIFIER MARK

This field comprises 7 bytes (see figure 1 - 6). The 6 bytes of zeros in front of the address mark byte are for synchronisation of the data separator in the host system. The ID-AM-byte contains a data pattern of FE where the clock bits C6, C5 and C4 are missing as explained before.

ADDRESS IDENTIFIER

The address identifier comprises the following 6 bytes :

1. track address (TRK) :

   This byte represents in binary notation the track address from 00 for the outermost track to 39 for the innermost track.

2. side address (SID) :

   Represents in binary notation the side address (00 or 01) of the mini disk.

3. sector address (SEC) :

   Represents in binary notation the sector address from 01 for the 1st sector to 16 for the last sector of a track.

4. sector length (LEN) :

   This byte identifies the length of the data field as follows :

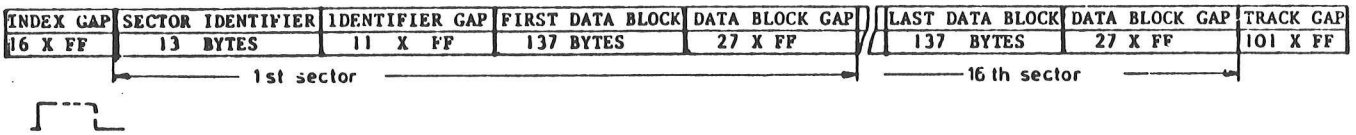
   00 : 128 bytes
   01 : 256 bytes
   02 : 512 bytes
   03 : 1 024 bytes

5. and 6. EDC-bytes (EDC) :

   These two bytes are hardware generated from the host system by shifting serially the bits of the sector identifier starting with the ID-AM and ending with the 4th byte of the sector identifier through a 16-bit shift register described by the generator polynominal :

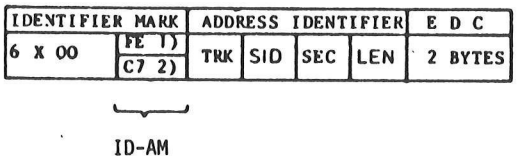
$$x^{16} + x^{12} + x^{5} + 1$$

   (for more details, read chapter EDC-implementation !).

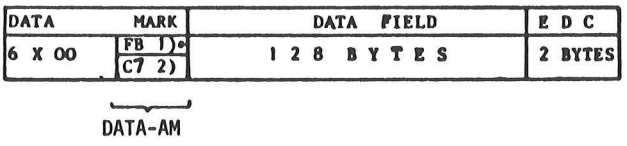


INDEX PULSE

SECTOR IDENTIFIER :



DATA BLOCK :



1) DATA PATTERN

2) CLOCK PATTERN

   DELETED AM : F8

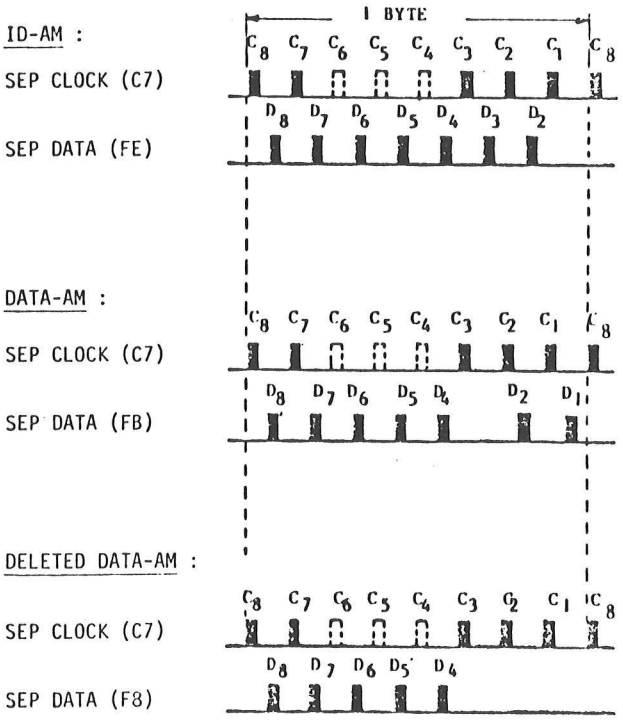


FIGURE 1 - 6 : SOFT SECTORED TRACK FORMAT WITH 16 SECTORS/TRACK FOR SINGLE DENSITY (FM)

DATA BLOCK

The data block contains the data mark, the data field and the EDC-bytes.

DATA MARK

This field comprises 7 bytes (see figure 1 - 6).The 6 bytes of zeros in front of the data address mark are for synchronisation of the data separator circuit in the host system. The data address mark byte contains FB in front of a normal data field. When a deleted data field follows, FB must be written. The clock pattern of the data address mark is C7 (C6,C5 and C4 missing).

DATA FIELD

This field comprises 128 bytes. If it comprises less than 128 bytes, the remaining positions shall be filled with zeros.

EDC-BYTES

These two bytes are hardware generated by the host system by shifting serially the bits of the data block starting with the DATA-AM and ending with the last byte of the data field through a 16-bit shift register described by the following generator polynominal :

$$x^{16} + x^{12} + x^{5} + 1$$

EDC-IMPLEMENTATION

Figure 1 - 7 is a simplified logic of a shift register, which may be used to generate the EDC-bytes.

Prior to the operation, all positions of the shift register are set to ONE. Input data are added (exclusive OR) to the contents of position C_{15} of the register to form a feedback. This feedback in turn is added (exclusive OR) to the contents of position C_4 and position C_{11}.

On shifting, the outputs of the exclusive OR gates are entered into positions C_0, C_5 and C_{12} respectively. After the last data bit was added, the register is shifted once more as specified above.
The register than contains the EDC-bytes. When further shifting is to take place during the writing of the EDC-bytes, the control signal inhibits exclusive OR operations.
To check for errors when reading, the data bits are added into the shift register in exactly the same manner as they were during writing. After the data, the EDC bytes are also entered into the shift register as if they were data. After the final shift,the register contents will be all ZERO if the record does not contain errors.

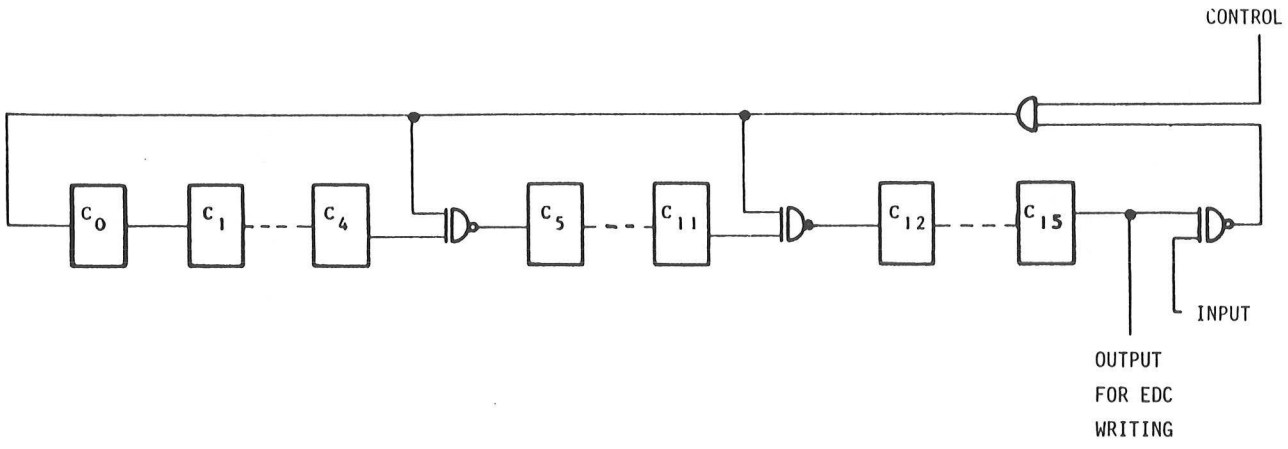


FIGURE 1 - 7 : SIMPLIFIED SHIFT REGISTER

1.8.1.2. SOFT SECTORED TRACK FORMAT FOR
SINGLE DENSITY
(9 SECTORS/TRACK à 256 BYTES)

In this format, which is shown in figure 1 - 8, each sector contains 256 bytes.

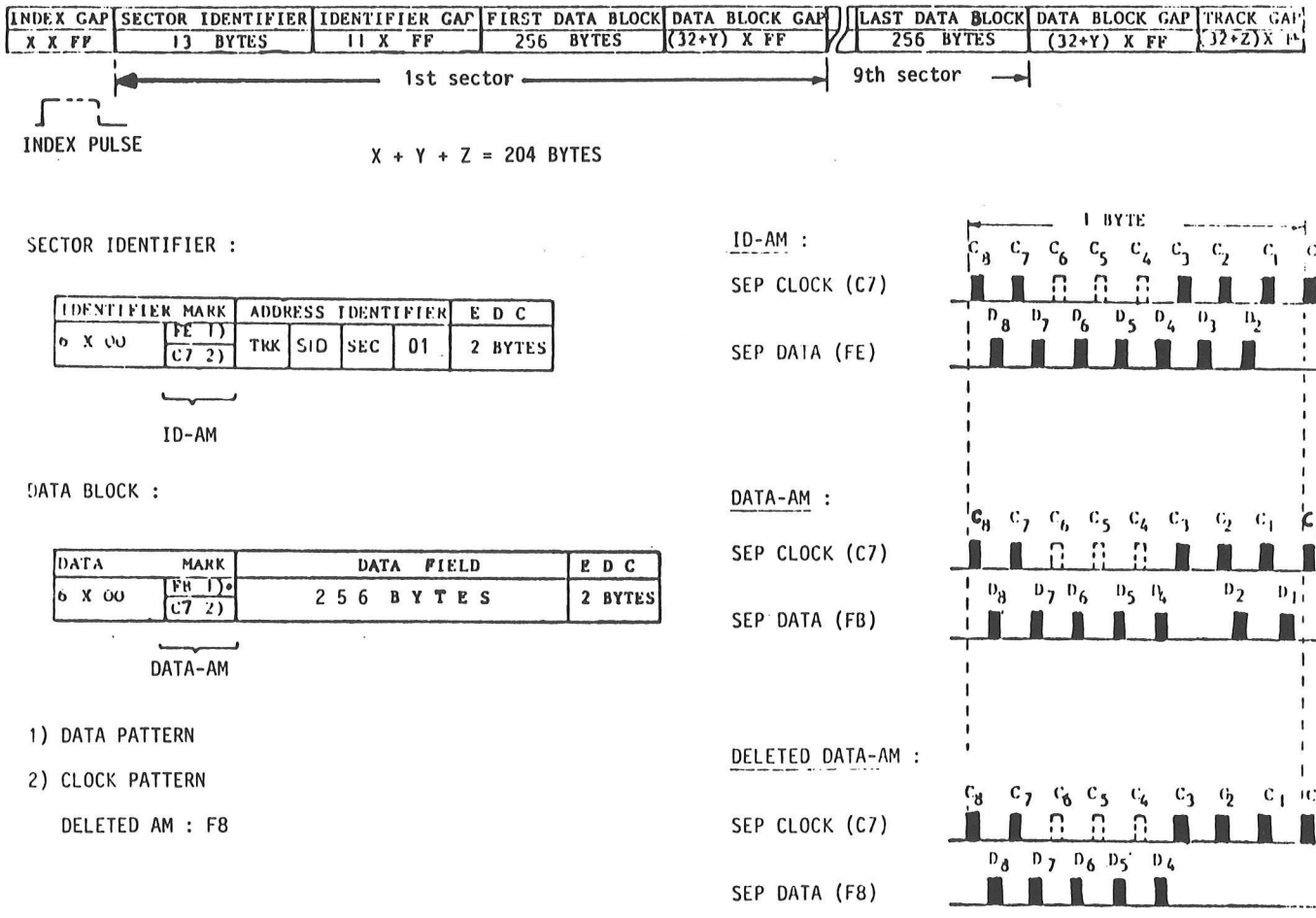
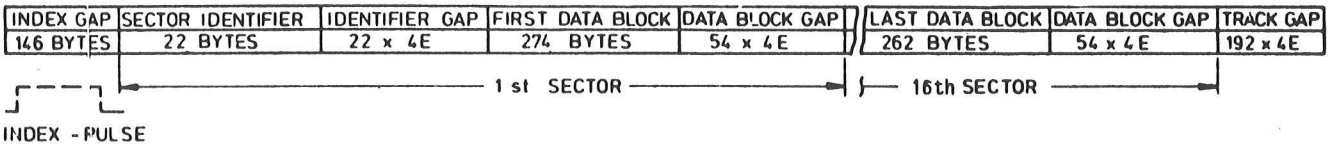


FIGURE 1 - 8 : SOFT SECTORED TRACK FORMAT WITH 9 SECTORS/TRACK

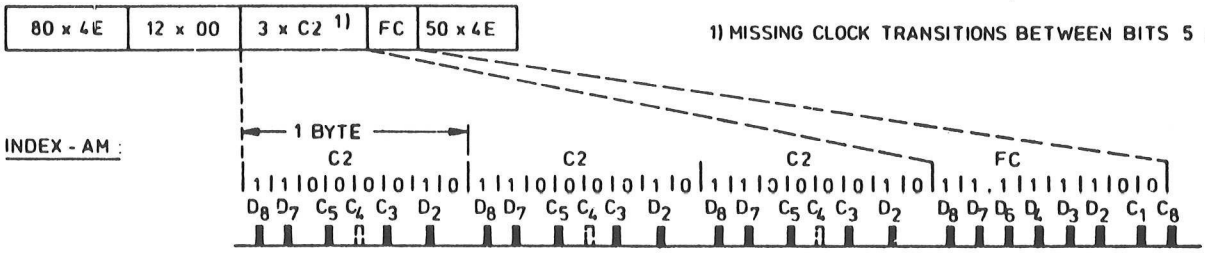
1.8.1.3. SOFT SECTORED FORMAT FOR DOUBLE DENSITY (16 SECTORS à 256 BYTES)

On double sided diskettes for double density, track 0 on side 0 is recorded in FM. For this track, only the previous described track format for single density is valid. All other tracks on the diskette are recorded in MFM. For these tracks, the following track format will be valid (see figure 1 - 9).

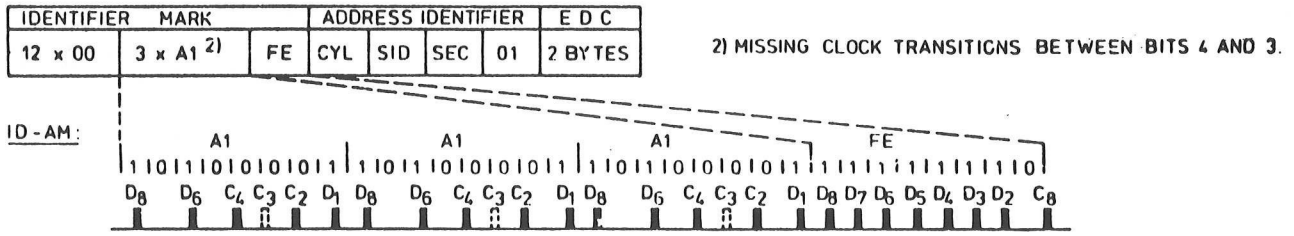
The content of the data blocks is doubled to 256 bytes. In MFM recording, the bit density is also doubled, the sector count will be the same as in single density format (1.8.1.1.). The meaning of the different fields and the generation of the EDC-bytes are the same as in single density recording. Only the address mark pattern is changed as shown in figure 1-9.



INDEX GAP :



SECTOR IDENTIFIER :



DATA BLOCK :

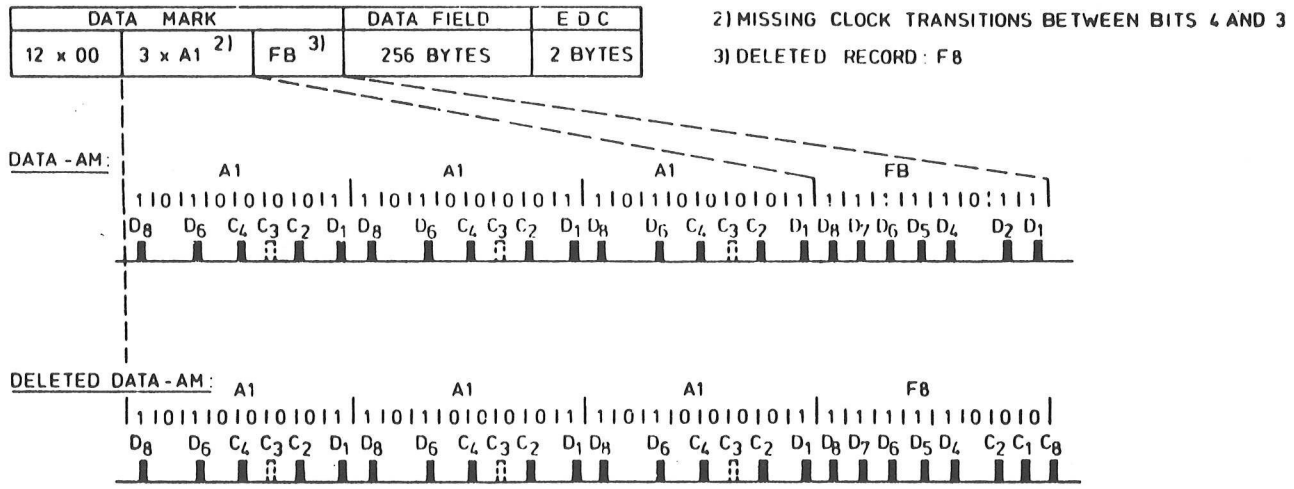


FIGURE 1 - 9 : SOFT SECTORED TRACK FORMAT FOR DOUBLE DENSITY (MFM)

SECTION II.
THEORY OF OPERATION

2.1. GENERAL

This section contains descriptive information on each function of the mini disk drive and detailed theory of operation of mechanism and electronics of the drive.

2.2. FUNCTIONAL DESCRIPTION

The models BASF 6106 and BASF 6108 comprise the following functions :

- drive mechanism
- spindle and front door mechanism
- positioning mechanism
- head load mechanism

2.2.1. DRIVE MECHANISM

The spindle is rotated at 300 rpm by a DC drive motor. Rotation of the spindle is provided by a belt and pulley. The drive motor is started and stopped by the interface signal MOTOR ON.
The ratio between motor and spindle speed is approximately 7:1.

2.2.2. SPINDLE AND FRONT DOOR MECHANISM

The main parts of this mechanism are the drive hub, the centering cone, the centering cone expander and the front door with pressure arm and door latch (see fig. 2 - 1). For loading, a diskette is inserted and the front door pressed. The pressure arm moves down, the centering cone enters the flexy disk. Just before the centering cone reaches the full down position, the centering cone expander is activated and expands the centering cone which grips the inner diameter of the flexy disk to ensure correct alignment. The door latch is activated and holds the front door in a closed position. For unloading a disk, the front door must be pressed again. The door latch opens and the pressure arm is moved upwards by a spring. The centering cone and centering cone expander also move upwards and disengage the mini disk from the drive hub.

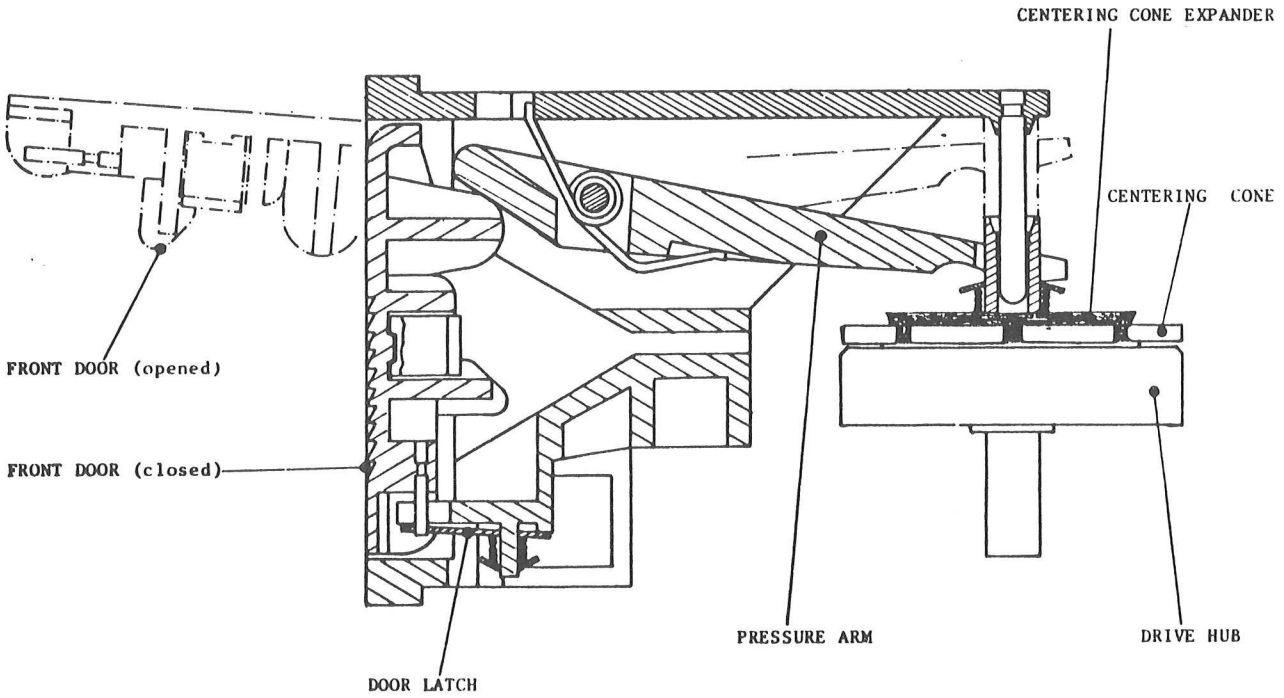


FIGURE 2 - 1 : SPINDLE AND FRONT DOOR MECHANISM

2.2.3. POSITIONING MECHANISM

The main parts of the positioning mechanism are (see fig. 2 - 2 and 2 - 3) :

- stepper motor
- spiral wheel
- carriage assembly

The stepper motor is a four phase motor and is rotated 15° by each step pulse.
The spiral wheel directly connected to the shaft of the stepper motor converts the rotational motion of the stepper motor to a linear motion of the read write head assembly.
The BASF 6106 carriage assembly (see fig.2 - 2) consists of the read/write head, and the head load pressure arm. The read/write head is inserted in the carriage assembly, which rides on two guide bars. The flexy disk is pressed against the read/write head by the head load pressure arm. The head load pressure arm is released by the head load mechanism.
In the BASF 6108 carriage assembly (see fig. 2 - 3), the head load pressure pad is replaced by the upper read/write head.

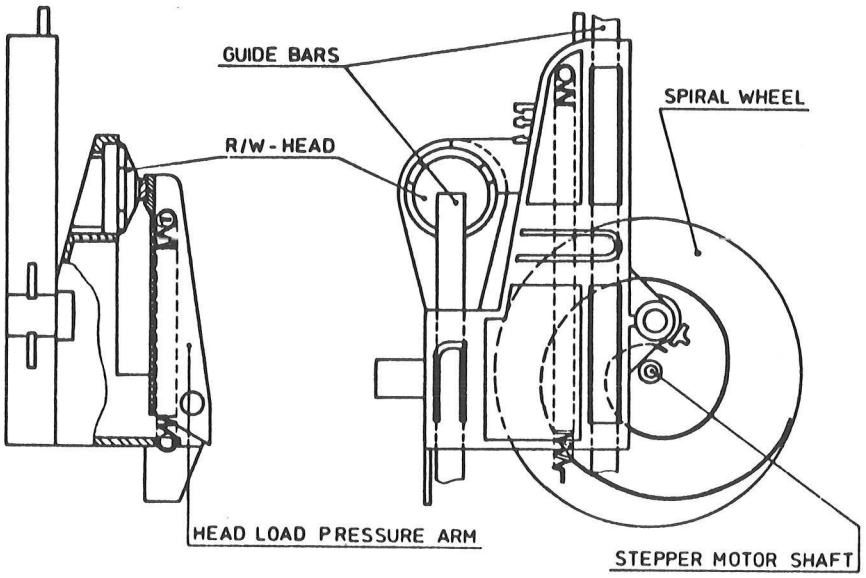


FIGURE 2 - 2 : POSITIONING MECHANISM BASF 6106

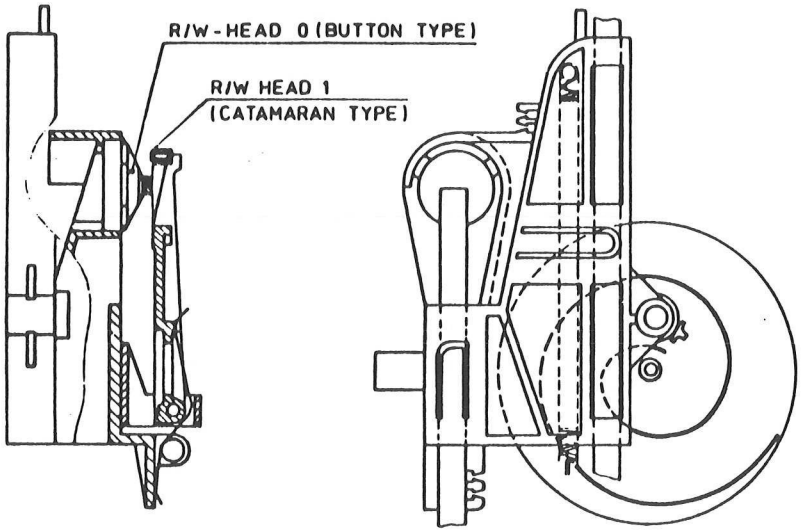


FIGURE 2 - 3 : POSITIONING MECHANISM BASF 6108

2.2.4. HEAD LOAD MECHANISM

The head load mechanism comprises (see fig. 2 - 4 and 2 - 5) :

- head load solenoid
- head load actuator

When the head load solenoid is energized, the head load actuator releases the head load pressure arm of the carriage assembly. On the single sided mini disk drive (BASF 6106), this causes the mini disk to be pressed against the read/write head by the head load pad.

On the double sided mini disk drive (BASF 6108), the flexy disk is pressed against the bottom head (HEAD 0) by the upper head (HEAD 1) mounted in the pressure arm. The pressure foam on the head load actuator stabilizes the flexy disk. When the head load solenoid is deenergized, the head load actuator is lifted by a sping. The head load pressure arm is lifted also.

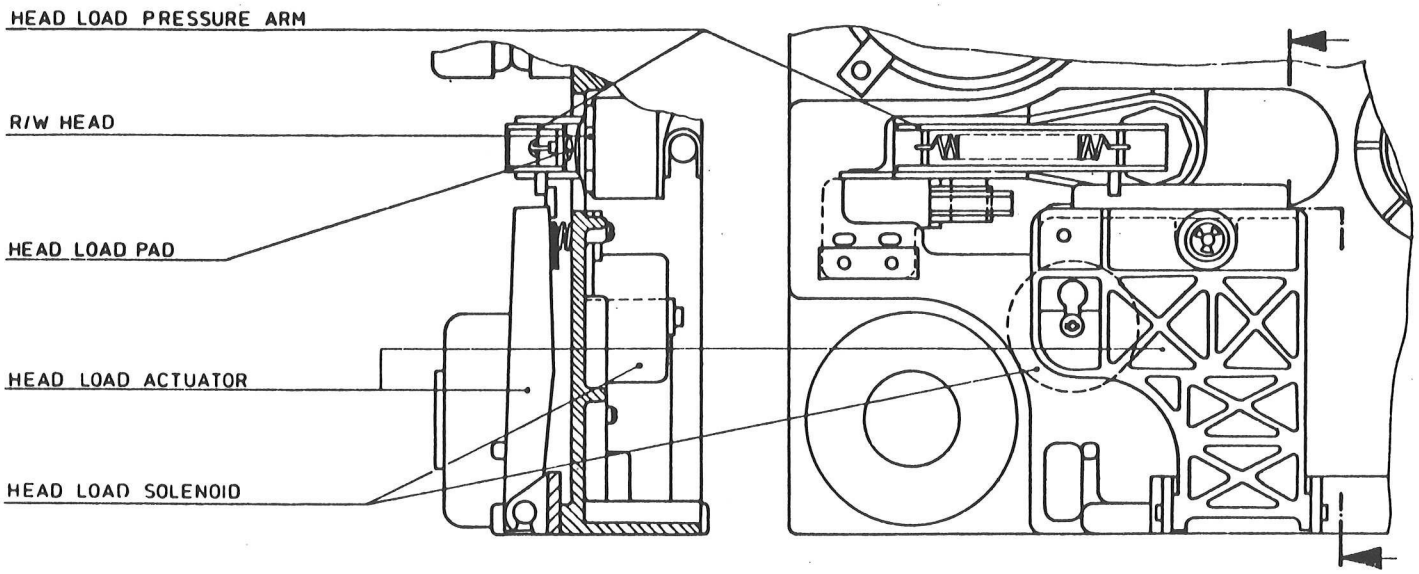


FIGURE 2 - 4 : HEAD LOAD MECHANISM BASF 6106

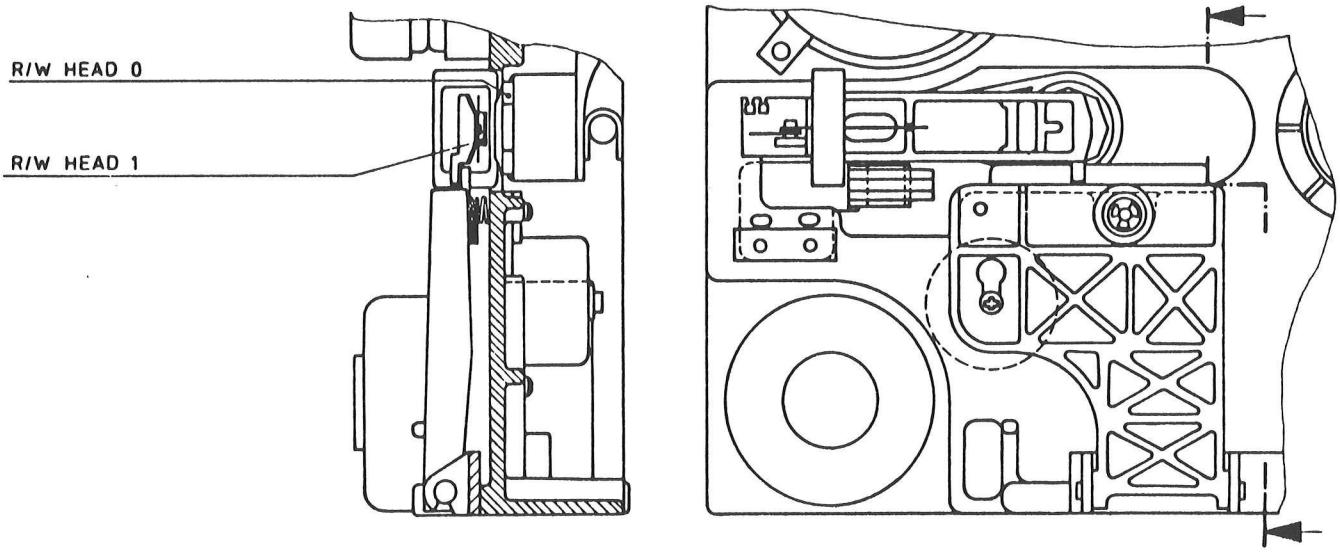


FIGURE 2 - 5 : HEAD LOAD MECHANISM BASF 6108

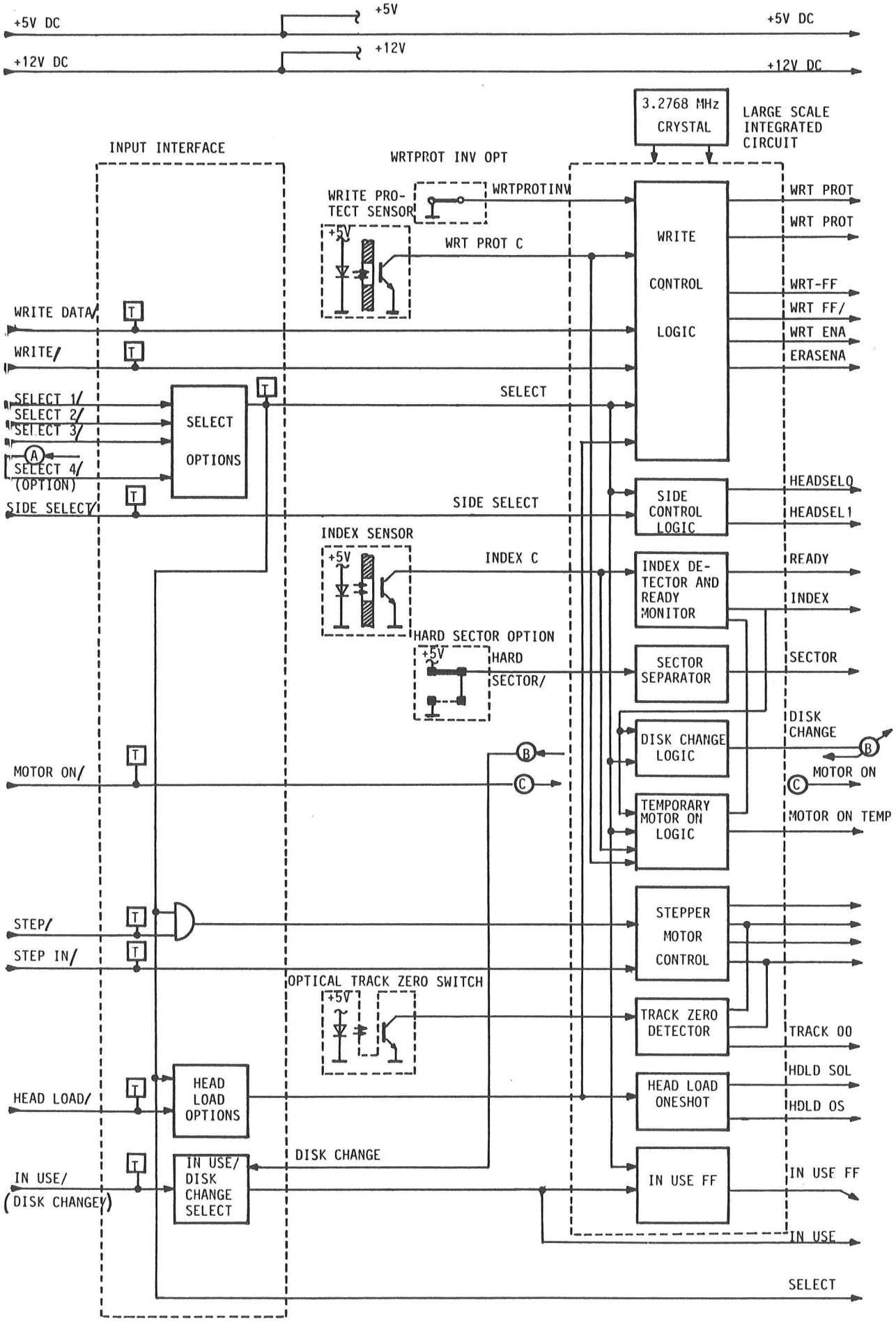


FIGURE 2 - 6 : BLOCK DIAGRAM

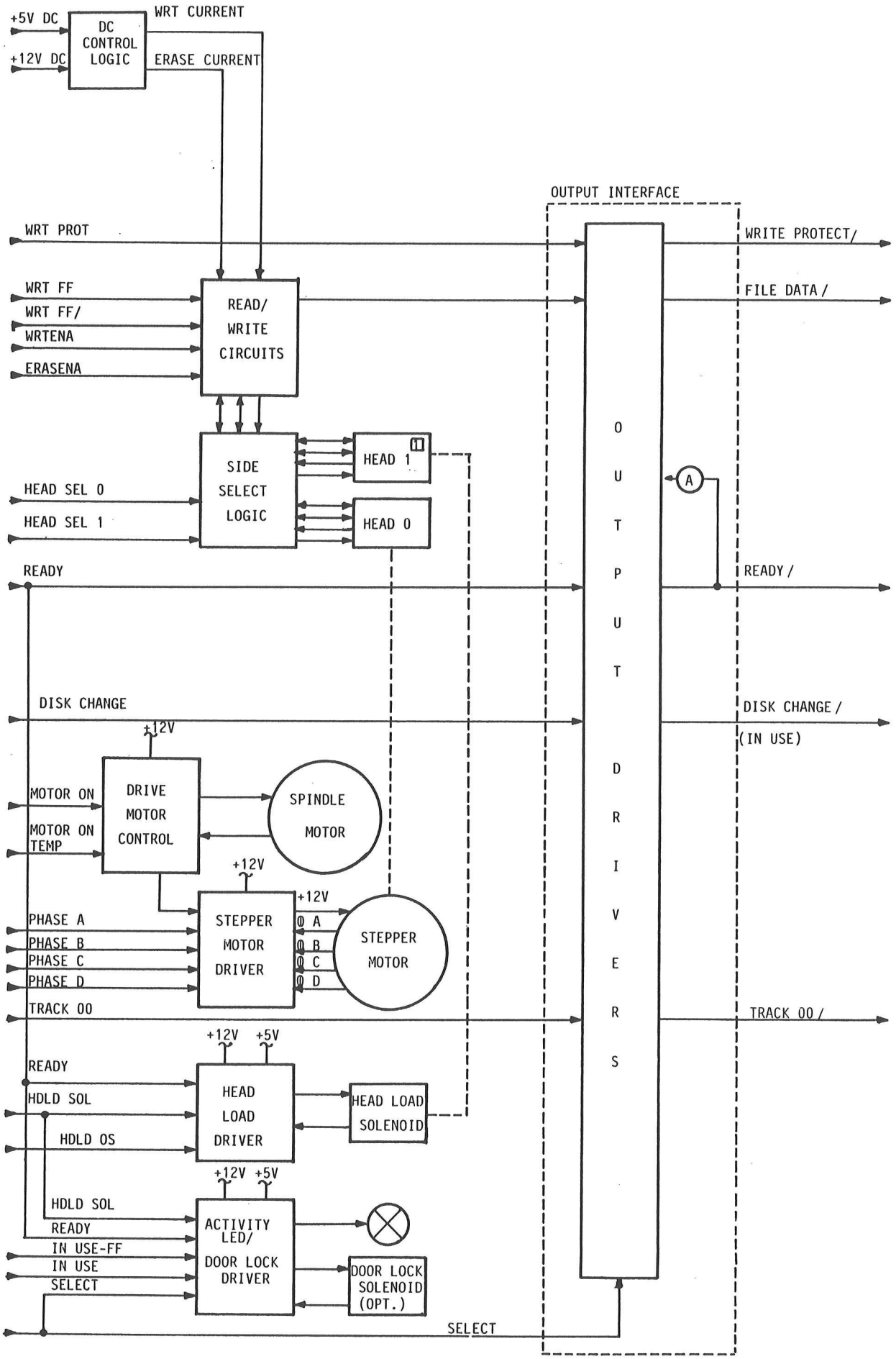


FIGURE 2 - 6 : BLOCK DIAGRAM

2.3. DRIVE ELECTRONIC DESCRIPTION

2.3.1. BLOCK DIAGRAM

Figure 2 - 6 is a block diagram of the drive control logic. The logic is divided into the following parts:

- input interface
- write control logic [1)]
- side control logic [1)]
- index detector and ready monitor [1)]
- sector separator [1)]
- disk change logic [1)]
- disk motor on logic [1)]
- stepper motor control [1)]
- track zero detector [1)]
- in use logic [1)]
- DC-control logic
- read/write circuits
- side select logic
- drive motor control
- stepper motor driver
- head load driver
- activity LED/door lock driver
- output interface

[1)] All these circuits are included in the BASF LSI-chip 81041

2.3.2. LARGE SCALE INTEGRATED CIRCUIT BASF 81041-001

The BASF FDD/MDD-LSI is a 40 pin NMOS large scale integrated circuit, designed for controlling of 8" and 5 1/4" floppy disk drives. The use of this circuit simplifies the electronic board and increases the reliability of the electronics.
The chip is programmed by 2 type select pins on the PCB for the different drives to be used.
The 3.2768 MHz crystal is used by the LSI-chip for generating the different time delay circuits (one shots) inside the chip. Other inputs (WRTPROTINV, AUTO ERASE, HARD SECTOR) are used to enable or disable the different options included in the LSI-chip.
Figure 2 - 7 shows the pin assignements of the LSI-chip.

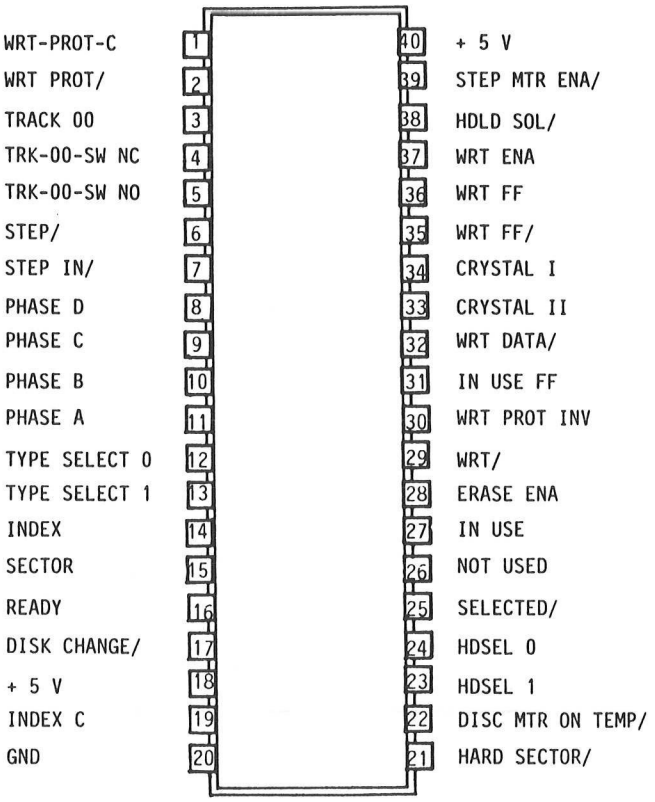
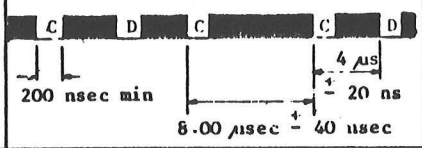


FIGURE 2 - 7 : PIN ASSIGNMENTS BASF LSI-CHIP 81041-001

2.3.3. INPUT INTERFACE

2.3.3.1. INPUT SIGNALS DEFINITIONS AND TERMINATION

The input interface receives the signals from the host system. Table 2 - 1 lists and defines the input signals.
The input lines are terminated by pull up resistors of 150 ohm. In a serial configuration only the last drive will contain the pull up resistor network.
The receivers send the input signals to the different parts of the drive electronics.

SIGNAL NAME	DEFINITION
SELECT (1-3,4[1])	Selects the desired mini disk drive. Enables all other interface lines except MOTOR ON, WRITE DATA, SIDE SELECT and DIRECTION IN.
WRITE DATA/	This line carries low active pulses representing data to be recorded on the mini disk. 
WRITE GATE/	Low input enables recording of WRITE DATA on disk. High input enables reading from the Flexy Disk.
MOTOR ON/	This line turns on the drive motor and the stepper motor and is not gated by SELECT. A recalibrate operation must be performed to obtain correct head positioning every time after the MOTOR ON signal goes active. Switching of the stepper motor may be disabled by removing a jumper. This avoids recalibrating after switching on the drive motor.
DIRECTION IN/	Defines motion of the read/write head LOW = in (towards Track 39) HIGH = out (towards Track 0) This line is not gated by SELECT.
STEP/	Used in conjunction with DIRECTION IN and causes the read/write head to be moved from track to track.
HEAD LOAD/	This line is used to press the mini disk against the read/write head if the mini disk drive is ready. To activate this line a jumper has to be changed.
IN USE/	This line controls the door lock solenoid. Also the activity LED can be switched on. If the IN USE/ signal is used, the disk change option must be disabled.
SIDE SELECT/	This line defines whether head 0 or head 1 of the mini disk drive is used. A high signal selects head 0, a low signal selects head 1. This line is not gated by SELECT. On BASF 6106 head 1 is not installed.

1) If SELECT4/ is used, the READY OUTPUT SIGNAL is not available

TABLE 2 - 1 : INPUT SIGNALS

2.3.3.2. SELECT OPTIONS

There are two possiblities to select the mini disk drive :

- auto select
- radial select

AUTO SELECT

This option is used when no SELECT lines are used. The input and output interfaces are always enabled, because SELECT is forced to a high. To install the AUTO SELECT option 2D(3-4) must be jumpered (see fig. 2 - 8).

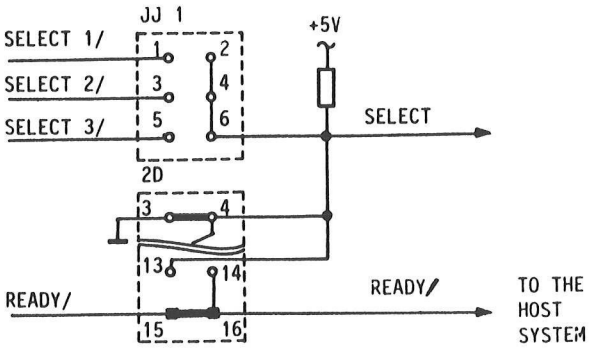


FIGURE 2 - 8 : AUTO SELECT OPTION

RADIAL SELECT

If radial select is normally, 3 mini disk drives can be connected to the host system.
The signal SELECT 1/ will select the mini disk drive jumpered between JJ1 1 - 2, SELECT 2/ will select the mini disk drive jumpered between JJ1 3 - 4 and SELECT 3/ will select the mini disk drive jumpered between JJ1 5 - 6. There is a possibility to select a fourth drive, if the READY-signal is not used. 2D(15-16) must be scratched and a jumper from 2D (13-14) installed. Only one select jumper is allowed in one drive. For enabling of the radial select option JJ2 5 - 6 must be jumpered and the auto select option must be disabled by removing jumper 2D (3-4).

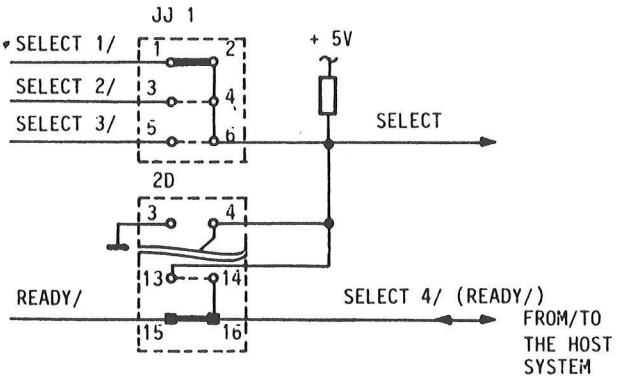


FIGURE 2 - 9 : RADIAL SELECT OPTION

2.3.3.3. HEAD LOAD OPTIONS

There are three possiblilities for the user to load the head :

- auto head load
- selected head load
- radial head load

AUTO HEAD LOAD

This option allows to load the read/write headas soon as the mini disk drive is selected.
If auto head load is desired, the jumpers must be set as shown in fig. 2 - 10.

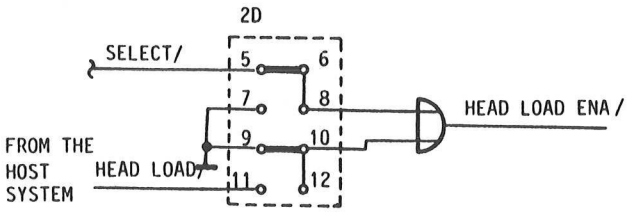


FIGURE 2 - 10 : AUTO HEAD LOAD OPTION

SELECTED HEAD LOAD OPTION

In this configuration, the head is loaded when the mini disk drive is selected and the HEAD LOAD signal is activated (see fig. 2 - 11).

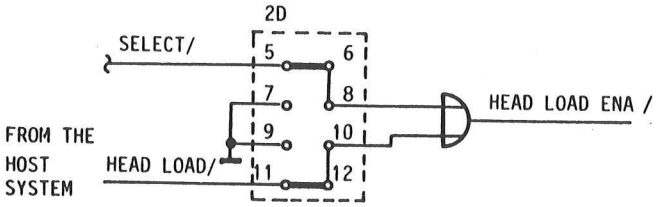


FIGURE 2 - 11 : SELECTED HEAD LOAD OPTION

RADIAL HEAD LOAD OPTION

This option allows the user to keep the head loaded without selection of the mini disk drive. The 48 msec head load time is then eliminated. To install this option, see fig. 2 - 12.

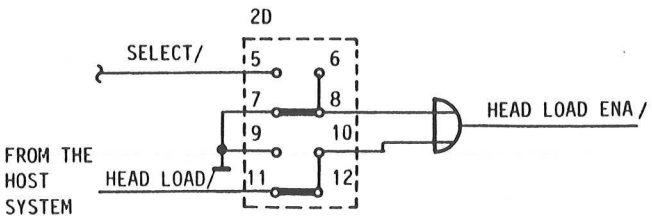


FIGURE 2 - 12 : RADIAL HEAD LOAD OPTION

2.3.4. OUTPUT INTERFACE

The output interface sends the read data pulses and the status signals WRITE PROTECT, INDEX, READY, TRACK 00 and DISK CHANGE (optional) to the host system (see table 2 - 2).
The output signals are gated by I/O-ENABLE and driven by the output drivers SN 7438.

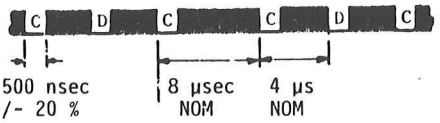
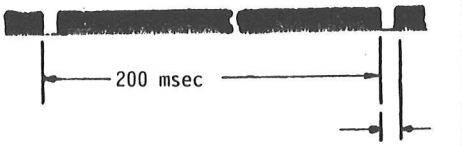
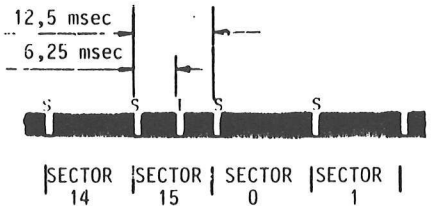
SIGNAL NAME	DEFINITION
READ DATA/	This line provides the "raw data" as detected by the read electronics. 
WRITE PROTECT	Low active status indicates that a write protected Flexy Disk is installed. The BASF 6106/08 will inhibit writing with a write protected Flexy Disk installed.
INDEX/	The leading edge of this signal indicates the beginning of a track when soft sector format is used.  If a hard sectored disk is used this signal indicates the sensing of an index or sector hole. To indicate the beginning of a track one index pulse is sensed in the middle of sector 15. 
TRACK 00/	This line indicates that the read/write head is positioned at track 00.
READY/	This line indicates that the inserted Flexy Disk has reached more than 60 % of full operation speed and three consecutive INDEX pulses have been sensed. For hard sectored Flexy Disks READY is activated as soon as the Flexy Disk starts turning and three consecutive SECTOR pulses have been sensed.
DISK CHANGE/ (OPTION)	An active (low) signal is provided when the SELECT line is activated if the drive while deselected has gone from a Ready to a Not Ready condition.

TABLE 2 - 2 : OUTPUT SIGNALS

2.3.5. STEPPER MOTOR LOGIC

The stepper motor is a four-phase DC-motor and is controlled by the stepper motor logic. The stepper motor logic comprises the stepper motor control logic, located in the LSI-chip and the stepper motor driver. The stepper motor control consists of a divide by four up/down synchron counters with control circuits. Each STEP pulse from the host system rotates the stepper motor for one step. Each step corresponds to a rotation angle of 15°. The rotation of the stepper motor is converted to a linear motion of the R/W-head(s) by the spiral wheel. The direction of the motion of the R/W-head(s) depends on the input signal DIRECTION IN/. If this signal is active (low), the R/W-head(s) will be moved towards track 39 (in). The R/W-head(s) move out by each STEP pulse, when DIRECTION IN/ is in a high state. Multiple track positioning is attained by the host system issuing a series of STEP pulses at 12msec intervals. Table 2 - 3 shows the output signals for "in" and "out" motion of the R/W-head(s). The DIRECTION IN-signal must be at the desired level 1 µsec before the trailing edge of the STEP pulse. Stepping is initiated by the trailing edge of the STEP pulse. The time between two consecutive STEP pulses must be 12 msec minimum (see fig. 2 - 13). As long as WRITE GATE is active during a write operation, the STEP pulse interface line is inhibited.

In figure 2 - 14, a Zener diode is used in addition to four free wheeling diodes. This undamps the magnetic response at switch off time, causes armature to oscillate across target position. This reduces the influence of friction upon target positioning, decreases hysteresis error, resulting in precise settling on target position.

STEPPER MOTOR SWITCHING OPTION

The stepper motor can be switched on and off by the MOTOR ON signal, if there is a jumper installed between 5D (1-2). If this jumper is installed, the power consumption of the drive is reduced, but the stepper motor must be repositioned by a recalibrate operation each time the drive motor is turned on. This option is recommended for battery operated systems.

I N						O U T					
STEP	PHASE	A/	B/	C/	D/	STEP	PHASE	A/	B/	C/	D/
-		L	H	L	H	-		L	H	L	H
1		H	L	L	H	1		L	H	H	L
2		H	L	H	L	2		H	L	H	L
3		L	H	H	L	3		H	L	L	H
4		L	H	L	H	4		L	H	L	H

TABLE 2 - 3 : SEQUENCE OF THE STEPPER MOTOR SIGNALS

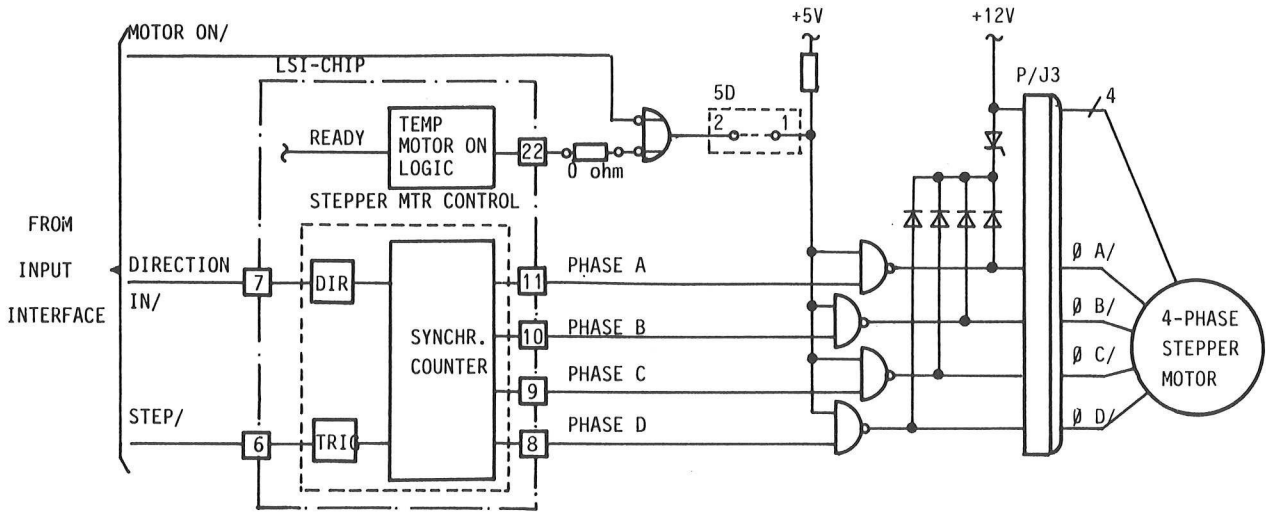


FIGURE 2 - 13 : STEPPER MOTOR LOGIC

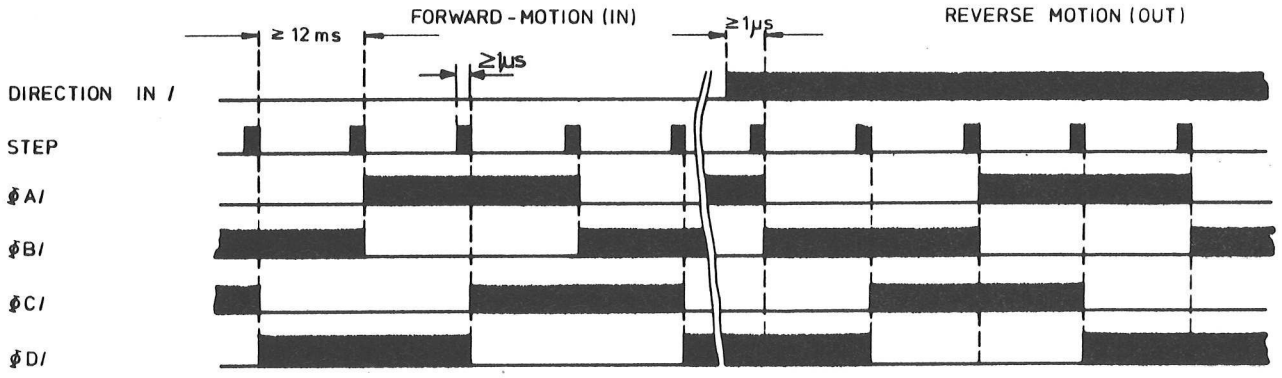


FIGURE 2 - 14 : STEPPER MOTOR - TIMING DIAGRAM

2.3.6. DRIVE MOTOR LOGIC

The drive motor used in the BASF 6106/08 is a DC-motor. Start and stop of the motor are controlled by the MOTOR ON-signal of the host system and the temporary motor on control logic in the LSI-chip.

2.3.6.1. TEMPORARY MOTOR ON LOGIC (fig. 2-15)

This logic is used to turn on the drive motor as soon as a diskette is inserted in the disk drive, even if the MOTOR ON-signal is not activated. The centering of the diskette will be improved during closing the front door by the turning spindle. As soon as the diskette passes the write protect sensor, the 10msec OS and in sequence, the 20sec OS are fired and the WRTPROT LTH is set (see timing diagram 2 - 16).
When the diskette passes the index sensor, the INDEX-FF is set and MTR ON TEMP/-signal is activated. The motor starts turning. As soon as the door is closed, the disk turns, READY will be generated by the ready monitor, which resets the INDEX FF and the WRTPRTLTH. The motor stops. If the door will not be closed after insertion of the diskette, the motor is stopped after the 20sec OS times out.

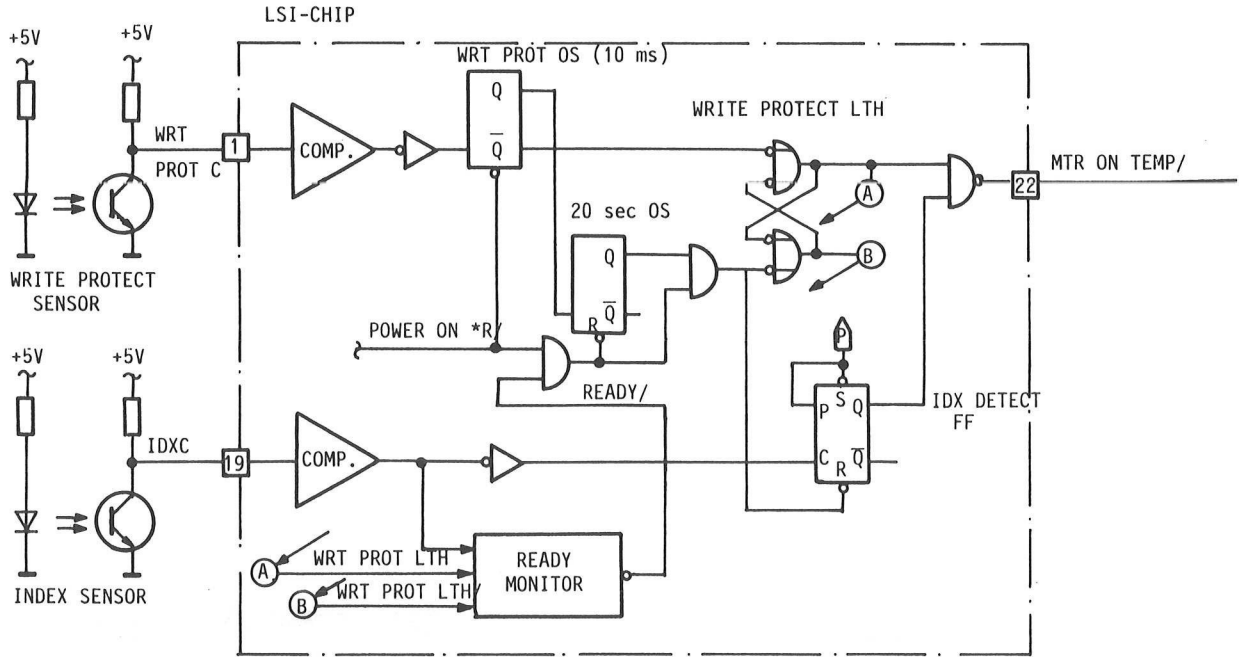


FIGURE 2 - 15 : TEMPORARY MOTOR ON LOGIC

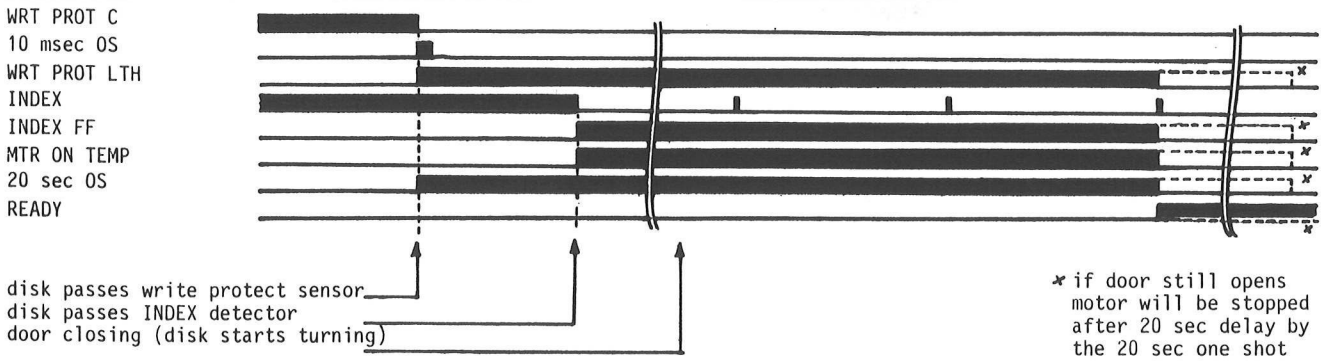


FIGURE 2 - 16 : TIMING DIAGRAM TEMPORARY MOTOR ON LOGIC

2.3.6.2. DRIVE MOTOR CONTROL (FIG. 2 - 17)

The speed of the drive motor is controlled by the integrated circuit ESM 227. It holds the EMF of the drive DC-motor to a constant value. Because the speed of the drive motor is porportional to its EMF, the speed will be also constant. With the potentiometer R47, the drive motor must be adjusted to a disk speed of 300 RPM. The output voltage of the ESM 227 is controlled by the MOTOR ON-signal at pin 12 of the chip.

If MOTOR ON is inactive (low), T1 will be closed and holds T2 open. The drive motor stops. An active MOTOR ON-signal opens T1 and T2 is enabled. The drive motor is running and regulated, so that the flexy disk is rotating at 300 RPM. T10 limits the drive motor start current to 0.7 A.
After the drive motor is started, a delay of 0.5 sec is needed to allow proper motor speed, before reading or writing.

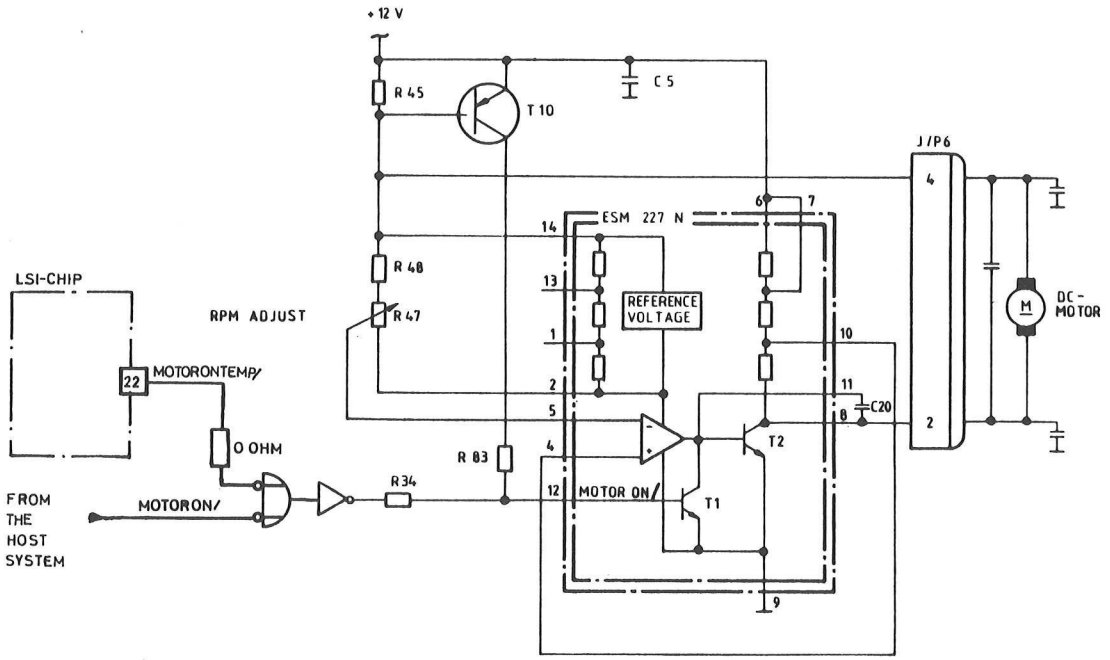


FIGURE 2 - 17 : DRIVE MOTOR CONTROL

2.3.7. HEAD LOAD LOGIC (FIG. 2 - 18)

The head load mechanism is activated by the head load solenoid, which is energized when HEADLOADENA is active and the mini disk drive is ready. READY is activated by the ready monitor in the LSI-chip. As the head load solenoid is activated, TA is closed for 20 ms by the HEAD LOAD ONE SHOT and applies +12V to the head load solenoid to supply sufficient starting current (see fig. 2 - 19). When the HEAD LOAD OS times out, transistor TA turns off, but transistor TB still remains on. +5V is now applied to the head load solenoid by the resistor R and the forward biased DIODE D. The head load solenoid remains activated by decreased power dissipation. DI supresses the spikes on power down.

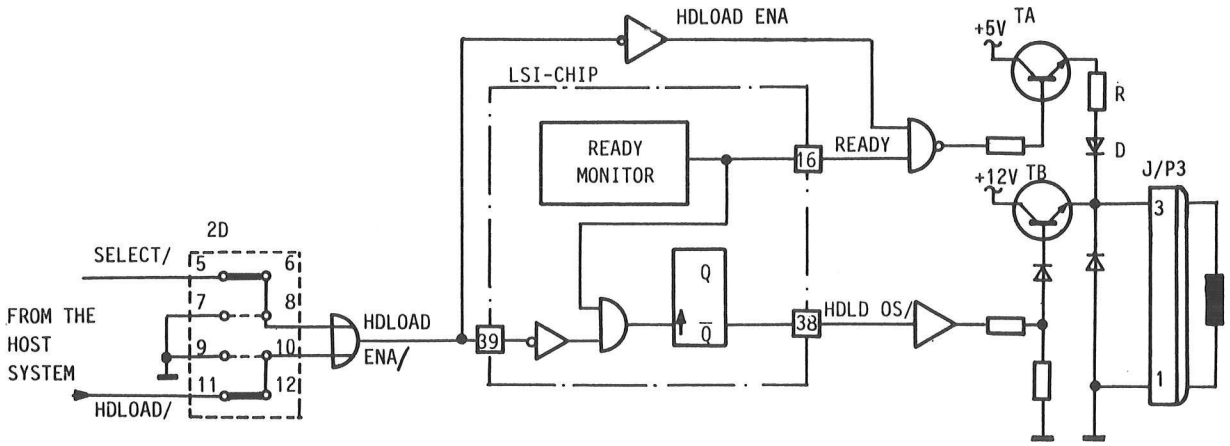


FIGURE 2 - 18 : HEAD LOAD LOGIC

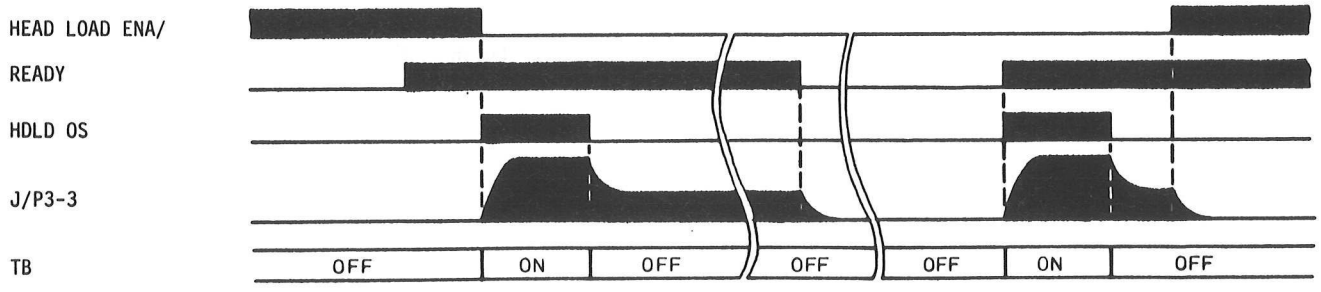


FIGURE 2 - 19 : HEAD LOAD TIMING DIAGRAM

2.3.8. ACTIVITY LED / DOOR LOCK LOGIC

This logic contains the driver, the jumper options and the door lock latch inside of the LSI-chip. Fig. 2 - 20 shows a circuit diagram of the complete logic.

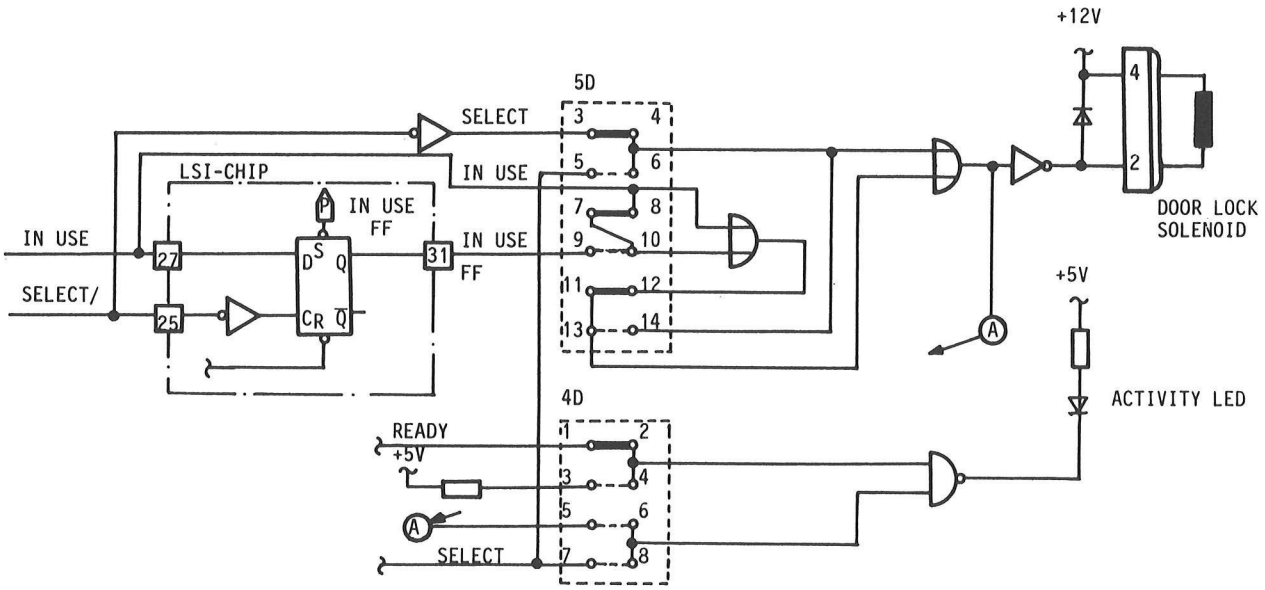


FIGURE 2 - 20 : ACTIVITY LED / DOOR LOCK LOGIC

2.3.8.1. DOOR LOCK LATCH OPTION

This option can be used by the host system, if the IN USE-signal is available. The door latch option allows the latching of the door lock solenoid under control of the SELECT and IN USE-signals, without maintaining the drive selected and without activating of the IN USE-signal. The IN USE-FF stores the state of the IN USE-signal with the selection of the drive (see timing diagram fig. 2 - 21). The door lock solenoid remains activated even if the mini disk drive is deselected and the IN USE-signal is deactivated. For unlocking of the door, the mini disk drive must be reselected with the IN USE-signal inactive. To enable the door lock latch option jumpers from 5D (9-10) and 5D (11-12) must be inserted.

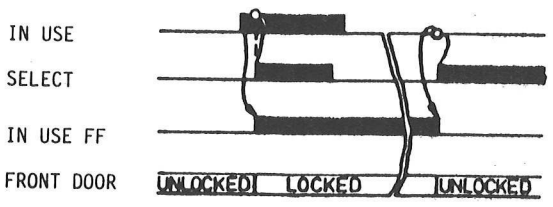


FIGURE 2 - 21 :
TIMING DIAGRAM DOOR LOCK LATCH OPTION

2.3.8.2. DOOR LOCK OPTIONS

There are a lot of possibilities to lock the front door :

1. - locking by the IN USE-signal
   jumpers : 5D (11-12 ; 7-8 ; 13-14)

2. - locking by the door lock latch option
   jumpers : 5D (9-11 ; 13-14)

3. - locking while the drive is selected
   jumpers : 5D (3-4 ; 13-14)

4. - locking while the heads are loaded
   jumpers : 5D (5-6 ; 13-14)

5. - if 1. or 2. is true (IN USE + IN USE FF)
   jumpers : 5D (9-10 ; 11-12 ; 13-14)

6. - if 1. or 3. is true (IN USE + SELECT)
   jumpers : 5D (3-4 ; 7-8 ; 11-12)

7. - if 1. or 4. is true (IN USE + HEAD LOAD)
   jumpers : 5D (5-6 ; 7-8 ; 11-12)

8. - if 2. or 3. is true (IN USE FF + SELECT)
   jumpers : 5D (3-4 ; 9-11)

9. - if 2. or 4. is true (IN USE FF + HEAD LOAD)
   jumpers : 5D (5-6 ; 9-11)

10. - if 1. or 2. or 3. is true (IN USE + IN USE FF + SELECT)
    jumpers : 5D (3-4 ; 9-10 ; 11-12)

11. - if 1. or 2. or 4. is true (IN USE + IN USE FF + HEAD LOAD)
    jumpers : 5D (5-6 ; 9-10 ; 11-12)

2.3.8.3. ACTIVITY INDICATOR OPTIONS

For illuminating of the activity indicator, the following conditions are possible :

1. illuminated while ready and head is located (READY.HEAD LOAD)
   jumpers : 4D (1-2 ; 7-8)

2. illuminated while ready and door is locked (READY.DOOR LOCKEN A)
   jumpers : 4D (1-2 ; 5-6)
   (for jumpering of the door lock, see 2.3.8.2.)

3. illuminated when the head is loaded (HEAD LOAD)
   jumpers : 4D (3-4 ; 7-8)

4. illuminated when the door is locked
   jumpers : 4D (3-4 ; 5-6)

2.3.9. TRACK ZERO DETECTOR

This logic generates the TRACK 00-signal when the read/write head is positioned at track zero.The host system uses this signal to recalibrate the positioning system. When the position of the read/write head is unknown, the host system sends step out pulses until TRACK 00/ goes low.

The track zero detector is comprised of the track zero switch, a comparator, a debounce circuit and a phase detector circuit, which detects the correct phase of the stepper motor. The track zero switch mounted on the deck assembly is activated by the head carriage. The logic circuit supports mechanical and optical track zero switches (see fig.2-22).

When the head carriage moves out, the track zero switch must be open before the read/write head reaches track four. When the head carriage moves towards the track zero position, the track zero switch must close after track four and before track zero. The TRACK ZERO-signal will be active when the track zero switch is closed and phase A and phase C of the stepper motor are activated. SELECT must be high.

Fig. 2 - 23 shows the timing diagram when the host system attempts to step the head carriage beyond track zero. The mechanical stop on the spiral wheel prevents the read/write head from moving out further and holds it near track zero. But the TRACK 00-signal will be deactivated, because the stepper motor is in a wrong phase (Ø B/, Ø C/). If the host system sends three more step out pulses, the phasing of the stepper motor is correct again, the TRACK 00-signal is activated and the read/write head is positioned at track zero.

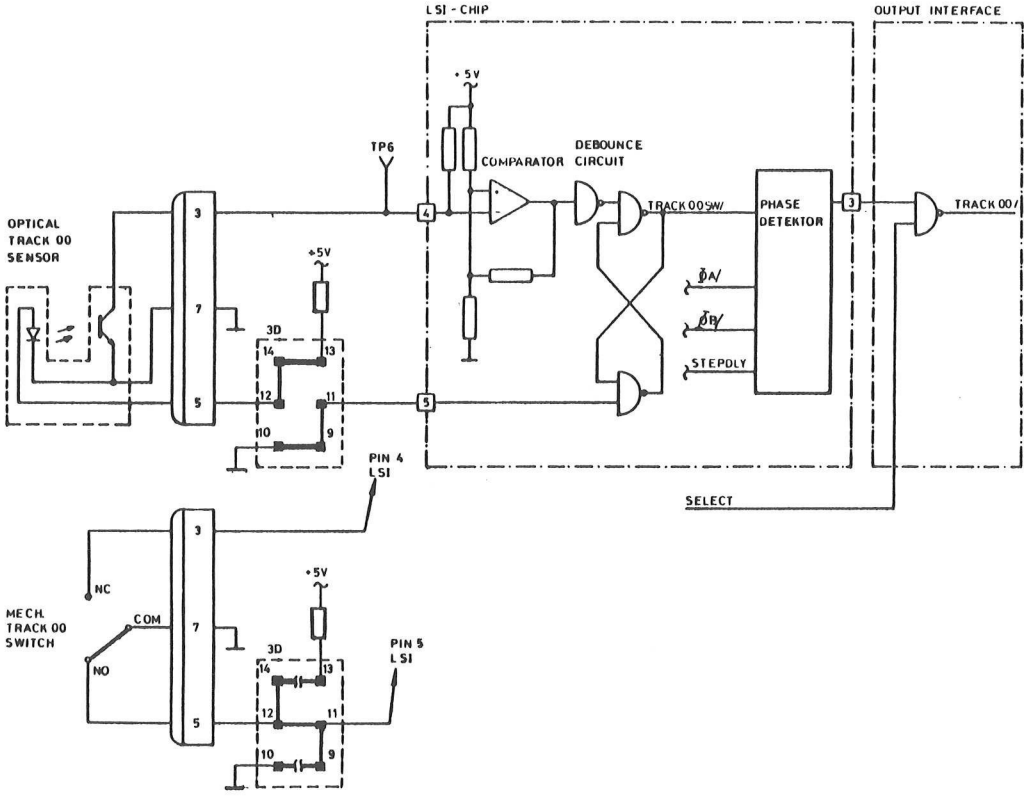


FIGURE 2 - 22 : TRACK ZERO DETECTOR

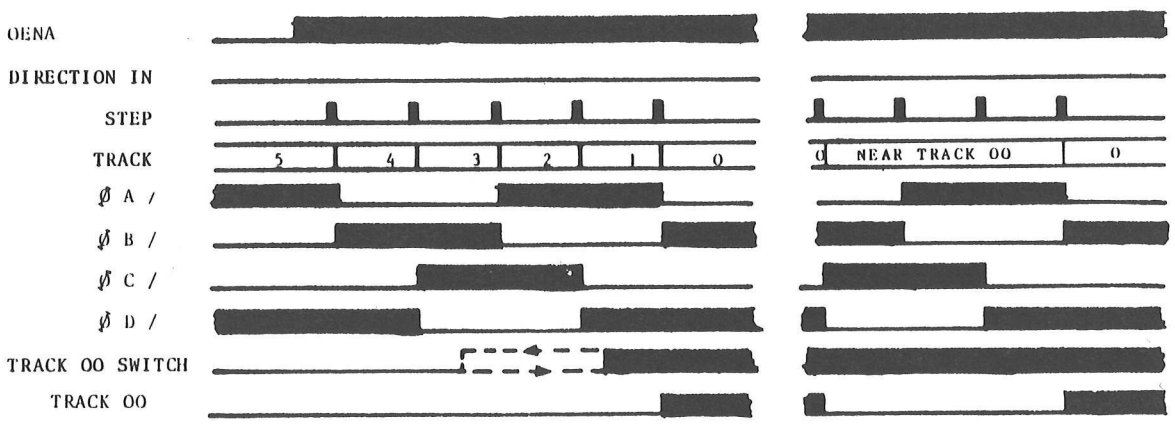


FIGURE 2 - 23 : TRACK ZERO - TIMING DIAGRAM

2.3.10. INDEX DETECTOR, SECTOR SEPARATOR AND READY MONITOR

2.3.10.1. INDEX DETECTOR

The index/sector detector comprises a phototransistor mounted on the deck assembly, a light emitting diode (LED) on the PCB and a comparator inside the LSI (see fig. 2 - 24). As the index hole or sector (optional) hole passes between LED and photo transistor , light from the LED is passed to the phototransistor. This results in a negative pulse of about 4 msec at the inverting input of the comparator.

The output pulse of the comparator is sent as INDEX signal to the host system when HARD SECTOR/ is high. If HARD SECTOR/ is low, the comparator output INDEX/ SECTOR is separated into SECTOR- and INDEX-pulses by the sector separator option. In this case, hard sectored diskettes must be used.

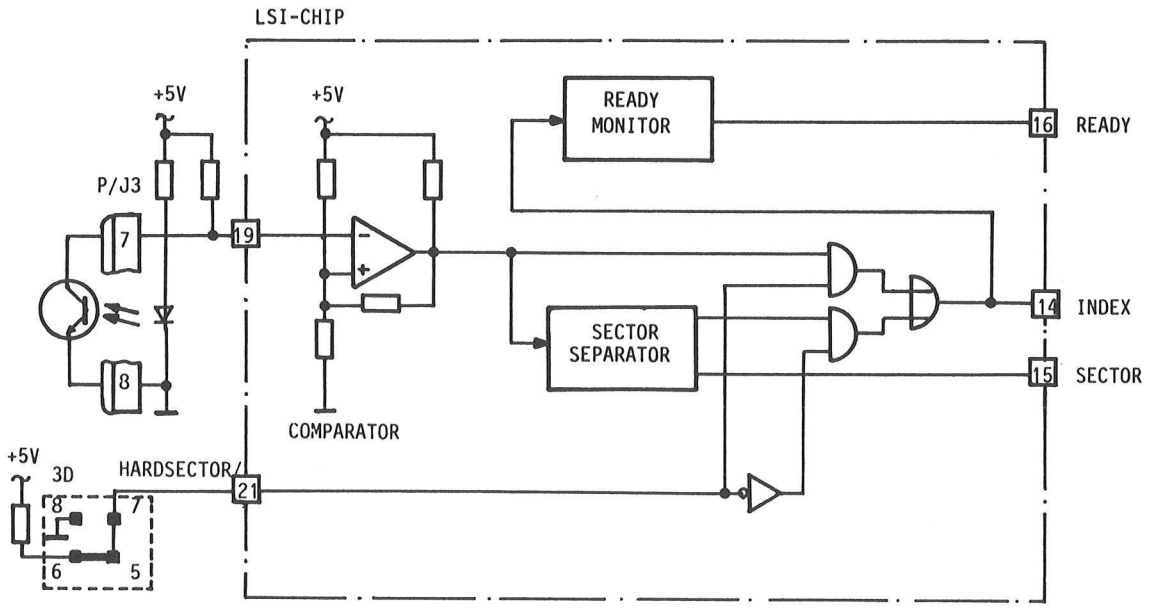


FIGURE 2 - 24 : INDEX DETECTOR

2.3.10.2. SECTOR SEPARATOR

The sector separator is used for hard sector applications only. A hard sectored mini diskette contains 10 or 16 sector holes and one index hole in the middle between two sector holes. The INDEX/SECTOR separator logic (see fig. 2 - 25) separates the INDEX pulse from the SECTOR pulses by the INDEX WINDOW (11.25 ms one shot), which is triggered by the trailing edge of the 0.4 ms one shot pulses (see timing diagram fig. 2 - 26). The INDEX-pulse width is limited to 0.4 ms by the 0.4 ms one shot when the sector separator option is used.

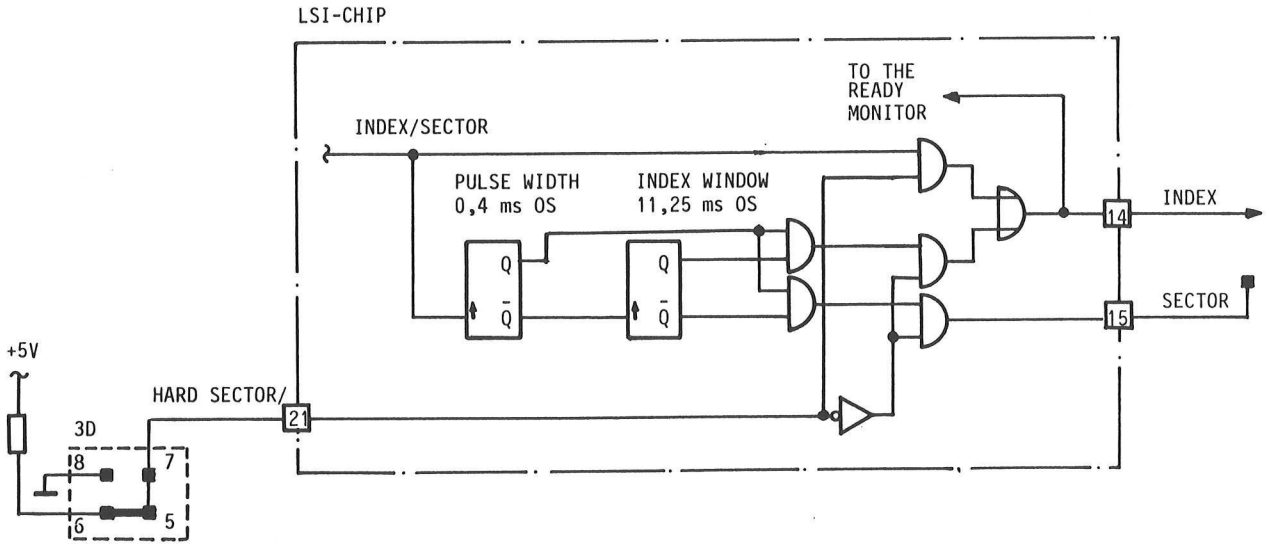


FIGURE 2 - 25 : SECTOR SEPARATOR

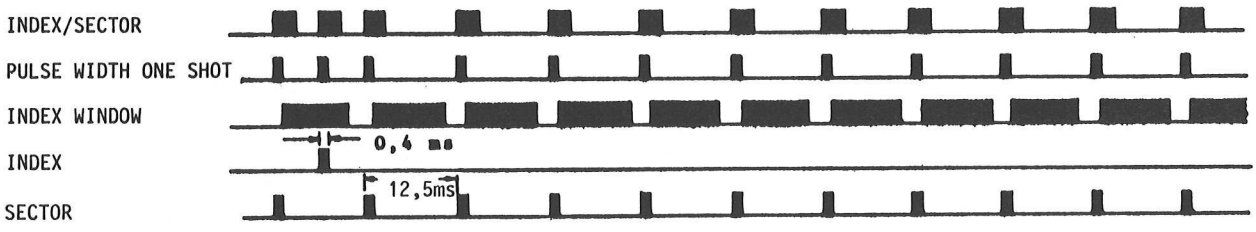


FIGURE 2 - 26 : TIMING DIAGRAM INDEX / SECTOR SEPARATOR

2.3.10.3. READY DETECTION

The ready detector (fig. 2 - 27) is used to monitor the INDEX pulses for the rotational speed of the disk. The INDEX pulses are input to the 430 msec hold-over-one shot. When the time between two consecutive INDEX pulses is greater than 430 msec, the index counter is held reset. If the time is less than 430 msec, the hold-over-one shot is held fired and enables the index counter.
READY is generated in two ways. If the drive motor starts (MOTOR ON = LOW) when the mini diskette has been already inserted, READY will be generated by the first INDEX pulse which occurs in a shorter distance than 430 ms because the WRTPROT FF of the temporary motor on logic is low. When the mini diskette is just inserted and the temporary motor on logic starts the motor (WRTPROT-FF = high) or the motor is already spinning, the READY-signal will be generated by the second INDEX pulse in a shorter distance than 434 ms (see timing diagram fig. 2 - 28).

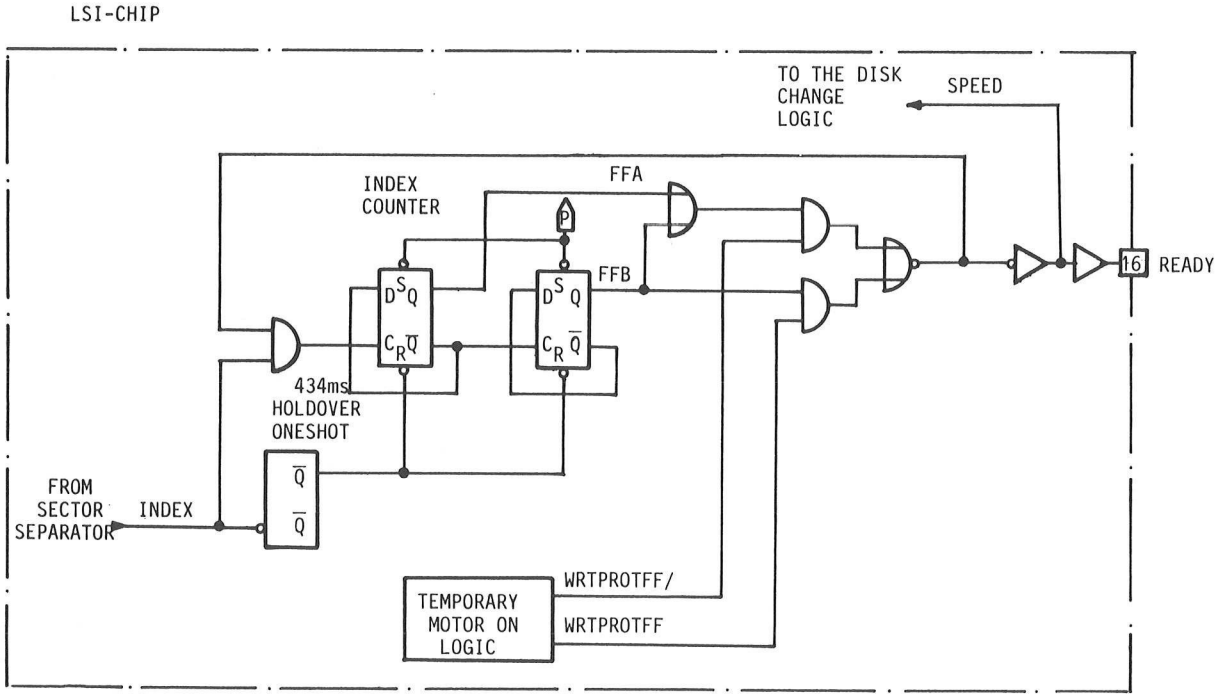
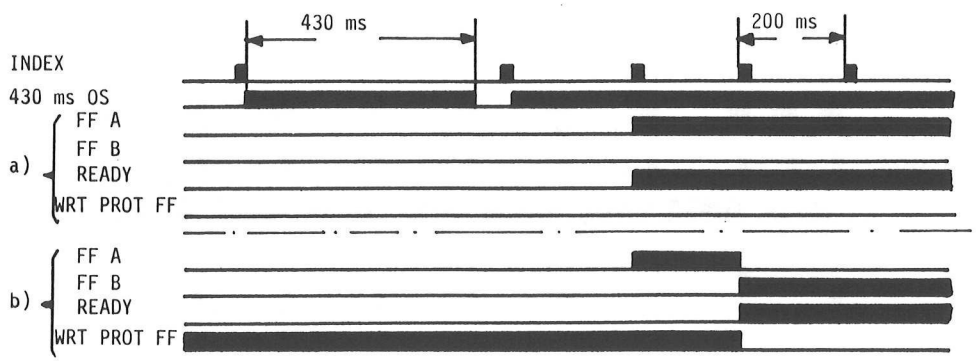


FIGURE 2 - 27 : READY DETECTOR



a) DISK ALREADY INSERTED
b) DISK JUST INSERTED (TEMP. MOTOR ON LOGIC)

FIGURE 2 - 28 : READY TIMING

2.3.11. DISK CHANGE OPTION (fig. 2 - 29)

Pin 34 of the interface can be used for the disk change option when the IN USE signal is applied to input pin 4 or the IN USE option is not used. The DISK CHANGE signal notifies the host system that the mini disk has been changed even if the drive was deselected. As soon as the mini disk is unloaded, the speed detector will deactivate the SPEED-signal and the DISK CHANGE-FF is set. The DISK CHANGE signal is sent to the host system when the drive is selected. The DISK CHANGE-FF will stay set when the new mini disk is loaded. To deactivate the DISK CHANGE signal, the host system must deselect the drive again. The DISK CHANGE-FF is than reset (see timing diagram fig. 2 - 30). The disk change option is enabled by a jumper from 4D (11-12).

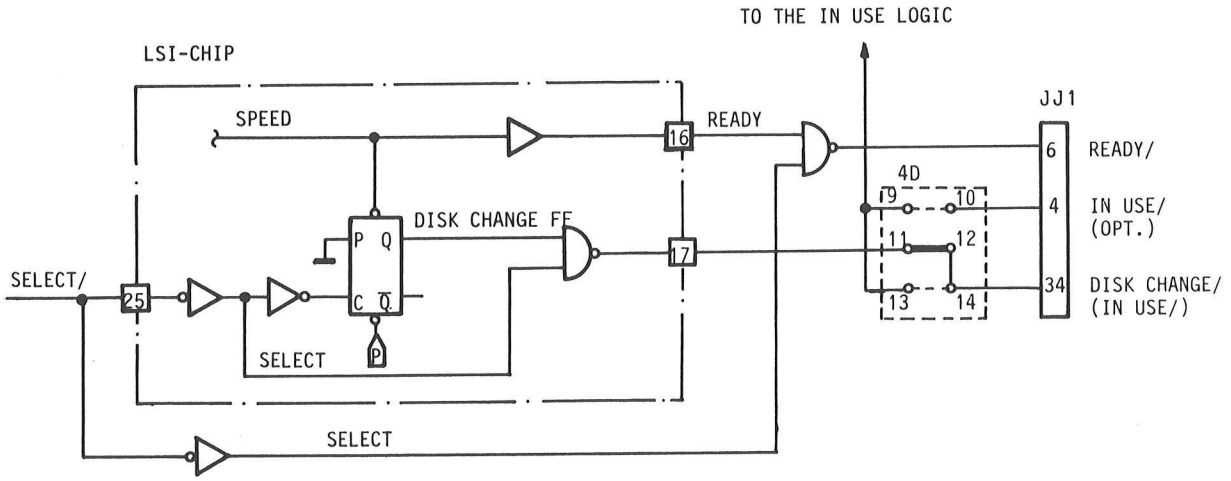


FIGURE 2 - 29 : DISK CHANGE LOGIC

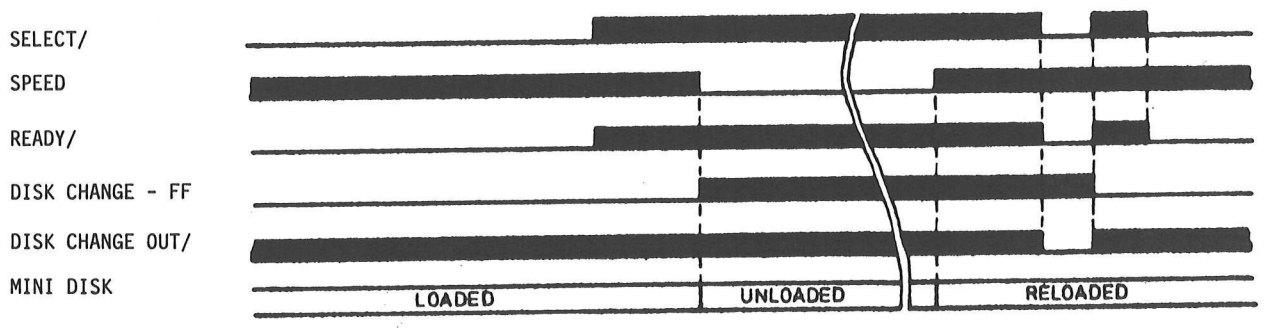


FIGURE 2 - 30 : TIMING DIAGRAM DISK CHANGE LOGIC

2.3.12. SIDE SELECT LOGIC

The side select logic is used by the double sided mini disk drive (BASF 6108) and selects either head 0 or head 1, depending whether the SIDE 1-signal from the input interface is high or low. The side select logic in fig. 2 - 31 consists of two head select switches (T 11, T 12 and associated circuits) and a diode matrix (D1, 2, 11, 12, 16, 17). If the SIDE 1-signal is low, transistor T 12 is on and head 0 is selected.The signal COM0/ is at ground and generates a forward bias to the diodes D 11, D 12 and D 16.

In a read operation, the read signal induced in the read/write coils of head 0, is transfered through the diodes D 11, D 12 to the read circuits. In a write operation, the write current generated in the write circuits flows through these diodes into the read/write coils. The erase current is fed to the erase coil by the diode D16. At the same time, the diodes D 1, D 2 and D 17 are blocked, because transistor T 11 is off. Transistor T 11 will be on when SIDE 1 is high and head 1 is activated.

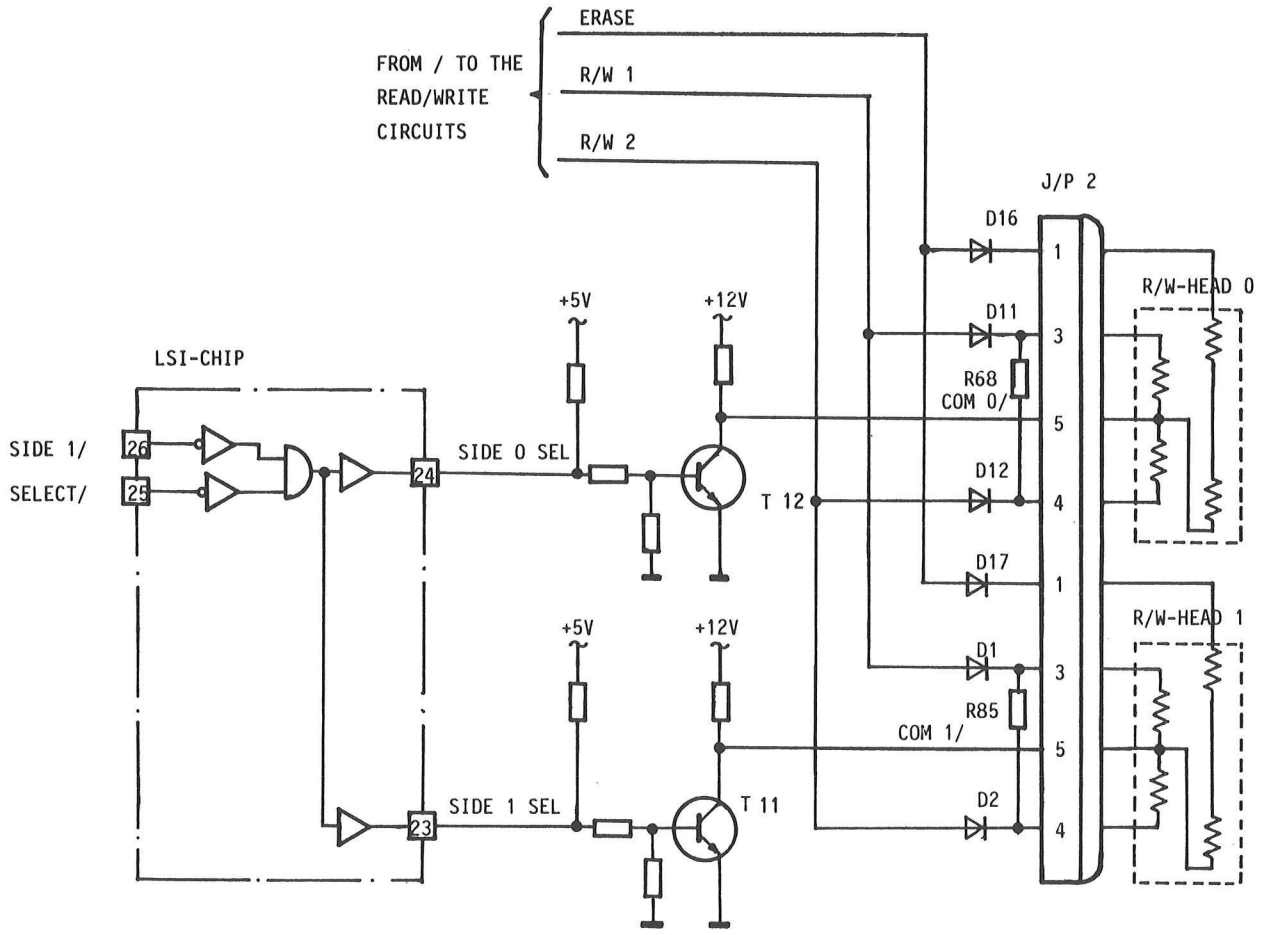


FIGURE 2 - 31 : SIDE SELECT LOGIC

2.3.13. READ/WRITE HEADS

The read/write heads used in the BASF 6106/6108 disk drives are tunnel erase type heads. Data is recorded at a flux density of 3536 to 5536 flux changes per inch (fci).

The nominal frequencies on the read/write head are 62.5 kHz and 125 kHz when FM recording technique and 62.5 kHz, 125 kHz and 83.3 kHz when MFM recording is used. In FM mode, the nominal distance between flux reversals is 4 µs or 8 µs. In MFM 6 µs flux reversal spacings are also encountered.

The radial density is 48 tracks per inch (tpi). This gives 0.0208 inch nominal track to track spacing.The tunnel erase gaps trim the track width from 0.014 inch after write to 0.013 inch after erase (see fig.2-32).

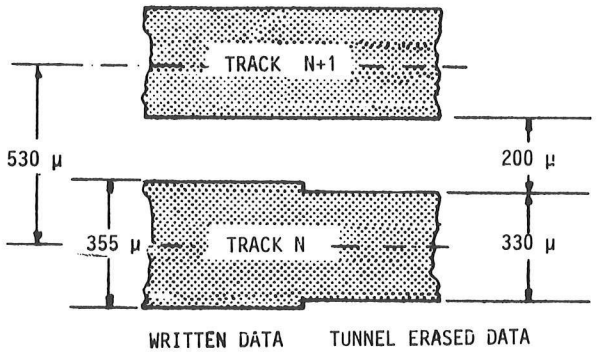


FIGURE 2 - 32 : TRACK GEOMETRY

The read/write head contains three coils : two read/write coils and the erase coil (see fig. 2 -).The erase coil is energized during each write operation and limits the track width and provides low noise guard bands on each side of the recorded track. The two read/write coils are wound on a single core and are center tapped. The electrical connections of the read/write head are shown in fig. 2 - 33. During a write operation, the write current will be directed alternately to one of the two read/write coils by a flipflop. This causes a flux change each bit to be written. The old data on the track will be overwritten by the new data stream.
On a read operation, an output voltage is induced in the read/write head by each flux change that passes the gap of the read/write head. This voltage is used by the read circuits to recover the written data.

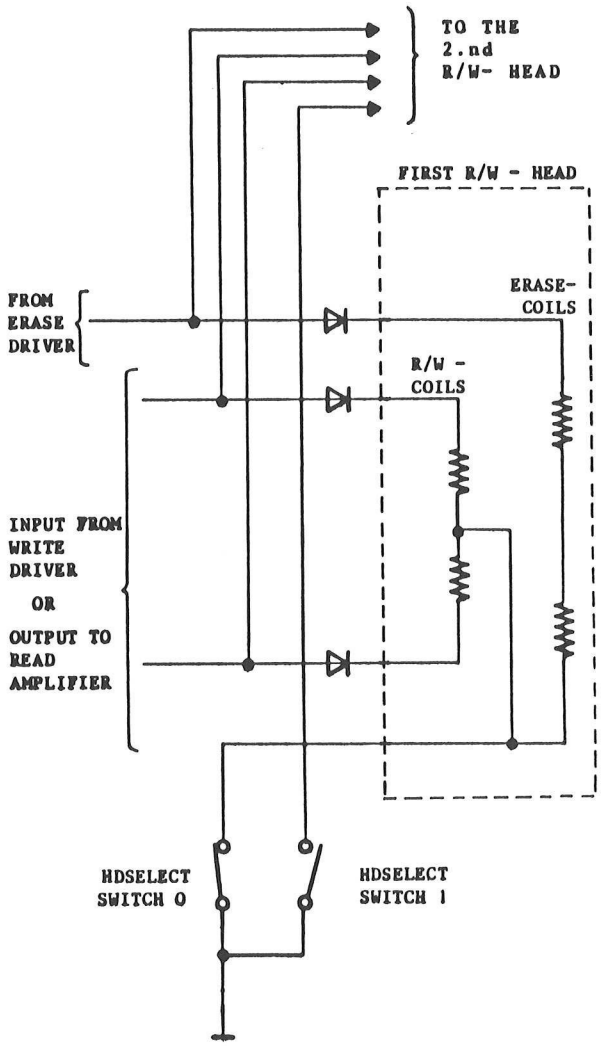


FIGURE 2 - 33 :
ELECTRICAL CONNECTION OF THE READ/WRITE HEAD

2.3.14. WRITE CIRCUITS

2.3.14.1. WRITE INITIATE

The write circuits encode serial data from the host system to magnetic flux patterns recorded on the flexy disk. A write operation is initiated by the host system activating the following input lines (see fig. 2 -34).

- SELECT/ : selects the drive and loads the head if no head load option is installed
- MOTOR ON/ : rotates the mini disk
- WRITE GATE/ : turns on the write circuits
- WRITE DATA/ : encoded write data
- HEAD LOAD/ : loads the head if head load option is used

2.3.14.2. WRITE LOGIC

A simplified logic of the write circuit is shown on fig. 2 - 35. The write circuits are activated by WRTENA/ which is active when the host system sends WRITE GATE. The drive must be selected and the disk not write protected. The data stream from the host system is divided by the write flipflop. It alternately turns on transistors T3 and T4 (see fig. 2-36). The write currents I_W and $I_{W'}$ which are determined by the resistor R 35 flow then alternately through the windings W_1 and W_2.
The write current and erase current can be blocked by the DC-control logic, if a power failure has been detected. The erase current I_E is turned on by transistor T5 when ERASENA/ is low. The write and erase current are blocked by the DC-control logic if a power failure occurs.

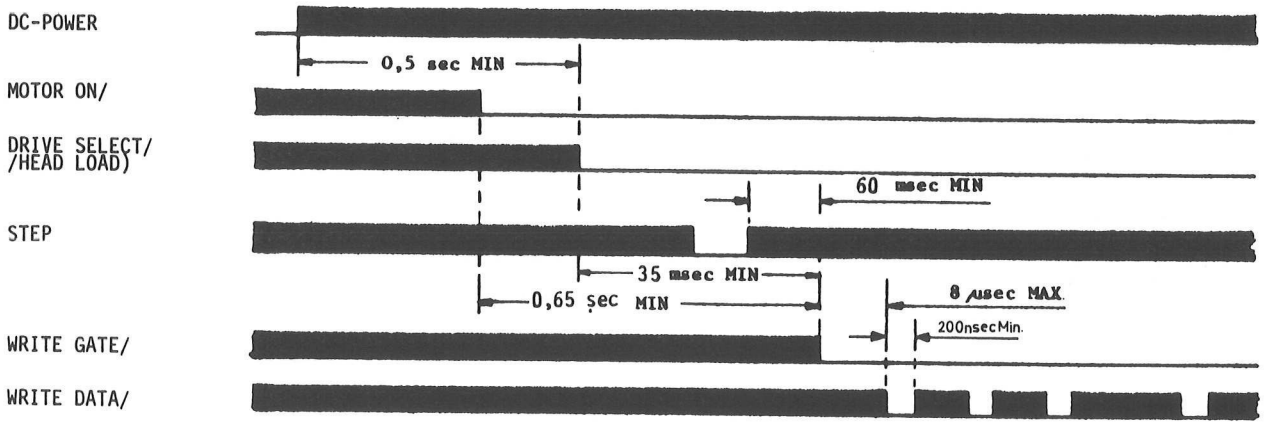


FIGURE 2 - 34 : WRITE INITIATE TIMING

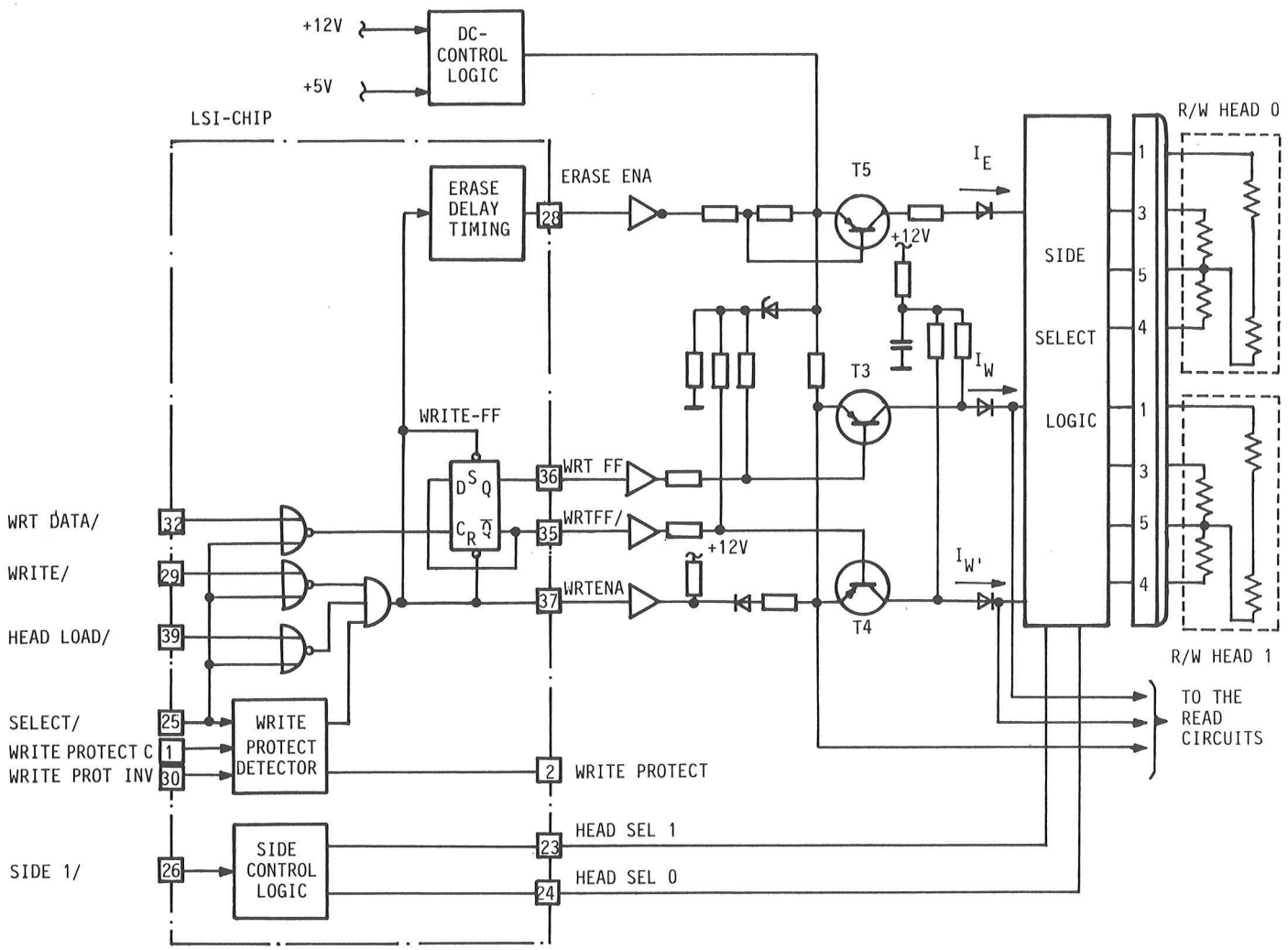


FIGURE 2 - 35 : SIMPLIFIED WRITE CIRCUITS BASF 6106/6108

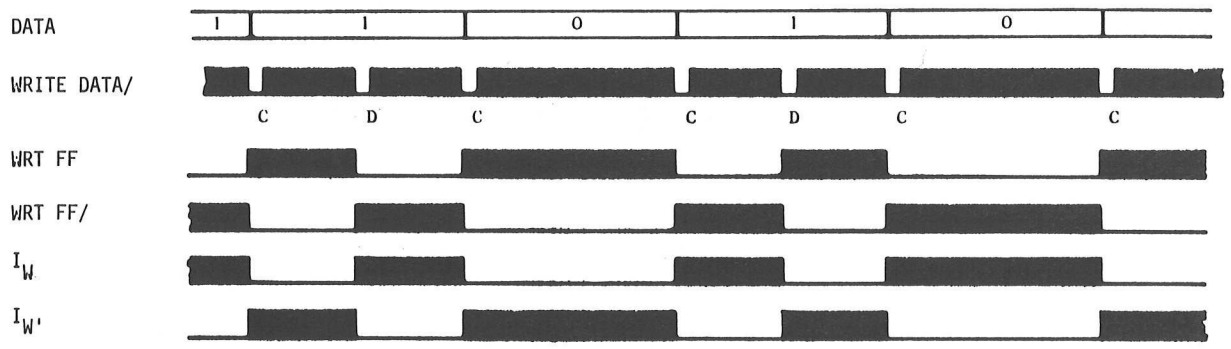


FIGURE 2 - 36 : TIMING DIAGRAM - WRITE OPERATION FM (SIMPLIFIED)

2.3.14.3. ERASE DELAY LOGIC

The erase current must be switched on (off) a certain delay after the write current has been switched on (off). This delay is necessary, because tunnel erase type read/write heads are used. The erase delay logic in the LSI comprises two one shots, one for the erase on delay time, the other for the erase off delay time and the ERASE ENA-FF (see figure 2 - 37).
The ERASE ENA-FF which the erase current turns on is reset during power on by the PWR ON*R/-signal. It is set when the ERASE ON DLY - one shot times out and is reset when the ERASE OFF DLY - one shot times out (see figure 2 - 38).

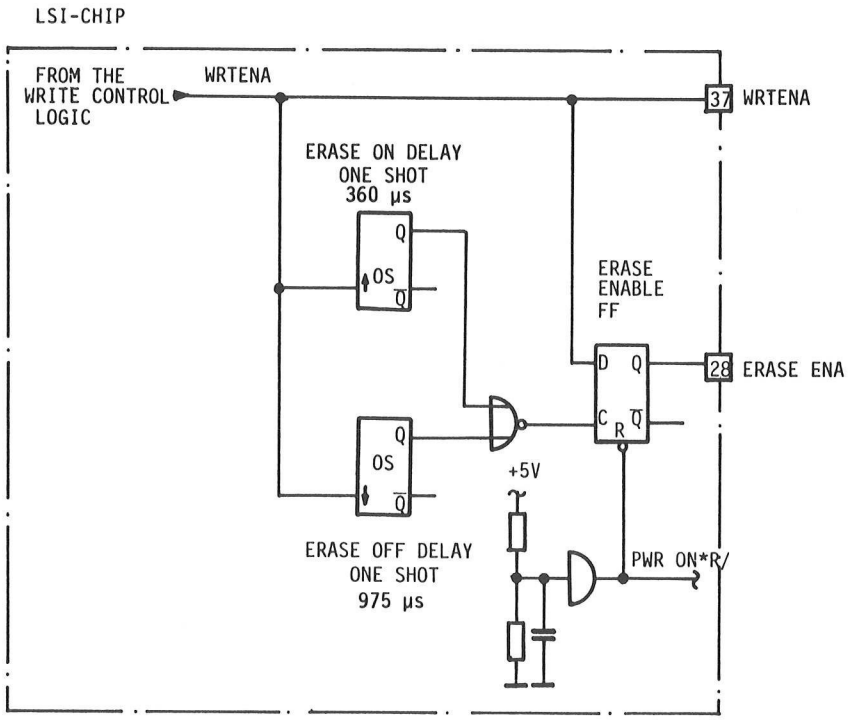


FIGURE 2 - 37 : ERASE DELAY LOGIC

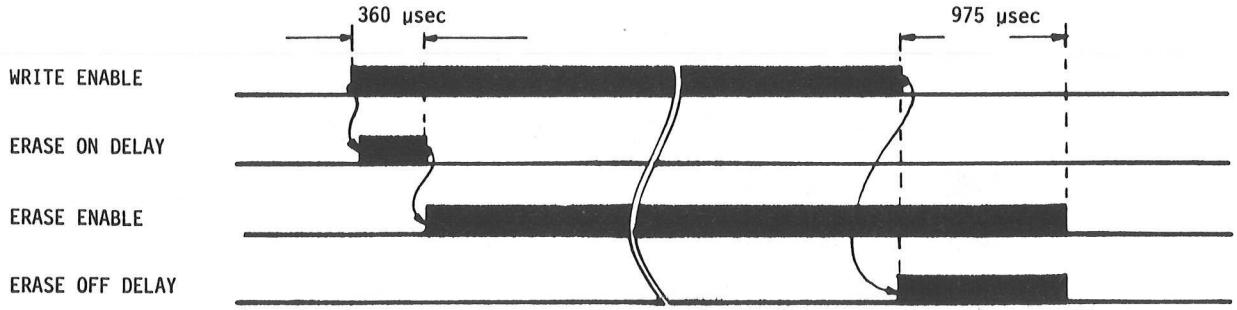


FIGURE 2 - 38 : ERASE DELAY TIMING

2.3.14.4. WRITE PROTECT DETECTOR

The write protect detector (fig. 2 - 39) is implemented like the index detector. A LED and a photo transistor are used with a comparator circuit to detect the write protect notch in the flexy disk. When a flexy disk with an open notch is inserted, the photo transistor will sense the light of the LED causing the negative input of the comparator to go low and the output of the comparator "NOTCH OPEN" will be high. The setting of the write protect inverse option jumper decides, whether writing is allowed or not (see the following table).

If WRITE INHIBIT is high, the WRITE ENABLE-signal is disabled. The mini disk drive is now unable to write even if the host system will activate the WRITE/ interface line. The WRITE PROTECT/-signal is sent to the host system when SELECT is high. The WRITE PROTECT line informs the host system, that a write protected flexy disk is inserted. If an unprotected flexy disk is inserted, WRITE PROTECT/ will be inactive and write operations are allowed.

JUMPER 2D (1-2)	NOTCH COVERED	NOTCH OPEN	REMARKS
INSERTED	unprotected	protected	optional
OPEN	protected	unprotected	ECMA

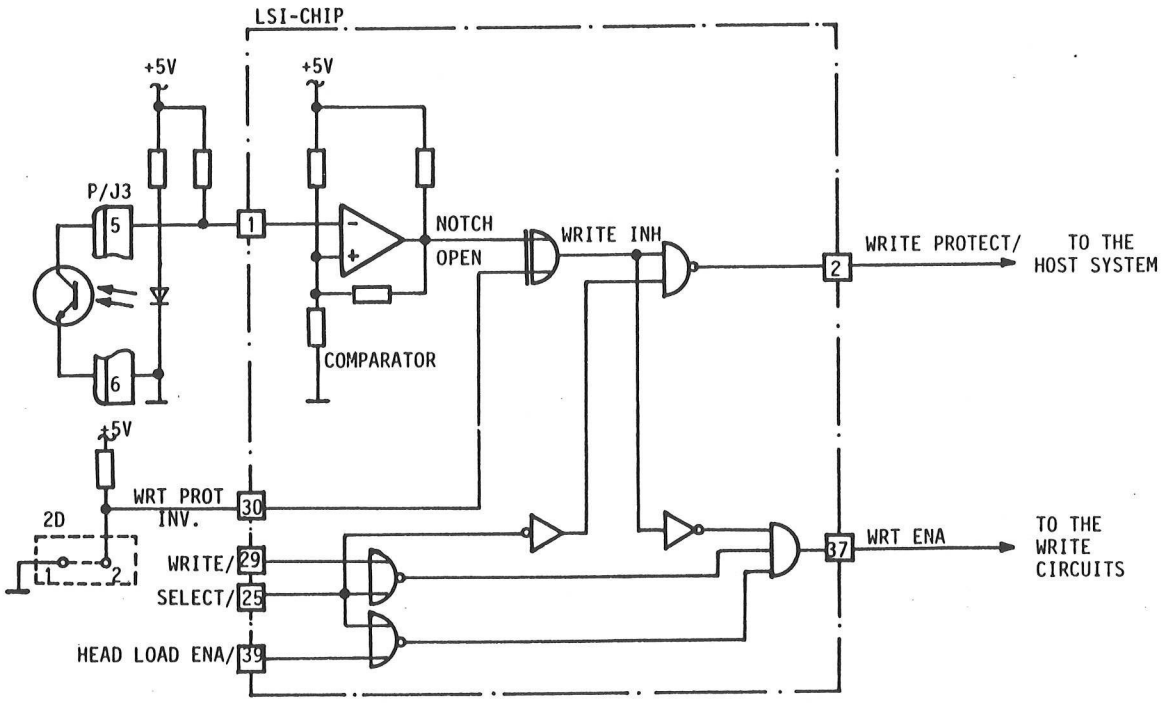


FIGURE 2 - 39 : WRITE PROTECT DETECTOR

2.3.15. READ CIRCUITS

2.3.15.1. READ INITIATE AND READ BLOCK DIAGRAM

The read circuits recover data recorded on the flexy disk by a write operation. A read operation is initiated from the host system by activating the following lines :

- SELECT/ : selects the drive and loads the head if auto head load option is used
- MOTOR ON/ : rotates the flexy disk
- HEAD LOAD/ : loads the head if head load option is used
- SIDE SELECT/ : selects head 0 or 1

The signal WRITE GATE/ must be inactive to enable the read circuits. Fig. 2 - 40 shows the read initiate timing. The read circuits shown on fig. 2 - 41 comprise an integrated read amplifier and the necessary external components.

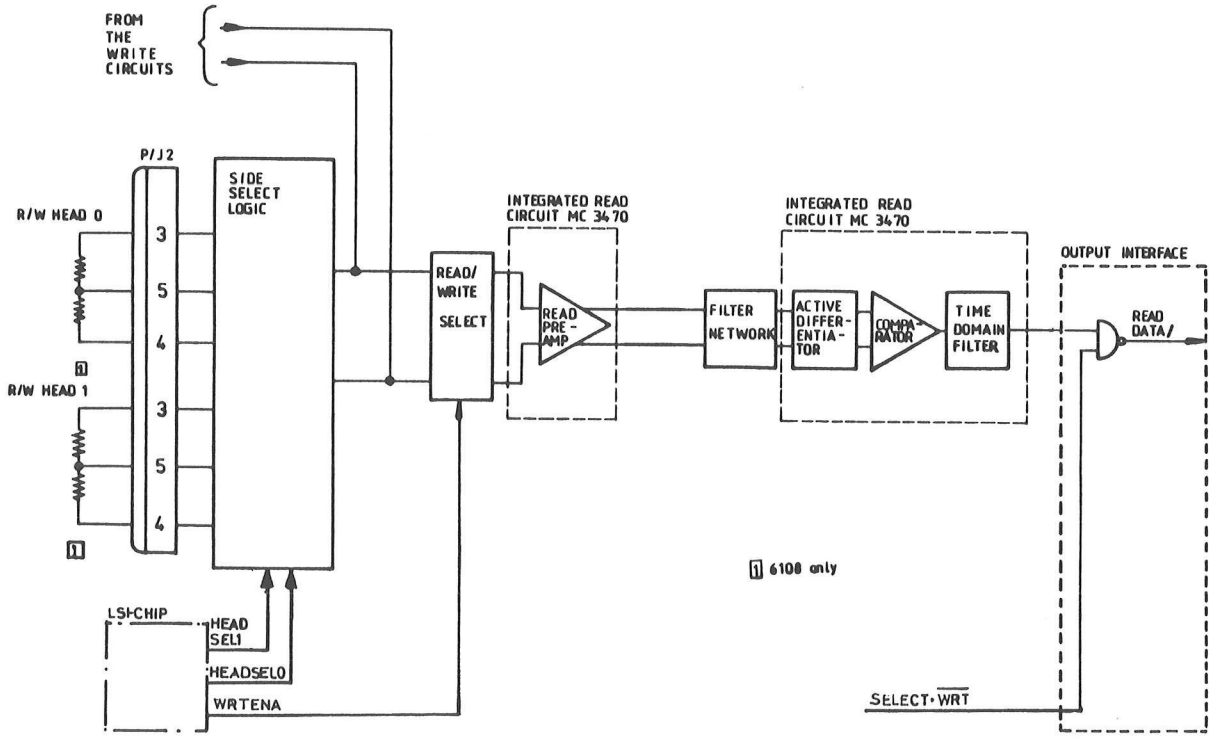


FIGURE 2 - 40 : READ CIRCUITS BASF 6106/6108 (SIMPLIFIED)

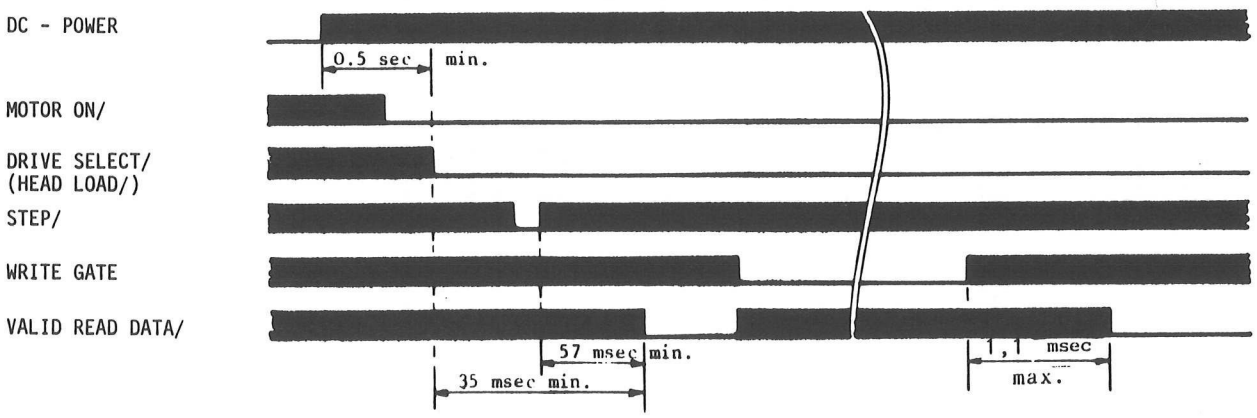


FIGURE 2 - 41 : READ INITIATE TIMING

2.3.15.2. READ/WRITE SELECT

The read/write select circuit consists of two MOS-FET switches. The inputs of the switches are connected to the read/write coils of the selected read/write head. The outputs of the switches are connected to the read preamplifier (see fig. 2 - 42).

When the disk drive is operating in the WRITE-mode, WRTENA:01 is high and T6 and T7 are open. The read/write coils are disconnected from the read preamplifier. In the READ-mode WRTENA:01 is low, the output signal of the selected read write head is switched to the read preamplifier.

2.3.15.3. READ AMPLIFIERS AND FILTER NETWORK (FIG. 2 - 43)

For amplification of the read signal, a high gain linear amplifier of the read LSI is used. The read signal is amplified by a gain of ~100. The amplifier outputs are used to drive a filter network. The filter is a linear phase low pass and has a -3db band width of 400 kilohertz.

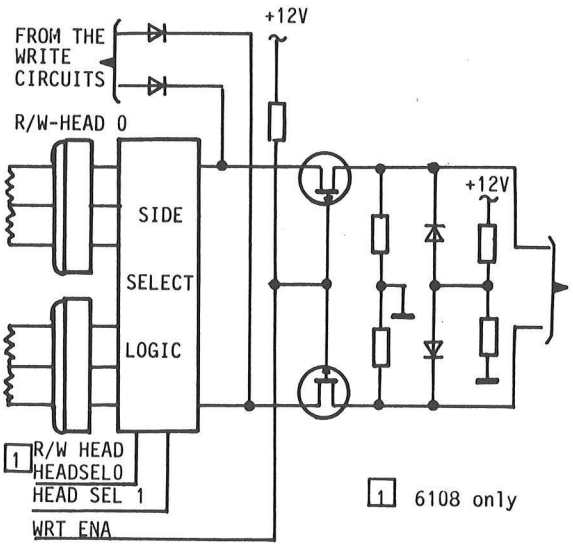


FIGURE 2 - 42 : READ/WRITE SELECT LOGIC

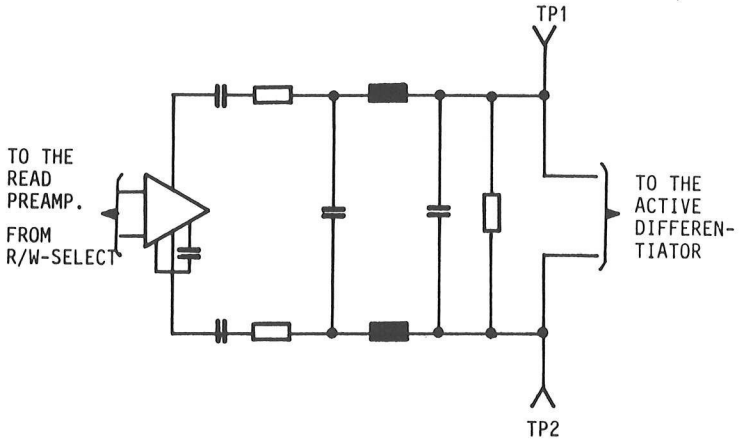


FIGURE 2 - 43 :
READ PREAMPLIFIER AND FILTER NETWORK

2.3.15.4. ACTIVE DIFFERENTIATOR AND COMPARATOR

Both circuits are part of the read LSI MC 3470. A simplified circuit is shown on fig. 2 - 44 . The active differentiator is implemented by a differential amplifier with capacitor coupled emitters. The current through this capacitor and also through the collector resistor will be a derivative of the input voltage.

$$I_C = C \cdot \frac{dV_{in(t)}}{dt}$$

Also the output voltage Vo of the differential amplifier will be a derivative of the input voltage.

$$V_0 = 2\,R \cdot I_C = 2\,R\,C \frac{dV_{in(t)}}{dt}$$

The output voltage Vo is applied to the comparator which provides zero crossing detection of the wave - form. Since the capacitor shifts the current $\sim$ 90° to the input voltage peak detection of the input voltage is performed. Fig. 2 - 46 shows a timing diagram of the differentiator and comparator circuit.

2.3.15.5. TIME DOMAIN FILTER AND CROSSOVER DETECTOR

The purpose of the time domain filter is to suppress false crossovers of the comparator caused by shouldering in the differentiated read signal. This can happen on outer tracks of high resolution disks when high resolution heads are used : the time domain filter contains a pulse generator, the time domain one shot and the time domain flipflop (see fig.2-45) and is part of the integrated read LSI. The pulse generator generates a short pulse for each transition on its input. These pulses are used to trigger the time domain one shot. The pulse duration of the time domain one shot is determined by an external RC-combination and is set to less than 2 µsec for the BASF 6106 and 6108. The state of the comparator output is loaded into the time domain flipflop by the trailing edge of the time domain one shot 2 µsec later (see fig. 2 - 46). Because false zero crossings always exist for a shorter time, the time domain flipflop will not change when it is clocked by false crossovers.

The crossover detector consists of a bidirectional one shot which is triggered by each transition of the time domain flipflop. The pulse width of the crossover detector can be adjusted by external elements. For the BASF 6106 and 6108, the output pulses (READ DATA/) of the crossover detector are set to 500nsec.

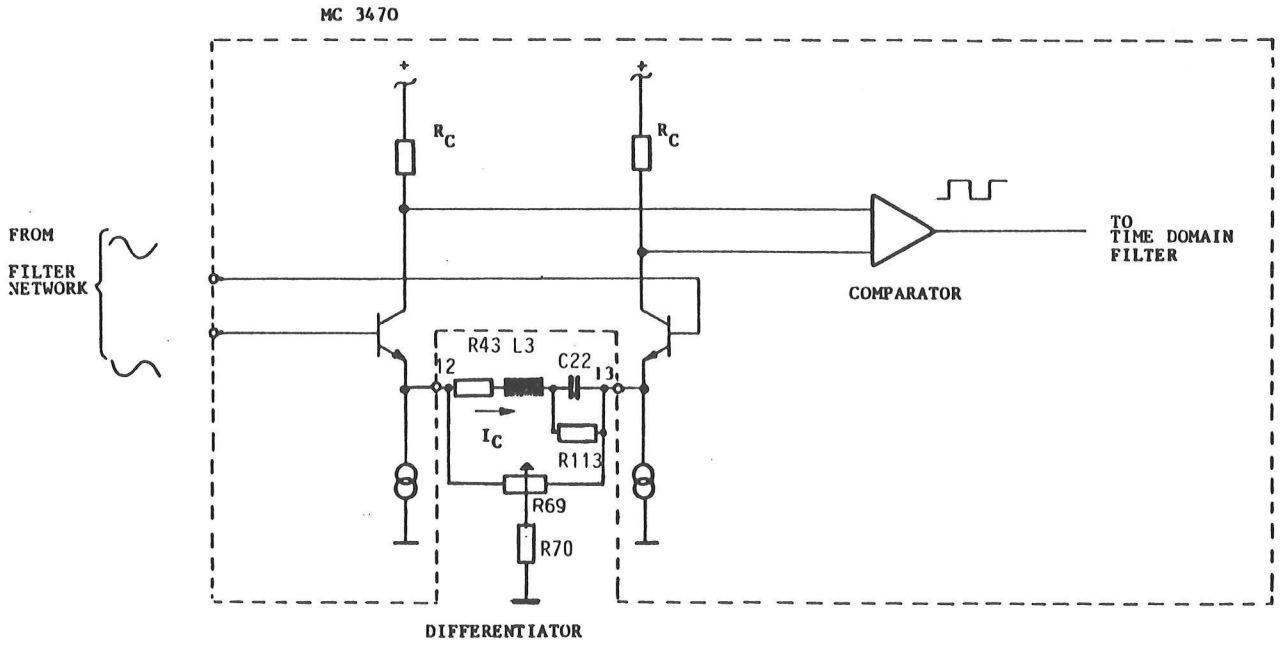


FIGURE 2 - 44 : ACTIVE DIFFERENTIATOR AND COMPARATOR

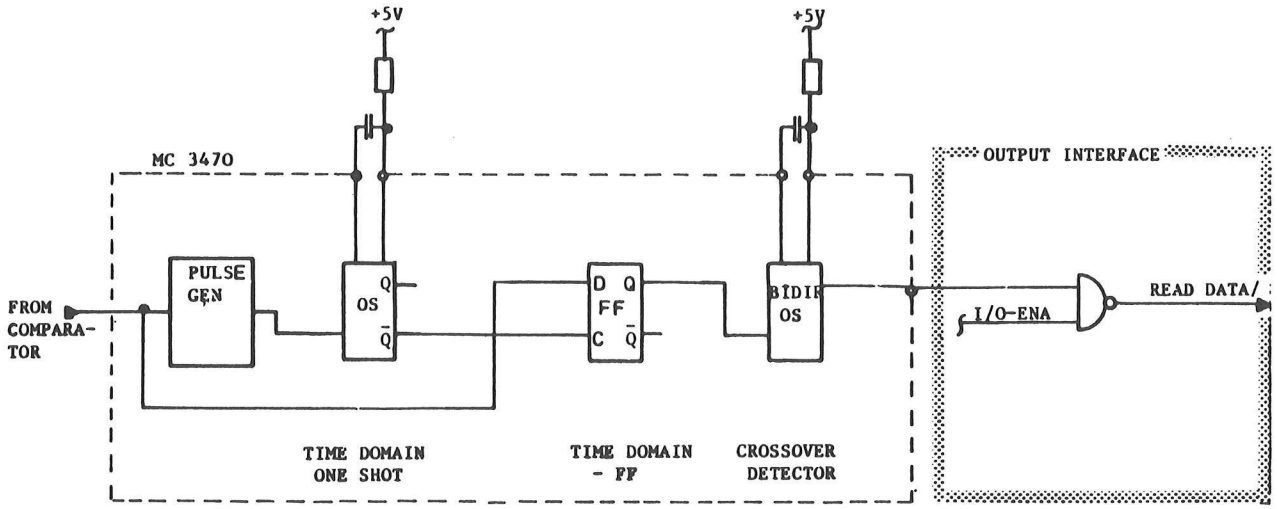


FIGURE 2 - 45 : TIME DOMAIN FILTER AND CROSSOVER DETECTOR

2.3.15.6. TIMING DIAGRAM READ CIRCUIT

Figure 2 - 46 is a timing diagram of the read circuits and illustrates the functions described above.

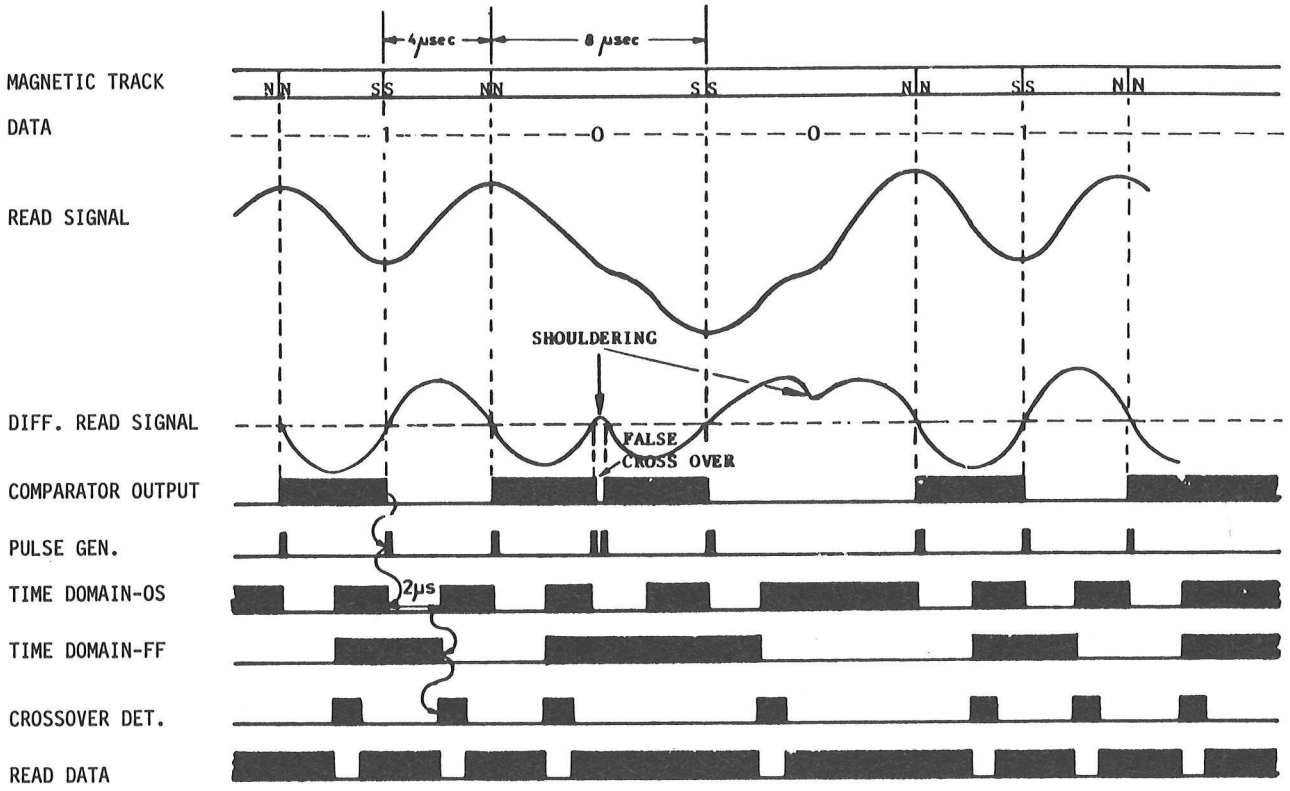


FIGURE 2 - 46 : TIMING DIAGRAM READ CIRCUIT

2.3.16. DC-CONTROL

The DC-control logic is shown on fig. 2 - 47. This logic monitors the DC-voltages +5V and +12V and disables the write and erase current source, if one of these voltages is missing or out of the following limits :

If +5V falls below 4,3V , DC-CONTROL goes high and disables T2.

If +12V falls below +9V, T2 is also blocked and the write and erase current inhibited.

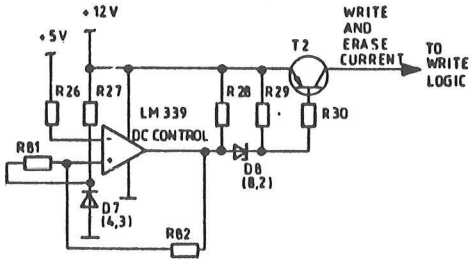


FIGURE 2 - 47 : DC-CONTROL LOGIC

SECTION III.

INSTALLATION AND OPERATION

3.1. INSTALLATION

3.1.1. GENERAL

This section provides informations for installation and configuration of the mini disk drive.

3.1.2. UNPACKING AND INSPECTION

The mini disk drive is packaged in a heavy duty container, designed to ensure adequate protection during shipping and handling (see figure 3 - 1). When the mini disk drive is installed, store the container and all packing material for possible future use. Use the following procedure during unpacking and inspection :

- Remove contents of shipping container and inspect for in-transit damage. If damage is evident, notify the carrier and BASF. Specify nature and extent of the damage ;
- Verify that content of shipping container agrees with shipping list. Notify a BASF representitive if anything is missing ;
- Verify that model designation and serial number agree with those on the shipping invoice ;

BASF 6108 :

- Inspect assemblies for loose hardware. Tighten hardware if necessary ;
- Remove red retainer ;
- Remove shipping disk ;
- Store shipping disk, red retainer and containers for a possible future use.

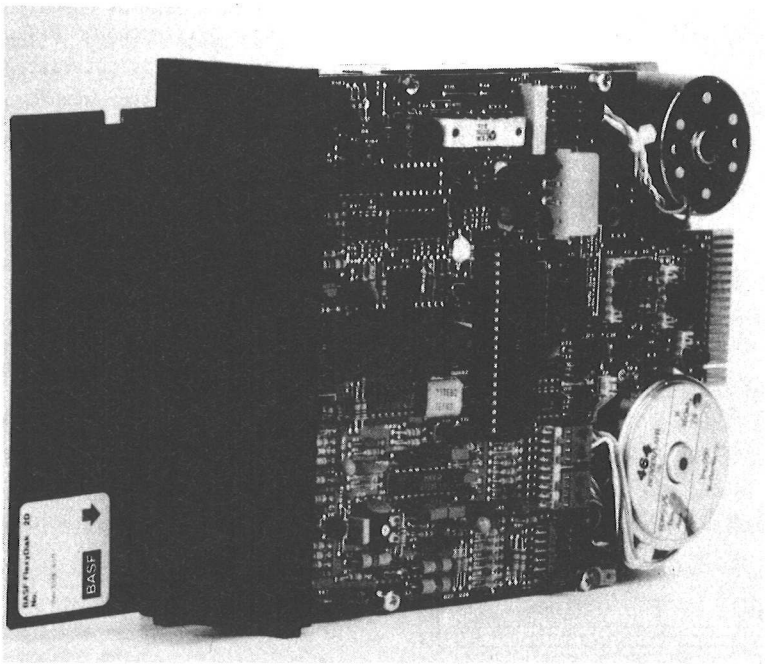


FIGURE 3 - 1 : BASF 6108 DRIVE EQUIPPED WITH SHIPPING PROTECTION

3.1.3. CONNECTING CABLES

The mini disk drive is connected to the host system by two connecting cables, the DC-cable and the interface cable. The DC-cable requires direct connection to each drive, regardless of connecting configuration. The interface cable is connected to the various connecting configurations (see 3.1.6.) and should not exceed 10 feet in length.

3.1.4. CONNECTORS

3.1.4.1. DC-CONNECTOR

DC power is connected to the disk drive through connector J5. The input pin assignments and voltage requirements are listed in table 3 - 1.

PIN No.	DC VOLTAGE	TOLERANCE	CURRENT	MAX. RIPPLE (p - p)
1	+ 12 V	± 0.6 V	+)1.75A	100 mV
2	+ 12V RET	-	-	-
3	+ 5V RET	-	-	-
4	+ 5 V	± 0.25V	0.7 A	50 mV

+) Plus 0.65 A motor starting current for max. 50 msec.

Voltages to be measured on testpoints on drive PCB.

TABLE 3 - 1 : DC-POWER REQUIREMENTS

The return lines for +12V and +5V (pins 2 and 3) should be separate lines and must be connected together in the system. DC power input connector J5 is mounted on the component side of the PCB beside the stepper motor (see figure 3 - 9). The 4 pin connector is BASF P/N 88359-001 (see figure 3 - 2) and is soldered directly to the PCB. The recommended mating connector is AMP P/N 1-480424-0 is using pins P/N 60619-1.

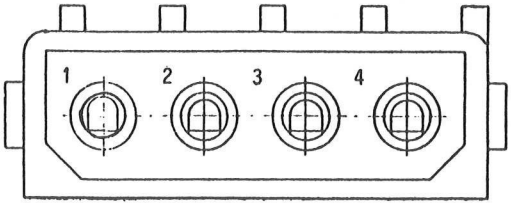


FIGURE 3 - 2 : DC-CONNECTOR

3.1.4.2. SIGNAL CONNECTOR

The signal cable is connected to the mini disk drive through connector J1. Connector J1 is a 34 pin PCB edge card connector located at the rear of the disk drive. The pins are numbered from 1 to 34 with the even pins on the component side. Pin 2 is located closest to the stepper motor and is marked. A keyslot is provided between pins 4 and 6 for optional connector keying. Recommended mating connectors for J1 are listed in table 3 - 2.

CABLE TYPE	MANUFACTURER	CONNECTOR P/N	CONTACT P/N
FLAT CABLE	SCOTCHFLEX	3463-0000	NA
		3463-0001	NA
TWISTED PAIR # 26	AMP	583717-5	1-583616-1

TABLE 3 - 2 : RECOMMENDED J1 MATING CONNECTORS

3.1.4.3. FRAME CONNECTOR

The mini disk drive must be frame grounded to the host system to insure proper operation. A fast on tab is provided on the drive near to the stepper motor. A fast on connector with AC ground from the host system can be attached or soldered if the mini disk drive is not fastened directly to the frame of the host system with a good AC ground. The tab is Grothe-Hartmann 17132 and its mating connector is Grothe-Hartmann 123211.

3.1.4.4. INTERCONNECTING DIAGRAM

Figure 3 - 3 is provided as an interconnecting diagram showing the connections directly to or from the PCB. Connectors J2, J3 and J6 are for internal drive use, connector J1 and J5 are from the controller.

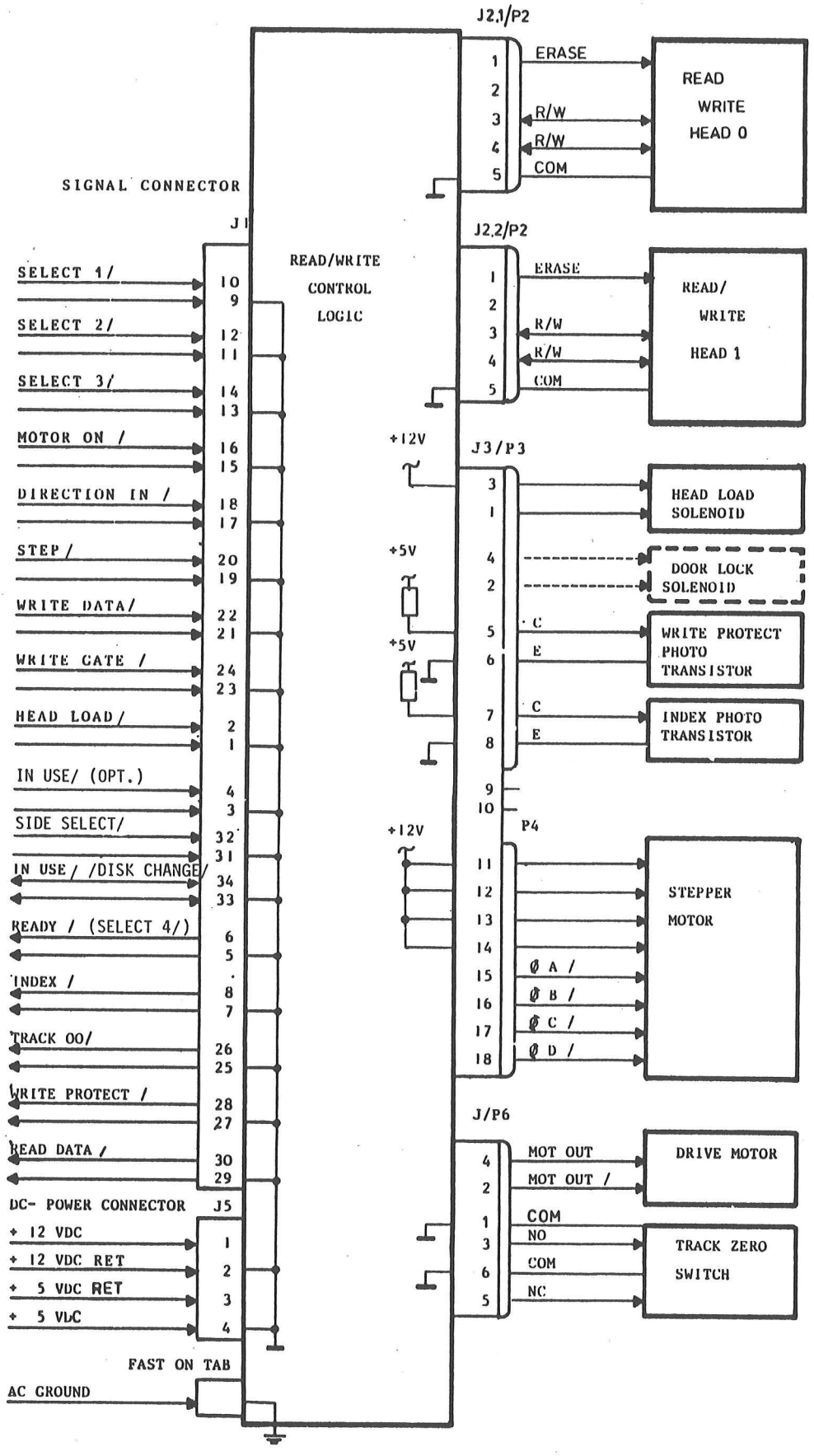


FIGURE 3 - 3 : INTERCONNECTING DIAGRAM

3.1.5. LOGIC LEVELS AND TERMINATION

Interface signals to and from connector J1 have the logic levels represented by figure 3 - 4. All signal inputs are terminated by a 150 ohm resistor network chip (position 4D). This chip can be removed for a daisy chain configuration, where only the last mini disk drive needs a termination network.

The BASF 6106/08 uses SN 7438 or equivalent as output driver. As input receiver SN 7404 or equivalent is used. Figure 3 - 5 shows the recommended interface logic.

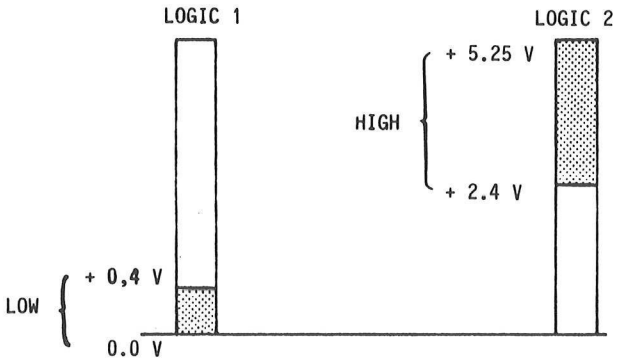


FIGURE 3 - 4 : INTERFACE LOGIC LEVELS

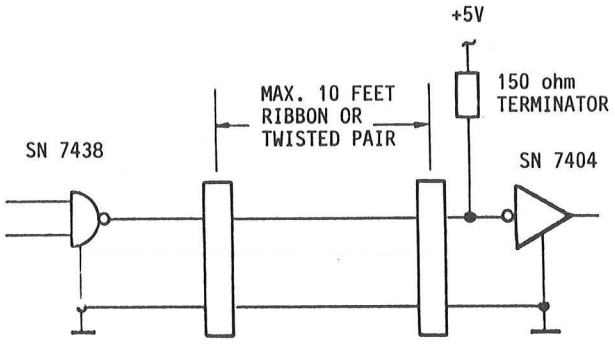


FIGURE 3 - 5 :
RECOMMENDED DRIVER / RECEIVER CIRCUIT

3.1.6. CONNECTING CONFIGURATION

The BASF 6106/6108 can be connected to the host system in different configurations :

- single drive configuration
- multi drive configuration

3.1.6.1. SINGLE DRIVE CONFIGURATION

Only one drive is connected to the host system as shown in figure 3 - 6.

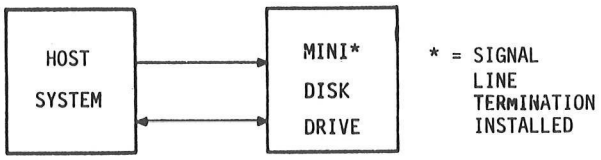
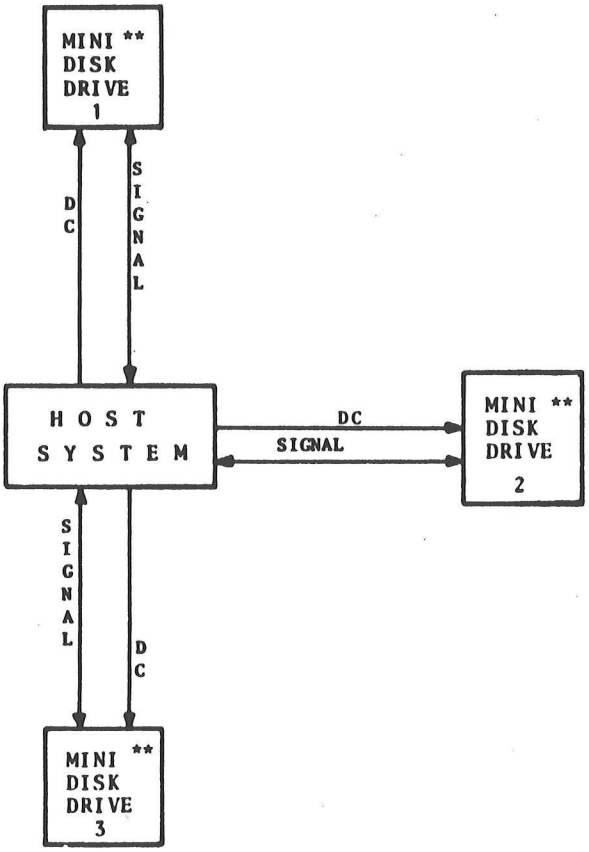


FIGURE 3 - 6 : SINGLE DRIVE CONFIGURATION

3.1.6.2. MULTIPLE DRIVE CONFIGURATION

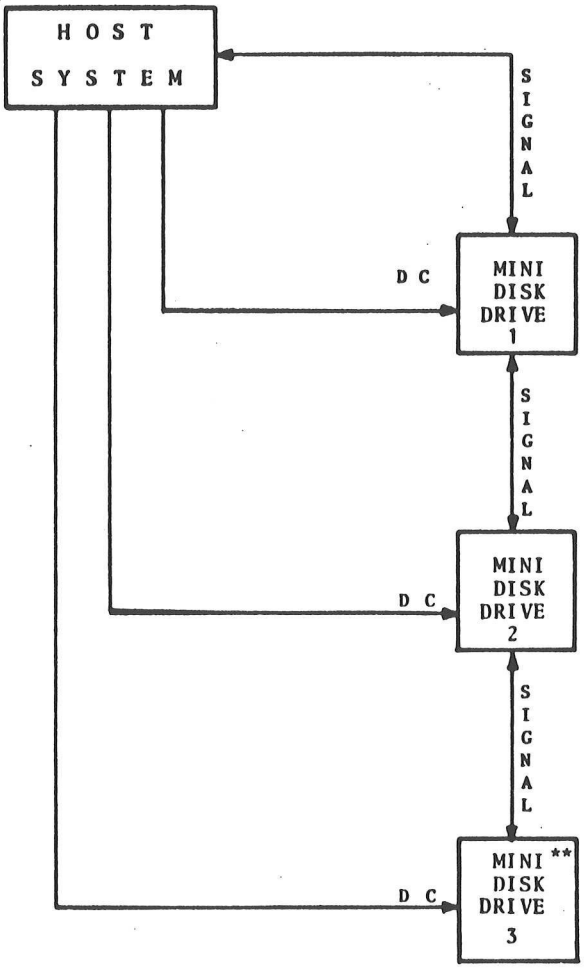
In multi drive configurations more than one drive is connected to the host system. In a multi drive configuration, the BASF 6106 can be connected in radial select or daisy chain fashion (see figures 3 - 7 and 3 - 8).

In a radial select configuration, all mini disk drives need terminator networks and in a daisy chain configuration, only the last drive needs a terminator chip.



** SIGNAL LINE TERMINATOR

FIGURE 3 - 7 : RADIAL SELECT CONFIGURATION



** SIGNAL LINE TERMINATOR

FIGURE 3 - 8 : DAISY CHAIN SELECT CONFIGURATION

3.1.7. SELECTION OF THE DESIRED OPTIONS

3.1.7.1. SELECT OPTIONS

In a single drive configuration, the auto select option will be used, in a multi drive configuration the radial select option must be used.

OPTION \ JUMPER		JJ 1			2 D		
		1-2	3-4	5-6	3-4	13-14	15-16
AUTO SELECT					X		T
RADIAL SELECT	DRIVE #1	X					T
	DRIVE #2		X				T
	DRIVE #3			X			T
	DRIVE #4*					X	C

X = jumper installed
T = trace
C = trace cut
* = no ready signal available on interface pin 6

TABLE 3 - 3 : SELECT OPTIONS JUMPERING

3.1.7.2. HEAD LOAD OPTIONS

There are three head load options :

- AUTO HEAD LOAD
  HEAD LOAD = SELECT
- SELECTED HEAD LOAD
  HEAD LOAD = SELECT.HEAD LOAD
- RADIAL HEAD LOAD
  HEAD LOAD = HEAD LOAD

OPTION \ JUMPER	2 D			
	5 - 6	7 - 8	9 - 10	11 - 12
AUTO HEAD LOAD	X		X	
SELECTED HEAD LOAD	X			X
RADIAL HEAD LOAD		X		X

TABLE 3 - 4 : HEAD LOAD OPTION JUMPERING

3.1.7.3. IN USE / DISK CHANGE OPTION

Pin 34 of the interface can be used as IN USE (INPUT) or DISK CHANGE (OUTPUT). Pin 4 of the interface can be used as IN USE INPUT (see table 3 - 5).

OPTION \ JUMPER	4 D		
	9 - 10	11 - 12	13 - 14
IN USE PIN 34			X
IN USE PIN 4	X		
DISK CHANGE OPTION		X	

TABLE 3 - 5 : IN USE / DISK CHANGE OPTION JUMPERING

3.1.7.4. DOOR LOCK OPTIONS

Locking of the door can be accomplished by the following conditions shown in table 3 - 6.

OPTION \ JUMPER		5 D						
		3-4	5-6	7-8	9-10	9-11	11-12	13-14
	IN USE*			X			X	X
D	IN USE-FF					X		X
O	SELECT	X						X
O	HEAD LOAD		X					X
R	IN USE + IN USE-FF				X		X	X
	IN USE + SELECT	X		X			X	
L	IN USE + HEAD LOAD		X	X			X	
O C K =	IN USE-FF + SELECT	X				X		
	IN USE FF+ HEAD LOAD		X			X		
	IN USE + IN USE-FF + SELECT	X			X		X	
	IN USE + IN USE-FF+ HEAD LOAD		X		X		X	

TABLE 3 - 6 : DOOR LOCK OPTIONS JUMPERING

3.1.7.5. ACTIVITY LED OPTIONS

The activity LED can be switched on by the following conditions shown in table 3 - 7.

OPTION \ JUMPER		4 D			
		1 - 2	3 - 4	5 - 6	7 - 8
ACTIVITY LED	HEAD LOAD . READY	X			X
	DOOR LOCK . READY	X		X	
	HEAD LOAD		X		X
	DOOR LOCK		X	X	

TABLE 3 - 7 : ACTIVITY LED OPTION JUMPERING

3.1.7.6. WRITE PROTECT OPTION

The manner in which the mini disk is write protected can be selected by a jumper as shown in table 3 - 8.

OPTION \ JUMPER	2 D
	1 - 2
WRITE PROTECT = NOTCH COVERED	X
WRITE PROTECT = NOTCH OPEN	

TABLE 3 - 8 : WRITE PROTECT OPTION JUMPERING

3.1.7.7. STEPPER MOTOR SWITCHING

If the stepper motor shall be enabled by the MOTOR ON signal, the following jumper must be installed (see table 3 - 9).

OPTION \ JUMPER	5 D
	1 - 2
STEP MOTOR ENABLE = MOTOR ON	X

TABLE 3 - 9 :

STEPPER MOTOR SWITCHING OPTION JUMPERING

3.1.7.8. HARD SECTOR OPTION

If sectored mini diskettes are used, hard sector option must be selected by the following jumpers (see table 3 - 10).

OPTION \ JUMPER		3 D	
		5 - 6	7 - 8
HARD SECTOR	inactive	T	
	active	C	T

T = TRACE
C = TRACE CUT

TABLE 3 - 10 :

HARD SECTOR OPTION JUMPERING

3.1.7.9. JUMPER MATRIX

Table 3 - 11 provides a jumper matrix for all options. For selecting the desired jumpers provide the following :

- Select one of the SELECT options and install the jumpers ;
- Select one of the HEAD LOAD options and install the jumpers ;
- Select IN USE or DISK CHANGE option ;
- Select one of the DOOR LATCH options, if door locking or activity LED is used. Install the jumpers ;
- Select one of the activity LED options and install the jumpers ;
- Select one of the WRITE PROTECT options and install the jumpers ;
- Install the stepper motor switching jumper if desired ;
- Activate the HARD SECTOR option if desired.

For location of jumpers, refer to figure 3 - 9.

OPTION		JUMPER	JJ 1			2 D								3D		4 D								5 D							
			1-2	3-4	5-6	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	5-6	7-8	1-2	3-4	5-6	7-8	9-10	11-12	13-14	1-2	3-4	5-6	7-8	9-10	9-11	11-12	13-14
SELECT OPTIONS	AUTO SELECT						X						T																	
		DRIVE # 1	X										T																	
		DRIVE # 2		X									T																	
		DRIVE # 3			X								T																	
		DRIVE # 4										X	C																	
HEAD LOAD OPTIONS	AUTO HEAD LOAD							X		X																				
	SELECTED HEAD LOAD							X			X																			
	RADIAL HEAD LOAD								X		X																			
IN USE/ DISK CHANGE	IN USE	= PIN 34																			X									
	IN USE	= PIN 4																		X										
	DISK CHANGE	= PIN 34																			X									
DOOR LOCK OPTIONS	DOOR LOCK	IN USE																								X			X	X
		IN USE-FF																										X		X
		SELECT																						X						X
		HEAD LOAD																							X					X
		IN USE + IN USE FF																									X		X	X
		IN USE + SELECT																						X		X			X	
		IN USE + HEAD LOAD																							X	X			X	
		IN USE FF + SELECT																						X				X		
		IN USE FF + HEAD LOAD																							X			X		
		IN USE + IN USE FF + SELECT																						X		X			X	
		IN USE + IN USE FF + HDLD																							X		X		X	
ACTIVITY LED OPTIONS	ACTIVITY LED	HEAD LOAD . READY														X			X											
		DOOR LOCK . READY														X		X												
		HEAD LOAD															X		X											
		DOOR LOCK															X	X												
WRITE PROTECT OPTION	WRITE PROTECT	NOTCH COVERED				X																								
		NOTCH OPEN																												
STEPPER MOTOR	STEP.MOT.ENA	MOTOR ON																						X						
HARD SECTOR OPT.	HARD SECTOR	ENABLED												C	T															

TABLE 3 - 11 : OPTION JUMPER MATRIX

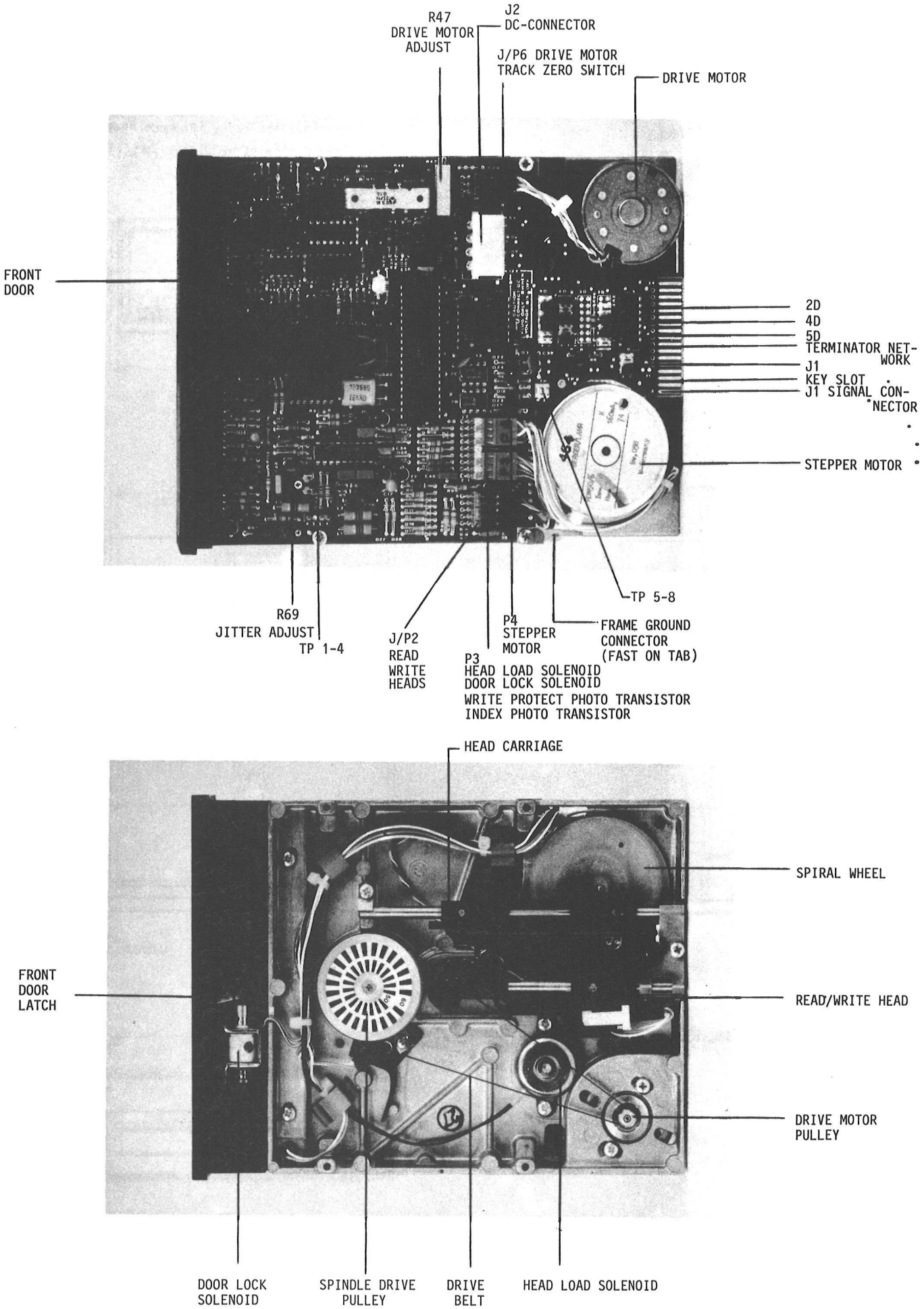


FIGURE 3 - 9 : PART LOCATIONS (PRINCIPAL)

3.1.8. DRIVE MOUNTING

3.1.8.1. MOUNTING POSITIONS

The mini disk drive may be mounted in any position.

3.1.8.2. MOUNTING DIMENSIONS

Figure 3 - 10 shows the outline and mounting dimensions of the mini disk drive. For more detailed information, see specification of the BASF 6106/08 mini disk drives.

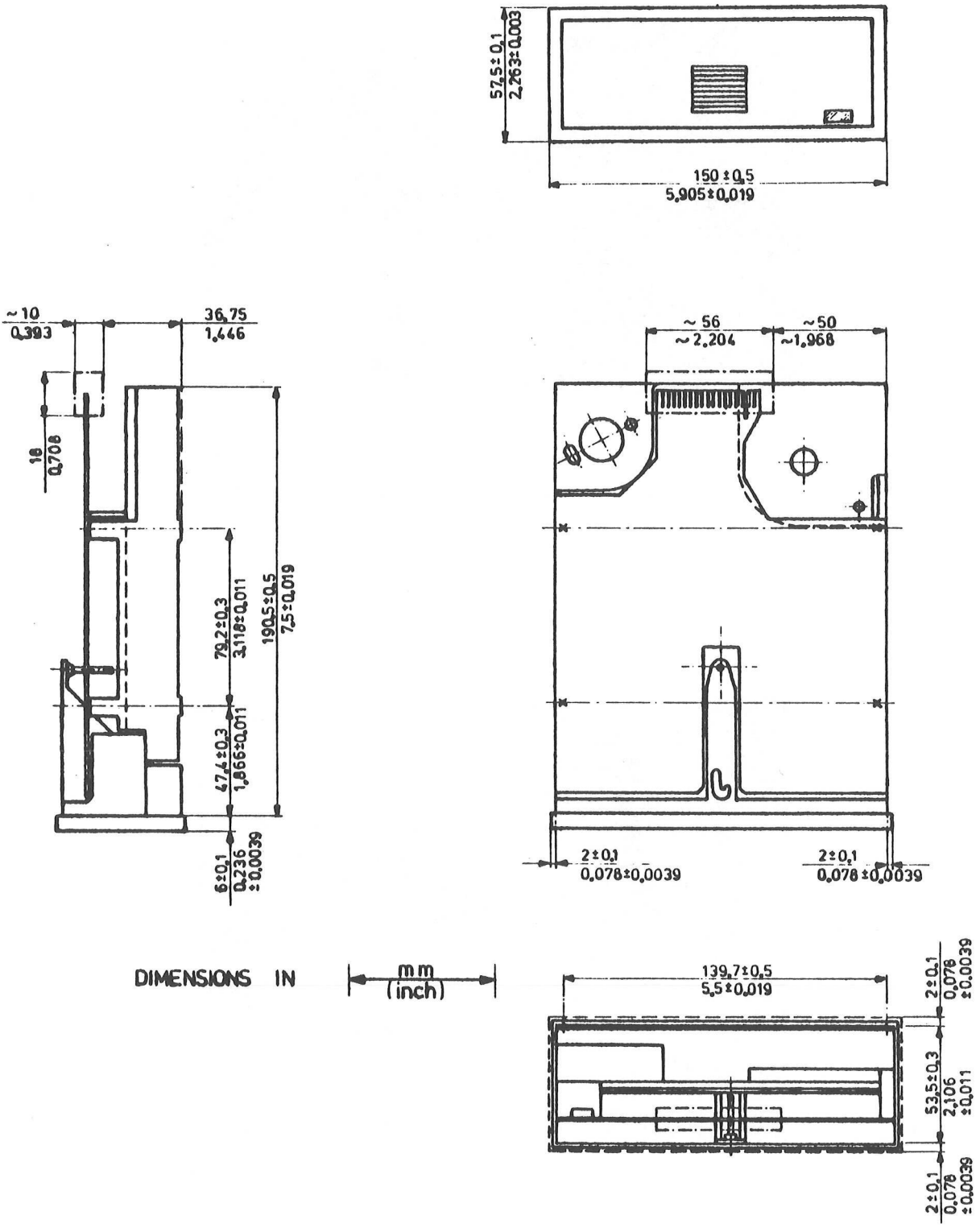


FIGURE 3 - 10 : MOUNTING SPECIFICATION

3.2. OPERATION

3.2.1. GENERAL

There are no front panel controls on the BASF 6106/ 6108. All power and control functions are handled through the interface. Operating procedures consist primarily of loading and unloading the mini disk.

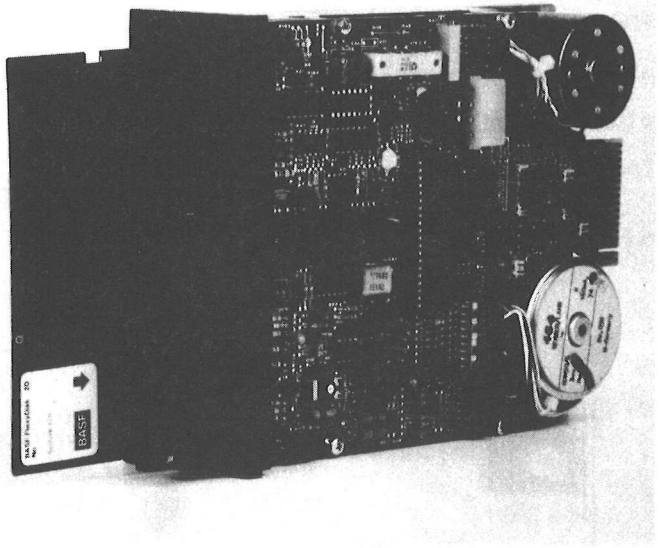
3.2.2. MINI DISK STORAGE AND HANDLING

The following are essential requirements for mini disk storage and handling :

- The mini disk should be stored in an environment that is clean and free from any magnetic influence;
- The mini disk should be in same temperature and humidity environment as the disk drive for a minimum of five minutes prior to use ;
- Return flexy disk to protective envelope when not in use ;
- Never place heavy objects on the mini disk cartridge ;
- Never touch the flexy disk through the cartridge opening when handling ;
- Never attempt to clean the flexy disk ;
- Do not bend of fold the flexy disk ;
- Do not use rubber bands or paper clips on the flexy disk ;
- Never write on cartridge (use labels) ;
- Do not expose flexy disk to excessive heat or sunlight.

Proper loading of the mini disk is vital to the operation of the mini disk and drive. Figure 3-11 shows the proper laoding of the mini disk.

Procedures for loading and unloading the mini disk drive are given in tables 3 - 11 and 3 - 12, respectively.



Caution : insert fully before closing the front door !

FIGURE 3 - 11 : FLEXY DISK LOADING

STEP	ACTION
1	Press front door and release to open
2	Insert Flexy Disk fully with label towards front door
3	Close front door

TABLE 3 - 12 : FLEXY DISK LOADING

STEP	ACTION
1	Press front door and release to open
2	Remove Flexy Disk

TABLE 3 - 13 : FLEXY DISK UNLAODING

3.2.3. WRITE PROTECT

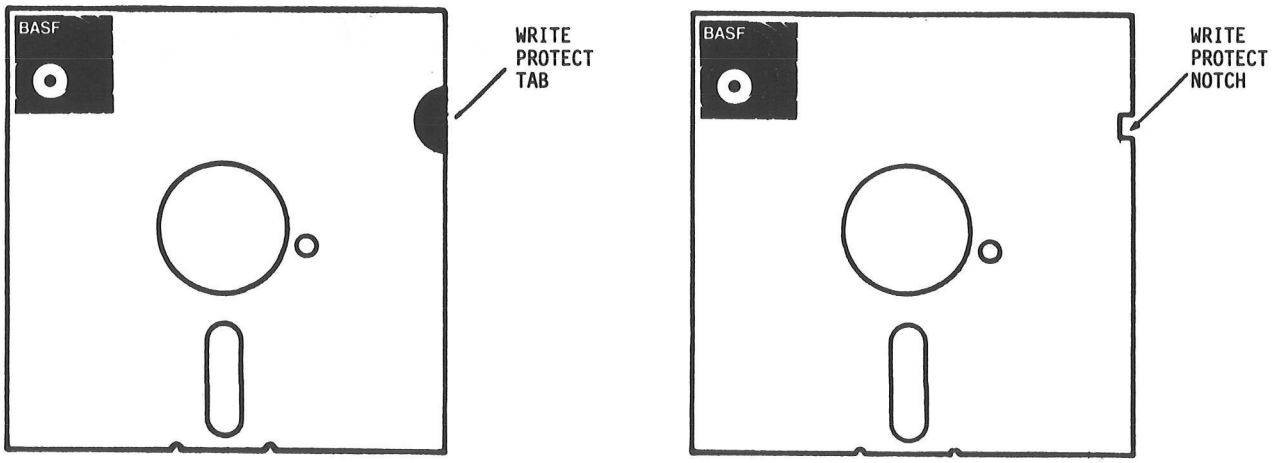
There are two methods used to protect a flexy disk from being written :

a) write protect if notch open (optional)

b) write protect if notch covered (ECMA)

3.2.3.1. WRITE PROTECT IF NOTCH OPEN (OPTIONAL)

Jumper : 2D (1-2) open



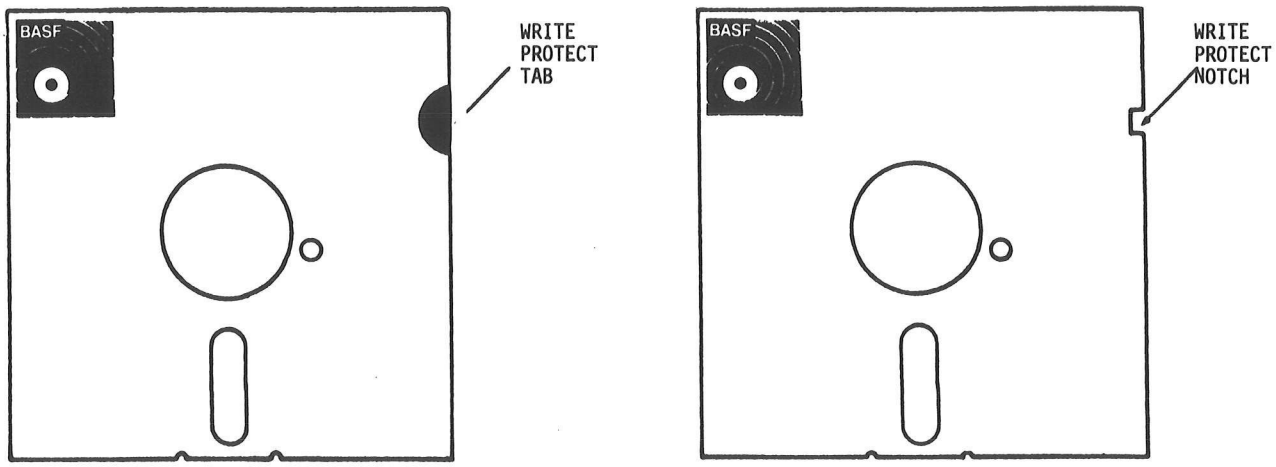
UNPROTECTED

WRITE PROTECTED

FIGURE 3 - 12 : WRITE PROTECT FEATURE (ECMA)

3.2.3.2. WRITE PROTECT IF NOTCH COVERED (ECMA)

Jumper : 2D (1-2)



WRITE PROTECTED

UNPROTECTED

FIGURE 3 - 13 : WRITE PROTECT FEATURE (SHUGART)

SECTION IV.
MAITENANCE

4.1. GENERAL

This section contains the procedures for performing operational checks, alignments and adjustments for the BASF 6106 and BASF 6108 LSI mini disk drives.

4.2. TOOLS AND TEST EQUIPMENT

To perform proper maintenance of the mini disk drive, certain tools, test equipment and supplies are required. A list of standard tools and test equipment is provided in table 4 - 1. Special tools and test equipment are listed in table 4 - 2.

Common hand tools
Freon
Cotton tipped swabs (Q-tips)
Soft lint free cloth (gauze)
Voltohmmeter
Oscilloscope
Inspection Mirror
Frequency Counter

TABLE 4 - 1 : STANDARD TOOLS AND TEST EQUIPMENT

The BASF 2007 exerciser is a portable unit to operate the mini disk drive off-line. The BASF 2007 will enable the user to make all adjustments and checks required on the BASF 6106 and BASF 6108 mini disk drives. The exerciser is provided with controls and indicators to execute all control operations and simulate and read and write operations.

BASF - CE - Mini Disk
BASF - CLEANING Mini Disk
Exerciser BASF 2007
Dial Gauge (Belt Tension Tool)

TABLE 4 - 2 : SPECIAL TOOLS AND TEST EQUIPMENT

4.3. READ/WRITE HEADS CLEANING

a. Read use instructions on the cover of the cleaning disk * ;

b. Turn on drive motor ;

c. Insert cleaning disk and clean head 0 ;

d. Remove cleaning disk after recommended cleaning time ;

6108 only :

e. Insert cleaning disk and clean head 1

f. Remove cleaning disk after recommended cleaning time.

* CAUTION !
Observe the recommended cleaning times !

4.4. CHECKS, ADJUSTMENTS AND REPLACEMENTS

4.4.1. PCB REPLACEMENT

a. Turn off DC voltages ;

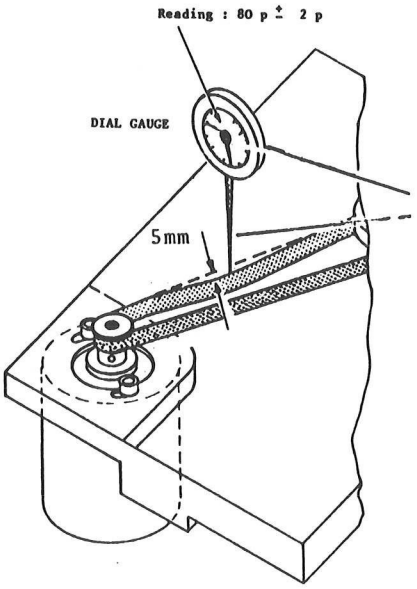
b. Remove P1, P2, P3, P4, P5, P6 ;

c. Remove the 4 mounting screws ;

d. To reinstall, reverse the above ;

e. Check and readjust the index-detector ;

f. Readjust the drive motor speed and jitter, if a new PCB was installed.



4.4.2. SPINDLE DRIVE SYSTEM

The spindle drive system consists of the drive motor, the drive motor pulley, the spindle drive belt and the spindle drive pulley.

4.4.2.1. DRIVE MOTOR AND DRIVE BELT CHECKS

a. Turn off the DC input power ;

b. Rotate drive motor manually and inspect drive belt from wear, cracks or fraying edges. Replace drive belt, if necessary ;

c. Rotate motor manually and inspect for bearing noise or binding. Replace drive motor, if necessary (ref. to drive motor replacement procedure) ;

d. Turn on DC power to mini disk drive ;

e. Start drive motor (MOTOR ON/active) ;

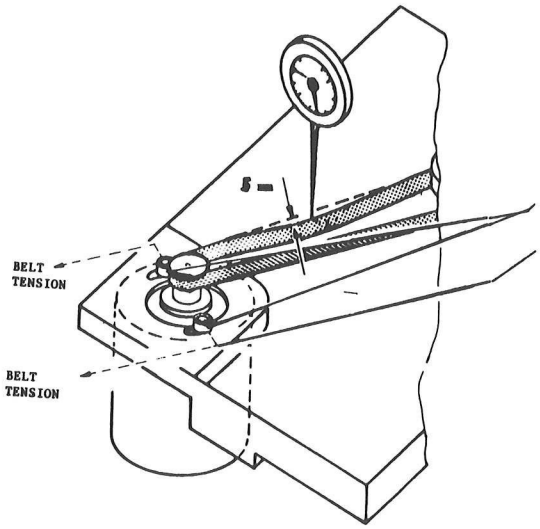
f. Verify that drive motor and drive belt operate normally and that drive belt tracks evenly and smoothly in center of both pulleys.

4.3.2.2. DRIVE BELT TENSION CHECK

a. Take a dial gauge and press it against the drive belt until the deflection of the belt is 5 mm ;

b. The reading on the gauge must be ~80 p +/- 5 p ;

c. If the measured value is out of limits, perform drive belt tension adjustment.



4.4.2.3. DRIVE BELT REPLACEMENT AND TENSION ADJUSTMENT

a. Slightly loosen the drive motor screws ;

b. Adjust the drive belt tension for a reading of 80 p +/- 5 p on the dial gauge, when the drive belt is 5 mm deflected ;

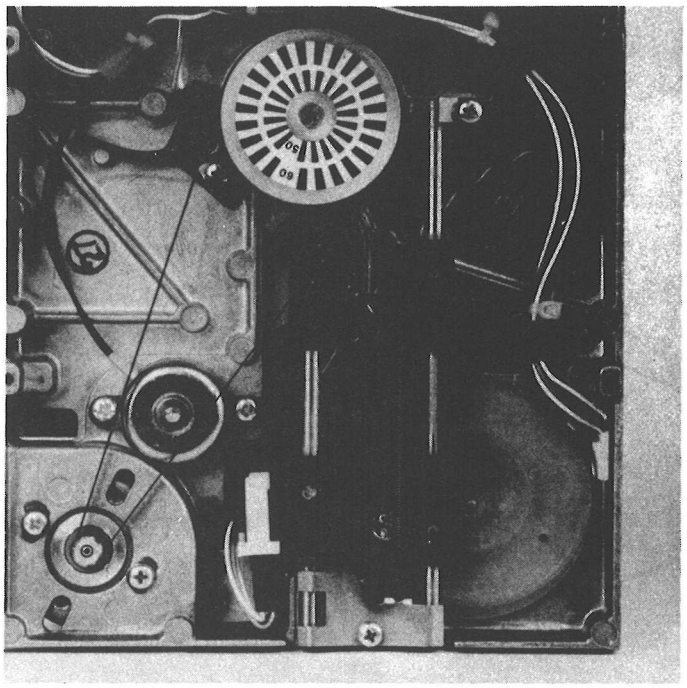
c. Tighten the drive motor setscrews ;

4.4.2.4. DRIVE MOTOR SPEED CHECK

a. Load a BASF CE-mini diskette ;

b. Turn on drive motor ;

c. Check that the dark lines of the tacho disk on the spindle pulley appear motionless. Use the inside ring for 50 Hz and the outside ring for 60 Hz *) ;



4.4.2.5. DRIVE MOTOR SPEED ADJUSTMENT

a. Load a BASF CE-mini diskette ;

b. Turn on drive motor ;

c. Position to track 16 and load head ;

d. Turn the potentiometer R 47 until the dark lines of the tacho disk on the spindle pulley appear motionless. Use the inside ring for 50 Hz and the outside ring for 60 Hz *).

*) This adjustment is only possible in an area where flourescent light exists. Otherwise, provide the adjustment or check as shown in 4.4.2.6.

4.4.2.6. DRIVE MOTOR SPEED ADJUSTMENT USING A FREQUENCY COUNTER

a. Load a BASF CE-mini diskette ;

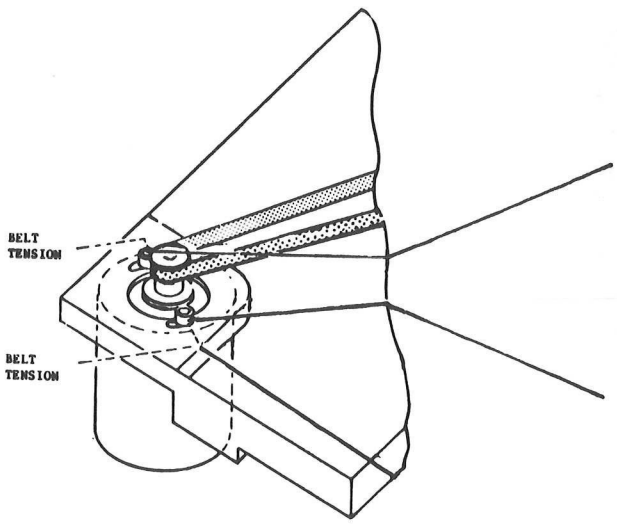
b. Connect a frequency counter to TP8 (INDEX) ;

c. Turn on the drive motor ;

d. Position to track 16 and load head ;

e. Measure time between two consecutive index pulses and adjust pot R 47 to 200 msec +/- 1 msec if necessary.

4.4.2.7. DRIVE MOTOR REPLACEMENT



a. Remove mini disk drive from mounting and place it on a clean work surface ;

b. Remove drive belt ;

c. Remove wire 2 and 4 of P6 ;

d. Remove the two drive motor set screws. Drive motor is now removed from disk drive ;

e. Place new drive motor in same position and fasten it snuggly. Tighten drive motor set screws ;

f. Reinstall wires 2 and 6 of P6 ;

g. Install drive belt and verify correct tracking ;

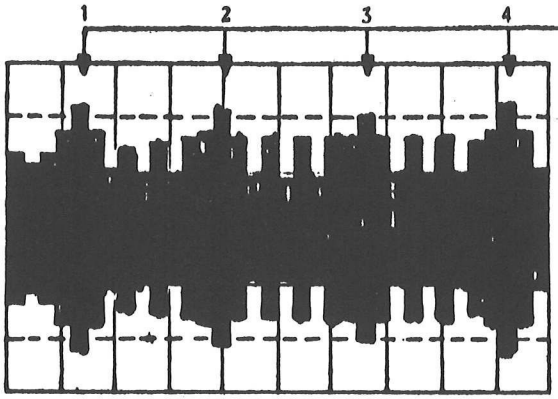
h. Provide drive belt tension adjustment procedure (4.4.2.3.) ;

i. Perform speed adjustment.

4.4.3. POSITIONING SYSTEM

The positioning system consists of the stepper motor with spiral wheel, the head carriage assembly and the optical track 00 switch.

4.4.3.1. TRACK ADJUSTMENT CHECK



a. Load a BASF-CE mini diskette ;

b. Start the drive motor and select the mini disk drive ;

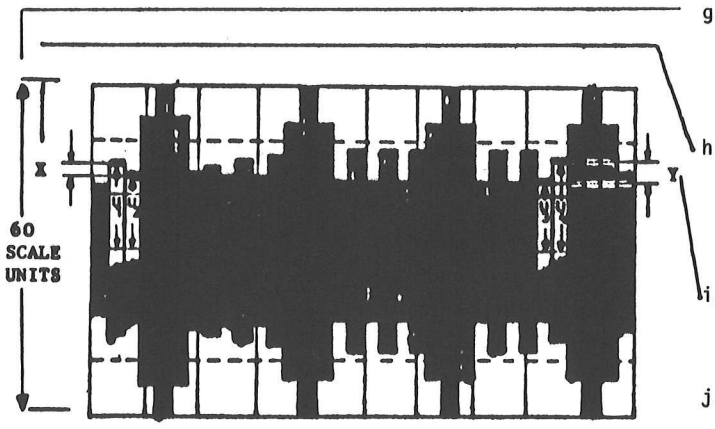
c. Select head 0 ;

d. Step to track 16 ;

e. Measure with oscilloscope :

SYNC	:	EXT. POS. TP 8 INDEX
CH 1	:	AC 50 mV uncalibrated inverted TP 1
CH 2	:	AC 50 mV uncalibrated TP 2
MODE	:	ADD
TIME BASE:		10 ms/Div. uncalibrated

f. Monitor the read signal on the screen and adjust the time base of the scope until four orientation bursts are shown ;



g. Turn the variable gain potentiometer of the scope until the amplitude of the orientation burst reaches 60 scale units ;

h. Determine X and Y (see example !) :
$X = U_1 - U_2$ Caution : pay attention to sign
$Y = U_3 - U_4$

i. Calculate Z :
$Z = X + Y$

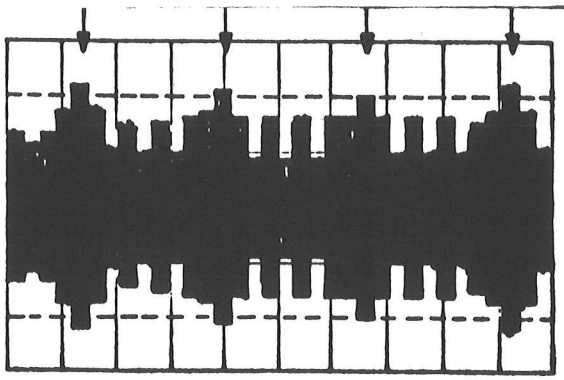
j. If Z exceeds 18 scale units, proceed with point f of track adjustment procedure (4.4.3.2.). Continue for BASF 6108 (1 DIV = 10 SCALE UNITS) ;

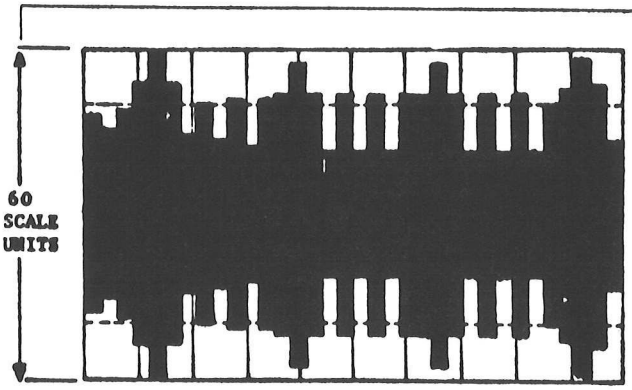
k. Select head 1 ;

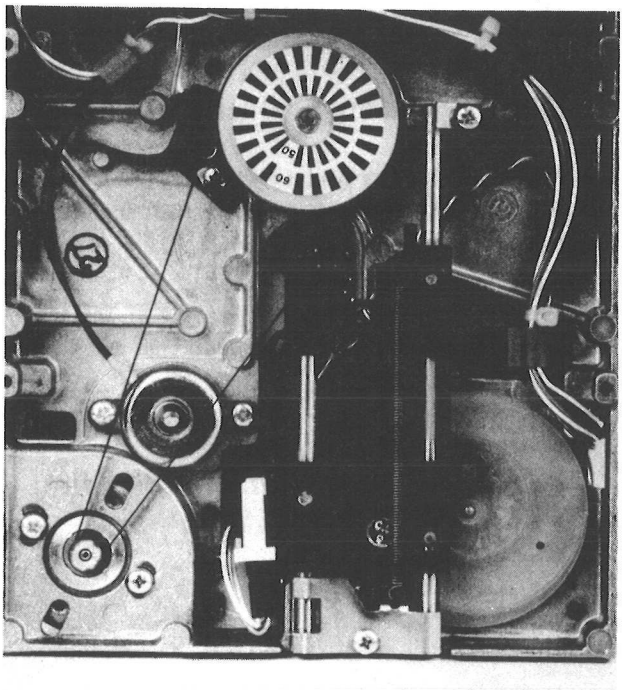
l. Proceed through point f to i for head 1 ;

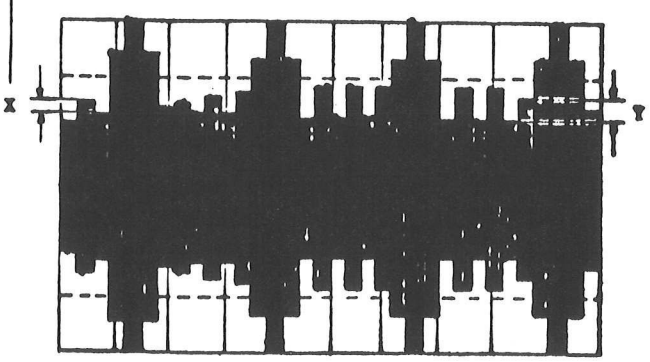
m. If Z exceeds 18 scale units, proceed with point f of track adjustment procedure (4.4.3.2.). If Z is lower than 21 scale units, the track adjustment is o.k.

EXAMPLE:
$X = U_1 - U_2 = +2$ scale units
$Y = U_3 - U_4 = -4$ scale units
$Z = X + Y = +2 - 4 = -2$ scale units









4.4.3.2. TRACK ADJUSTMENT PROCEDURE

a. Load a BASF CE-mini diskette ;

b. Start the drive motor and select the mini disk drive ;

c. Select head 0 ;

d. Step to track 16 ;

e. Measure with oscilloscope :

SYNC	:	EXT. POS. TP 8 INDEX
CH 1	:	AC 100 mV uncalibrated inverted TP 1
CH 2	:	AC 100 mV uncalibrated TP 2
MODE	:	ADD
TIME BASE	:	10 msec/Div. uncalibrated

f. Loosen the mounting screws of the stepper motor and rotate body of the stepper motor until the maximum amplitude of the orientation bursts is reached ;

g. Monitor the read signal on the screen and adjust the time base of the scope until four orientation bursts are shown ;

h. Turn the variable gain potentiometer until the amplitudes of the orientation bursts reach 60 scale units ;

i. Rotate the body of the stepper motor until X and Y have the same value, but opposite sign, or both are zero ;

j. Tighten the mounting screws of the stepper motor ;

k. Recheck the adjustment. If X and Y exceed 4 scale units, readjust the stepper motor (pay attention to sign !) ;

l. For BASF 6106, perform track zero switch adjustment check ;

For BASF 6108 :

m. Select head 1 and begin with d. until f.

n. Provide points g. and h. for head 1 ;

o. Measure X + Y. It must be less than 4 scale units. Readjust, if necessary ;

p. Check the adjustment from head 0, if X + Y is lower than 10 scale units ;

q. Perform track zero switch adjustment check (4.3.3.3.).

4.4.3.3. ADJUSTMENT CHECK FOR OPTICAL TRACK ZERO SWITCH

a. Select mini disk drive and start drive motor ;

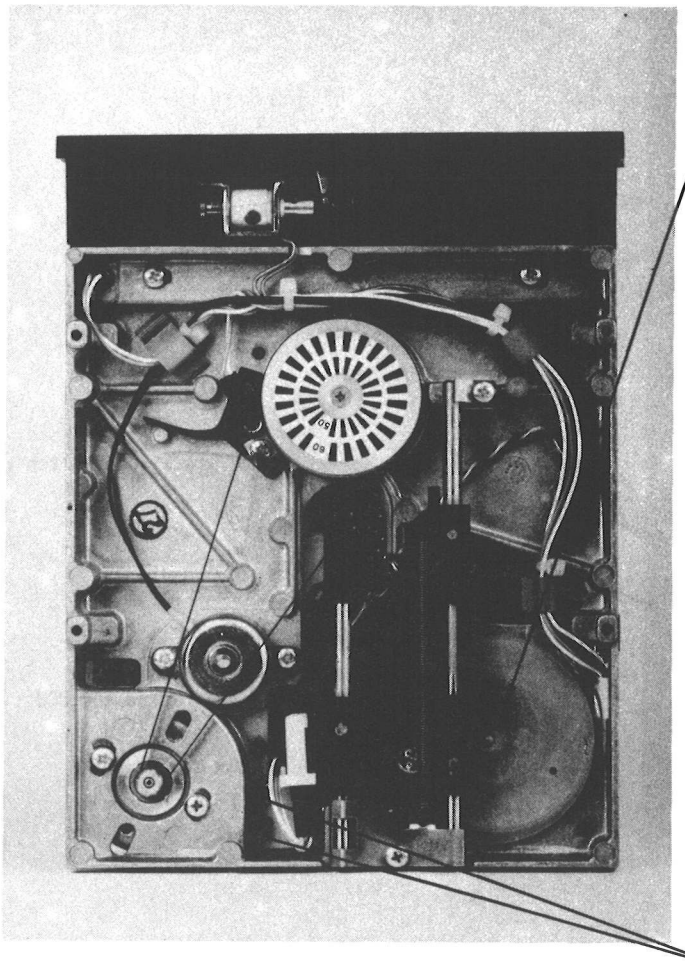
b. Monitor TP 6 (TRACK ZERO SWITCH) :

SYNC : AUTO
CH 1 : 2 V/Div. TP 6)
MODE : CH 1 only
TIME BASE : 10 msec/Div.

c. Step out to track 0 ;

d. Check space between head carriage and outer stop for 2,5 mm.
If the space is not correct, provide track zero switch adjustment ;

e. Check if track zero switch closes (TP 6 low) between track 3 and 2 when stepping towards track zero and opens (TP 6 high) between tracks 2 and 3 when stepping from track 0 to track 4. If the track zero switch will not change within these limits, provide track zero switch adjustment.



4.4.3.4. ADJUSTMENT FOR OPTICAL TRACK ZERO SWITCH

a. Load BASF flexy disk ;

b. Select mini disk drive and start drive motor ;

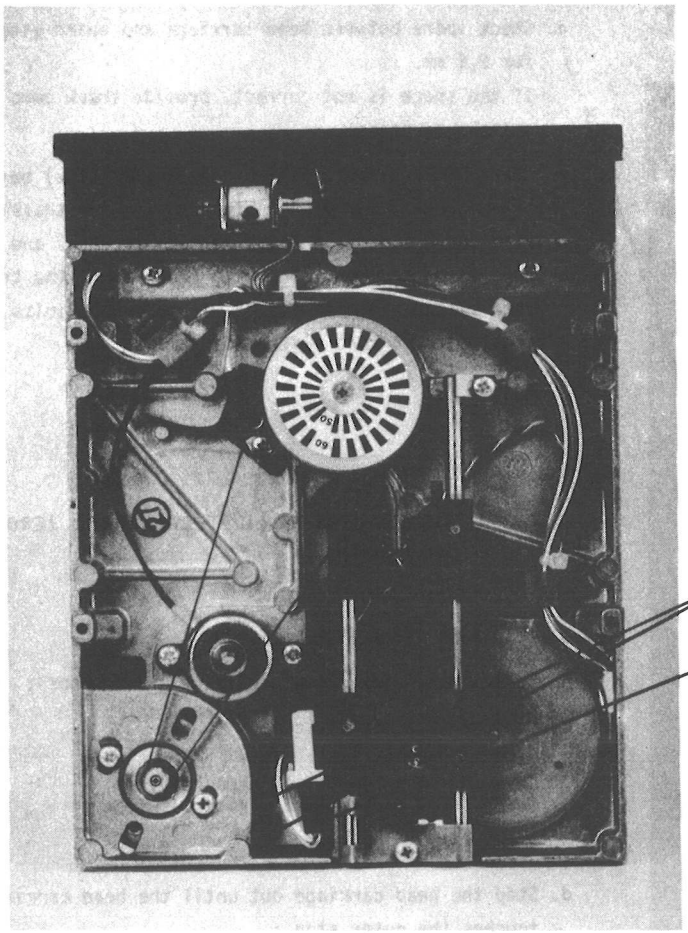
c. Measure with oscilloscope :

SYNC : AUTO
CH 1 : 2 V/Div. ID-13 (track 00)
CH 2 : 2 V/Div. TP 6 (Track 0-switch)
MODE : chopped
TIME BASE: 10 msec/Div.

d. Step the head carriage out until the head carriage touches the outer stop ;

e. Step in until CH 1 goes high (normally one step in). Now the head carriage is positioned at track 0 ;

f. Loosen the track 0 switch and adjust it that it will close (TP 6 : high → low) between tracks 3 and 2 when the head carriage is moved towards track 0 and will open (TP 6 : low → high) between tracks 2 and 3 when the head carriage is stepped from track 0 to track 4.



4.4.3.5. TRACK ZERO SWITCH REPLACEMENT

Optical track zero switch :

a. Turn off all DC input power ;

b. Remove PCB ;

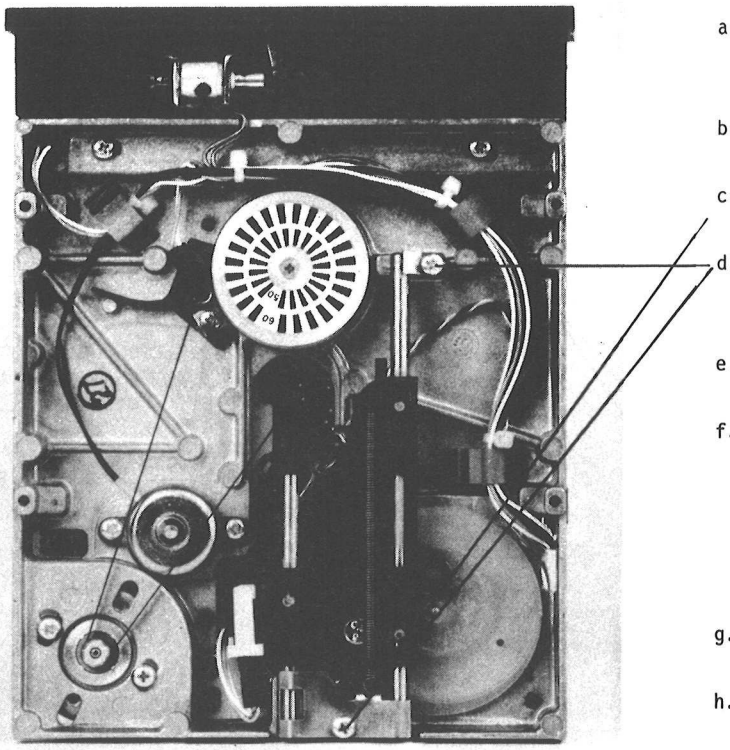
c. Remove holding screws of the track zero switch ;

d. Disconnect the track zero switch ;

e. Connect the new track zero switch ;

f. Install the new track zero switch and the PCB ;

g. Provide the track zero switch adjustment.



4.4.3.6. HEAD CARRIAGE REPLACEMENT

a. Remove mini disk drive from mounting and place it on a clean working surface ;

b. Disconnect P 2.1 (2.2) ;

c. Disengage the spring ;

d. Loosen the two holding screws and take out the carriage with the guide bars carefully ;

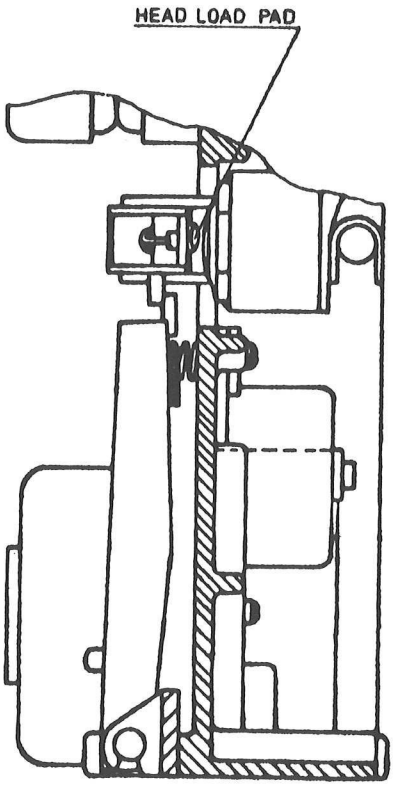
e. Pull out the guide bars from the R/W head carriage ;

f. To reinstall the new head carriage, reverse the above procedure ;

CAUTION : Handle spring carefully during reinstallation

g. Provide the track adjustment accordingly (4.4.3.2.) ;

h. Check the track zero switch adjustment (4.4.3.3.).



4.4.3.7. HEAD LOAD PAD REPLACEMENT
(BASF 6106 ONLY !)

a. Remove the PCB (4.3.1.) ;

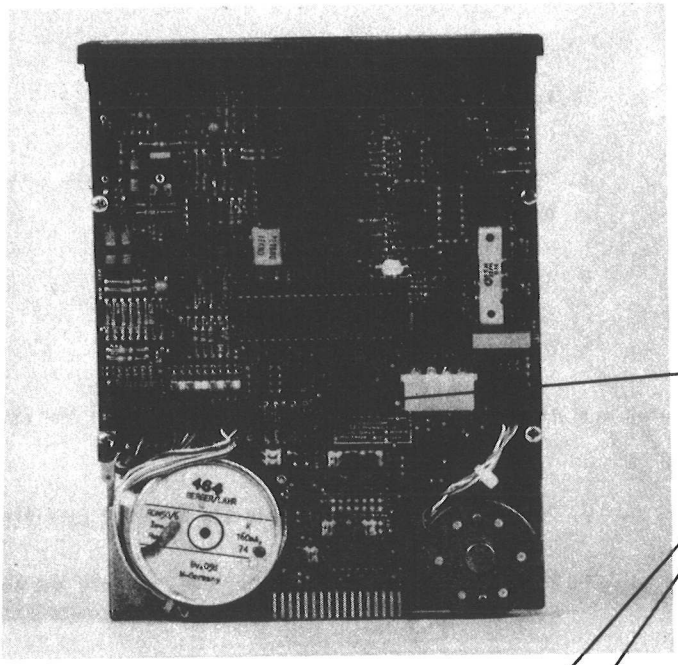
b. Remove the old head load pad ;

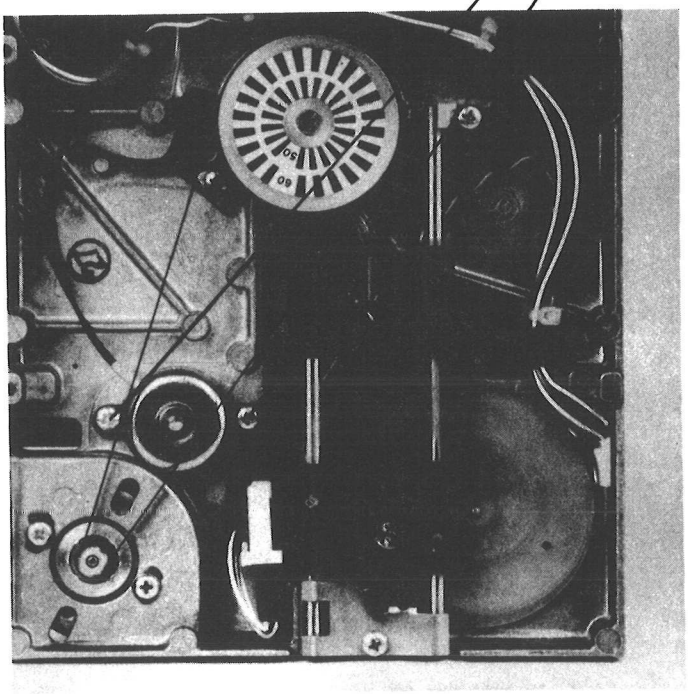
c. Install the new head load pad ;

d. Install the PCB ;

e. Check the jitter adjustment (4.4.5.1.) ;

f. Index adjustment.





4.4.4. HEAD LOAD MECHANISM

4.4.4.1. HEAD LOAD SONELOID REPLACEMENT

a. Remove mini disk drive from mounting and place it on a clean working surface ;

b. Extract wires 1 and 3 from connector P3 ;

c. Loosen the two holding screws and remove the head load solenoid ;

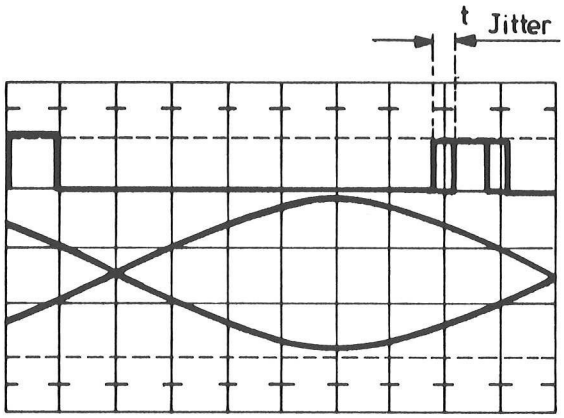
d. To reinstall the head load solenoid, reverse the above ;

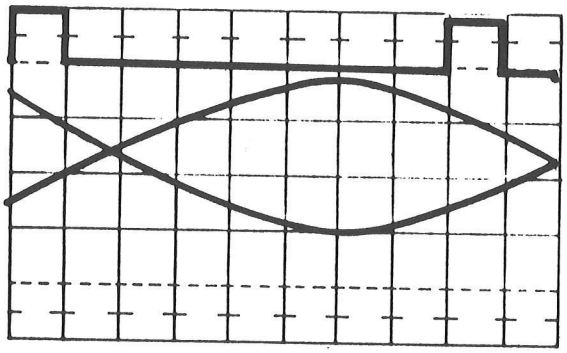
e. Check the airgap between head load actuator and the pin on the head load pressure arm for 0.3 to 1 mm.

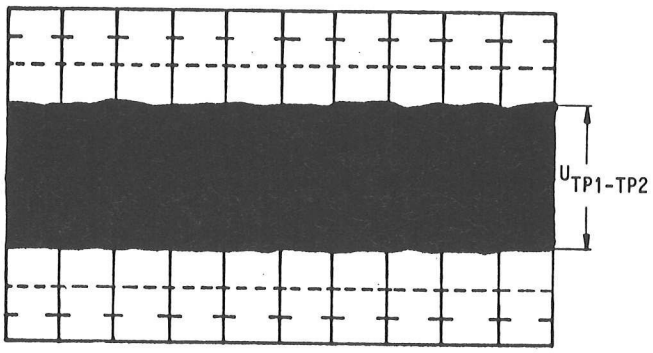
4.4.4.2. HEAD LOAD ACTUATOR CHECK

a. Load the head ;

b. The clearance between the head load actuator and the pin on the head load pressure arm should be between 0.3 mm and 1 mm.







4.4.5. READ/WRITE ELECTRONICS

4.4.5.1. JITTER CHECK AND ADJUSTMENT

a. Load a BASF flexy disk ;

b. Turn on drive motor ;

c. Step to track 39 ;

d. Write all FM-ZEROS (1F) for BASF 6106 (head 0), for BASF 6108 (head 0 and 1) ;

e. Measure with oscilloscope :

SYNC	: INT.	POS.	CH 1
CH 1	: DC	2V/Div.	TP 5 READDATA
CH 2	: AC	50 mV/Div.	TP 1
TRIGGER	: Read data		

f. Trigger oscilloscope, that the read data signal "cateyes" are displayed ;

g. Measure jitter. If jitter of head 0 or head 1 (track 39, 1F) is $\geq$ 500 ns, adjust pot R 69 ;

- for minimum jitter at BASF 6106
- for best compromise between jitter of head 0 and head 1 for BASF 6108.

4.4.5.2. READ AMPLITUDE CHECK

a. Load a BASF flexy disk ;

b. Turn on drive motor ;

c. Step to track 39 ;

d. Select head 0 ;

e. Write all "ones" ;

f. Measure with oscilloscope :

SYNC	: EXT. POS. TP 8 INDEX
CH 1	: AC 50 mV/Div. inverted TP 1
CH 2	: AC 50 mV/Div. TP 2
MODE	: ADD
TIME BASE	: 20 msec/Div.

g. Check the measured read voltage at TP 1-TP 2 for the following limits :

$$U_{TP1-2} \geq 70 \text{ mVpp}$$

Continue for BASF 6108 !

h. Select head 1 ;

i. Write all "ones" ;

j. Check the measured read voltage at TP1-TP2 for the following limits :

head 0 $U_{TP1-2} \geq 70$ mVpp

head 1 $U_{TP1-2} \geq 70$ mVpp

4.4.6. PHOTO TRANSISTORS AND LED'S

4.4.6.1. PHOTO TRANSISTOR REPLACEMENT

a. Disconnect plug of defective photo transistor ;

b. Remove photo transistor ;

c. Insert new photo transistor ;

d. Reconnect plug ;

e. Check the function of the photo transistor ;

f. Provide the index detector adjustment, if the index photo transistor has been changed.

4.4.6.2. LED REPLACEMENT

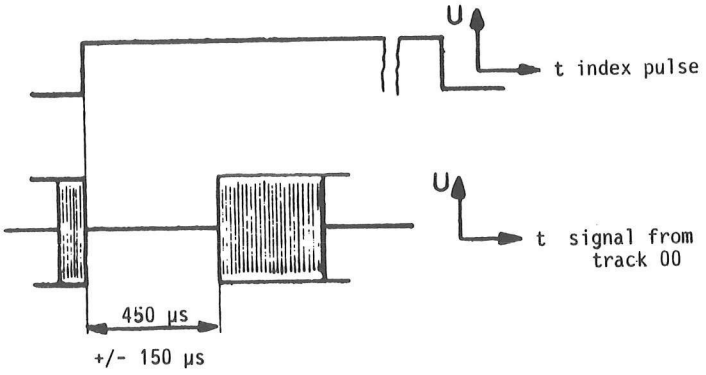
a. Remove the LED from PCB board ;

b. Put in the new LED ;

c. Check the function of the LED ;

d. Provide the index detector adjustment.

4.4.6.3. INDEX DETECTOR ADJUSTMENT CHECK



The tracks 00 are prewritten with 1F containing an index alignment gap at the beginning of track.

The index sensor is aligned properly when the beginning of the gap is time-coincident with the leading edge of index pulse (see figure to the left).

a. Load a BASF CE-mini disk ;

b. Select head 0 ;

c. Start the drive motor and select the mini disk drive ;

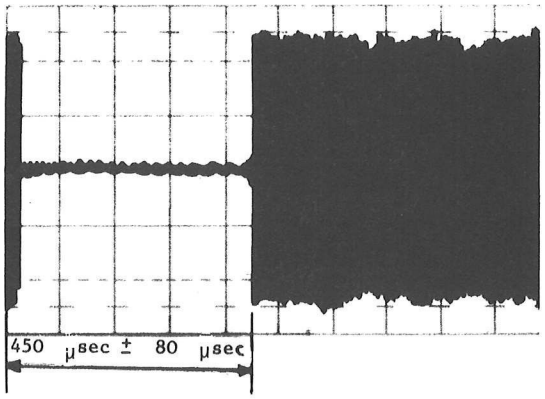
d. Step to track 0 ;

e. Measure with oscilloscope :

SYNC	:	INT. POS. CH 1
CH 1	:	DC 2V inverted TP 8 (index)
CH 2	:	AC 100 mV TP 1 (read data)
TIME BASE:		100 µsec/Div.

f. Check the timing between start of the sweep and the data burst for 450 µsec +/- 150 µsec ;

g. Provide the index detector adjustment (4.4.6.4.) if necessary.



4.4.6.4. INDEX DETECTOR ADJUSTMENT

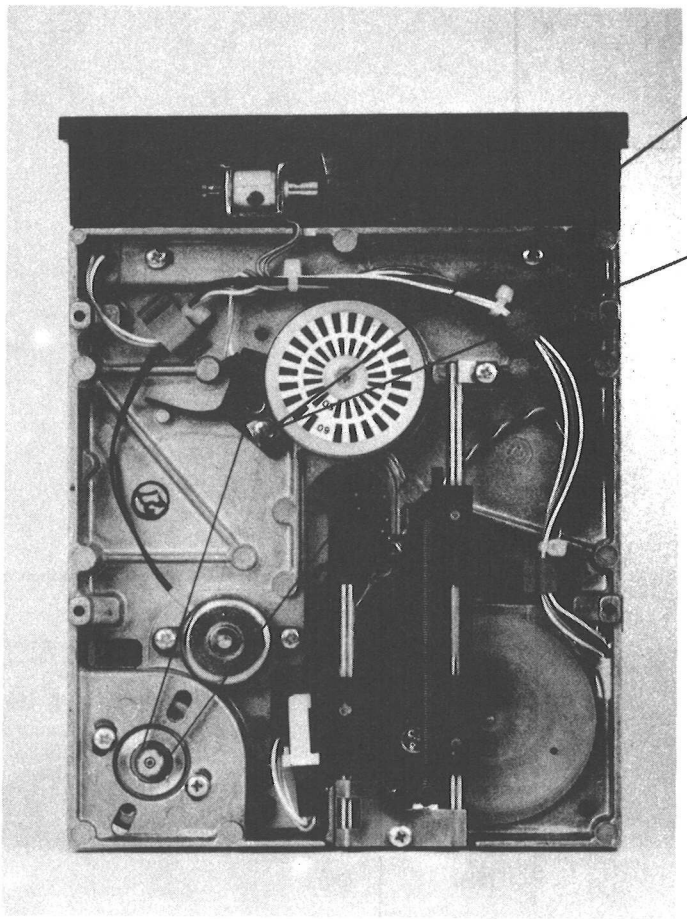
a. Load a BASF CE flexy disk ;

b. Start the drive motor and select the mini disk drive ;

c. Step to track 0 ;

d. Measure with oscilloscope :

SYNC	:	EXT.POS. TP8 INDEX
CH 1	:	AC 50 mV inverted TP 1
CH 2	:	AC 50 mV
MODE	:	100 µsec/div.
TIME BASE	:	100 µsec/div.

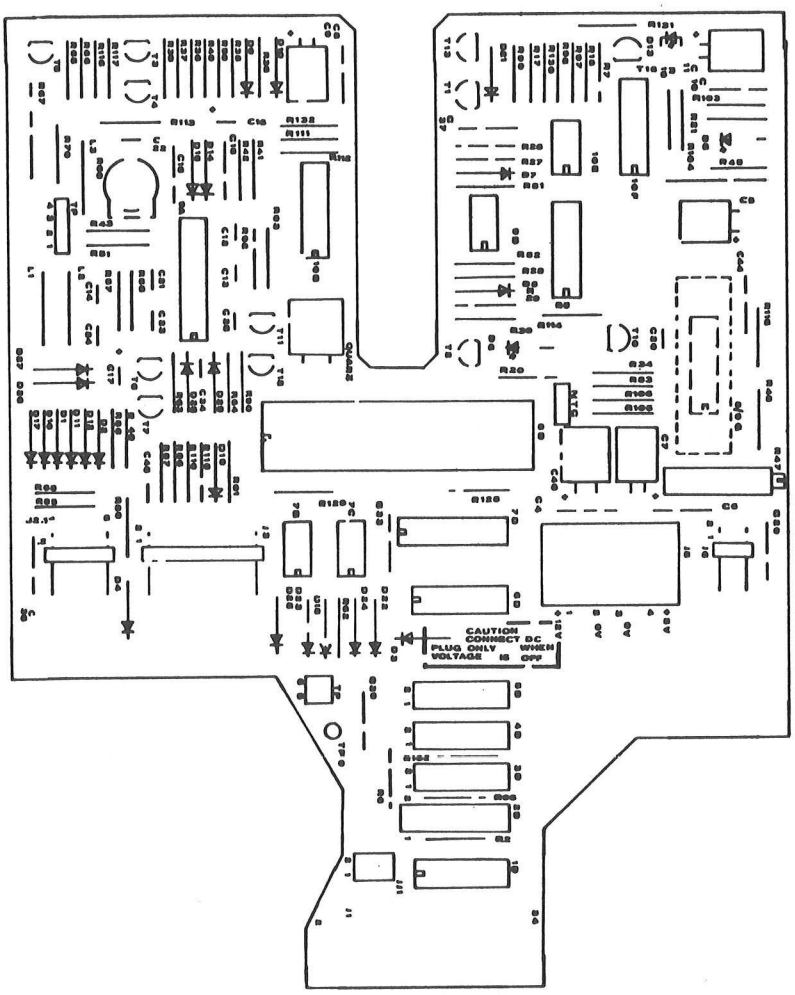


e. Loosen the set screw of the index holder ;

f. Adjust the time delay between start of the sweep and the data burst to 450 µsec +/- 80 µsec ;

g. Tighten the index holder set screw.

4.5. LOCATION OF TESTPOINTS, IC's, POTENTIOMETERS AND CONNECTORS



POTI	FUNCTION
R 47	Drive motor adjust
R 69	Jitter adjust

CONNECTOR		FUNCTION
J 1		Signal - Interface
J 2		Read/write - head(s)
J 3	1, 3	Head load solenoid
	2, 4	Door lock solenoid
	5, 6	Write protect phototransistor
	7, 8	Index phototransistor
	11, 18	Stepper motor
J 5		DC - connector
J 6	2, 4	Drive motor
	3,5,6,7	Track zero optical switch

TEST POINTS	SIGNAL
TP 1, 2	Read signal (differentiator input)
TP 3	GND
TP 4	Jitter voltage
TP 5	Read data
TP 6	GND
TP 7	GND
TP 8	Index
TP 9	GND

APPENDIX D

EXORSET 33/100 POWER SUPPLY DESCRIPTION

EXORset 33/100 Switching Power Supply

The quadruple power supply is of the secondary switching type. It contains a ring core mains transformer with very low magnetic radiation. To prevent interference, the mains input is supplied with a VDE-tested anti-interference filter together with a built-in fuse and spare fuse. All components and the assembled unit meet VDE requirements.

The power supply can be switched from 220 V to 110 V. Just unscrew the upper cover (3 cylindrical screws M3 x 6) and change the soldering of the solder strap shown on the silkscreen. (Recommended is a Cu-Si-wire of min. 0.5 mm Ø.)

The output voltages of + 5 V, + 12 V, and CRT + 12 V can also be adjusted on the assembled unit by approximately $\pm$ 20 %.

The power supply is mounted in the EXORset with M4 rivet nuts and M4 holes at the back (see mechanical drawing).

Specification

Input Voltage	220 VAC + 20 % / - 15 % mains supply; 47 - 60 Hz Internal supply selection with soldered jumper to 110 VAC + 20 % / - 15 %
Output Voltages	110 VAC transformer tapping for connection of fan

DC Voltages:

U_1 = + 5 V / 10 A

U_2 = -12 V / 0.5A U_1, U_3 + U_4 with potentiometer adjustable by $\pm$ 20%

U_3 = 12 V / 4 A

U_4 = +12 V / 1.2 A for 9" CRT

U_5 = 25 VAC for 12 " CRT

Output Currents

U_1 : I_{nom} = 10 A, I_{max} = 10.5 - 11.5 A,
I_k = 3.5 $\pm$ 0.5 A

U_2 : I_{nom} = 0.5 A, I_{max} = 0.6 A,
I_k = 0.6 A

U_3 : I_{nom} = 4 A, I_{max} = 4.2 - 4.8 A,
I_k = 2.5 $\pm$ 0.5 A

U_4 : I_{nom} = 1.2 A, I_{max} = 1.3 - 1.5 A,
I_k = 1.3 - 1.5 A

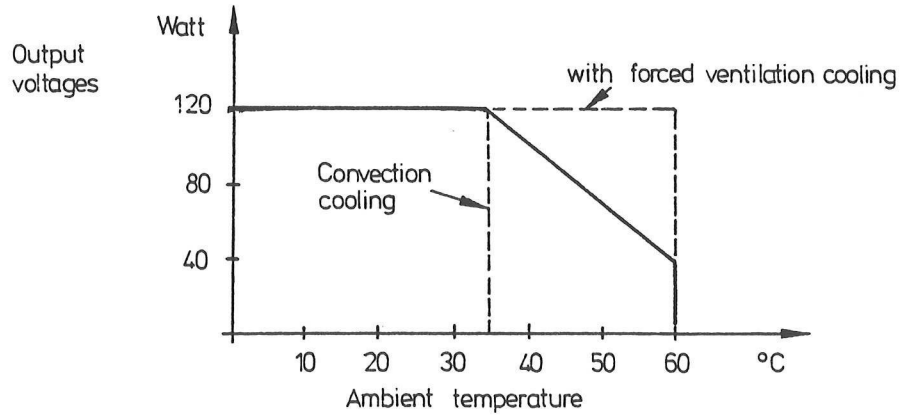
U_5 : I_{nom} = 1.2 A eff

- I_k is short circuit current

- outputs U_1 - U_4 are short-circuit-proof.
  U_1 and U_3 with foldback characteristic

Noise and Ripple	$U_1 < 40\ mV_{pp}$ $U_2 \leq 50\ mV_{pp}$ $U_3 < 50\ mV_{pp}$ $U_4 < 50\ mV_{pp}$
Overvoltage Protection	U_1: + 6.0 V $\pm$ 0.4 V U_3: + 14.5 V $\pm$ 1.0 V
Sense Line	U_1
Line Regulation	Power, 220 VAC + 20 % - 10 %, all voltages 0.3 % load
Load Regulation	Full load, no-load, U_1, U_3 + U_4 0.5 %, U_2 1 %
Regulation Timing	Load change 50 % to 100 % causes DC voltage change of typically 1 %. This is corrected back to nominal value within less than 2 ms
Temperature Coefficient	0.3 °/oo / °C

Operating Temperature	0° C to +60° C (see temperature characteristic curve)



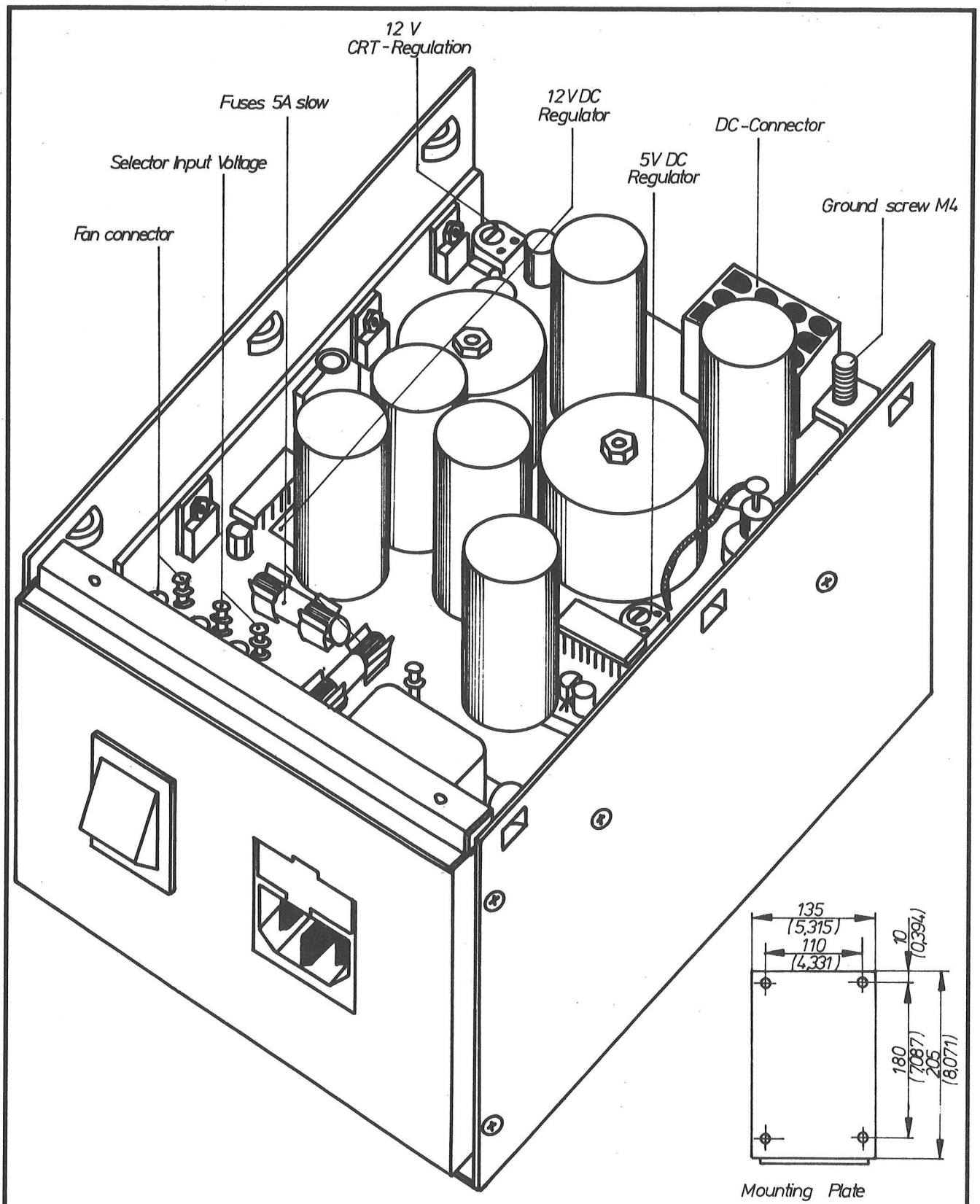
Storage Temperature	- 20° C to + 85° C
Power Fail Protection	10 ms at full load
Current Surge upon Power on	Less than 25 A
Isolation Voltage	Any Input to any Output 2500 VAC
Vibration	Sine 10 - 250 Hz, acceleration 2g
Shock	Half-Sine, 10 ms, acceleration 50g

BILL of MATERIAL

Switching Power Supply EXORset 33/100

R1	2k	SK2	R33	500 Keramik Poti	
R2	2k	MK2	R34	1k	SK2
R3	2.2k		R35	18k	SK2
R4	3k	MK2	R36	0.02 Ohm	
R5	16k	MK2	R37	1.5 "	SK2
R6	470 Ohm	SK2	R38	10k	MK2
R7	220 Ohm 1/2 W	SK2	R39	2.2k	MK2
R8	27k	SK2	R40	20 Ohm	SK2
R9	5.1k	MK2	R41	1 Ohm	SK2
R10	5.1k	MK2	R42	1 Ohm	SK2
R11	1k	SK2	R43	1 Ohm	SK2
R12	200k	SK2	R44	9.1 Ohm	MK2
R13	Poti 500 Ohm Keramik		R45	2.2k Keramik Poti	
			R46	3k	MK2
R14	1k	SK2	R47	5.1 Ohm	SK2
R15	7.5k	SK2	R48	150 Ohm	SK2
R16	0.02 Ohm		R49	300 Ohm	SK2
R17	1.5k	SK2			
R18	3k	MK2			
R19	2.2k	MK2	C1	4.700µ/40V standing	
R20	20 Ohm	SK2	C2	-	
R21	20 "	SK2	C3	4.700µ/40V	"
R22	2k	MK2	C4	2.200µ/25V	"
R23	2.2k Keramik Poti		C5	10µ/35V	Tant.
R24	3k	MK2	C6	2.2n/100V	foil
R25	-		C7	2.2n/100V	"
R26	820 Ohm	SK2	C8	2.2n/100V	"
R27	330 Ohm 1/2 W	SK2	C9	47n/50V	cer.
R28	27k	SK2	C10	10n/100V	foil
R29	8.2k	MK2	C11	4.700µ/40V standing	
R30	2.2k	MK2	C12	47n/50V	cer.
R31	1k	SK2	C13	1.000µ/16V standing	
R32	300k	SK2	C14	2.2n/50V	cer.

C15	10µ/35V Tant.	T1	BC 182 (BC547B)
C16	47µ/25V standing	T2	BDX 34B
C17	0.22µ/63V foil	T3	BDX 34B
C18	0.22µ/63V foil	T4	BDX 34B
C19	4.700µ/40V standing		
C20	10µ/35V "		
C21	2.2n/50V cer.	Th1	TIC 116 D
C22	2.2n/100V foil	Th2	TIC 116 D
C23	470p/50V cer.		
C24	47n/50V "		
C25	10n/50V "	IC1	µA 7912
C26	4.7n/100V foil	IC2	SG 3524 N
C27	4.700µ/40V standing	IC3	MC 3458
C28	10n/50V cer.	IC4	MC 3423
C29	2.200µ/25V standing	IC5	SG 3524N
C30	47µ/25V "	IC6	L 200
C31	47µ/25V "	IC7	MC 3423
C32	0.22µ/63V foil		
C33	2.2n/50V cer.		
C34	10µ/35V Tant.	Dr.1	5V/10A coil
C35	0.22µ/63V foil	Dr.2	12V/ 4A "
		Dr.3	12V/ 1A "
D1	KBPC 25-04 (10A)		
D2	ZPD 18	Si1	M2A fuse
D3	B250C 1500	Si2	T5A "
D4	1N5830	Si3	T5A "
D5	ZPD 4.3		
D6	1N4002		
D7	B250 C1500	Tr.	Transformer BV 14.0481/1
D8	1N3882		
D9	ZPD 4.3		
D10	1N4002		



Mounting Plate

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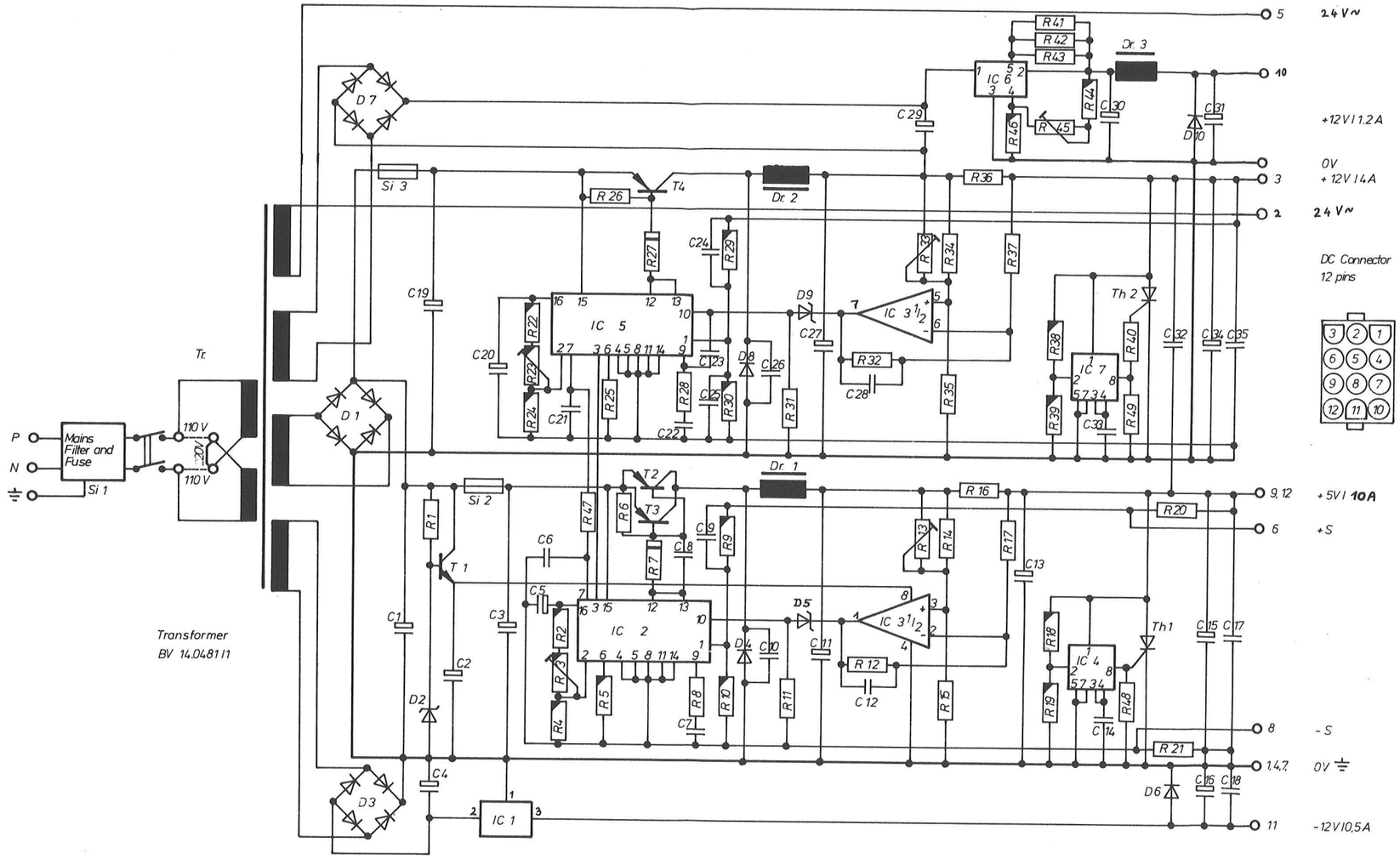
DIMENSIONS: MM (INCHES)			
SCALE		EXOR set 33 / 100 Power Supply	
REMOVE ALL BURRS AND SHARP EDGES: SURFACE QUALITY IN MICROMETER	DRAWN BY: Thumer / 6 — DATE: Mai '82		
TOLERANCE. 2 PLACE DEC ± : HOLES: 3 PLACE DEC ± : ANGLES:	CHECKED BY: M. Schaefer — 12.5.82		
	ENGINEER: M. Schaefer — 12.5.82	DRAWING: 01AG4040M	ISSUE 'B'
BM:	MANAGER: Hajek — 18.5.82		SHEET 1 OF 1

GVO Bestell-Nr. 51.6006



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DIMENSIONS: MM (INCHES)		
SCALE:		TITLE: EXORset 33/100 Power Supply
REMOVE ALL BURRS AND SHARP EDGES / SURFACE QUALITY IN MICROMETER	DRAWN BY: Thumer /6 — DATE: Mai '82	
TOLERANCE: 2 PLACE DEC.= ± HOLES ± 3 PLACE DEC.= ± ANGLES ±	CHECKED BY: M. Schaefs — 12.5.82	DRAWING NO. 63CG4040M ISSUE 'B'
BM:	ENGINEER: M. Schaefs — 12.5.82	SHEET: 1 OF: 1
	MANAGER: — 13.5.82	