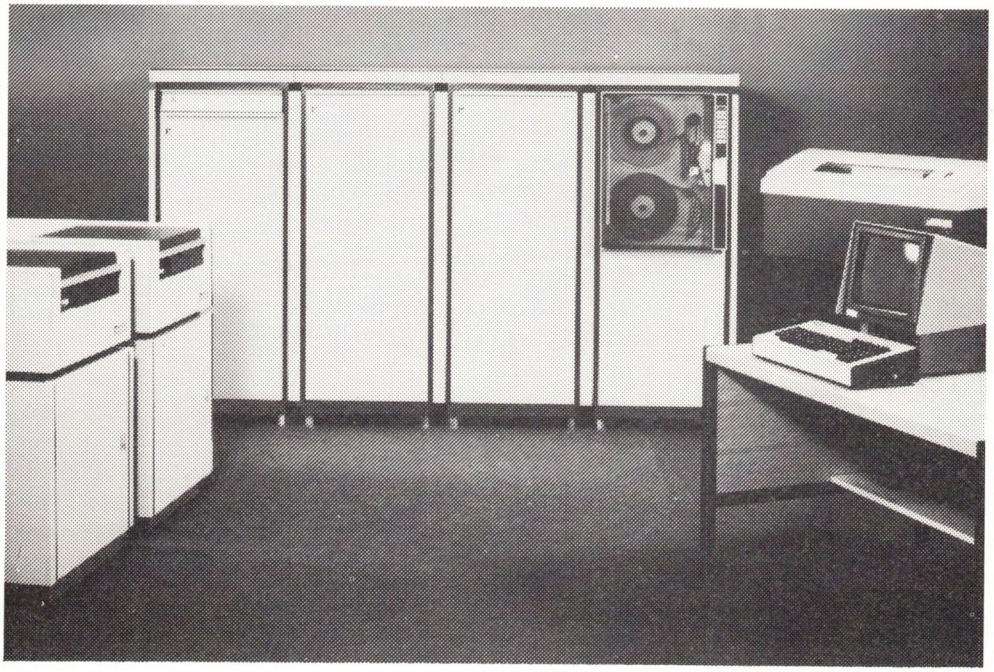
RC 8000-55S

Processing Unit

- 24-BIT WORD LENGTH
- MICROPROGRAMMED
- CACHE MEMORY
- SEMICONDUCTOR MEMORY WITH EROR CORRECTION
- MICROCODED SELF-DIAGNOSTICS
- FLOATING-POINT ARITHMETIC

The outline of an RC 8000-55S processing system



GENERAL

The RC 8000-55S processing unit is a general-purpose processor. The word length is 24 bits. The 4-accumulator, microprogrammed processor is based on TTL bit-slice technology. Instruction prefetch implemented as hardware feature is used to enchance processing speed. The high speed 4 K words cache memory between CPU and main memory in addition hereto effectively reduces the access times of instructions and operands.

The main memory is implemented with 16 K dynamic MOS memory chips. Each storage word consists of 24 data bits and a 6-bit error correction code. The ECC hardware automatically corrects all single-bit errors and detects double-bit as well as some multiple-bit errors. The RC 8000-55S processing system offers main memory sizes ranging from 64 K words to 4 M words. Each memory expansion module is 64 K words.

Extensive microcode resident self-diagnostics of CPU, main memory, and cache memory are standard features, activated automatically at autoload. The diagnostics can as well be operated from the technicians console during servicing of the equipment.

The processor has a 24-bit single address instruction format with 64 basic instructions. All instructions can work on all 4 accumulators. They have a 12-bit address displacement and 16 addressing modes including relative, indexed, and indirect addressing. 12-bit halfwords are directly addressable.

Integer arithmetic uses 24-bit words and 12-bit half-words, floating-point and extended range integer arithmetic use 48-bit double-words. Data manipulation is aided by half-word operations and word comparison functions. Logical operations permit setting and testing of single bits. Program protection is obtainned by means of limit registers and priveliged instructions executable only in monitor mode. Dynamic program relocation is possible through use of modified base register technique. An escape facility can be used to cause programmed action on preselected events.

Typical instruction execution times of the RC 8000-55S processing unit are 0.4 - 1.6 μsec. The combination of fast processing, powerful interrupt system, program protection system, and real-time feature makes the RC 8000-55S well-suited to perform multiprogramming. The processing power can be further underlined applying the optional floating-point processor.

Data transfers to and from the peripherals are controlled by channel programs stored in the memory. The peripherals are connected by means of dedicated or general-purpose controllers.

SPECIFICATIONS

PROCESSING UNIT

Control store:	4 K words, 48-bit each, PROM
CPU cycle time:	135 - 270 ns
Instr. exec. time:	0.4 - 1.6 μs, typically
Interrupt system:	8 internal, 56 external levels; response time: 10 μs approx.
Real-time clock:	0.1 ms resolution, stability: 4 s/24 h
Standard features:	Autoload via disc channel or device controller. Interrupt generating 25.6 ms interval timer. Microcoded self-diagnostics
Optional features:	Technicians console. Floating-point processor (RC 8051)

CACHE MEMORY

Capacity:	4 K words, high-speed static MOS
Word length:	24-bit data, 11-bit tag, 4 parity bits
Speed:	Access time: 135 ns, cycle time: 180 ns

MAIN MEMORY

Capacity:	64 K (65536) to 4 M (4196304) words, dynamic MOS
Word length:	24-bit data, 6-bit error correction code
Speed:	Access time: 600 ns, cycle time: 700 ns

ENVIRONMENTAL

Power requirements:	220 v AC, 50 Hz, 1300 W
Temperature, amb.:	10-27 °C (50-80 °F)
Humidity:	20-80% relative, non-condensing
Heat dissipation:	4700 kJ/h (1120 kcal/h, 4450 BTU/h)
Mounting:	19-inch cabinet (2 cabinets included), the processing unit occupies 88.6 cm (34.8 ins) in height and the weight is 94 kg (207 lbs.)
Cabinets, min:	Height: 143 cm (56 ins), width: 116 cm (45.6 ins), depth: 80 cm (31.5 ins), weight: 138 kg (204 lbs.)