ID-7061 RC-3500 Peripheral Interface Module
for
ID-7000 Microprocessor System

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Note: This description is preliminary and may be subject for some changes.

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1. GENERAL DESCRIPTION.

This module can be used to connect peripherals designed to interface an RC-3500[+)] I/O-channel. (such as the RC-810 CRT terminal) to the ID-7000 microprocessor system. Seen from the peripheral the module functions as an RC-3500 General Purpose Controller. The module contains two 16 bits registers TXBUF and RXBUF for buffering data to and from the peripheral. These registers can be loaded and read by the ID-7000 CPU using normal ID-7000 I/O instructions. The data transfer between ID-7000 and the peripheral is performed in serial according to the standards of RC-3500, using four twisted pairs for data and clock transfer in either direction with a clock rate of 5MHz.
Fig. 1 is a blocked schematic of the module.

+) RC-3500 is a General Purpose Controller from Regnecentralen A/S

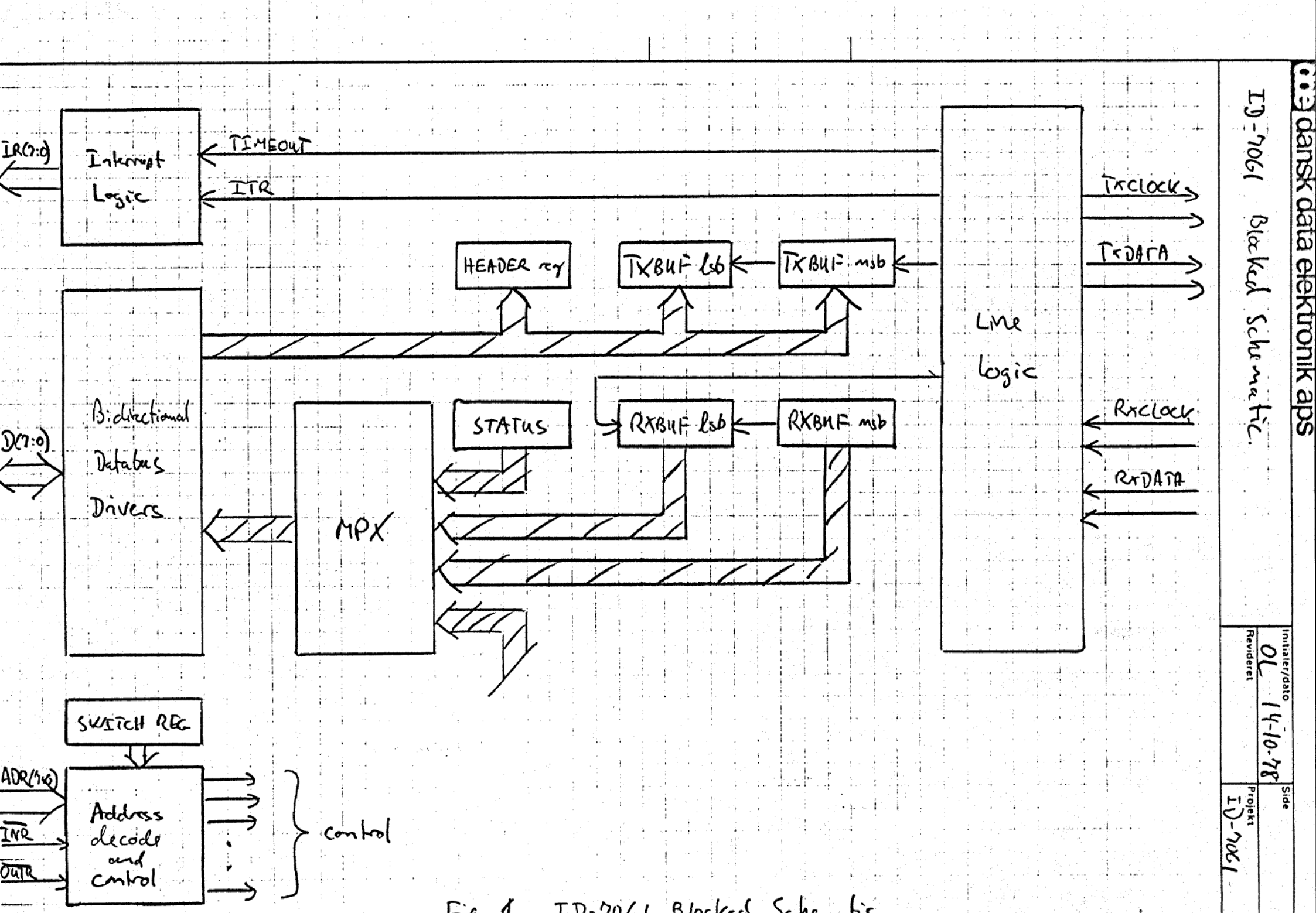

Fig. 1 ID-7061 Blocked Schematic

2. COMMUNICATION WITH THE PERIPHERAL

The module can send four different messages to the peripheral:

Header "1" X_0 X_1 "1"	Message
1 0 0 1	Read Data
1 0 1 1	Read Status
1 1 0 1	Write Data
1 1 1 1	Write Control

The output message from the module always consists of 20 bits, 4 header bits and 16 information bits. (In the Read Data and the Read Status message, the information bits are undefined.) The information bits of the Write Data and the Write Control message is determined by the contents of the TXBUF register.

When a Read Data or a Read Status header is sent, the module is ready to receive data from the peripheral in the RXBUF register. The two header information bits of the received message is sampled in the STATUS register of the module. The following headers may be received

Header "1" X_0 X_1 "1"	Message
1 0 0 1	16 bits (word
1 0 1 1	EoI (end of information)
1 1 0 1	8 bits (byte)
1 1 1 1	1 bit (bit)

It should be noticed, that the module always expects 20 clocks on the input clock line. 16 bits of information are always sampled in the RXBUF register. If an input message from the peripheral is not completed within a time interval of 20 µsec. from the initi-

ation of the Read Data or Read Status message, a TIMEOUT flag is activated. This flag is a part of the STATUS word of the module. It can also be connected to an interrupt request line of the ID-7000 microprocessor system.

The module also detects interrupts from the peripheral device. The peripheral may send an interrupt by sending a single data-bit to the data input of the module. To insure that none of the interrupts are neglected by the module, interrupts may not be sent during the period in which the module is transmitting clock pulses. Furthermore during READ-instructions interrupts must not be generated in a period of 3 µsec after the completion of the input message to the module. An interrupt from a peripheral device sets the ITR-flag of the module STATUS-register. This flag can also be connected to the ID-7000 interrupt request for interrupting the ID-7000 CPU.

3. COMMUNICATION WITH THE ID-7000 CPU

The communication between the ID-7000 CPU and the module is performed using normal input and output instructions. The module uses four consecutive I/O-instructions. The base address of the module is determined by a 6 bit switch register on the board.

Input instructions:

IN 4n+0=	reads least significant byte from RXBUF-register
IN 4n+1=	reads most significant byte from RXBUF-register
IN 4n+2=	reads the STATUS register of the module
IN 4n+3=	reads all 0's.

Output instructions:

OUT 4n+0=	loads least significant byte of the TXBUF register.
OUT 4n+1=	loads most significant byte of the TXBUF register and initiates transmission of a message according to the contents of the HEADER register.
OUT 4n+2=	loads the HEADER register. This header is used when an OUT 4n+1 instruction is performed. Bit 1 of the accumulator loads the X_0 information. Bit 0 of the accumulator loads the X_1 information.

OUT 4n+3= This output instruction is used to clear the ITR-flag and the TIMEOUT-flag in the STATUS register. If ACC(7)=1, the ITR flag is cleared. If ACC(0)=1 the TIMEOUT flag is cleared.

STATUS-word:

ITR	0	0	0	0	X0	X1	TIMEOUT
7	6	5	4	3	2	1	0

bit 0 TIMEOUT-flag. This flag is set according to the rules described in section 2. It is cleared by performing an OUT 2n+3 instruction with ACC(0)=1

bit 2:1 X_0,X_1 These bits contain the header information from the last received peripheral message.

INTERRUPTS.

Using a strap socket the ITR-flag and the TIMEOUT-flag may be connected to the interrupt request bus of the ID-7000 microprocessor system, to generate interrupts to the ID-7000 CPU.