DANSK DATA ELEKTRONIK

ID 7060 RC 3500 INTERFACE MODULE

for the

ID 7000 MICROPROCESSOR SYSTEM

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Author: Ole Lading
Knud Arne Nielsen

1. General Description.

This module is used to connect the ID 7000 microprocessor system to an I/O channel of an RC 3500 General Purpose Controller from Regnecentralen A/S. The module functions as s periphal device connected to the RC 3500. The module contains two 16 bit registers TXBUF and RXBUF for buffering data to and from the RC 3500. These registers can be loaded and read by the ID 7000 CPU using normal ID 7000 I/O instructions. The data transfer between RC 3500 and ID 7000 is performed in serial according to the standards of RC 3500, using four twisted pair for data and clock transfer in eighter direction with a clock rate of 5 MHz.

2. Output from RC 3500 to ID 7000

The output message from RC 3500 always consist of 20 bits:
4 header bits and 16 information bits.
The four header bits are decoded by the interface and proper action is taken. The interpretation af the header is as follows:

Header				Message
1	x0	x1	1	
1	0	0	1	Read data
1	0	1	1	Read status
1	1	0	1	Write data
1	1	1	1	Write control

When the read instructions are preformed the interface starts transmission after the header bits are received.

When write instructions are performed, 16 bits of data are sampled in RXBUF and the RXRDY flag in the status word of the module is activated and an interrupt to the ID 7000 CPU is generated. The RXRDY flag is cleared when the most significant byte of the RXBUF-register is read by the CPU.

3. Input to RC 3500 from ID 7000.

Following a Read data or a Read status command header from the RC 3500, the interface transmits the 16 bit TXBUF register preceeded by the following information:

Header				Message
1	x0	x1	1	
1	0	0	1	16 bits data
1	0	1	1	EOI

The selection of header is under program control in the ID 7000. See section 5.3

4. RC 3500 Interrupts.

The interface can generate an interrupt to the RC 3500 under program control from the ID 7000 . An interrupt is generated when a "1" is sent to the RC 3500, at a time when no data is requested. During a write command interrupts must be inhibited when the RC 3500 is transmitting clock pulses. Furthermore during READ instructions, 3 usec. must be added after transmission of the input message to the RC 3500 is completed. There are two causes of RC 3500 interrupts:

a. The ID 7000 has performed an OUT 4n+2 or an OUT 4n+3 instruction.

b. The ID 7060 module has received a Write control command from RC 3500 when the TXBUF register is not empty.

5 Communication with the ID 7000.

The communication between the module and the ID 7000 is performed using normal I/O instructions and interrupts.

5.1 Input Instructions.

The module uses four consecutive input addresses.
The base address of the module is determined by a 6 bit switch on the board.

IN 4n+0

Reads the least significant data byte from the RXBUF register.

IN 4n+1

Reads the most significant data byte from the RXBUF register.
Clears the RXRDY flag in the status register.
Clears the RXBUF register

IN 4n+2

Reads the module STATUS register.

IN 4n+3

Not used. Reads all zeros.

5.2 The Status Register.

bit 0: RXRDY

RXRDY. This flag indicates that a Write data or Write control output message has been sent from the RC 3500. The RXBUF re-gester contains 16 bits of information. This flag is cleared when the most significant data byte is fetched by the ID 7000 CPU (i.e. when an IN 4n+1 instruction is executed.

bit(2:1): x0, x1

x0, x1. These bits contains the header information from the last received RC 3500 output message.

bit(6:3): Not used. Always zero.

bit(7): TXEMPTY

TXEMPTY. This flag indicates that the TXBUF register is ready to be loaded by new 16 bit data information. It is set and reset according to the rules described in section 3.

5.3 Output Instructions.

The module uses four consecutive output addresses. The base address is determined by the same switch register as used for input instructions.

OUT 4n+0

Loads the least significant byte of the TXBUF register.

OUT 4n+1

Loads the most significant byte of the TXBUF register.
The information is later transmitted with a data header.
Optionally an interrupt to RC 3500 is generated.
This option can be activated by a strap.

OUT 4n+2

Loads the most significant byte of the TXBUF register.
The information is later transmitted with an EOI header.
Optionally an interrupt to the RC 3500 is generated.
This option can be activated by a strap.

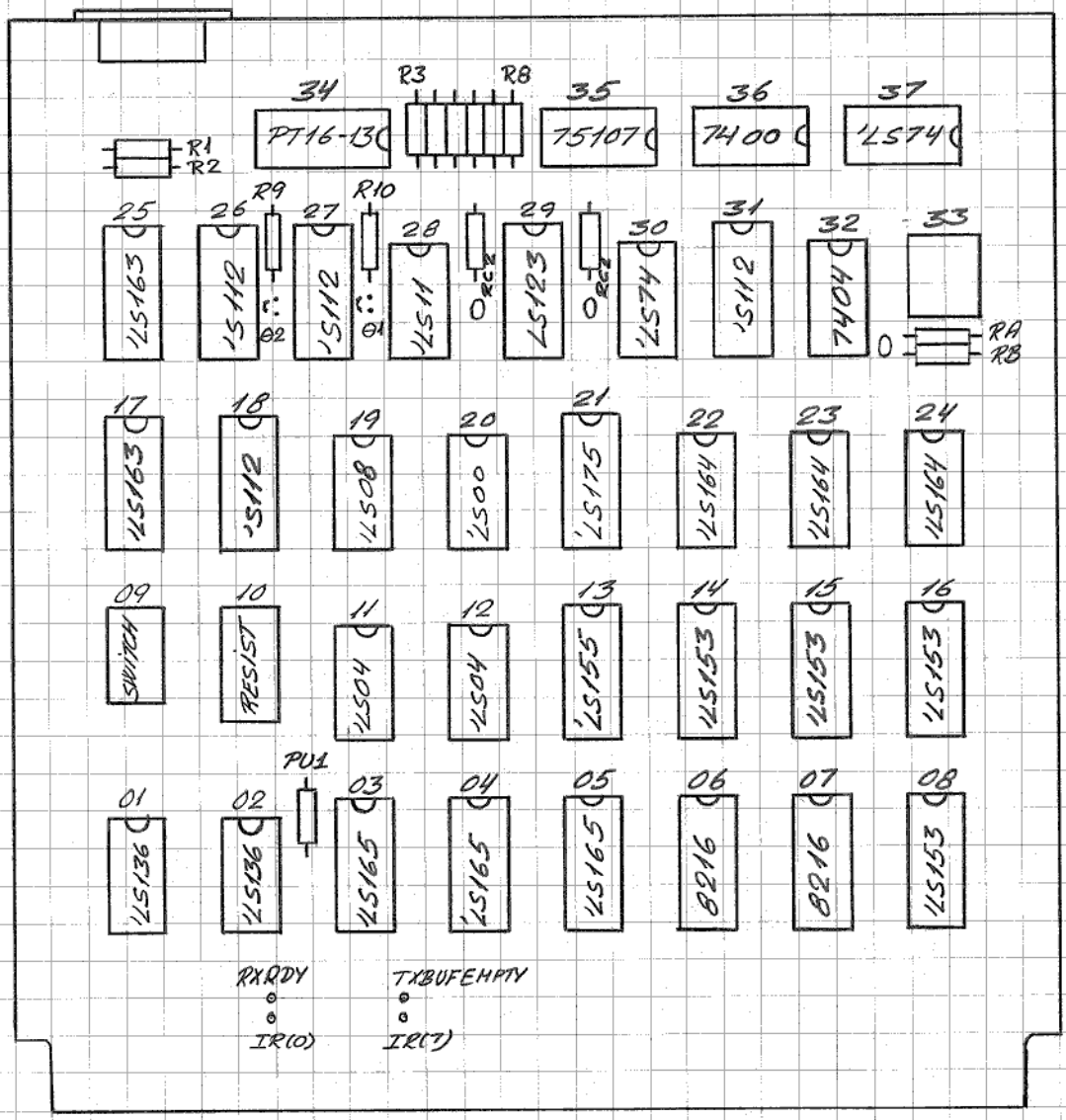
OUT 4n+3

Generates an interrupt to RC 3500.

6. ID 7000 Interrupts.

The RXRDY flag and the TXEMPTY flag of the status register may be connected to the ID 7000 interrupt request bus IR(7:0).

ID 7060


34
PT16-13
R3
R8
35
75107
36
7400
37
LS74
R1
R2
25
LS163
26
LS112
R9
27
LS112
R10
28
LS11
29
LS123
30
LS74
31
LS112
32
7404
33
RA
RB
17
LS163
18
LS112
19
LS08
20
LS00
21
LS175
22
LS164
23
LS164
24
LS164
09
SWITCH
10
RESIST
11
LS04
12
LS04
13
LS155
14
LS153
15
LS153
16
LS153
PU1
01
LS136
02
LS136
03
LS165
04
LS165
05
LS165
06
8216
07
8216
08
LS153
RXRDY
IR(0)
TXBUFEMPTY
IR(7)

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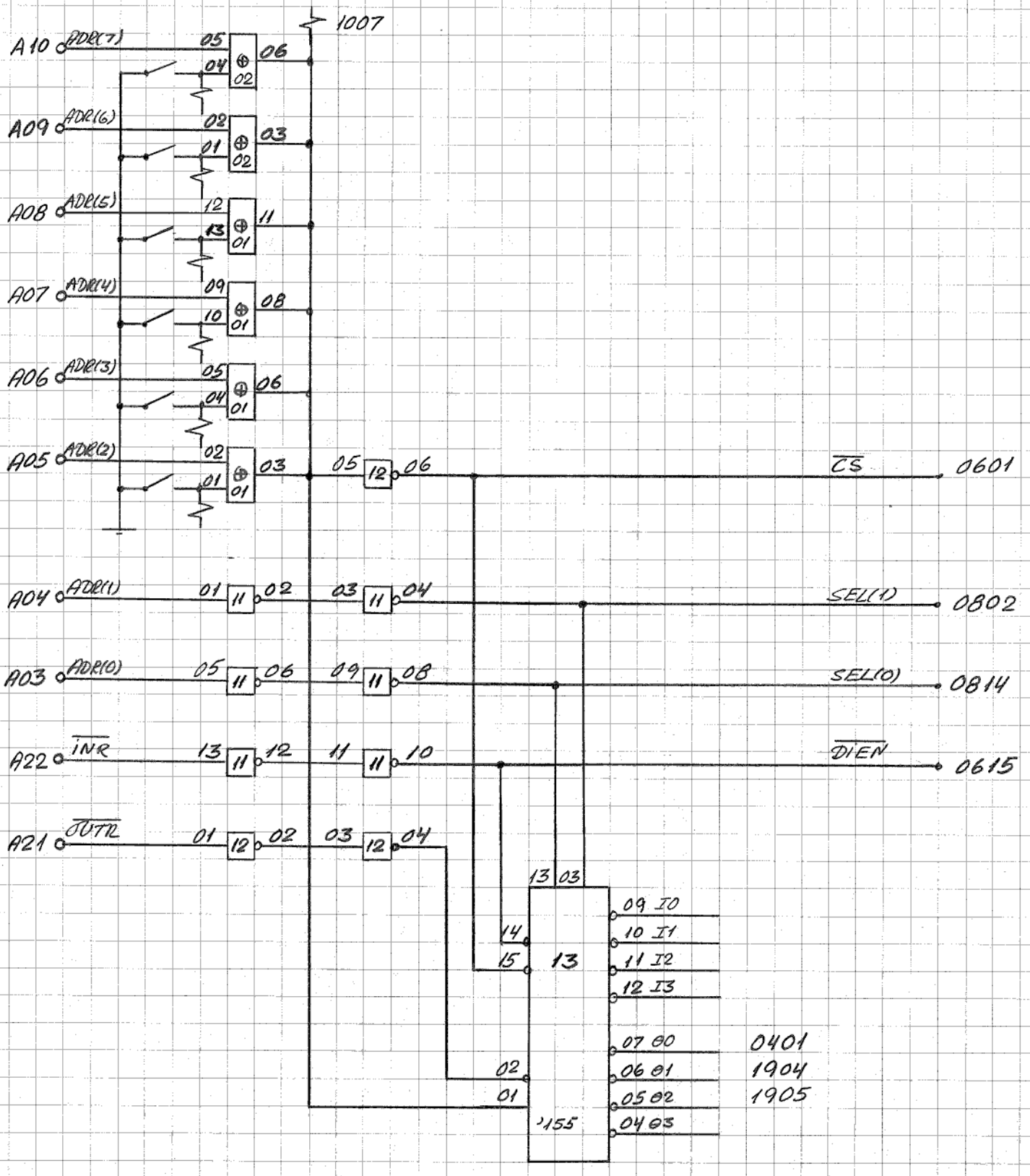
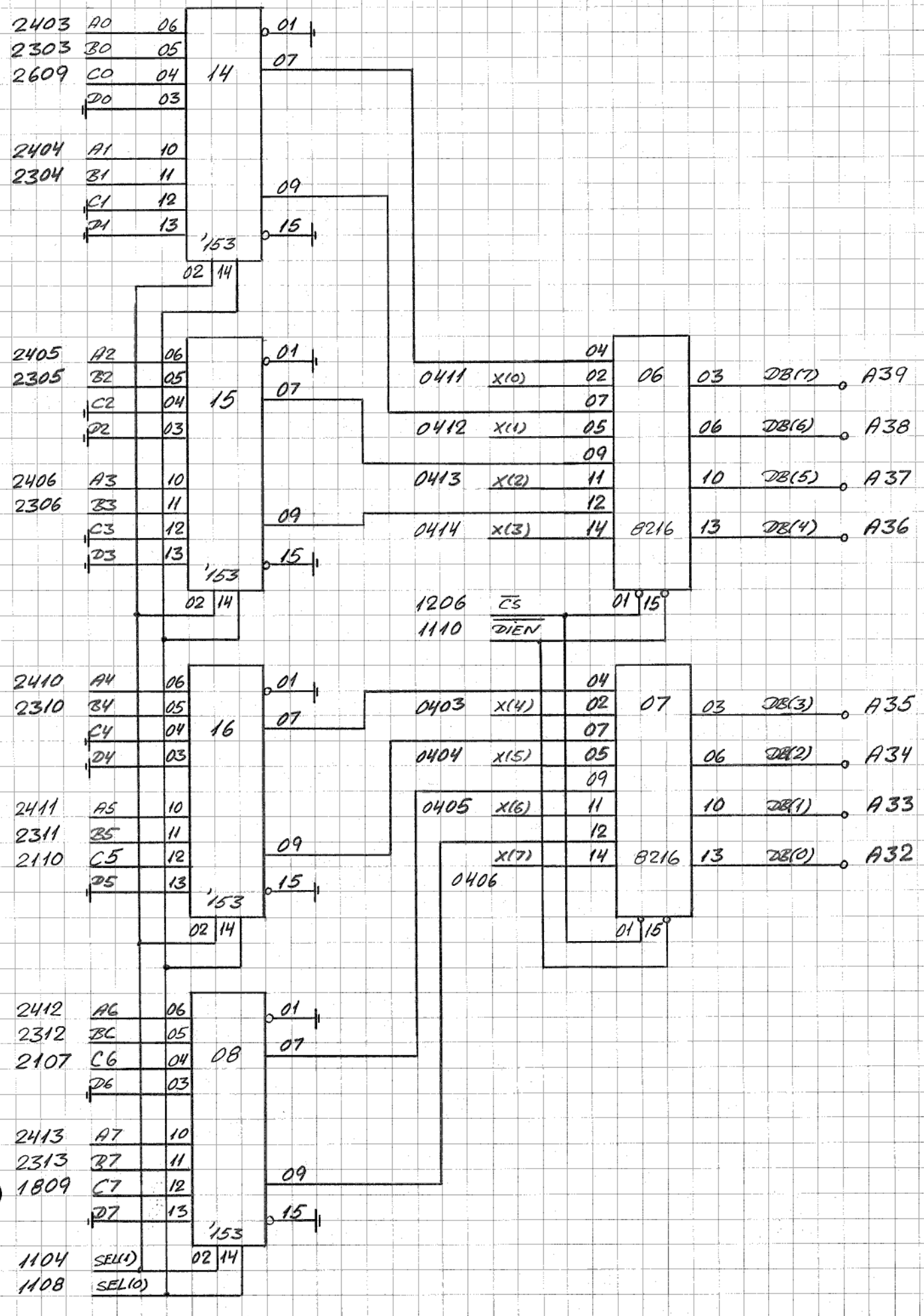
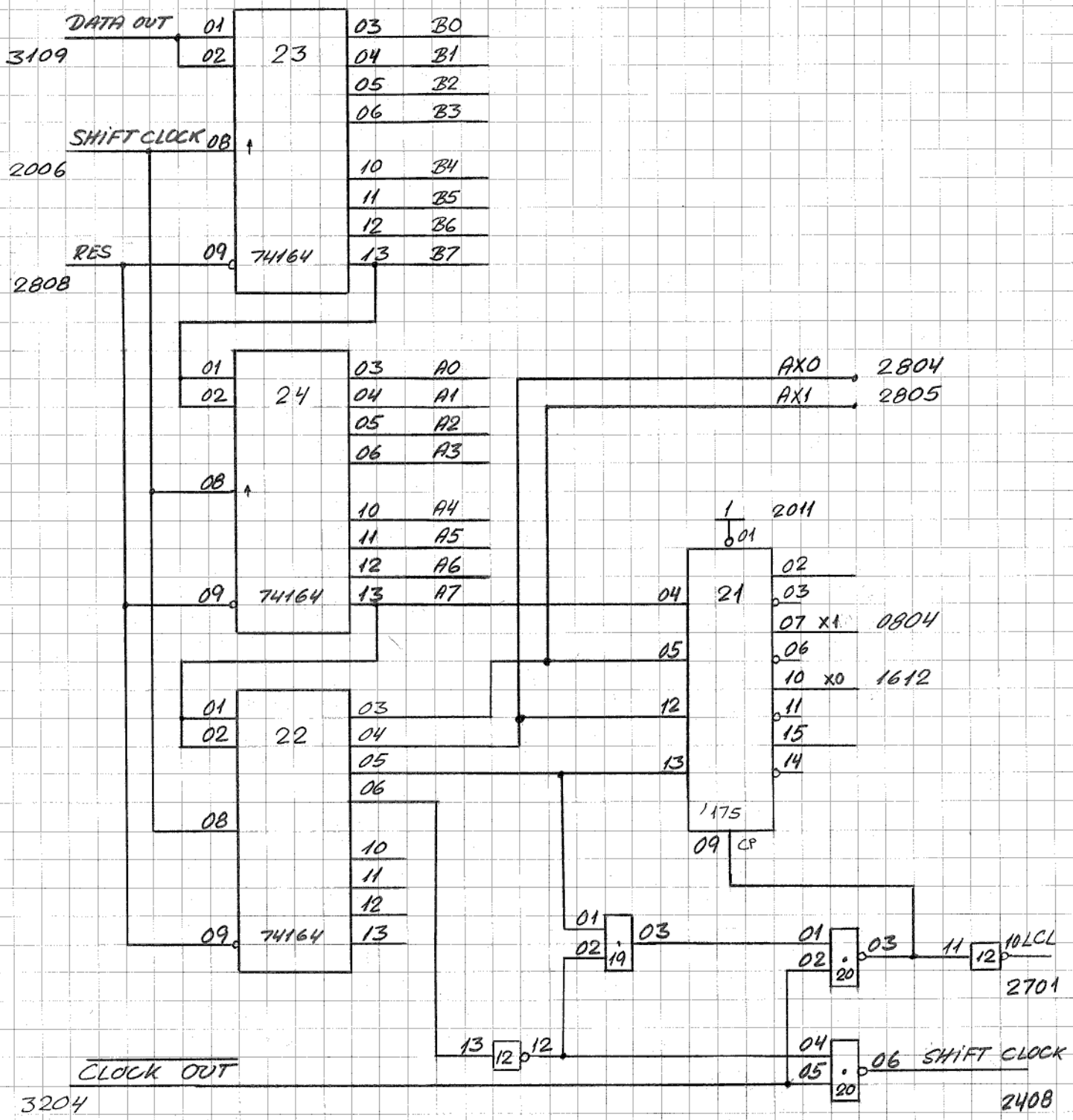
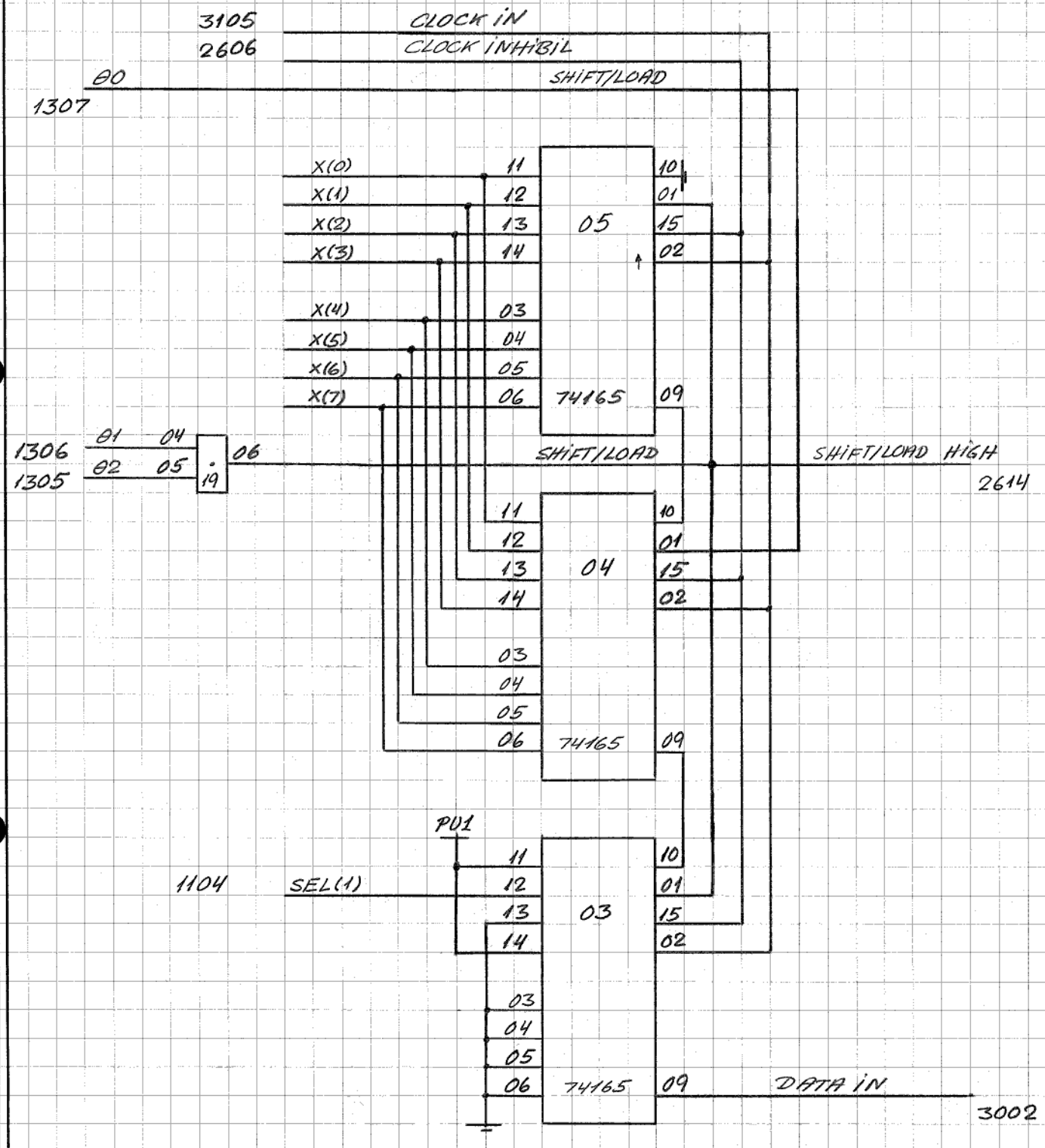
ID-7000 ordre dekodning

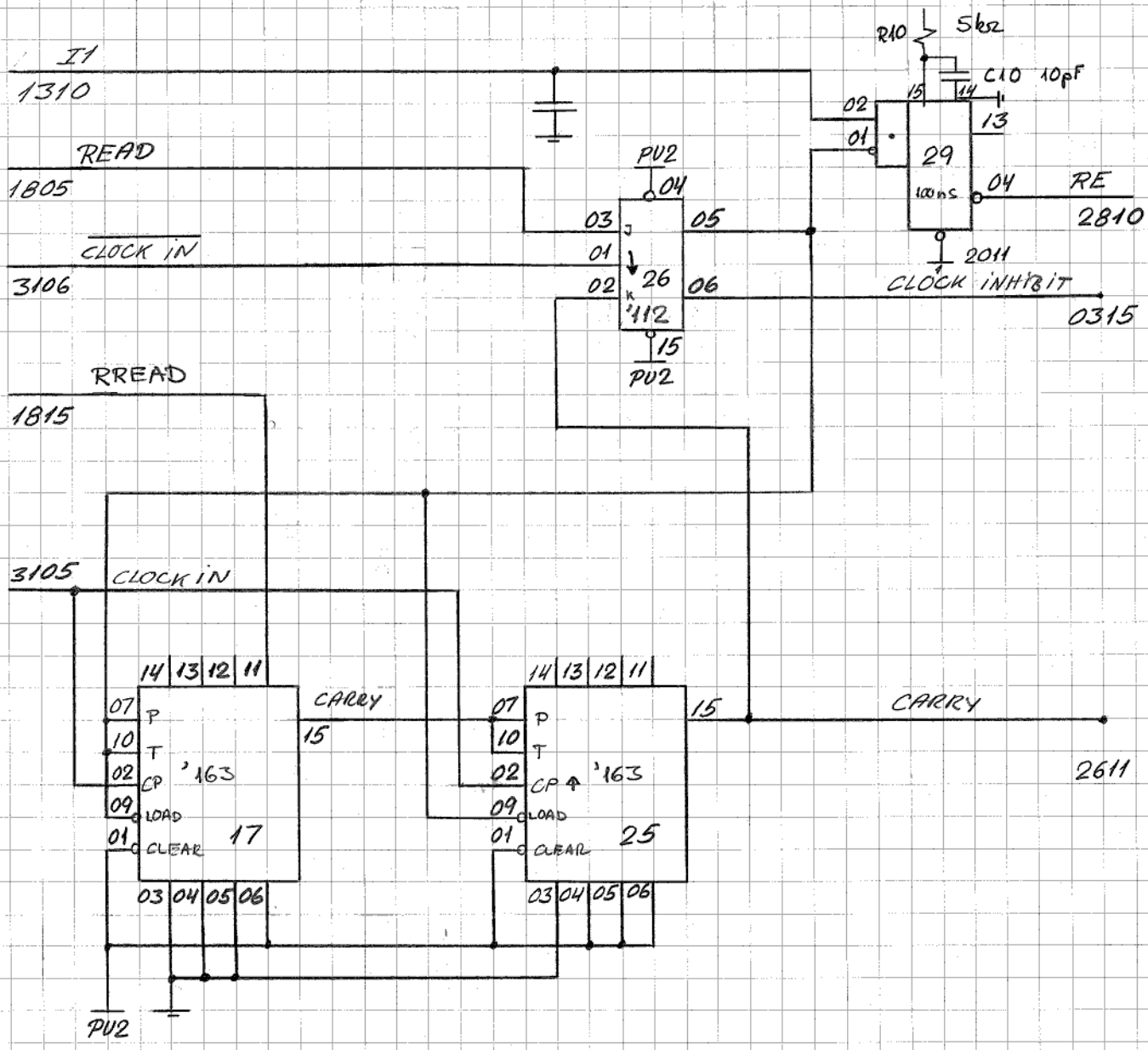
Initialer/dato	Side
KAN 790109	1
Revideret	Projekt
	ID 7060

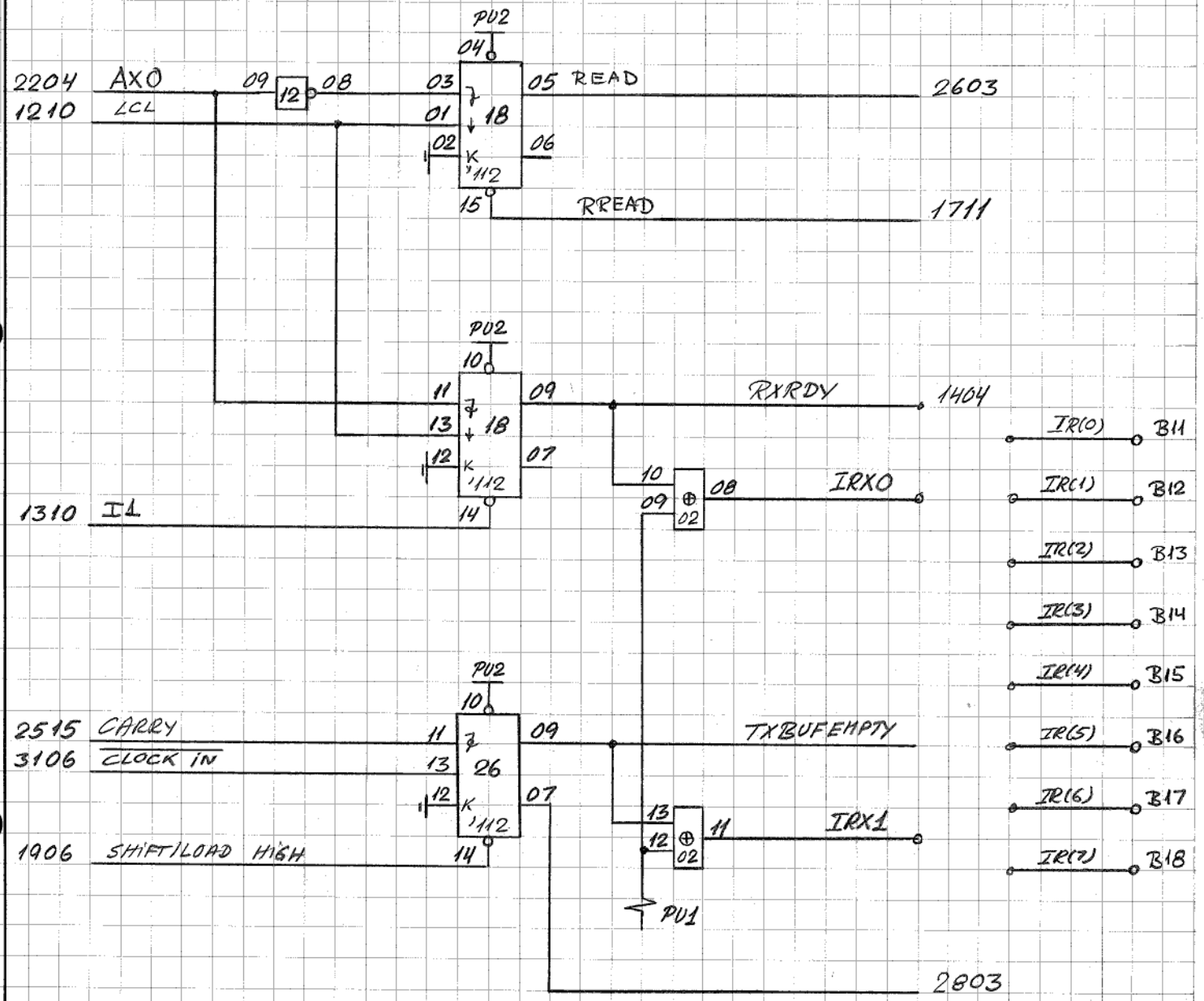


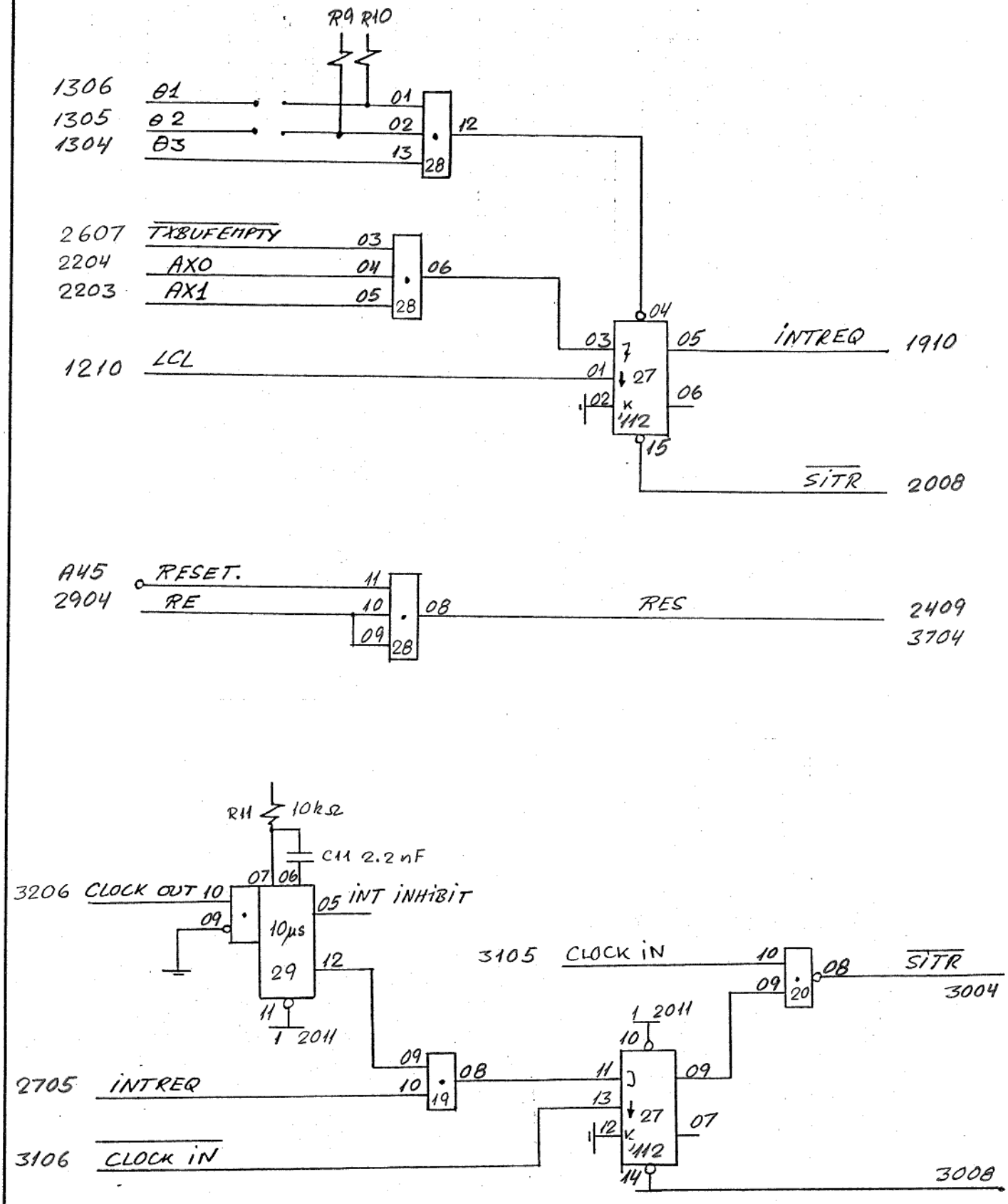

2403 A0 06
2303 B0 05
2609 C0 04
D0 03
14
01
07
2404 A1 10
2304 B1 11
C1 12
D1 13
09
15
'153
02 14
2405 A2 06
2305 B2 05
C2 04
D2 03
15
01
07
2406 A3 10
2306 B3 11
C3 12
D3 13
09
15
'153
02 14
2410 A4 06
2310 B4 05
C4 04
D4 03
16
01
07
2411 A5 10
2311 B5 11
2110 C5 12
D5 13
09
15
'153
02 14
2412 A6 06
2312 B6 05
2107 C6 04
D6 03
08
01
07
2413 A7 10
2313 B7 11
1809 C7 12
D7 13
09
15
'153
1104 SEL(1)
1108 SEL(0)
02 14
0411 X(0) 04 02 07
0412 X(1) 05 09
0413 X(2) 11 12
0414 X(3) 14
06
8216
03 DB(7) A39
06 DB(6) A38
10 DB(5) A37
13 DB(4) A36
1206 CS
1110 DIEN
01 15
0403 X(4) 04 02 07
0404 X(5) 05 09
0405 X(6) 11 12
X(7) 14
0406
07
8216
03 DB(3) A35
06 DB(2) A34
10 DB(1) A33
13 DB(0) A32
01 15


DATA OUT
3109
SHIFT CLOCK
2006
RES
2808
23
24
22
74164
01
02
03
04
05
06
08
09
10
11
12
13
B0
B1
B2
B3
B4
B5
B6
B7
A0
A1
A2
A3
A4
A5
A6
A7
AX0
2804
AX1
2805
1
2011
21
07 X1
0804
10 X0
1612
14
15
175
CP
19
20
10LCL
2701
CLOCK OUT
3204
SHIFT CLOCK
2408


3105
CLOCK IN
2606
CLOCK INHIBIL
00
SHIFT/LOAD
1307
X(0)
X(1)
X(2)
X(3)
X(4)
X(5)
X(6)
X(7)
11
12
13
14
03
04
05
06
05
74165
10
01
15
02
09
1306
1305
01
04
02
05
19
06
SHIFT/LOAD
SHIFT/LOAD HIGH
2614
04
74165
PU1
1104
SEL(1)
03
74165
DATA IN
3002


I1
1310
READ
1805
CLOCK IN
3106
RREAD
1815
3105
CLOCK IN
R10
5kΩ
C10
10pF
29
100nS
RE
2810
2011
CLOCK INHIBIT
0315
PU2
26
'112
CARRY
'163
17
25
CARRY
2611
PU2


PU2
04
2204 AX0
1210 LCL
09
12
08
03
01
02
7
18
K
112
05 READ
2603
06
15
RREAD
1711
PU2
10
11
13
12
09
07
14
RXRDY
1404
1310 I1
10
09
02
08
IRX0
IR(0) B11
IR(1) B12
IR(2) B13
IR(3) B14
IR(4) B15
IR(5) B16
IR(6) B17
IR(7) B18
PU2
10
2515 CARRY
3106 CLOCK IN
11
13
12
09
07
14
26
TXBUFEMPTY
1906 SHIFT/LOAD HIGH
13
12
11
IRX1
PU1
2803


R9 R10
1306 Θ1
1305 Θ2
1304 Θ3
2607 TXBUFEMPTY
2204 AX0
2203 AX1
1210 LCL
INTREQ 1910
SITR 2008
A45 2904 RESET. RE
RES 2409 3704
R11 10kΩ
C11 2.2nF
3206 CLOCK OUT
INT INHIBIT
10µs
2705 INTREQ
3106 CLOCK IN
3105 CLOCK IN
SITR 3004
3008

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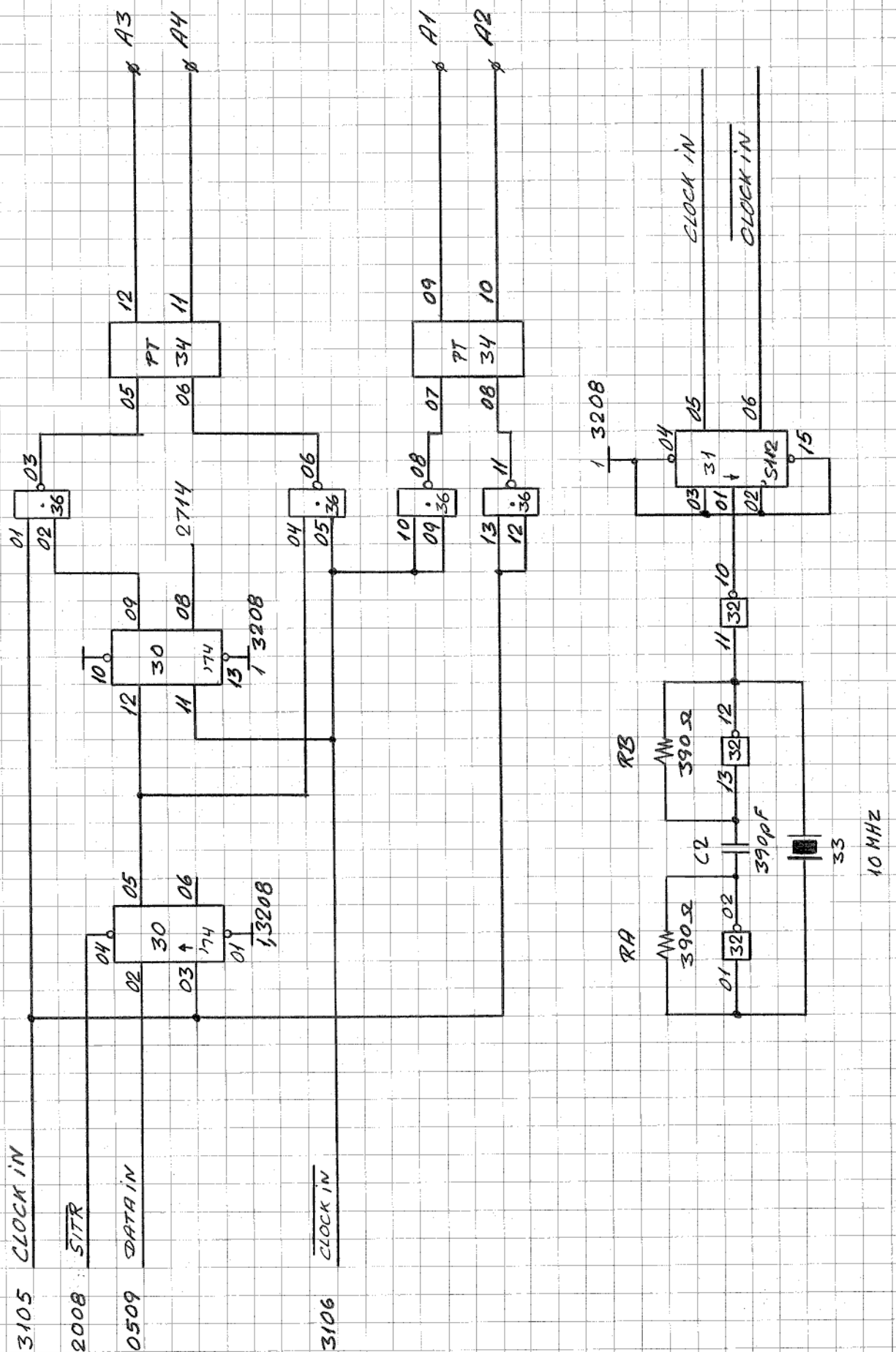
DRIVER CIRCUIT

Initialer/dato	Side
KAN 790112	8
Revideret	Projekt 7060



RECEIVER CIRCUIT