ID-7060 RC-3500 Interface Module
for
ID-7000 Microprocessor System
oct. 1978

Note: This description is preliminary and may be subject to som changes.

written by Ole Lading.

GENERAL DESCRIPTION.

This module is used to connect the ID-7000 microprocessor system to an I/O channel of an RC-3500 General Purpose Controller from Regnecentralen A/S. The module functions as a peripheral device connected to the RC-3500. The module contains two 16 bit registers TXBUF and RXBUF for buffering data to and from the RC-3500. These registers can be loaded and read by the ID-7000 CPU using normal ID-7000 I/O-instructions. The data transfer between RC-3500 and ID-7000 is performed in serial according to the standards of RC-3500, using four twisted pairs for data and clock transfer in either direction with a clock rate of 5MHz.

Fig. 1 is a blocked schematic of the module.

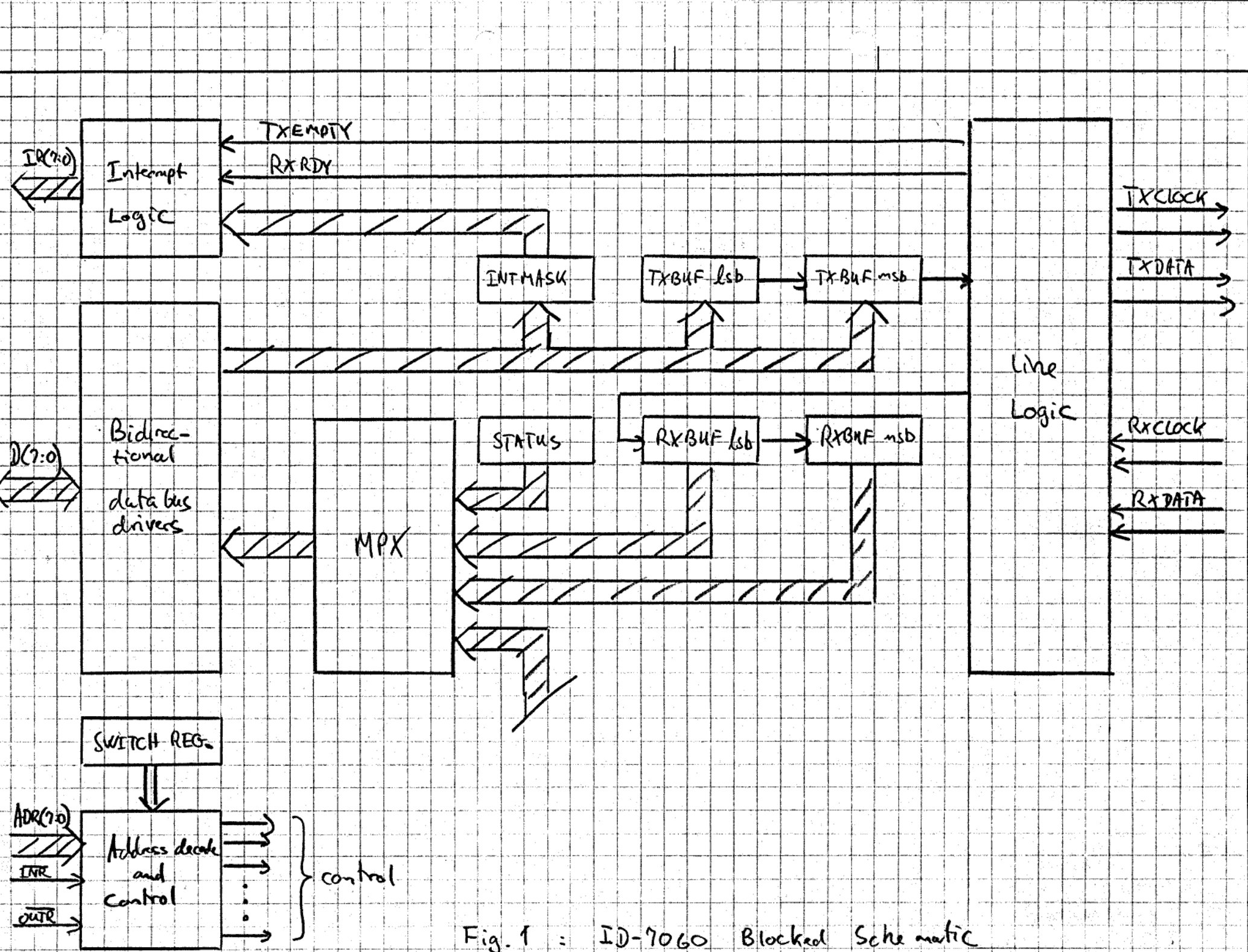

Fig. 1 : ID-7060 Blocked Schematic

dansk data elektronik aps

ID-7060 Blocked Schematic

Initialer/dato OL 14-10-78

Revideret

Side

Projekt ID-7060

2. Output from RC-3500 to ID-7000

The output message from the computer always consists of 20 bits; 4 header bits and 16 information bits.
The four header bits are decoded by the interface and proper action is taken. The interpretation of the header is as follows:

Header				Message
"1"	X_0	X_1	"1"	
1	0	0	1	Read Data
1	0	1	1	Read Status
1	1	0	1	Write Data
1	1	1	1	Write Control

When the read instructions are performed no data is sampled at the interface and the interface starts transmission (according to section 3) immidiately after the header bits are received.

When the write instructions are performed,16 bits of data are sampled in the RXBUF and the RXRDY flag in the status word of the module is activated and an interrupt to the ID-7000 CPU is generated. The RXRDY flag is cleared when the most significant byte of the RXBUF-register is read by the CPU.

3. Input to RC-3500 from ID-7000.

Following a Read Data or a Read Status command-header from the RC-3500, the interface immediately transmits the 16 bit TXBUF register preceeded by the following header information:

Header				Message
"1"	X_0	X_1	"1"	
1	0	0	1	16 bits data
1	0	1	0	E O T

This first header is used if new information was loaded to the TXBUF register since last transmission. The second header is used if no new information was loaded to the TXBUF register since last

transmission. ~~The second header is used if no new information was loaded to the TXBUF register since last transmission.~~ This is indicated by the TXBUFEMPTY-flag. This flag is reset when the most significant byte of the TXBUF-register is loaded. It is set when the transmission of the message to the RC-3500 is completed.

4. RC-3500 interrrupt.

The interface can generate an interrupt to the RC-3500 under program control from the ID-7000 CPU. An interrupt is generated when a "1" bit is sent to the RC-3500, at a time when no data is requested. (During a write command interrupts must be inhibited when the RC-3500 is transmitting clock pulses. Furthermore during READ instructions, 3 µsec. must be added after transmission of the input message to the RC-3500 CPU is completed.

5. Communication to ID-7000 CPU.

The communication between the module and the ID-7000 CPU is performed using I/O instructions and interrupts.

Input specifications: The module uses four consecutive input instructions. The base address of the module is determined by a 6 bit switch register on the board.

IN 4n+0= reads least significant data byte from the RXBUF-register.

IN 4n+1= reads most significant data byte from the RXBUF-register. Clears the RXRDY-flag in the status register.

IN 4n+2= reads the module STATUS register.

IN 4n+3= not used, reads all 0's.

Status register:

TXEMPTY	0	0	0	0	X_0	X_1	RXRDY
7	6	5	4	3	2	1	0

bit 0 RXRDY. This flag indicates that a WRITE DATA or WRITE CONTROL output message has been sent from the RC-3500. The RXBUF register contains 16 bits of information. This flag is cleared when most significant data byte is fetched by the ID-7000 CPU (i.e. when an IN 4n+1 instruction is executed).

bit2:1 X_0,X_1. These bits contains the header information from the last received RC-3500 output message.

bit 6:3 always 0

bit 7 TXEMPTY. This flag indicates that the TXBUF-register is ready to be loaded by new 16 bit data information. It is set and reset according to the rules described in section 3.

Output instructions. The module uses four consecutive output instructions. The base address is determined by the same switchregister as used for input instructions.

OUT 4n+0= Loads least significant byte of the TXBUF register.

OUT 4n+1= Loads most significant byte of the TXBUF register. Optionally an interrupt to the RC-3500 is generated. (this option can be activated by a strap.)

OUT 4n+2= Loads the interrups mask flip-flops of the module. Bit 7 of ACC determines the contents of the TXINTMASK. Bit 0 of ACC loads the RXINTMASK. A logical "1" in the mask flip-flop enables the interrupt.

OUT 4n+3= Generates an interrupt to RC-3500

Interrupts. The RXRDY-flag and the TXEMPTY flag of the status register may be connected to the ID-7000 interrupt request bus (IR(70)) as interrupts using a strap socket on the module. The flags are ANDED with the interruptmasks before entering the IR-bus.