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Abstract:

This paper contains a technical description of a high resolution graphic option to the RC702/RC703 microcomputer family.

(48 pages)

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1. INTRODUCTION

The VPB701, Video Graphic Board, is a graphic controller that adds bit-mapped-raster-scan graphic drawing and display functions to the Piccolo line of microcomputers RC702 and RC703. The VPB701 is designed for installation onto the RC702/703 printed circuit board as a "piggyback", and power supplied from this computer.

The VPB701 works in two modes:

- Black/white mode. In this mode the 275x560 pixels graphic picture from VPB701 is ored with the normal character picture from RC702/703 video circuit. The mixed graphic/character video result is shown on the normal piccolo monitor.

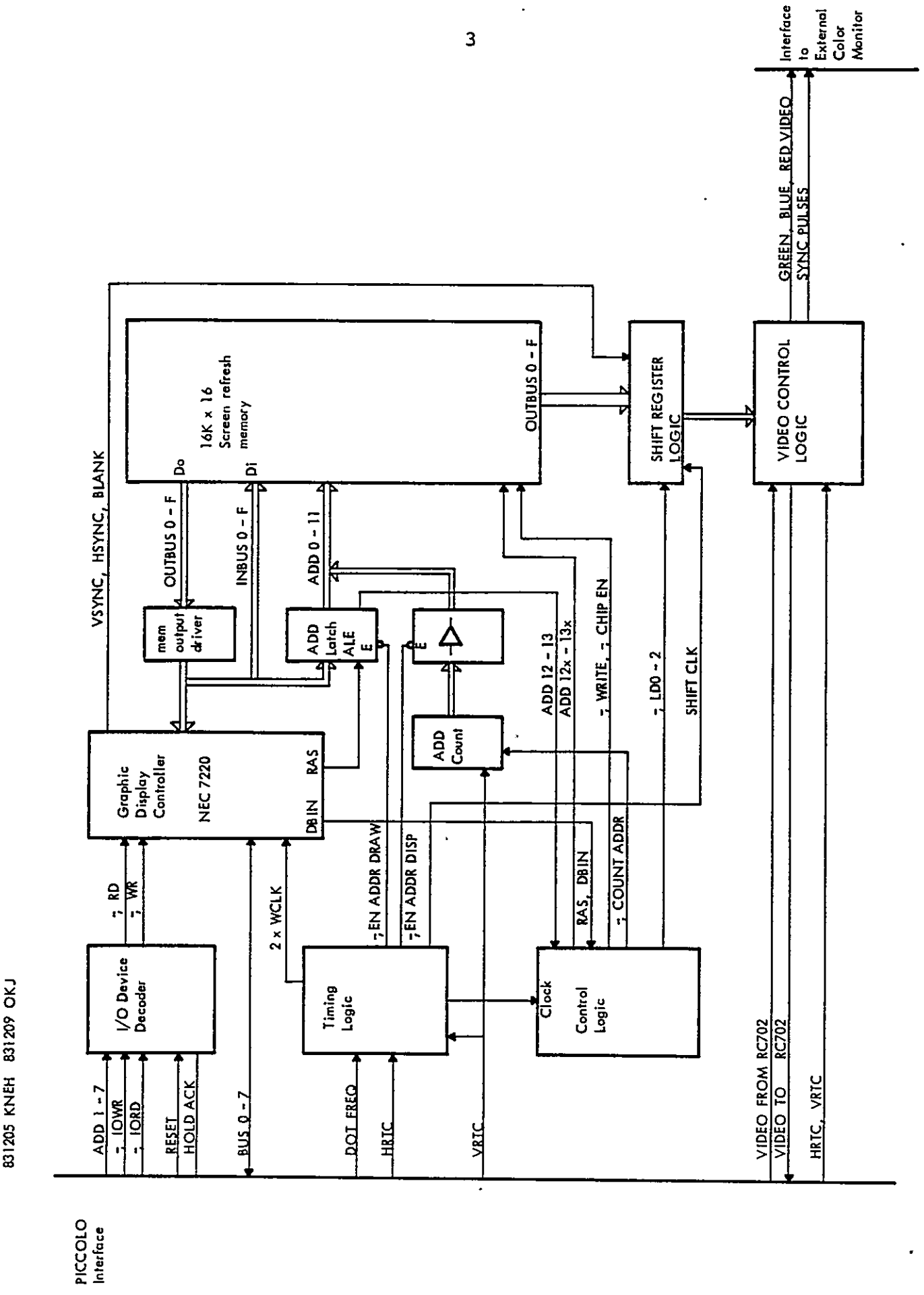
- Color mode. In this mode the VPB701 generates a 256x256 pixels eight color picture on an external color monitor. Switching between the 2 modes is controlled by hardware straps; and its too neccessary to change a PAL-logic IC.

2. GENERAL DESCRIPTION 2.

The VPB701, Video Processor Board, is designed to work with the RC702/703 microcomputer in order to implement a computer graphics system. The VPB701 is attached to the host processor board via the normal Z80 microprocessor I/O bus (bus 0-7, add 0-7 and control signals); and is used to qenerate the basic video signals to the video display monitor.

The host processor passes commands and data to VPB701 using programmed I/O instructions. The VPB701, upon receipt of commands, performs all of the tasks needed to manage the display memory. In addition to the display function, the VPB701 implements high-speed, vector-to-raster scan conversion.

The commands sent to the VPB701 consists of a series of instructions and their associated parameters. These commands and their associated parameters are used to construct a geometric figur or graphic character into the display memory bit-a-bit. This geometric figure or graphic character drawn in the display memory can then be displayed on the monitor. The monitor is a window into the display memory. The drawinq commands which define the element of the figure include lines, arcs, circles, rectangles, character/symbol painting, and area fills. The commands also allow user- selected linen styles and patterns with which to draw and display figures on the monitor. The host processor (under control of the user´s graphic software program) performs the preliminary calculations to prepare the drawing parameters, provides the starting point into the display memory and other associated parameters of the figure to be drawn. The VPB701 calculates the display memory addresses bit-by-bit for the graphic figure to be drawn and completes the drawing without further intervention from the host processor.



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VIDEO PROCESSOR BOARD TO RC702/ RC703

Block Diagram

Fig. 1.

For example, if a rectangle is to be drawn on the attached monitor, the VPB701 is given a command which defines the type of drawing followed by the starting address and several other parameters that define the length and height of the rectangle. The VPB701 is then given the start drawing command to draw a rectangle. The VPB701 takes the command and draws the figure in the display memory.

3. FUNCTIONAL DESCRIPTION 3.

The VPB701 consists of the logical blocks shown on the blockdiagram fig. 1. All these logical blocks are described in the following subsections.

3.1 I/O Device decoder 3.1

For details refer to logic diagram p.2.
This circuits decodes the I/O device numbers used by the VPB701. This circuit is implemented by a PAL (PAT560) shown on fig. 2. The decoded device numbers are listed in the following table:

Device number table		
Dev.no. (HEX)	Read	Write
C8	Status from 7220	Data,(Parameters) to 7220
C9	Data from 7220	Command to 7220
CC		disable graphic video
CE		Enable graphic video

The power on reset signal will set the disable graphic video function.

```
PAL16L8                      PAL DESIGN SPECIFICATION
PAT560                       1983.05.25;KNEH
I/O DECODER TO VPB701;GRAPHIC UNIT TO RC702/703.

XADD7 XADD6 XADD5 XADD4 XADD3 XADD2 XADD1 /IORD /IOWR GND
RESET /RD HACK NC 15 /BLANK 17 NC /WR VCC


IF (VCC)  /15 = HACK + /XADD7 + /XADD6 + XADD5 + XADD4 + /XADD3
IF (VCC) BLANK= RESET + 17 + 15*XADD2*/XADD1*IOWR
IF (VCC)  /17 = /BLANK + /RESET*15*XADD2*XADD1*IOWR
IF (VCC)   RD = 15*IORD*/XADD2*/XADD1
IF (VCC)   WR = 15*IOWR*/XADD2*/XADD1

DESCRIPTION:
THIS CIRCUIT DECODES THE I/O DEVICES USED BY
RC702/703 TO CONTROL THE GRAPHIC UNIT.

DEVICE C8H  READ FROM STATUS_REG .WRITE PARAMETER INTO FIFO.
DEVICE C9H  READ FROM FIFO. WRITE COMMAND INTO FIFO.
DEVICE CCH-CDH  SET BLANK GRAPHIC VIDEO FLIP-FLOP
DEVICE CEH-CFH  RESET BLANK GRAPHIC VIDEO FLIP-FLOP

THE BLANK FLIP-FLOP IS TOO SET BY THE "RESET" SIGNAL.
```

Fig. 2. Pal Design Specification (PAT560)

3.2 Graphic Display Controller

3.2

Refer to logic diagram p.1, the heart of the VPB701 is the NEC7220 (or INTEL 82720) Graphic Display Controller (6DC). The Graphic Display Controller (GDC) is an intelligent microprocessor peripheral designed as a raster-scan computer graphics controller. Control of the GDC by the host microprocessor is achieved via a standard 8 bit I/O bus (8 data bits, add 0-7 and control signals) interface. This interface allows the host microprocessor to send command and parameter bytes to start the drawing process. The host processor begins the process by retrieving status information from the VPB701 board concerning the drawing process. This status information from the VPB701 is readable at any time by the host processor. Access to the GDC is coordinated via flags in the

status register. The First In First Out (FIFO) buffer is integral to the GDC and is the GDC's interface to the host processor connector through which all commands and data pass. Access to the 16-byte FIFO is controlled by the host processor via the GDC's command set. The host processor coordinates the transfers by checking the appropriate status register bits. Commands and parameter bytes are send to the GDC's FIFO and are differentiated based on the state of the address bit 0. All commands are written to the GDC.

When the write control line (>WR) is activated, the GDC configures the FIFO as an input buffer to receive the command and the parameter bytes. If a read command is issued to the GDC, the GDC interprets the command, configures the FIFO as an output buffer and places the requested data into the FIFO. The status register indicates that the data is ready to retrieve. The host processor can then retrieve the requested information by activating the read control line (>rd).

When the host processor sends a command byte and activates the write control line to the GDC, the GDC interprets the contents written into the FIFO, decodes the command, distributes the succeeding parameter bytes to the proper registers within the GDC, and then initiates the required operation. Any parameter byte following a command is truncated by the receipt of the nect command.

The host processor programs the GDC sync logic during initalization with either a reset command or a sync command and the associated parameters.

In color mode the GDC generates the sync signals (horizontal and vertical) as well as he blanking signals to the CRT monitor for any interlaced or non-interlaced video format.

In the Black/White mode the GDC acts as a slave to the CRT logic in the RC702/703. In this mode no Start Display command is given to the GDC.

3.3 Timing and Control Logic 3.3

For details refer to the logic diagram p.2.
This circuit contain 2 pal-logic-circuit. In Black/White mode PAT562 and PAT563. In color mode PAT562 and PAT564. Each mode is further described in the following 2 subsections.

3.3.1 Black/White mode 3.3.1

The PAT562 acts as a 4 bits down counter. This counter is synchronized with the RC702 video timing by the signal >STOP STATE. The counter is driven by the DOT FREquency clock from RC702 (-10MHz). PAT563 decodes the state of the counter and generates load signal for the green video shift register (used for black/white video), and counting of the RC702 graphic refresh address.
Selecting between Black/White and color mode is controlled by the following straps:

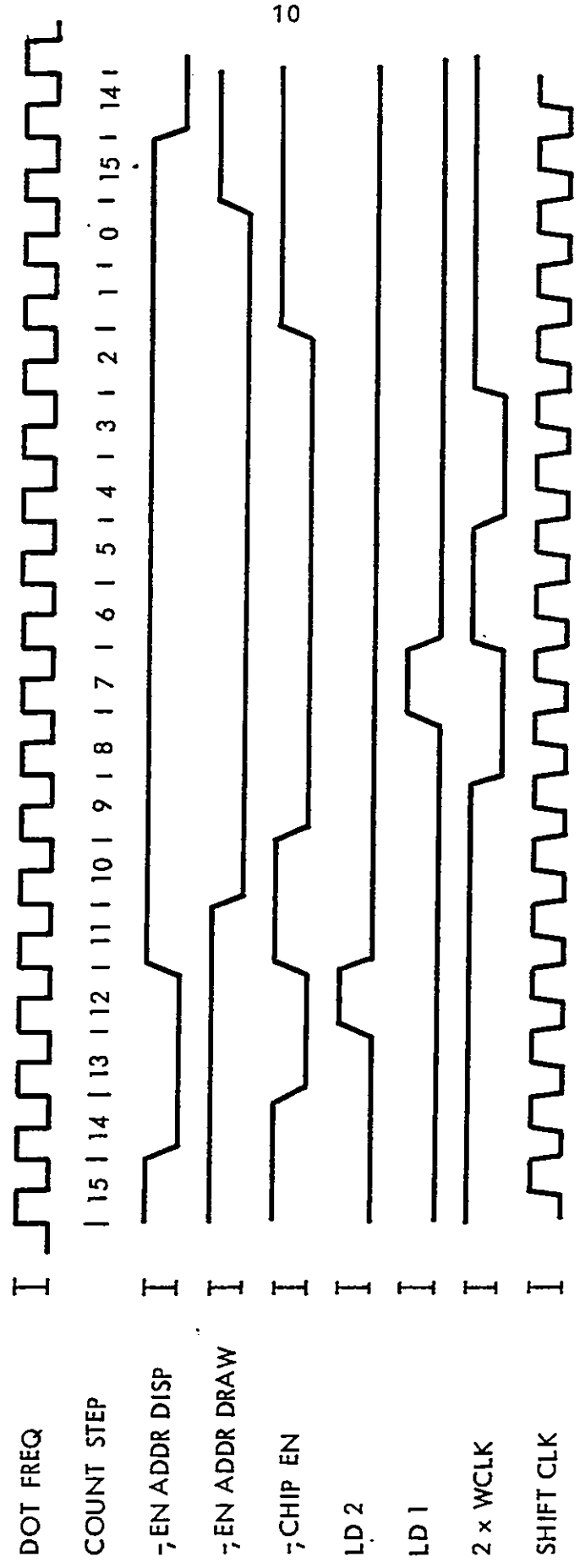
STRAP	BLACK/WHITE	Color
S2 (1-18)	OFF	ON
S2 (2-17)	OFF	OFF
S2 (3-16)	OFF	OFF
S2 (4-15)	OFF	ON
S2 (5-14)	ON	OFF
S2 (6-13)	ON	ON
S2 (7-12)	OFF	OFF
S2 (8-11)	ON	OFF
S2 (9-10)	OFF	ON

Fig. 3. Straps

Fig. 4 gives the timing details for the Black/White mode.
Fig. 7 gives the logic defination for PAT562.
Fig. 8 gives the logic definitions for PAT563.

3.3.2 Color mode

The PAT563 is replaced with PAT564 and the strapfield S2 is changed as shown above.
The control pal PAT564 aids the GDC in controlling access to the display memory. There are two types of accesses to the display memory; Display cycles and Read-Modify-Write (RMW) cycles. During display cycles, the data at the addressed location is read and sent to the shift register for subsequent display on the monitor. During a RMW cycle, data is accessed from display memory. The modifications done to the data at the addressed location are: complement, set, clear or replace.



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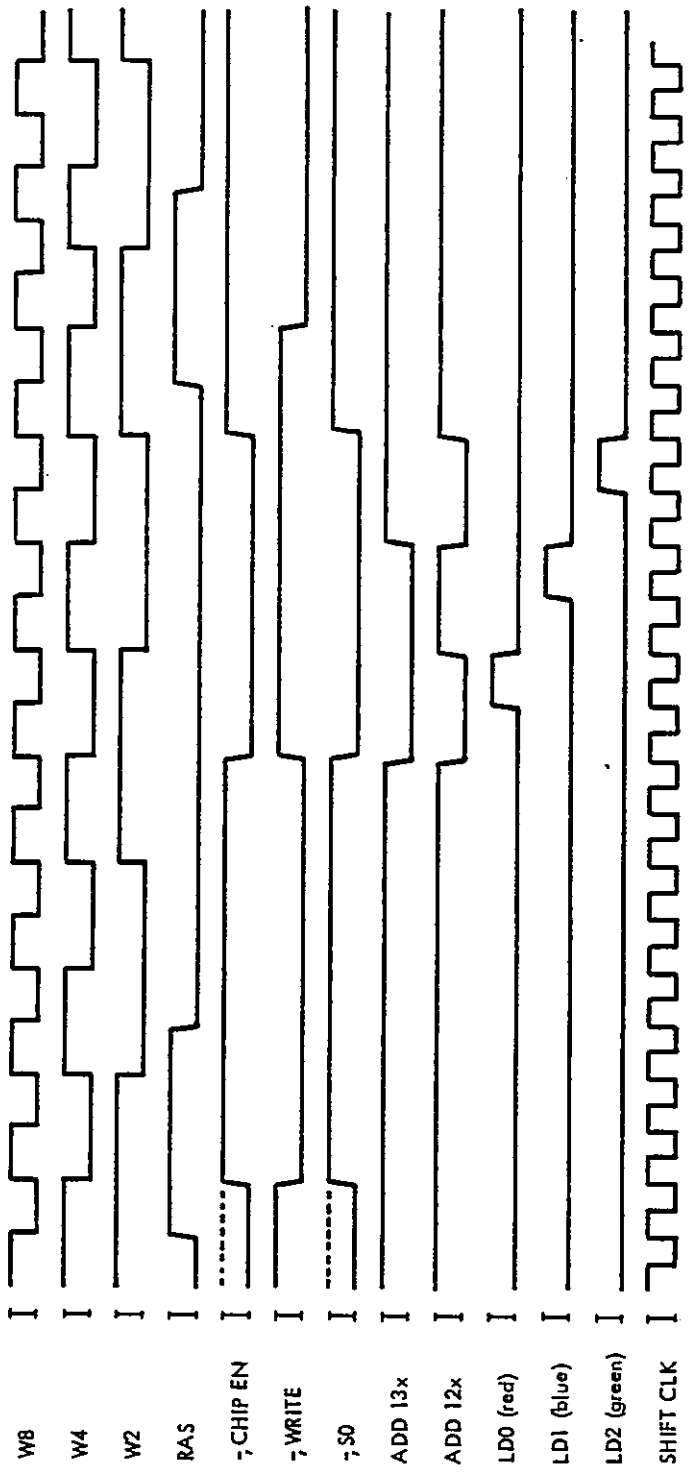
BLACK/ WHITE MODE
(PAT 562 and PAT 563)
Timing Diagram

Fig. 4.



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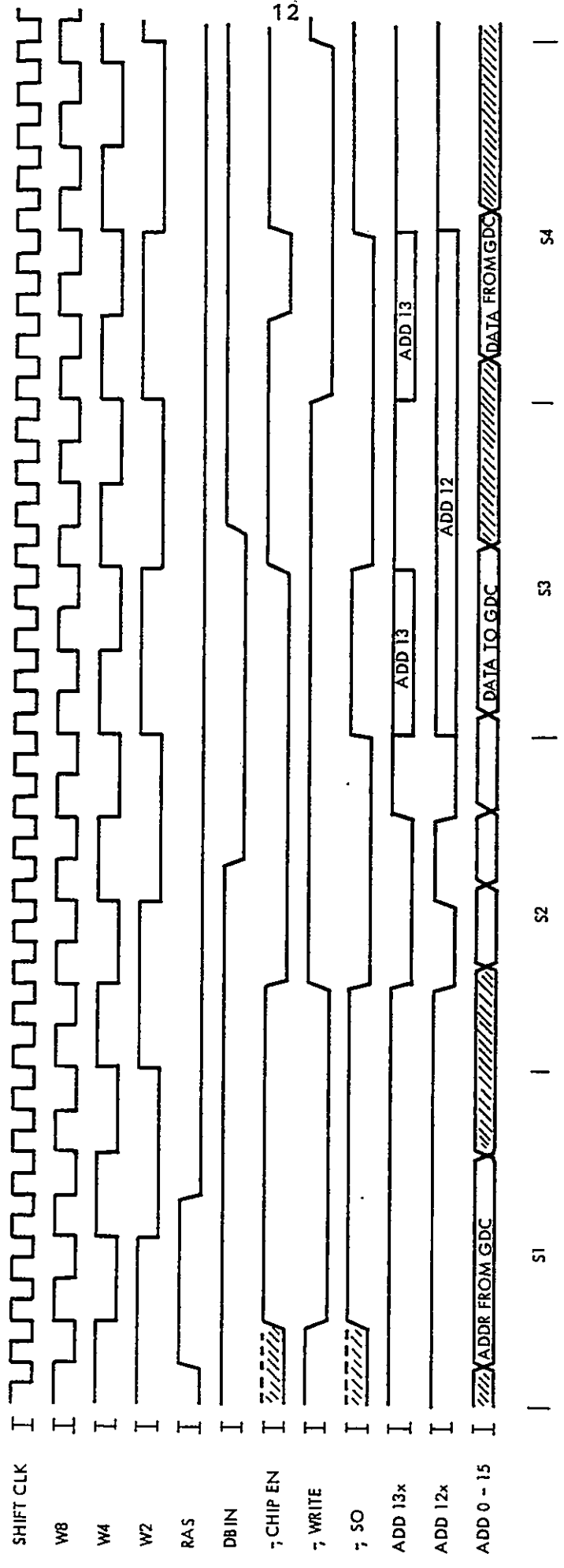
DISPLAY MEMORY CYCLE IN COLOR MODE

Timing Diagram

Fig. 5.



READ - MODIFY - WRITE MEMORY CYCLE IN COLOR MODE

Timing Diagram

Fig. 6

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```
PAL16R4                          PAL DESIGN SPECIFICATION.
PAT562                           1983.07.27;KNEH.
TIMING PULSE GENERATOR TO VPB701.

CLK HRTC /STOP S0 S1 DCLK RESET NC NC GND
/OE SHCLK /EADSP DIV W8 W4 W2 /EADRW WCLK2 VCC

/DIV := RESET + DIV + S0*STOP
/W8 :=/DIV*W8 + DIV*/W8 + S0*STOP + RESET
/W4 :=S0*/DIV*/W8*W4*/STOP*/RESET +DIV*/W4*S0*/STOP*/RESET
      +W8*/W4*S0*/STOP*/RESET +/S0*/DIV*/W8*/RESET
      +/S0*DIV*/W4*/RESET +W8*/W4*/S0*/RESET
/W2 :=/DIV*/W8*/W4*W2*S0*/STOP*/RESET
      +DIV*/W2*S0*/STOP*/RESET+W8*/W2*S0*/STOP*/RESET
      +W4*/W2*S0*/STOP*/RESET+/DIV*/W8*/W4*W2*/S0*/RESET
      +DIV*/W2*/S0*/RESET+W8*/W2*/S0*/RESET
      +W4*/W2*/S0*/RESET

IF (VCC) /SHCLK=/S0*S1*/DIV + /S0*/S1*/DCLK + S0*DCLK
IF (VCC) EADSP =S0*W2*W4*/W8 + S0*W2*W4*W8*/DIV
IF (VCC) EADRW =/S0+/W2*W4+/W2*/W4+W2*/W4*/W8+W2*/W4*W8*/DIV
IF (VCC) /WCLK2=/S0*/W2
                 +W2*/W4*/W8*/DIV*S0 + /W2*W4*W8*DIV*S0
                 +/W2*W4*/W8*/DIV*S0 + /W2*/W4*W8*DIV*S0

DESCRIPTION:
S0=0 7220 DELIVERS SYNC PULSES.
S0=1 SYNCHRONIZATION WITH HRTC PULSE FROM RC702/703.

S1=0 SHIFT CLOCK= DOT FREQ.
S1=1 SHIFT CLOCK= DOT FREQ/2.
```

Fig. 7. Pal Design Specification (PAT562)

```
PAL16L8                         PAL DESIGN SPECIFICATION
PAT563                          1983.05.29,KNEH
SHIFT REGISTER LOAD DECODER

W8 A13IN A12IN RAS DBIN W2 W4 CLK SEL GND
DIV /LD2 /LD1 A12OUT 15 16 17 A13OUT /LD0 VCC

IF (VCC) LD2=W2*W4*/W8*/DIV
IF (VCC) LD1=/W2*W4*W8*DIV
IF (VCC) /A12OUT= /A12IN
IF (VCC) /A13OUT=/A13IN
IF (VCC) /15 = W2*W4*/W8 + W2*/W4*/W8
               + /W2*W4 + /W2*/W4*W8

DESCRIPTION:

LOAD DOT PATTERN IN TIME SLOT 12.
COUNT IN ADDRESS IN TIME SLOT 7.
```

Fig. 8. Pal Design Specification (PAT563)

```
PAL16R4                          PAL DESIGN SPECIFICATION
PAT564                           1983.05.31;KNEH
DECODER

CLK A12 A13 /RAS /DBIN W2 W4 W8 SEL GND
/OE /LD2 /LD1 BS0 /CS /WE /S0 /BS1 /LD0 VCC

IF (VCC) LD0 = SEL*/W8*/W4*CS*W2*S0*/WE
IF (VCC) LD1 = SEL*/W8*W4*CS*/W2*S0*/WE
IF (VCC) LD2 = /W8*/W4*CS*/W2*/WE*S0
IF (VCC) BS1= /SEL*/A13 + SEL*/W4*CS*W2*/WE*S0
              +SEL*W4*CS*/W2*/WE*S0
              +SEL*CS*/WE*/A13*/S0
              +SEL*WE*S0*/A13
S0:= W4*/CS*W2*WE*/S0*RAS + W4*CS*/WE*S0*RAS
    +CS*W2*/WE*S0*RAS + /W4*CS*/WE*/S0*RAS + /CS*S0*RAS
WE:= /RAS + /W4*/CS*WE*/S0
    +/CS*/W2*WE*/S0 + /W4*/CS*/WE*S0
    + /CS*WE*S0

CS:= W4*/CS*W2*WE*/S0*RAS + CS*W2*/WE*RAS*S0
    +W4*CS*/WE*RAS*S0 + CS*/WE*/S0*RAS*W4
    +/CS*WE*S0*RAS + RAS*S0*/WE*CS*DBIN*/WE

/BS0:= /SEL*/A12 + SEL*W4*/CS*W2*WE*/S0
      +SEL*W4*CS*/WE*S0*/W2 + SEL*/W4*CS*/WE*S0*/A12*/W2
      +SEL*CS*/WE*/S0*/A12 + SEL*/CS*S0*/A12

DESCRIPTION:
THIS CIRCUIT IS USED IN COLOR MODE REPLACING PAT563.

SEL=1 COLOR MODE.
SEL=0 B/W   MODE.
```

Fig. 9. Pal Design Specification (PAT564)

Fig. 5 gives the timing for a display cycle.
Fig. 6 gives the timing for a Read-Modify-Write cycle.
Fig. 9 gives the logic definitions for PAT564.

3.4 Display memory 3.4

For details refer to logic diagram p.4.

The display memory consists of sixteen 16Kx1 static RAMs which provide 256K bits memory arranged as 16Kx16 bits word. The address of the display memory is calculated by the GDC and latched in the address latch. The data stored at the addressed location may be modified by the GDC, passed back to the host processor, or displayed on the attache monitor. In the black/ white mode 9,625K words are accessible as display memory. The refresh on the monitor is controlled by a counter synchronized with the video sync pulses (HRTC and VRTC) from RC702. In color mode, one block (1/4) of the display memory is available for each color (or 3/4 of the total memory).

3.5 Refresh Address Counter 3.5

For datails refer to logic diagram p.3.
This counter is only used in black/white mode to control the refresh of the graphic video on the RC702 monitor. During vertical retrace (VRTC) the counter is set to zero, indicating that the graphic picture starts at location zero of the display memory, corresponding to the upper left corner on the monitor. During horizontal retrace the counting is disabled.

3.6 Shift Register and Buffer Logic 3.6

For details refer to logic diagrams p.5 and p.6.
The shift register logic consists of three 16-bit registers (one for each color) and a series of D-flip-flaps. Each shift register performs the parallel-to-serial conversion that produces the video bit stream sent to the attached monitor. Additional D-type flip-flaps are used to resynchronize the video data with the synchronizing signals and blanking signals. In the black/white mode, only one shift register (the green) is used. The video signals are buffered and gated with the blanking signals in the PAL-circuit PAT561. This circuit is controlled by 2 straps given the following functions.

Mode	S1 S4 (1-4)	S0 S4 (2-3)	Description
Black/White	ON	ON	Graphic Video (green) is ored with RC702 character video.
Color	OFF	ON	External color Monitor. Positive HOR and VER pulses.
Color	ON	OFF	External color Monitor. Negative HOR and VER pulses.
Color	OFF	OFF	External color Monitor. Common negative sync pulse for HOR and VER.

Fig. 10.

Fig. 11 gives the logic definitions for PAT561.

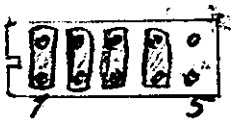
```
PAL16L8                        PAL DESIGN SPECIFICATION
PAT561                         1983.05.25;KNEH
VIDEO CONTROL CIRCUIT TO VPB701;GRAPHIC UNIT TO RC702/703.

RIN BIN VSYNC HSYNC BLSYNC /BVID VRTC HRTC VIN GND
GIN VOUT S1 S0 VER HOR ROUT BOUT GOUT VCC

IF (VCC) /VOUT = /S0*/S1*/VIN*BVID + /S0*/S1*HRTC*/VIN + /S0*/S1*VRTC
                 +/S0*/S1*/VIN*/GIN*/BVID + S0*/VIN + S1*/VIN
IF (VCC) /GOUT = BVID + BLSYNC + /GIN
IF (VCC) /BOUT = BVID + BLSYNC + /BIN
IF (VCC) /ROUT = BVID + BLSYNC + /RIN
IF (VCC) /HOR  = /S0*S1*/HSYNC + S0*/S1*HSYNC + /S0*/S1 + S0*S1
IF (VCC) /VER  = /S0*S1*/VSYNC + S0*/S1*VSYNC
                 +S0*S1*VSYNC + S0*S1*HSYNC + /S0*/S1

DESCRIPTION:

 S0  S1 !     FUNCTION
-------------------------------------------------------------
  0   0 ! INTERNAL  BLACK/WHITE
  0   1 ! EXTERNAL MONITOR POSITIVE HOR;VER PULSES
  1   0 ! EXTERNAL MONITOR NEGATIVE HOR;VER PULSES
  1   1 ! EXTERNAL MONITOR COMMON NEGATIVE SYNC PULSE FOR
        ! BOTH HOR AND VER SEND ON PIN15.
-------------------------------------------------------------
```

Fig. 11. Pal Design Specification

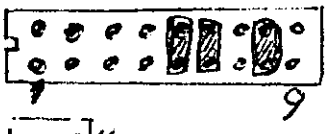
4. LOGIC DIAGRAMS

Jumper setting, Black, white.

S1 =

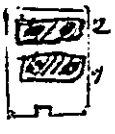


S2 =



S3 =

S4



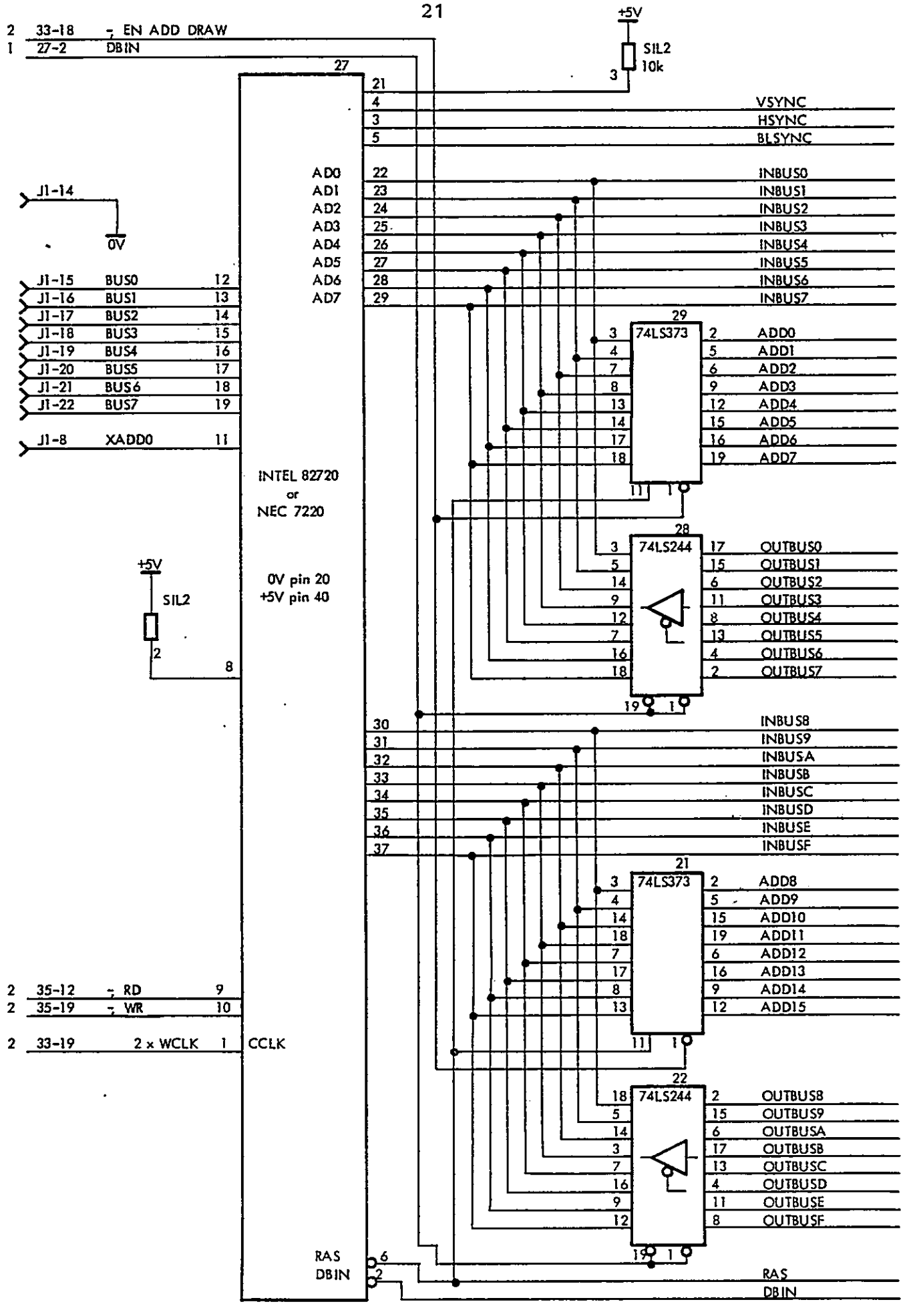
SIGNAL	DESTINATION	DESCRIPTION
ADD O-13	p. 9	Output from the address latch bit 0-11. Address for a GDC memory cycle.
BLSYNC	p. 6	Blanking signal from the GDC to be anded with the video signal.
DBIN	p. 2 p. 3	Data Bus Input Enable The assertion of the DBIN identifies the time the GDC will accept the data read from ram during RMW cycles.
HSYNC	p. 6	Horizontal SYNC output.
Inbus O-F	p. 4	Input data Bus bit O-F to the ram memory.
Outbus O-F	p. 7	Output data Bus from the ram memory.
RAS	p. 2	Address latch enable signal. This signal identifies the start of a memory cycle from the GDC.
VSYNC	p. 6	Vertical SYNC output

Designed by

Drawn by

Dwg. Office Check

Unit VPB701	Signal List	p.1
Dwg. No: A26276		



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VPB 701

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GRAPHICS DISPLAY CONTROLLER

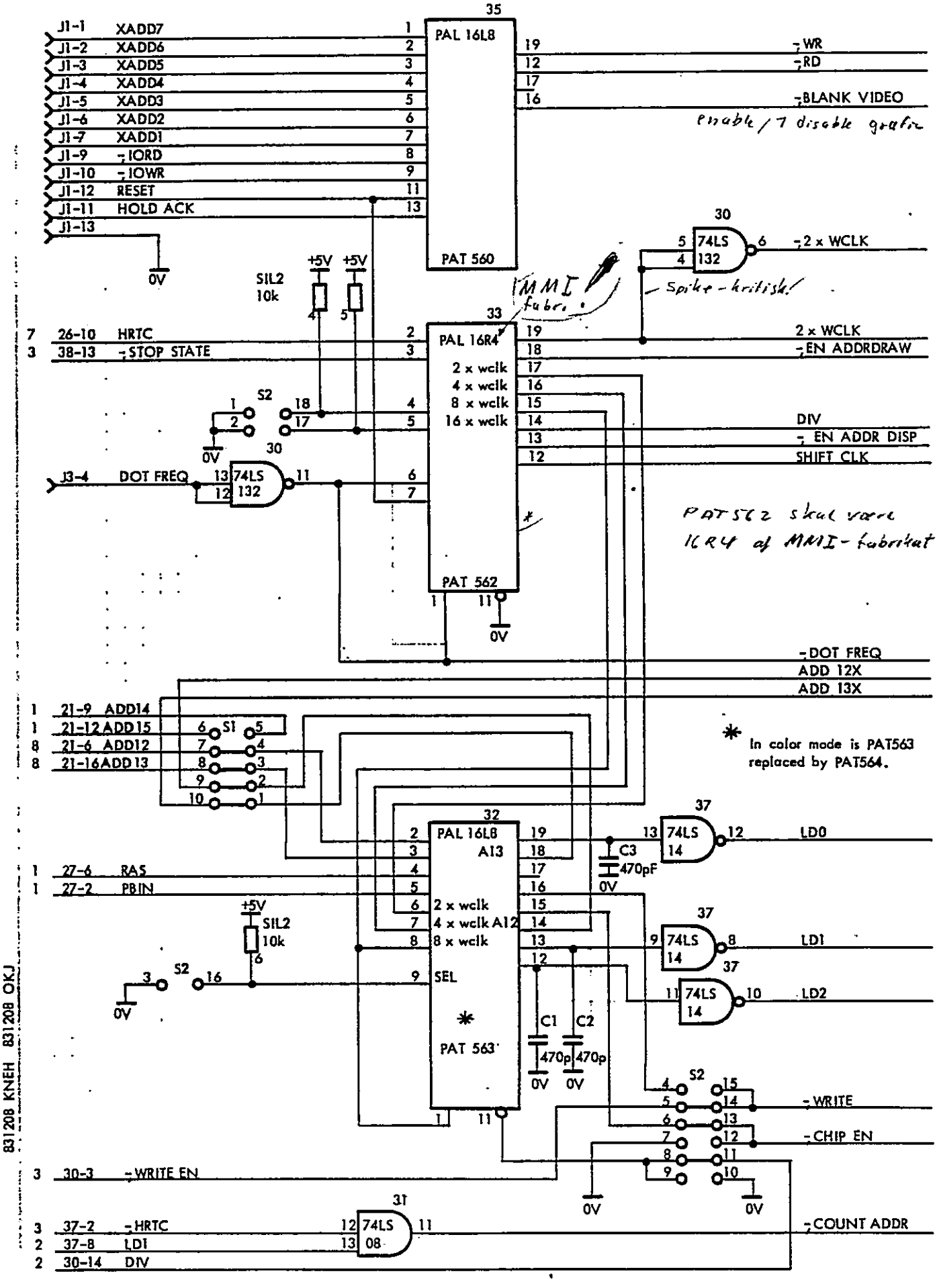
Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
ADD12X-13X	p. 4	Most significant address bits to the ram memory.
>Blank video	p. 6	Output from the Blank Flag. Used to blank the graphic video, controlled by software.
>Count addr	p. 3	Count signal to the RC702 address counter. This signal is disabled during horizontal retrace (HRTC).
>Chip en	p. 4	> Chip enable to the ram chips.
DIV	p. 2	Clock signal. DOT FREQ/2.
>DOT FREQ	p. 7	Dot Frequensy from RC702. ≃ 10M.HZ
>EN ADDR DISP	p. 3	>ENable the RC702 address counter output.
>ENADDR DRAW	p. 1	>ENable the GDC address latch.
LDO	p. 5	Load red video shift register. (only used in color mode).
LD1	p. 3 p. 5	Color mode: Load blue video shift-register. Black/White: trigger to RC702 synchronization circuit.
LD2	P. 5	Load green video (also used as black/white) shift register.
>RD	p. 1	Host processor read pulse to the GDC.
>WRITE	p. 4	Write pulse to the ram memory
>WR	p. 1	Host processor write pulse to the GDC.
SHIFT CLK	p.5	Shift clock to the video shift registers and pipe line registers.
2xWCLK	p. 1 p. 3 p. 6	GDC word clock.
> 2xWCLK	p. 3	Same as above.

Designed by

Drawn by

Dwg. Office Check



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VPB 701

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RC 702 I/O INTERFACE
CLOCK TIMING CIRCUIT
Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
ADD 0-13	p. 8	Address output from the RC702 address counter.
> HRTC	p. 2	Horizontal sync pulse from the RC702 video circuit.
> WRITE EN	p. 2	> WRITE Enable to the ram memory.
> STOP STATE	p. 2	Synchronization of the timing circuit to the RC702 video timing.
1-gen	p. 5 p. 6	

Designed by

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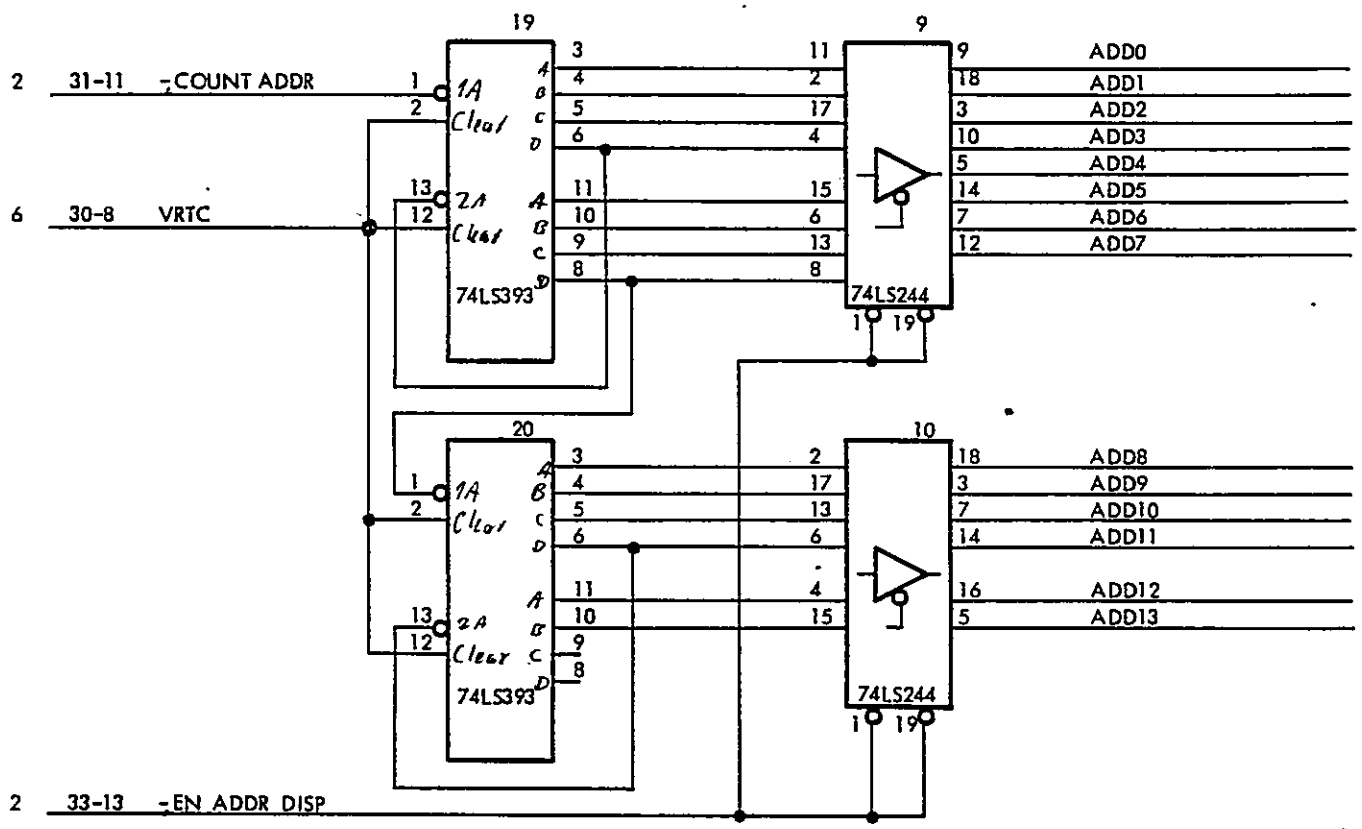

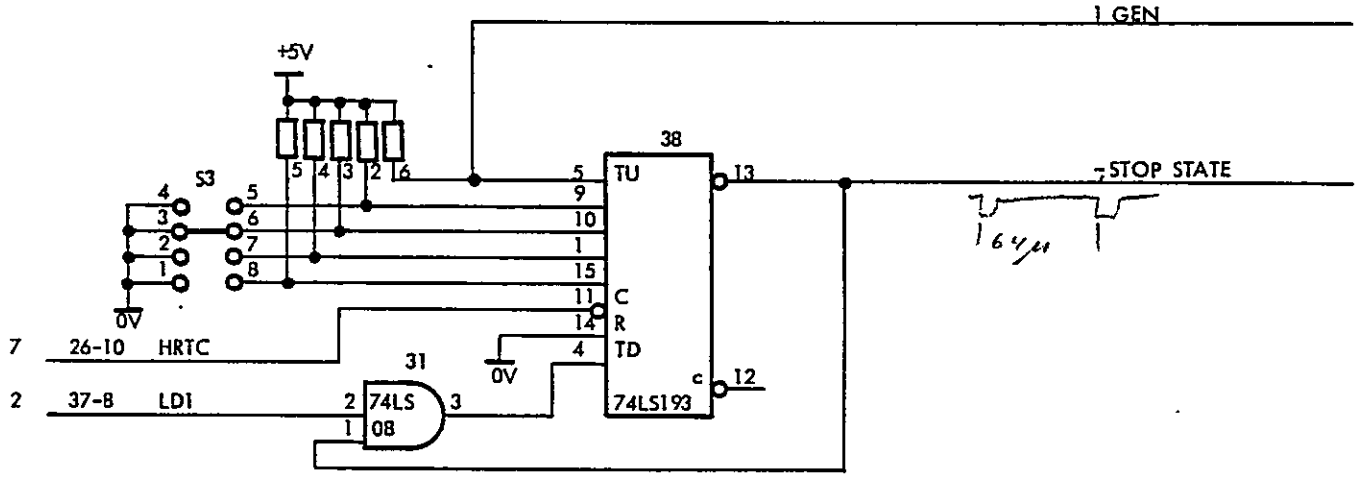

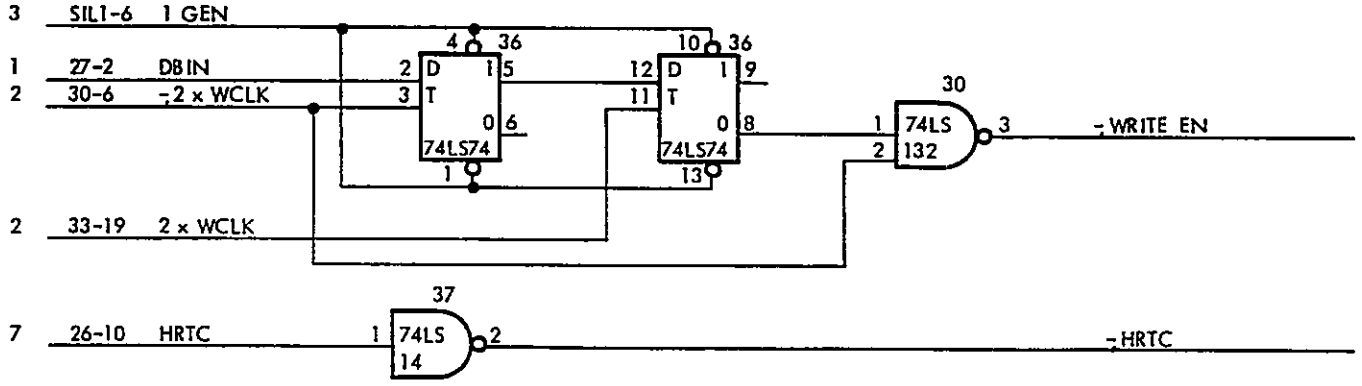

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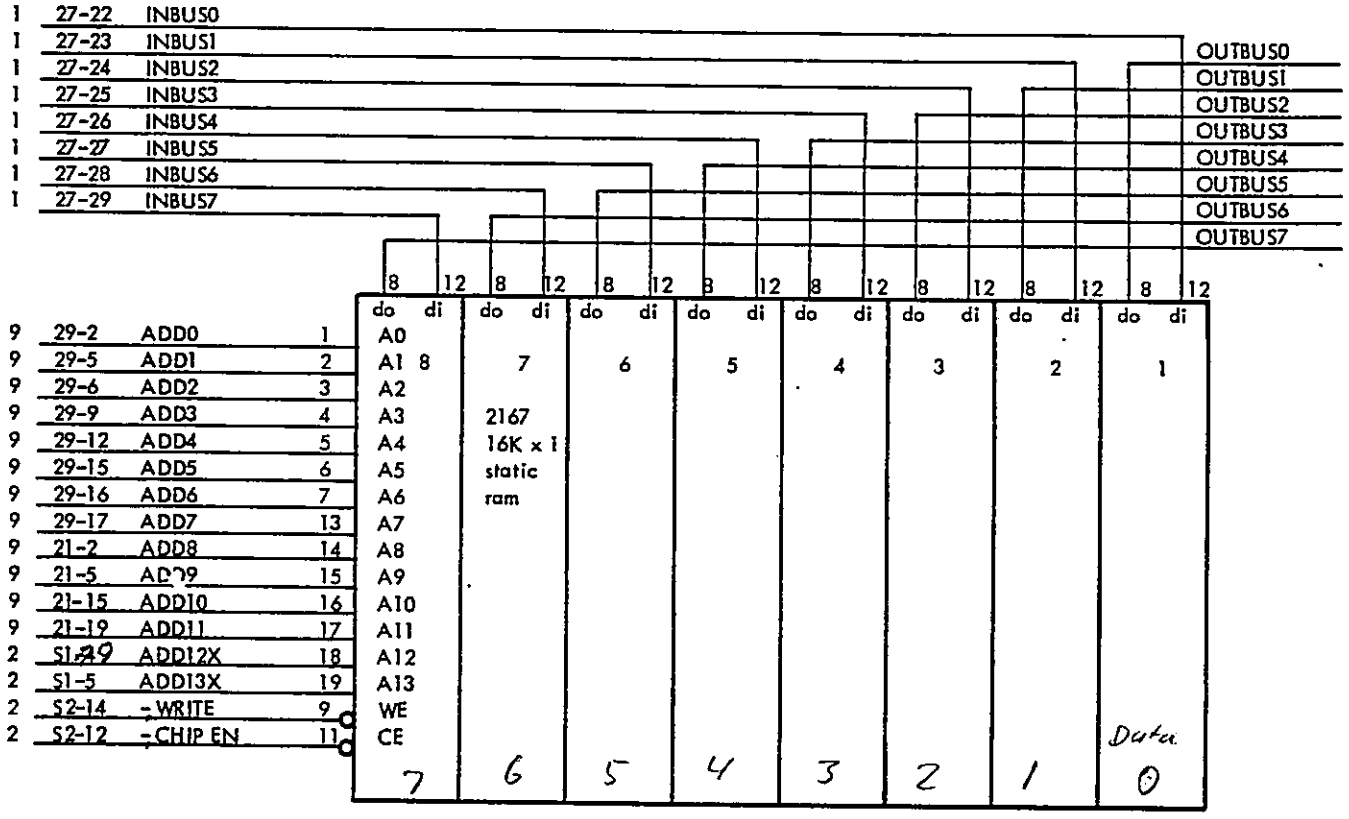
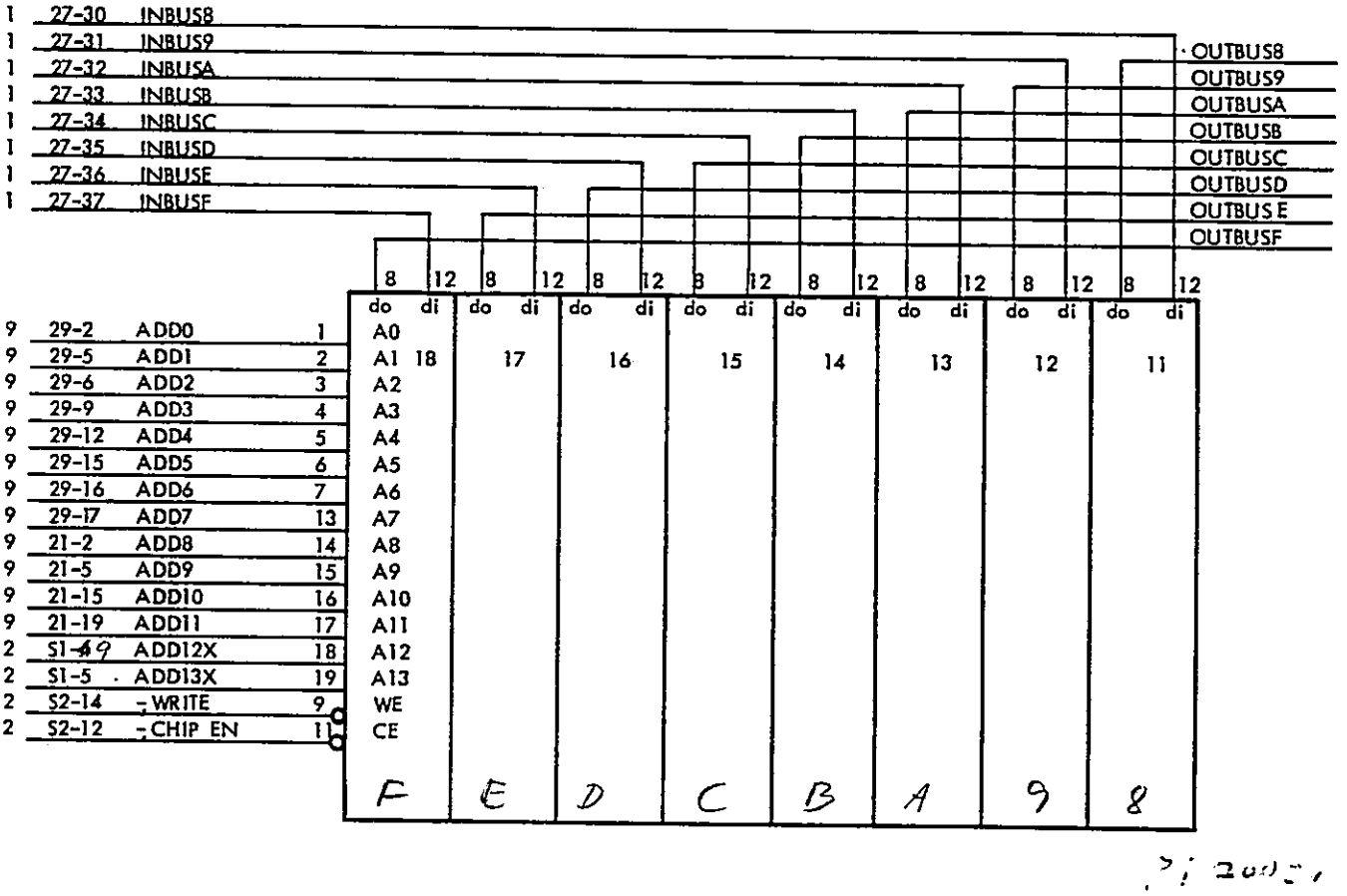
SIGNAL	DESTINATION	DESCRIPTION
OUTBUS 0-F	p. 7	OUTput data BUS bit 0-F from the ram memory.

Designed by

Drawn by

Dwg. Office Check





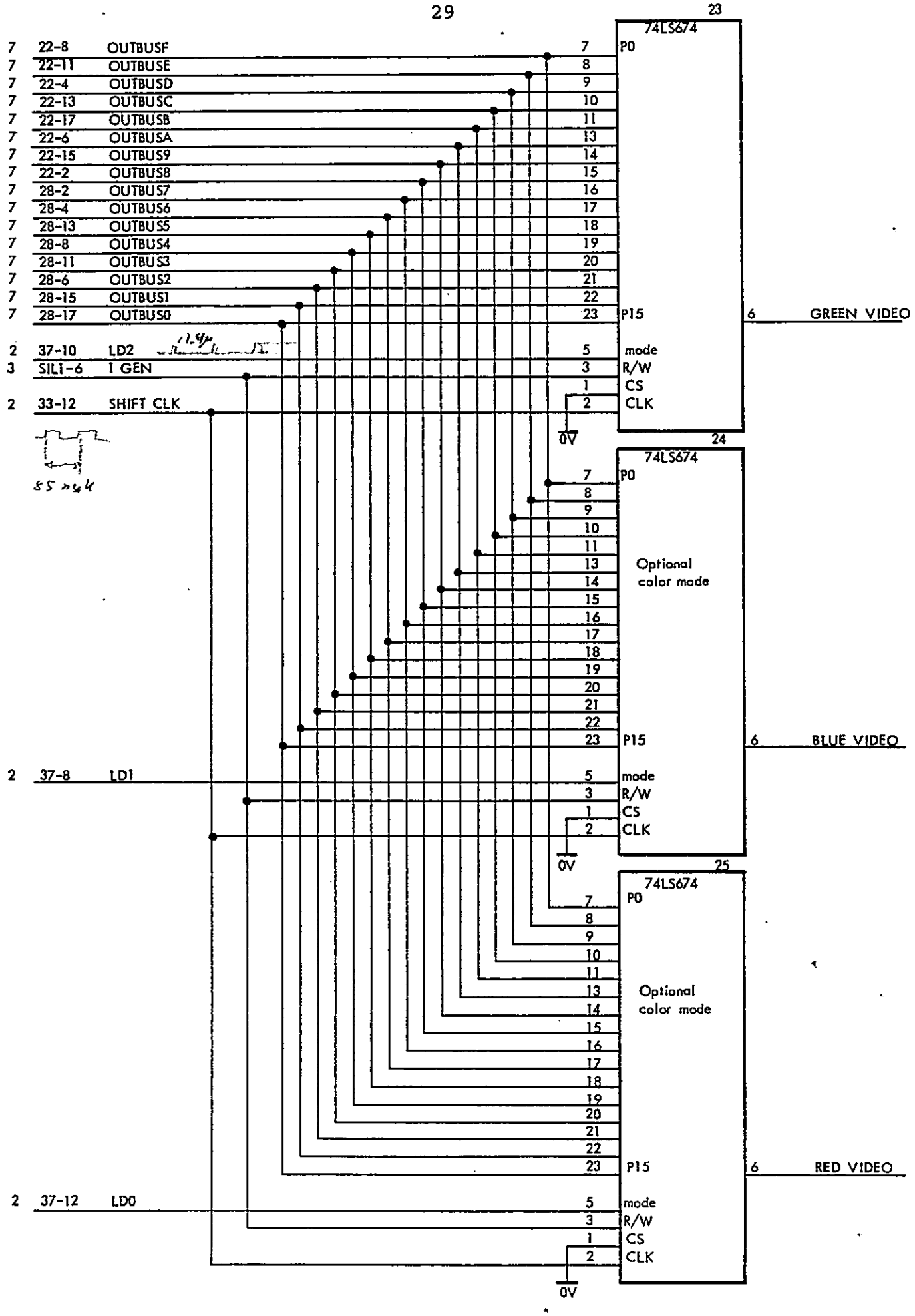
831208 KNEH 831208 OKJ

SIGNAL	DESTINATION	DESCRIPTION
Blue video	p. 6	
Green video	p. 6	
RED video	p. 6	

Designed by

Drawn by

Dwg. Office Check



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VPB 701

A14594

VIDEO SHIFT REGISTER

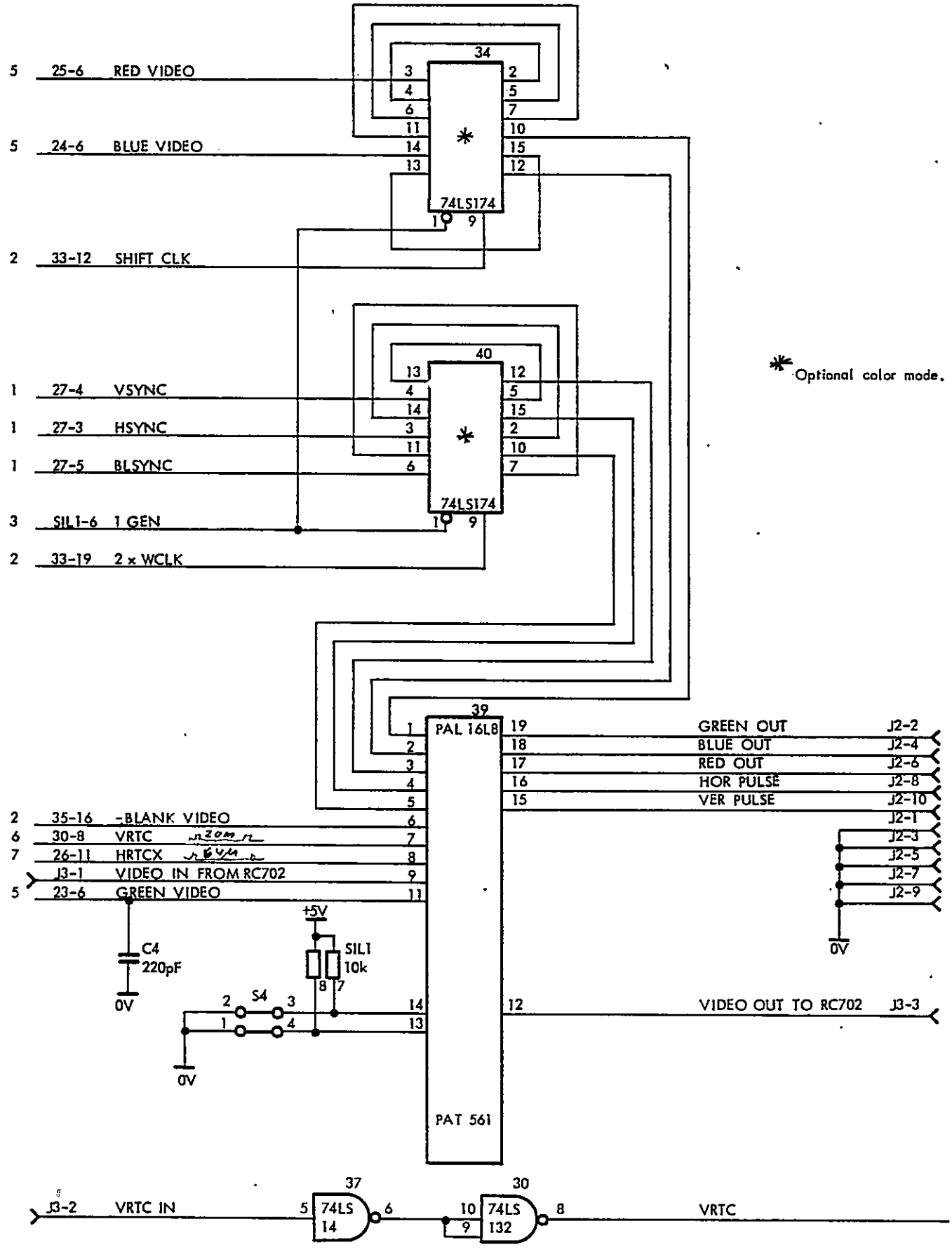
Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
BLUE OUT	J2	BLUE video OUTput to external color monitor.
GREEN OUT	J2	GREEN video OUTput to external color monitor.
RED OUT	J2	RED video OUTput to external color monitor.
VER PULSE	J2	VERtical retrace pulse to external color monitor.
VIDEO OUT TO RC702	J3	RC702 character video ored with the graphic video.
VRTC	p. 3	Vertical retrace pulse from RC702 video circuit.
HOR PULSE	J2	VERtical retrace pulse to external color monitor.

Designed by

Drawn by

Dwg. Office Check



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VPB 701

A14595

VIDEO CONTROL CIRCUIT

Circuit Diagram

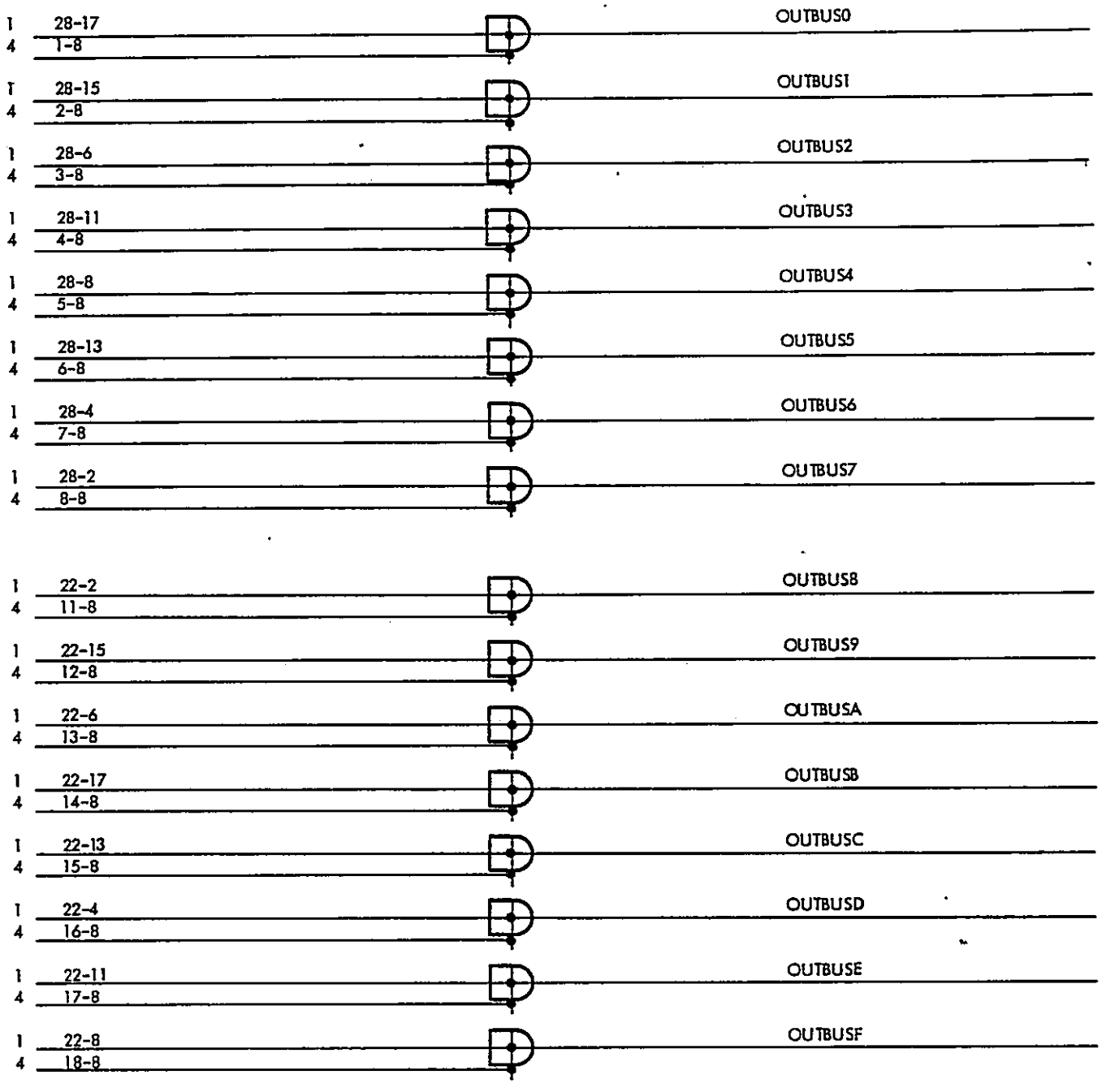
p. 6.

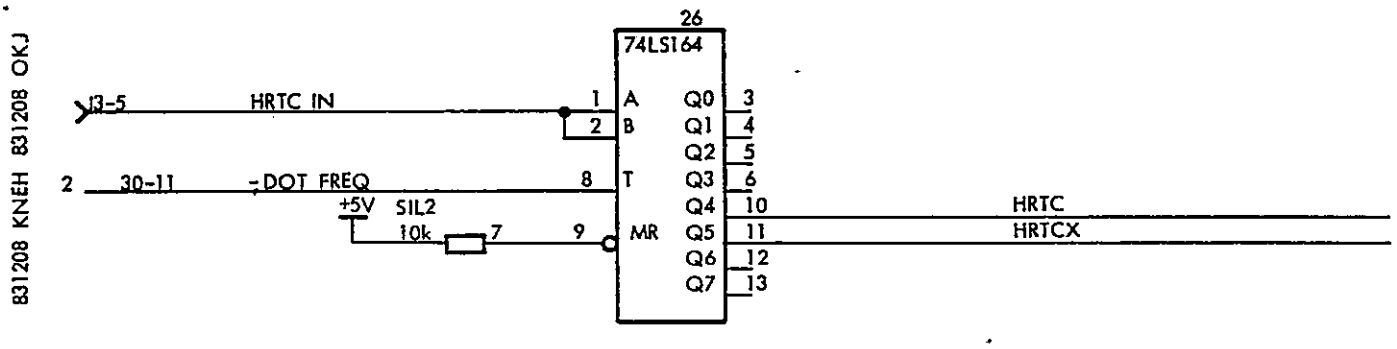
SIGNAL	DESTINATION	DESCRIPTION
HRTC	p.2 p.3	Horizontal retrace from RC702 delayed by 5 dot clocks.
HRTCX	p.6	Horizontal retrace from RC702 delayed by 6 dot clocks.

Designed by

Drawn by

Dwg. Office Check


1 28-17 4 1-8 OUTBUS0
1 28-15 4 2-8 OUTBUS1
1 28-6 4 3-8 OUTBUS2
1 28-11 4 4-8 OUTBUS3
1 28-8 4 5-8 OUTBUS4
1 28-13 4 6-8 OUTBUS5
1 28-4 4 7-8 OUTBUS6
1 28-2 4 8-8 OUTBUS7
1 22-2 4 11-8 OUTBUS8
1 22-15 4 12-8 OUTBUS9
1 22-6 4 13-8 OUTBUSA
1 22-17 4 14-8 OUTBUSB
1 22-13 4 15-8 OUTBUSC
1 22-4 4 16-8 OUTBUSD
1 22-11 4 17-8 OUTBUSE
1 22-8 4 18-8 OUTBUSF

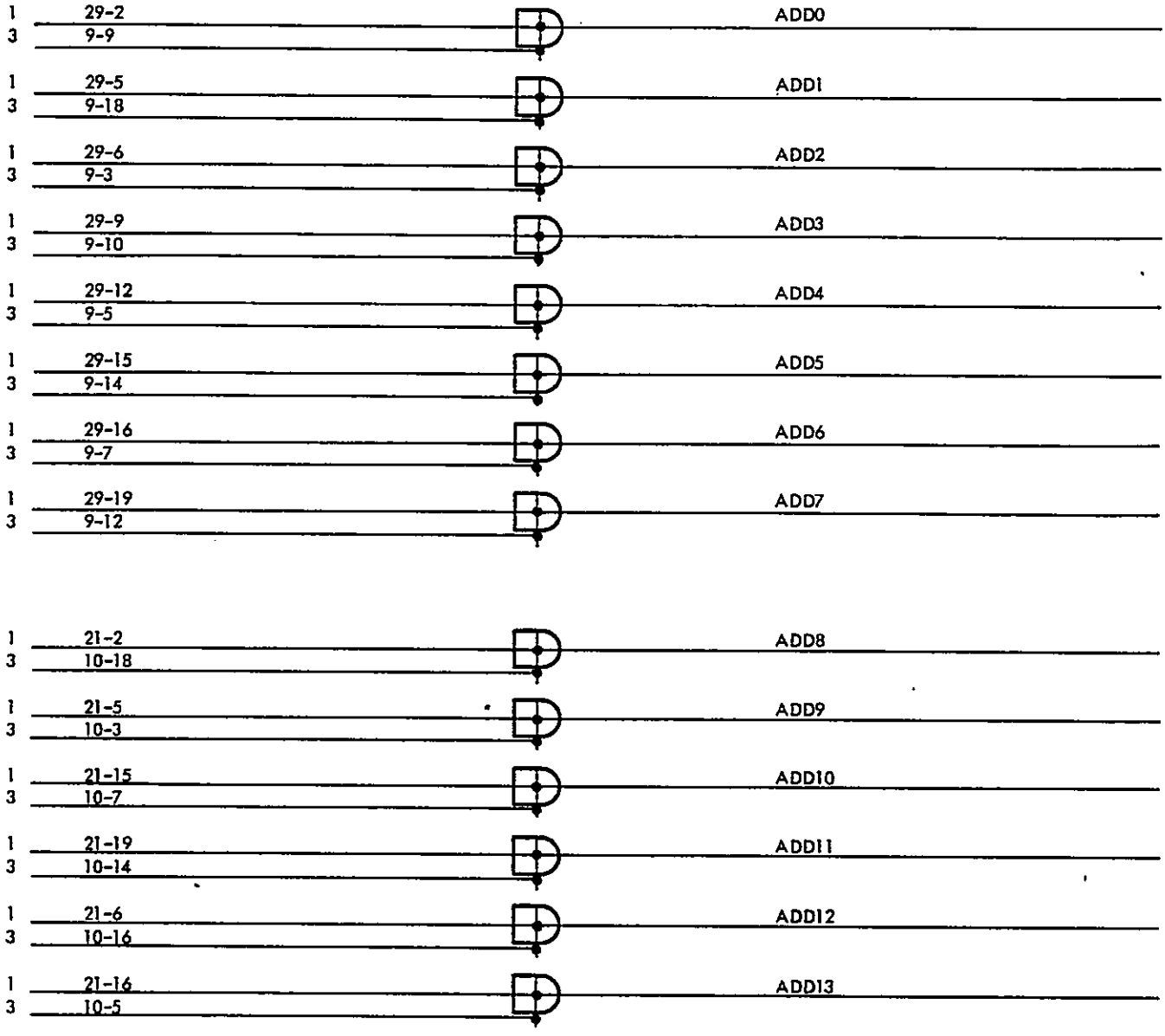

831208 KNEH 831208 OKJ
26
74LS164
13-5 HRTC IN
2 30-11 -DOT FREQ
+5V SIL2
10k
A B T MR
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
HRTC
HRTCX

SIGNAL	DESTINATION	DESCRIPTION
ADD 0-11	p. 4	ADDress input bit 0-11 to the ram memory.
ADD 12-13	p. 2	Color plane module select in color mode. Normal address input in Black/White mode.

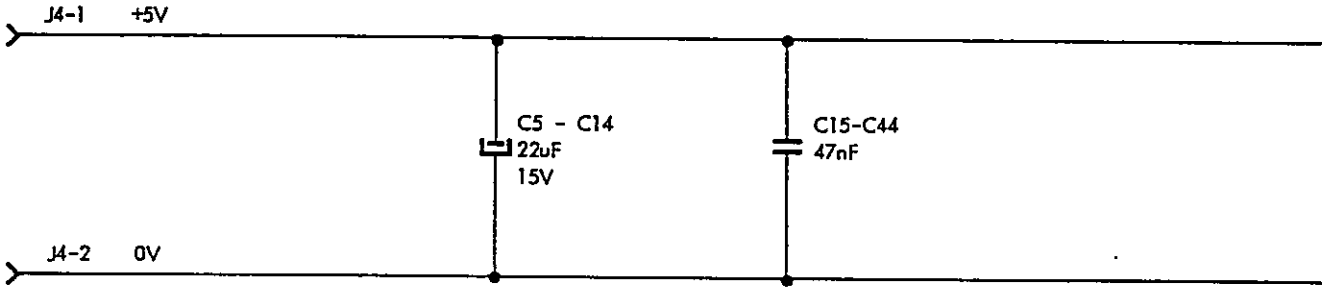
Designed by

Drawn by

Dwg. Office Check



831208 KNEH 831208 OKJ



5. ASSEMBLY DRAWINGS

Fig. 12 contains signal lists for all connectors on VPB701.

Fig. 13 contains a wiring list between VPB701 and the DMA controller in the RC702/703 microcomputer.

Fig. 14 shows the cabling to the RC702 main printed circuit board.

Fig. 15 shows the placing of the IC's on VPB701.

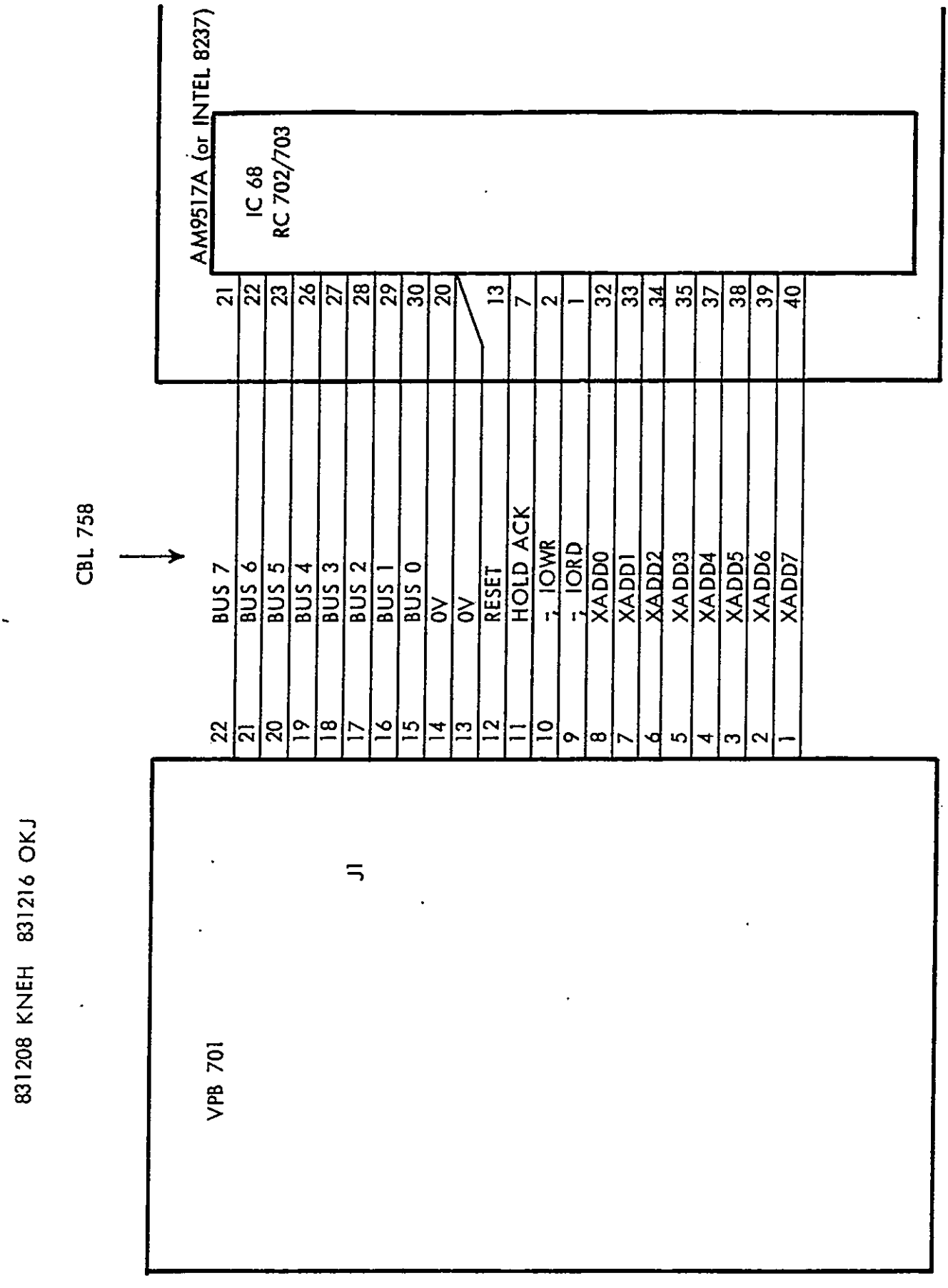
J1 CONNECTOR TO RC 702 DMA SOCKET	
Pin	Signal name
1	ADD 7
2	ADD 6
3	ADD 5
4	ADD 4
5	ADD 3
6	ADD 2
7	ADD 1
8	ADD 0
9	¬ IORD
10	¬ IOWR
11	HOLD ACK
12	RESET
13	0V
14	0V
15	BUS 0
16	BUS 1
17	BUS 2
18	BUS 3
19	BUS 4
20	BUS 5
21	BUS 6
22	BUS 7

J2 CONNECTOR TO EXTERNAL COLOR MONITOR	
Pin	Signal name
1	0V
2	GREEN OUT VIDEO
3	0V
4	BLUE OUT VIDEO
5	0V
6	RED OUT VIDEO
7	0V
8	HOR SYNC PULSE
9	0V
10	VER SYNC PULSE

J3 CONNECTOR TO RC 702 VIDEO CIRCUIT	
Pin	Signal name
1	VIDEO IN FROM RC 702
2	VRTC
3	VIDEO OUT TO RC 702
4	DOT FREQ
5	HRTC

J4 POWER CONNECTOR	
Pin	SIGNAL NAME
1	+5V
2	0V

831205 KNEH 831216 OKJ



VPB 701

Wiring List

Fig. 13

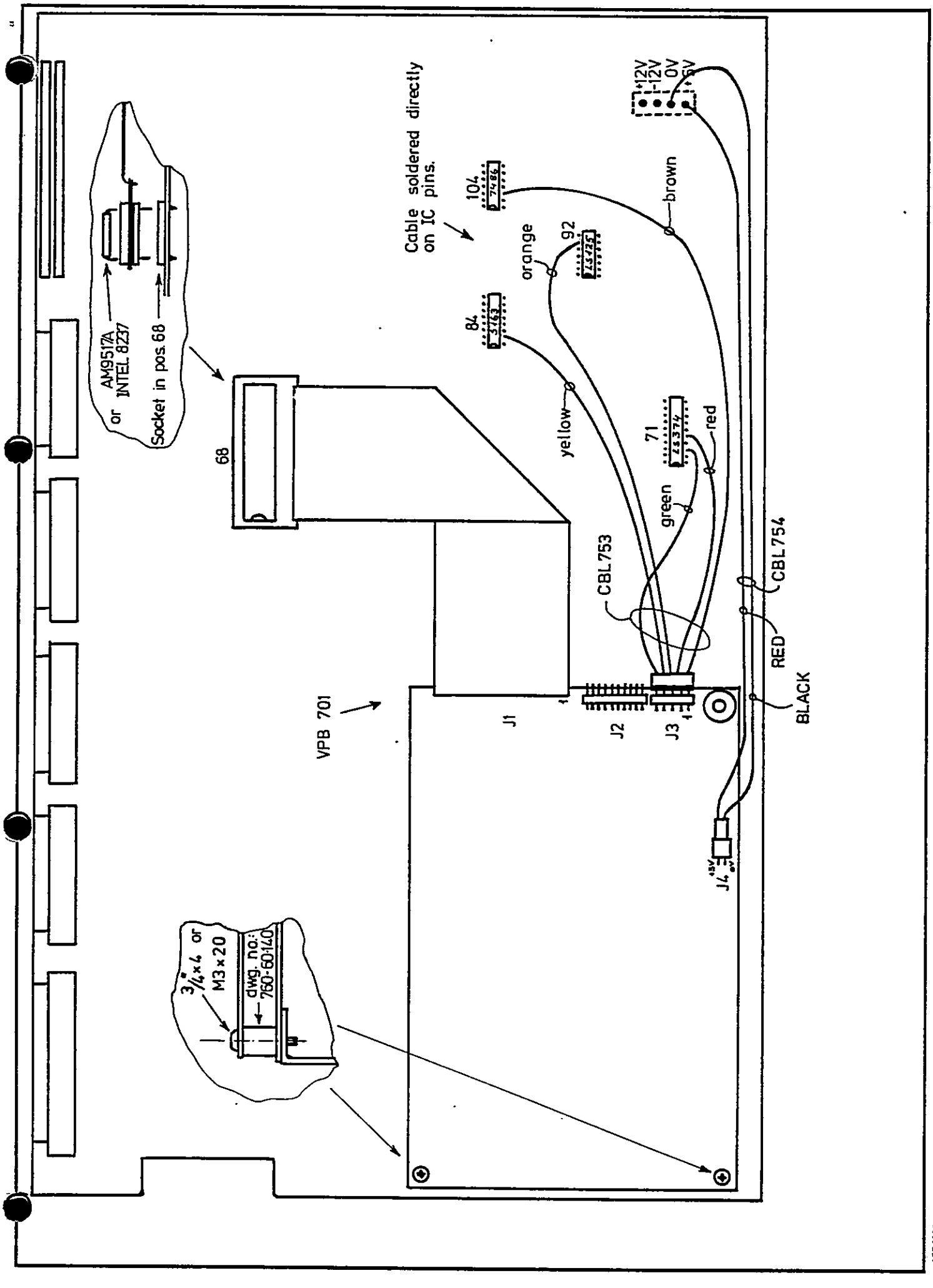


Fig. 14: Installation of VPB701 in RC702/703

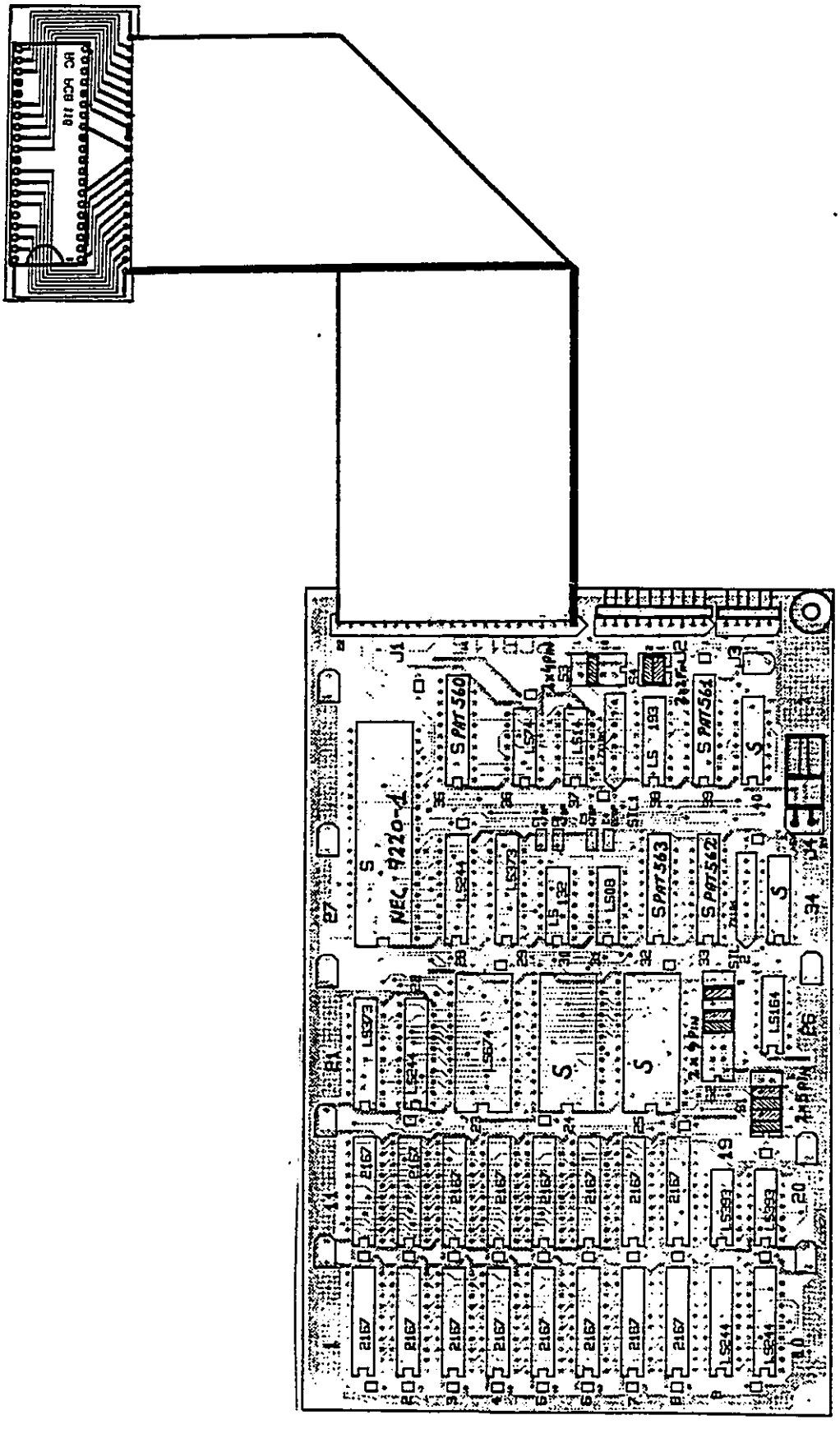


Fig. 15: Assembly Drawing.

6. POWER REQUIREMENTS

+5V (+ 5%) 1.5A max.

A. INDICES

A.

A.1 Survey of Figures

A.1