6-7-73 SRN

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Author: Jørgen Carøe
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RC 3500
GENERAL PURPOSE CONTROLLER
GENERAL INFORMATION

Keyword: RC 3500 General Purpose Controller, General Information, Hardware

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Abstract: This paper describes the hardware modules of RC 3500; furthermore it informs about the instruction set and how to operate the RC 3500.

A/S REGNECENTRALEN
3-9, Guldsmedgade
8000 Aarhus C.

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3500 General Purpose Controller is essentially a minicomputer which combines a very fast Interrupt Handling with an Input/Output system featuring low-cost-cabling and great flexibility in physical placing of the attached peripheral devices.

3500 operates with 32 interrupt levels each containing a set of 4 registers. One of the registers contains a program counter and a carry indication, whereas the remaining 3 registers act as accumulators or index registers. A selectable fixed priority of the interrupt levels secures suitable handling of high and low speed I/O devices.

3500 makes it possible to switch from one program to another within a few microseconds.

3500 contains 32 I/O channels which are capable of handling 32 medium speed I/O devices (< 100 000 char./sec.) or up to 256 low speed I/O devices (< 60 char./sec.). Direct Memory Access (DMA) is optional.

Each of the 32 I/O channels can be connected to the most suitable interrupt level.

3500 operates the 32 I/O channels in a STAR-coupling keeping all encodings and decoding of addresses internal in the computer.

Input and output is performed in serial mode (except for DMA) whether the device connected is a serial or a parallel device.

Transmission rate: 5M bit/sec.

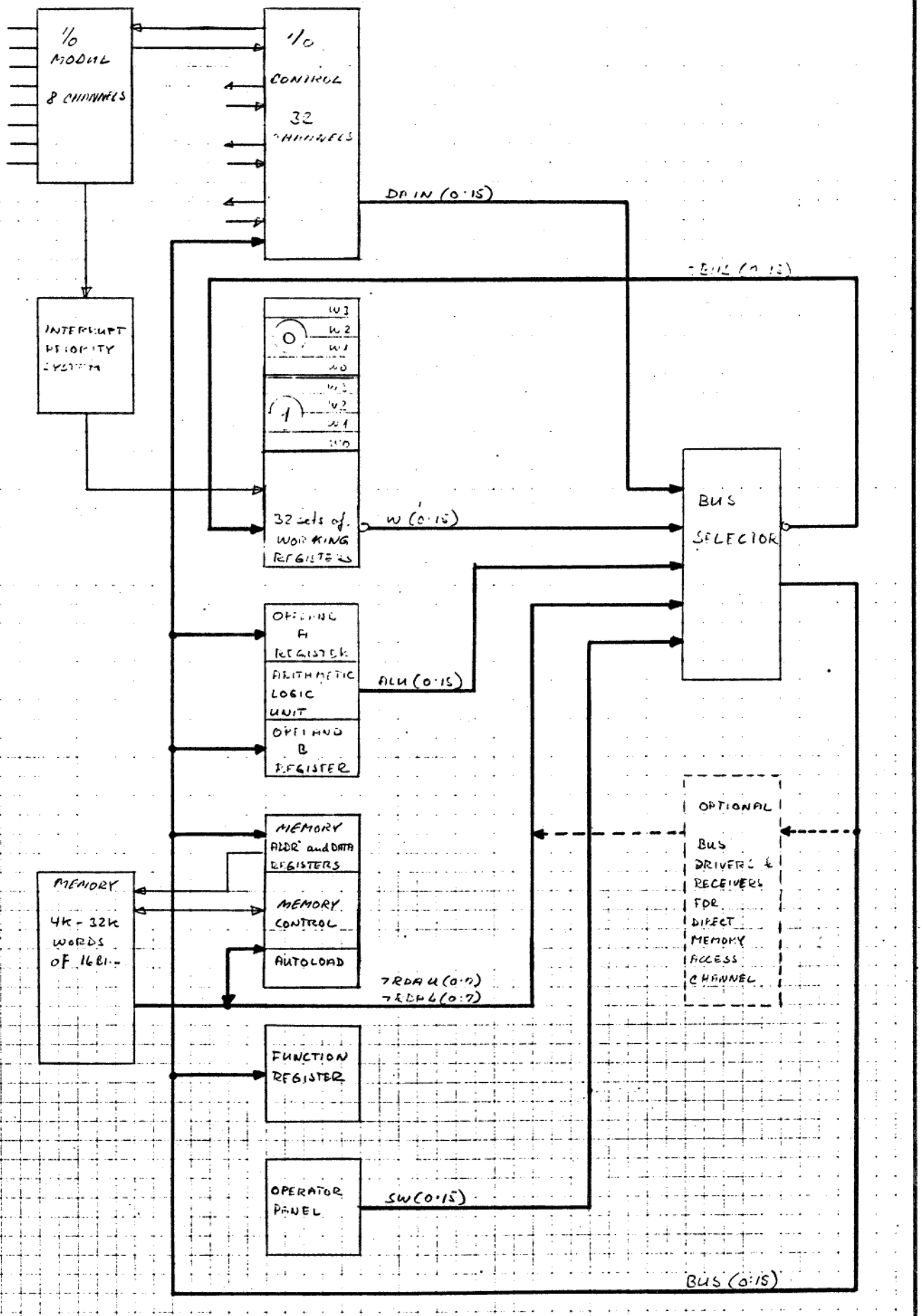
The serial transmission is performed over a 4 pairs cable for each I/O channel using magnetic insulators at each end of the cable to ensure the great noise immunity.

Memory:	Fully integrated MOS memory. Basic storage: 4096 words of 16 bits expandable up to 32768 words in modules of 4096 words. Fully expandable within the basic frame. (Magnetic core optional). Cycle time: 950 nSec. (675 nSec., 450 nSec. optional). Access time: 550 nSec. (450 nSec., 325 nSec. optional).
Memory addressing:	8-bit bytes and 16-bit words are direct addressable.
Arithmetic:	Parallel 16-bit binary integers, two's complement arithmetic.
Interrupt levels:	32 interrupt levels are included in the basic version.
Working registers:	32 sets of 4 registers, fully integrated. Access time: 60 nSec.
Instruction set:	50 instructions of which 30 refer to the memory.
Instruction form:	1, 2, or 3 consecutive words.
Input/Output:	Basic version 8 I/O channels expandable to 32 in modules of 8. Mode of transmission: Serial. Cables: 4 pairs, impedance: 100 Ohm nom. Cable coupling: Magnetic insulators. Cable length: 100 meters max. (Direct Memory Access channel is optional available).

Available interfaces:	48K bits/sec. synchron interface. 2400-9600 bits/sec. synchron interface. 0-1200 bits/sec. asynchron multiplexer for 8 or 16 devices attached to one I/O channel. Single low speed asynchron interface. RC 500, RC 2500 paper tape reader interface. RC 4070 paper tape punch interface. Matrix printers. Line printers. RC 804 low speed datatransmission display. RC 810 high speed special display. RC 811 display system. Any other interface available on request.
Initial loading:	An autoload function may be supplied enabling initial load or reload from a paper tape reader, a high speed data transmission line or any suitable source.
Dimensions	
Table model:	Height: 45 cm, width: 42 cm, depth: 60 cm.
Weight:	50 kg.
Power requirements:	220V AC $\pm$ 10%, 50/60 Hz, 600V A.
Temperature:	10°-40° Celsius.
Relative humidity:	90% max.
Software:	Assembler program for the RC 4000 and the CDC Cyber (called SLAM). Driver and monitor programs for each standard interface.

Reference: RCSL 52-AA316, RC 3500 Reference Manual

RCSL 52-AA319, RC 3500 Assembler Manual



Unit 3-00	FUNCTIONAL UNITS AND DATA FLOW IN 3500 GENERAL PURPOSE CONTROLER	fig 1
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OPERATIONAL DESCRIPTION 2

The primary design objectives of the 3500 General Purpose Controller were to construct a low cost minicomputer with a flexible input/output system and with a powerful instruction set for ease of programming. Furthermore, peripheral devices should be connected to the computer with a minimum of interfacing.

The 3500 processes 16-bit binary integers in parallel using two's complement notation. The signed numbers used as displacement in referencing memory and as operands for the arithmetic instructions utilize the two's complement representation for negatives. In a word or byte used as a signed number, the left most bit represents the sign, 0 for positive, 1 for negative. In a positive number the remaining bits are the magnitude in ordinary binary notation. The negative of a number is obtained by taking its two's complement, with the sign bit included in the operation as though it were a more significant magnitude bit.

Working Registers. 2.1

Internal registers of importance to the programmer are three 16-bit general registers, one 15-bit program counter, and a carry indication. The advantage of more than one general register is that it reduces the number of storage references required in a given program. The general registers of the 3500 computer act both as accumulators and index registers, for which reason the full instruction set becomes available for address modifications. The collection of the above-mentioned programmable registers is referred to as a set of working registers.

The computer has not only one set of working registers, but 32 sets, namely one for each interruption level. Hence, we have eliminated the storing of current status (program counter, carry, and accumulators) and loading of new status, whenever program switching is demanded by the

interruption system. The response time for answering an interrupt is thus reduced to a minimum, and the input/output system is designed to take full advantage of this fact.

Figure 2.1 depicts the working registers, W0 to W3, associated to each interruption level.

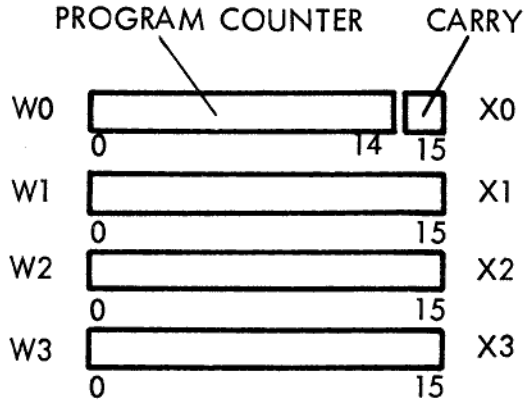

Figure 2.1.1. A Set of Working Registers

Registers W1 to W3 are used by the programmer both as accumulators and index registers, in the latter case they are referred to as X1 to X3. Register W0 occupies, in some respects, an exceptional position, because bits 0 to 14 specify the program counter, PC, and bit 15 equals the value of CARRY. Fifteen bits are just enough to locate any instruction in storage, since instructions are always an integer number of full words.

Although there is a distinction in interpretation of W0 and the other registers, they are all alike with respect to instruction execution. By this we mean that any instruction which is executed with an operand in, say W2, also is executed if the operand were placed in W0. For example, a LOAD instruction may load any of the W registers with a word from storage, but, of course, loading of W0 has the special effect of executing a program jump.

Inter register load and store instructions are also provided, which makes it possible to transfer information between W registers belonging to the same or different interruption levels.

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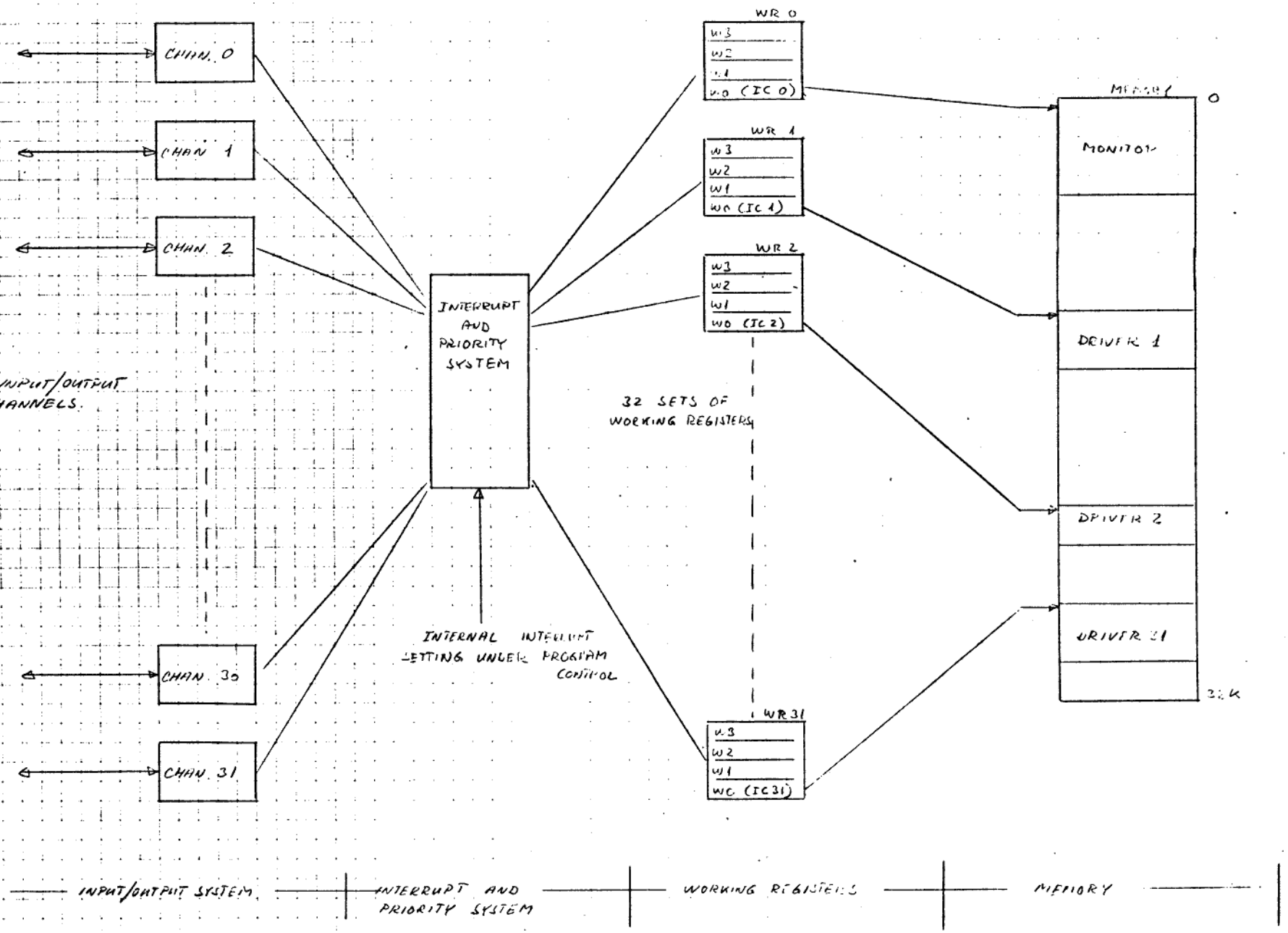
3500 INTERRUPT AND WORKING REGISTER STRUCTURE

Rig 2.1.2



Function Register. 2.2

This register holds the instruction being executed. All functions are decoded from this register. The value of the function register bits is described in section 3.

Arithmetic-Logic-Unit (ALU). 2.3

The 3500 is provided with a 16-bit ALU surrounded by two operand registers (OPA and OPB) and a CARRY flag.

For arithmetic operations, operands are treated as 16-bit unsigned numbers. The program, however, can interpret them as signed numbers in two's complement notation as described at the beginning of this chapter.

The CARRY flag is used to detect a carry out of bit 0 in an arithmetic operation. The CARRY flag may be set or reset by a number of instructions, just as there is a possibility for branching on the current value of CARRY.

Memory. 2.4

The memory is direct addressable, both byte-wise and word-wise. The minimum memory size is 4K 16-bit, expandable up to 32K 16-bit in modules of 4K.

The memory used is a MOS integrated memory with a cycle time of 925 nSec. (Core memory is optional). For autoload purpose part of the memory is substituted by a ROM memory (optional). This memory is addressable, but the contents cannot be altered electrically.

Memory restrictions:

- 32,624 to - 32,768: Autoload.

Note that even if the memory module 28K-32K is not present in the machine, the autoload is still active in the mentioned addresses.

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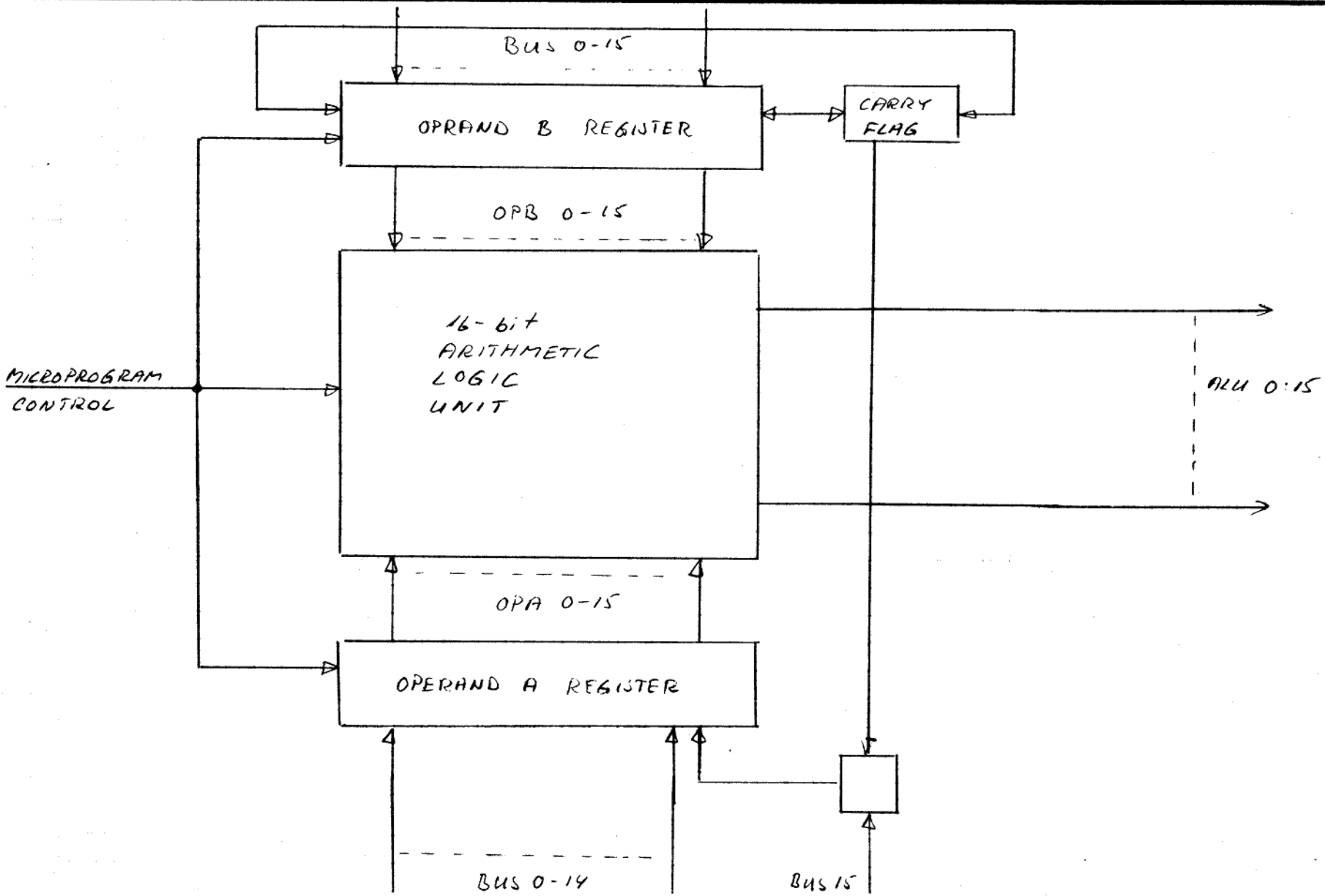
ARITHMETIC-LOGIC-UNIT

BLOCKSCHEME

Fig. 2.3.1



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The input/output system is modular expandable up to 32 input/output channels in modules of 8 channels.

The data transfer between CPU and peripherals is performed in serial mode, but the data are treated as serial and parallel data, depending on the characteristics of the peripheral in question. Peripherals having high transfer rates communicate in blocks of words or bytes direct with memory.

Any peripheral is connected to the CPU by means of a 4 pairs cable, which is transformer coupled at both ends to secure a very high noise immunity.

The transmission of data is performed in serial mode whether the device connected is of parallel or of serial natur. The data word transferred consists of a 4 bits header and 0 to 16 information bits.

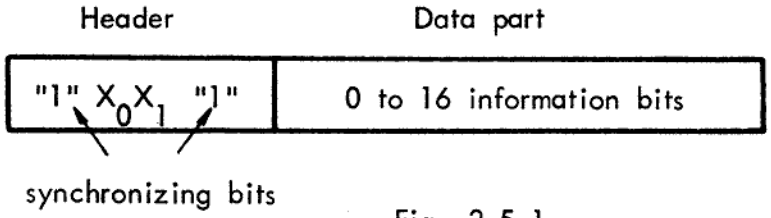


Fig. 2.5.1.

The header contains the following information:

TRANSMISSION FROM CPU TO PERIPHERAL

"OUTPUT HEADER"	1 0 0 1	Read data
	1 0 1 1	Read status
	1 1 0 1	Write data
	1 1 1 1	Write control

TRANSMISSION TO CPU FROM PERIPHERAL

"INPUT	1 0 0 1	16 bits (word)
HEADER"	1 0 1 1	EOI (End of Information)
	1 1 0 1	8 bits (byte)
	1 1 1 1	1 bit (bit)

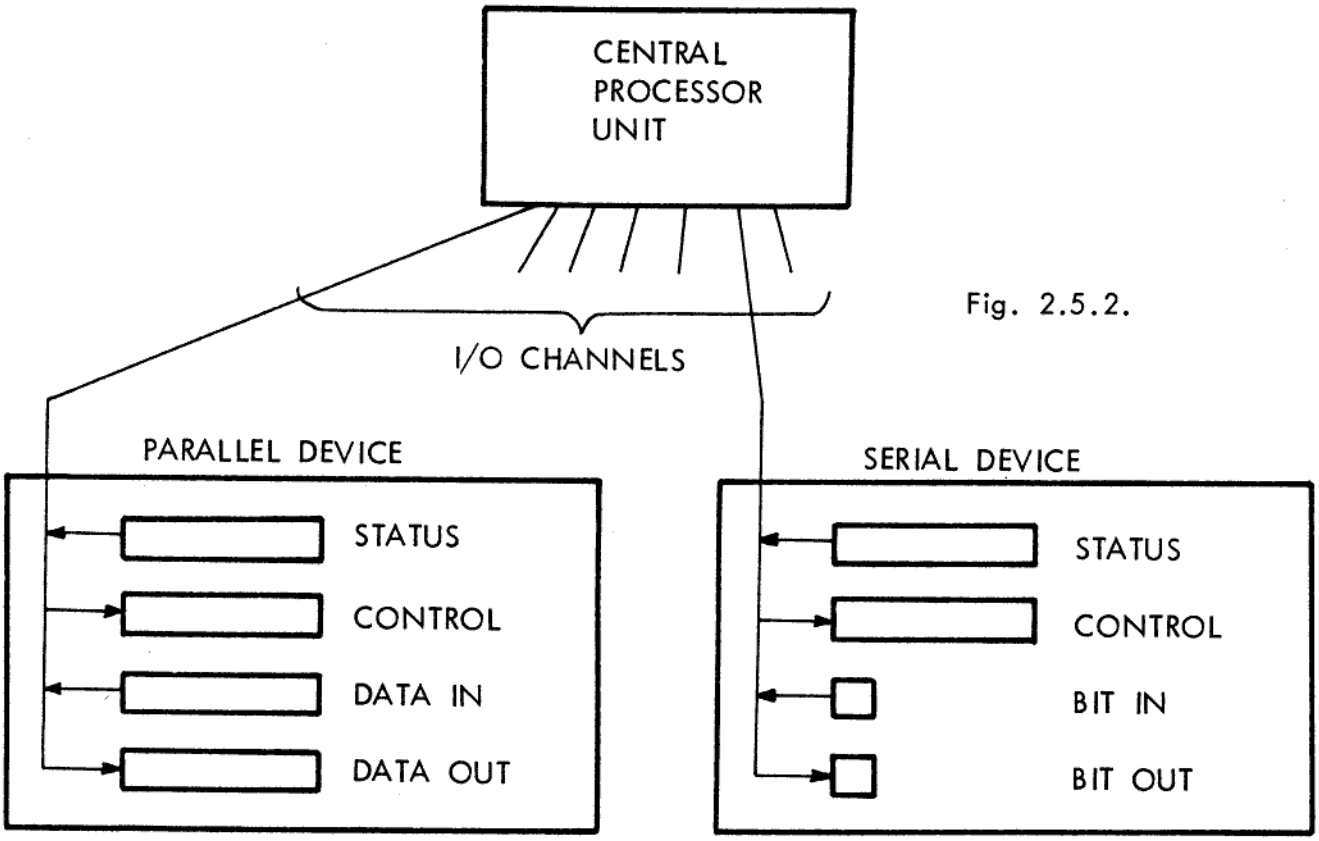
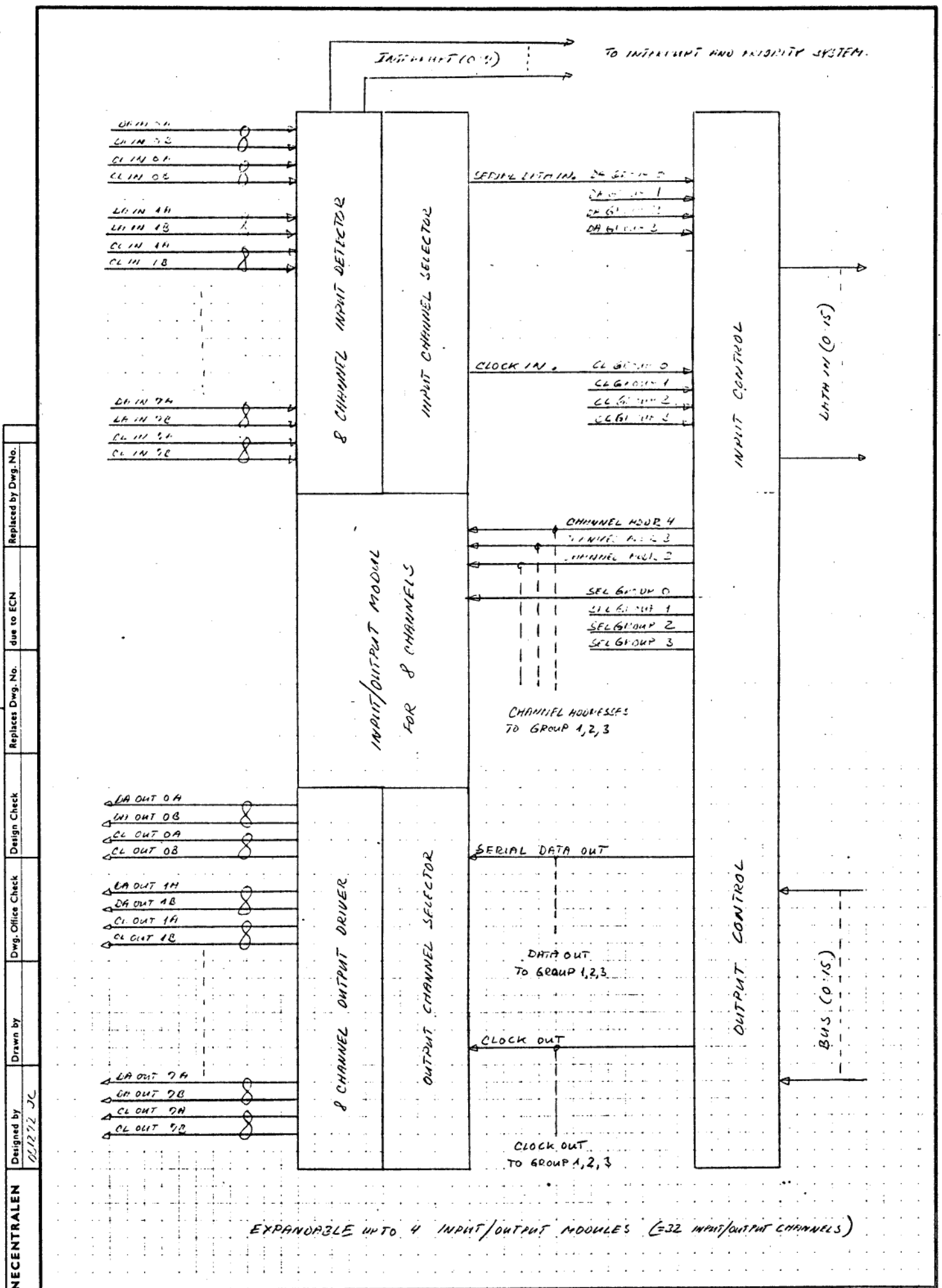


Fig. 2.5.2.

In principle each device contains 4 16-bit registers. The registers are 2 data registers (one for each direction of flow), one control register and one status register. However, for actual devices one or more of the registers may be omitted, some of the registers may be combined to one, or the register lengths may be shortened from 16 bits right down to 1 bit. The central processor initiates an I/O instruction by selecting the I/O cable leading to the device addressed, whereafter the data are transferred.

Communication may be initiated either by program or by interrupt from a device. An interrupt is detected on the data line, when a "1" bit is sent to the CPU, and it has not asked for data.



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Unit		Fig. 2.5.3
Dwg. No.	INPUT/OUTPUT SYSTEM FOR 3500	

RC doc. VB 140

A program interrupt feature permits an automatic switching from the current program sequence to another sequence in immediate response to specific external or internal events. The efficiency of an interruption system is direct related to the time it takes the central processor to perform this switching. Therefore, in the 3500, we have associated a set of working registers to each interruption level, so switching is reduced to connect a new set of working registers to the control and arithmetic unit; confer figure 2.6.1.

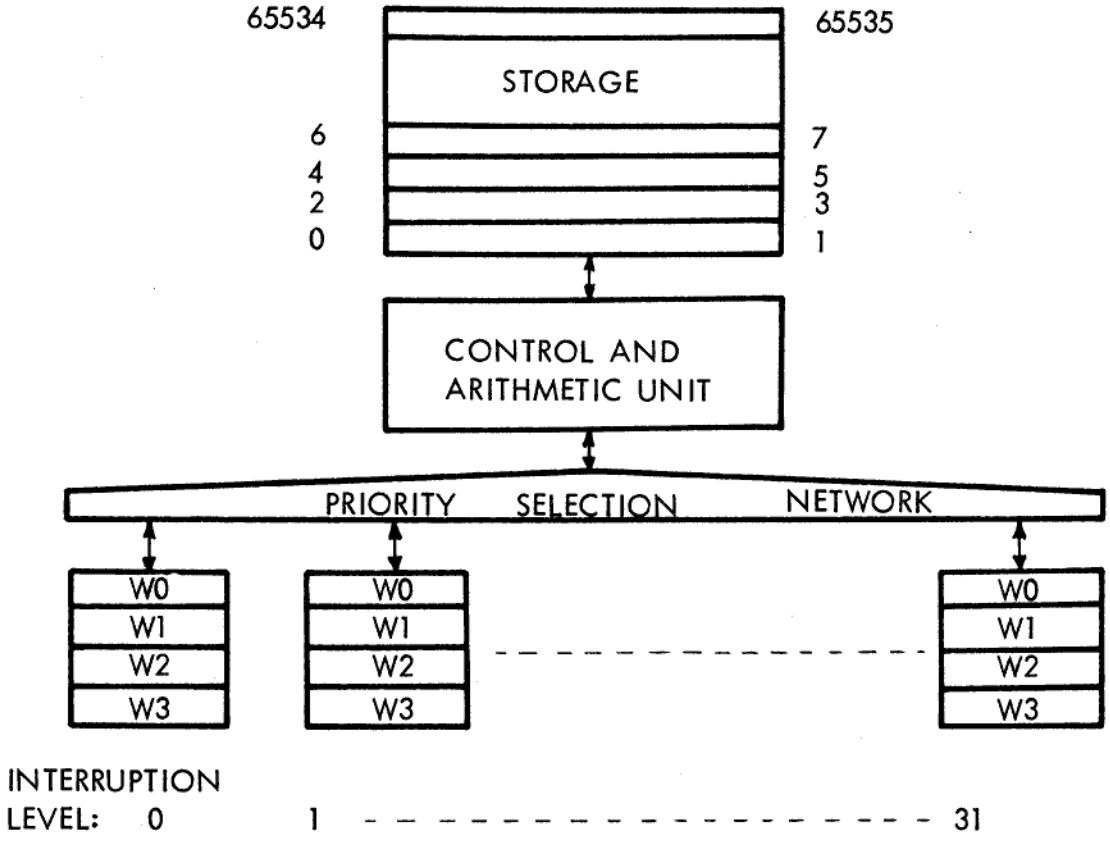

Figure 2.6.1. 3500 Block Diagram

The priority selection network contains a 32-bit interrupt request buffer, IR, of which bits 1 to 31 can collect up to 31 incoming interrupt signals. A one in a bit position corresponds to an interrupt request, and bit N corresponds to the Nth interruption level. Bit 0 in register IR occupies

an exceptional position, because the value of this bit remains one equivalent to a permanent interrupt request.

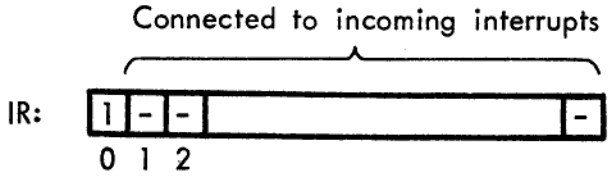

Figure 2.6.2. Interrupt Request Register

Simultaneous interrupt signals are served in order of priority, and the signal which is wired to the highest bit number in IR has highest priority. Input/output devices with a high transfer rate should therefore have their interrupt lines wired to the right most bits of register IR. If all incoming interrupt signals are honoured and no new requests arrive, interruption level 0 is automatically selected.

Microprogram. 2.7

The microprogram forms the CPU by controlling the BUS, the ALU, the conditions, and several DO-functions. It is physically contained in a Read-only-Memory of 144 words of 48 bit. The time per microstep is 313 nSec.

Each word of a microinstruction contains the following information:

bit	
0- 7	next microstep basis address
8-12	condition select for modification of the basis address
13-17	selects the source to be distributed to the BUS
18-23	selects the ALU function to be performed
24-47	DO-functions

RC doc VB 140

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Unit

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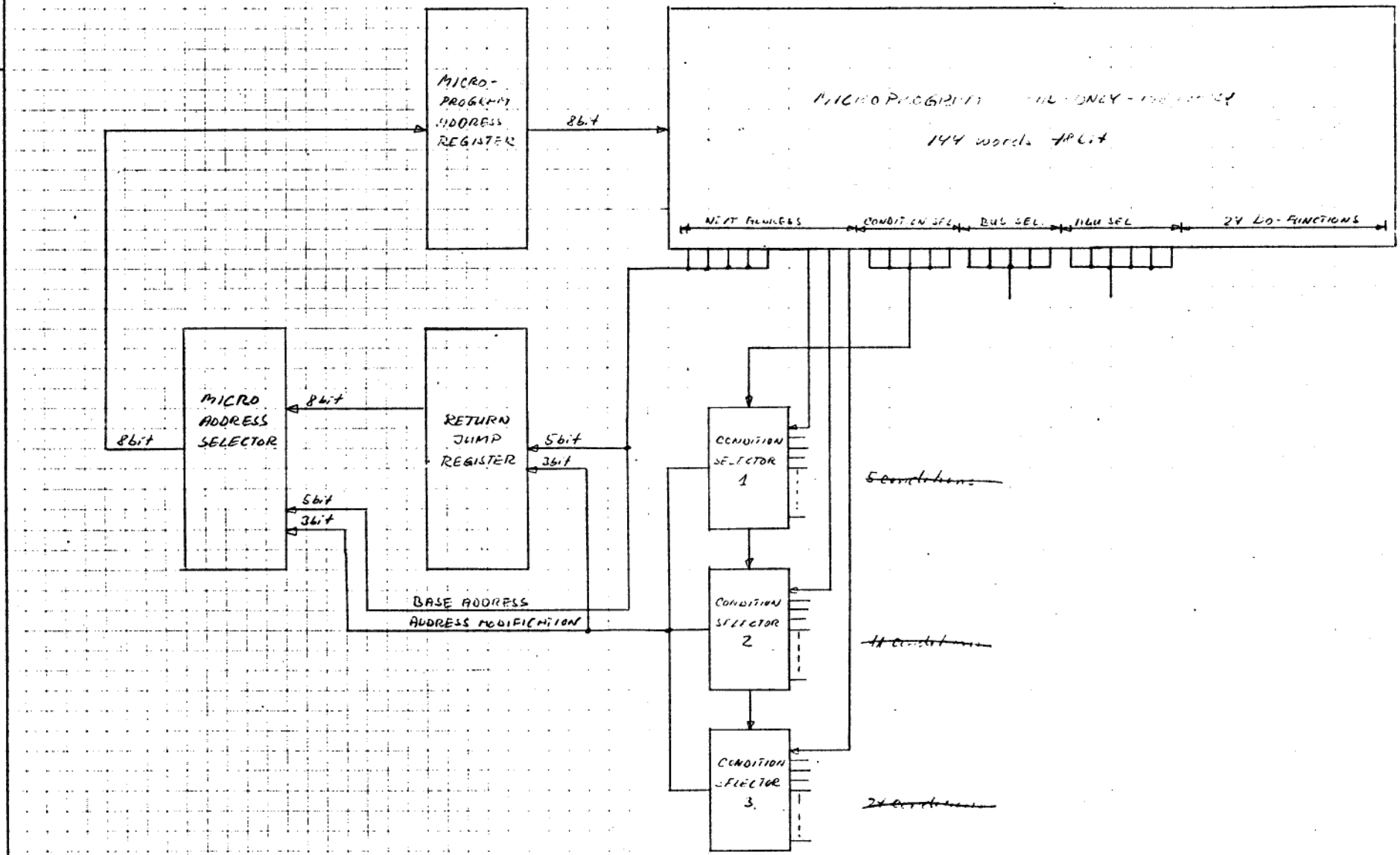
3500 MICROPROGRAM STRUCTURE

By 221



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The 3500 may be equipped with an automatic load program called a bootstrap. loader placed in a Read-only-Memory containing 144 words of 16 bit. The ROM is arranged as the last 144 words of the possible memory: addresses 32624 to 32768 incl.

The autoloading can be performed from devices as:

Paper tape reader
Asynchronous devices such as teletypes
Synchronous devices
Direct Memory Access channel

There are two different ways to start an autoload function:

a. Local Autoload can be performed when the operator has turned the switch lock to the ON position (not LOCK), so that the switches on the operator's panel are active.

   Before pressing the AUTO switch, the operator on the data switches must set up the device number wanted as input medium, its appropriate Interrupt Level, multiplexer address, and device type.

b. Remote Autoload (optional) can be performed, when the switch lock is left in the LOCK position. The necessary information about device number, interrupt level, and multiplexer address is now read from a switch panel physically placed in the BUS module. This information is alterable by technician intervention. The autoload function is now started, when an EXT. AUTOLOAD signal is activated.

When started the autoload program enters the ROM part of the memory according to the data switches (on the operator's panel or in the BUS module) and reads data from the input medium.

At the end of the read operations the program counter is switched to 0, and the normal program run is performed.

The 3500 can be equipped with a DMA option enabling the connection of very fast input/output devices. Max. transfer rate is 1.5 uSec. per word. 7 external devices may be connected to one DMA. A priority system enables the correct connection of low orders and high orders devices.

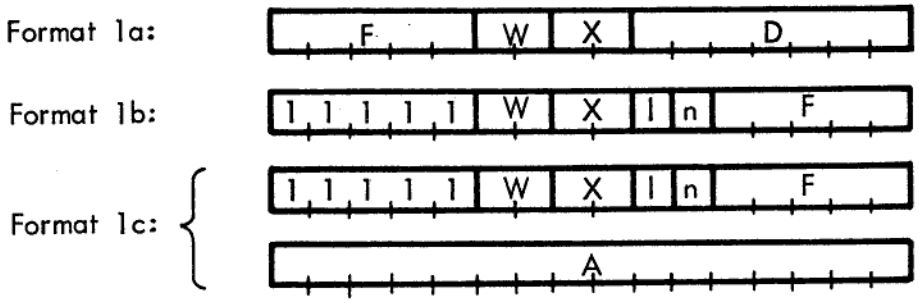
When installed the DMA holds part of the memory (4K to 32K) for its disposal, and it is to this part only the external access is performed on a cycle stealing basis.

This cut up in two of the memory enables undisturbed program run, when the program is placed in the CPU part of the memory, and maximum transfer rate on the DMA, if the data block is placed in the DMA part.

For detailed information about instructions see:

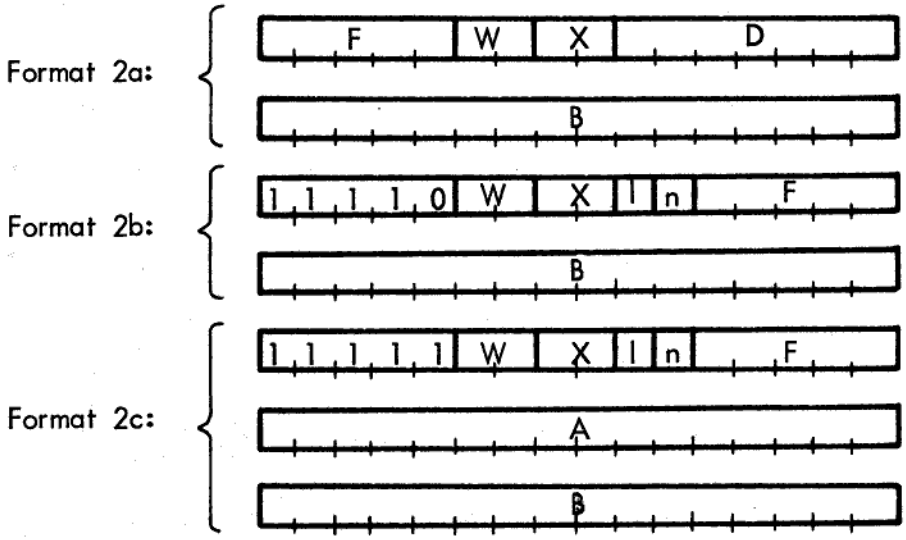
RC 3500 Reference Manual, RCSL: 52-AA316.

Arithmetic and Logical Instructions.



		F0	F1	F2	F3	F4
ldr	Load Register	0	0	0	0	0
ldc	Load Complement	0	0	0	0	1
ldi	Load Indirect	0	0	0	1	0
str	Store Register	0	0	0	1	1
sti	Store Indirect	0	0	1	0	0
xsr	Exchange Store and Register	0	0	1	0	1
ldb	Load Byte	0	0	1	1	0
stb	Store Byte	0	0	1	1	1
add	Add Integer Word	0	1	0	0	0
sub	Subtract Integer Word	0	1	0	0	1
and	Logical AND	0	1	0	1	0
lor	Logical OR	0	1	0	1	1
xor	Logical Exclusive OR	0	1	1	0	0
lce	Load Register Clear Interrupt and Enable	0	1	1	0	1
	Not used	0	1	1	1	0
rsw	Read Switches	0	1	1	1	1

Branch and Continue Instructions.

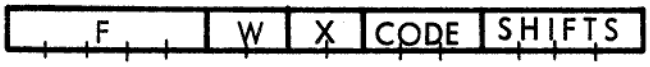


		F0	F1	F2	F3	F4
bgw	Branch if Greater	1	0	0	0	0
bew	Branch if Equal	1	0	0	0	1
blw	Branch if Less	1	0	0	1	0
bgb	Branch if Greater than Byte	1	0	0	1	1
beb	Branch if Equal to Byte	1	0	1	0	0
blb	Branch if Less than Byte	1	0	1	0	1
bsz	Branch if All Selected Bits are Zero	1	0	1	1	0
bop	Branch if Selected Bits have Odd Parity	1	0	1	1	1

Continue instructions as mentioned above, with the suffix "n" added to the mnemonic code.

Shift-Rotate Instructions.

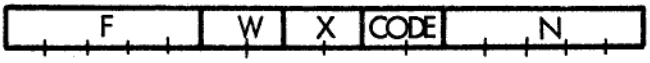
Format 3:



ror	Rotate Right	0	0	0	1	1	1	0	0
rol	Rotate Left	0	0	1	1	1	1	0	0
lsr	Logical Shift Right	0	1	0	1	1	1	0	0
lsl	Logical Shift Left	0	1	1	1	1	1	0	0
asr	Arithmetic Shift Right	1	1	0	1	1	1	0	0
	Undefined	1	0	0	1	1	1	0	0
	Undefined	1	0	1	1	1	1	0	0
	Undefined	1	1	1	1	1	1	0	0

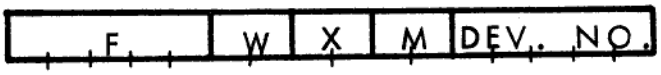
Interlevel Instructions.

Format 3:



ild	Interlevel Load	1	1	0	1	0
ist	Interlevel Store	1	1	0	1	1
	Not used	1	1	1	0	1
	Format b	1	1	1	1	0
	Format c	1	1	1	1	1

Format 3:



					F0	F1	F2	F3	F4
rsc	Read Status and Compare	0	1	(P or S)	1	1	0	0	0
wcc	Write Control and Clear	0	1	-	1	1	0	0	1
rwc	Read Word and Compare	0	0	(P)	1	1	0	0	0
rbb	Read Block of Bytes	1	0	-	1	1	0	0	0
rbw	Read Block of Words	1	1	-	1	1	0	0	0
wwc	Write Word and Compare	0	0	-	1	1	0	0	1
wbb	Write Block of Bytes	1	0	-	1	1	0	0	1
wbw	Write Block of Words	1	1	-	1	1	0	0	1
rbc	Read Bit and Compare	0	0	(S)	1	1	0	0	0
rbb	Read Block of Bits	1	0	-	1	1	0	0	0
wbc	Write Bit and Compare	0	0	-	1	1	0	0	1
wbb	Write Block of Bits	1	0	-	1	1	0	0	1
	Undefined	1	1	-	1	1	0	0	0
	Undefined	1	1	-	1	1	0	0	1

P = Parallel Device

S = Serial Device

Address Calculation Times (AT).

This scheme describes the execution times (AT) for the address calculation dependent of the format and the index register selected, and if immediate addressing is selected.

These times must be added to the times listed below for the instructions to get the total executing time of an instruction.

Instruction executing time: T = AT + ET.

Ex.: ldr W3 X0 (format 1a) T = 3,2 + 1,0 = 4,2 uSec.

rwc W3 X2 D27 (format 3); number of bits n = 8, bit time t = 0,2 uSec.

AT = 2,9 uSec.

ET = 4,5 uSec. + (2t + 4t + nt) uSec. =

4,5 uSec. + 2 x 0,2 + 4 x 0,2 + 8 x 0,2 uSec. = 7,3 uSec.

T = AT + ET = 2,9 + 7,3 uSec. = 10,2 uSec.

AT		FORMAT 1 & 2			FORMAT 3	
		a	b	c		
I = 0	X = X0		5,4	7,0		uSec.
	X<>X0	5,7	5,7	7,3		uSec.
I = 1	X = X0	3,2	3,8	5,4		uSec.
	X<>X0		4,2	5,7		uSec.
FORMAT 3					2,9	uSec.

Execution Times (ET).

This scheme describes the times which must be added to the ADDRESS CALCULATION TIMES (AT) to get the exact execution time for an instruction.

FORMAT 1 & 2

ldr	1,0	uSec.	
ldc	1,9	-	
ldi	2,5	-	
str	1,3	-	
sti	1,3	-	
xsr	1,6	-	(for I = 1 & X <> 0 add 0,3 uSec.)
ldb	1,3	-	
stb	1,3	-	
add	1,6	-	
sub	1,6	-	
and	1,0	-	
lor	1,0	-	
xor	1,0	-	
lce	1,0	-	
rsw	1,0	-	

If count is specified, 0,3 uSec. must be added for byte operations and 0,6 uSec. for word operations.

bgw	1,6	uSec.	For branch and continue instructions
bew	1,6	-	the same timing is valid; if the
blw	1,6	-	instruction, however, branches, 1,6
bgb	2,2	-	uSec. must be added.
beb	2,2	-	
blb	2,2	-	
bsz	1,6	-	
bop	1,6	-	

bgw (N)	3,2 uSec.	
bew -	3,2 -	
blw -	3,2 -	

FORMAT 3

ror	1,9 uSec.	
rol	1,9 -	
lsr	1,9 -	
lsl	1,9 -	
asr	1,9 -	
ild	0,6 uSec.	
ist	0,6 -	
rsc (P+S)	4,5 uSec.	NOTE
wcc -	1,6 -	
rwc (P)	4,5 -	NOTE
rbb -	4,8 -	NOTE
rbw -	4,8 -	NOTE
wwc -	2,5 -	
wbb -	3,5 -	
wbw -	3,8 -	
rbc (S)	4,5 -	NOTE
rbb -	4,5 -	NOTE
wbc -	3,2 -	
wbb -	3,5 -	

Add 0,6 uSec. per shift

If w equals x or EOI is received, subtract 0,3 uSec.

P = Parallel Device

S = Serial Device

NOTE: add (2t + 4t + nt) uSec., where t is the bit length (in uSec.) of the selected device, and n is the number of bits transferred.

All operations are performed from the operator's panel which is illustrated in figure 4.1.1.

The operator's panel can be parted in 3 functional units, the register part, the status part, and the operating part.

The register part in the centre of the panel consists of two parts: 3 rows of lights and a register of switches.

Mentioned from top to bottom there are the following displays:

FUNCTION	indicates the instruction in progress
ADDRESS	indicates the current memory address
BUS	indicates the last information transferred via the BUS

Below the BUS indicators there is a register of data switches, through which the operator can supply addresses and data to the processor (the up position of a switch represents a 1). The switch register is used in conjunction with the operating switches, and its contents may be read by program by the READ SWITCHES instruction.

The status part contains information about:

RUN	the processor is in normal operation; when the light turns off, the processor is stopped.
DISABLE	indicates that a number of instructions is executed without interference of external interrupts; when turned off, the processor is in enable mode.

PRIORITY LEVEL ADDRESS	The display indicates the interrupt level being serviced; below the indication a set of 5 switches enables the operator to look-up and/or alter any desired interrupt level by means of EX W or DEP W.
W-REG. ADDRESS	The display indicates which working register of the current interrupt level being serviced. The switches below enable the operator to select any of the 4 working registers in the interrupt level selected by Priority Level Address Switches.

The operating part contains the operating switches and a 3-position key-operated rotary switch. The latter controls power and locks the panel. The 3 key-positions:

OFF	power is turned off.
LOCK	power is turned on, but all the panel functions are disabled. Also the data switches are disabled, and the information to the program is supplied from a set of data switches placed in the BUS module.
ON	power is on, and all panel functions are enabled. The data switches in the BUS module are disabled.

Operating switches are 3-position switches with common off position in the centre. Functions are listed below:

RUN	begin normal operation and disable the other operating switches except STOP.
STOP	the processor stops when the current instruction is finished. The FUNCTION light shows the instruction

just finished. The PRIORITY LEVEL ADDRESS lights indicates the next interrupt level to be executed. All other operating switches are enabled.

EX — loads the contents of the data switches into the memory address register (displayed on ADDRESS lights) and displays the contents of the addressed memory location on the BUS lights.

EX NEXT — adds 2 to the memory address specified by the ADDRESS lights and displays the contents of the new memory location on the BUS lights.

DEP — deposits the contents of the data switches in the memory location specified by the ADDRESS lights. The BUS lights display the word deposited.

DEP NEXT — adds 2 to the memory address specified by the ADDRESS lights and deposits the contents of the data switches in the new memory location. The BUS lights display the word deposited.

EX W — examines the contents of the working register specified by the PRIORITY LEVEL ADDRESS switches and the W-REG ADDRESS switches. The contents are displayed on the BUS lights.

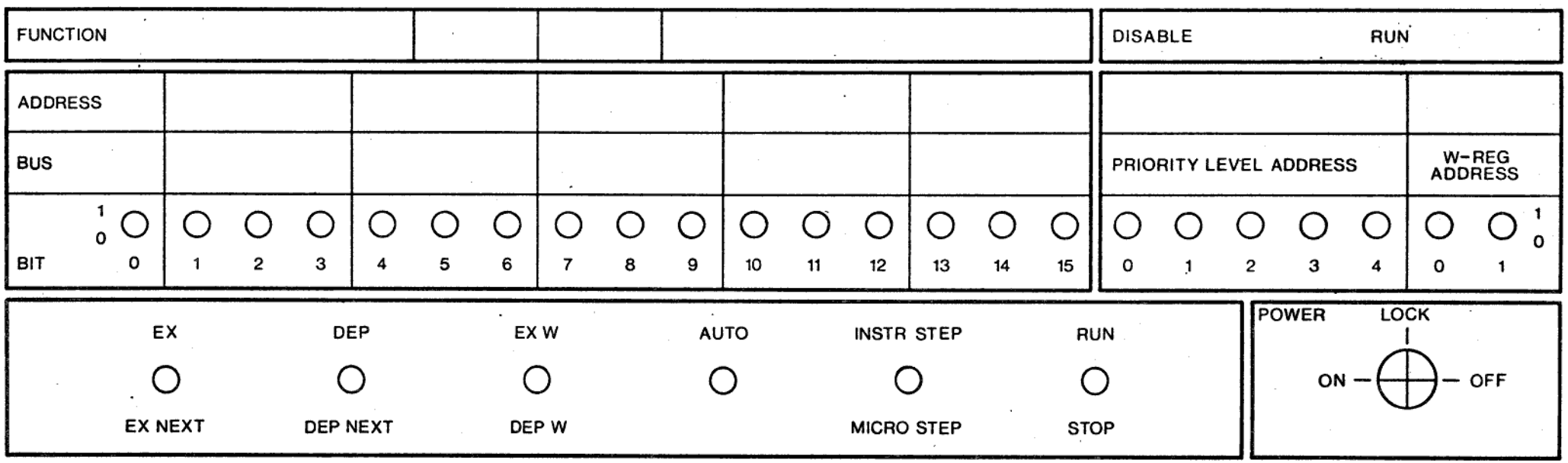
DEP W — deposits the contents of the data switches in the working register specified by the PRIORITY LEVEL ADDRESS switches and the W-REG ADDRESS switches. The BUS lights display the word deposited.

AUTO — when pressed, the program reads the contents of the data switches and uses it for definitions of input

medium. Interrupt level 31 is set with instruction counter set to 32768, and the processor is started (optional).

INSTR STEP — one single instruction is executed.

MICRO STEP — one single micro instruction is executed and the lights display the results of the micro instruction.



3500 OPERATORS PANEL

RC 3500
A 11483

FORPLADETEGNING.

4.1.1

ROUTINE MAINTENANCE 5

Cleaning of Front Panel. 5.1

When necessary, clean the front panel with a soft cloth dipped in lukewarm water.

Cleaning of Air Filter. 5.2

The air filter front cover is removed and the filter pulled out every month. The filter is vacuum-cleaned or washed in lukewarm water.

Every six months or less the filter must be exchanged.

Check of DC Voltage Levels. 5.3

Whenever convenient, but at least once every 3 months, do check the DC voltage levels.

The measurement is performed by using the test-bushings situated on the motherboard. The access is made from the rear of the machine.

The adjustment is performed on the individual power supply units by loosening the operator's panel and then pull forward the whole power supply system.

Transfer of I/O-information is accomplished by two-way serial transmission over four twisted pairs, two pairs in either direction. Those four pairs are physically localized in the same I/O-cable. In both directions are carried clock signals in one pair and data signals in the other.

Transmission rate is nominally 5 MHz.

Maximal transmission length is 100 m.

Output from 3500 to Peripheral. 6.1

The output message from the computer always consists of 20 bits, 4 header bits and 16 information bits.

The four header bits must be decoded by the interface and proper action taken. The interpretation of the header is as follows:

"1"	X_0	X_1	"1"	
1	0	0	1	Read Data
1	0	1	1	Read Status
1	1	0	1	Write Data
1	1	1	1	Write Control

The header is appearing at the interface as read from left to right (i.e. X_0 before X_1).

As far as the read instructions are concerned, input to RC 3500 from peripheral may be initiated after receipt of the header information, but must be completed at least 10 uSec. after completion of the output message.

For further explanation of the I/O-instructions refer to 3500 Reference Manual.

Input to 3500 from Peripheral. 6.2

The input message to the computer consists of the header and subsequent bits, the number of which is indicated by means of the input header. The interpretation of the header is as follows:

"1"	X_0	X_1	"1"	
1	0	0	1	16 bits (word)
1	0	1	1	EOI (End of Information)
1	1	0	1	8 bits (byte)
1	1	1	1	1 bit (bit)

It is defined that EOI is sent to the computer to indicate that the accompanying information has no meaning.

Clock signals to send an input message must be supplied from the interface. Nominal frequency is 5 MHz. Deviations from this frequency must never exceed $\pm$ 1 MHz.

Interrupt to the 3500. 6.3

An interrupt is a request-for-service-signal sent via the data in line to the computer. The interrupt pulse is sent to the CPU, whenever the peripheral wants to communicate.

To ensure that none of the interrupts are neglected by the CPU, some time-dependent conditions must be fulfilled.

Internal to the interface an inhibition must be generated, preventing interrupt to be transmitted to the CPU, when the particular interface is selected. This means that the interrupt inhibit period is defined as the period, where the CPU is transmitting clock-pulses. Further, during READ instructions 3.0 uSec. must be added, after transmission of the input message to the CPU is completed.

Receiver Specifications. 6.4

Signals are received on a balanced twisted pair and must be referenced to zero volt at the interface through a special pulse transformer (DALE PT 16-13, or equivalent).

Clock and data are in-phase signals.

Cable impedance: app. 100 Ohms.

Voltage swing: 400 mV < Vin < 3,0 V depending on attenuation of the cable.

Wave form of the communication:

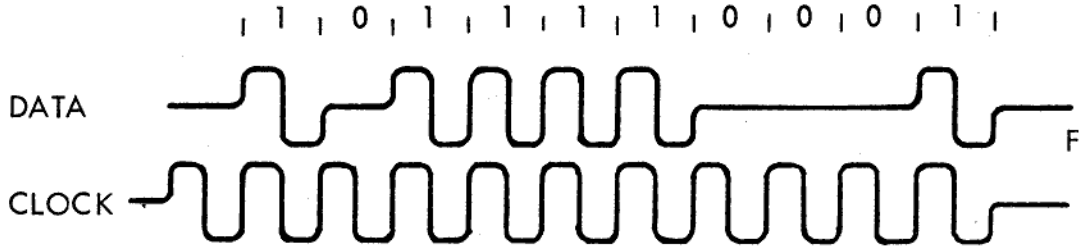


Fig. 6.4.1

Recommended receiver circuit: See fig. 6.5.1.

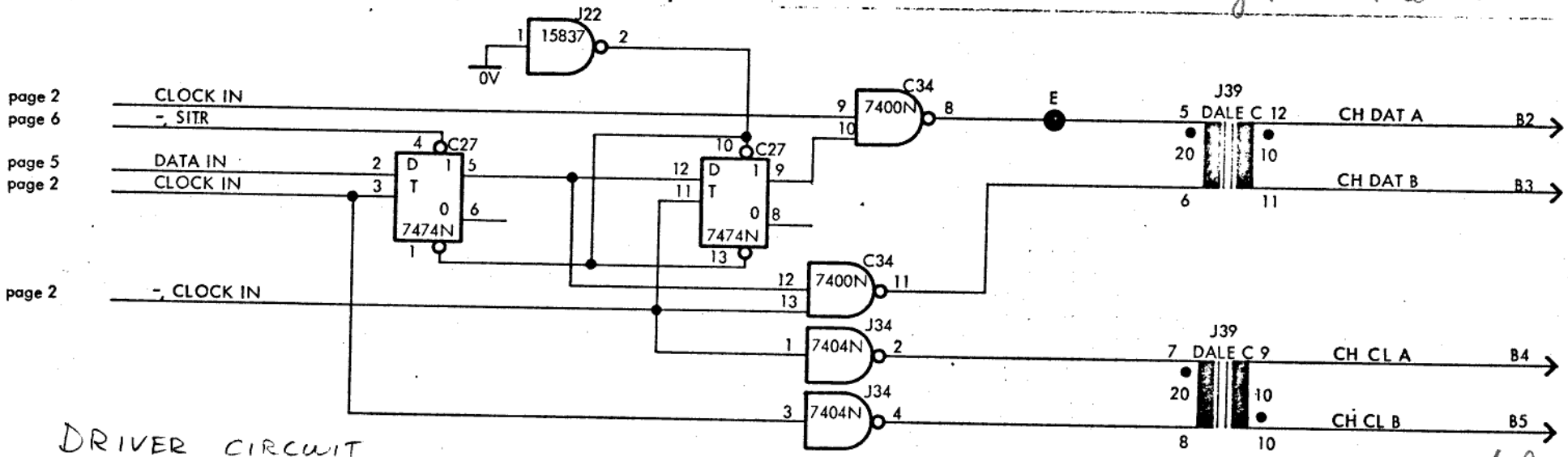
Driver Specifications. 6.5

Signal must be transmitted in balanced mode. This is established through the special interface pulse transformer (DALE PT 16-13, or equivalent), and driving the transformer like the recommended driver circuit provides sufficient drive for a maximum cable length of 100 m.

Recommended driver circuit: See fig. 6.5.1.

100372 KNEH 180372 ELBH 190772 JN

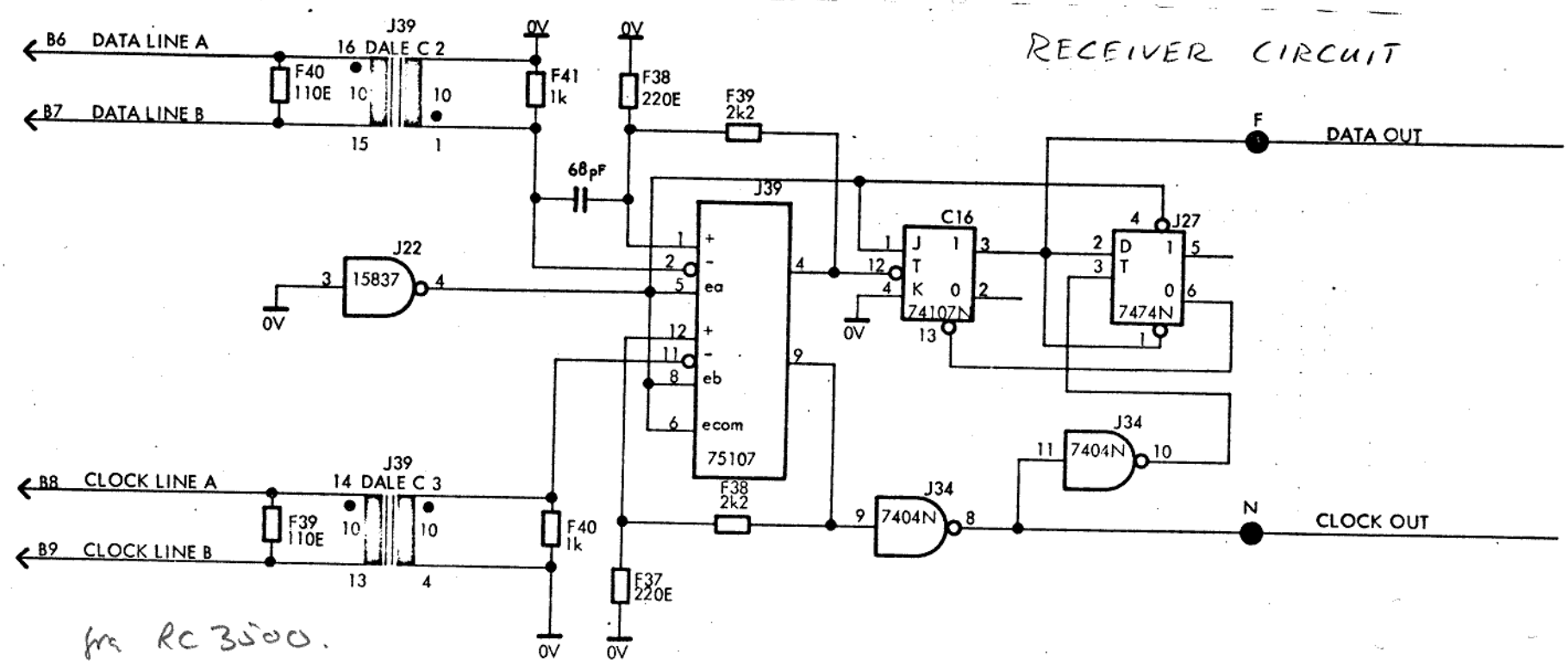
Rev for enhed.



DRIVER CIRCUIT

→ mod RC 3500

RECEIVER CIRCUIT



fra RC 3500.

All interfaces mentioned must be externally power supplied and housed.

Where no remarks are made, each interface is connected to one input/output channel in 3500.

Cabinets and power supplies for the interfaces can be supplied.

Available interfaces for:

RC 500, RC 2500	paper tape readers
Facit 4070	paper tape punch
Centronic 101	printer
Digitronic 200	printer
Calcomp	plotter
Hewlett Packard	card reader
Analogic	A/D converter
Rikke	minicomputer
3500	general purpose controller
810	alpha numeric display
811	display system

Asynchronous data-transmission (8 or 16 channel multiplexers, 75-1200 bps.)

Synchronous data-transmission (2400-48000 bps.)

Any other interface available on request.

Mains supply:

220V AC $\pm$ 10%, 50-60 Hz., single phase with ground.

Consumption:

600 VA.

Temperature range:

10°-40° Celsius.

Relative humidity:

Max. 90% non-condensating.

Size:

Height: 45 cm, width: 42 cm, depth: 60 cm.

Weight:

Approx. 50 kg.

Size of 19" rack:

Height: 180 cm, width: 58 cm, depth: 73 cm.

Weight: approx. 50 kg.

The 3500 General Purpose Controller is a stand-alone unit, which may be placed on a table or mounted in a standard 19" rack.

It is recommended that the ambient temperature at the installation be maintained between 20° and 30° C., but the temperature may vary from 10° to 40° without adverse effect. The equipment may be stored in temperatures between 0° to 70° C. The relative humidity may be as high as 90% non-condensating.

The 3500 is supplied with a 5 m long power cable, which has a Danish standard 3-wire plug. The 3500 should be connected to a power source capable of supplying 10 amperes.