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Technical Manual

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Abstract:

This manual contains a technical description of the RC702 and RC703 Microcomputers.

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PREFACE

First edition: RCSL No 44-RT2056

This manual replaces the manuals RCSL No 44-RT1974 and RCSL No 44-RT2030.

Mogens V. Pedersen
A/S REGNECENTRALEN af 1979, February 1983

1. INTRODUCTION

This manual gives a technical description of the RC702/RC703 Microcomputers.

The RC702/RC703 are self-contained computer systems - together with keyboard, video monitor and flexible disc they make up an operational system. Basic system configuration is briefly introduced in subsection 1.1.

The microcomputers themselves contain the following parts (a more specific explanation is given in subsection 1.2):

Part	Functional description and diagrams in
Microcomputer Board & Character Generator	Chapter 2.
Cabinet (with cables, transformer and rectifier unit) & Power supply	Chapter 3.

To the extent suitable, all diagrams and figures are contained on the right-hand pages and the matching text on the corresponding left-hand pages.

1.1 System Configuration

1.1

Basic system configuration follows the pattern shown:

		RC702			RC703		
		-1	-2	-3	-1	-2	-3
Keyboard	RC721	+	+	+	N/A	N/A	N/A
	RC722,001	+	+	+	N/A	N/A	N/A
	RC722,008	N/A	N/A	N/A	+	+	+
Monitor	RC752	+	+	+	+	+	+
Flexible	RC761-1	N/A	i	i	N/A	N/A	N/A
Disc	RC761-2	N/A	+	i	N/A	N/A	N/A
Drive	*RC762-1	m	N/A	N/A	m	N/A	N/A
	*RC762-2	+	N/A	N/A	+	N/A	N/A
	*RC764	m	N/A	N/A	m	N/A	N/A
	RC765-1	N/A	N/A	N/A	N/A	i	i
	RC765-2	N/A	N/A	N/A	N/A	+	i

+ = available
N/A = not available
m = mandatory
i = inclusive

MIC702/703

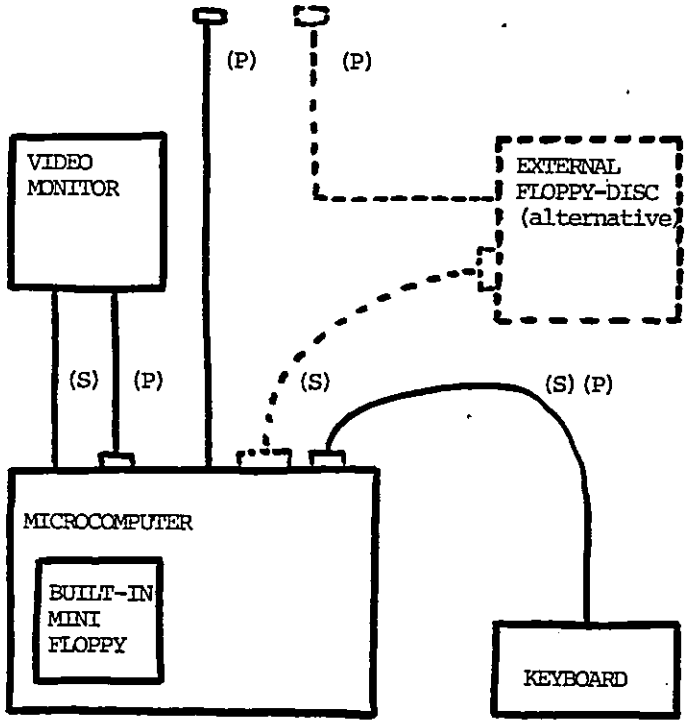
MIC704/705

FCO 19-008

*) RC762 and RC764 mutually exclude one another.

Technical manuals are issued seperately for each of the item groups above as well as for other optional equipment.

Fig. 1 shows an example of how to connect the units.



(S) = Signal cable
(P) = Power cable

Figure 1: Configuration; connections; example.

1.2 Microcomputer Construction 1.2

The construction of the microcomputers is based on the following components:

MICxxx - Microcomputer Board.
ROXxxx - Firmware Module (Character Generator, etc.).
KBNxxx - Cabinet Module (Cables, Transformer, etc.).
POWxxx - Power Supply.

The relationship between RC702/RC703 and specific modules is as follows:

RC7xx	MICxxx	KBNxxx	POWxxx	Note:
RC702 (48 KB RAM)	MIC702	KBN702	POW739	1)
RC702 (64 KB RAM)	MIC703	KBN702	POW739	1)
RC702 (64 KB RAM)	MIC704	KBN702	POW739	2)
RC703 (64 KB RAM)	MIC705	KBN705	POW746	2)

1) FCO 19-008 *) may be used
2) FCO 19-008 *) implemented on the board

*) The FCO (Field Change Order) concerns the installation of a data separator - further information is found throughout the subsections 2.3.12 and 2.4.2.

The relationship between MIC7xx and ROXxxx is as follows:

MICxxx	PROM SEL (pos.55)	AUTO LOAD (pos.66)	PROM 1 (pos.65)	CHAR GEN (pos.81)	SEMI CHAR GEN (pos.82)
MIC702	ROA320	ROA375	-	ROA296	ROA327
MIC703	ROA320	ROA375	-	ROA296	ROA327
MIC704	ROB268	ROB237	-	ROA296	ROA327
MIC705	ROB268	ROB357	ROB388	ROA296	ROA327

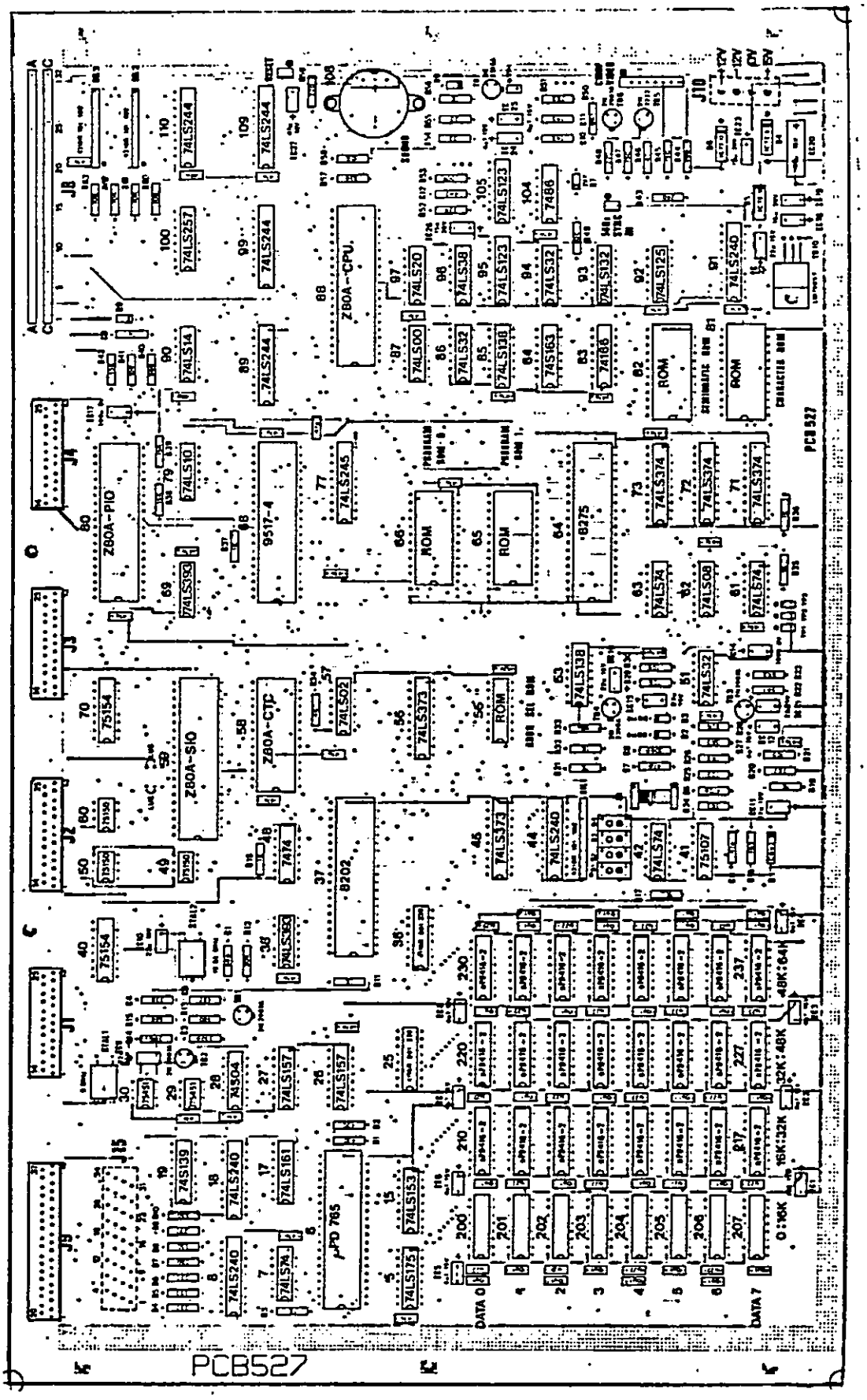


Figure 2: MIC702 - Microcomputer Board; layout.

2. MICROCOMPUTER AND CHARACTER GENERATOR 2.

2.1 General Description 2.1

The microcomputer board is built on a single circuit board. Power is supplied via a 4 pin connector, and the following supply is required:

+5 V typical 2.5 Amp.
+12 V typical 0.1 Amp.
-12 V typical 0.1 Amp.

The board layout is shown in fig. 2 which also shows the input/output connections.

2.2 Block Diagram 2.2

Fig. 3 shows a block diagram of MIC70x (the same diagram applies to all microcomputer boards). In the diagram is shown where each block is found in the circuit diagrams.

2.3 Functional Description 2.3

The functional description follows the block diagram. This paper does not contain a full description of all the functions of the VLSI circuits used. This kind of informations may be supplied by the manufactures of the VLSI circuits.

The description is almost the same for the different boards. If there are differences, they are mentioned - if not, the boards are referred to as MIC70x.

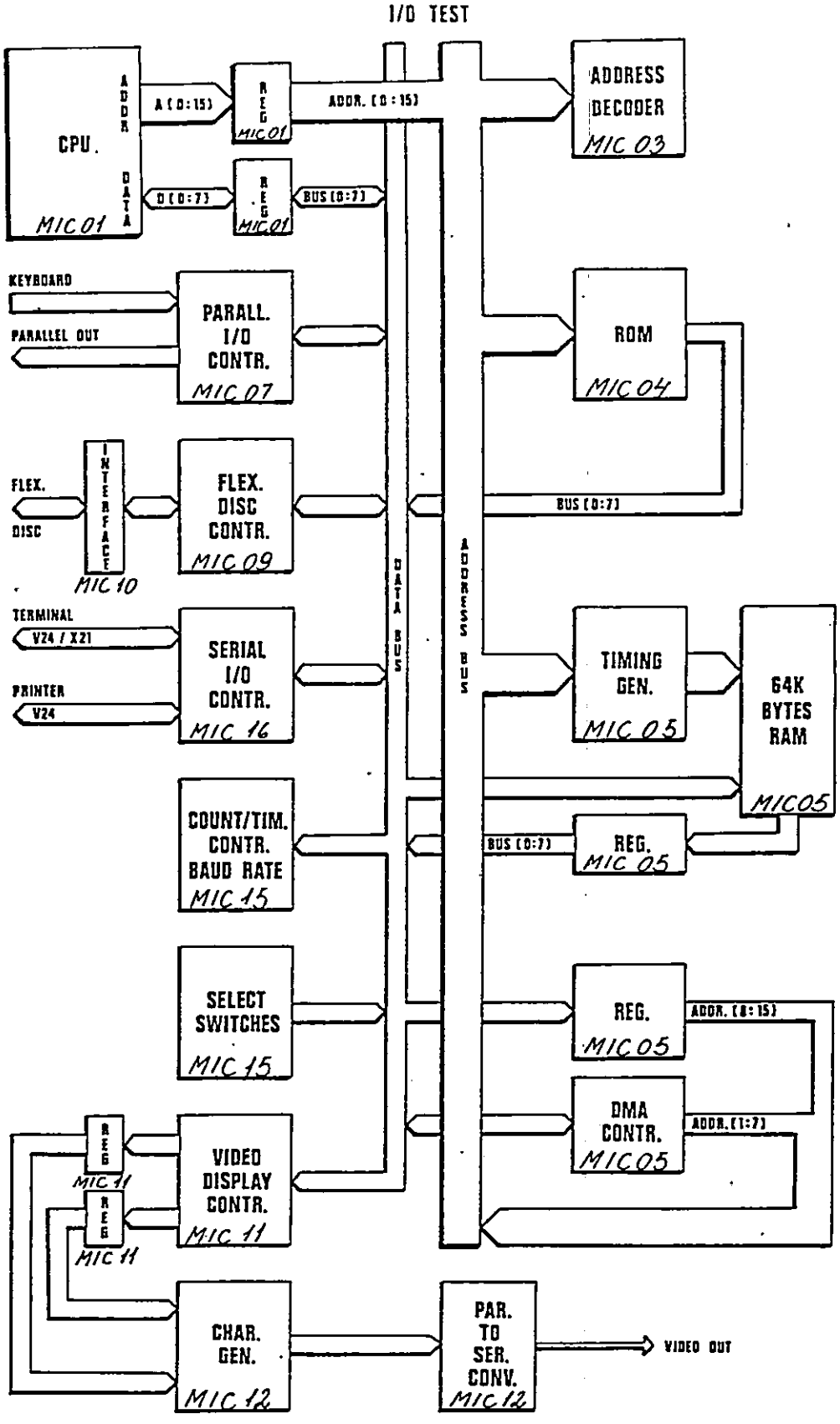


Figure 3: MIC70x; block diagram.

2.3.1 CPU Description

2.3.1

A block diagram of the architecture of the Z-80A CPU is shown in fig. 4. The diagram shows all the major elements in the CPU and it should be referred to throughout the following description.

Z-80A CPU contains 208 bits of R/W memory that are accessible to the programmers. Fig. 5 illustrates how this memory is configurated into eighteen 8-bit registers and four 16-bit registers.

All Z-80A registers are implemented using static RAM. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or in pairs as 16-bit registers. There are also two sets of accumulators and flag registers.

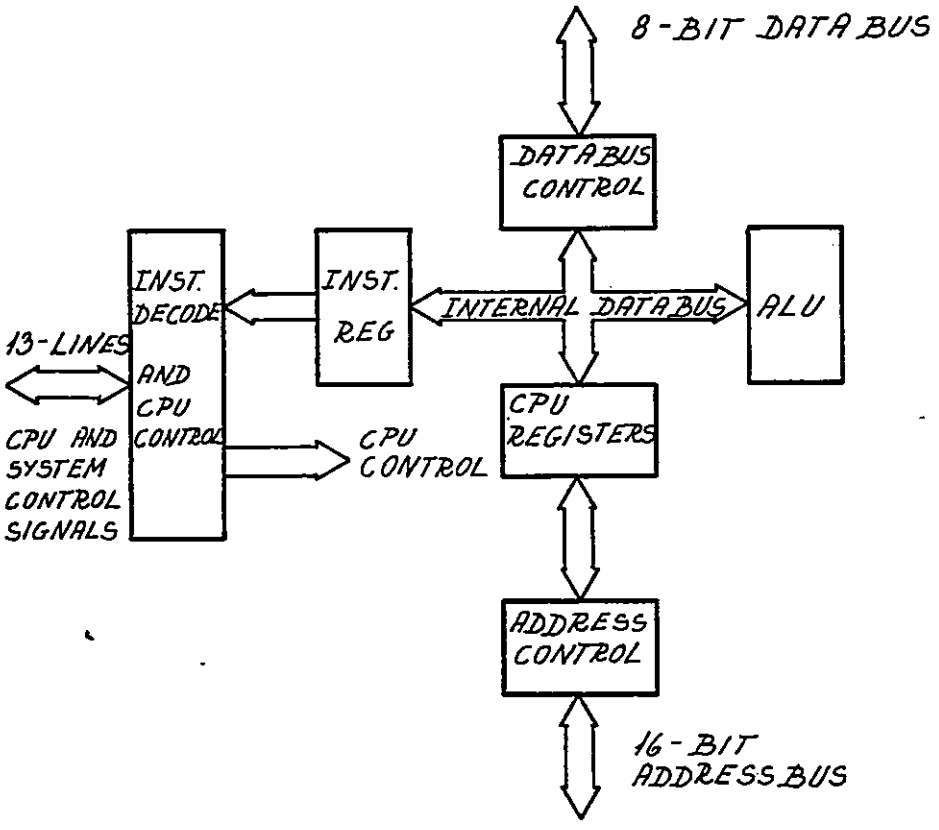


Figure 4: Z80A-CPU; block diagram.

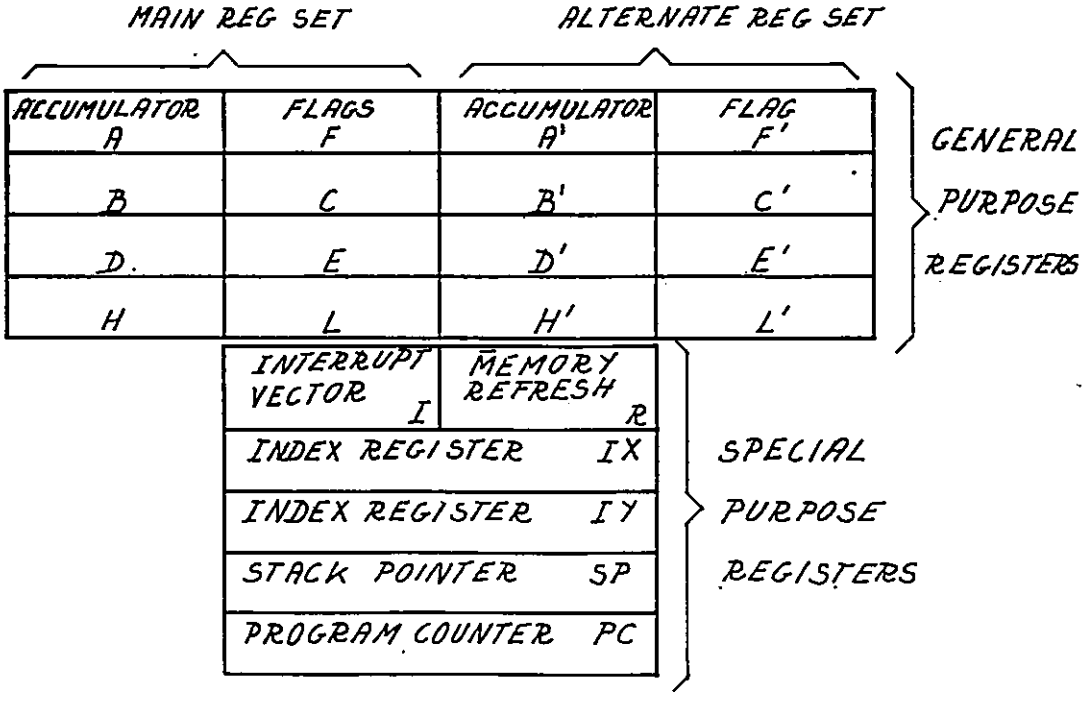


Figure 5: Z-80A-CPU; registers.

CPU timing can be broken down into a few very simple timing diagrams. The diagrams show basic operations with one wait state (the wait state is added to synchronize the CPU to the RAM memory). Figs. 6 to 8 show the CPU timing.

The Z80A CPU can execute 158 different instruction types including all 78 of the 8080A CPU. A description of this may be obtained from Zilog Z80A CPU Technical Manual.

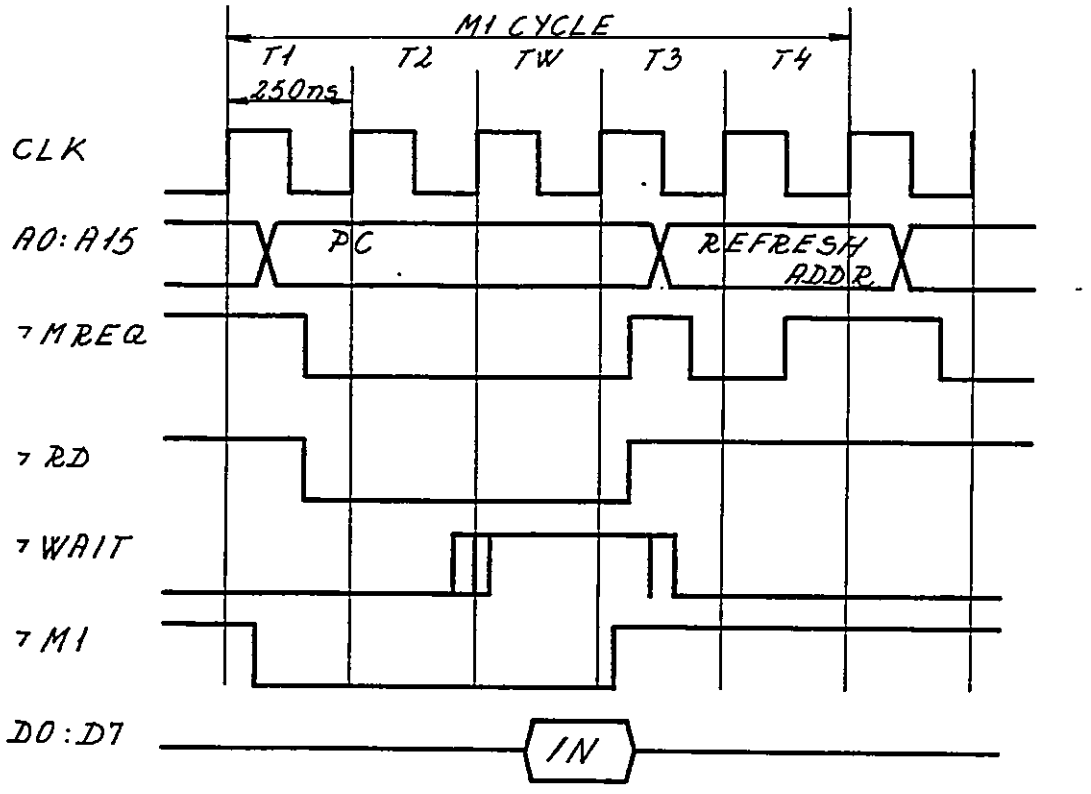


Figure 6: Instruction OP Code Fetch.

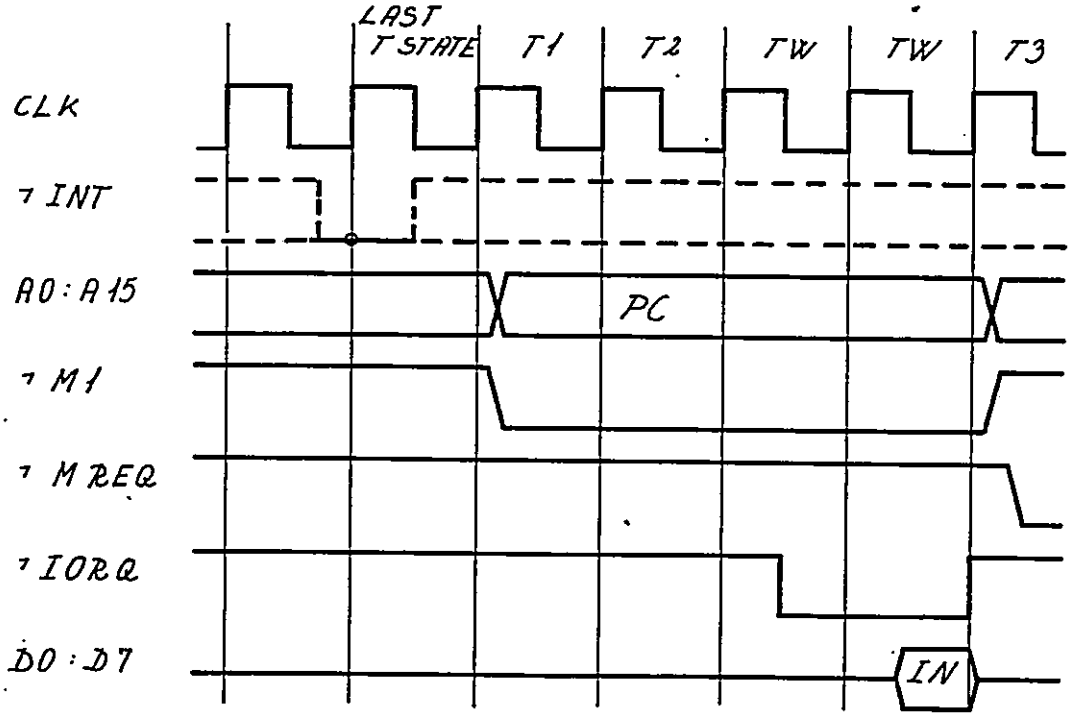


Figure 7: Interrupt Request/Acknowledge.

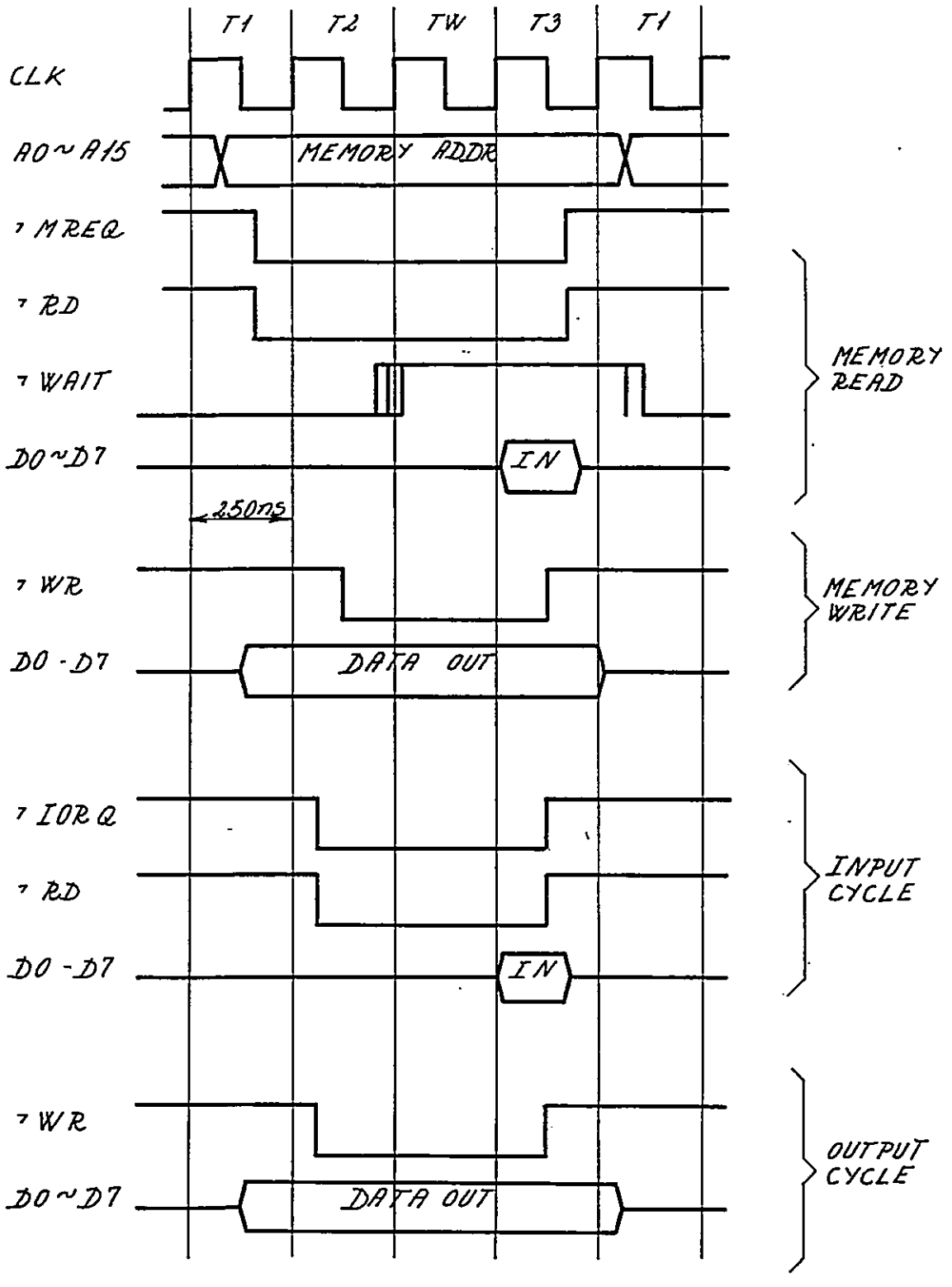


Figure 8: Z80A-CPU; timing waveform diagram.

2.3.2 Address Decoder

The addressing of devices is made very simple with the circuit shown in diagram page MIC03. Each device uses 4 addresses except the DMA controller which uses 16 addresses. This is shown in fig. 9.

Addr. No	Name	IC type	Comments
00	DISP	I8275	Parameter port
01	-		Command port
02	-		
03	-		
04	FLOP	µPD 765	Main status reg
05	-		Data reg
06	-	or I8272	
07			
08	SIO	Z80A-SIO2	Data channel A
09	-		Data channel B
0A	-		Control channel A
0B	-		Control channel B
0C	CTC	Z80A-CTC	Channel 0 to SIOA
0D	-		Channel 1 to SIOB
0E	-		Channel 2 int disp
0F	-		Channel 3 int flop
10	PIO	Z80A-PIO	Data keyboard
11	-		Data parallel I/O
12	-		Control keyboard
13	-		Control parallel I/O
14	SWITCH		Input: 8 bit from switch
15	-		Output: bit 0 controls
16	-		Motor enable, bit 1
17	-		Controls MAXI select
18	Enable PROM 0.1		In MIC702 and MIC703 all four
19	Disable PROM 0.1		Instructions disables PROM 0.1
1A	Enable PROM 1		(both PROM's);
1B	Disable PROM 0.1		(See also fig. 10).
1C	Enable sound		In MIC702 and MIC703 all four
1D	-		instructions enables the sound
1E	Sync select if		
1F	bit 0 = 1		
20			
21			
EE			
EF			
F0	DMA	AM9517A-4	Use of the 16 Registers
.	-	or	is described in the
.	-	I8237-2	MANUFACTURER's MANUAL
.	-		
.	-		
FF	-		

Figure 9: Address decoding.

Addressing of dynamic RAM and ROM is made using the PROM in Pos. 55.

Program instructions which set the flip-flop differ according to MIC70x applied:

MICxxx board	Program instruction	PROM 0	PROM 1
MIC702 MIC703	OUT (18 HEX), A	DISABLE	DISABLE
MIC704	OUT (19 HEX), A	DISABLE	DISABLE
MIC705	OUT (18 HEX), A	ENABLE	ENABLE
	OUT (1A HEX), A *)	DISABLE	ENABLE *)

*) A special flip-flop, PROM CONTROL 1, makes it possible only to enable PROM 1, leaving PROM 0 disabled.

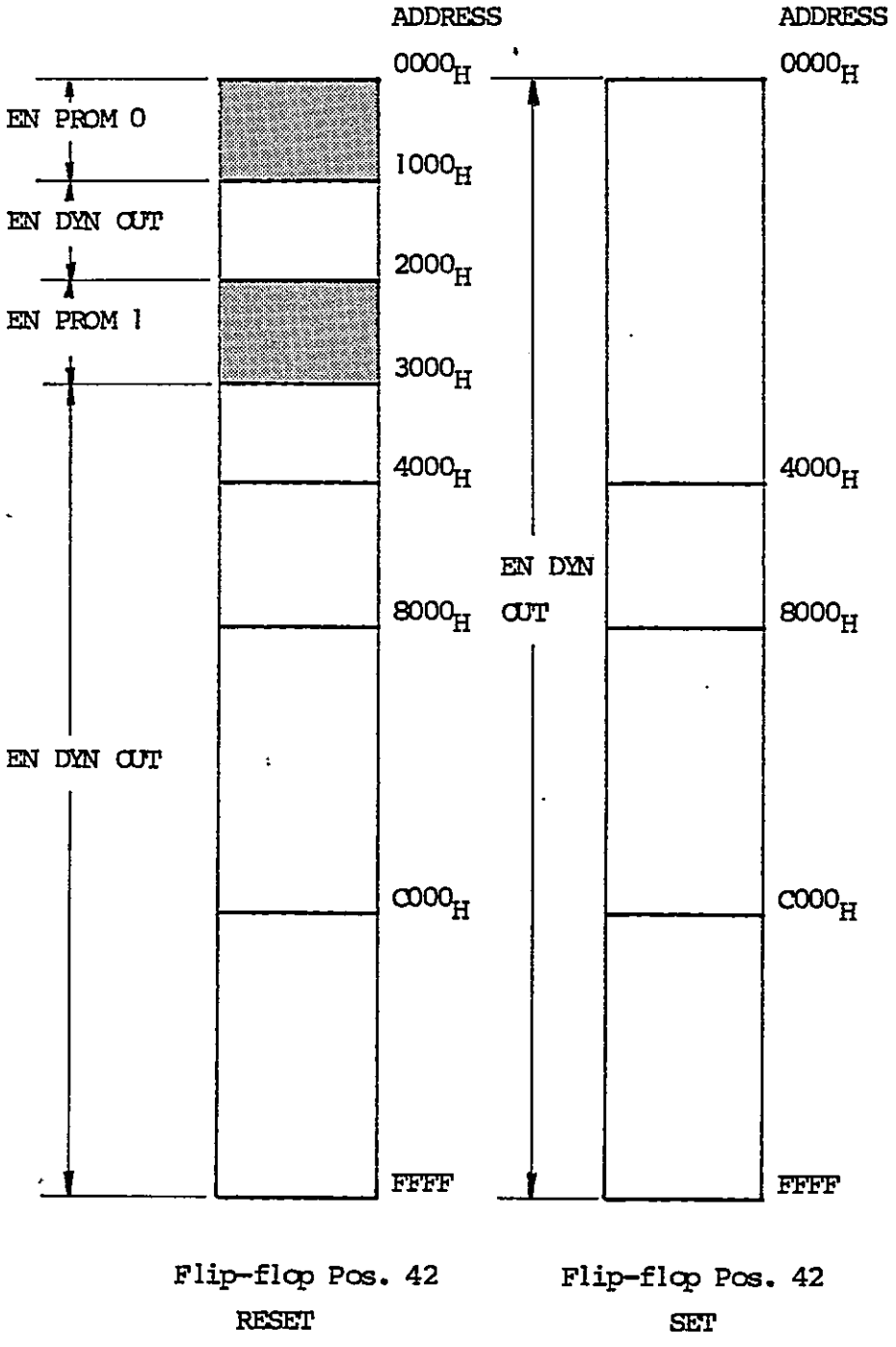


Figure 10: MIC70x; address space.

2.3.3 Parallel I/O Controller

2.3.3

The Z-80A parallel I/O (PIO) interface controller is a programmable, two port device which provides interface between the CPU and the two connectors for keyboard and for parallel I/O. The diagram is shown on page MIC07. The block diagram is shown in fig. 11. The internal structure of the Z80A-PIO consists of a bus interface, internal control logic, port A I/O logic, port B I/O logic, and interrupt control logic.

Each of the two port I/O logic is composed of 6 registers. The registers include: an 8-bit input register, an 8-bit output register, a 2-bit moderegister, an 8-bit mask register, an 8-bit input/output select register, and a 2-bit mask control register.

Before using the PIO it has to be programmed to the wanted Interrupt Vector and operating mode. This is described in manuals from Zilog.

The timing diagram in fig. 12 shows input from keyboard. The interrupt system is described in subsection 2.3.7.

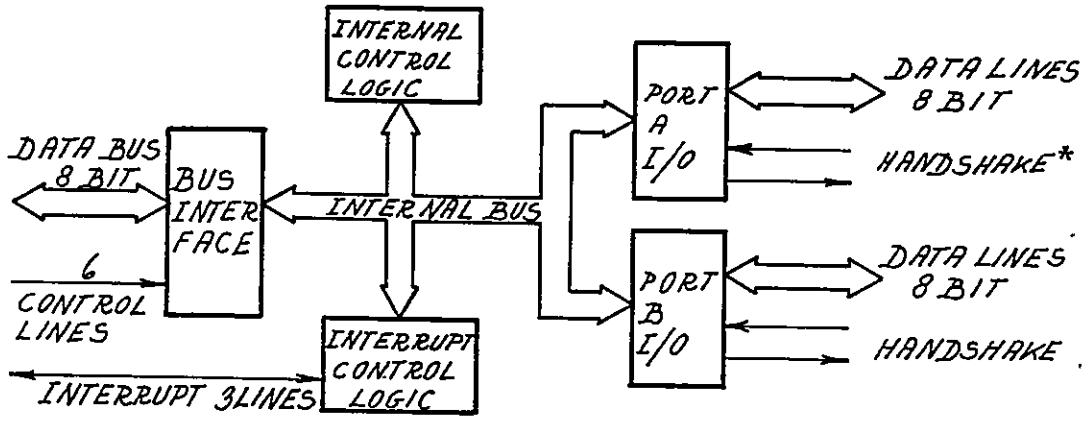


Figure 11: Z80A-PIO; block diagram.

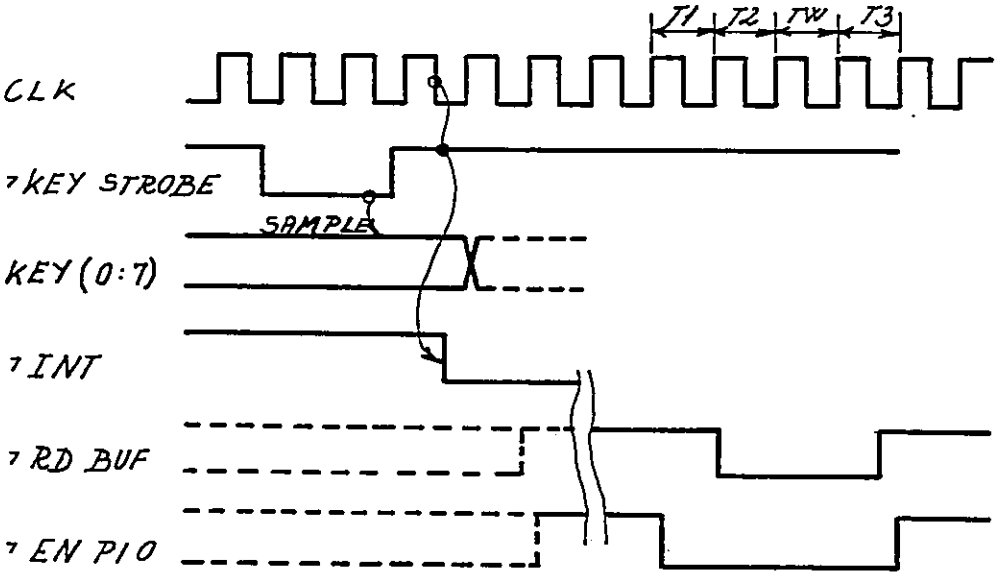


Figure 12: Keyboard input; timing diagram.

2.3.4 Serial Input/Output Controller

2.3.4

The Z80-SIO/2 (Serial Input/Output) is a dual-channel multi-function peripheral component designed to satisfy a wide varity of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller, but - within that role - it is configurable by system software so its "personality" can be optimized for a given serial data communications application.

The Z80-SIO/2 can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. Block diagram for the Z80-SIO/2 is shown in fig. 13.

The internal structure includes Z80A CPU interface, internal control and interrupt logic, and two full duplex channels. Each channel contains read and write registers, and discreet control and status logic that provides interface to modems.

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs, Clear to Send (CTS) and Data Carrier Detect (DCD) are monitored by the discreet control logic under program control. All the modem control signals are general purpose in nature.

The programming for the SIO/2 is very complex and is described in manuals from Zilog.

The Z80-SIO/2 in connection with MIC702 and MIC703 is capable of handling asynchronous formats; in connection with MIC704 and MIC705 it is also possible to handle synchronous formats.

The interface for MIC704 and MIC705 is extended the following way:

1. The modem input signals CALLING INDICATOR and DATA SET READY may be sensed by the program when using the instruction:

   IN (1C HEX), A

   The contents of A will be:

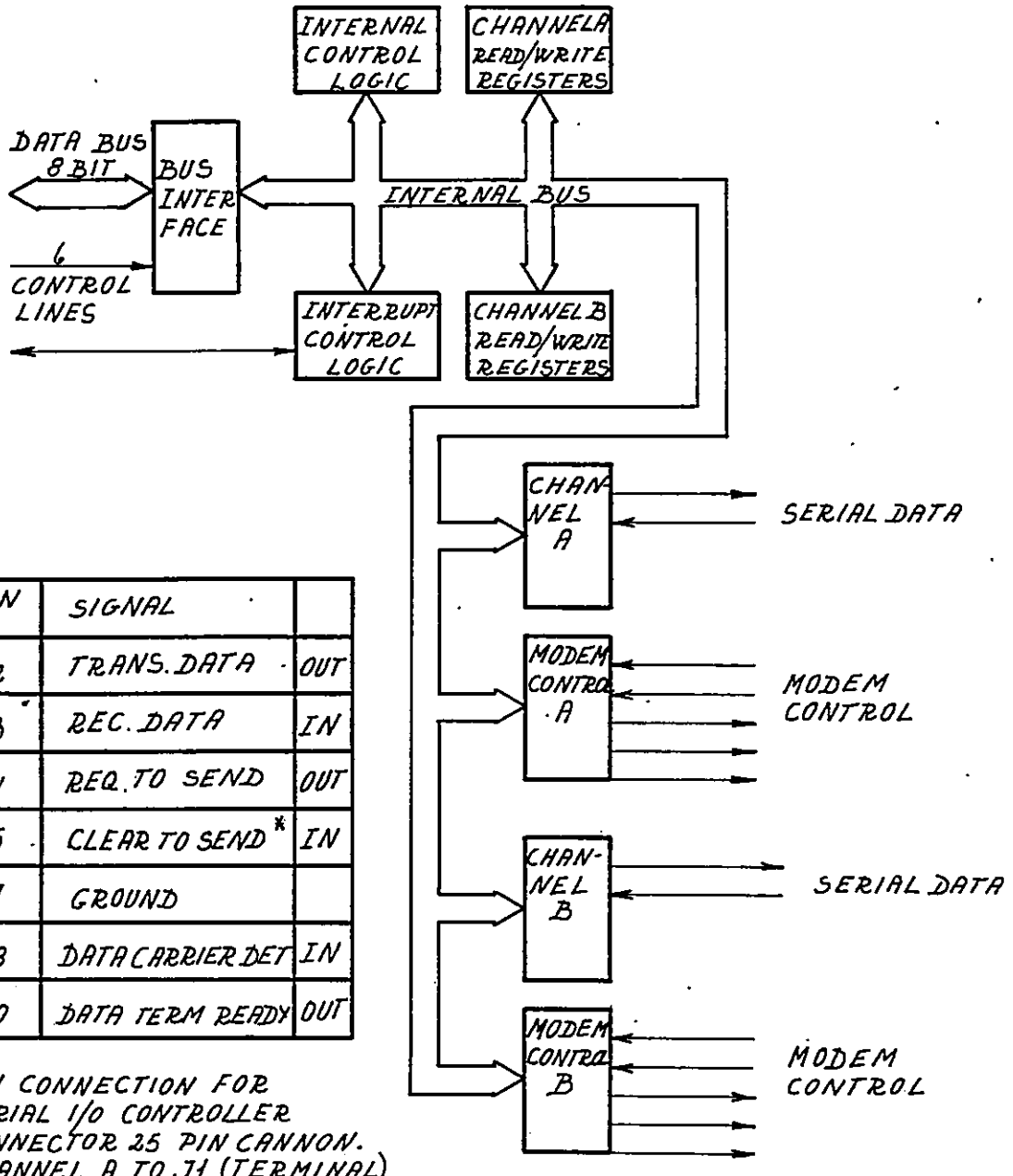
   BIT 0 - CALLING INDCIATOR A
   BIT 1 - DATA SET READY A
   BIT 2 - CALLING INDICATOR B
   BIT 3 - CATA SET READY B

2. The SIO channel A may be used in syncrhonous mode. In this mode the clock signals are supplied from the modem. To do so, a flip-flop has to be set by using the following instruction

   OUT (1E HEX), A

   The resulting state of the flip-flop depends on the value in A bit 1,

   - if 1: flip-flop set.
   - if 0: flip-flop reset.



PIN	SIGNAL	
2	TRANS. DATA	OUT
3	REC. DATA	IN
4	REQ. TO SEND	OUT
5	CLEAR TO SEND *	IN
7	GROUND	
8	DATA CARRIER DET	IN
20	DATA TERM READY	OUT

PIN CONNECTION FOR
SERIAL I/O CONTROLLER
CONNECTOR 25 PIN CANNON.
CHANNEL A TO J1 (TERMINAL)
CHANNEL B TO J2 (PRINTER)
* IF PRINTER CONNECTOR TO 7 BUSY.

Figure 13: Z80A-SIO/2; block diagram; signal connection to J1 and J2.

2.3.5 Counter Timer Controller

The Z80A Counter Timer Controller (CTC) is a programmable four channel device that provides counting and timing functions for the system. The diagram is shown in page MIC15 and the block diagram is shown in fig. 14.

The internal structure of the Z80-CTC consists of a Z80 CPU bus interface, internal control logic, four counter channels, and interrupt control logic. Each channel has an interrupt vector for automatic interrupt vectoring, and interrupt priority is determined by channel number with channel 0 having the highest priority.

The channel logic is composed of 2 registers, 2 counters, and control logic as shown in fig. 15. The registers include an 8-bit constant register and an 8-bit channel control register. The counters include an 8-bit readable down counter and an 8-bit prescaler. The prescaler may be programmed to divide the system clock by either 16 or 256.

Channel 0 and 1 are used to generate the clock to channel A and B in the Z80A-SIO/2. The clock delivered to the SIO is again divided in the SIO to make the baudrate for the terminal and printer connections. Input to these two channels is a clock of 0.614 Mhz. How the clock is divided in the SIO is shown in fig. 16.

Channel 2 and 3 are initiated in counter mode with interrupt enabled and with a time constant of 1. This means that for every clock input an interrupt is sent to the CPU. Channel 2 is connected to the display controller and channel 3 is connected to the floppy controller, and in this way their interrupt is connected to the CPU.

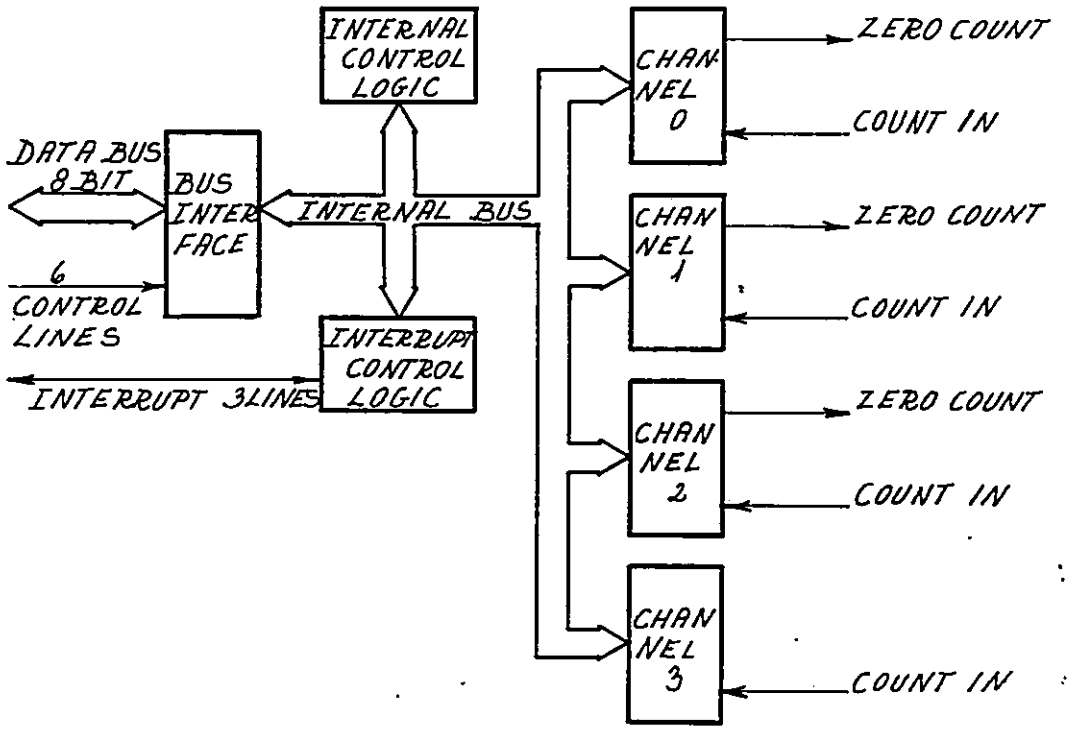


Figure 14: Z80A-CIC; block diagram.

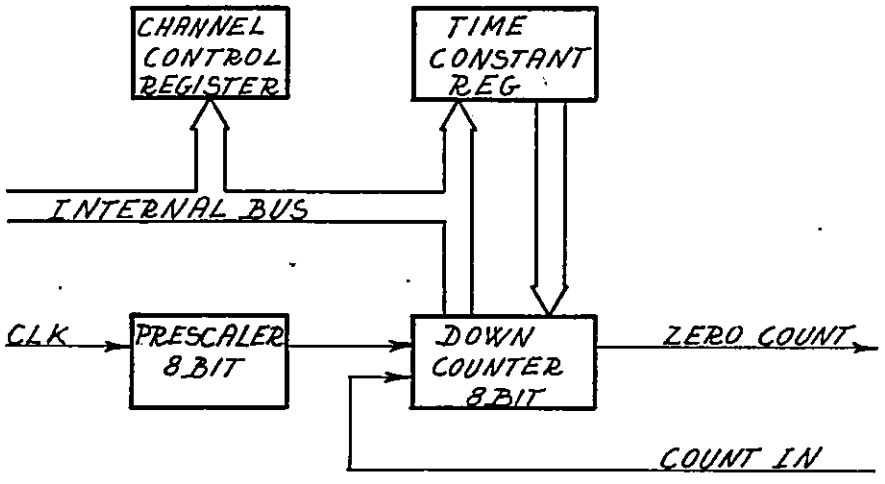


Figure 15: Z80A-CIC; channel; block diagram.

CTC Input	CLOCK Divided by	CTC OUTPUT	SIO Divided by	SIO Period	SIO BAUD RATE
T in µsec	decimal	T in µsec	decimal	µsec	bps
0.614	193	314	64	19.970	50
0.614	128	208	64	13.310	75
0.614	88	144	64	9.222	110
0.614	64	104	64	6.667	150
0.614	32	52	64	3.333	300
0.614	64	104	16	1.667	600
0.614	32	52	16	833.3	1200
0.614	16	26	16	416.7	2400
0.614	8	13	16	208.3	4800
0.614	4	104	16	104.2	9600
0.614	2	52	16	52.1	19200

Fig. 16: Generation of baudrate.

2.3.6 Interrupt System

The CPU has two interrupt inputs, a software maskable interrupt and a non-maskable interrupt. The non-maskable interrupt (NMI) cannot be disabled by the program and is not used in MIC70x. The CPU can be programmed to respond to maskable interrupts in one of three modes. In MIC70x mode 2 is selected. In this mode a single 8-bit byte from the controller (the interrupt vector) is used to make an indirect call instruction.

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted a special M1 cycle (INTA) is generated. During this M1 cycle IORQ becomes active (instead of MREQ) indicating the INTA cycle. The Z80 peripherals have an interrupt enable input (IEI) and an interrupt enable output (IEO) and are connected in daisy chain. The peripheral with IEI high and IEO low, will during INTA place the preprogrammed 8-bit interrupt vector on the data bus.

IEO is held low until a return from interrupt (RETI) instruction is executed by the CPU while IEI is high. The 2-byte RETI instruction is decoded internally by the peripheral for this purpose.

Fig. 17 shows the daisy chain interrupt system in MIC70x.

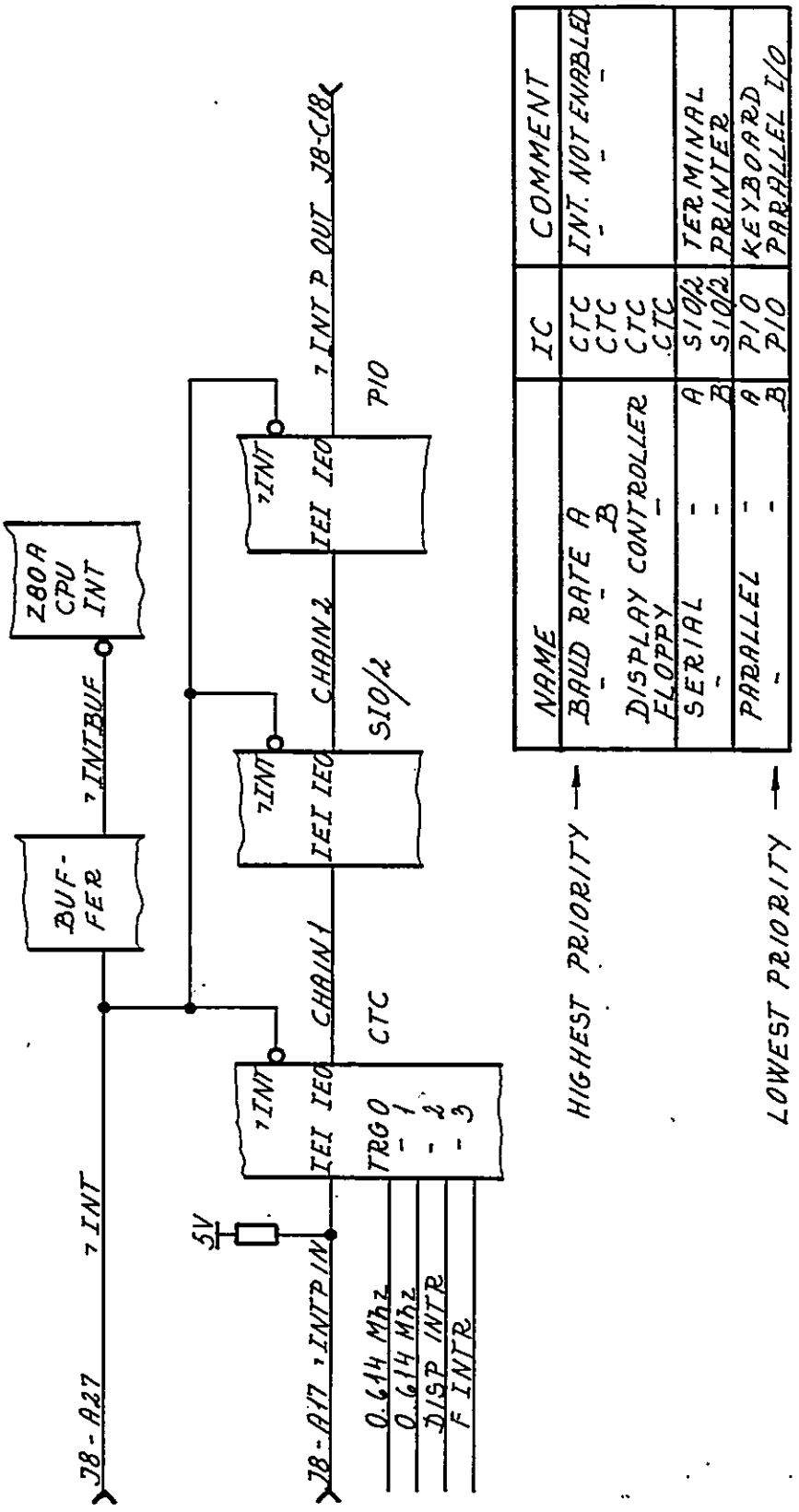


Figure 17: MIC70x; interrupt priority.

2.3.7 ROM Memory

The ROM, Read Only Memory, contains the autoload program. After a reset signal is generated, the CPU starts to execute the program stored in ROM pos. 66. In subsection 2.3.3 is shown how this addressing is made. In a test situation both ROM pos. 66 and 65 may contain a ROM. The ROMs are normally 2 K bytes PROM.

ROM pos. 65 on MIC705 contains a built-in PROM with test programs.

2.3.8 RAM Memory

The RAM, Random Access Memory, is shown in 3 blocks in the block diagram: the TIMING GEN block, the 64 K BYTES RAM block, and the REG. block. This subsection describes these 3 blocks. The circuit diagram is on page MIC05. The timing generator is made using the IC I8202A. This circuit makes all the signals which the RAM circuits need. Fig. 18 shows the block diagram for the I8202 and the timing diagram for the whole RAM circuit is shown in fig. 19.

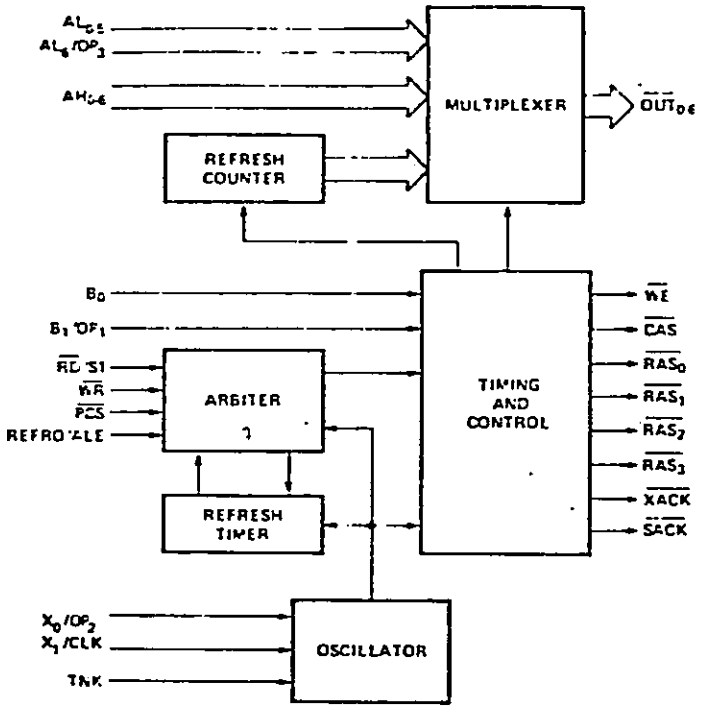


Figure 18: I8202A-RAM Controller; block diagram.

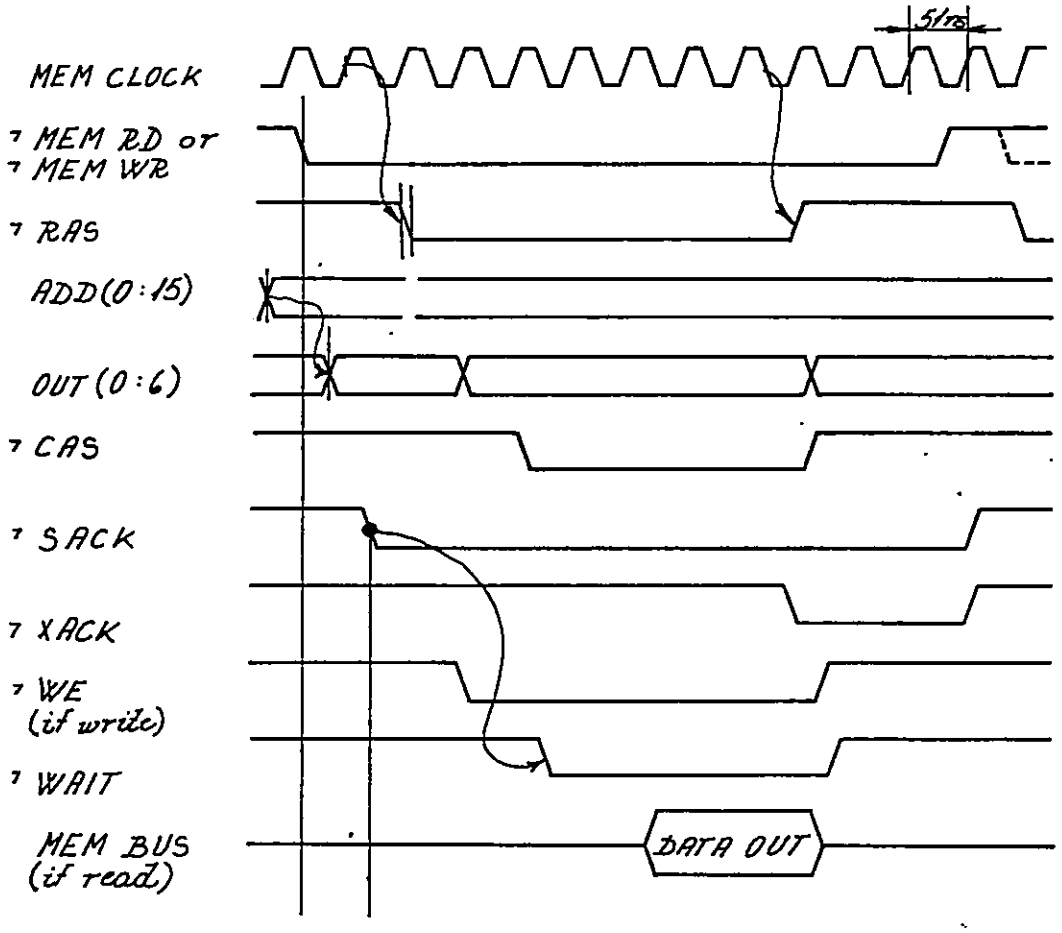


Figure 19: RAM System; timing diagram.

2.3.9 DMA Controller

The DMA controller to MIC702 is based on the Am9517A-4 from Advance Micro Devices or an 8237A-5 from Intel. The IC is designed to be used in conjunction with an external 8-bit address register made by an 74LS373. The circuit diagram is shown in MIC06. The Am9517A-4 contains 4 channels which have full 64 K address and word count capability.

The four channels are in MIC70x used in the following way:

channel 0 : External debugger
channel 1 : Floppy disk controller
channel 2 : Display controller
channel 3 : Display controller.

The block diagram for Am9517A-4 is shown in fig. 20.

Fig. 21 shows the timing diagram for a normal operation of Am9517A-4.

A more specific description of the units may be obtained from one of the two manufacturers.

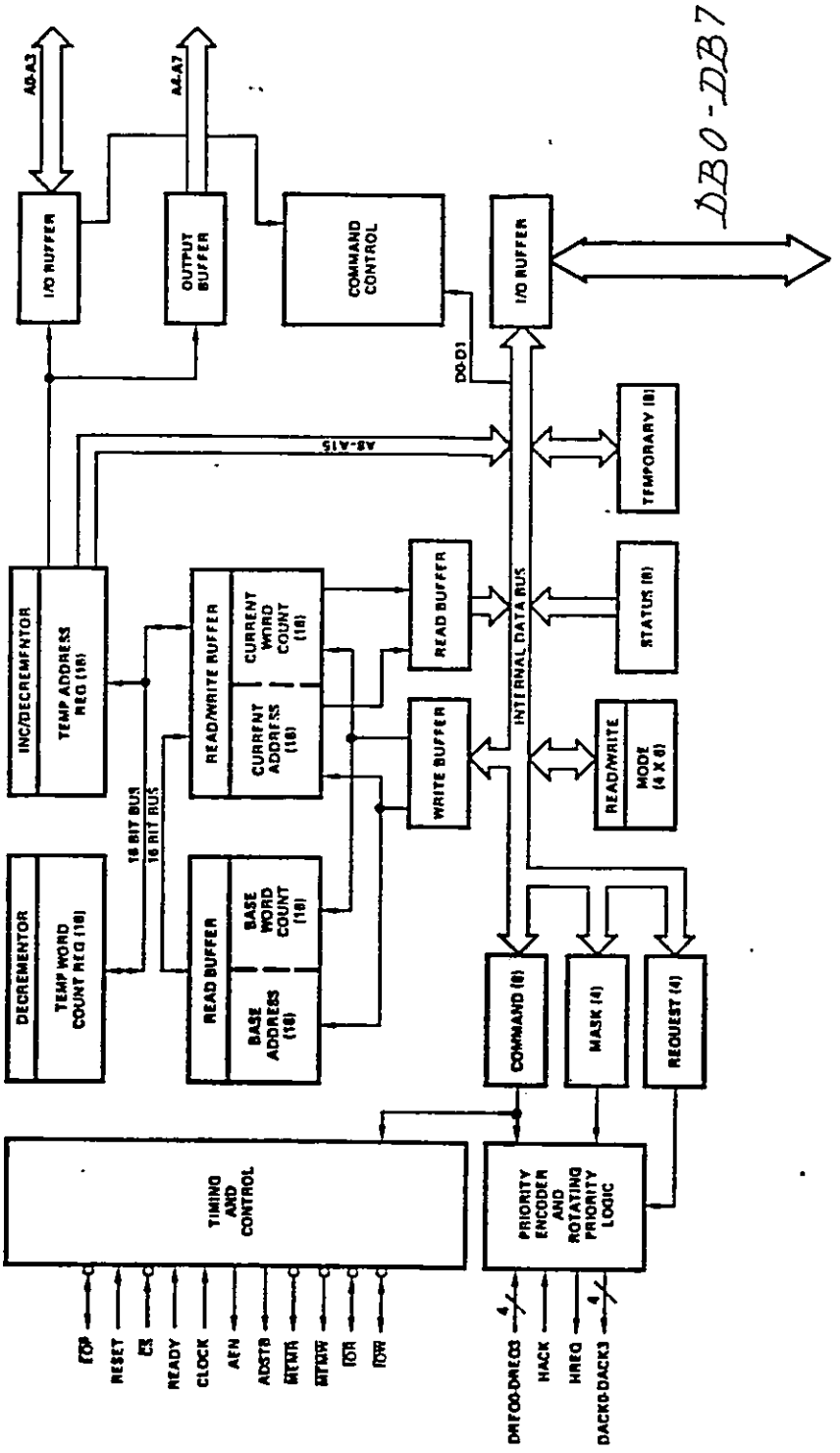
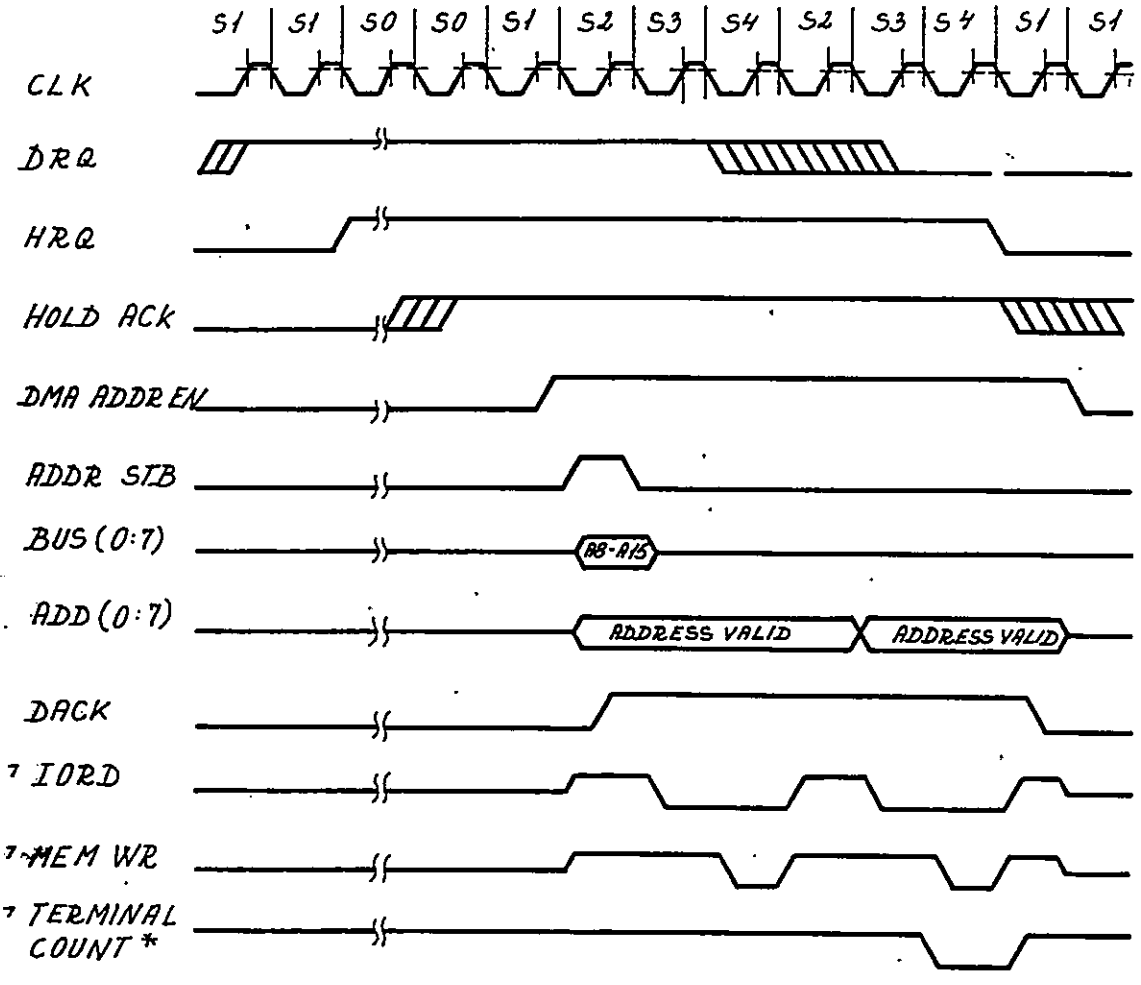


Figure 20: Am9517A-4 - DMA Controller; block diagram.



* Only if last byte in the block.

Figure 21: Am9517A-4 - DMA Controller; timing diagram.

2.3.10 Select Switches

MIC702 and MIC703

These MIC boards are equipped with 8 switches which can be sensed by the program.

One switch (BIT 7) is used for selection of MINI or MAXI floppy discs and reading this switch indicates the kind of floppy with which the system is equipped.

MIC704 and MIC705 (see also diagram MIC17)

These MIC boards are equipped with 7 switches (BIT 0-6).

The selection between MINI/MAXI floppy is made using two switches (see diagram MIC17). Using these switches provide for 3 possibilities:

1. MINI SELECTED
2. MAXI SELECTED
3. PROGRAM SELECTS MINI OR MAXI.

When PROGRAM SELECTS... is used, a reset signal selects MINI. Using the instruction:

OUT (14 HEX), A

the selection depends on the value of A bit 1:

- if 1: selects MAXI
- if 0: selects MINI

Reading BIT 7 indicates which kind of floppy is selected (just the same way as for MIC702/MIC703).

2.3.11 Display Controller

2.3.11

The display controller is based on the 8275 programmable CRT controller from Intel. The device interfaces the CRT raster scan display with the system. The controller refreshes the display by buffering the information from the memory and it keeps track of the display position of the screen. Fig. 22 shows a block diagram for the 8275 controller.

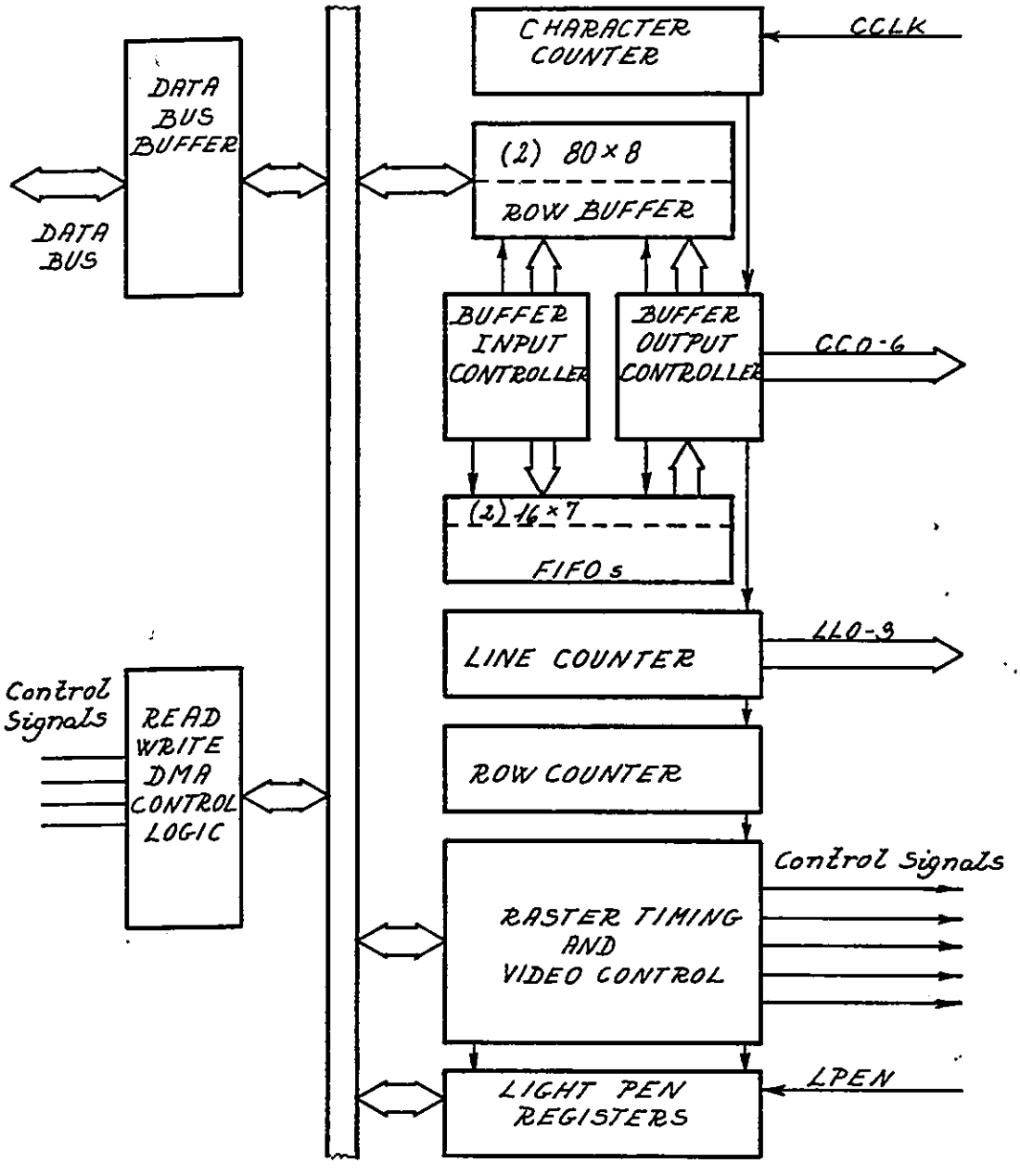


Figure 22: I8275 - CRT Controller; block diagram.

The program initiates the controller to make the wanted picture. The initiations needed may be seen in the description from Intel.

The initiation made in MIC702 is listed in fig. 23.

Initiation of 8275 makes the following picture on the monitor used.

		Comments
80	Chars per row	
25	Rows of characters	
5	Char. Dot matrix width	Made in Char. generator
9	Char. Dot matrix height	Made in Char. generator
7	Char cell width	
11	Char cell height	
50 Hz	Frame frequency	Sync. with mains freq.
275	Active scan lines	
33	Vertical blanking intervals	
308	total scan lines	
15.4 Khz	Line frequency	
65 µsec	Line periode time	
150 µsec	Vertical sync. time	Made with monostable
28	Char. time for horz. blank	
108	Char. time each line	
0.601 µsec	Char time	
86 nsec	DOT time	
11.64 MHz	DOT frequency	
4.5 µsec	Horizontal sync. width	Made with monostable
5.8 µsec	Horizontal sync delay	Made with monostable
	Blinking field cursor	

Figure 23: I3275-CRT controller; initiation.

The display controller needs a number of registers, etc. to support it. These circuits are shown in diagram pages MIC11 to MIC14. Fig. 24 shows a block diagram with this circuit.

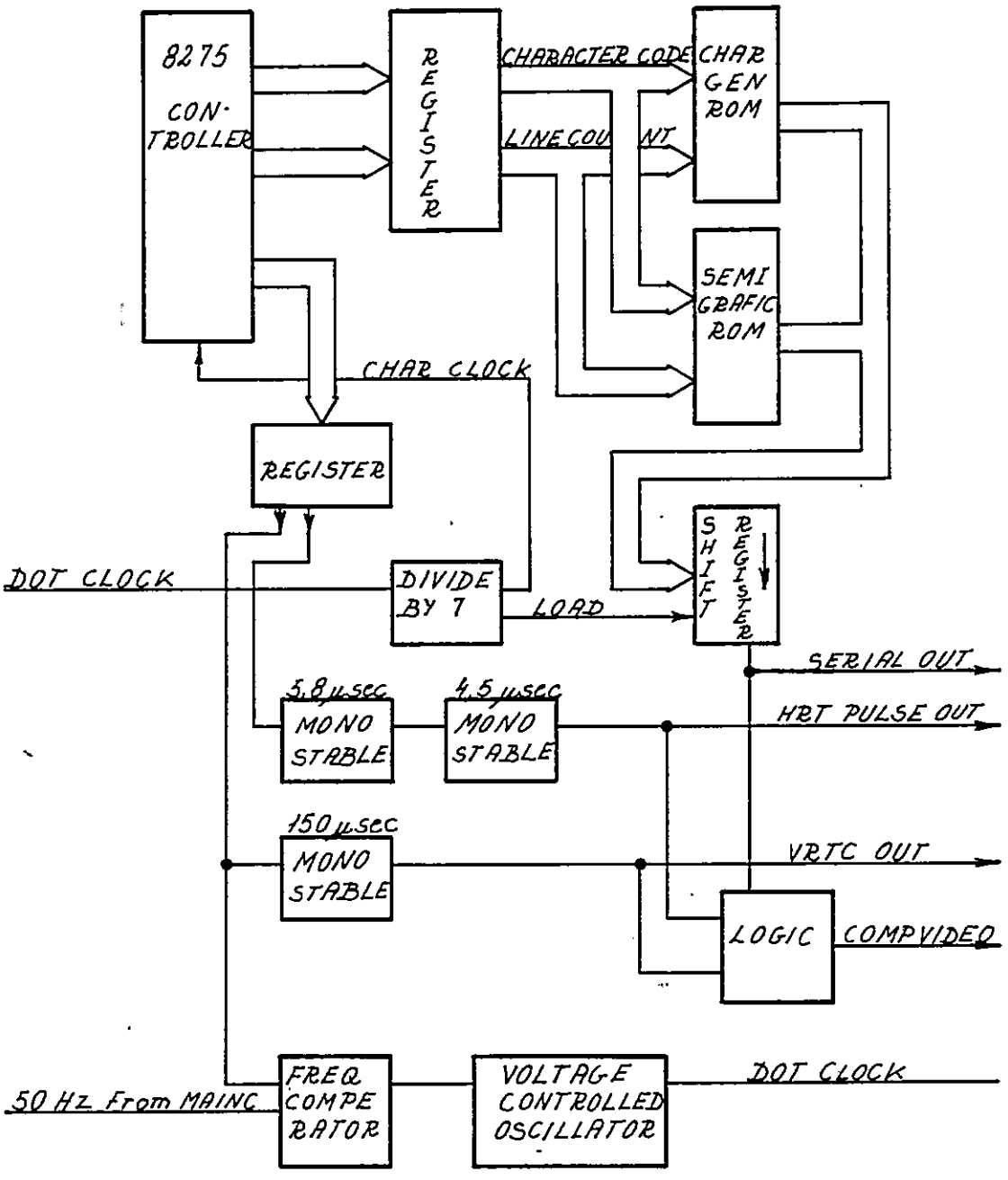


Figure 24: Display System; block diagram.

Note: Only comp.sync. is used in MIC702.

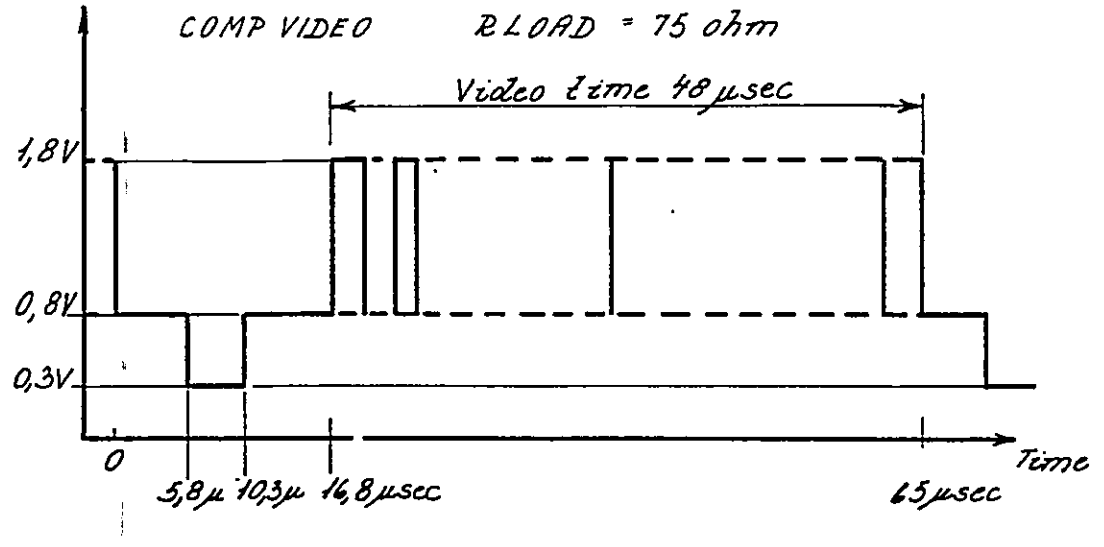
The output from the display controller system is made with comp. sync and with normal TTL signal output. In RC702 the comp. sync. is used and fig. 25 shows the timing of this signal.

As described in the manual for 8275, it is possible to use 'Field Attributes'.

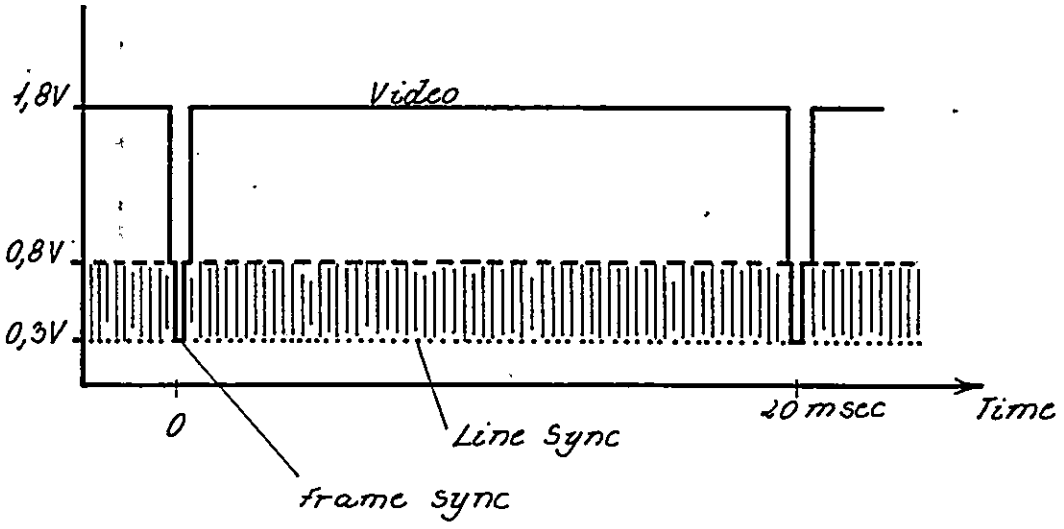
MIC70x

The following codes may be used:

Blink
Reverse video
Underline
Semigraphic (general purpose bit 2).



Comp. Sync signal for one Line.



Comp. Sync signal for one frame.

Figure 25: MIC702; COMP. SYNC. signal; timing diagram.

2.3.12 Floppy Disk Controller

2.3.1

The floppy disk controller to MIC70x is based on the FDC chip µPD765 from NEC or 8272 from Intel. The chip contains the circuitry and control functions for interfacing the processor to 4 floppy disk drives. It supports both IBM3740 single density format (FM) and IBM system 34 double density format including double sided recording.

Fig. 26 shows a block diagram for the controller chip.

NOTE!

To allow for a better Read Recovery, improvements have been made in the circuits which interacts with the controller.

The improvements are:

1. The digital Read Recovery has been changed from a 4-bit to a 5-bit system.

2. The write precompensation timing has been modified to reflect the Low Current signal of MAXI floppy discs (the signal is active at the inner trac) as follows:

   Low Current off: 125 nsec write cycle
   (the normal condition)

   Low Current on : 250 nsec write cycle
   (modified condition)

The improvements are implemented as follows:

MIC702 and MIC703

Applying the FCO 19-008. The FCO is not required if single density recording is used only.

MIC704 and MIC705

Incorporated in the MIC board construction.

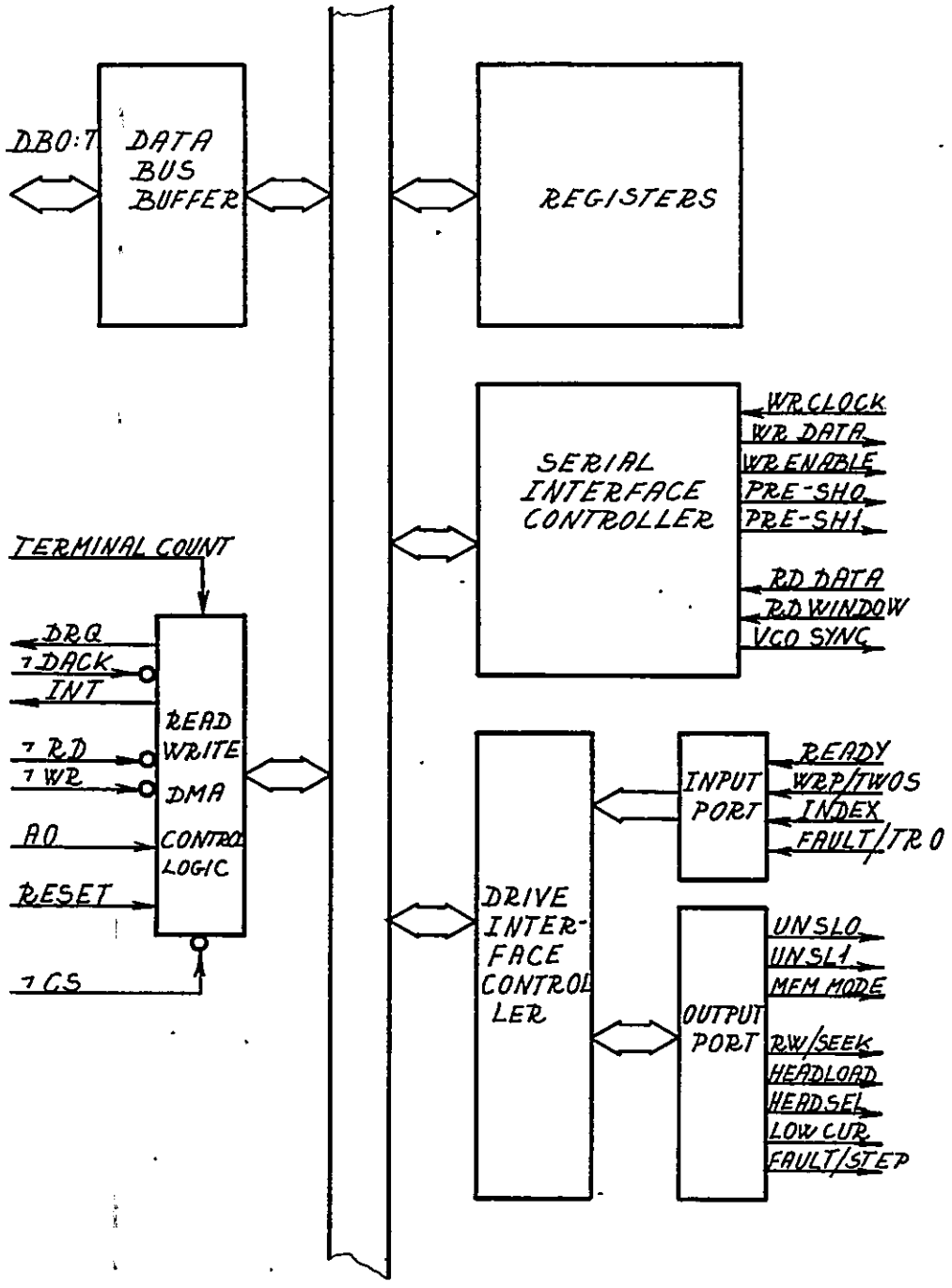
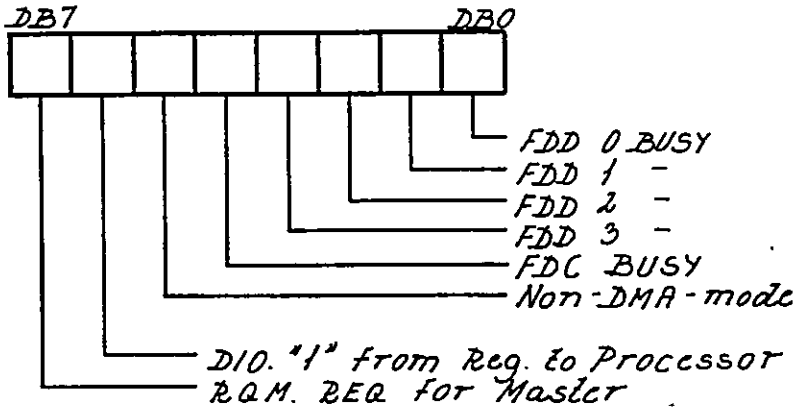


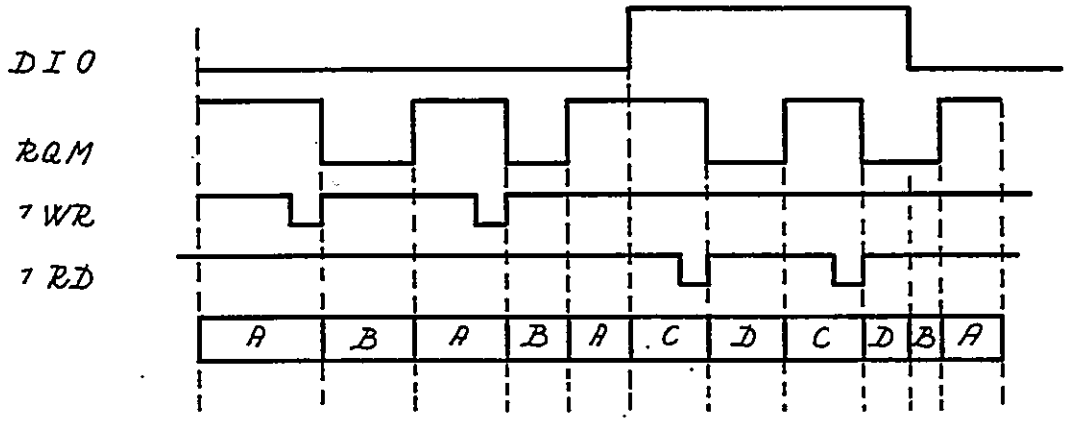
Figure 26: µPD765 - Floppy Disc Controller; block diagram.

The μPD765 contains two registers which may be accessed by the program. The 8-bit main status register contains the status information of the FDC and may be accessed at any time. The 8-bit data register (actually consists of several registers in stack with only one register present to the bus at a time), which stores data, commands, parameters, and floppy disk drive information. Fig. 27 shows the information stored in the status register.

STATUS REGISTER (MAIN STATUS REGISTER)

One 8-bit byte with inf. of the controller.





A Data register ready to be written into by CPU

B - - not ready - - - - - - -

C - - ready for next byte to be read

D - - not ready - - - - -

Figure 27: µPD765 - Floppy Disc Controller; status register.

Fig. 28 shows the information delivered to and from the data register during a read or write instruction to the controller. The programming of µPD765 is very complex and is described by the manufacturer. The controller interfaced to both Maxi- and Mini disk drives. The circuits on diagrams MIC09 and MIC10 show this.

PHASE	R/W	DATA BUS D7 D6 D5 D4 D3 D2 D2 D0	REMARKS
		READ DATA	
Command	W	MT MF SK 0 0 1 1 0	
	W	X X X X X HD US1 US0	
	W	Cylinder number (current)	
	W	Head address	
	W	Record (Sector number)	
	W	Number (of data bytes/sector)	
	W	End of track	
	W	Gap Length	
	W	Data Length	
Execute			
Result	R	Status 0	
	R	Status 1	
	R	Status 2	
	R	Cylinder number (current)	
	R	Head address	
	R	Record (sector number)	
	R	Number (of data bytes/sector)	

Figure 28: µPD765 - Floppy Disc Controller; data register; read/write information flow.

Data Register of 8-bit bytes (Several registers in a stack). All commands contains a command phase, an execution phase and a result phase.

Fig. 29 shows the data media/floppy diskette. The diskette contains a number of tracks which again are divided into a number of sectors as shown in fig. 30. The controller is able to format, read, or write the diskette. Information about the actual formats used is available in the software manuals. Fig. 31 shows the two recording methods used.

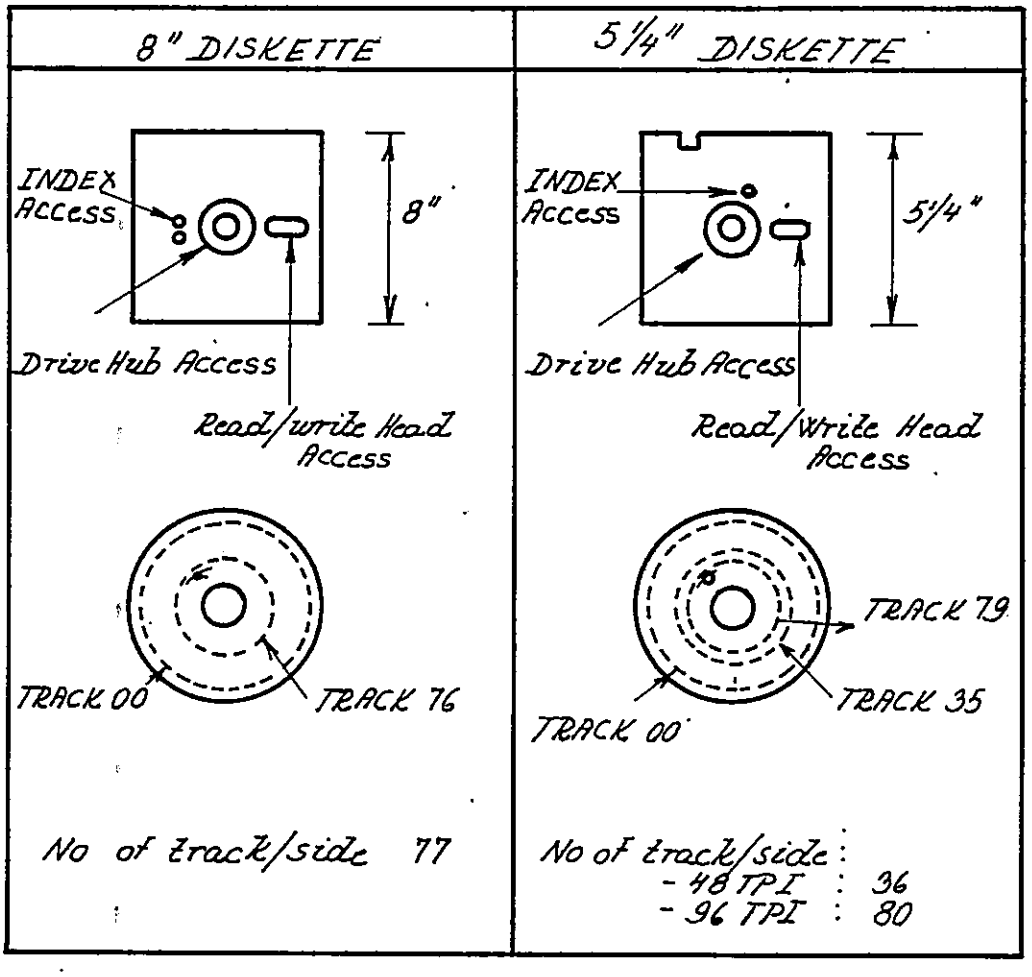
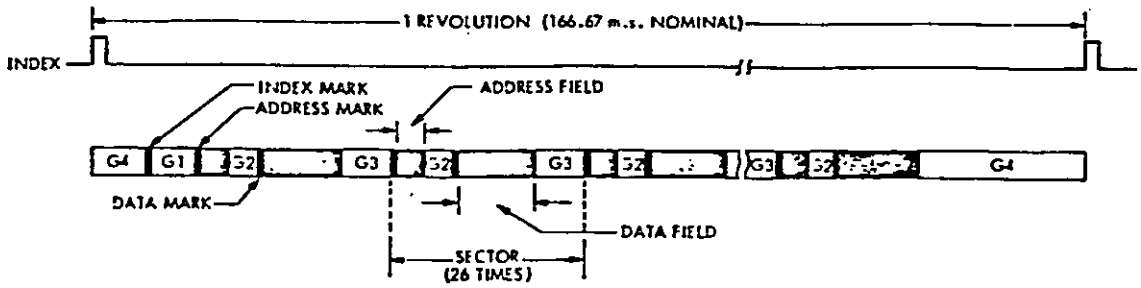
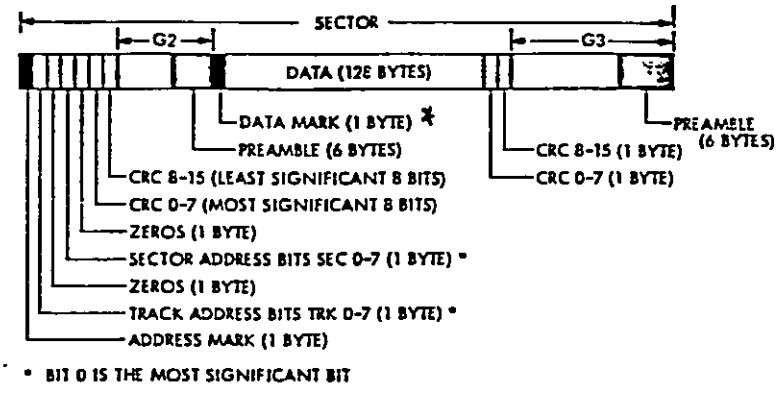


Figure 29: Floppy disc; data media.



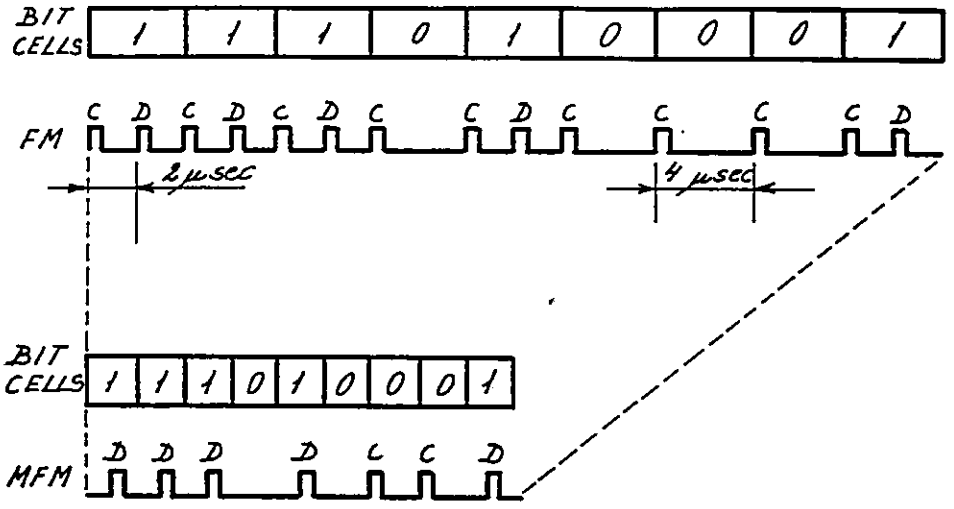


GAP FIELDS

G1 = 26 BYTES HEX FF
6 BYTES HEX 00
G2 = 11 BYTES HEX FF
6 BYTES HEX 00
G3 = 27 BYTES HEX FF
6 BYTES HEX 00
G4 =314 BYTES HEX FF
6 BYTES HEX 00

* DATA MARK is also called 'Data Address Mark'

Figure 30: Diskette track; information storage; example (8" diskette).



D ~ Data Pulse
C ~ Clock -"-

FM is also called single Density.
MFM - - - double -

	8" DISK		5¼" DISK	
	FM	MFM	FM	MFM
Bit Cell	4 µs	2 µs	8 µs	4 µsec
Flux Changes/Cell	2	1	2	1
- - /Inch	6536	6536	2728	5456
Kilo Bits/Sec	250	500	125	250
Frecuency Ratios	2/1	2/1	2/1	2/1
Bit to Bit spacing	2 µs 4 µs	2 µs 3 µs 4 µs	4 µs 8 µs	4 µs 6 µs 8 µs

Figure 31: Floppy disc; recording methods.

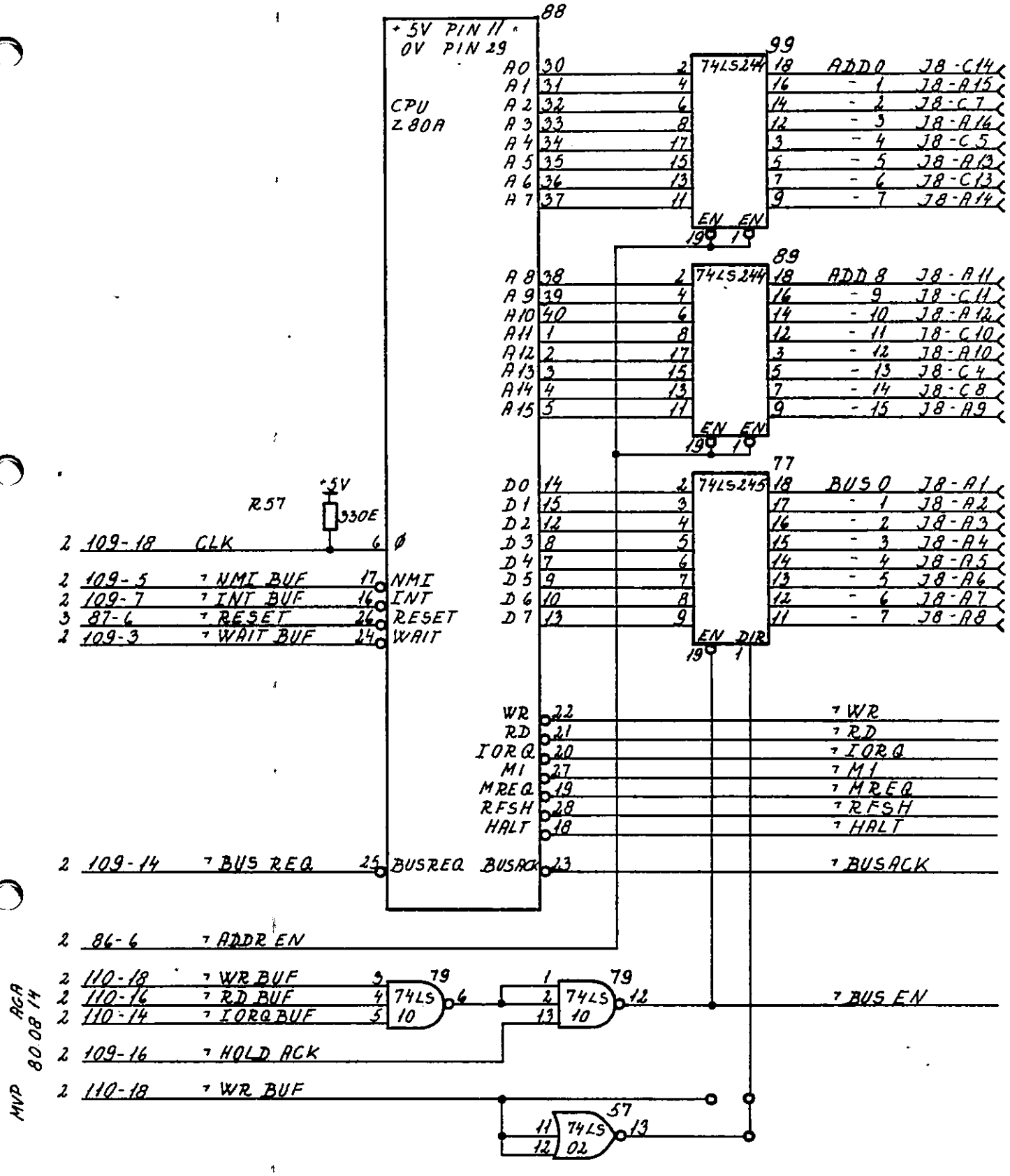
2.4 Schematic Diagrams

This subsection contains diagrams as follows:

Note: The MIC-diagrams are referred to by MICxx numbers, not figure numbers.

2.4.1 MIC702/MIC703

Signal	Destination MIC No.	Description
ADD(0:15)	3, 4, 5, 6, 7, 9, 11, 15, 16	The address bus is the TRI-state bus supplying address information to all the controllers.
BUS(0:7)	3, 5, 6, 7, 9	The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
WR	2	WRITE output from the CPU.
RD	2	READ - - - -
IORQ	2	INPUT OUTPUT REQUEST, when active the WR or RD pulse is addressing a controller and not the memory.
MI	2	MACHINE CYCLE ONE, indicates the op code fetch cycle of the CPU.
MREQ	2	MEMORY REQUEST, indicates a read or write memory cycle.
RFSH	2	REFRESH, indicates a refresh cycle by the CPU, the signal is not used in MIC702.
HALT		HALT indicates that the CPU is executing a halt instruction. An error situation.
BUS ACK	2	BUS ACKNOWLEDGE, the CPU has received a BUS REQ and lets the DMA use the BUS.
BUS EN	1	BUS ENABLE for the CPU.



MIC 702
MIC 703

MICROPROCESSOR CPU AND ADDR/DATA REGISTERS

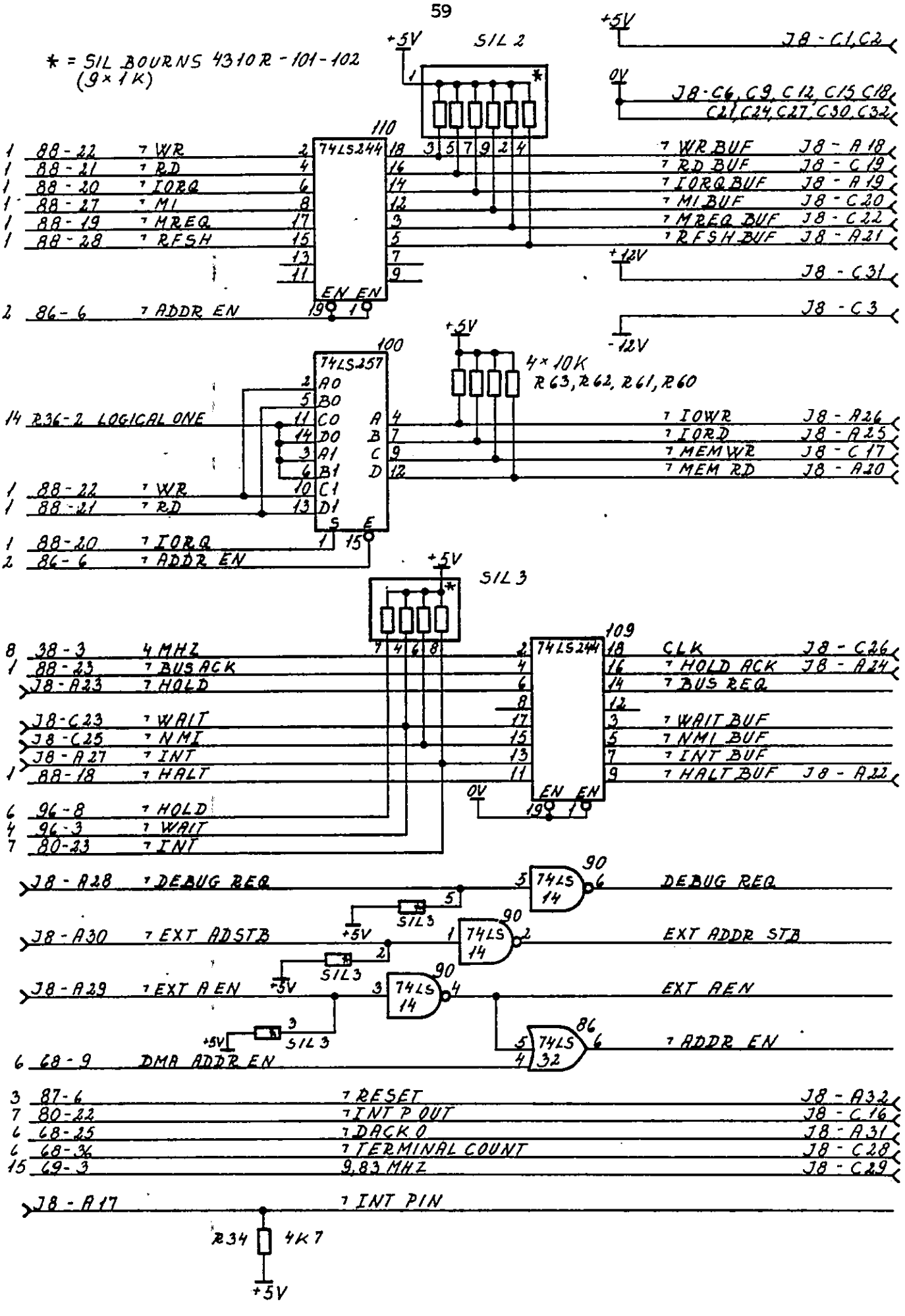
MIC 01

R 13617

Signal	Destination MIC No.	Description
WR BUF	1	* WRITE output pulse from the CPU
RD BUF	1, 7, 15, 16	* READ - - - - -
IORQ BUF	1, 7, 15, 16	* IORQ - - - - -
M1 BUF	7, 15, 16	* M1 - - - - -
M REQ BUF	4	* M REQ - - - - -
RFSH BUF		* RFSH - - - - -
IOWR	3, 6, 7, 9	** INPUT/OUTPUT WRITE, write pulse to controllers which are not of the Zilog type.
IORD	6, 9, 11, 15	** INPUT/OUTPUT READ, read pulse to controllers which are not of the Zilog type.
MEM WR	4, 5	** MEMORY WRITE pulse.
MEM RD	3, 4, 5	** MEMORY READ pulse.
CLK	1, 4, 6, 7, 15, 16	4 MHz symmetric clock to the system.
HOLD ACK	1, 6	BUS ACK signal through a buffer.
BUS REQ	1	The DMA controller or the tester demand control over the BUS.
WAIT BUF	1	This signal inserts at least one wait state in each CPU cycle.
NMI BUF	1	NON MASKABLE INTERRUPT, only used by a tester.
INT BUF	1	INTERRUPT REQUEST to CPU.
HALT BUF		HALT signal through a buffer.
DEBUG REQ	6	DMA REQUEST from a tester.
EXT ADDR STB	6	DMA REQUEST signal from a tester.
EXT AEN		- - - - - -
ADDR EN	1, 2, 3, 4, 6	ADDRESS ENABLE when active the CPU controls the BUS system.
INT PIN	15	INT PIN may be used by a unit connected to J8 and is interrupt priority in.

* signal is only active, when ADDR EN is active.

** Signal may also be active when ADDR EN is active. The DMA also uses these signals, which are of the TRI-state type.



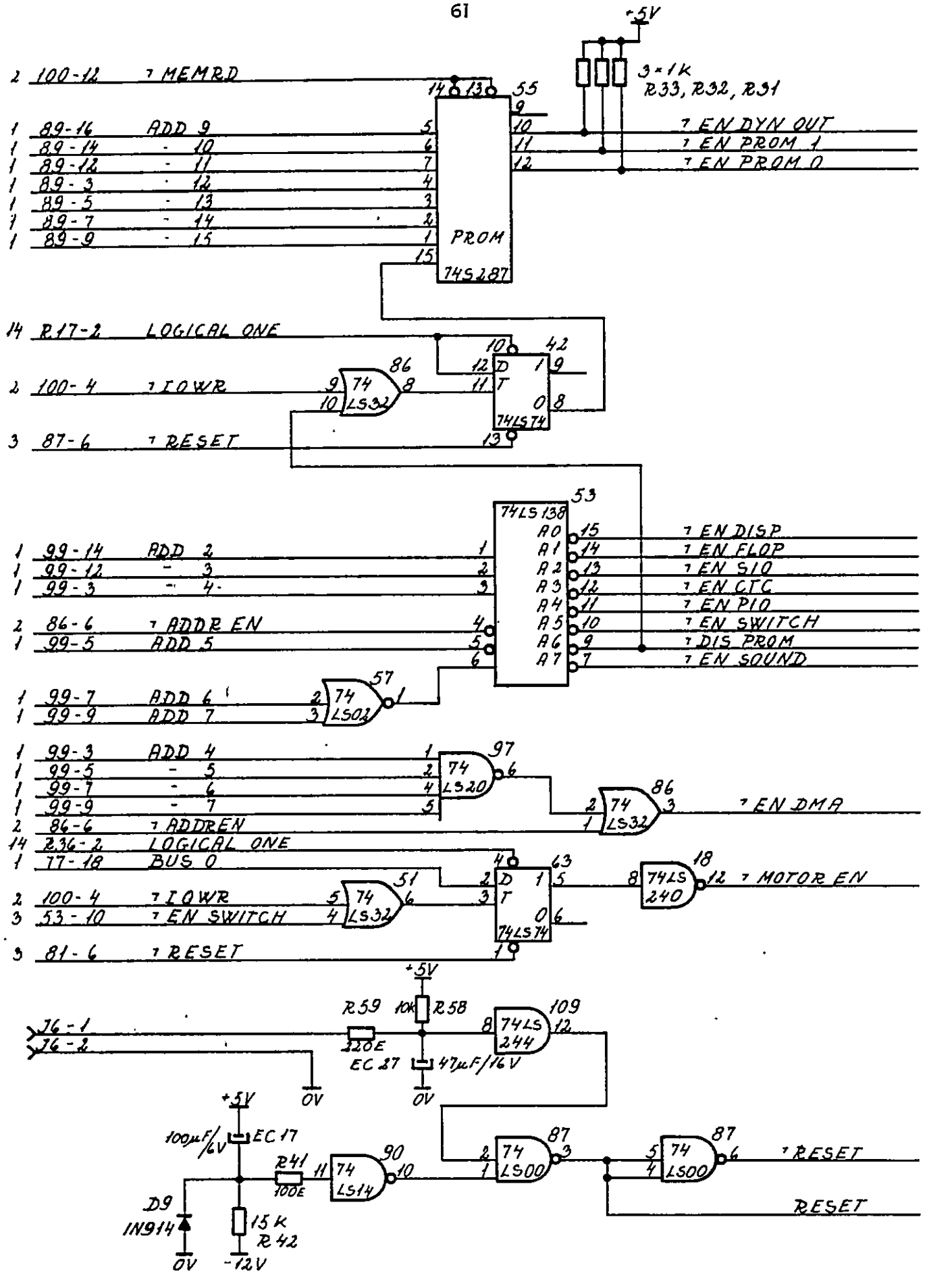
MIC 702
MIC 703

CONTROL SIGNALS RECEIVERS AND TRANSMITTERS

MIC 02

R 13618

Signal	Destination MIC No.	Description
EN DYN OUT	5	* This signal enables the output register from the RAM.
EN PROM 1	4	* This signal enables the output from PROM 1 which is only used when running a testprogram.
EN PROM 0	4	* This signal enables the output from PROM 0 which contains the program used under initiation.
EN DISP	11	* ENABLE DISPLAY controller
EN FLOP	9	* ENABLE FLOPPY controller
EN SIO	16	* ENABLE SERIAL IN/OUT controller
EN CTC	15	* ENABLE COUNTER/TIMER controller
EN PIO	7	* ENABLE PARALLEL IN/OUT controller
EN SWITCH	3, 15	* ENABLE SWITCHES
DIS PROM		* DISABLE PROM, the signal is used to disable the PROM and enable the whole RAM
EN SOUND	7	* ENABLE SOUND gives the accoustic signal
EN DMA	6	* ENABLE DMA controller
MOTOR EN	10	MOTOR ENABLE is used to switch on and off the motor used in the Mini floppy disk drive.
RESET	1, 3, 6, 9, 11 15, 16	RESET is the power up reset or a RESET initiated from the switch on the front of the computer.
		* Subsection 2.3.3. describes the actual addresses used in MIC702.



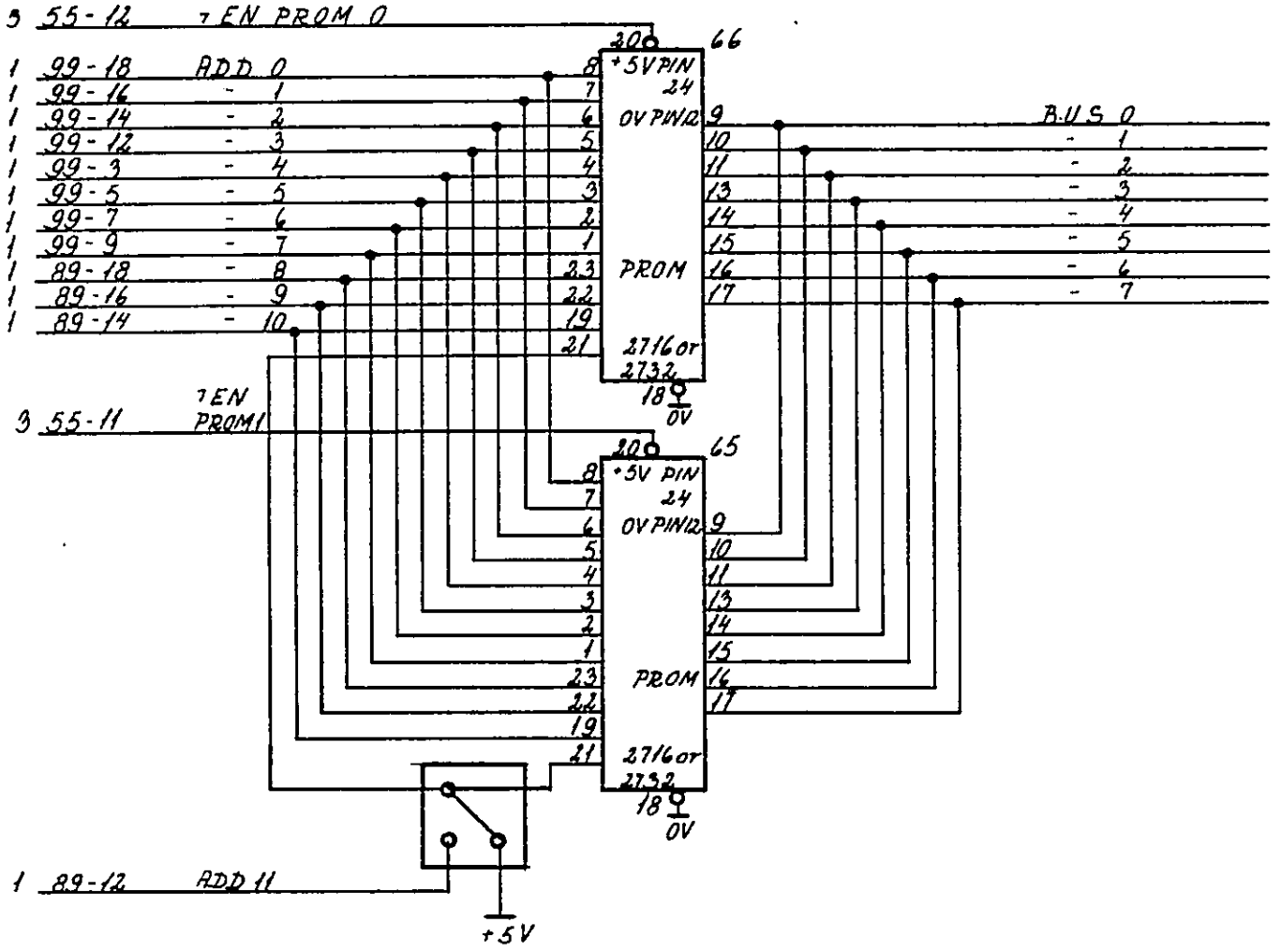
MIC 702
MIC 703

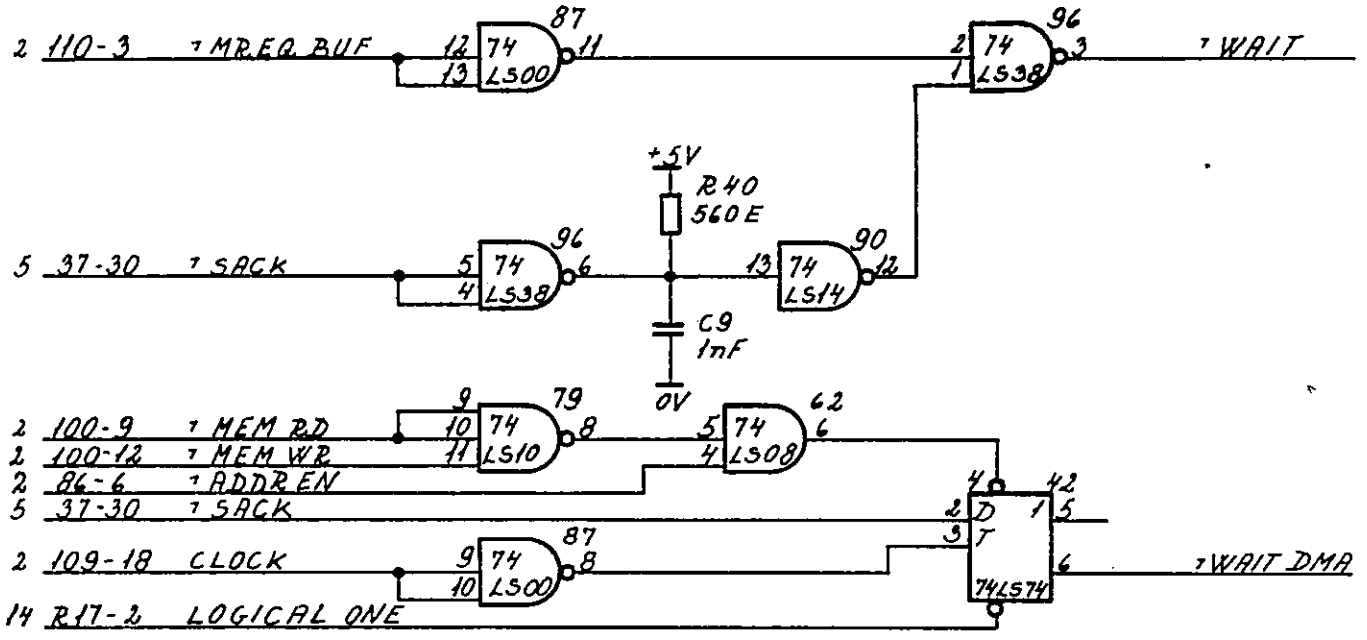
ADDRESS DECODERS & RESET CIRCUIT

MIC 03

R13619

Signal	Destination MIC No.	Description
BUS(0:7)		The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
WAIT	2	WAIT supplies at least one wait state to the CPU-fetch cycle. More wait states are inseted when the RAM controller is making a refresh cycle.
WAIT DMA	6	WAIT DMA supplies at least one wait state in the DMA-cycle. More wait states are supplied when the memory controller is making a refresh cycle.





MVP AGA 80 08.14

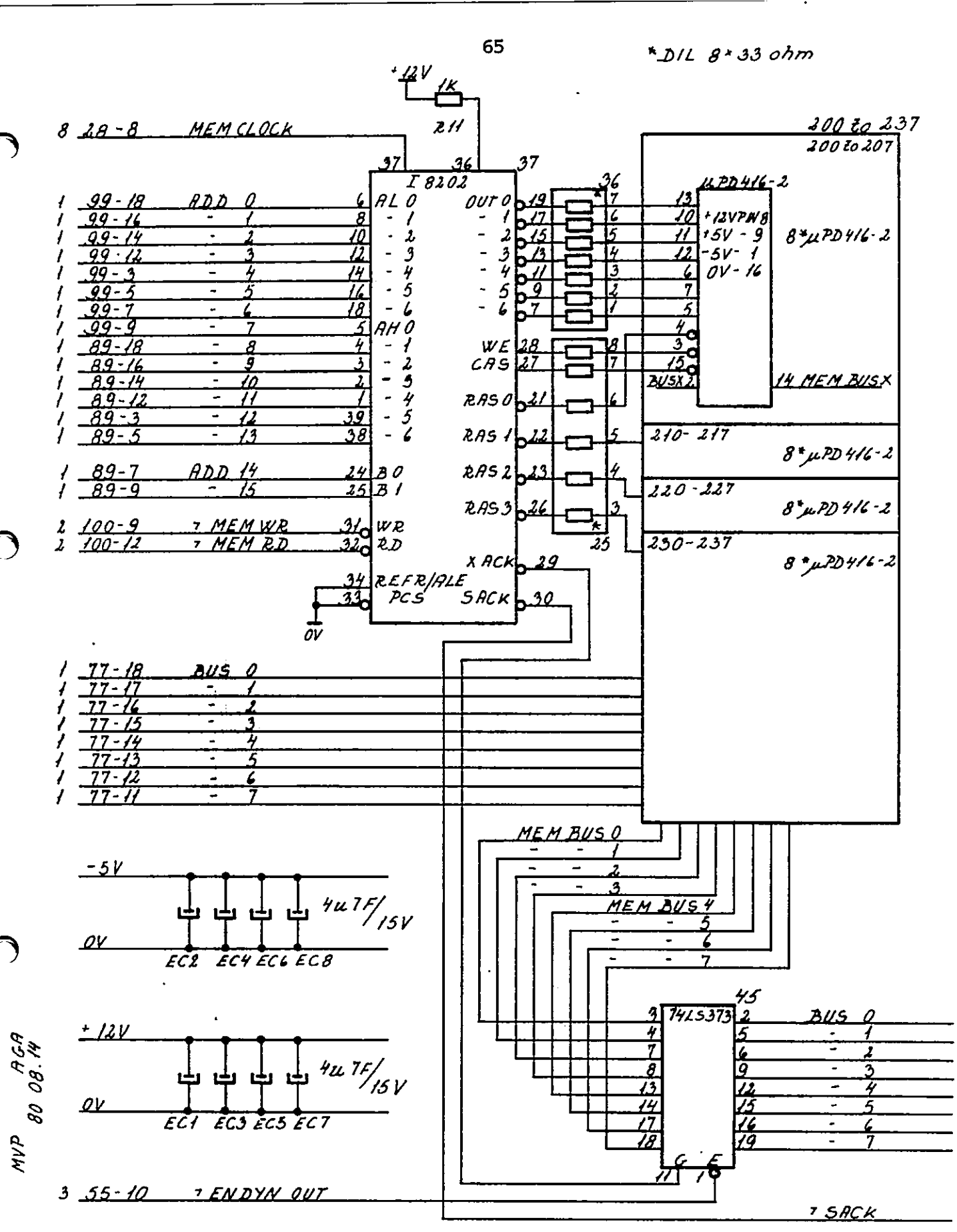
MIC 702
MIC 703

PROM MEMORY & WAIT STATE GENERATION

MIC 04

R 13620

Signal	Destination MIC No.	Description
BUS(0:7)		The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
SACK	4	Output signal from the RAM controller showing that the cycle is finished. (SACK means System Acknowledge).



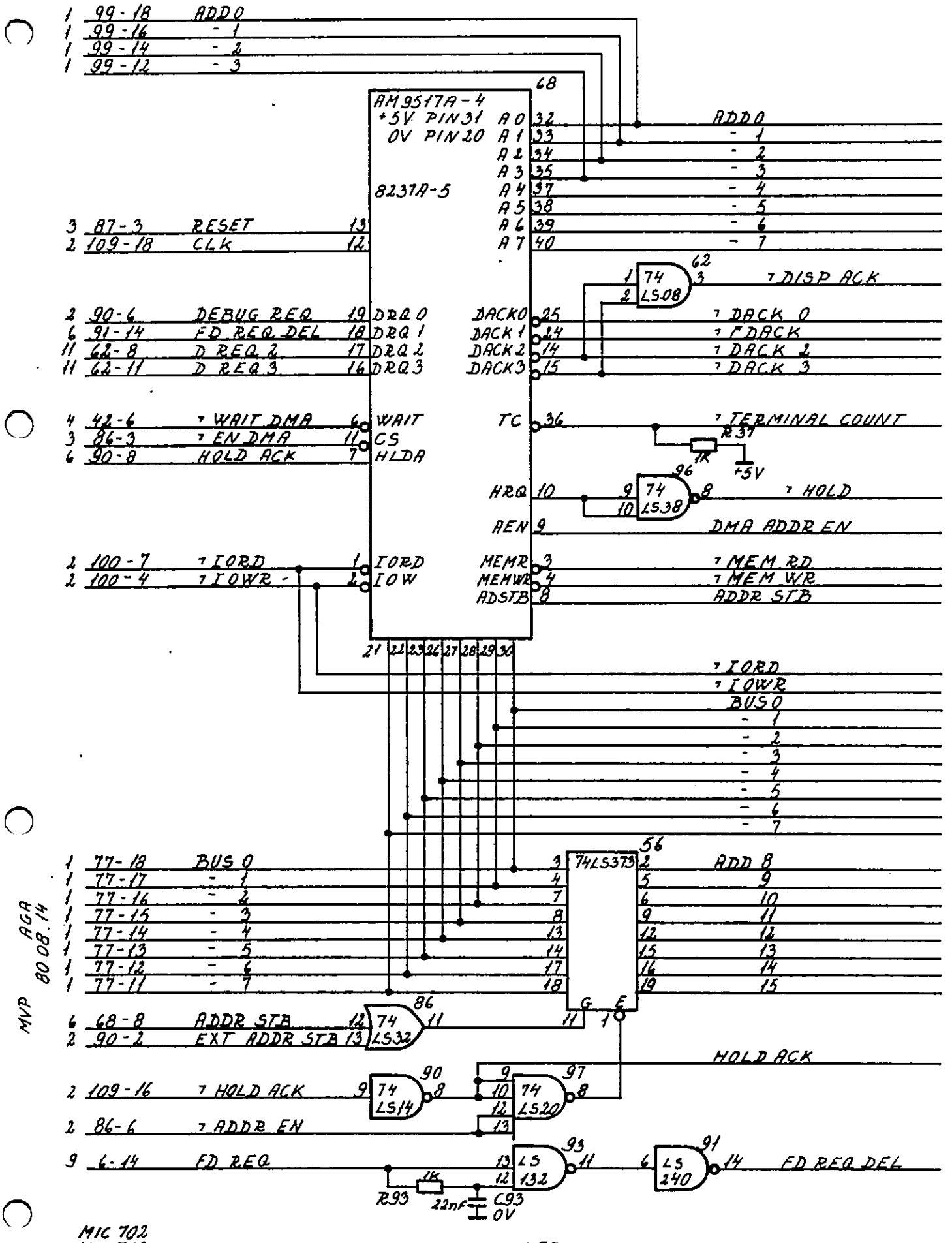
MIC 702
MIC 703

64 K BYTES DYNAMIC RAM ARRAY & TIMING

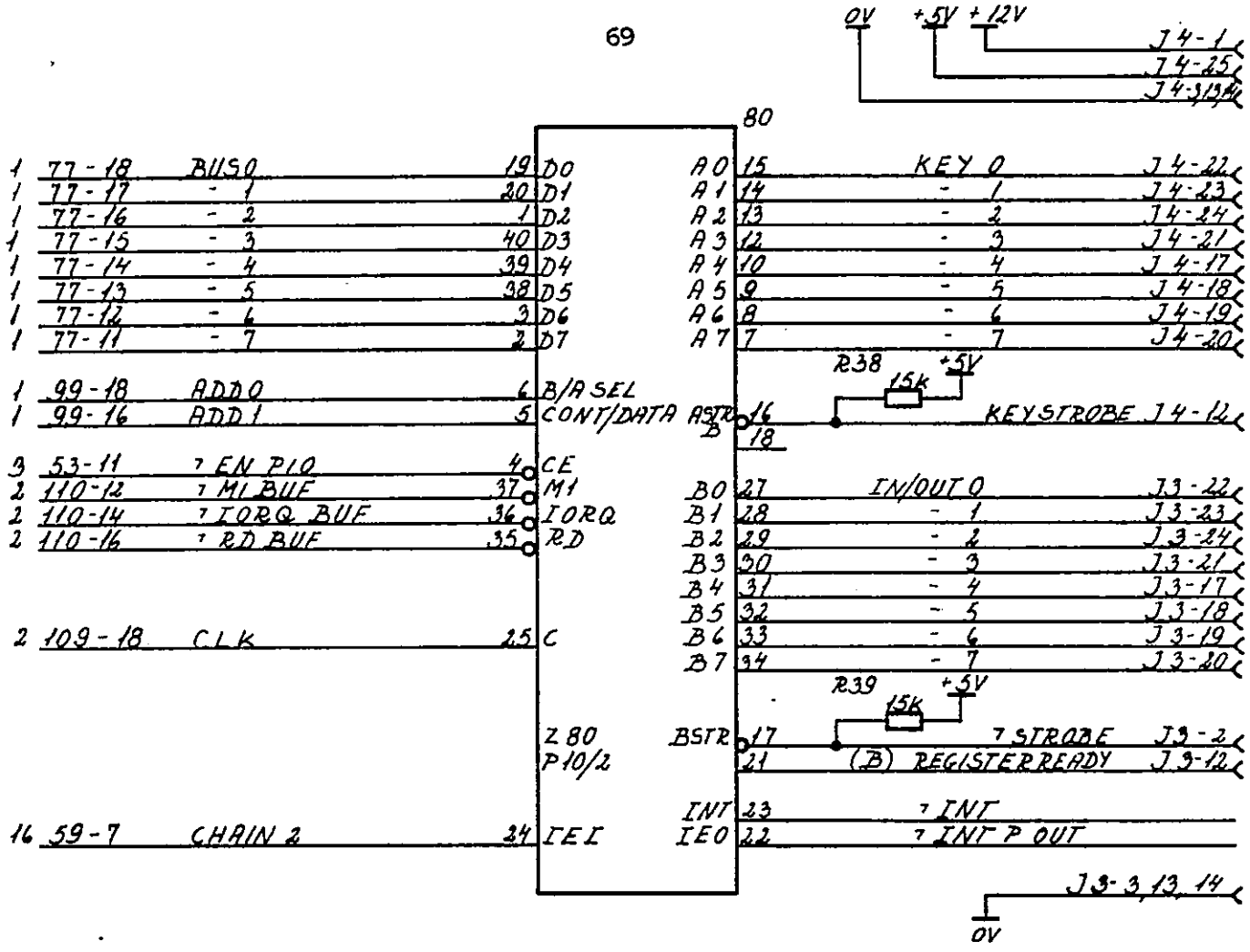
MIC 05

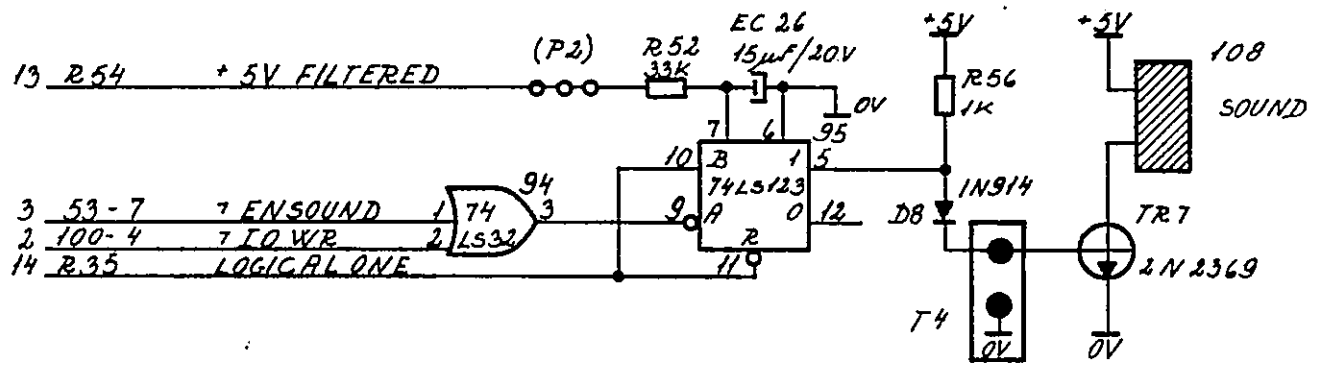
R 13621

Signal	Destination MIC No	Description
ADD(0:7)		Address lines containing the 8 most significant bits. Bit (0:4) is both input to the DMA controller (under programming) and output from the DMA controller (under DMA-cycle).
DACK 0	2	Data acknowledge answer to debug request.
FDACK	9	Floppy data acknowledge, answer to FD req. delay.
DACK 2	11	Data acknowledge answer to DREQ2.
DACK 3		Data acknowledge answer to DREQ3.
DISP ACK	11	Display acknowledge. The display controller uses two channels in the DMA.
TERMINAL COUNT	2, 9, 11	The signal is used to terminate the operation.
HOLD	2	Request to stop the CPU.
DMA ADDR EN	2	Request to gain control over the data and address bus.
MEM RD		Memory read output from the DMA.
MEM WR		Memory write output from the DMA.
ADDR STROBE	6	Address strobe is a pulse to load the address register.
BUS(0:7)		Data bus used to supply information between the CPU and the controllers. Here also used to send address information from the DMA controller to the address register.
HOLD ACK		Hold acknowledge is the replay from the CPU that the bus is idle.
FD REQ DEL		DMA request signal from floppy disk controller.


AM9517A-4
+5V PIN31
0V PIN20
8237A-5
68
A0 32
A1 33
A2 34
A3 35
A4 37
A5 38
A6 39
A7 40
ADD 0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
RESET 13
CLK 12
DEBUG REQ 19 DRQ0
FD REQ DEL 18 DRQ1
D REQ 2 17 DRQ2
D REQ 3 16 DRQ3
DACK0 25 ¬DACK 0
DACK1 24 ¬FDACK
DACK2 14 ¬DACK 2
DACK3 15 ¬DACK 3
62 74 LS08 ¬DISP ACK
¬WAIT DMA 6 WAIT
¬EN DMA 11 CS
HOLD ACK 7 HLDA
TC 36 ¬TERMINAL COUNT
R37 1K +5V
HRQ 10 96 74 LS38 ¬HOLD
AEN 9 DMA ADDR EN
¬IORD 1 IORD
¬IOWR 2 IOW
MEMR 3 ¬MEM RD
MEMWR 4 ¬MEM WR
ADSTB 8 ADDR STB
21 22 23 26 27 28 29 30
¬IORD
¬IOWR
BUS 0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
56 74LS373
BUS 0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
ADD 8 9 10 11 12 13 14 15
G E
ADDR STB 12 86 74 LS32 11
EXT ADDR STB 13
HOLD ACK
90 74 LS14
¬HOLD ACK
97 74 LS20
¬ADDR EN
93 LS 132
FD REQ
R93 1K 22nF C93 0V
91 LS 240
FD REQ DEL
MVP AGA 80.08.14
MIC 702
MIC 703
DMA-CONTROLLER
MIC 06
R 13622

Signal	Destination MIC No.	Description
KEY(0:7)		8-bit parallel input used to receive information from the keyboard.
KEY STROBE		Input strobe from the keyboard.
IN/OUT(0:7)		8-bit parallel input/output used to receive or transmit information to and from an external unit.
STROBE		Input strobe from external unit.
REGISTER READY		Output showing that output from the 8-bit input/output port is ready.
INT	2	Interrupt request.
INT P OUT	2	Interrupt priority out.





MVP 80 08 AGA 14

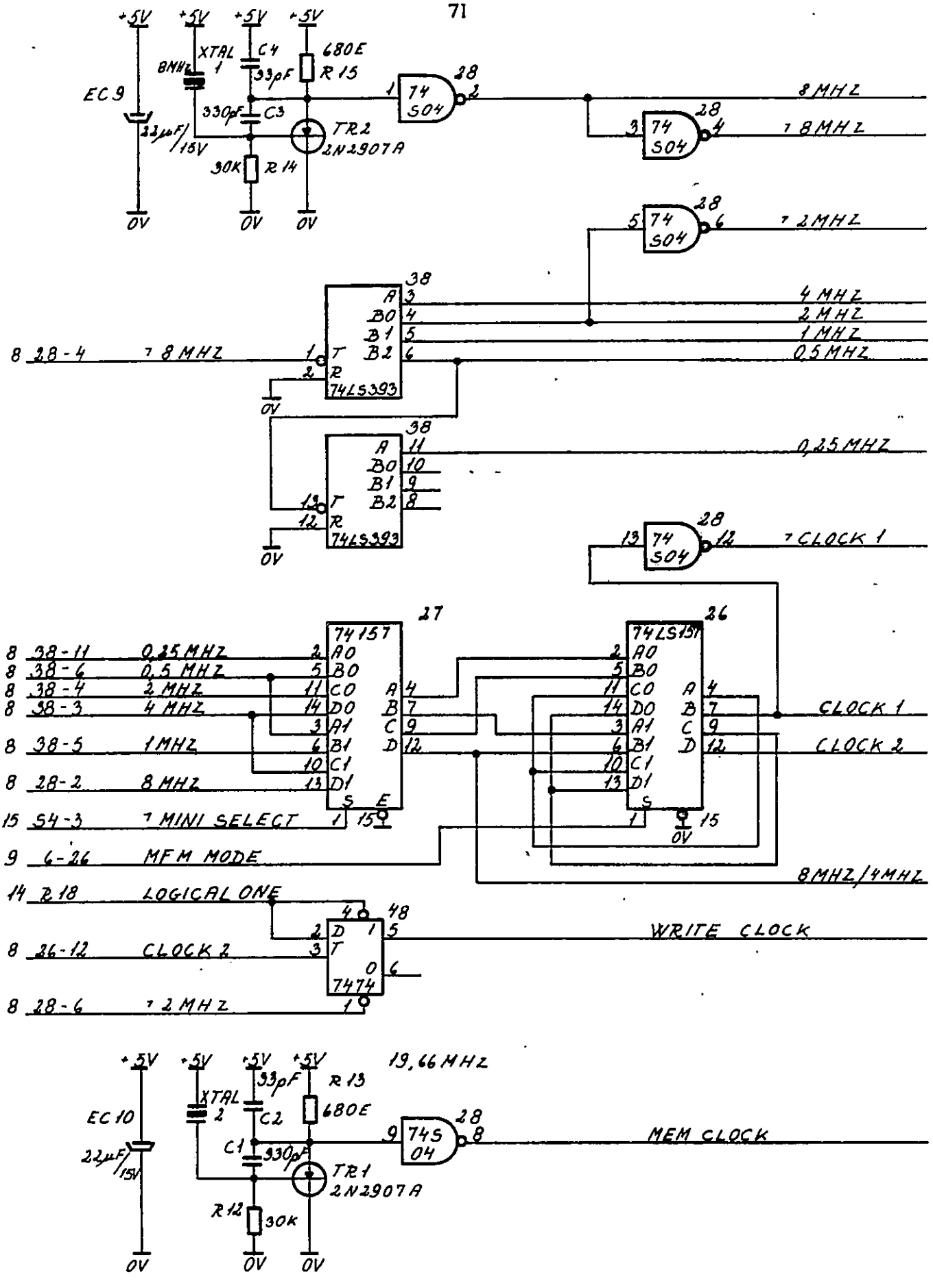
MIC 702
MIC 703

KEYBOARD & PARALLEL IN/OUT

MIC 07

R 13623

Signal	Destination MIC No.	Description
8 MHz	8, 9	Symmetric clock signal of 8 MHz
4 MHz	2, 8	- - - - 4 MHz
2 MHz	8	- - - - 2 MHz
1 MHz	8	- - - - 1 MHz
0.5 MHz	8	- - - - 0.5 MHz
0.25 MHz	8	- - - - 0.25 MHz
CLOCK 1	10	Clock to read logic for the
CLOCK 2	8	floppy controller. Frequency is selected by the controller and by the MINI SELECT switch.
8 MHz/4 MHz	9	Clock to the floppy controller 8 MHz for Maxi floppy and 4 MHz for Mini floppy drive.
WRITE CLOCK	9	Clock input to floppy controller. The frequency is selected by the controller and by the MINI SELECT switch.
MEM CLOCK	5, 15	Clock to the memory controller. The frequency is 19.66 MHz.



MVP AGA-80.08.14

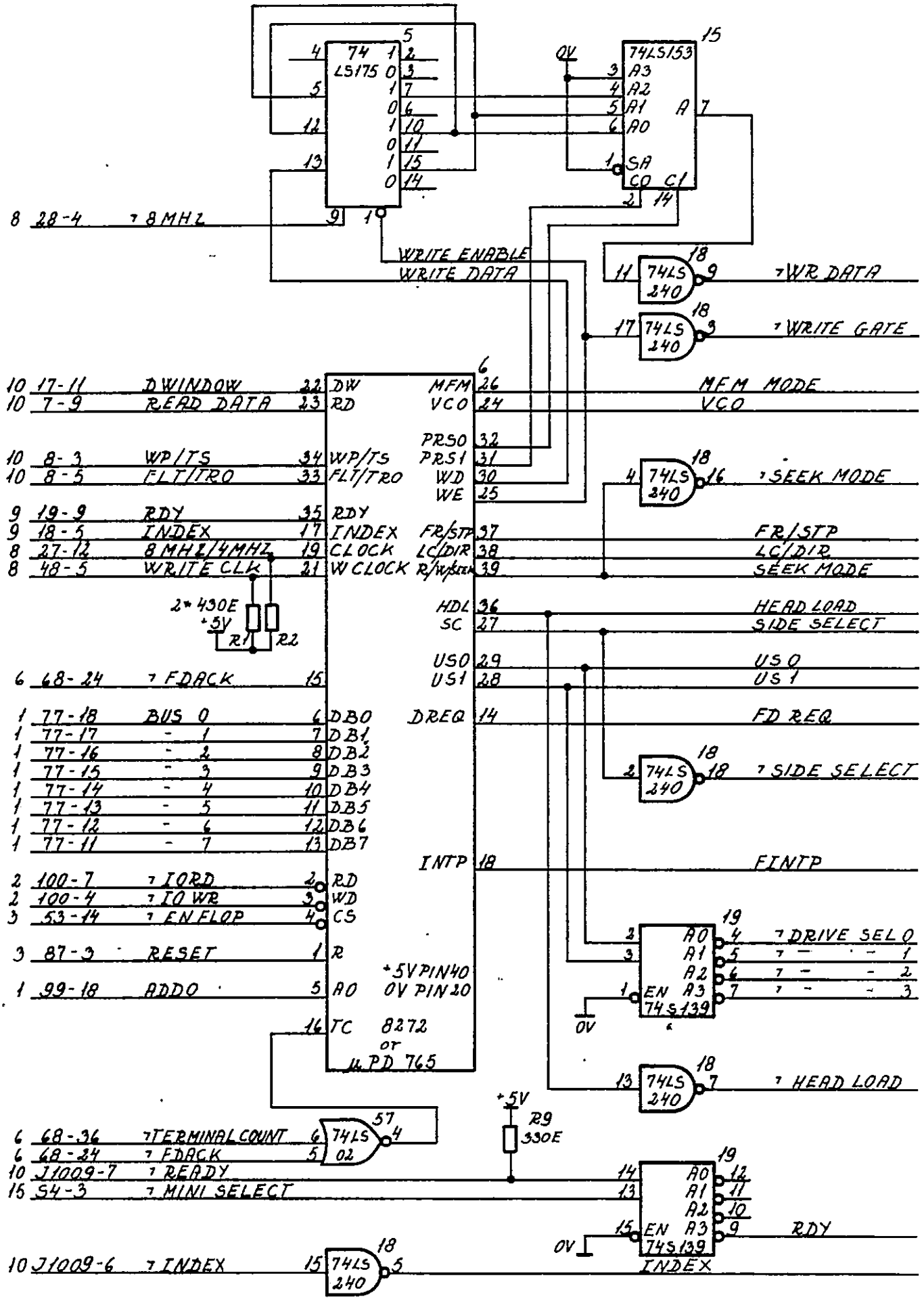
MIC 702
MIC 703

CLOCK SYSTEM

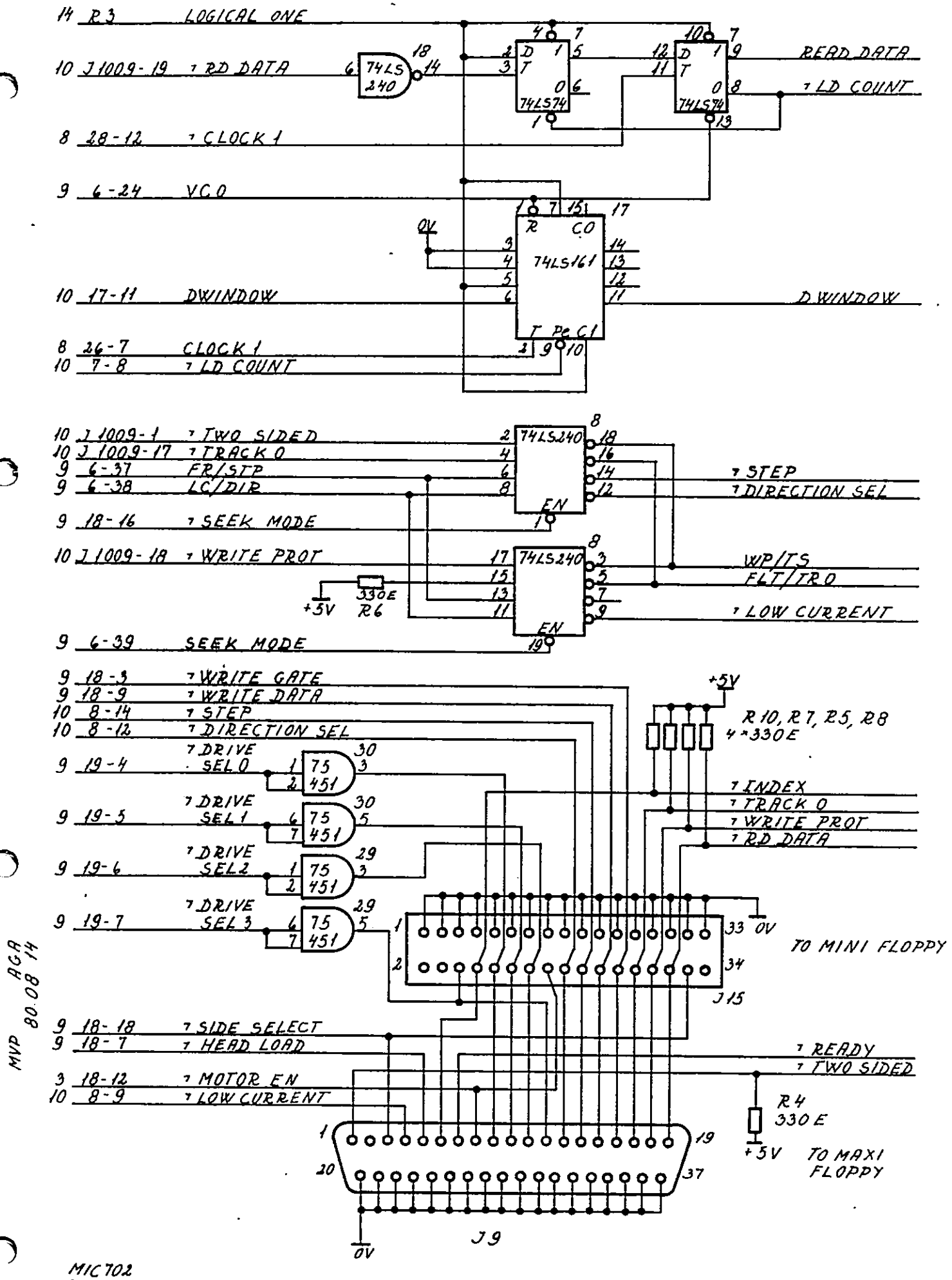
MIC 08

R13624

Signal	Destination MIC No.	Description
WR DATA	10	WRITE DATA to the floppy disk drive. Valid when WRITE GATE is on.
WRITE GATE	10	Control signal to floppy disk drive. Informs that now the WR DATA is valid.
MFM MODE	8	MFM mode is dual density, FM mode is single density.
VCO	10	Signal to control the voltage controlled oscillator.
SEEK MODE	10	Sets the selectors in seek mode.
FR/STP	10	Control signal; Fault Reset/ Step
LC/DIR	10	Control signal; Low Current/ Direction
HEAD LOAD	10	Control signal; Head Load
SIDE SELECT	10	Control signal; Side Select
US0, US1		Unit select decoded to:
DRIVE SEL 0	10	Drive Select 0
DRIVE SEL 1	10	Drive Select 1
DRIVE SEL 2	10	Drive Select 2
DRIVE SEL 3	10	Drive Select 3.
FD REQ	6	DMA reguest from floppy controller.
F INTP	15	Floppy controller interrupt request.
RDY	9	Ready from floppy controller. Note that Mini floppy is always ready.
INDEX	9	Index mark from floppy disk drive.


74LS175
74LS153
74LS240
74LS139
74LS02
8272
or
μPD 765
8 28-4 ↗8MHZ
WRITE ENABLE
WRITE DATA
↗WR DATA
↗WRITE GATE
10 17-11 DWINDOW
10 7-9 READ DATA
MFM MODE
VCO
10 8-3 WP/TS
10 8-5 FLT/TRO
↗SEEK MODE
9 19-9 RDY
9 18-5 INDEX
8 27-12 8MHZ/4MHZ
8 48-5 WRITE CLK
2*430E
+5V
R1
R2
FR/STP
LC/DIR
SEEK MODE
HDL
SC
HEAD LOAD
SIDE SELECT
USO
US1
6 68-24 ↗FDACK
FD REQ
1 77-18 BUS 0
1 77-17 - 1
1 77-16 - 2
1 77-15 - 3
1 77-14 - 4
1 77-13 - 5
1 77-12 - 6
1 77-11 - 7
↗SIDE SELECT
INTP
FINTP
2 100-7 ↗IORD
2 100-4 ↗IO WR
3 53-14 ↗ENFLOP
3 87-3 RESET
1 99-18 ADDO
+5V PIN40
0V PIN20
↗DRIVE SEL 0
↗HEAD LOAD
6 68-36 ↗TERMINAL COUNT
6 68-24 ↗FDACK
10 J1009-7 ↗READY
15 S4-3 ↗MINI SELECT
R9
330E
RDY
10 J1009-6 ↗INDEX
INDEX
MIC 702
MIC 703
FLOPPY DISK CONTROLLER
MIC 09
R 13625
MVP
AGA
80.08.14

Signal	Destination MIC No.	Description
READ DATA	9	Read data from the floppy, synchronized with the VCO to separate phase bits and data bits.
LD COUNT	10	Load counter is used to synchronize the window counter.
D WINDOW	9, 10	Data Window is used by the controller to separate data bits from phase bits.
STEP	10	Output pulse to make the floppy head move from one cylinder to the next.
DIRECTION SEL	10	Direction select is used together with the STEP pulse. A low signal and the head moves towards the counter of the disc.
WP/TS	9	Write Protect/Two Sided signal from the floppy disk drive.
FLT/TRO	9	Fault/Track 0 signal from floppy disk drive.
LOW CURRENT	10	Output signal to Maxi floppy disc drive. Used to decrease the write current when close to the center of the disk.
INDEX	9	Index mark signal from the floppy.
TRACK 0	10	Track 0 signal from the floppy.
WRITE PROT	10	The diskette used is writeprotected.
RD DATA	10	Read data supplied from the floppy disk drive including data and phase bits.
READY	9	Ready signal from the Maxi floppy drive.
TWO SIDED	10	The Maxi floppy is a two sided version.



MVP 80.08 AGA

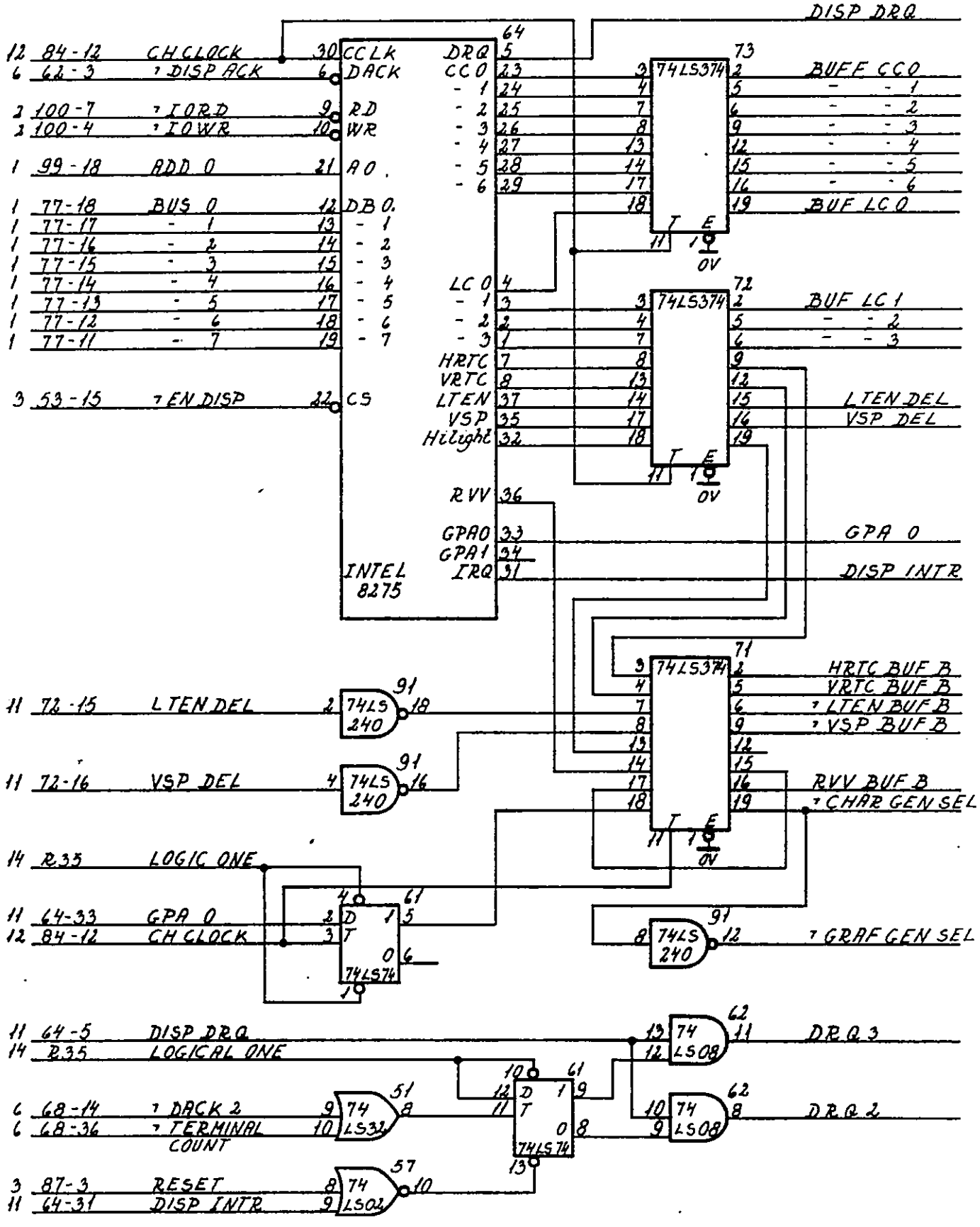
MIC 702
MIC 703

FLOPPY DISK READ & SELECT CIRCUIT

MIC 10

R 13626

Signal	Destination MIC No.	Description
DSP DRQ	11	DMA request from the display controller.
BUFF CC(0:6)	12	Output from the display controller containing the address of the character to be written on the display.
BUFF LC(0:3)	12	Output from the display controller containing the line number written on the display.
LTEN DEL	11	Light enable from the display.
VSP DEL	11	Video suppression. This output signal is used to blank the video to the display.
GPA 0	11	Control signal used to select semigraphic PROM.
DISP INTR	11, 15	Display interrupt request.
HRTC BUF B	13	Horizontal retrace signal.
VRTC BUF B	13	Vertical retrace signal.
LTEN BUF B	13, 14	LTEN DEL delayed one CHAR CLOCK
VSP BUF B	13	VSP DEL delayed one CHAR CLOCK
RVV BUF B	13	REVERSE VIDEO. This output is used to reverse the video signal to the display.
CHAR GEN SEL	12	This signal selects the standard character generator.
GRAF GEN SEL	12	This signal selects the semigraphic character generator.
DRQ3 and DRQ2	6	The display controller uses two channels out of the DMA>s four channels. This is done to make the roll function of the display. DRQ2 and DRQ3 are the two data request signals.



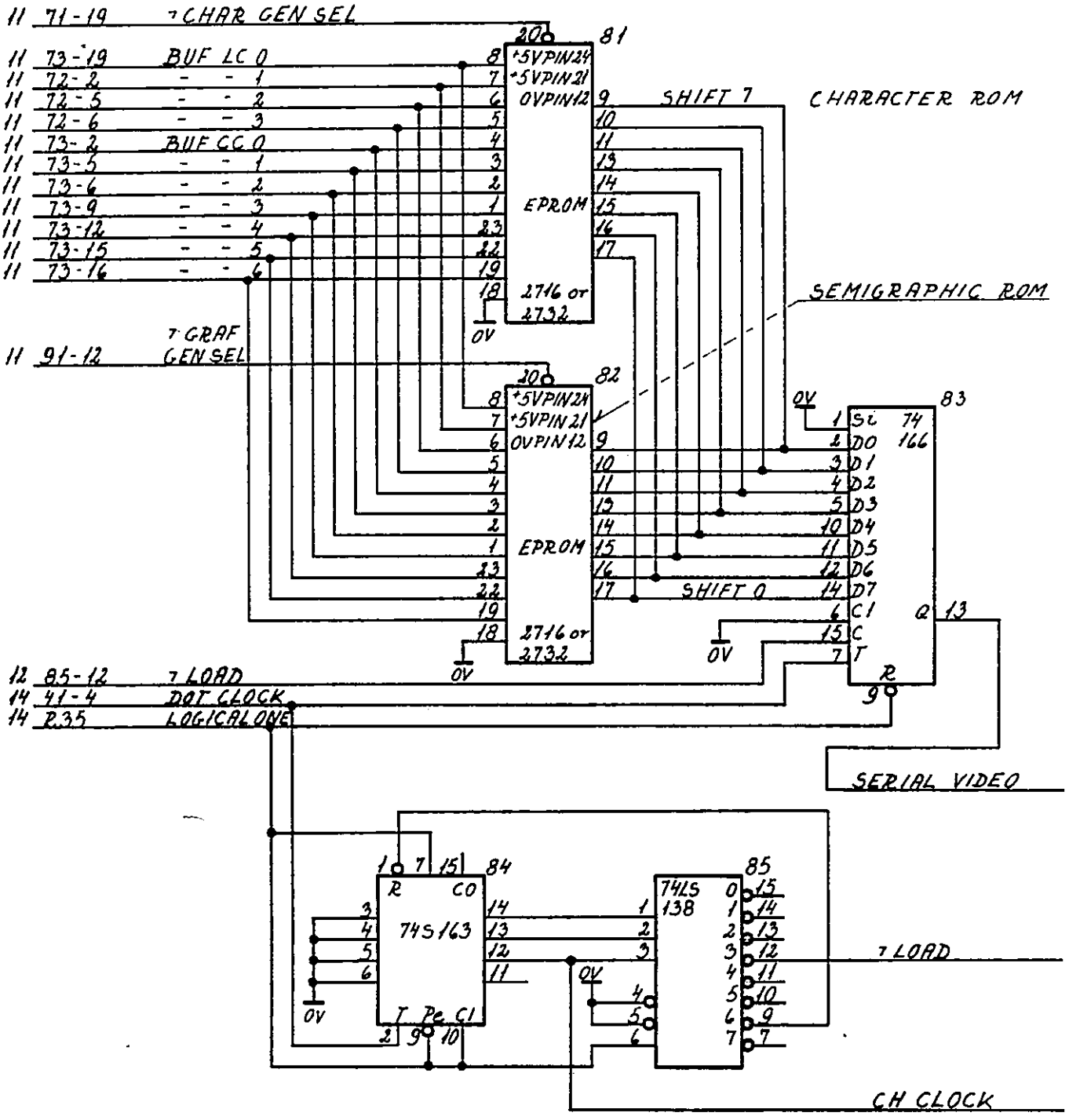
MIC 702
MIC 703

VIDIO DISPLAY CONTROLLER

MIC 11

213627

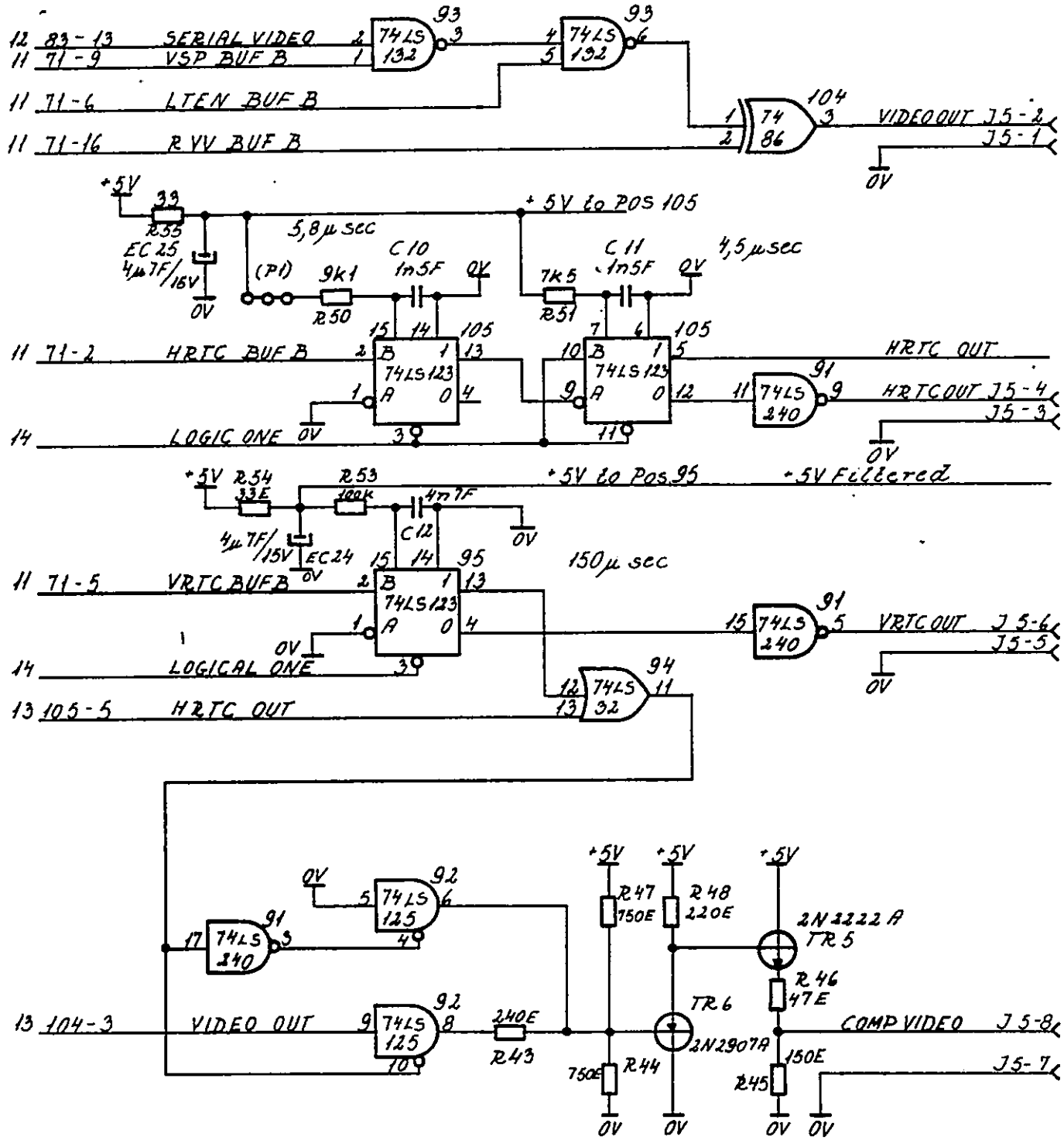
Signal	Destination MIC No.	Description
SERIAL VIDEO	13	The video output from the shift register.
LOAD	12	Signal to load the output from the character ROM or the semigraphic ROM into the shift register.
CH CLOCK	11	Character clock. The period time of this clock is 7 times the DOT CLOCK time. 7 x 86 nsec. = 0.601 usec.



MIC 702
MIC 703 CHARACTER GENERATOR, VIDIO SHIFT REGISTER & DOT COUNTER MIC 12

R 13628

Signal	Destination MIC No.	Description
VIDEO OUT	13	Video out signal. *)
HRTC OUT	13	Horizontal output pulse. *)
VRTC OUT		Vertical output pulse. *)
		*) These three signals are ready to be used if a video monitor without decoding for comp. video is used. RC702 uses comp. video signals.
COMP VIDEO		Compressed video is the signal containing both video horizontal sync. and vertical sync.
+5 V filtered	7	+5 V supply after an RC filter.



MVP 80.08.14 AGA

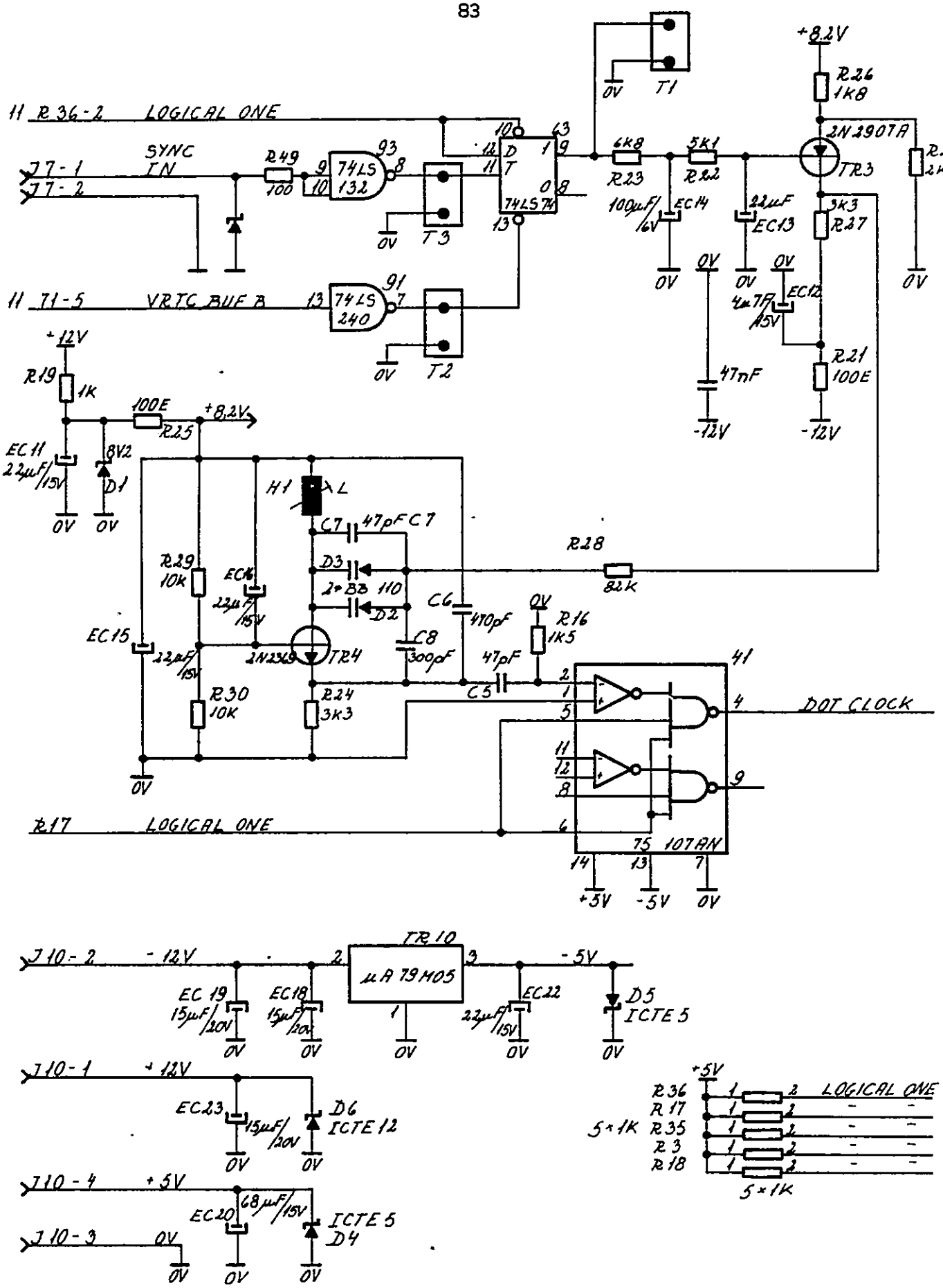
MIC 702
MIC 703

VIDEO GENERATOR

MIC 13

R13 C29

Signal	Destination MIC No.	Description
DOT CLOCK	12	The dot clock is an 11.64 MHz clock which is synchronized with the main frequency.
SYNC IN		The input is a 50 Hz signal from the REC701 rectifier unit.
T1		Testpoint 1. The signal here is a 50 Hz signal and the coil H1 is adjusted until the dutycycle of this signal is 50%.
-5 V		The -5 V is used by the dynamic RAM.



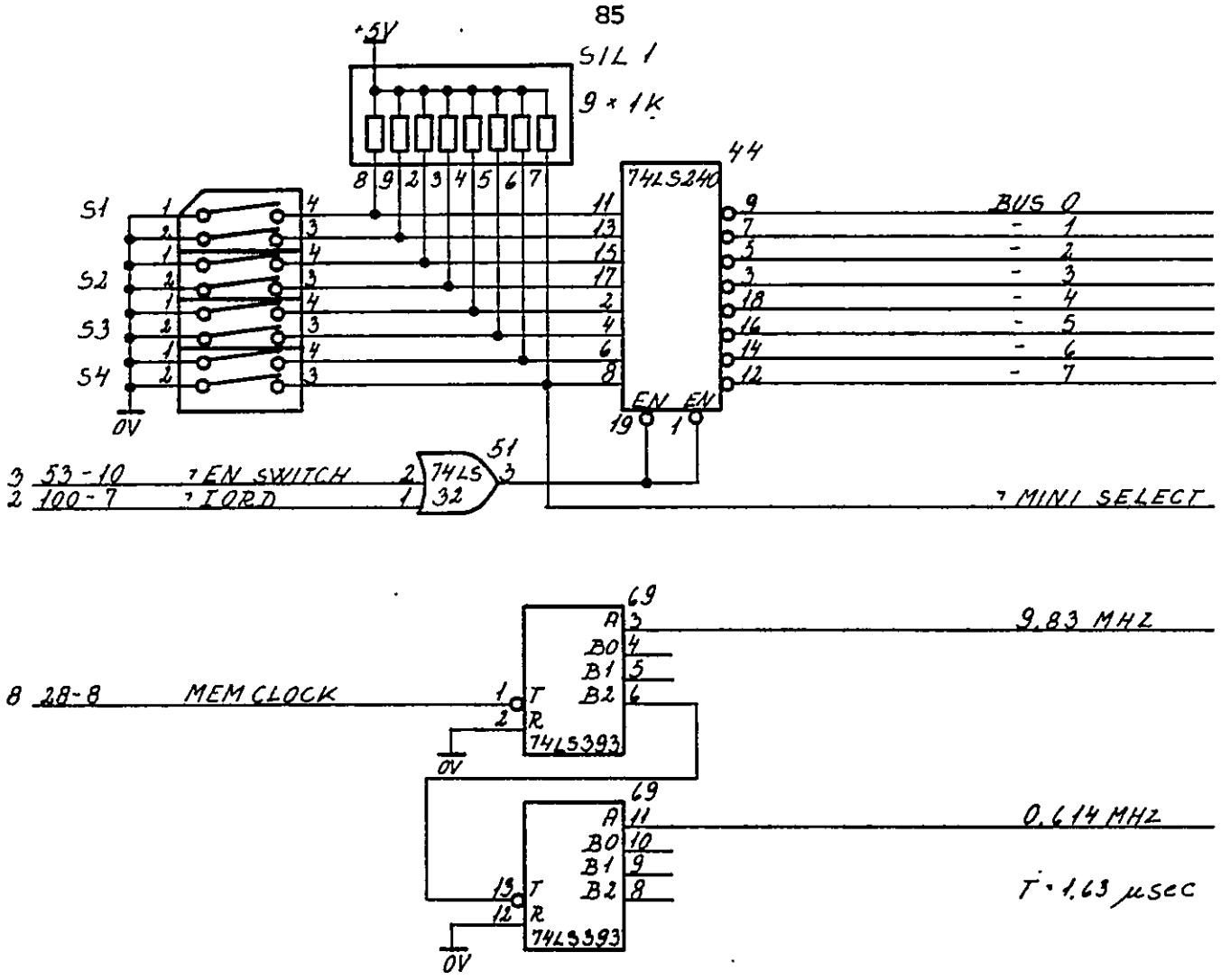
MIC 702
MIC 703

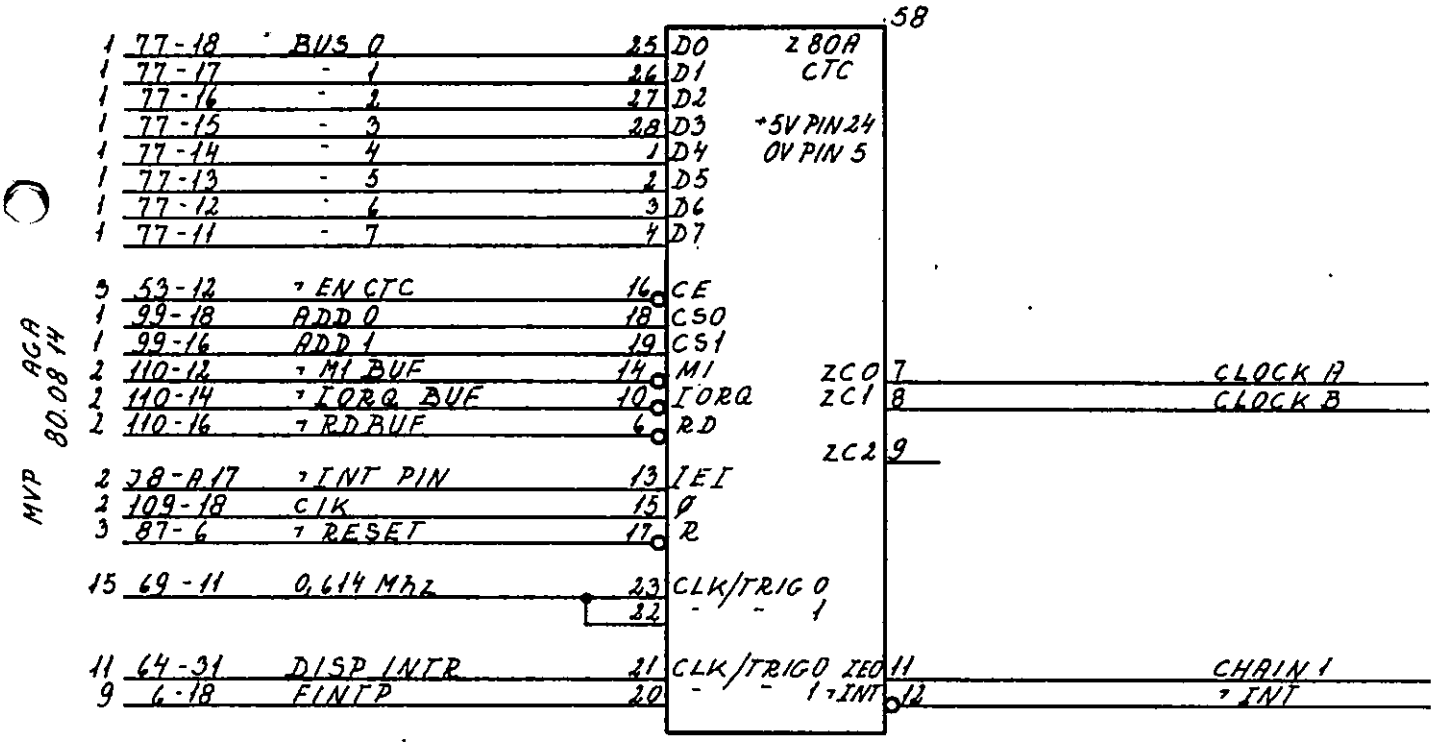
PHASE LOCK LOOP

MIC 14

R 13 C 30

Signal	Destination MIC No.	Description
BUS(0:7)	1	The data bus is the TRI-state bus supplying data information between the CPU and all of the controllers.
MINI SELECT	8, 9	Control signal selects Mini floppy disk drives. The signal is supplied to the clock generator and divides the clock signals to the floppy controller by two.
9.63 MHz	2	Clock of 9.63 MHz is not used on the board but supplied to the output plug J8.
0.614 MHZ	15	Clock of 0.614 MHz is used as input to the counter timer controller to be counted down to make the clock signal to the two Serial In/Out Channels.
CLOCK A CLOCK B	16 16	Clock signal to the two Serial In/Out Channels just mentioned.
CHAIN 1	16	Interrupt priority chain
INT		Interrupt from the counter timer controller.



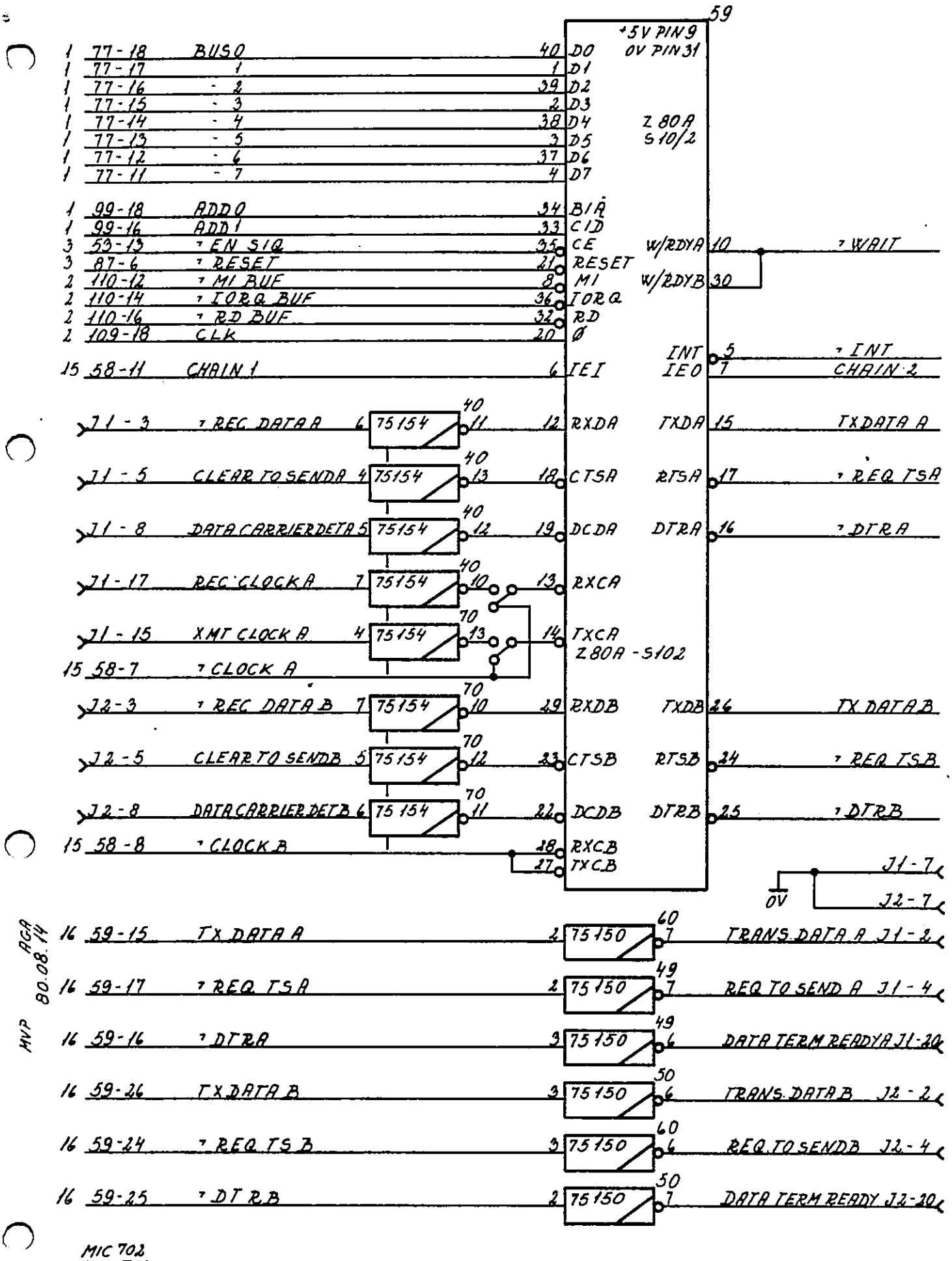


MIC 702
MIC 703

SWITCH INPUT TO PROGRAM & BAUD RATE GENERATOR MIC 15

2 13 631

Signal	Destination MIC No.	Description
WAIT	4	This open collector output from the SIO is connected to the WAIT signal generated on page 04 and slows the CPU down to wait for the SIO.
INT	2	Interrupt request from the SIO/2.
CHAIN	2	Interrupt priority chain out from the SIO/2.
V.24 input outputs		Pin 2 TRANS DATA - 3 REC DATA - 4 REQ TO SEND - 5 CLEAR TO SEND - 7 Ground - 8 DATA CARRIER DETECT - 20 DATA TERM READY J1 to channel A (Terminal) J2 to channel B (Printer)



MVP PGA 80.08.14

MIC 702
MIC 703

SERIAL INPUT OUTPUT

MIC 16

R13632

2.4.2 FCO 19-008 Diagrams

The FCO 19-008 is based on the DSP701 - Data Separator Print board; fig. 32 shows the layout.

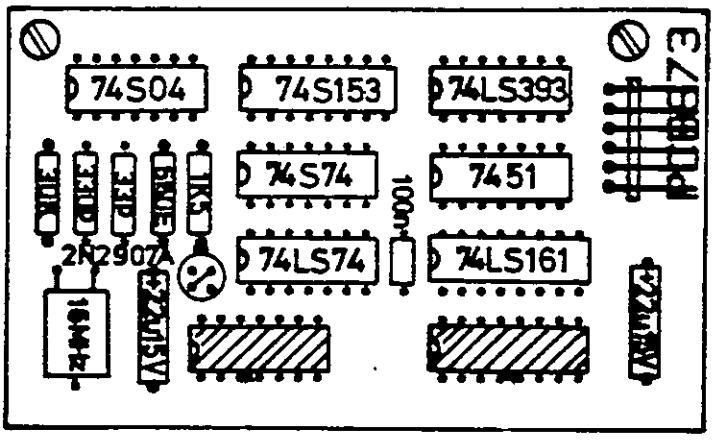


Figure 32: DSP701 - Data Separator Print; layout; FCO 19-008 item.

Implementing the FCO 19-008 on the MIC702/MIC703 board requires that the IC's in pos 17 and 7 are replaced by the DSP701.

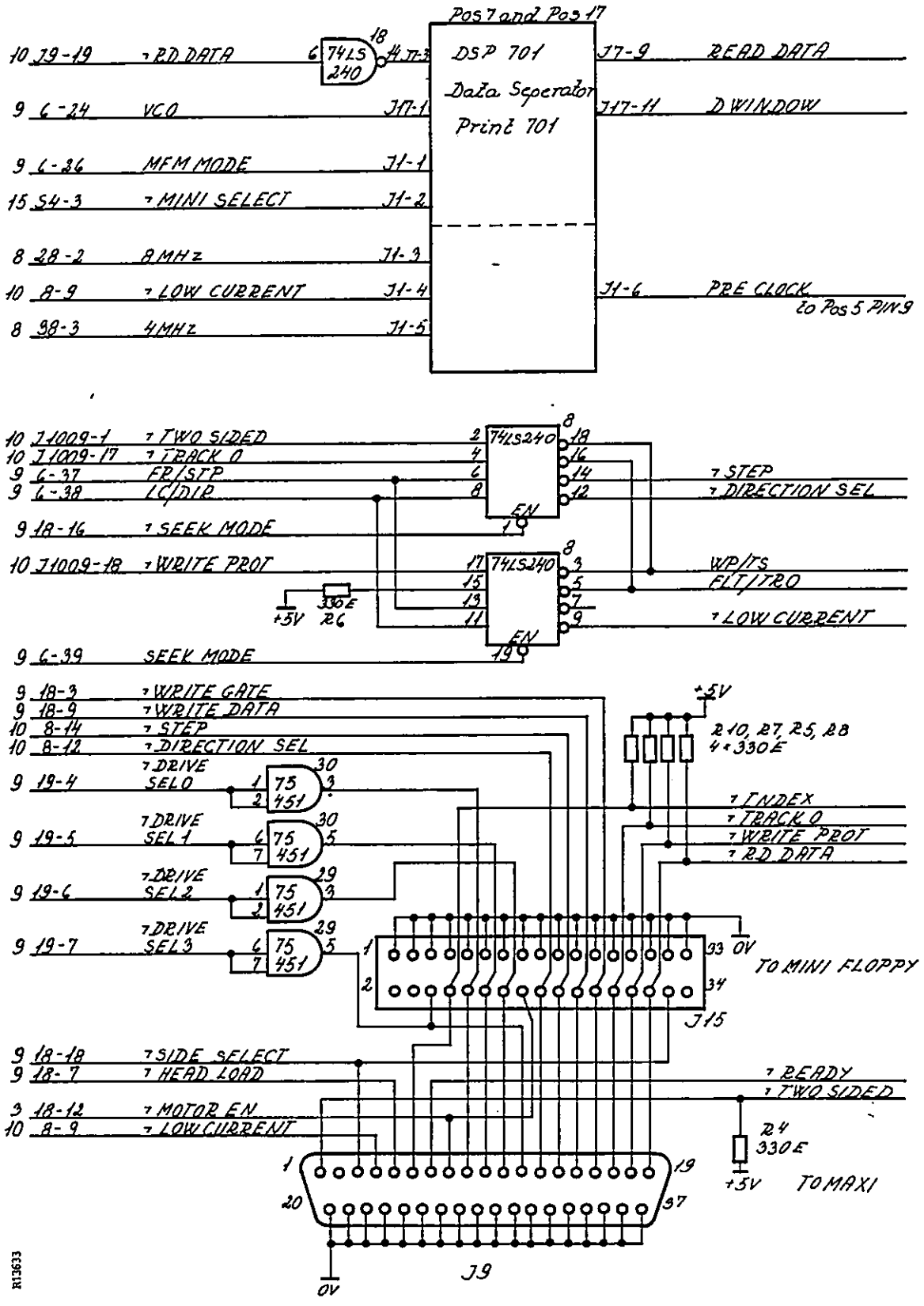


Figure 33: MIC702/MIC703; installation of DSP701 (diagram normally MIC10).

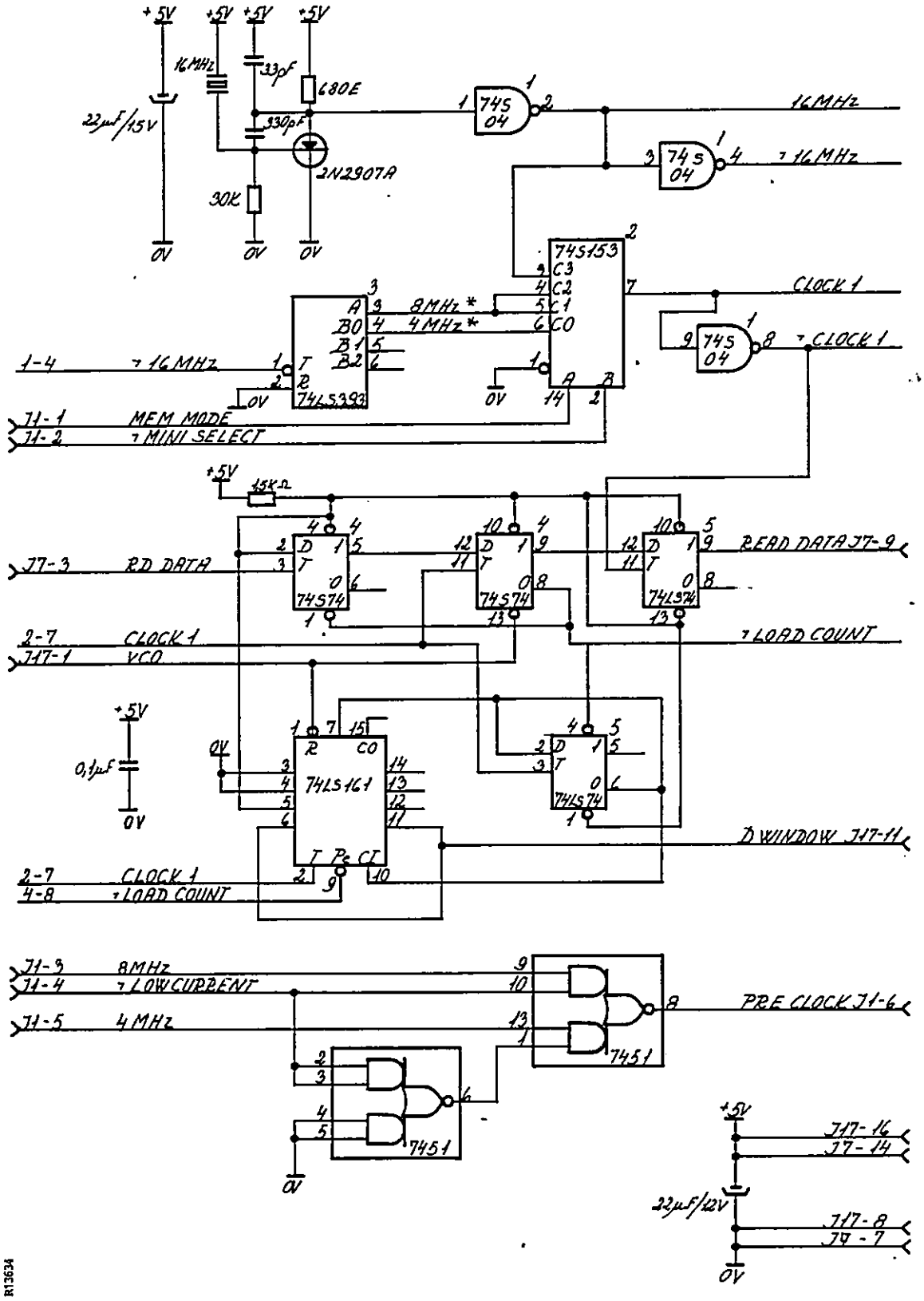
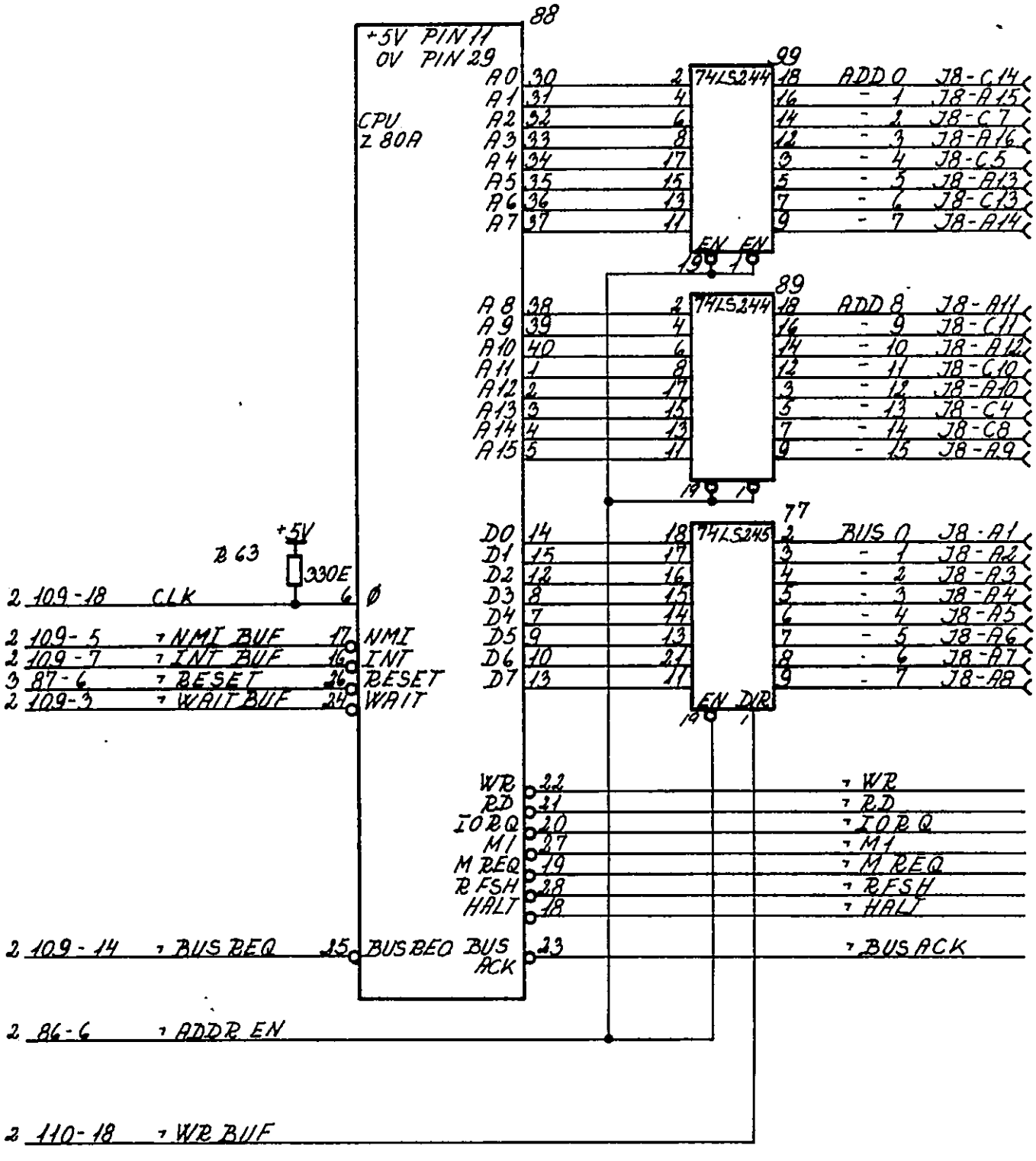


Figure 34: DSP701; schematic diagram.

2.4.3 MIC704/MIC705

Signal	Destination MIC No.	Description
ADD(0:15)	3, 4, 5, 6, 7, 9, 11, 15, 16	The address bus is the TRI-state bus supplying address information to all the controllers.
BUS(0:7)	3, 5, 6, 7, 9	The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
WR	2	WRITE output from the CPU.
RD	2	READ - - - -
IORQ	2	INPUT OUTPUT REQUEST, when active the WR or RD pulse is addressing a controller and not the memory.
MI	2	MACHINE CYCLE ONE, indicates the op code fetch cycle of the CPU.
MREQ	2	MEMORY REQUEST, indicates a read or write memory cycle.
RFSH	2	REFRESH, indicates a refresh cycle by the CPU, the signal is not used in MIC704.
HALT		HALT indicates that the CPU is executing a halt instruction. An error situation.
BUS ACK	2	BUS ACKNOWLEDGE, the CPU has received a BUS REQ and lets the DMA use the BUS.
BUS EN	1	BUS ENABLE for the CPU.



MIC 704
MIC 705

MICROPROCESSOR CPU AND ADDR/DATA REGISTERS

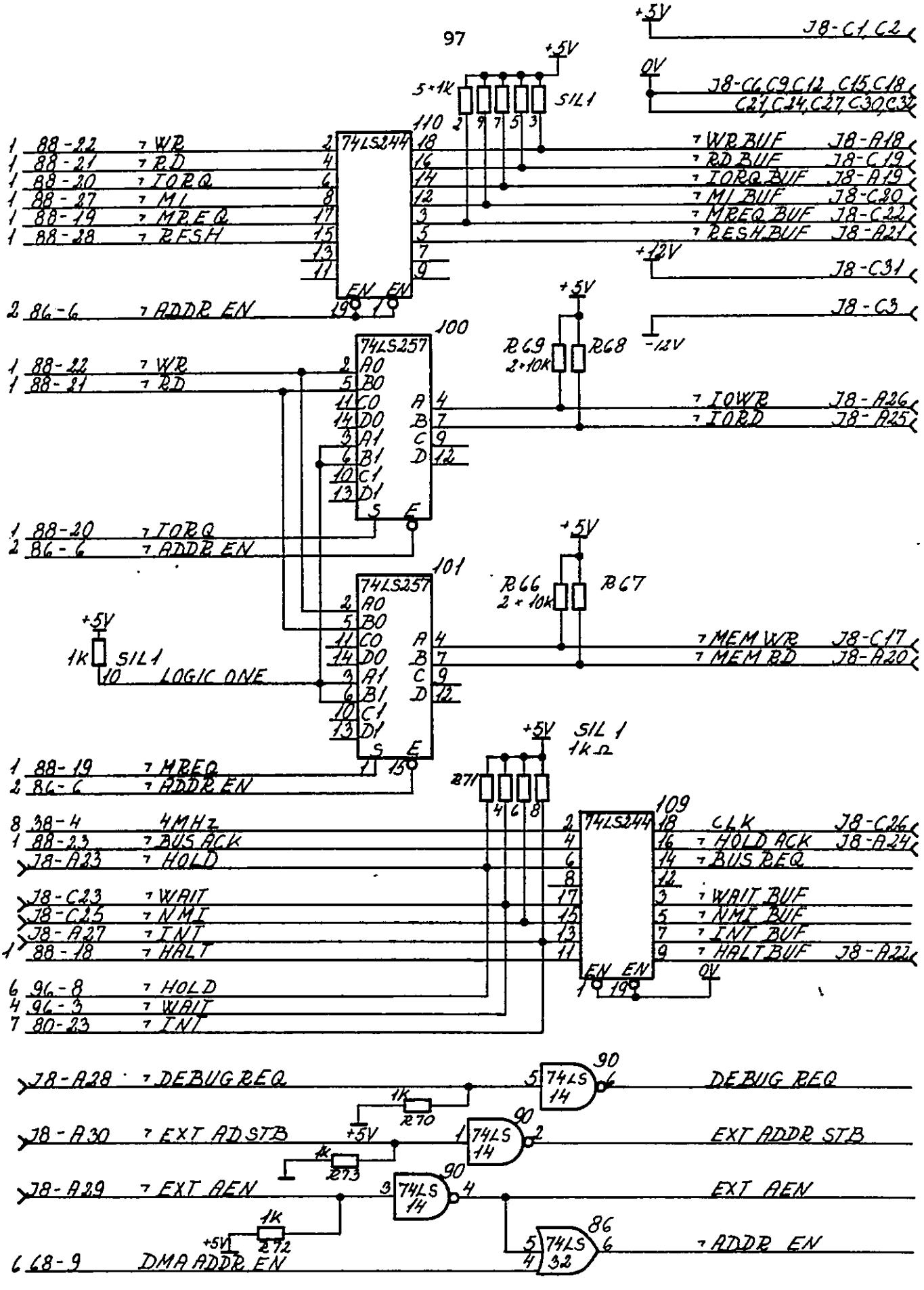
MIC 1

R 13635

Signal	Destination MIC No.	Description
WR BUF	1	* WRITE output pulse from the CPU
RD BUF	1, 7, 15, 16	* READ - - - - -
IORQ BUF	1, 7, 15, 16	* IORQ - - - - -
M1 BUF	7, 15, 16	* M1 - - - - -
M REQ BUF	4	* M REQ - - - - -
RFSH BUF		* RFSH - - - - -
IOWR	3, 6, 7, 9	** INPUT/OUTPUT WRITE, write pulse to controllers which are not of the Zilog type.
IORD	6, 9, 11, 15	** INPUT/OUTPUT READ, read pulse to controllers which are not of the Zilog type.
MEM WR	4, 5	** MEMORY WRITE pulse.
MEM RD	3, 4, 5	** MEMORY READ pulse.
CLK	1, 4, 6, 7, 15, 16	4 MHz symmetric clock to the system.
HOLD ACK	1, 6	BUS ACK signal through a buffer.
BUS REQ	1	The DMA controller or the tester demand control over the BUS.
WAIT BUF	1	This signal inserts at least one wait state in each CPU cycle.
NMI BUF	1	NON MASKABLE INTERRUPT, only used by a tester.
INT BUF	1	INTERRUPT REQUEST to CPU.
HALT BUF		HALT signal through a buffer.
DEBUG REQ	6	DMA REQUEST from a tester.
EXT ADDR STB	6	DMA REQUEST signal from a tester.
EXT AEN		- - - - - -
ADDR EN	1, 2, 3, 4, 6	ADDRESS ENABLE when active the CPU controls the BUS system.
INT PIN	15	INT PIN may be used by a unit connected to J8 and is interrupt priority in.

* signal is only active, when ADDR EN is active.

** Signal may also be active when ADDR EN is active. The DMA also uses these signals, which are of the TRI-state type.



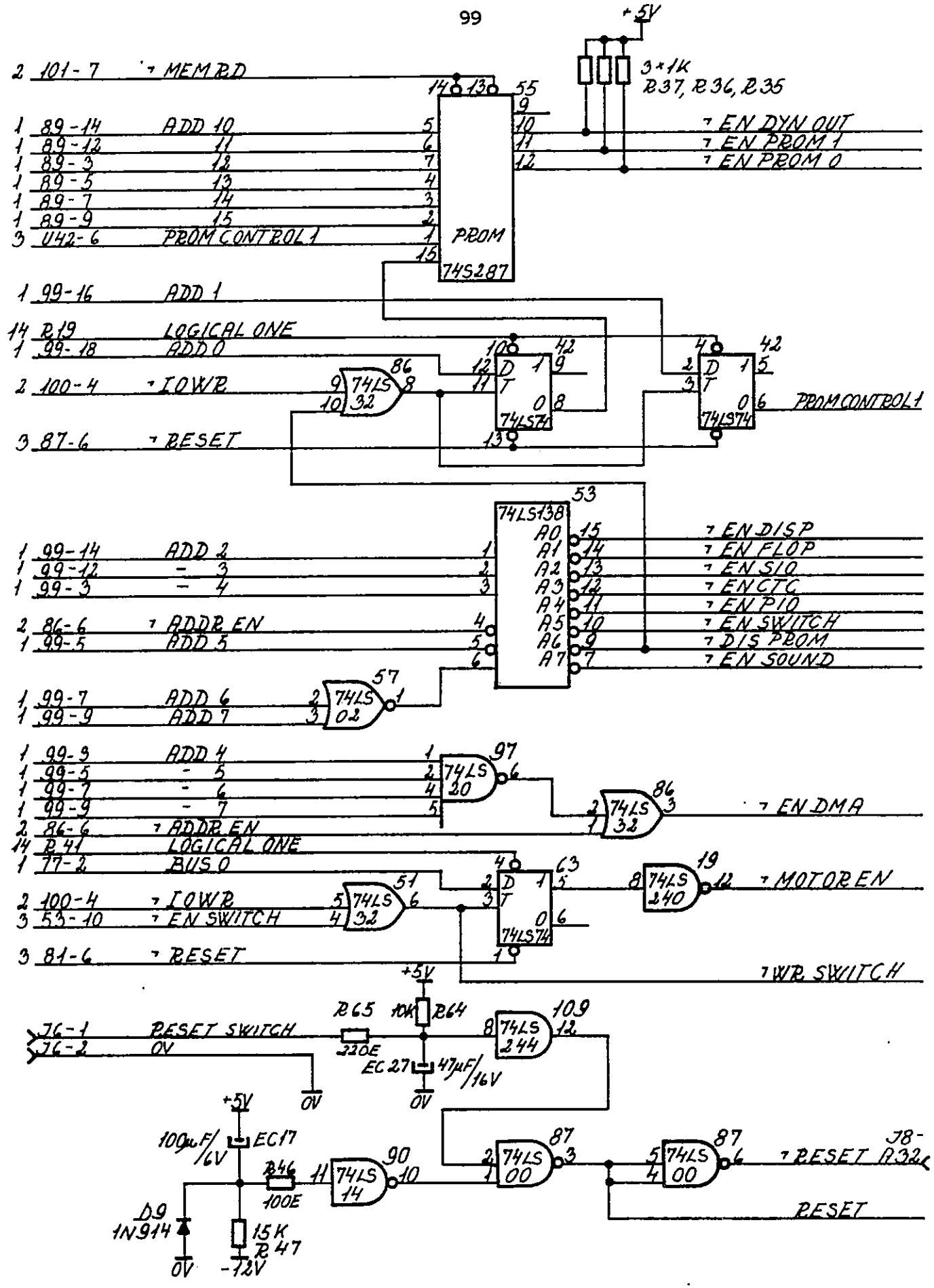
MIC 704
MIC 705

R13636

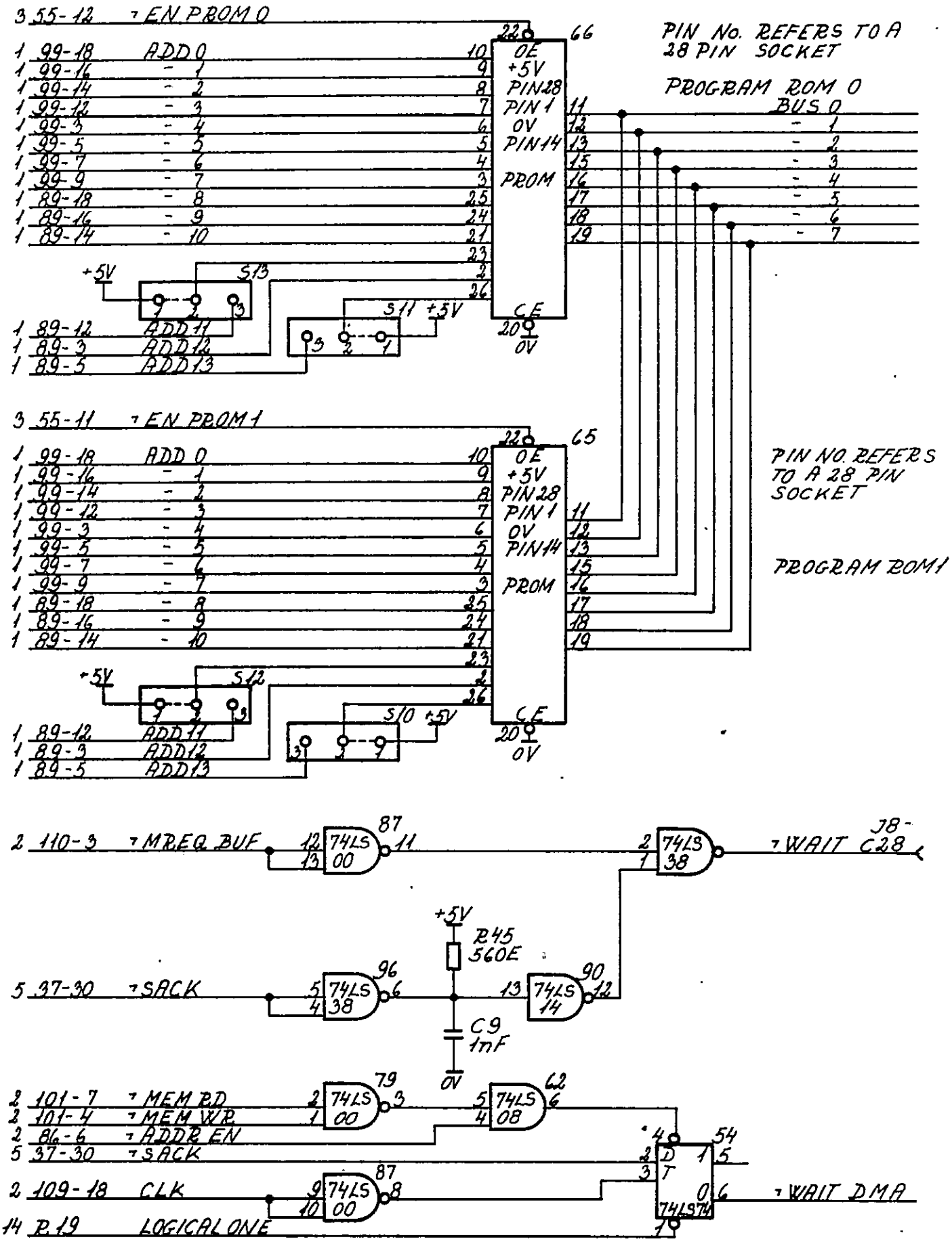
CONTROL SIGNALS RECEIVERS AND TRANSMITTERS

MIC 2

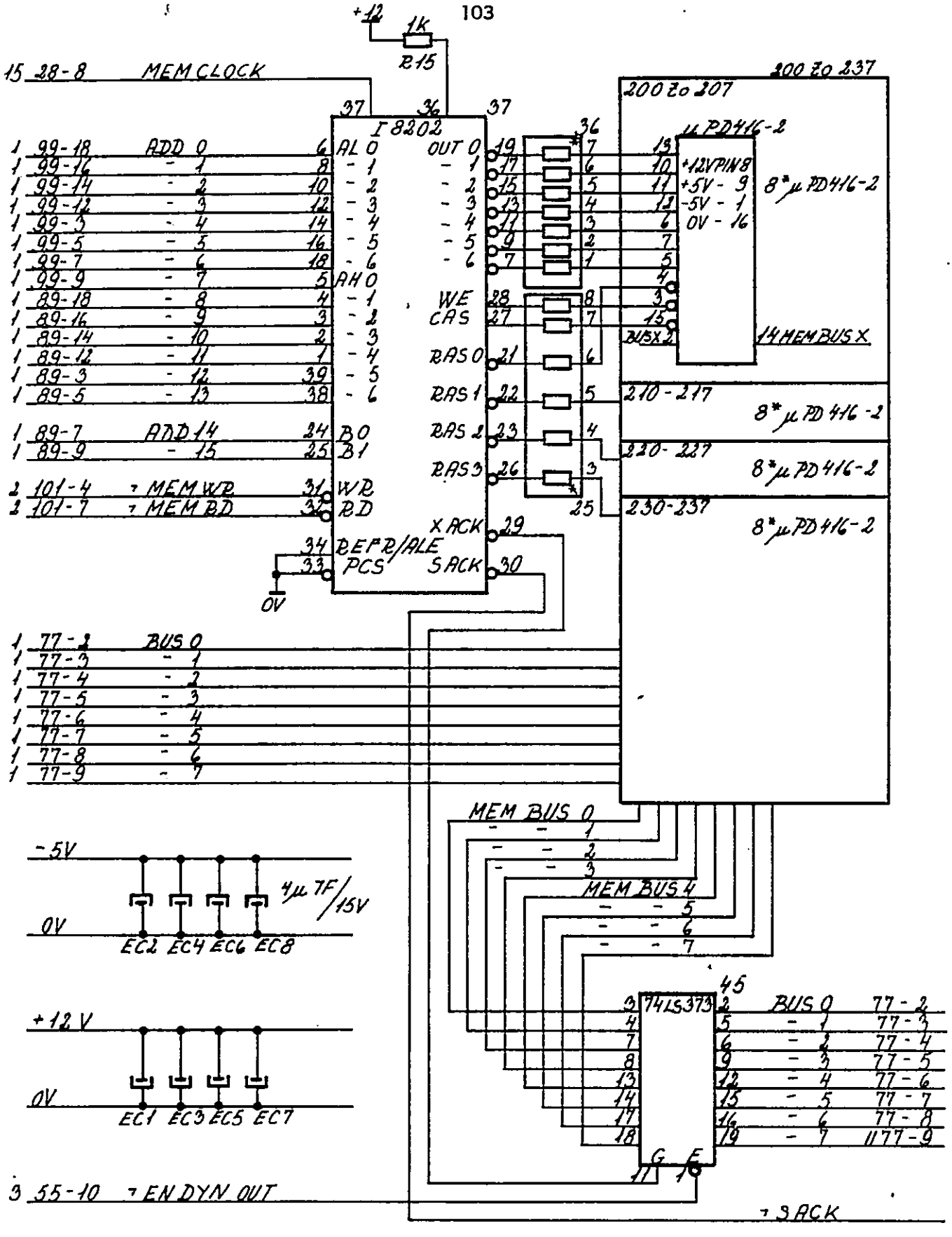
Signal	Destination MIC No.	Description
EN DYN OUT	5	* This signal enables the output register from the RAM.
EN PROM 1	4	* This signal enables the output from PROM 1 which is only used when running a testprogram.
EN PROM 0	4	* This signal enables the output from PROM 0 which contains the program used under initiation.
EN DISP	11	* ENABLE DISPLAY controller
EN FLOP	9	* ENABLE FLOPPY controller
EN SIO	16	* ENABLE SERIAL IN/OUT controller
EN CTC	15	* ENABLE COUNTER/TIMER controller
EN PIO	7	* ENABLE PARALLEL IN/OUT controller
EN SWITCH	3, 15	* ENABLE SWITCHES
DIS PROM		* DISABLE PROM, the signal is used to disable the PROM and enable the whole RAM
EN SOUND	7	* ENABLE SOUND gives the acoustic signal
EN DMA	6	* ENABLE DMA controller
MOTOR EN	10	MOTOR ENABLE is used to switch on and off the motor used in the Mini floppy disk drive.
RESET	1, 3, 6, 9, 11 15, 16	RESET is the power up reset or a RESET initiated from the switch on the front of the computer.
		* Subsection 2.3.3. describes the actual addresses used in MIC704.


+5V
3*1K
R37, R36, R35
2 101-7 ~MEMRD
1 89-14 ADD 10
1 89-12 11
1 89-3 12
1 89-5 13
1 89-7 14
1 89-9 15
3 U42-6 PROM CONTROL 1
PROM
74S287
~EN DYN OUT
~EN PROM 1
~EN PROM 0
1 99-16 ADD 1
14 R19 LOGICAL ONE
1 99-18 ADD 0
2 100-4 ~IOWR
3 87-6 ~RESET
74LS 32
74LS74
PROM CONTROL 1
74LS138
1 99-14 ADD 2
1 99-12 - 3
1 99-3 - 4
2 86-6 ~ADDR EN
1 99-5 ADD 5
1 99-7 ADD 6
1 99-9 ADD 7
74LS 02
~EN DISP
~EN FLOP
~EN SIO
~EN CTC
~EN PIO
~EN SWITCH
~DIS PROM
~EN SOUND
1 99-9 ADD 4
1 99-5 - 5
1 99-7 - 6
1 99-9 - 7
74LS 20
~EN DMA
14 R41 LOGICAL ONE
1 77-2 BUS 0
3 53-10 ~EN SWITCH
74LS 240
~MOTOR EN
3 81-6 ~RESET
~WR SWITCH
J6-1 RESET SWITCH
J6-2 0V
R65 10K
R64
220E
EC27 47µF/16V
74LS 244
100µF/16V
EC17
R46
100E
D9 1N914
15K R47
-12V
74LS 14
74LS 00
~RESET R32
RESET
MIC 704
MIC 705
R13637
ADDRESS DECODERS & RESET CIRCUIT
MIC 3

Signal	Destination MIC No.	Description
BUS(0:7)		The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
WAIT	2	WAIT supplies at least one wait state to the CPU-fetch cycle. More wait states are inseted when the RAM controller is making a refresh cycle.
WAIT DMA	6	WAIT DMA supplies at least one wait state in the DMA-cycle. More wait states are supplied when the memory controller is making a refresh cycle.
S10 S11 S12 S13		When jumper is mounted (as shown with dotted lines) the sockets are prepared for a 2 KB PROM like 2716.


3 55-12 ¬EN PROM 0
1 99-18 ADD 0
1 99-16 - 1
1 99-14 - 2
1 99-12 - 3
1 99-3 - 4
1 99-5 - 5
1 99-7 - 6
1 99-9 - 7
1 89-18 - 8
1 89-16 - 9
1 89-14 - 10
+5V
S13
1 89-12 ADD11
1 89-3 ADD12
1 89-5 ADD13
S11 +5V
66
OE
+5V
PIN28
PIN 1
OV
PIN14
PROM
CE
OV
PIN No. REFERS TO A 28 PIN SOCKET
PROGRAM ROM 0
BUS 0
- 1
- 2
- 3
- 4
- 5
- 6
- 7
3 55-11 ¬EN PROM 1
1 99-18 ADD 0
1 99-16 - 1
1 99-14 - 2
1 99-12 - 3
1 99-3 - 4
1 99-5 - 5
1 99-7 - 6
1 99-9 - 7
1 89-18 - 8
1 89-16 - 9
1 89-14 - 10
+5V
S12
1 89-12 ADD11
1 89-3 ADD12
1 89-5 ADD13
S10 +5V
65
OE
+5V
PIN28
PIN 1
OV
PIN14
PROM
CE
OV
PIN NO. REFERS TO A 28 PIN SOCKET
PROGRAM ROM 1
2 110-3 ¬MREQ BUF
87
74LS 00
74LS 38
J8-C28 ¬WAIT
+5V
R45 560E
5 37-30 ¬SACK
96
74LS 38
74LS 14
90
C9 1nF
0V
2 101-7 ¬MEM RD
2 101-4 ¬MEM WR
2 86-6 ¬ADDR EN
5 37-30 ¬SACK
79
74LS 00
62
74LS 08
2 109-18 CLK
87
74LS 00
14 R 19 LOGICAL ONE
54
74LS74
¬WAIT DMA
MIC 704
MIC 705
R 13638
PROM MEMORY & WAIT STATE
MIC 4

Signal	Destination MIC No.	Description
BUS(0:7)		The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
SACK	4	Output signal from the RAM controller showing that the cycle is finished. (SACK means System Acknowledge).



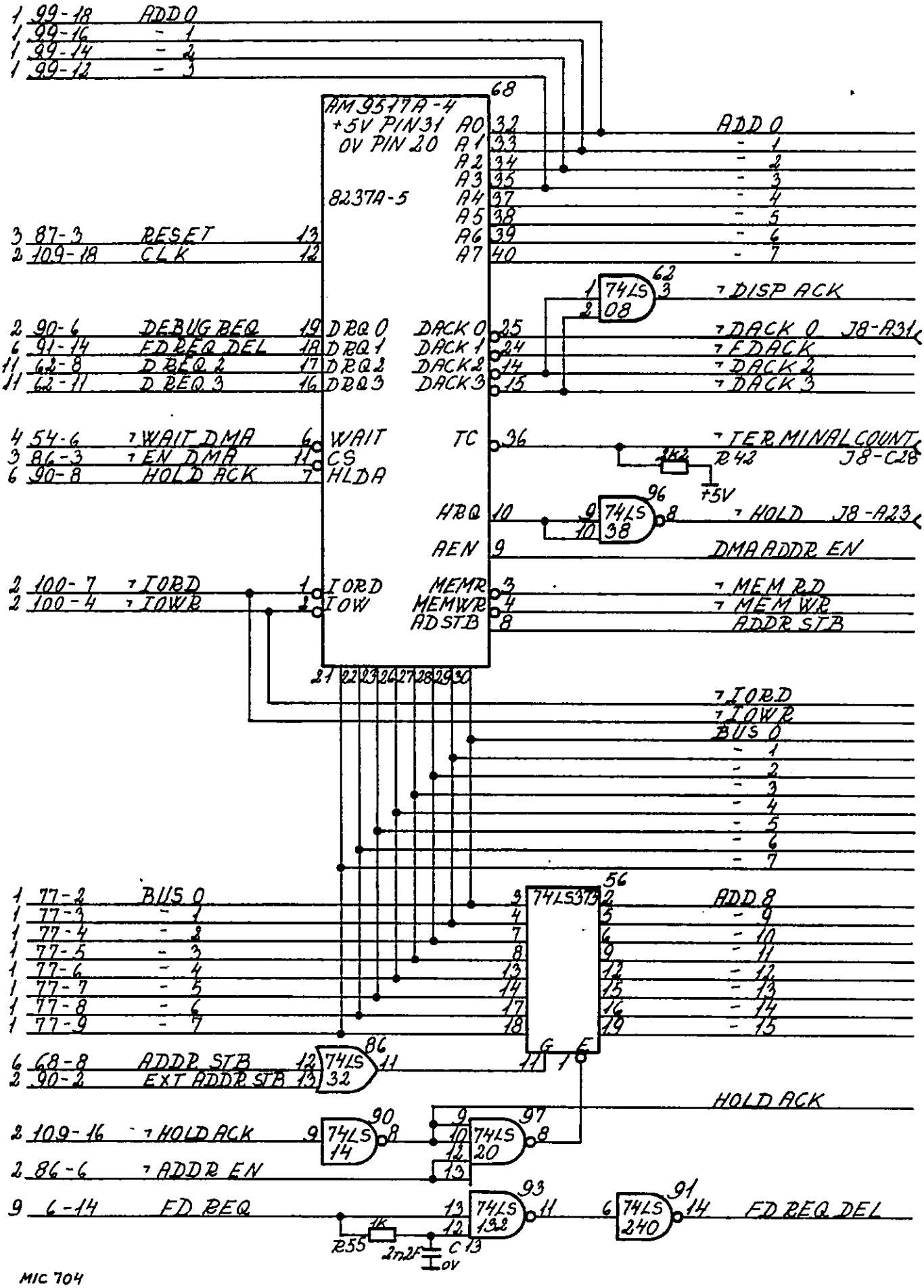
MVP 82.10.01 AGA 82.2.18

MIC 704
MIC 705
R 13639

64 K BYTES DYNAMIC RAM ARRAY & TIMING

MIC 5

Signal	Destination MIC No	Description
ADD(0:7)		Address lines containing the 8 most significant bits. Bit (0:4) is both input to the DMA controller (under programming) and output from the DMA controller (under DMA-cycle).
DACK 0	2	Data acknowledge answer to debug request.
FDACK	9	Floppy data acknowledge, answer to FD req. delay.
DACK 2	11	Data acknowledge answer to DREQ2.
DACK 3		Data acknowledge answer to DREQ3.
DISP ACK	11	Display acknowledge. The display controller uses two channels in the DMA.
TERMINAL COUNT	2, 9, 11	The signal is used to terminate the operation.
HOLD	2	Request to stop the CPU.
DMA ADDR EN	2	Request to gain control over the data and address bus.
MEM RD		Memory read output from the DMA.
MEM WR		Memory write output from the DMA.
ADDR STROBE	6	Address strobe is a pulse to load the address register.
BUS(0:7)		Data bus used to supply information between the CPU and the controllers. Here also used to send address information from the DMA controller to the address register.
HOLD ACK		Hold acknowledge is the replay from the CPU that the bus is idle.
FD REQ DEL		DMA request signal from floppy disk controller.



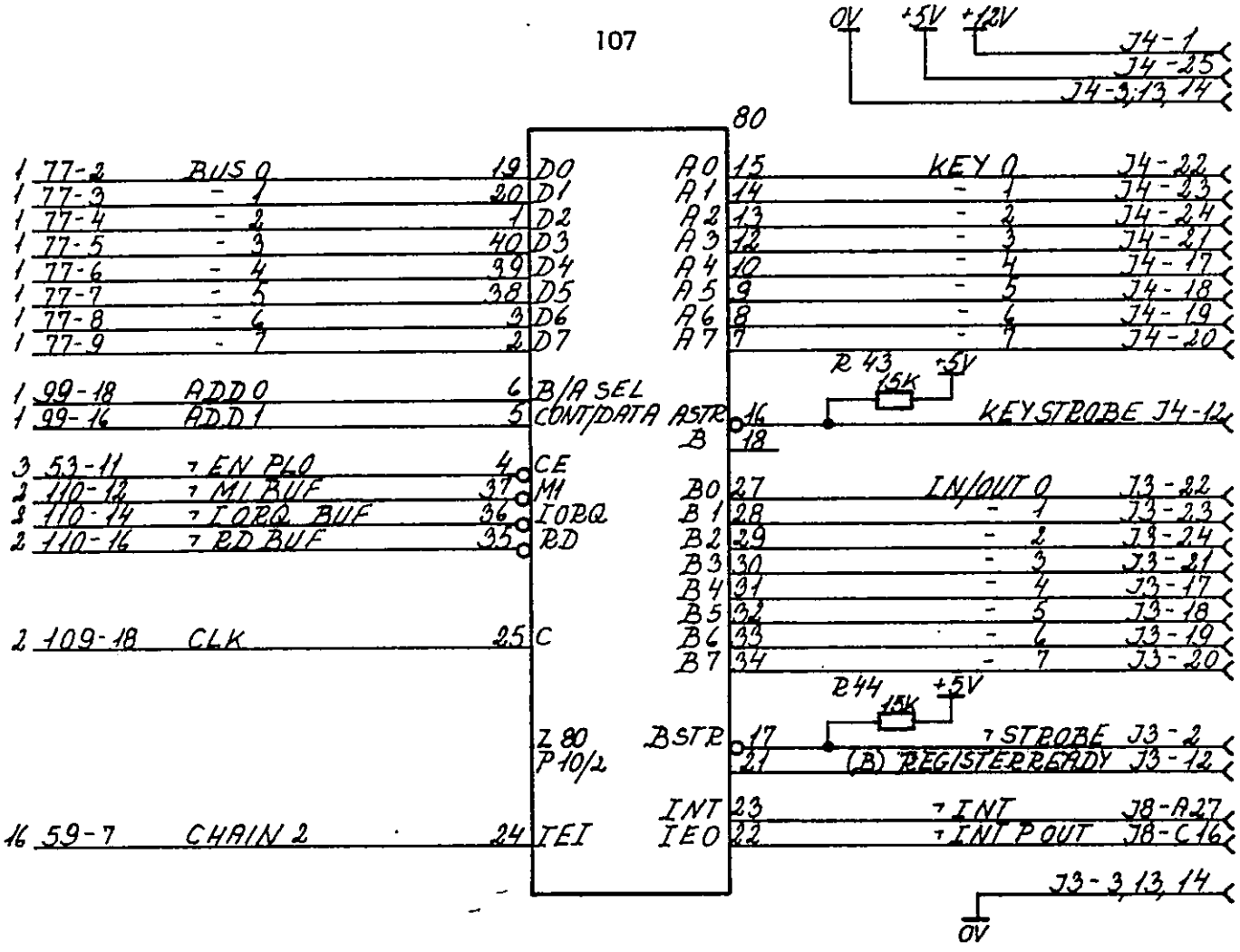
MIC 704
MIC 705

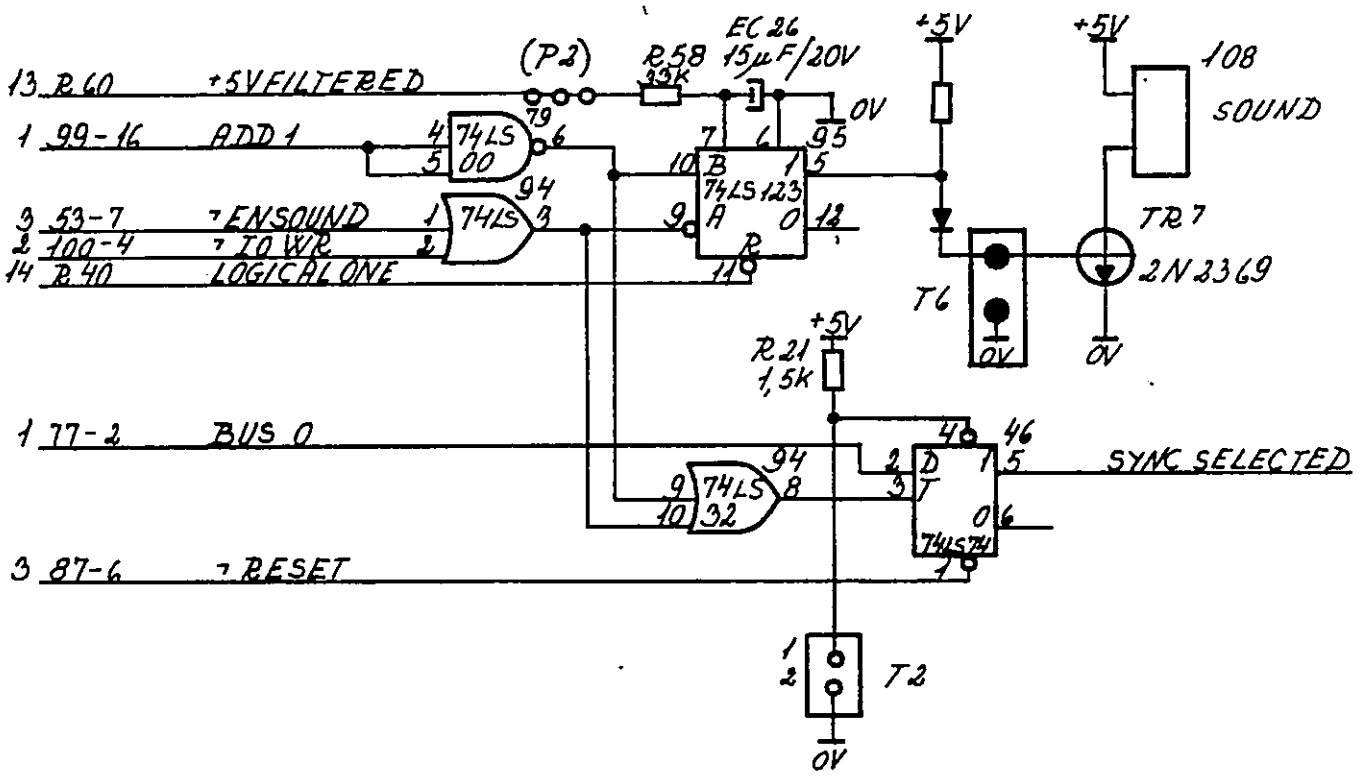
R 13C40

DMA - CONTROLLER

MIC 6

Signal	Destination MIC No.	Description
KEY(0:7)		8-bit parallel input used to receive information from the keyboard.
KEY STROBE		Input strobe from the keyboard.
IN/OUT(0:7)		8-bit parallel input/output used to receive or transmit information to and from an external unit.
STROBE		Input strobe from external unit.
REGISTER READY		Output showing that output from the 8-bit input/output port is ready.
INT	2	Interrupt request.
INT P OUT	2	Interrupt priority out.
SYNC SELECTED	17	This flip flop is set, when the program wants to use synchronous data transmission on SIO/2 channel A.





MIC 704
MIC 705

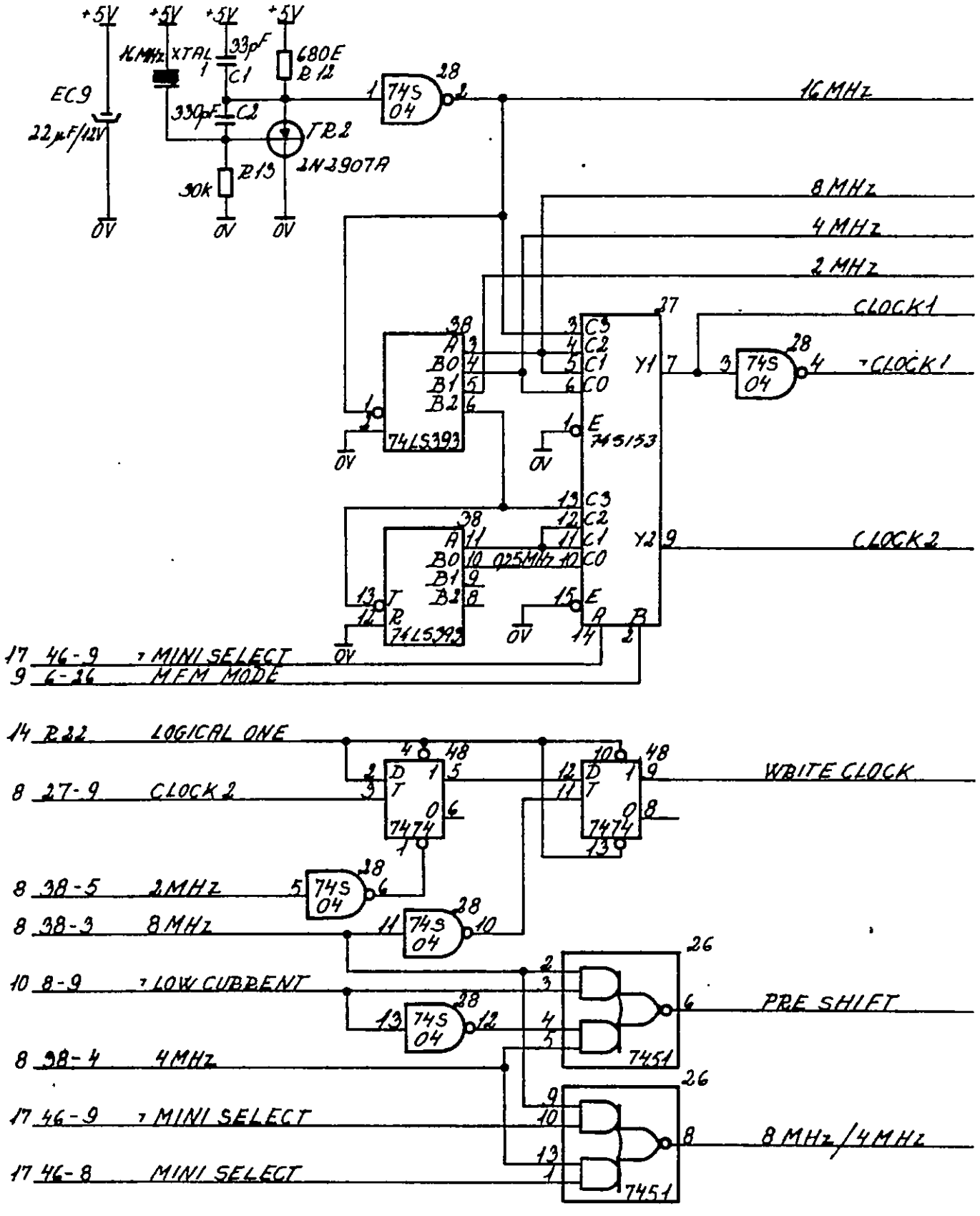
KEYBOARD & PARALLEL IN/OUT

MIC 7

R 13641

MIO 82.10.01 1964 82.2.16

Signal	Destination MIC No.	Description
16 MHz		Symmetric clock signal of 16 MHz
8 MHz	8, 9	- - - - 8 MHz
4 MHz	2, 8	- - - - 4 MHz
2 MHz	8	- - - - 2 MHz
1 MHz	8	- - - - 1 MHz
0.5 MHz	8	- - - - 0.5 MHz
0.25 MHz	8	- - - - 0.25 MHz
CLOCK 1	10	Clock to read logic for the
CLOCK 2	8	floppy controller. Frequency is selected by the controller and by the MINI SELECT switch.
8 MHz/4 MHz	9	Clock to the floppy controller 8 MHz for Maxi floppy and 4 MHz for Mini floppy drive.
WRITE CLOCK	9	Clock input to floppy controller. The frequency is selected by the controller and by the MINI SELECT switch.
PRE SHIFT	9	Input clock to shift register for write data.
MEM CLOCK	5, 15	Clock to the memory controller. The frequency is 19.66 MHz.



MIC 704
MIC 705

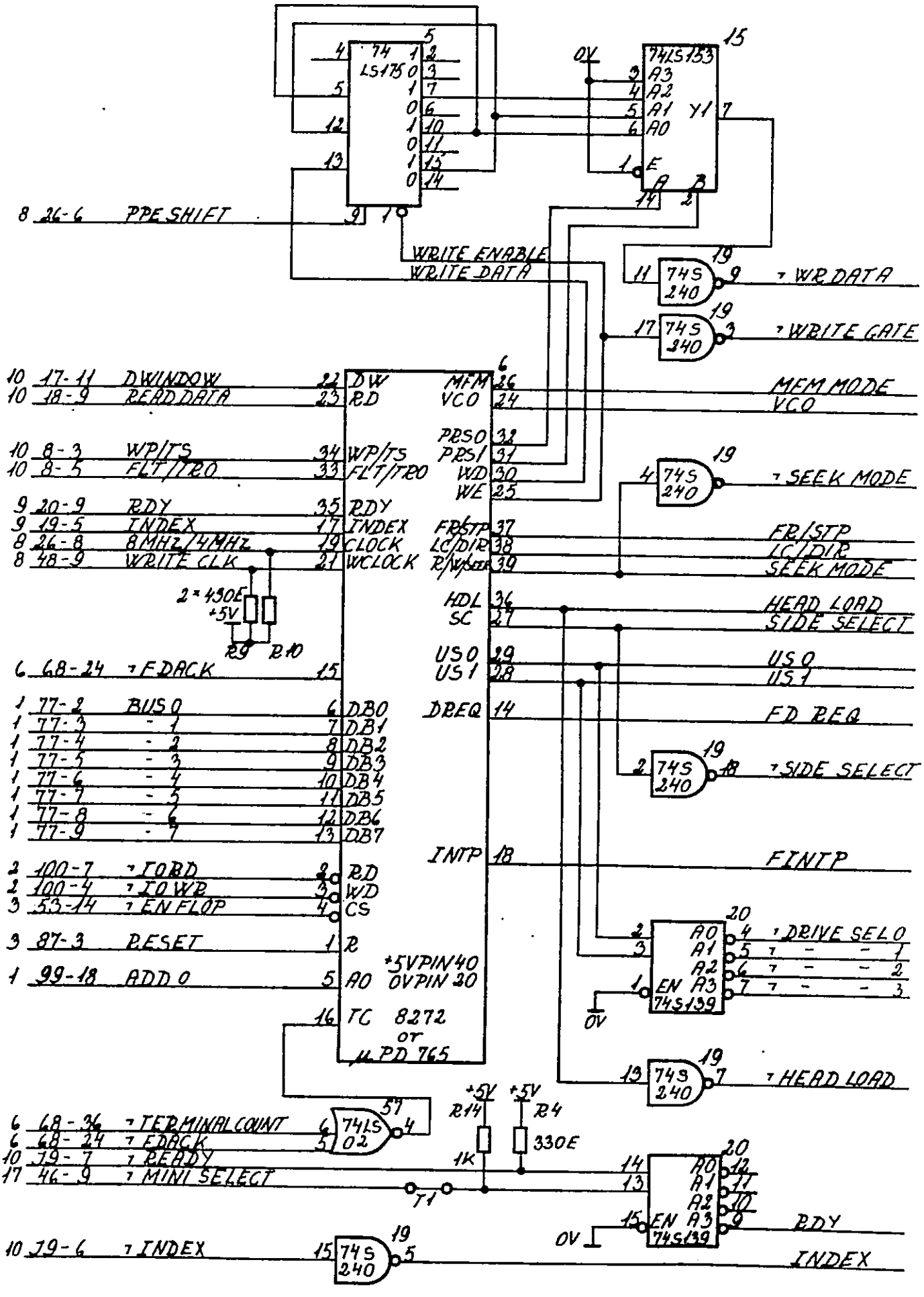
CLOCK SYSTEM

MIC 8

R 13642

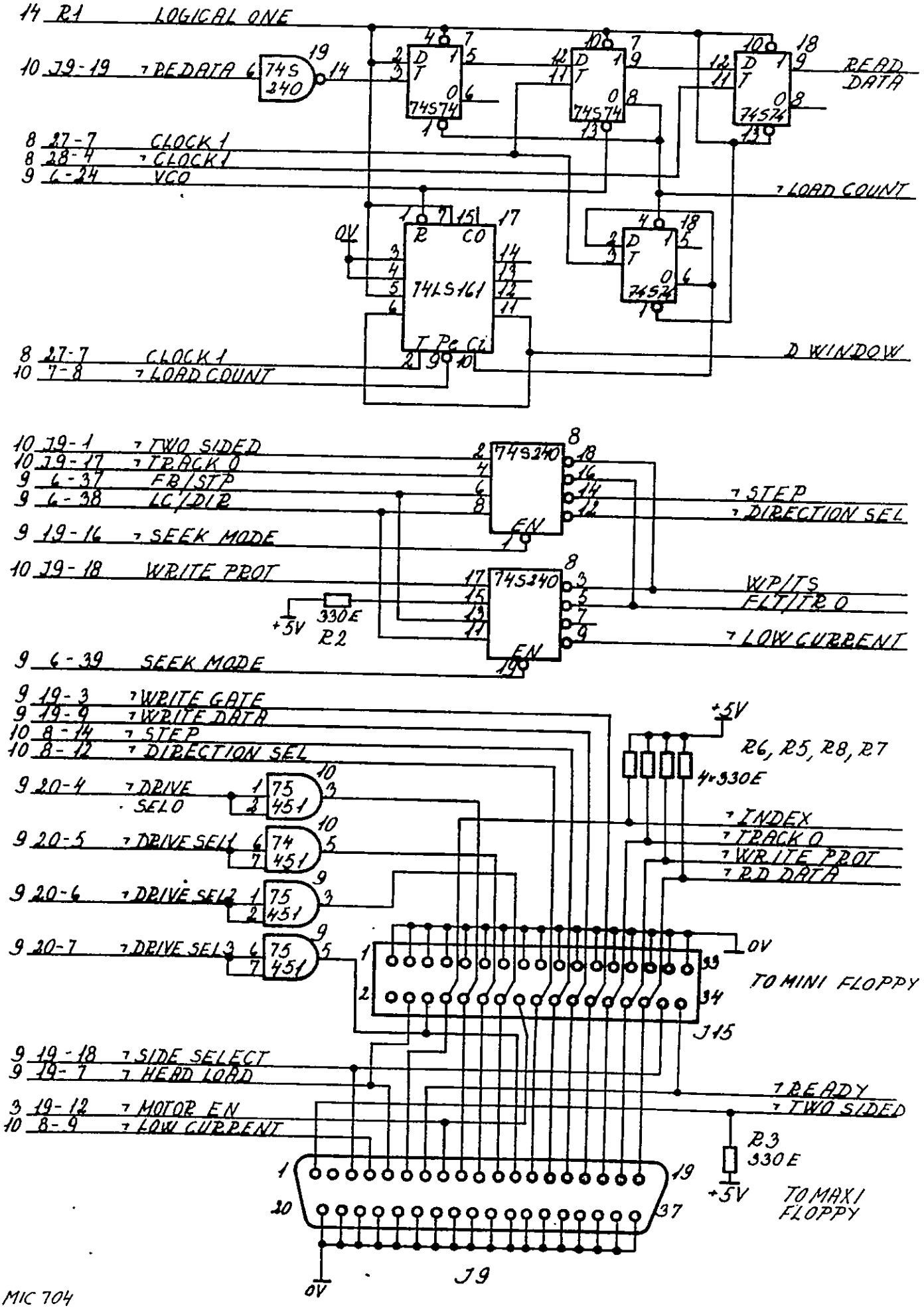
Signal	Destination MIC No.	Description
WR DATA	10	WRITE DATA to the floppy disk drive. Valid when WRITE GATE is on.
WRITE GATE	10	Control signal to floppy disk drive. Informs that now the WR DATA is valid.
MFM MODE	8	MFM mode is dual density, FM mode is single density.
VCO	10	Signal to control the voltage controlled oscillator.
SEEK MODE	10	Sets the selectors in seek mode.
FR/STP	10	Control signal; Fault Reset/ Step
LC/DIR	10	Control signal; Low Current/ Direction
HEAD LOAD	10	Control signal; Head Load
SIDE SELECT	10	Control signal; Side Select
US0, US1		Unit select decoded to:
DRIVE SEL 0	10	Drive Select 0
DRIVE SEL 1	10	Drive Select 1
DRIVE SEL 2	10	Drive Select 2
DRIVE SEL 3	10	Drive Select 3.
FD REQ	6	DMA reguest from floppy controller.
F INTP	15	Floppy controller interrupt request.
RDY	9	Ready from floppy controller. Note that Mini floppy is always ready.
INDEX	9	Index mark from floppy disk drive.

T1 is closed in MIC704 and open in MIC705. MIC705 uses mini-floppies with 96 tpi and with a Ready signal.


74LS153
74LS175
74S240
74LS139
74LS02
8272
or
μPD 765
8 26-6 PPE SHIFT
WRITE ENABLE
WRITE DATA
7 WR DATA
7 WRITE GATE
10 17-11 DWINDOW
10 18-9 READ DATA
10 8-3 WP/TS
10 8-5 FLT/TRO
9 20-9 RDY
9 19-5 INDEX
8 26-8 8MHz/4MHz
8 48-9 WRITE CLK
2 × 430E
+5V
R9
R10
6 68-24 7 FDACK
1 77-2 BUS 0
1 77-3 - 1
1 77-4 - 2
1 77-5 - 3
1 77-6 - 4
1 77-7 - 5
1 77-8 - 6
1 77-9 - 7
2 100-7 7 IORD
2 100-4 7 IOWR
3 53-14 7 ENFLOP
3 87-3 RESET
1 99-18 ADD 0
MFM
VCO
PRS0
PRS1
WD
WE
FR/STP
LC/DIR
R/W sect
HDL
SC
US0
US1
DREQ
INTP
MFM MODE
VCO
7 SEEK MODE
FR/STP
LC/DIR
SEEK MODE
HEAD LOAD
SIDE SELECT
US 0
US 1
FD REQ
7 SIDE SELECT
FINTP
7 DRIVE SEL 0
7 - - 1
7 - - 2
7 - - 3
7 HEAD LOAD
+5V PIN 40
0V PIN 20
6 68-36 7 TERMINAL COUNT
6 68-24 7 FDACK
10 19-7 7 READY
17 46-9 7 MINI SELECT
+5V
R14
1K
R4
330E
T1
RDY
10 19-6 7 INDEX
INDEX
MIC 704
MIC 705
R13643
FLOPPY DISK CONTROLLER
MIC 9

Signal	Destination MIC No.	Description
READ DATA	9	Read data from the floppy, synchronized with the VCO to separate phase bits and data bits.
LD COUNT	10	Load counter is used to synchronize the window counter.
D WINDOW	9, 10	Data Window is used by the controller to separate data bits from phase bits.
STEP	10	Output pulse to make the floppy head move from one cylinder to the next.
DIRECTION SEL	10	Direction select is used together with the STEP pulse. A low signal and the head moves towards the counter of the disc.
WP/TS	9	Write Protect/Two Sided signal from the floppy disk drive.
FLT/TRO	9	Fault/Track 0 signal from floppy disk drive.
LOW CURRENT	10	Output signal to Maxi floppy disc drive. Used to decrease the write current when close to the center of the disk.
INDEX	9	Index mark signal from the floppy.
TRACK 0	10	Track 0 signal from the floppy.
WRITE PROT	10	The diskette used is writeprotected.
RD DATA	10	Read data supplied from the floppy disk drive including data and phase bits.
READY	9	Ready signal from the Maxi floppy drive.
TWO SIDED	10	The Maxi floppy is a two sided version.

The connections J15 pin 34 to J9 pin 7 and J15 pin 4 to J9 pin 5 have not been made on all MIC704 boards. In fact, these connections are only utilized with the MIC705.



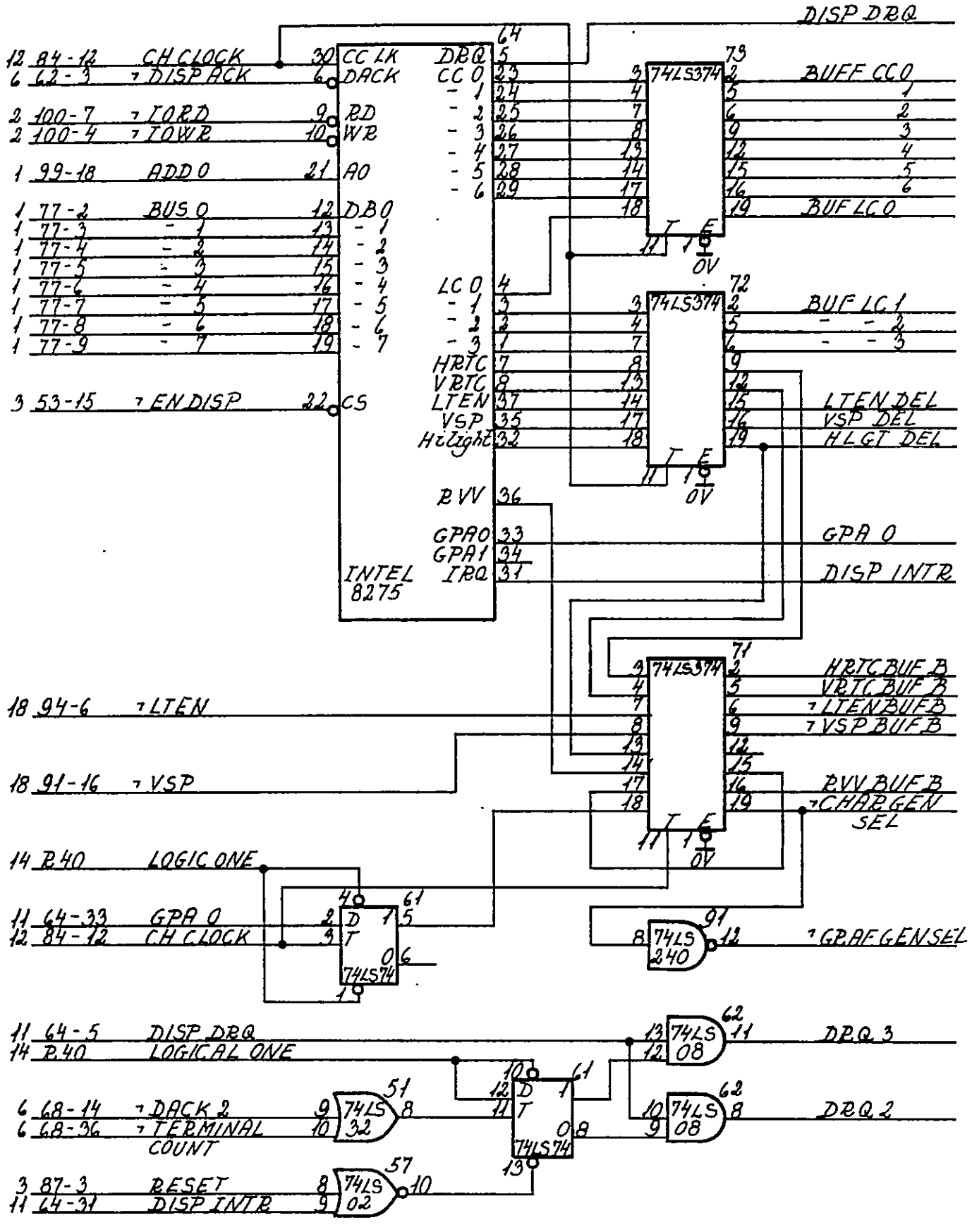
MIC 704
MIC 705

R 13644

FLOPPY DISK READ & SELECT CIRCUIT

MIC 10

Signal	Destination MIC No.	Description
DSP DRQ	11	DMA request from the display controller.
BUFF CC(0:6)	12	Output from the display controller containing the address of the character to be written on the display.
BUFF LC(0:3)	12	Output from the display controller containing the line number written on the display.
LTEN DEL	11	Light enable from the display.
VSP DEL	11	Video suppression. This output signal is used to blank the video to the display.
GPA 0	11	Control signal used to select semigraphic PROM.
DISP INTR	11, 15	Display interrupt request.
HRTC BUF B	13	Horizontal retrace signal.
VRTC BUF B	13	Vertical retrace signal.
LTEN BUF B	13, 14	LTEN DEL delayed one CHAR CLOCK
VSP BUF B	13	VSP DEL delayed one CHAR CLOCK
RVV BUF B	13	REVERSE VIDEO. This output is used to reverse the video signal to the display.
CHAR GEN SEL	12	This signal selects the standard character generator.
GRAF GEN SEL	12	This signal selects the semigraphic character generator.
DRQ3 and DRQ2	6	The display controller uses two channels out of the DMA's four channels. This is done to make the roll function of the display. DRQ2 and DRQ3 are the two data request signals.



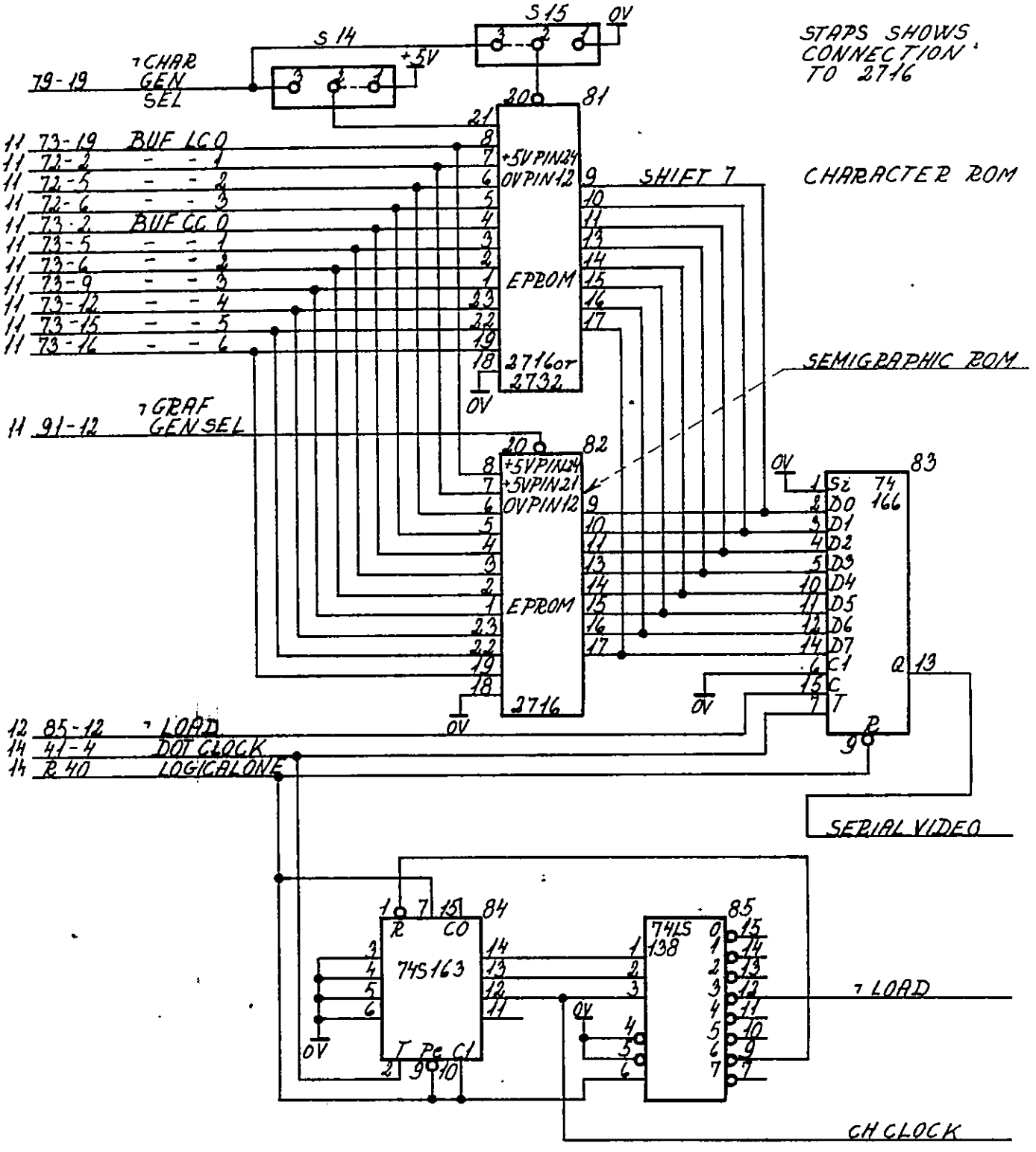
MIC 704
MIC 705

VIDIO DISPLAY CONTROLLER

MIC 11

R 13645

Signal	Destination MIC No.	Description
SERIAL VIDEO	13	The video output from the shift register.
LOAD	12	Signal to load the output from the character ROM or the semigraphic ROM into the shift register.
CH CLOCK	11	Character clock. The period time of this clock is 7 times the DOT CLOCK time. 7 x 86 nsec. = 0.601 usec.



MIP 82.10.01 AGA 82.2.16

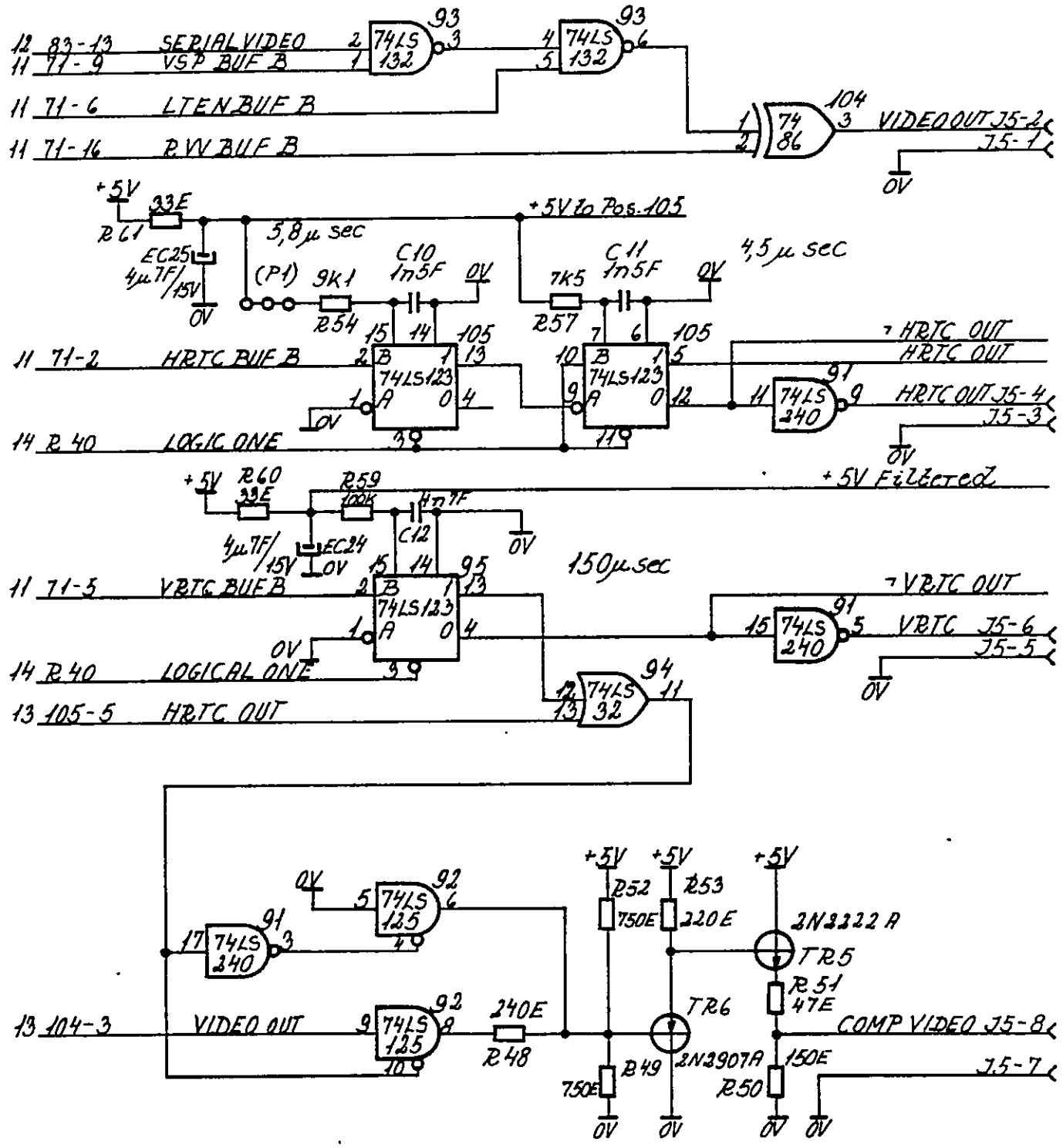
MIC 704
MIC 705

CHARACTER GENERATOR, VIDIO SHIFT REGISTER & DOT COUNTER

MIC 12

R 13646

Signal	Destination MIC No.	Description
VIDEO OUT	13	Video out signal. *)
HRTC OUT	13	Horizontal output pulse. *)
VRTC OUT		Vertical output pulse. *)
		*) These three signals are ready to be used if a video monitor without decoding for comp. video is used. RC702 uses comp. video signals.
COMP VIDEO		Compressed video is the signal containing both video horizontal sync. and vertical sync.
+5 V filtered	7	+5 V supply after an RC filter.



RGB 82.2.16

MVO 82.10.01

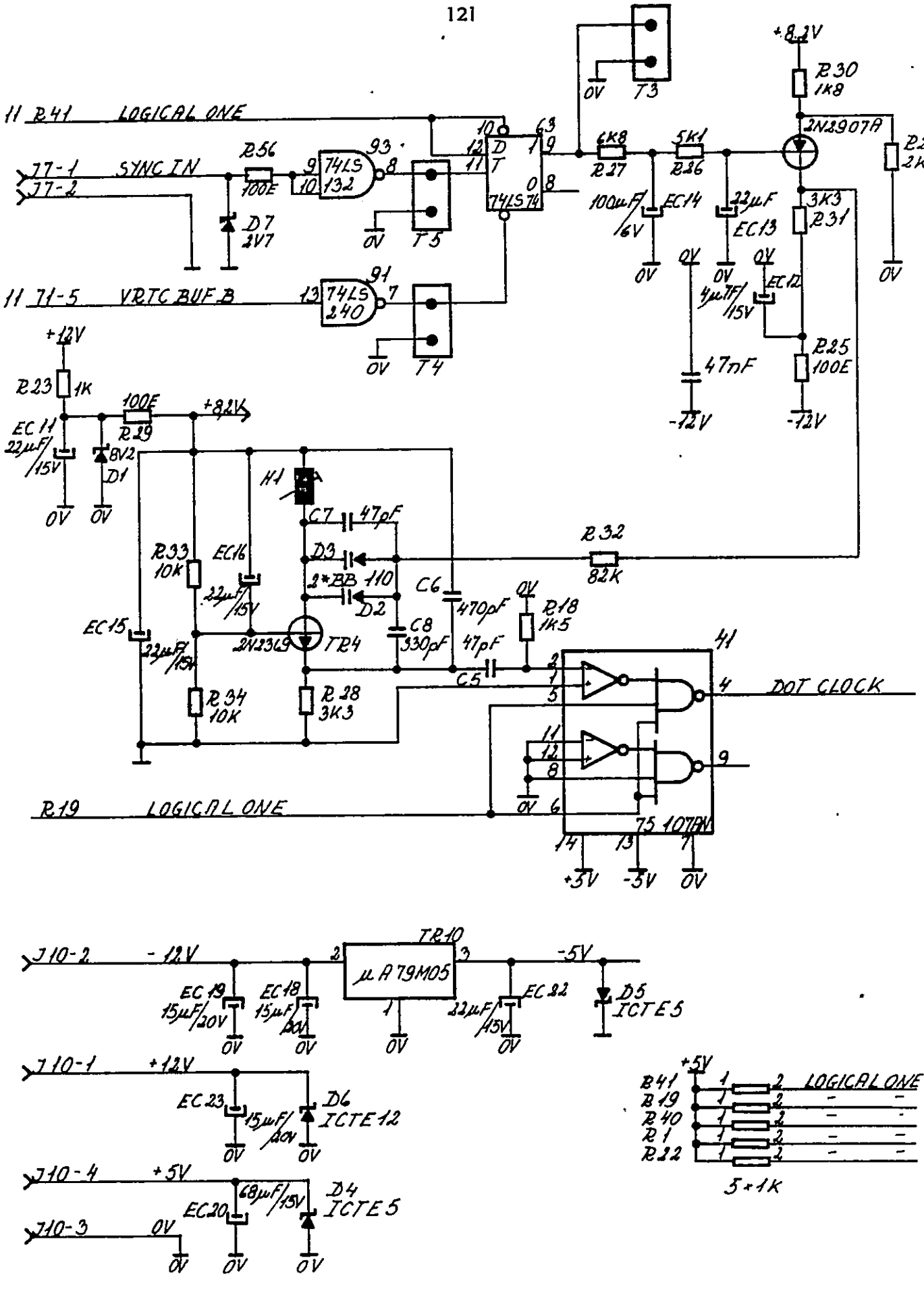
MIC 704
MIC 705

VIDEO GENERATOR

MIC 13

R 13647

Signal	Destination MIC No.	Description
DOT CLOCK	12	The dot clock is an 11.64 MHz clock which is synchronized with the main frequency.
SYNC IN		The input is a 50 Hz signal from the REC701 rectifier unit.
T3		Testpoint 1. The signal here is a 50 Hz signal and the coil H1 is adjusted until the dutycycle of this signal is 50% (between 40% and 60%).
-5 V		The -5 V is used by the dynamic RAM.



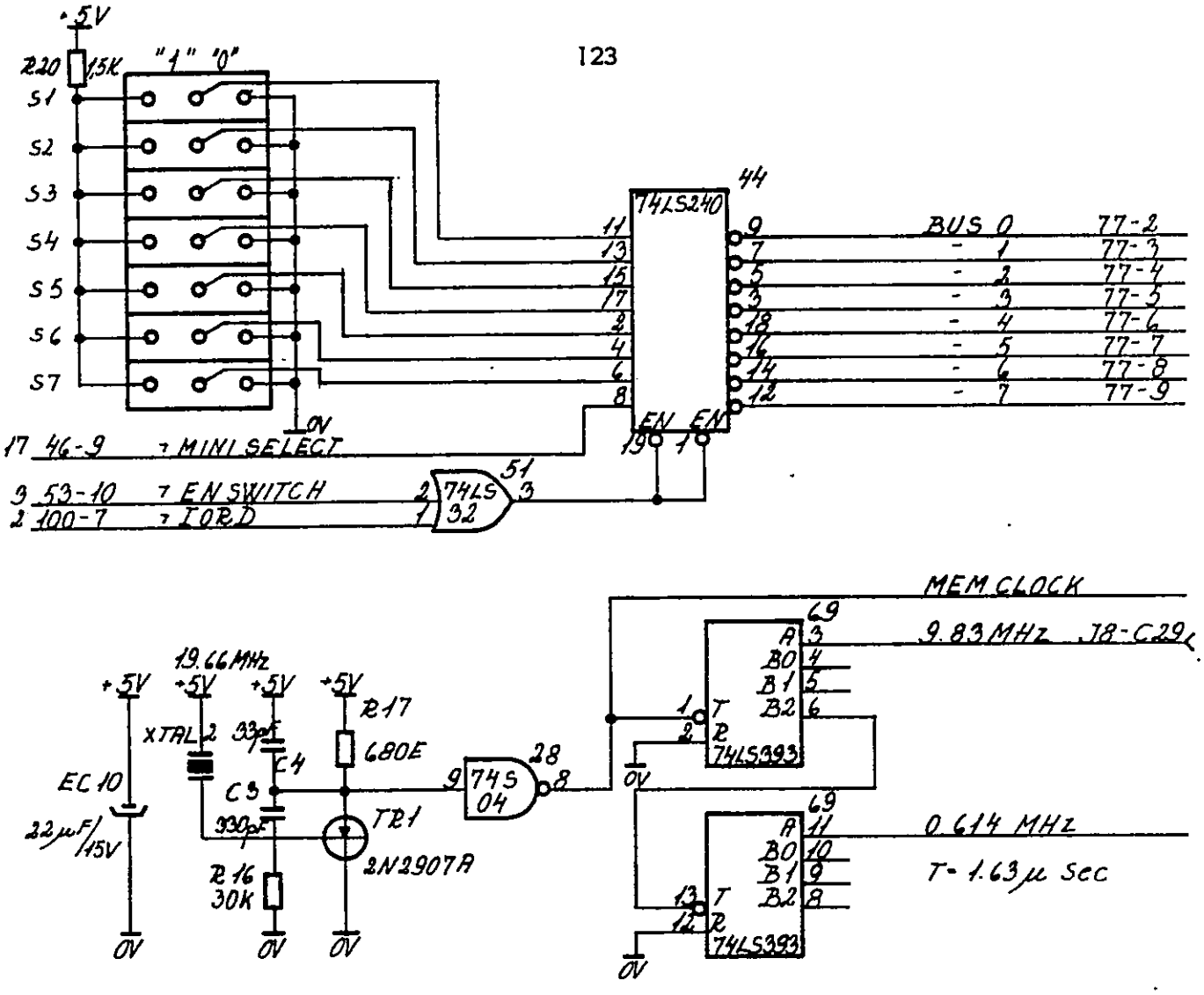
MIC 704
MIC 705

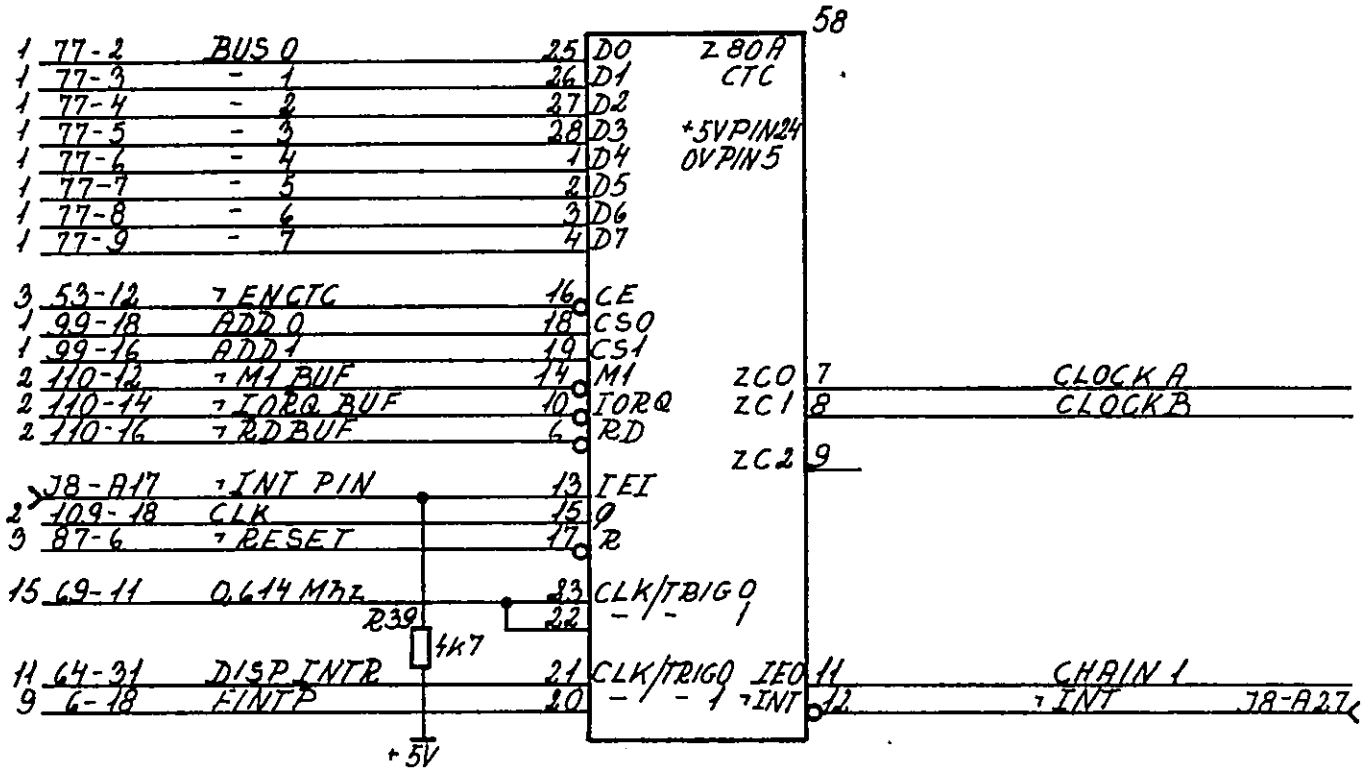
PHASE LOCK LOOP

MIC 14

R13647

Signal	Destination MIC No.	Description
BUS(0:7)	1	The data bus is the TRI-state bus supplying data information between the CPU and all of the controllers.
MEM CLOCK	5	Clock of 19.66 MHz supplied to RAM controller.
9.63 MHz	2	Clock of 9.63 MHz is not used on the board but supplied to the output plug J8.
0.614 MHz	15	Clock of 0.614 MHz is used as input to the counter timer controller to be counted down to make the clock signal to the two Serial In/Out Channels.
CLOCK A CLOCK B	16 16	Clock signal to the two Serial In/Out Channels just mentioned.
CHAIN 1	16	Interrupt priority chain
INT		Interrupt from the counter timer controller.





MIC 704
MIC 705

SWITCH INPUT TO PROGRAM & BAUD RATE GENERATOR MIC 15

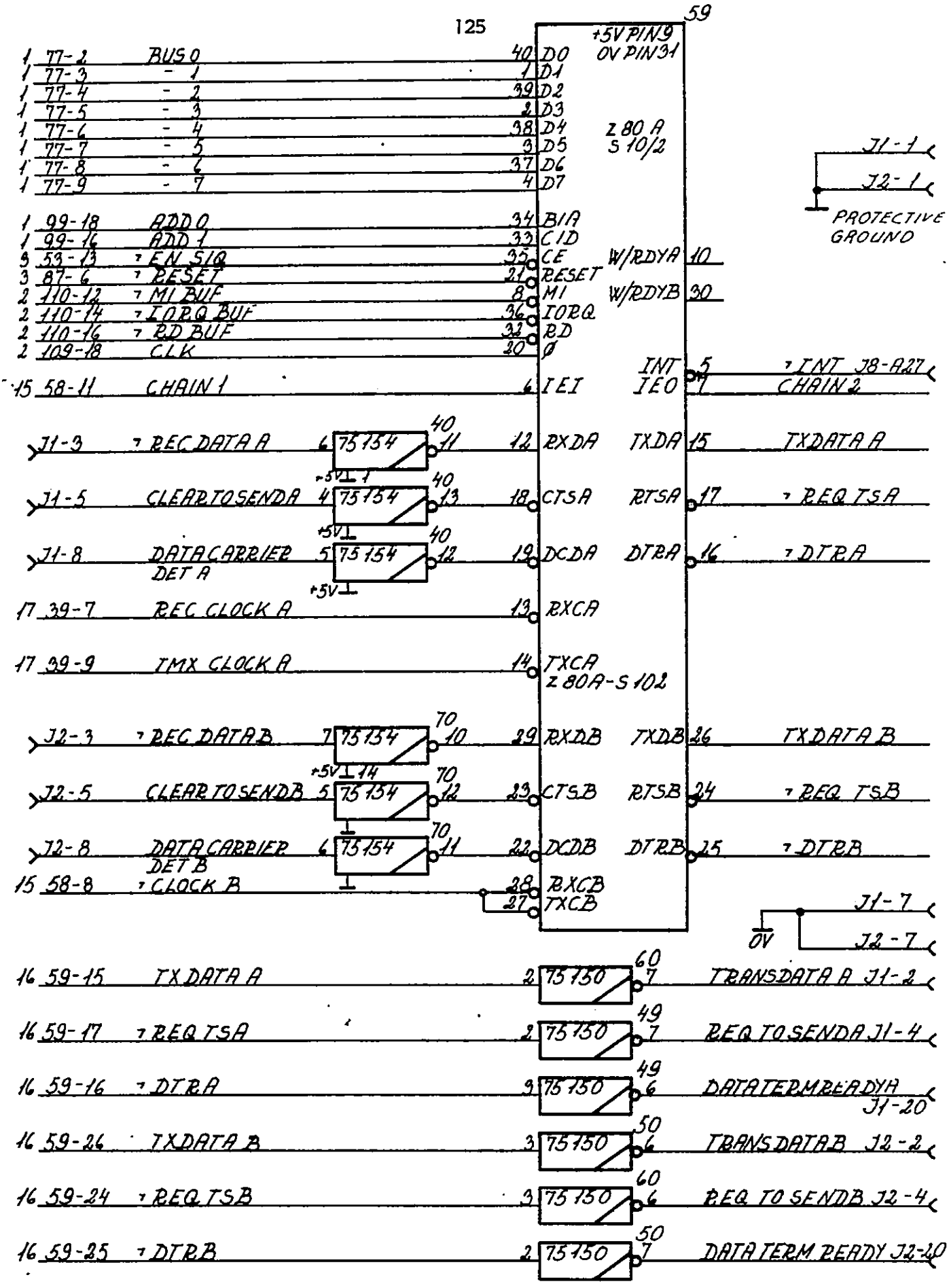
R 13648

Signal	Destination MIC No.	Description
INT	2	Interrupt request from the SIO/2.
CHAIN	2	Interrupt priority chain out from the SIO/2.

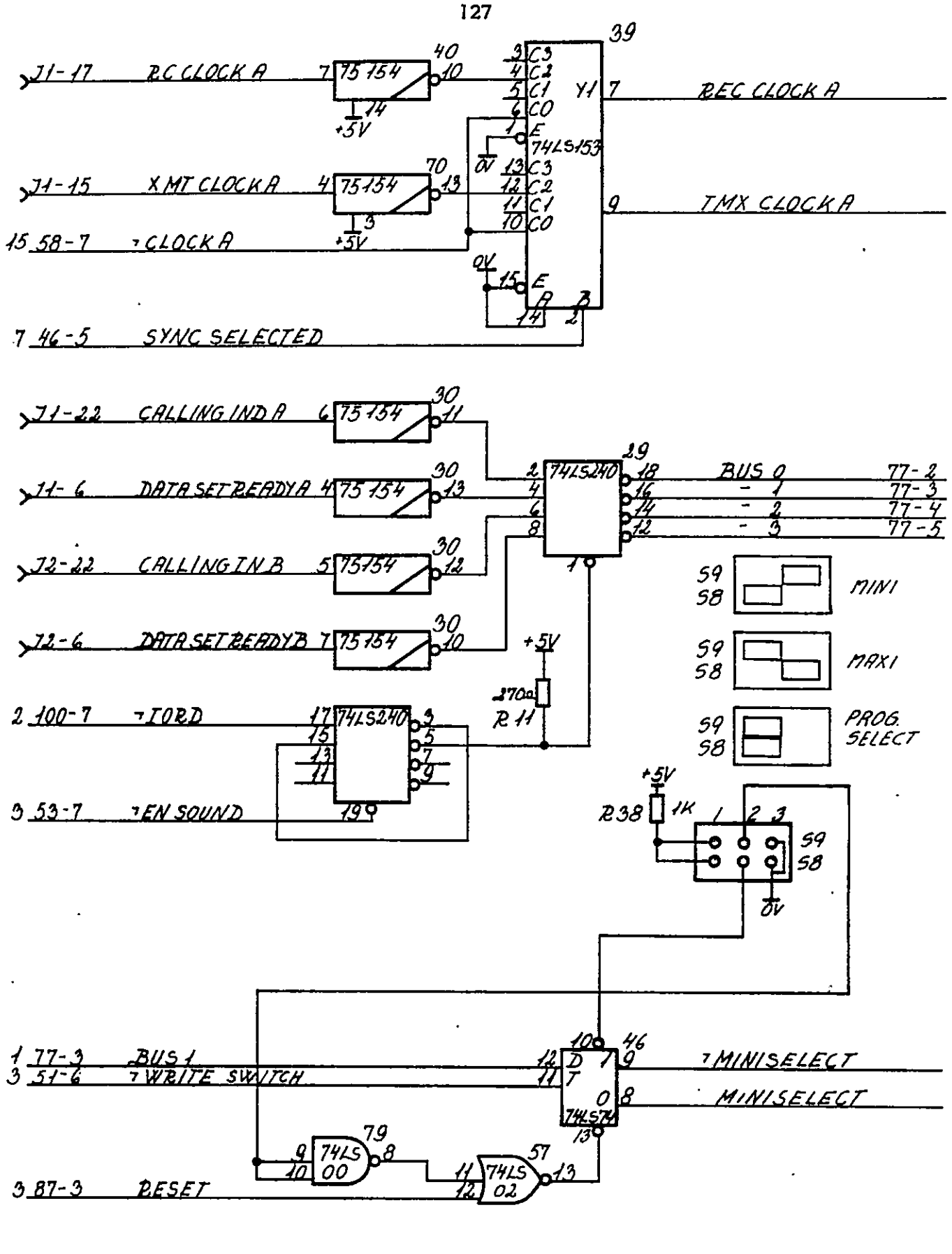
V.24 input outputs

Pin 1 PROTECTIVE GROUND
- 2 TRANS DATA
- 3 REC DATA
- 4 REQ TO SEND
- 5 CLEAR TO SEND
- 7 Ground
- 8 DATA CARRIER DETECT
- 20 DATA TERM READY

J1 to channel A (Terminal)
J2 to channel B (Printer)


59
+5V PIN 9
0V PIN 31
Z 80 A
S 10/2
1 77-2 BUS 0
1 77-3 - 1
1 77-4 - 2
1 77-5 - 3
1 77-6 - 4
1 77-7 - 5
1 77-8 - 6
1 77-9 - 7
40 D0
1 D1
39 D2
2 D3
38 D4
3 D5
37 D6
4 D7
J1-1
J2-1
PROTECTIVE GROUND
1 99-18 ADD 0
1 99-16 ADD 1
9 53-13 ↑ EN SIO
3 87-6 ↑ RESET
2 110-12 ↑ MI BUF
2 110-14 ↑ IORQ BUF
2 110-16 ↑ RD BUF
2 109-18 CLK
34 BIA
33 CID
35 CE
21 RESET
8 MI
36 IORQ
32 RD
20 Ø
W/RDYA 10
W/RDYB 30
INT 5 ↑ INT J8-A27
15 58-11 CHAIN 1
6 IEI
IEO 1 CHAIN 2
J1-3 ↑ REC DATA A
J1-5 CLEAR TO SEND A
J1-8 DATA CARRIER DET A
75154
+5V
40
6
4
5
11
13
12
12 RXDA
18 CTSA
19 DCDA
TXDA 15 TXDATA A
RTSA 17 ↑ REQ TSA
DTRA 16 ↑ DTRA
17 39-7 REC CLOCK A
13 RXCA
17 39-9 TMX CLOCK A
14 TXCA
Z 80A-S 102
J2-3 ↑ REC DATA B
J2-5 CLEAR TO SEND B
J2-8 DATA CARRIER DET B
70
7
5
6
10
12
11
29 RXDB
23 CTSB
22 DCDB
TXDB 26 TX DATA B
RTSB 24 ↑ REQ TSB
DTRB 25 ↑ DTRB
15 58-8 ↑ CLOCK B
28 RXCB
27 TXCB
J1-7
0V
J2-7
16 59-15 TX DATA A
16 59-17 ↑ REQ TSA
16 59-16 ↑ DTRA
16 59-26 TX DATA B
16 59-24 ↑ REQ TSB
16 59-25 ↑ DTRB
75150
60
49
50
2
9
3
7
6
TRANS DATA A J1-2
REQ TO SEND A J1-4
DATA TERM READY J1-20
TRANS DATA B J2-2
REQ TO SEND B J2-4
DATA TERM READY J2-20
MIC 704
MIC 705
SERIAL INPUT OUTPUT
MIC 16
213649

Signal	Destination MIC No.	Description
REC CLOCK A	16	The clock inputs to the SIO/2 channel A. In asynchronous mode clock A is selected, and in synchronous mode the modem supplies the clock.
BUS(0:3)		The data bus is here used to make it possible for the program to read the four modem signals.
MINISELECT	8, 9	This flip flop is set to show if the floppy is a MAXI or a MINI. It may be controlled from the program if it is strapped the correct way.



MVP BE 2.16 A6A
BE 10.01

MIC 704
MIC 705

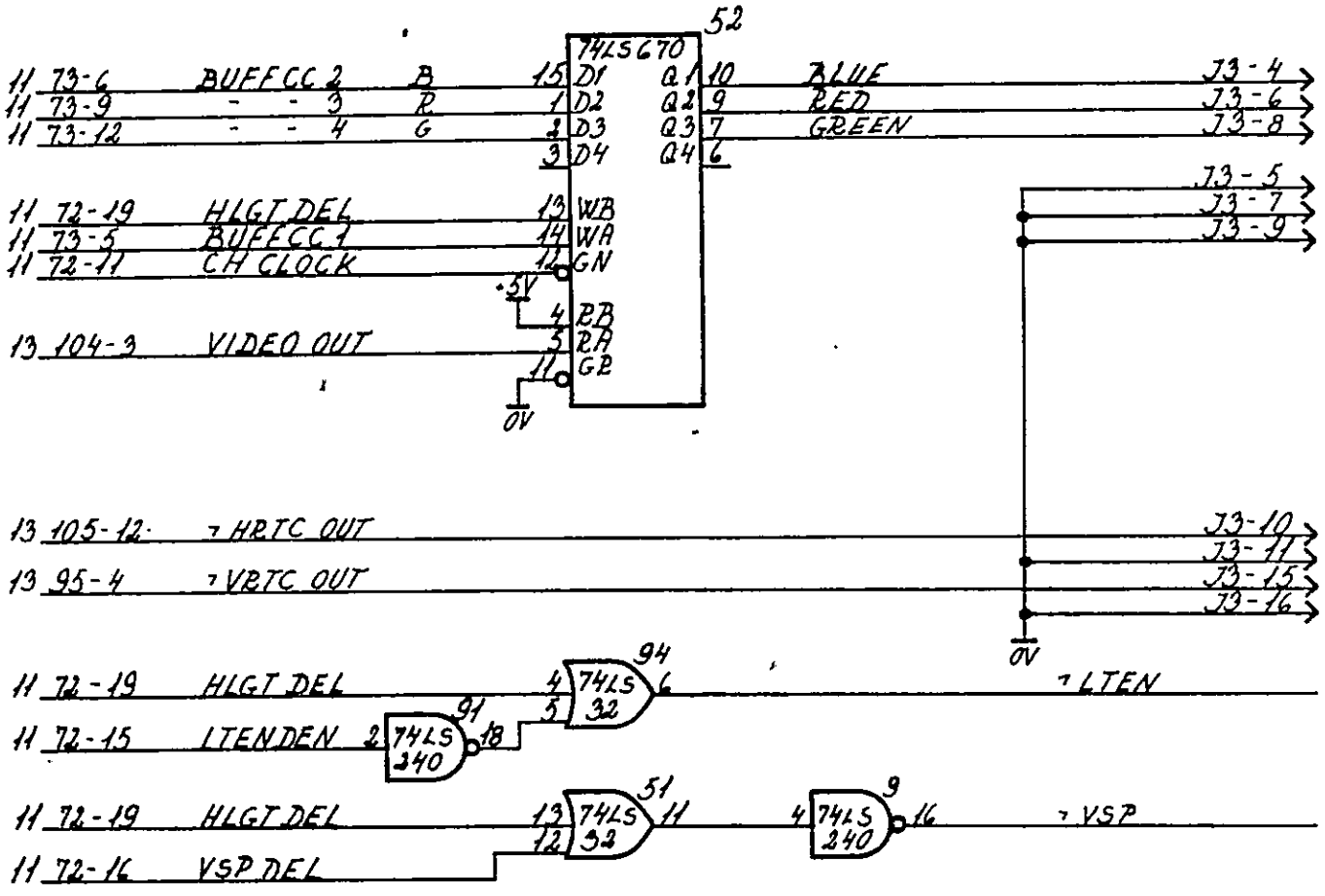
SYNC - TRANS. SELECT AND V. 24 CONTROL SIGNALS

MIC 17

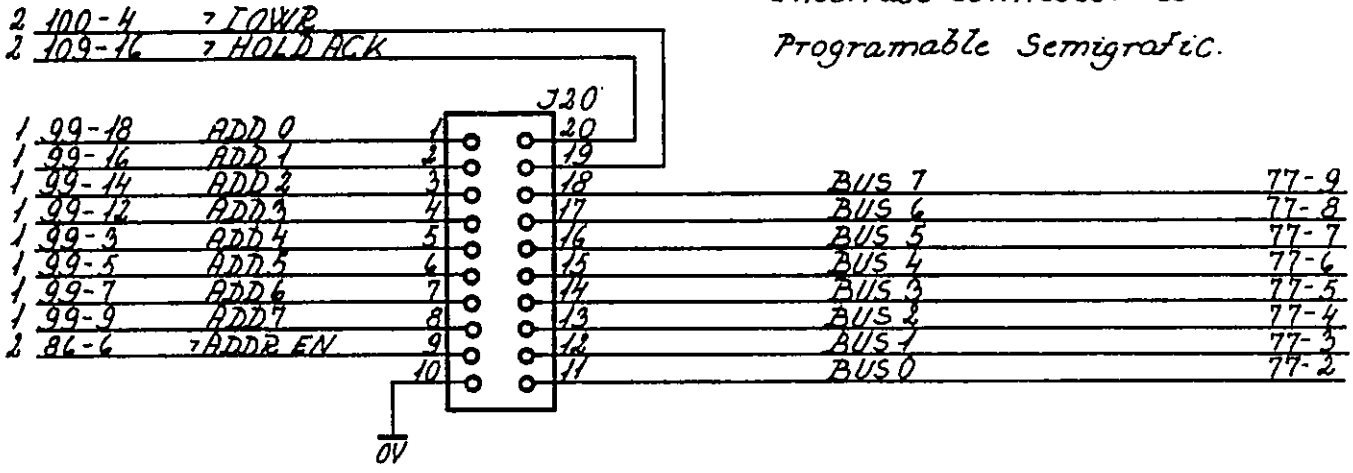
R 13650

Signal	Destination	Description
LTEN	11	Light enable, output signal from the CRT-controller.
VSP	11	Video suppression, output signal from the CRT controller.

Note: Pos. 52 is prepared for mounting of an IC; on some print boards the IC 74LS670 has been mounted. The system, however, does not utilize the facility.



Interface Connector to Programable Semigrafic.



2.5 Character Generator

The character generators are implemented with ROM modules as follows:

Graphic Character Set : ROM module: ROA296
See fig. 35.

Semigraphic Character Set: ROM module: ROA327
See fig. 36.

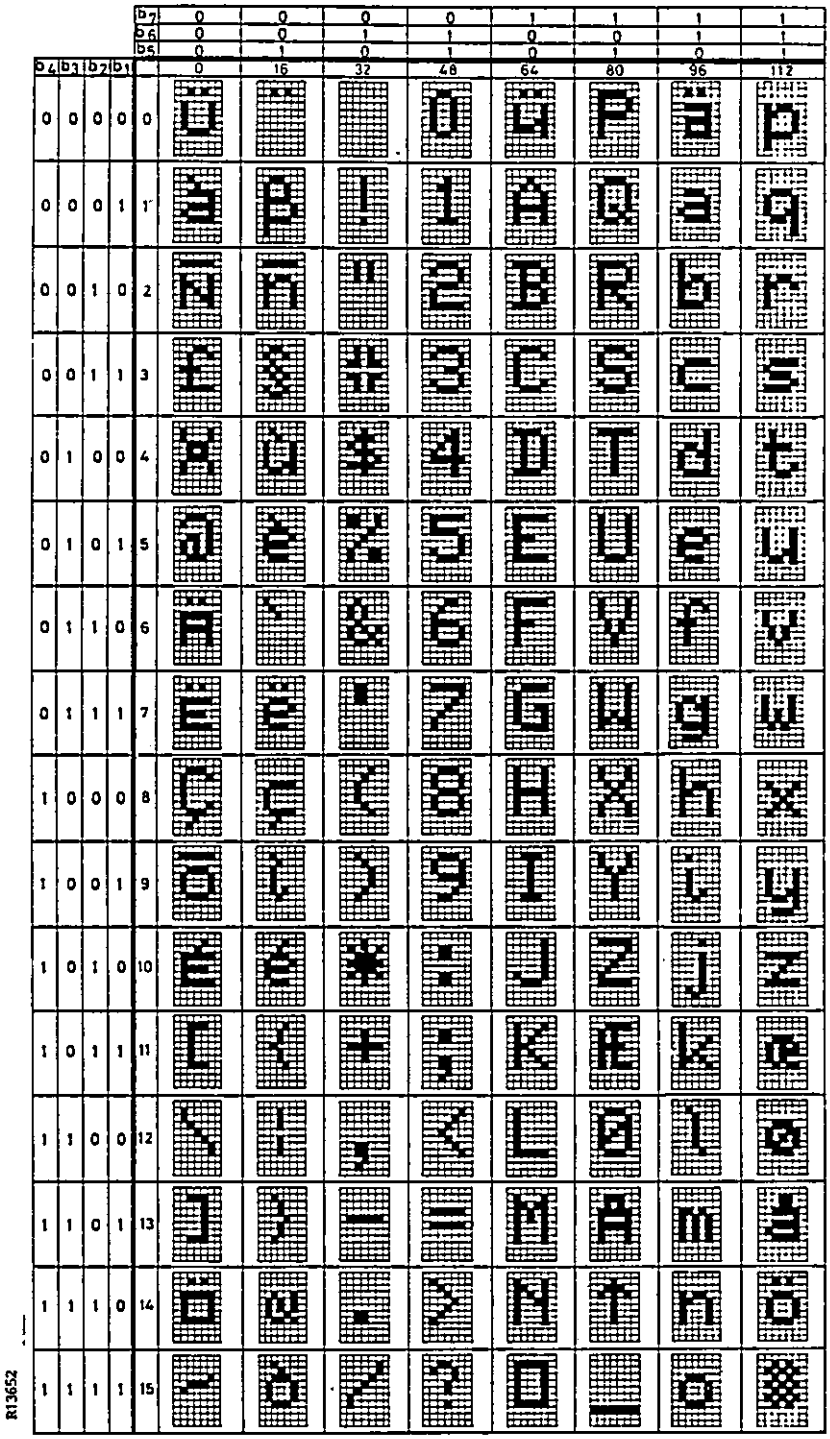


Figure 35: Character Generator (ROA296).

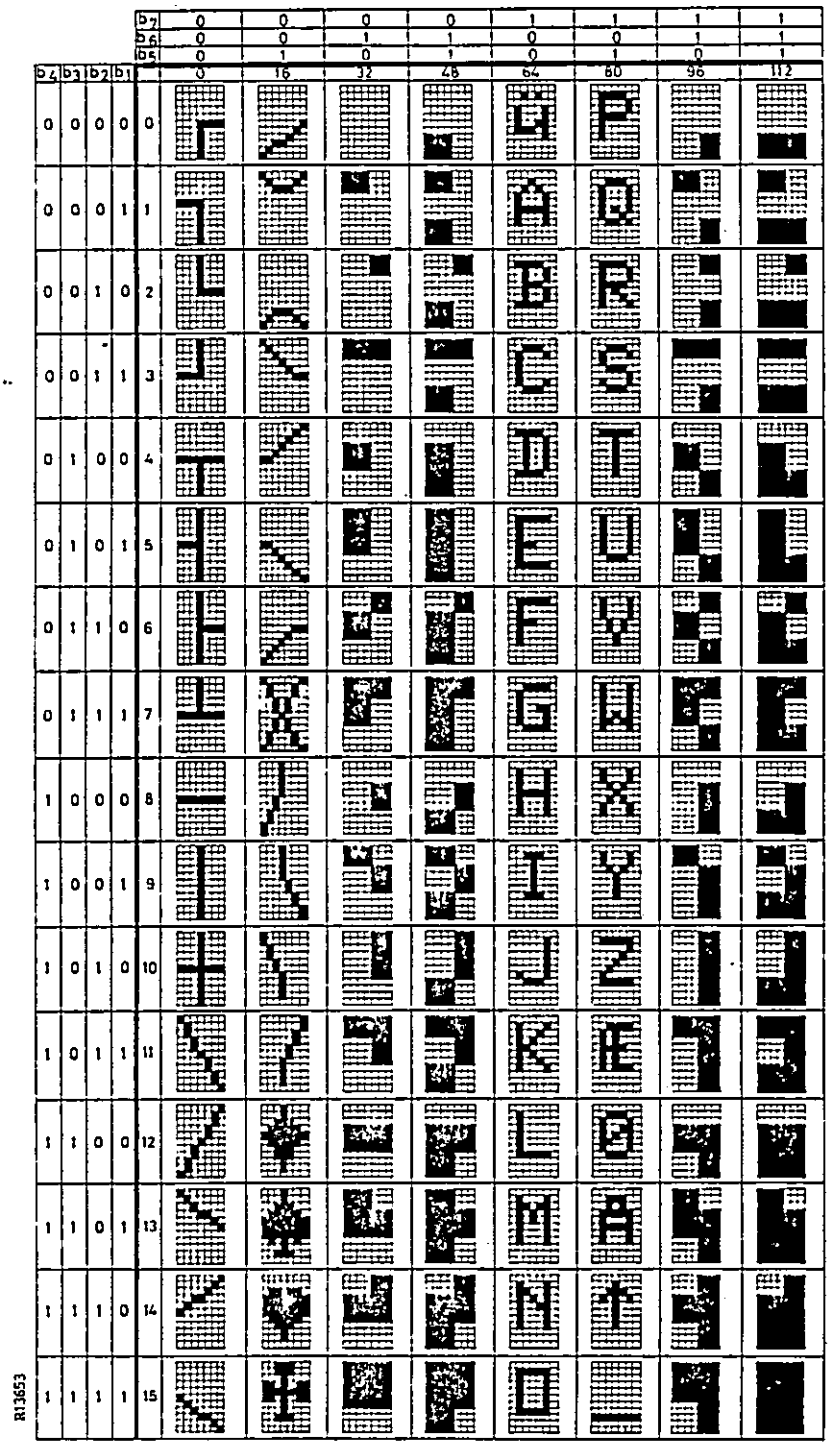


Figure 36: Semigraphic Character Generator (ROA327).

3. CABINET AND POWER SUPPLY 3.

3.1 KBN702 & POW739 3.1

Fig. 37 shows the cabinet KBN702 with the power supply POW739 mounted. The cabinet itself contains transformer, blower, mains connection, rectifier unit RC702, and the internal cable.

Fig. 38 shows the cabinet with MIC702 mounted.

Fig. 39 shows diagram for rectifier unit (REC702) and transformer, blower, and mains connection.

Fig. 40 shows the internal cable in the KBN702.

Fig. 41 shows the cables connection KBN702 to MIC702 and POW739.

Fig. 42 shows the power cable CBL440.

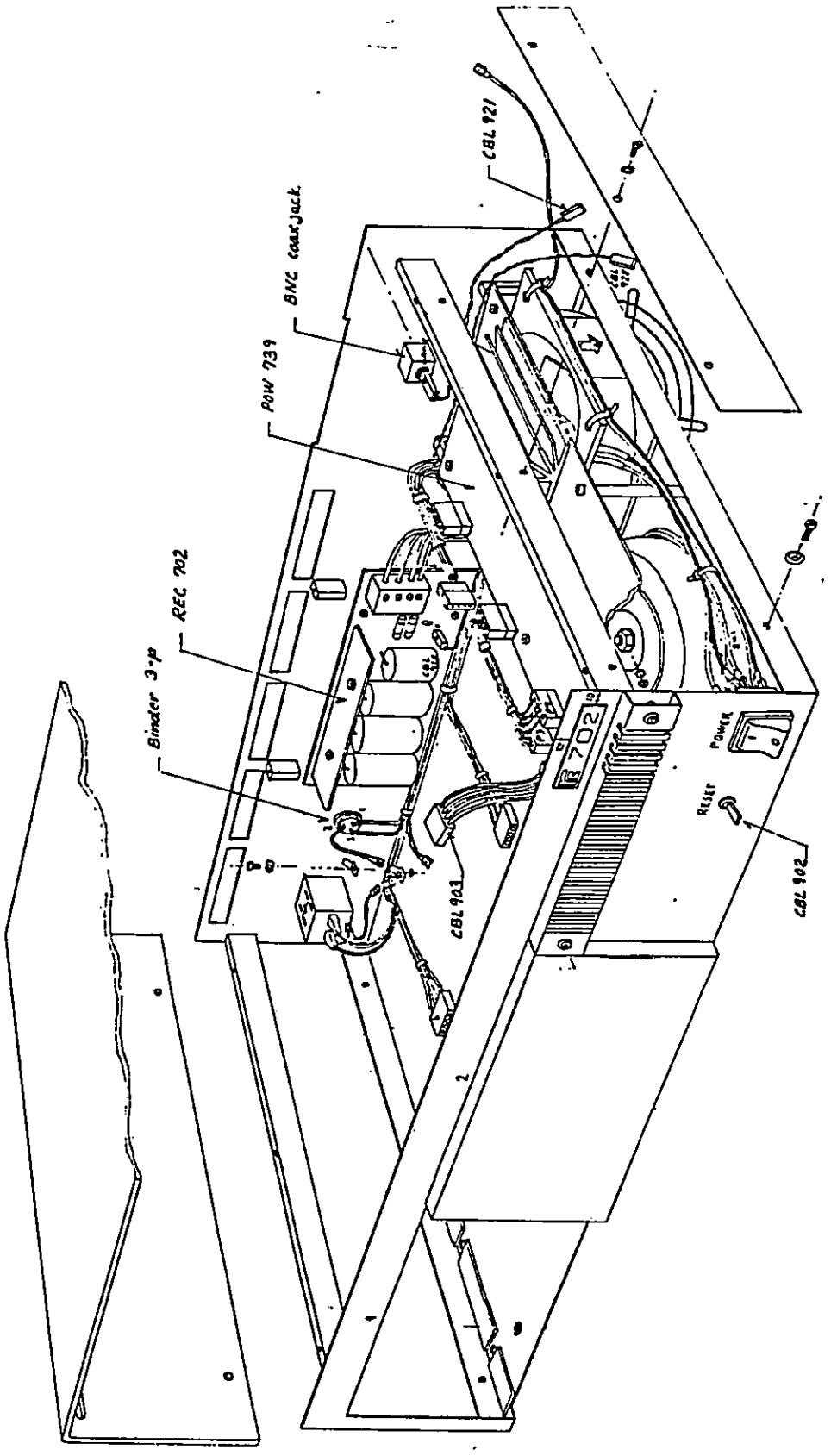


Figure 37: KBN702 & POW739; assembly drawing.

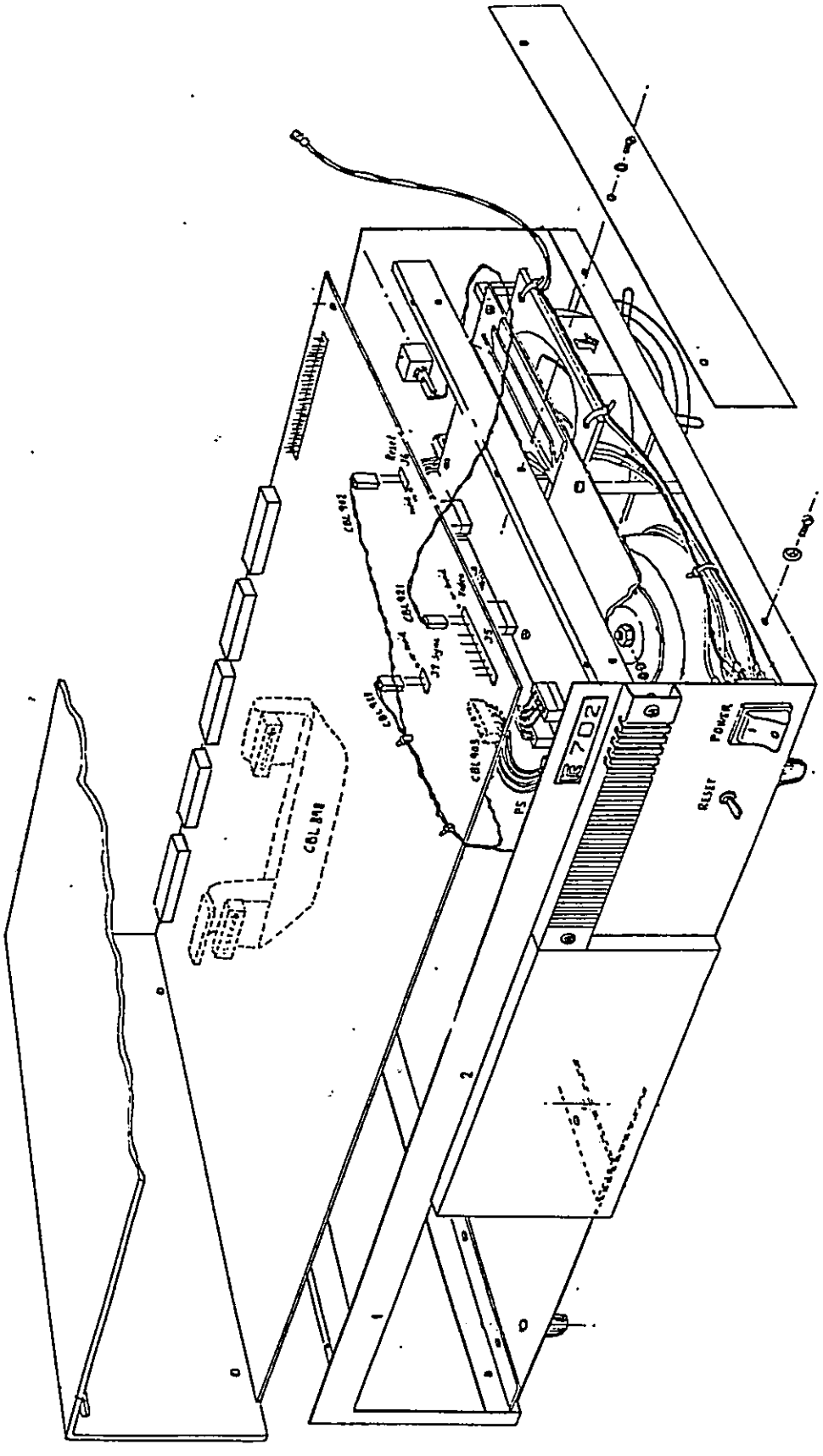


Figure 38: KBN702 & MIC702; assembly drawing.

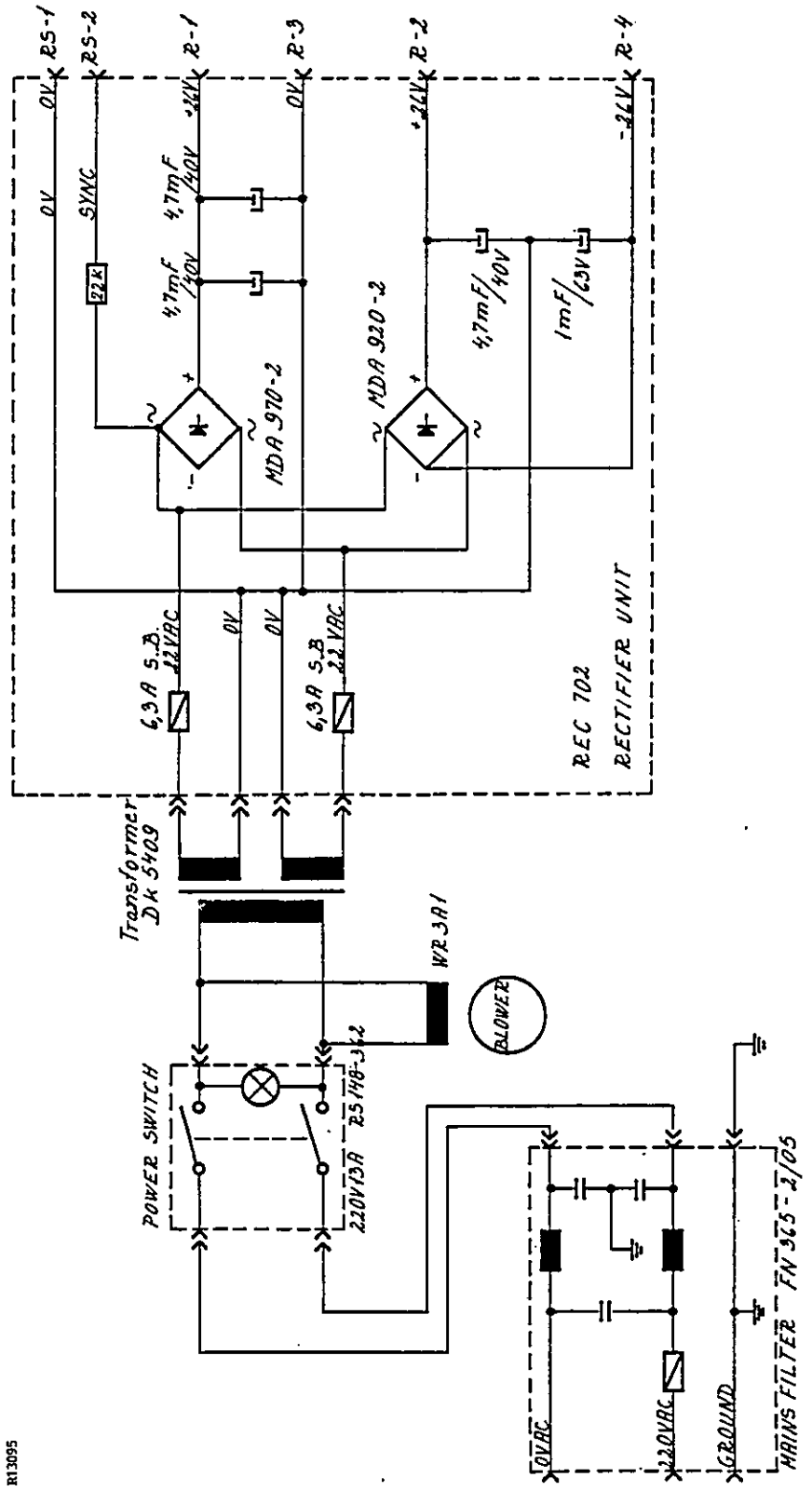
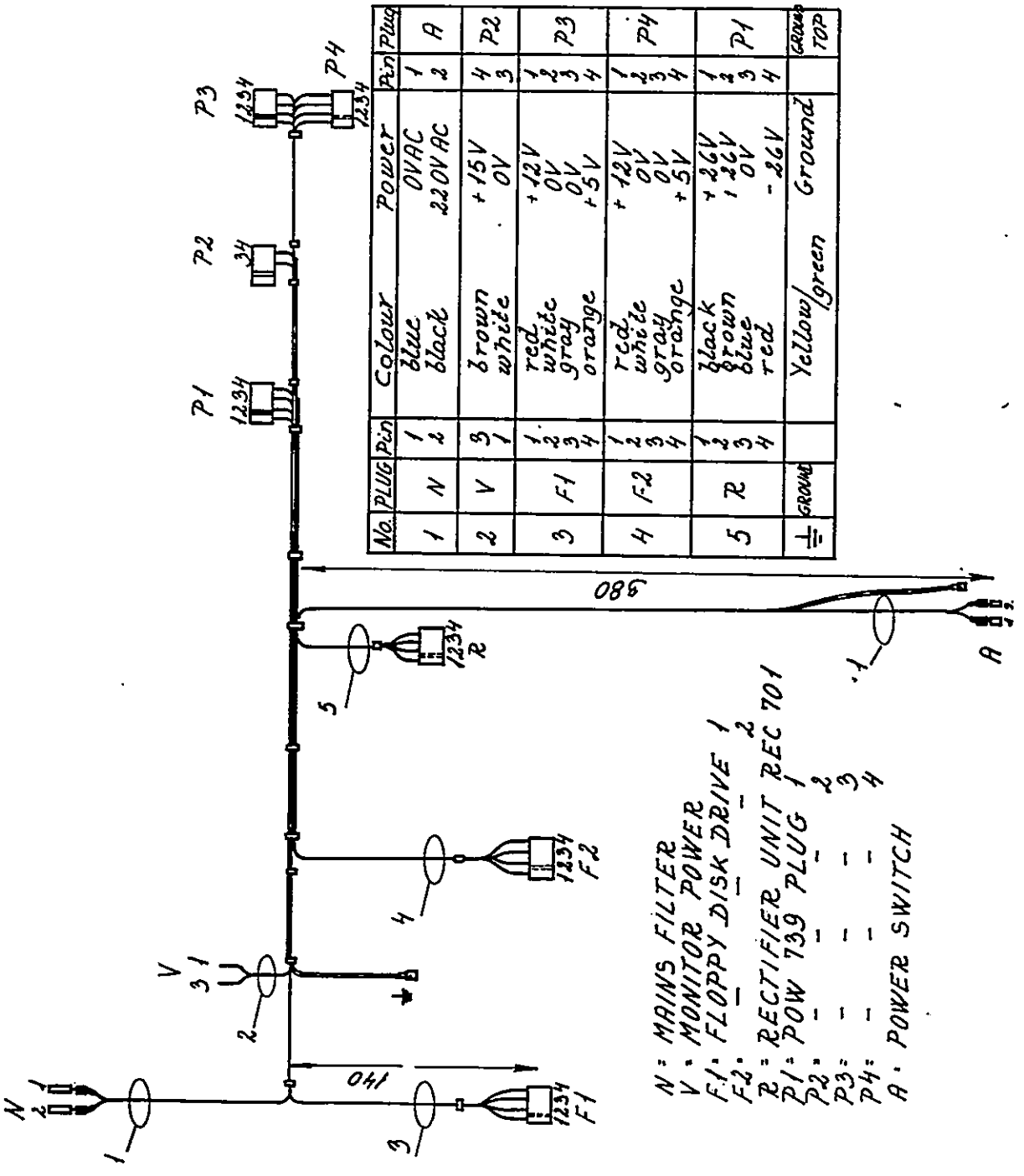


Figure 39: KBN702; filter, transformer, blower and rectifier unit.



No.	PLUG	Pin	Colour	Power	Pin	Plug
1	N	1	blue	0VAC	1	A
		2	black	220VAC	2	
2	V	3	brown	+15V	4	P2
		1	white	0V	3	
3	F1	1	red	+12V	1	P3
		2	white	0V	2	
		3	gray	0V	3	
		4	orange	+5V	4	
4	F2	1	red	+12V	1	P4
		2	white	0V	2	
		3	gray	0V	3	
		4	orange	+5V	4	
5	R	1	black	+26V	1	P1
		2	brown	+26V	2	
		3	blue	0V	3	
		4	red	-26V	4	
⏚	GROUND		Yellow/green	Ground		GROUND TOP

Figure 40: KBN702; internal cables.

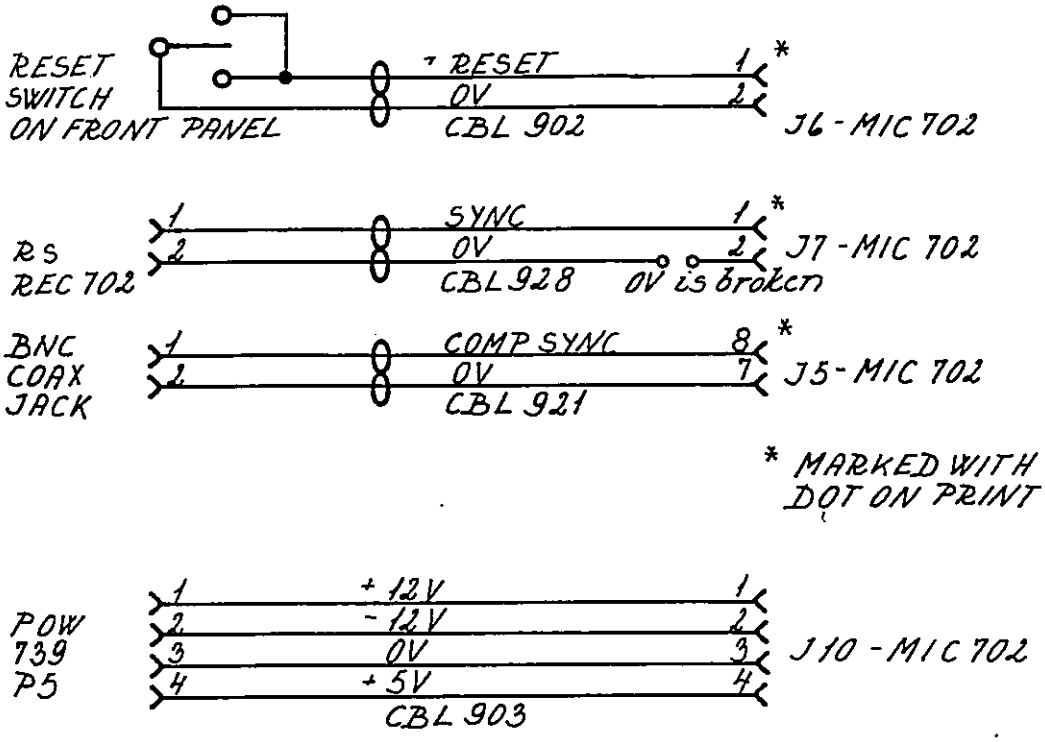


Figure 41: KEN702 & MIC702 & POW739; cable connections.

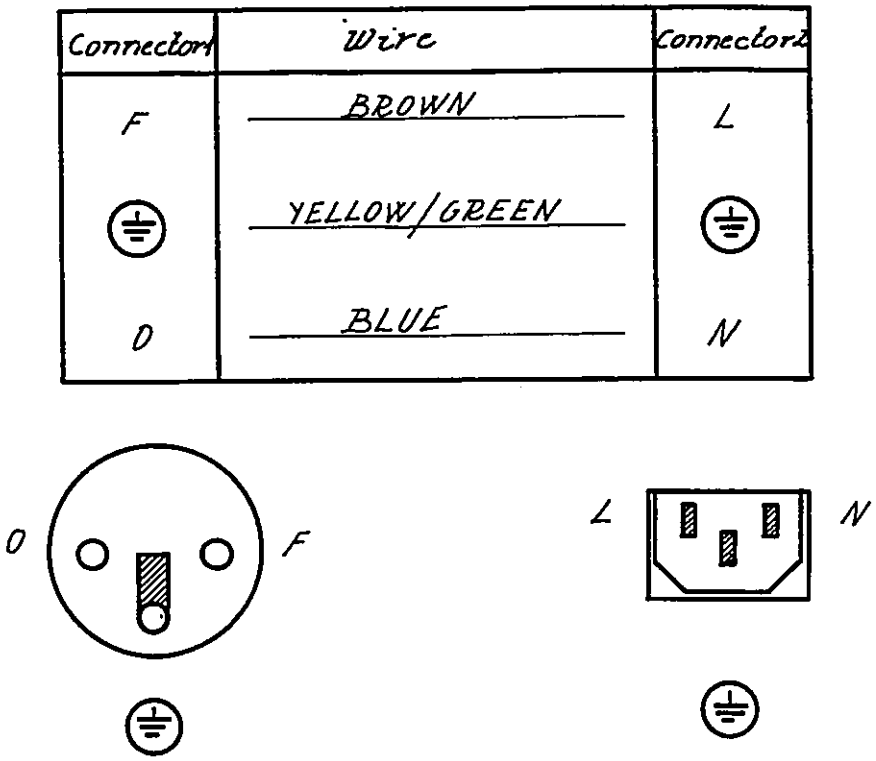


Figure 42: CBL440 - Power Cable.

3.1.1 POW739

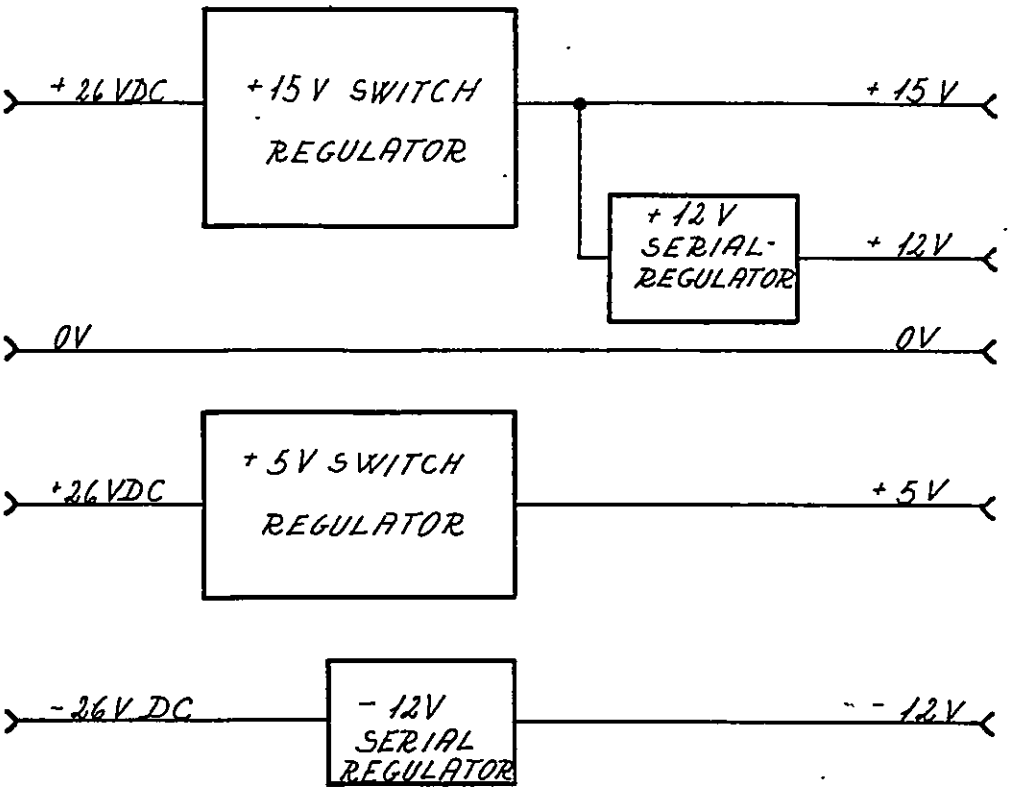
The power supply to RC702 is built on a single printed circuit board. Fig. 43 shows a block diagram for the POW739.

Input to the power supply is +26 V DC and -26 V DC delivered from REC702 rectifier unit. This unit is described in section 3.1

Fig. 44 shows the layout of the printed circuit board.

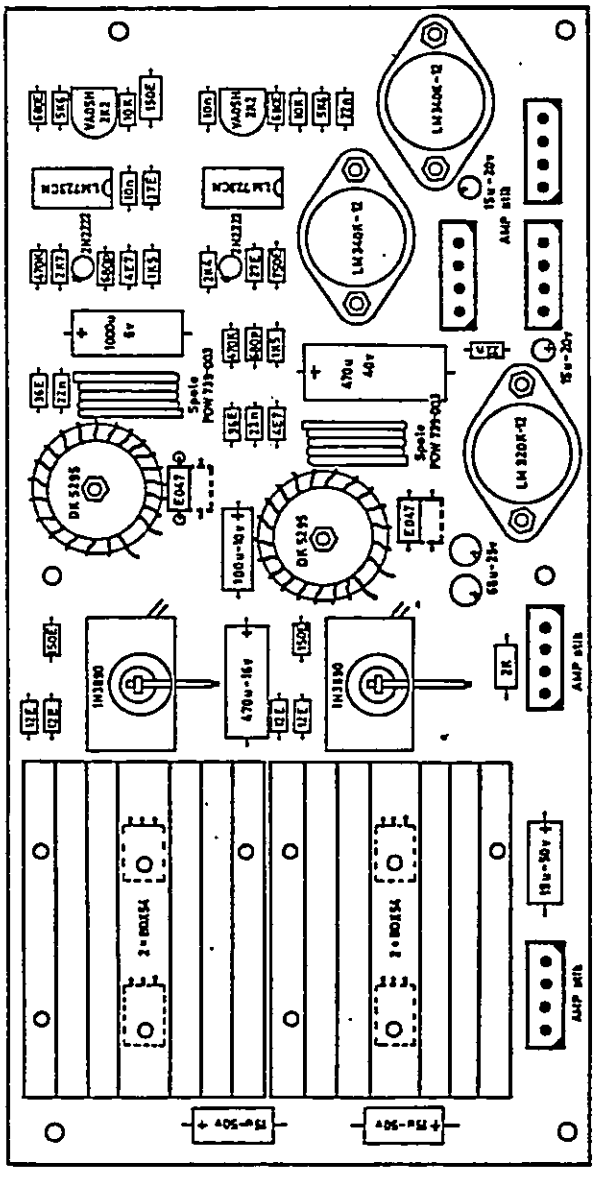
Fig. 45 and fig. 46 show the circuit diagram for the unit.

Fig. 47 and fig. 48 show the timing diagram for the unit.



V OUT	IMAX	ΔV MAX
+15V	1,4A	± 0,5V
+12V	2,6A	± 0,5V
+5V	5,0A	± 0,1V
-12V	0,2A	± 0,5V

Figure 43: POW739; block diagram.



P5 to MIC 702
MICRO PROCESSOR

P3, P4 to RC 761
FLOPPY DISK DRIVE

P2 to RC 752
VIDEO MONITOR

P1 from REC 701
RECTIFIER UNIT

Figure 44: POW739; layout.

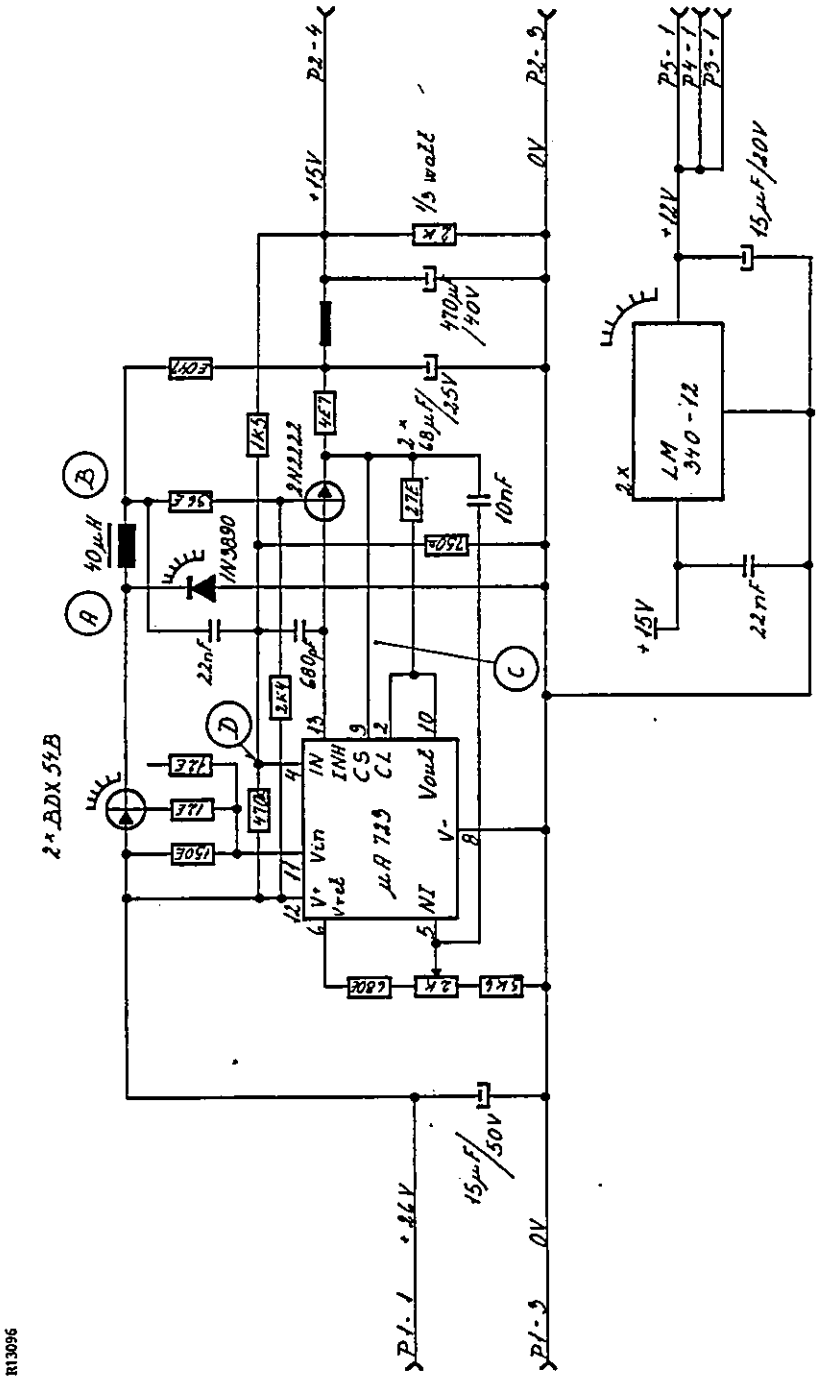


Figure 45: POW739; +15 V and +12 V power supply.

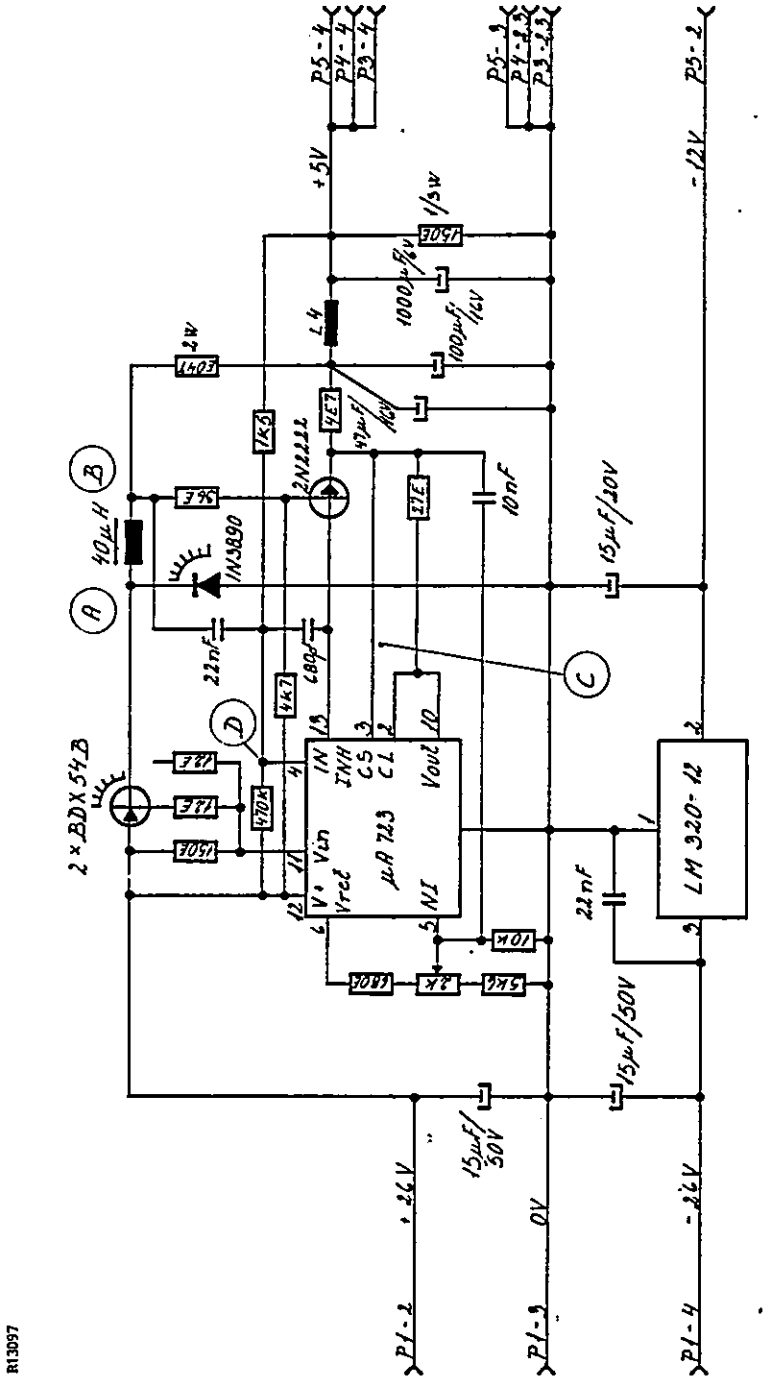


Figure 46: POW739; +5 V and -12 V power supply.

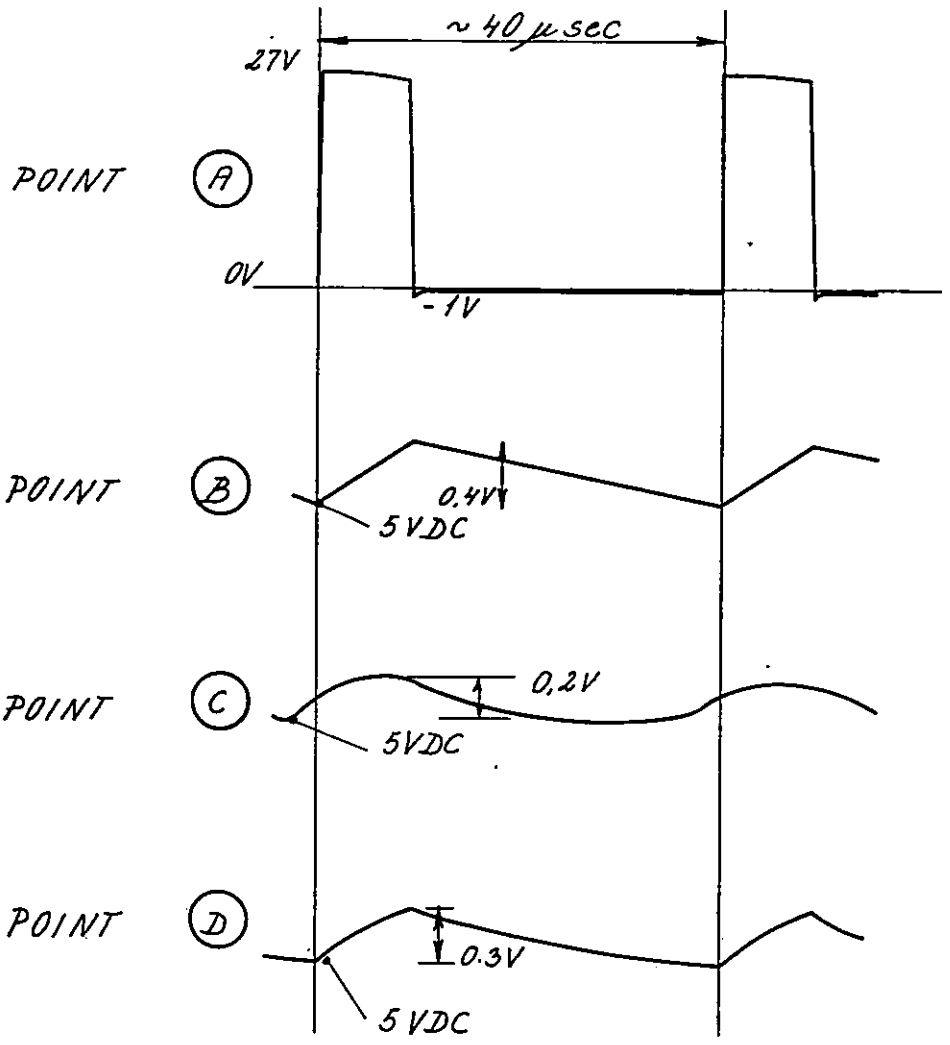


Figure 47: POW739; +5 V supply; timing diagram; load: MIC702 & one mini floppy.

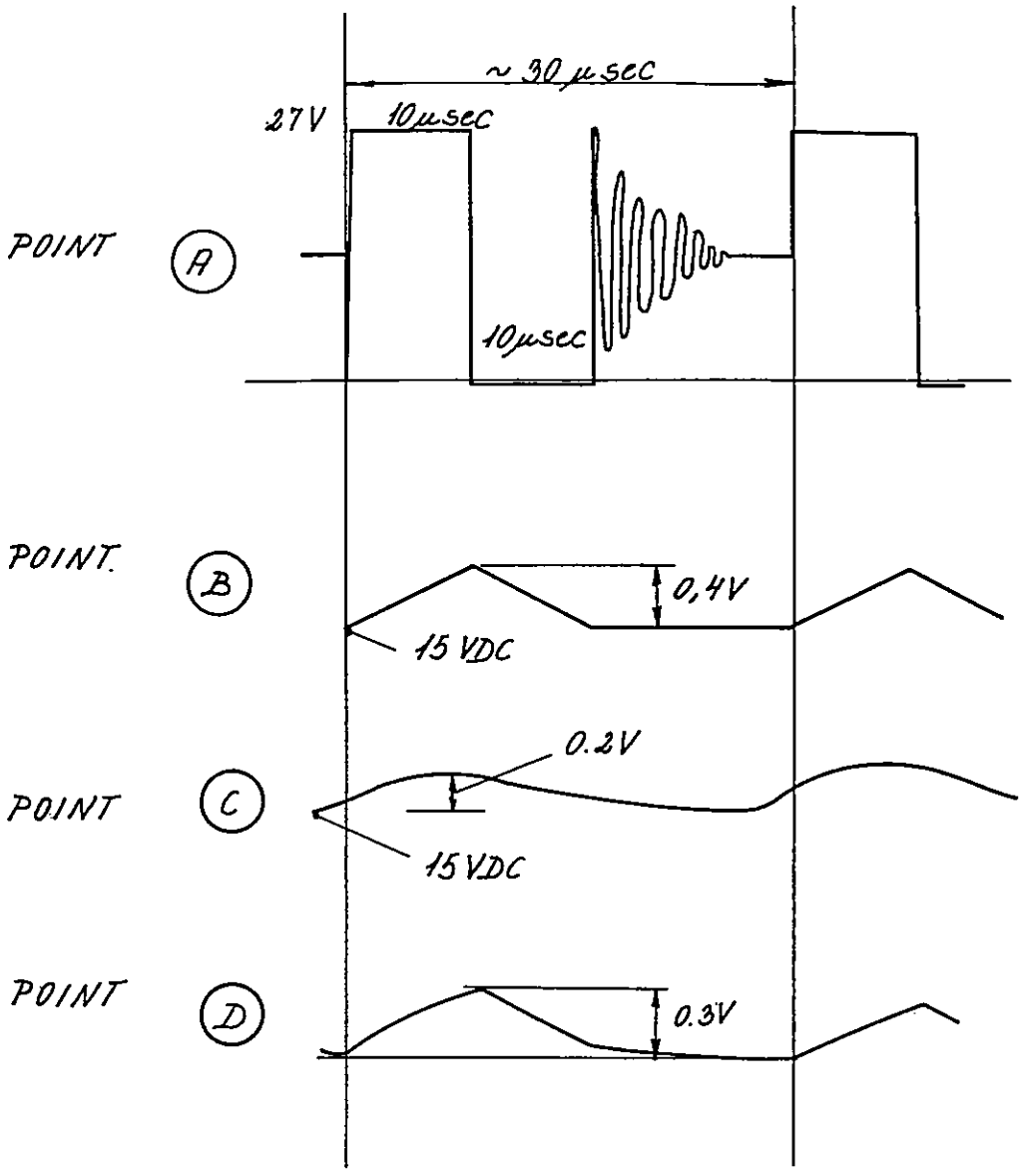


Figure 48: POW739; +15 V supply; timing diagram; load: MIC702 & one mini floppy & video monitor.

3.2 KBN705 & POW746 3.2

KBN705 is the second version of the cabinet and is used in both RC702 and RC703 systems. The microcomputer board is mounted the same way as in KBN702.

The main improvements of KBN705 are:

1. Contains new power supply (POW746) with reduced magnetic radiation.

2. Rectifier unit (REC701) not used.

3. Fan Regulator Circuit which reduces the acustic noise produced by the fan.

4. Internal cabling simplified.

5. Reset Switch in new position.

Fig. 49 shows the internal cables in KBN705.

Fig. 50 shows the cables which connect KBN705 to the microcomputer board and to the floppy disc drives, etc.

Notes to fig. 49.

No.	PLUG	PIN	COLOUR	Signal/Power	Pin	PLUG
1	J5	2	Red	+15V	3	MP
		3	Black	0V	1	
2	TS	1	Green	24VAC		transf.
		2	Red	0VAC		
		3	Brown	0VAC		
		4	Blue	24VAC		
3	J2	1	Brown	+12V	1	MB
		2	Brown	-12V	2	
		3	Brown	0V	3	
		4	Brown	+5V	4	
		5	Gray	Sync.	1	SMB
8	Mains		Brown	220VAC	8	Power switch
9	Filter		Blue	0VAC	9	in
10	Power		White	220VAC	10	To FAN REG.
11	switch		Gray	0VAC	11	CIRCUIT and transformer
12			Yellow/	Ground		12
13			green	Ground		13

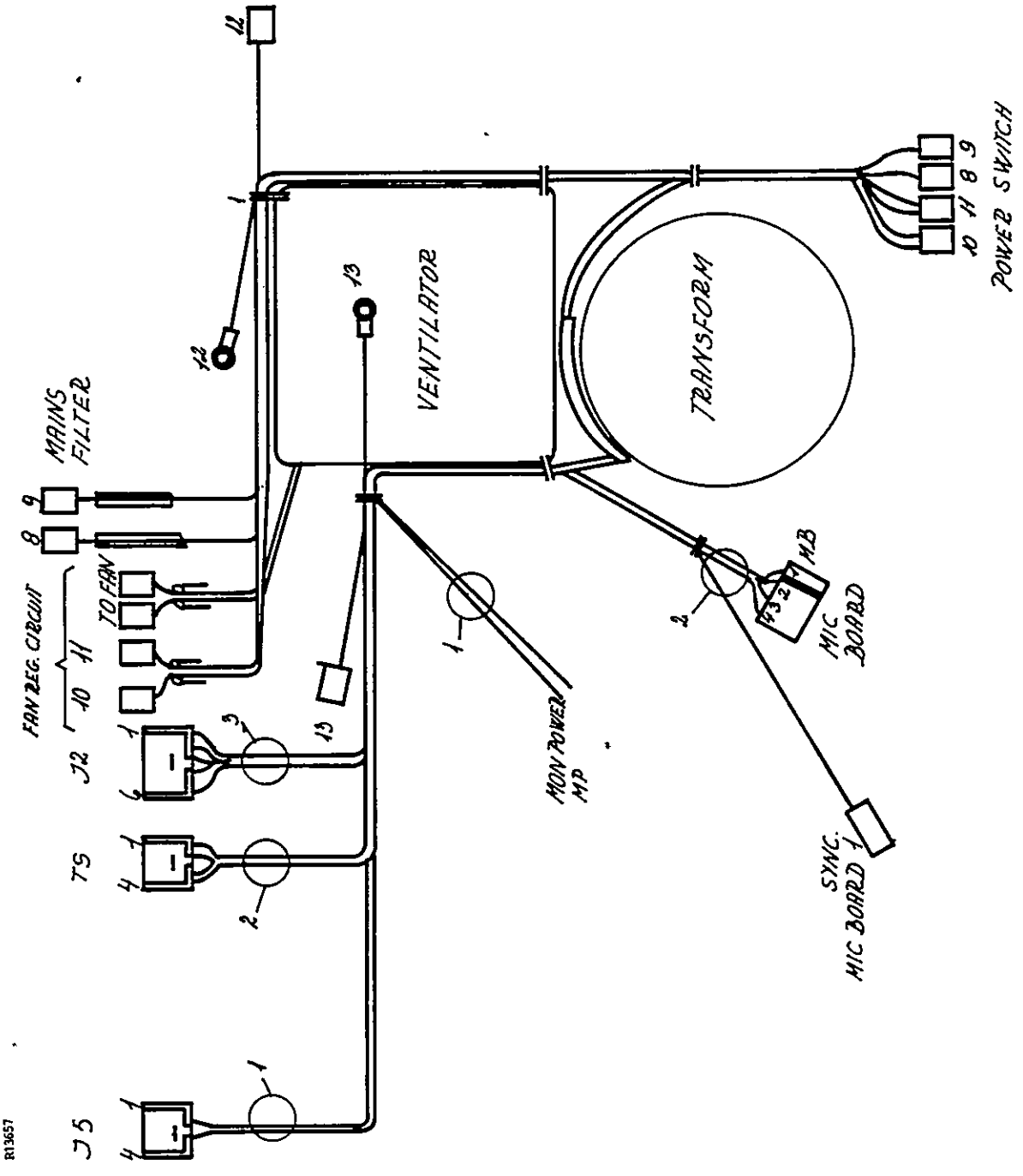


Figure 49: KBN705; internal cables.

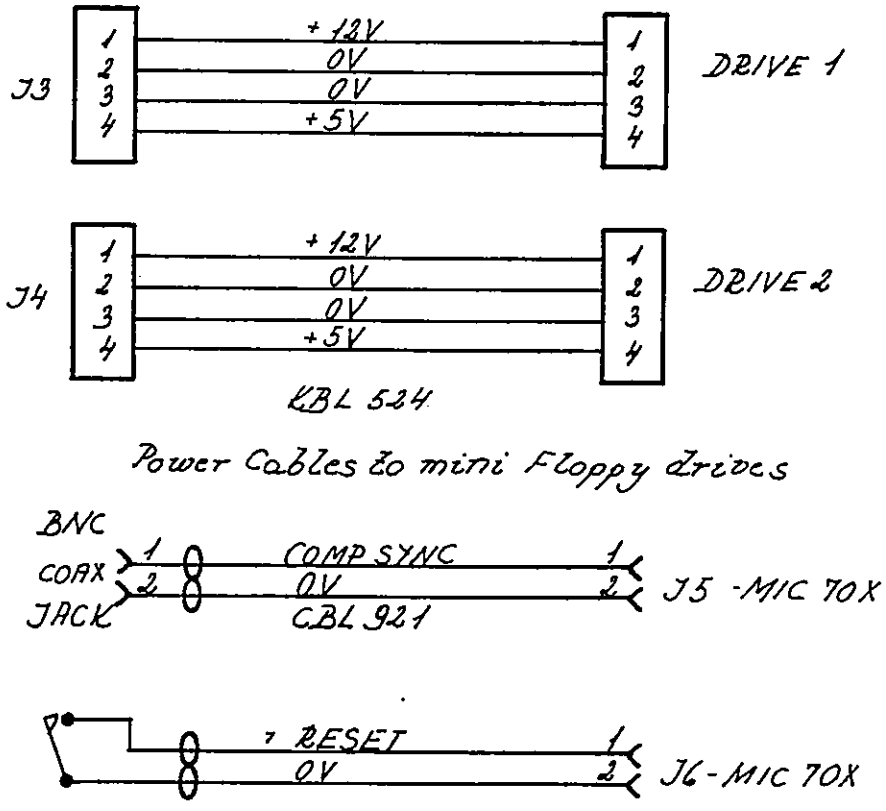


Figure 50: KEN705; cable connections to MIC70x and Floppy Disc Drive.

3.2.1 POW746 3.2.1

The POW746 - Power Supply is built on a single print board.

Fig. 51 shows the block diagram for the power supply, including the input/output connections. Input is 2x24 V AC which is supplied by the transformer (DK7755) housed in KEN705.

Fig. 52 gives the specifications for POW746 and transformer (DK7755).

Note: Input voltage range covers both Continental Europe and United Kingdom.

Fig. 53 shows the POW746 Layout.

Fig. 54 shows the Circuit diagram for POW746.

Fig. 55 shows the timing diagram for POW746.

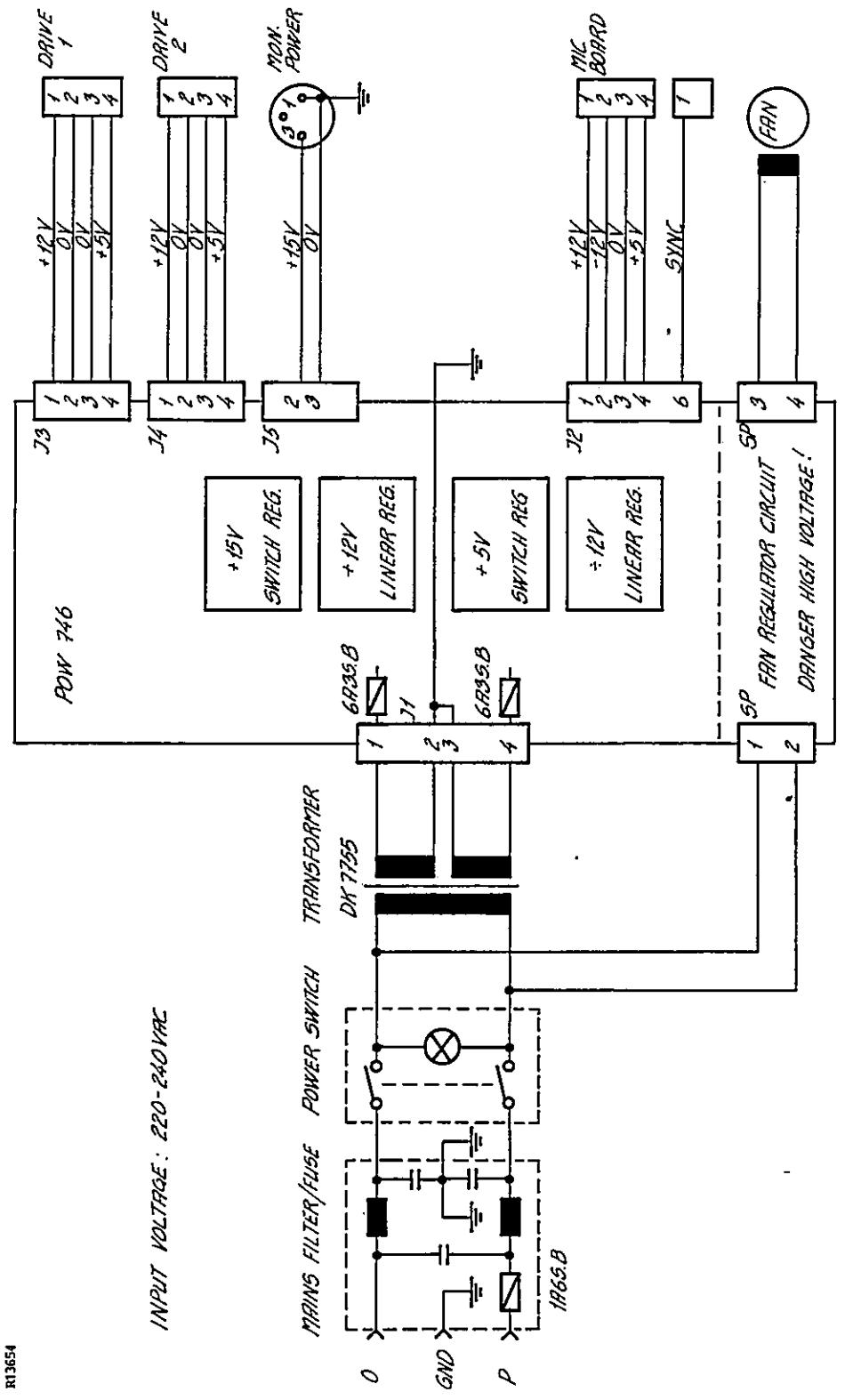


Figure 51: POW746; block diagram.

Input voltage: 220 V - 240 V ± 10%, 50 Hz

Power consumption: Max. 150 W

Output voltages:

V out	V out	V ripple	I max
+15 V	± 0,5 V	<100 mV_{pp}	1,4 A
+12 V	± 0,5 V	< 50 mV_{pp}	2,6 A
+ 5 V	± 0,5 V	< 50 mV_{pp}	5 A
-12 V	± 0,5 V	<100 mV_{pp}	0,2 A

Fan regulator range: ~ 0-1600 rpm.

Figure 52: POW746; power specifications.

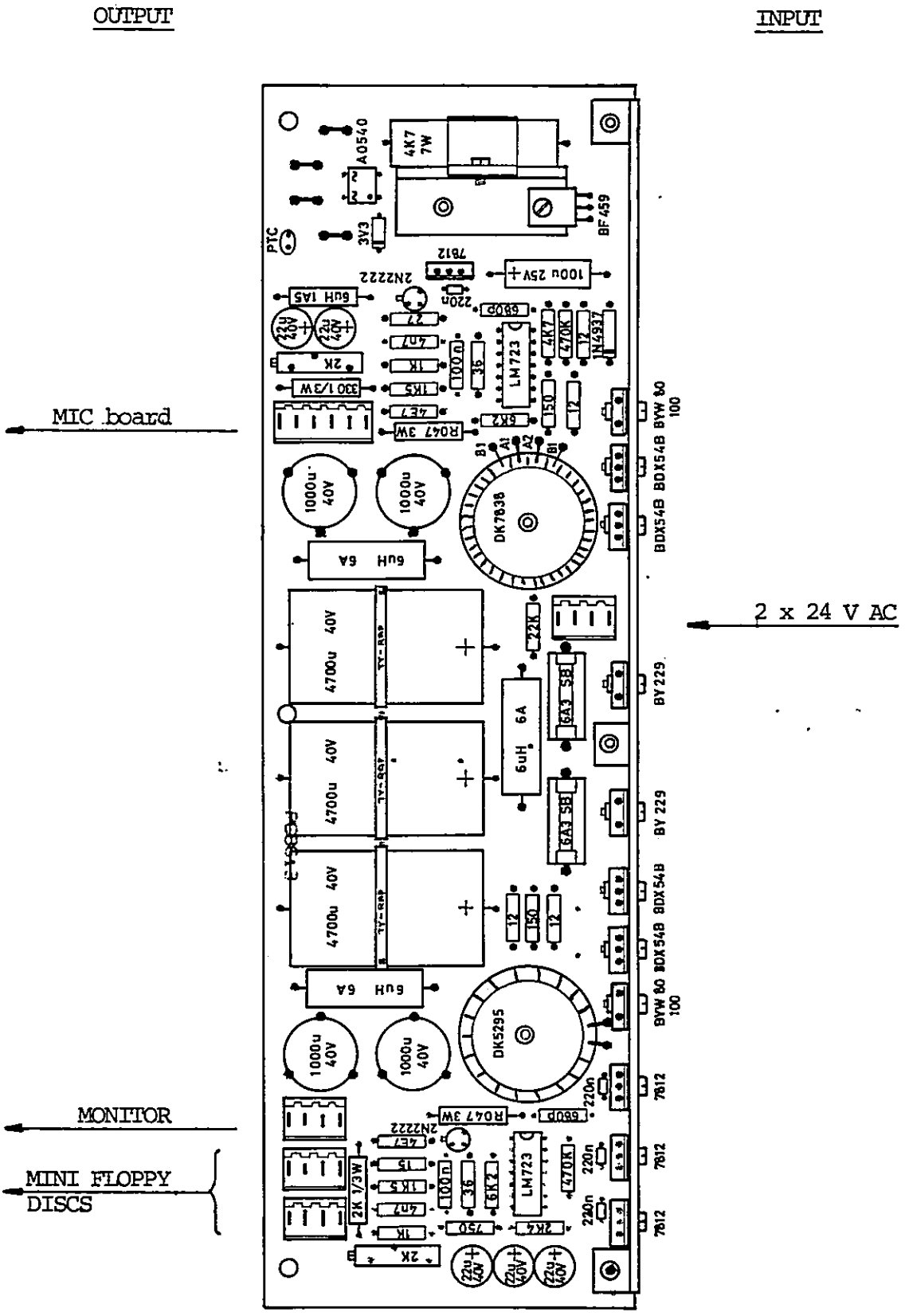


Figure 53: POW746; layout.

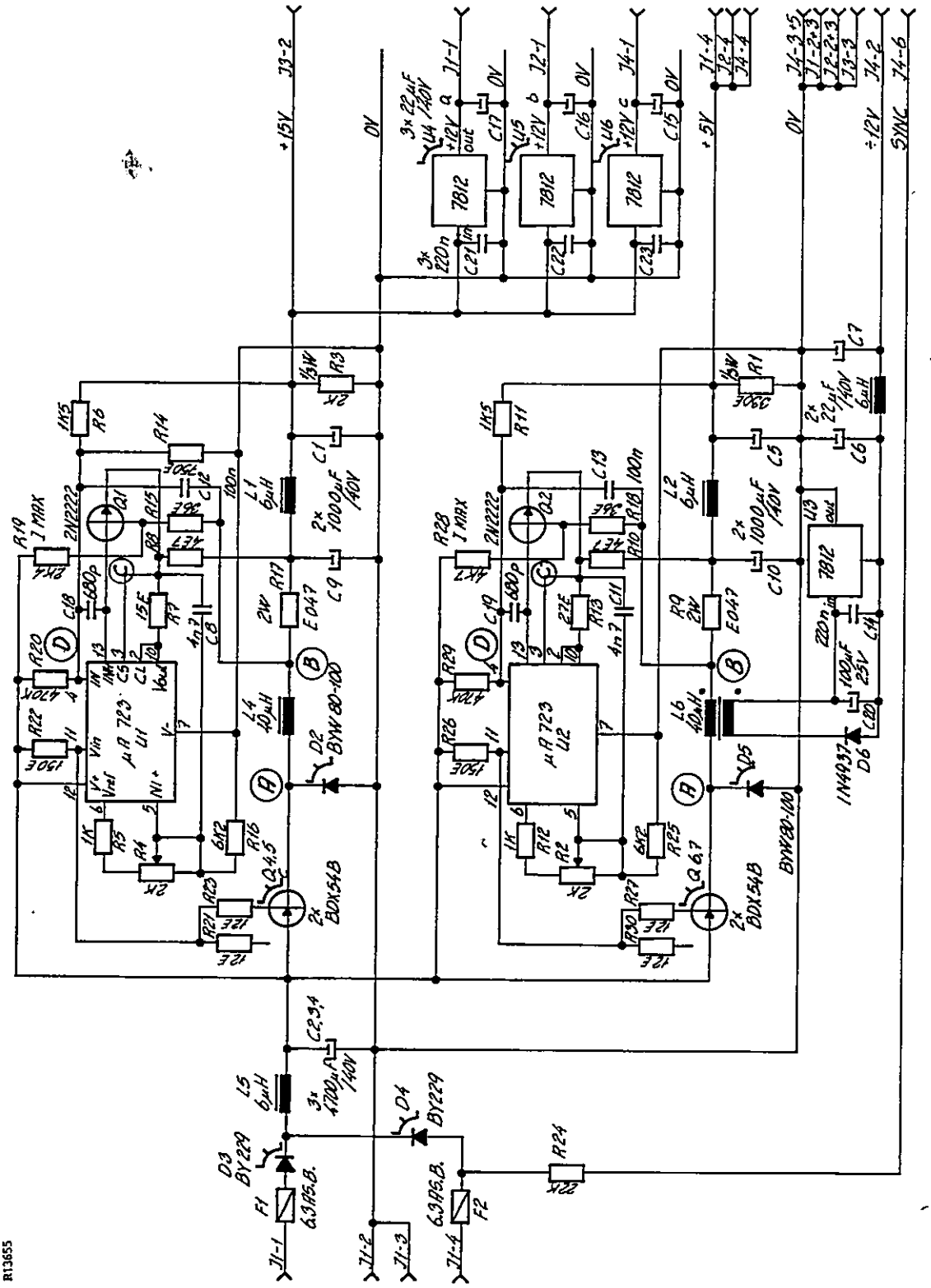


Figure 54: POW746; schematic diagram.

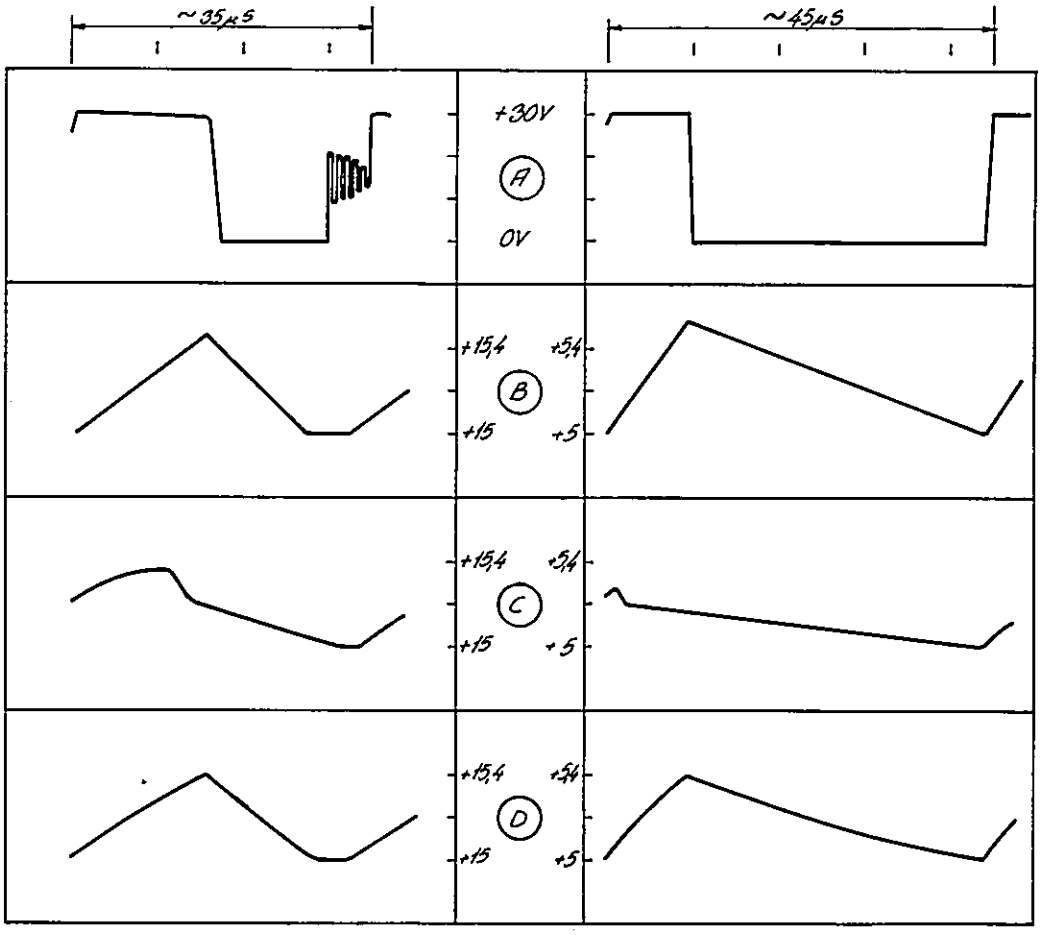


Figure 55: POW746; timing diagram.

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