RCSL No: 44-RT2060

Edition: March 1983

Author: Steen Nørgaard

Title:

RC703 Built-in Testsystem
Version 1.0
User's Guide

RCSL No 42-I 2164

A/S REGNECENTRALEN
af 1979

Keywords:

RC703, Built-in testprograms.

Abstract:

This manual describes the built-in testsystem and the test programs for the RC703 Piccolo. The test programs described in this manual are: the memory test, the DMA test, the CTC test and the FDD test.

(22 printed pages)

Printed by A/S Regnecentralen af 1979, Copenhagen

RCSL No 42-I 2164

TABLE OF CONTENTS PAGE

1. INTRODUCTION

This manual describes the built-in diagnostic test programs for the RC703 microcomputer.

The test programs are testing the basic functions of the different parts of the hardware in the computer.

The sequence of the different test programs in the test system is organized with rising complexity. As far as possible, no part of the hardware is used before it is tested.

1.1 Load and Start

Starting the built-in selftest system:

- after pushing reset button pushing "T" on the keyboard will force the program control to the built-in testsystem.

The testsystem tests the hardware which has connection to the flexible disk drives. The tests are: RAM test, DMA test, CTC test and FDD test.

2. THE TESTS

2.

The testsystem described in this manual consists of 4 tests. The tests are ran under control of a testrouter, which has the purpose of administering the mode in which a particular test is ran. The four tests are:

Memory test
DMA test
CTC test
FDD test

3. THE TESTROUTER

The testrouter is a central program which main purpose is to compute the address of the next test in the sequence. The address of the next test is derived from a variable holding the present testnumber and normally incremented by one. Every time a test has finished and is not in looping mode, the testrouter is entered.

3.1 Switch Parameters

The variable holding the test number also contains four switch bits, by which the testrouter decides how to administer the tests.

7	6	5	4	3	2	1	0
				test No			

h	l	k	s
a	o	e	u
l	o	y	p
t	p	b	r
		.	.
		o	p
		n	r
			i
			n
			t

halt: 0: halt on error
1: proceed though error

loop: 0: sequential, big loop of all tests
1: looping in the present test

keyb on: 0: the system has not been informed about an installed keyboard
1: a key on the keyboard has been struck at least once

supr print: 0: messages are printed on the display
1: no messages are printed (usable for fast looping)

Initial values of the switch parameters are all zeroes.

3.2 Keyboard Management 3.2

To enter the keyboard management is only possible when a strucked key has informed the system that a keyboard is connected. When this has happened, the testrouter answers with the valid capital letters and digits.

Valid keys are as follows:

H: set halt bit to 0
R: set halt bit to 1
L: set loop bit to 1
G: set loop bit to 0
S: set suppress print bit to 1
P: set suppress print bit to 0
(Please note that capital letters are used)

<esc>: will stop execution.

This is also the fact for any other key. Striking the <return> key will have the test system reentering the looping or running state.

Numbers between 0-F will insert a new test number into the variable.

All other keys will give no response.

If one for example wants to loop in test 6 and not go into a HALT state if error, then strike the keys R, L, 6 (not necessarily this sequence). Furthermore if one wants to test fast for measuring purpose, one can suppress print by typing S. Suppress print means that nothing from now on will be written into the screen-buffer.

Relationship between the test numbers and actual tests is as follows:

Test No	Test name
0	PROM checksum and RAM test
1	DMA test
2	CTC test
3	FDD test
4	not used
5	not used
6	not used
7	not used
8	not used
9	not used
A	not used
B	not used
C	not used
D	not used
E	not used
F	not used

The test numbers not used yet will force the test system to return to test number 0.

3.3 Output 3.3

The testrouter will respond with some output. This is a version data and a test number. It also responds with the state of the test. This could be either running, stopped, looping or halted.

3.4 Specialities 3.4

The testrouter has a waiting point of 3 seconds when entered from the test number 0 to give the user time to key in some input to change parameters.

4. THE MEMORY TEST 4.

The memory test consists of two tests. A PROM checksum test and a RAM test.

4.1 PROM Checksum Test 4.1

A check on the contents of the PROM (containing tests) is performed by adding the contents of all locations in the PROM and checking that the result is FF (Hex).

If a difference from FF (Hex) is found, an attempt is made to write an error message on the first line of the display.

The error message has the following layout:

<RC703 TESTSYSTEM chksum err>

4.2 RAM Test 4.2

The memory test thereafter performs a test of the dynamic RAM memory. Of course, all memory cells are tested by the memory test (all variables are kept in CPU registers).

First the upper part (addresses higher than the last PROM address) of the memory is tested. If this was found OK, the test is moved to this memory area and the memory space shaded by PROM is tested.

The test pattern for the dynamic RAM memory consisting of chips of 1 bit x 16 k is three times 00 followed by three times FF (Hex). When all memory cells have been tested, they are again tested with the inversed pattern. This means that all bits are tested for "zero" and "one" insertion. It is the most convenient pattern for discovering addressing errors because this modulus 3 pattern will not be repeated equivalent in a higher modulus address.

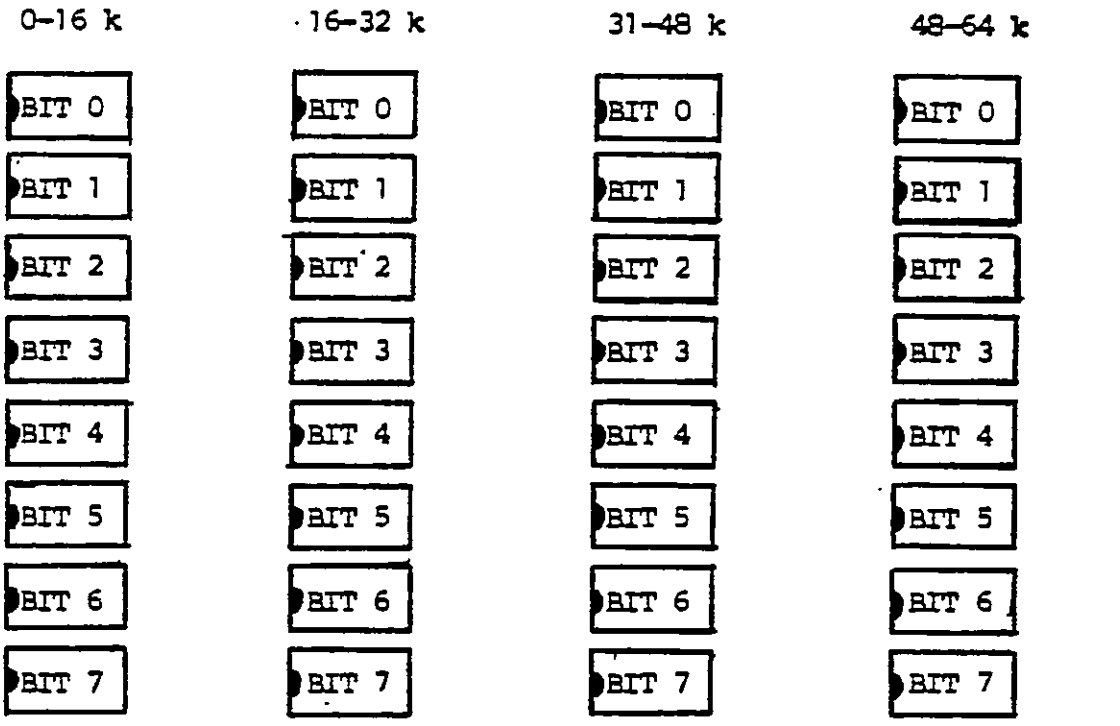
If an error occurs, a message will be written on the first line of the display. The layout is the following:

<RC703 TESTSYSTEM mem err ha la ex re>

where "ha" is high address, "la" is low address, "ex" is expected value and "re" is received value. All numbers are in hexadecimal notation. (To find any defective chip, consult fig. 1).

When both the PROM checksum test and the RAM memory test are terminated, an attempt is made to write on the display (whether there has been an error or not). This is done as simple as possible without any standard program (without interrupt service). On the first 17 positions of the first line, the identification of the system type will be written followed by a possible error message.

The total turn around time for the RAM test is 7.5 seconds.



0 0 0 0 3 F F F	0-16 k
4 0 0 0 7 F F F	16-32 k
8 0 0 0 B F F F	32-48 k
C 0 0 0 F F F F	48-64 k

Figure 1: Layout of 64K RAM memory.

5. DMA TEST

The DMA test loop is testing DMA transfers between channel 0 and channel 1. This is done as a memory to memory transport. Channel 1 is receiving and channel 0 is transmitting.

When the transport is finished, the receiving buffer is checked against the transmitted buffer byte by byte.

The DMA test will write its messages on the fifth line of the display.

Apart from the identification of the test, the possible messages from the DMA test are:

<OK>
<TC timeout 200 ms>
<data error, byte no: xx xx exp: xx rec: xx>

All numbers are in hexadecimal notation. "TC timeout ms" shows that the terminal count bit for channel 1 in the DMA status register has not been set within 200 ms. and that the transport is therefore not successful.

The transmitted pattern is a buffer of 1 k containing a counting pattern. The pattern is as follows: 00 FF FE FD etc. repeated 4 times.

6. CTC TEST

6.

This program is testing the counter timer circuit which is used for baud rate generator and as interrupt circuit for the CRT and the FDC controller.

It is tested that the circuit will generate interrupt and that the vector (interrupt address) is correct.

The four channels 0, 1, 2 and 3 are tested. Channels 0 and 1 are tested in counter mode, counting on the fixed input clock giving interrupt after approx. 423 µs. Channels 2 and 3 are tested in timer mode. The timer is for channel 2 started by the interrupt signal from the CRT controller. For channel 3 the timing is started automatically.

The test is based on a timeout loop, so it is checked if the interrupt was received within a specified time (300 ms.). It is also checked that only the specified channel interrupts.

The test can end up with 2 different error messages:

<illegal interrupt, port: xx>
meaning that another channel than the specified has interrupted.

<no interrupt, ch:>
meaning that the test has timed out before interrupt was received.

Texts will be written on the sixth line of the display.

7. FDD TEST 7.

This test is testing the flexible disk controller and up to four connected drives, either 8" or 5 1/4". It is not a complete test of the flexible disk, but rather a fast verification of the basic functions of the controller and the drives connected to it.

The test has to be selected by its number (3). The test does not write on the diskette.

Please note that before the FDD test is entered, a writeable diskette should be placed in the drive. For diskette stations connected to an RC703 Piccolo, it is recommendable only to use properly formatted diskettes of the type dual head, double side, soft sector, double density with the format 15 sectors/512 bytes on 8" diskettes and 10 sectors/512 bytes on 5 1/4" diskettes.

The test will initialize the controller to a step rate time of maximum 6 ms., a head unload time of maximum 160 ms. and a head load time of maximum 40 ms.

When the testing is initiated, the units which are ready, will be recalibrated. If no units are ready, the text <* all drives: not ready> will be written, and the test enters an idle state. Whenever a unit changes its state from not ready to ready, the testing will start on this unit.

If minidrives are used, the test will use some seconds to find out the drives which are ready.

Because of the READY signal when the drives are 5 1/4" diskette drives, they are only asked one time, if they are ready or not. This is done by trying a recalibration of the drives. Once a drive has been known ready or not, the testprogram expects it to be in this state throughout the test, also in looping. Every drive connected to the system is tested.

The testing sequence for a unit is first a recalibration and then the cyclic sequence, seek, read. Not the complete diskette is tested, but only the following 16 tracks are used for data re-

covery checkout:

For 8" units: 1, 66, 2, 65, 3, 64, 8, 40, 63, 9, 62, 36, 61, 37, 38, 39.

For 5 1/4" units: 1, 79, 2, 78, 3, 77, 20, 34, 76, 21, 75, 35, 74, 36, 60, 59.

The sector number varies from 1 throughout 9. On the first track the data checkout will be performed on sector 1, on the second track on sector 2 and so on.

The test pattern written on the diskette is a counting pattern of 512 bytes, which is transferred via the DMA controller channel 1. When the data is read from the diskette, it is placed in a buffer in the memory, and the write- and read-buffers are compared.

When the test is in loop mode, each byte of the test buffer is incremented by one for each pass.

It is possible that a recalibration error is detected the first time the FDD test is run. It may be due to the fdc.

If an error is detected one of the following errortexts till be written.

7.1 FDD Test Error Messages 7.1

<*fault in main status reg>

Indicates an error in the controller main status register bit 7 or 6.

<not ready>

Indicates that the ready state for a specified drive has been set to not ready (bit 3 of status register 0).

<timeout>

The specified drive has not responded to an operation with an interrupt within approx. 2 s.

<*fault in fdc xx>

Indicates that the status bits of status register 0 are in an invalid state. xx is a hexadecimal number showing the contents of this register.

<seek error>

The drive could not find the specified track of the command issued (bit 5 of status register 0).

<command abort>

The command issued was invalid. The command was never started. It will appear if an earlier command was not terminated correctly (bit 7 = 1 and bit 6 = 0 of status register 0).

<door open>

The drive door has been opened during execution.

<recalibrate error>

The seek end bit did not occur after a recalibrate command (bit 5 of status register 0).

<track 0 signal not found>

The track 0 signal fails to occur after 77 step pulses (bit 4 of status register 0).

<missing address mark in datafield>

No address mark in the datafield (bit 0 of status register 2).

<missing address mark in id-field>

No address mark is detected in the id field (bit 0 of status register 1).

<bad cylinder>

The contents of the cylinder number on the medium are different from the internal register and cylinder number appears to be FF Hex (bit 1 of status register 2).

<wrong cylinder>

The contents of the cylinder number on the medium are different from the internal register (bit 4 of status register 2).

<cannot find sector>

The controller cannot find the sector specified in the internal register (bit 2 of status register 1).

<crc fault in id-field>

The CRC check discovered an error in the id field (bit 5 of status register 1, when bit 5 of status register 2 is zero).

<crc fault in data field>

The CRC check discovered an error in the data field (bit 5 of both status register 1 and 2).

<overrun>

If the controller is not services by the DMA controller within a certain time interval, the error occurs (bit 4 of status register 1).

<access beyond last sector>

The controller has tried to access a sector beyond the final sector of a cylinder (bit 7 of status register 1).

When one of the mentioned error messages, which has relation to a specific drive occurs, a heading is written before the message identifying the drive. The drives are numbered 0 through 3.

Texts will be written on the eighth line of the display.

8. ERROR CODES

The testrouter outputs an error code, which is specific for the type of error discovered on port 50 Hex. This enables the use to run the testsystem on a MIC board alone without display. The error information may then be detected if a device which can decode the numbers is installed on the system bus.

The error codes are as follow:

0: OK, no error
1: PROM checksum error
2: RAM error
3: data error in DMA test
4: DMA channel 1 has not set the terminal count bit within 200 ms. in DMA test
5: not used
6: not used
7: not used
8: not used
9: not wanted interrupt in CTC test
A: not used
B: CTC test has timed out without interrupt
C: not used
D: not used
E: not used
F: not used
10: not used
11: not used
12: not used
13: not used
14: not used
15: not used
16: not used
17: not used
18: not used
19: not used
20: not used
31: fault in FDC (in FDD test)
32: seek error

33: FDC command abort
34: open door
35: recalibration error
36: track 0 signal not found
37: missing address mark in data field
38: bad cylinder
39: wrong cylinder
3A: missing address mark in ID field
3B: cannot find sector
3C: CRC fault in ID field
3D: CRC fault in data field
3E: drive not ready
3F: overrun in FDC
40: trying to access beyond last cylinder
41: not used
42: flexible disk drive timeout
43: flexible disk data error
50: not used
51: not used
52: not used
53: not used
54: not used
55: not used
56: not used
57: not used
58: not used
59: not used
5A: not used
5B: not used
5C: not used
5D: not used

RETURN LETTER

Title: RCSL No.:

A/S Regnecentralen af 1979/RC Computer A/S maintains a continual effort to improve the quality and usefulness of its publications. To do this effectively we need user feedback, your critical evaluation of this manual.

Please comment on this manual's completeness, accuracy, organization, usability, and readability:

Do you find errors in this manual? If so, specify by page.

How can this manual be improved?

Other comments?

Name: Title:

Company:

Address:

Date:

Thank you

42:i 1288

..... Fold here .....

..... Do not tear - Fold here and staple .....

Affix
postage
here

REGNECENTRALEN
af 1979
Information Department
Lautrupbjerg 1
DK-2750 Ballerup
Denmark