SUPERMAX HARDWARE

Programmers Manual
for the
DIOC MODULE 400
October 1983

This document describes the Disk I/O Controller module in the SUPERMAX computer system as seen by the programmer. The document contains information about how to configure and install DIOC modules in the SUPERMAX computer.

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1. INTRODUCTION.

The SUPERMAX computer concept and basic functions are described in the manual: "SUPERMAX hardware characteristics". Some general information is repeated here.

The SUPERMAX computer system is a modular, multi-CPU computer system. The main processing elements are the CPU modules. A SUPERMAX Computer system consists of a number of CPU modules, each with its own main memory, and a number of intelligent I/O controllers, IOCs.

The IOCs performs all input/output between the CPU modules and peripherals. An IOC is able to transfer data directly to and from user memories without any CPU intervention. CPU modules and IOCs are connected to a common I/O bus.

The I/O bus is basically a memory bus, because all units connected to the bus are accessed as memory from the I/O bus. A bus transfer involves two units: one, the active, takes the initiative to the bus cycle, and addresses the other unit, the passive, and performs a read or write cycle in its memory. CPU modules and IOCs can participate in bus transfers both as active and passive units. When a module is the passive unit in a bus transfer, it is just a port to its own main memory. When a module is the active part in a bus transfer, it is able to access an address space of 16 Mb in 15 units connected to the I/O bus. 16 units can be connected to the I/O bus. A module is able to address only 15 units because it is not able to address itself via the I/O bus.

Units connected to the common bus are able to interrupt each other. A unit sends an interrupt to another unit by writing in a certain part of its memory. Each unit connected to the I/O bus has a part of its memory reserved for this purpose. Interrupts generated in this manner are called external interrupts. Normally a unit has a number of interrupt sources on the unit itself, for examble, timer interrupt and various error interrupts. These interrupts are called internal interrupts.

2. BASIC HARDWARE ELEMENTS.

The DIOC is a single printed circuit board with standard SUPERMAX dimensions. The DIOC performes all input output between disks and the SUPERMAX I/O bus.

The PCB contains the following basic hardware elements:

* CPU.
* Memory.
* Service port.
* Interrupt unit.
* Memory mapping unit.
* I/O bus interface.
* Direct Memory Access, DMA.
* Block Transport Unit, BTU.
* Winchester disk interface.
* Streaming tape interface.
* Floppy disk interface.
* Error detection and handling circuit.

3. CPU.

The CPU used in the intelligent Disk I/O Controller is an INTEL 8085-A2, running with an effective speed of 5 MHz. The 8085 is a 8 bit general purpose microprocessor. The processor is capable of accessing 64 kbyte of memory. All peripherals are serviced by I/O mapped I/O, not memory mapped I/O.

4. MEMORY LAYOUT.

The on-board memory consists of 64 kbyte parity-checked dynamic RAM and 8 kbyte EPROM. The EPROM is divided into two parts. One half is placed in the address space from address 0x0000 to 0x1000. The other half is placed from address 0xE000 to 0xFFFF. The lower part of the EPROM is selected by the 8085 signal SOD. Upon power up reset the signal is active, and the lower part of the EPROM is selected. The RAM in the same address area is, of cource, deselected. The lower part of the EPROM is deselected by deactivating SOD.

The address area 0x1000 to 0xbfff is always RAM. The decoding of the addresses from 0xc000 to 0xffff depends on the content of the address mapping register.

AMR(7:0), Address Mapping Register.
Access mode : I/O write.
I/O address : 0x68
Upon power up reset: AMR(7:0) = 0

AMR(0) : /EDEB, Enable DEBugger.

AMR(0) = 0 : The EPROM is enabled in address area 0xe000 to 0xffff.
AMR(0) = 1 : The RAM is enabled in address area 0xe000 to 0xffff.

AMR(1) : ENBO, Enable Bus Out.

AMR(1) = 0 : The RAM is enabled from adr. 0xc000 to 0xe000 or 0xffff depending on AMR(0).
AMR(1) = 1 : Any memory access in area 0xc000 to 0xe000 or 0xffff will be performed as an I/O bus transfer.

AMR(2) : ENBI, Enable Bus In.

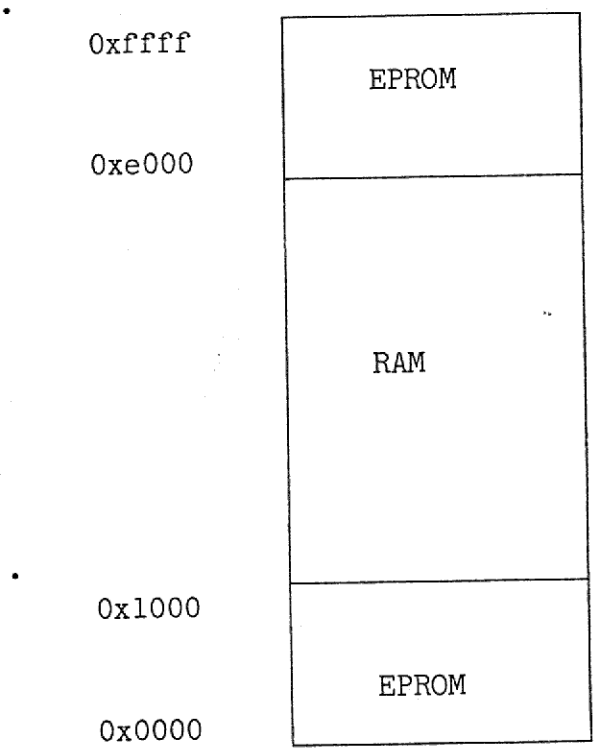
AMR(2) = 0 : An access to the DIOC module from the I/O bus is not answered.
AMR(2) = 1 : All locations in the 64 kbyte RAM memory are available from the I/O bus.

AMR(7:3) are not used.

The address area available to the DMA channels is 0x0000 to 0xffff. The DMA channels are not influenced by the contents of AMR:

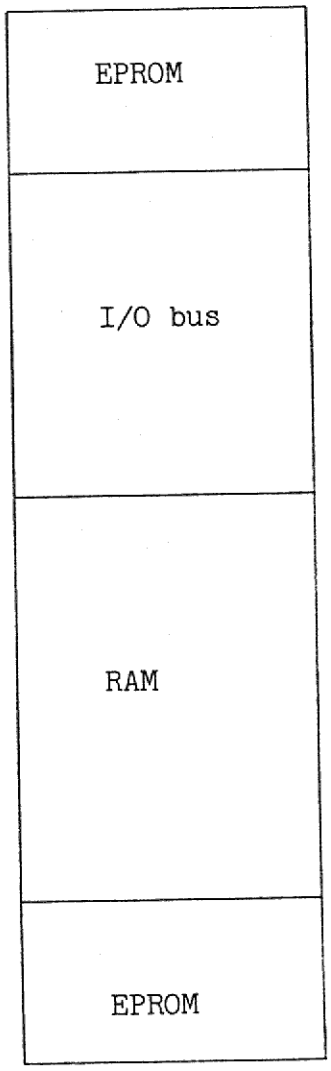
Memory layout after reset:

AMR(2:0) = 000



Memory layout for program development.

AMR(2:0) = 110

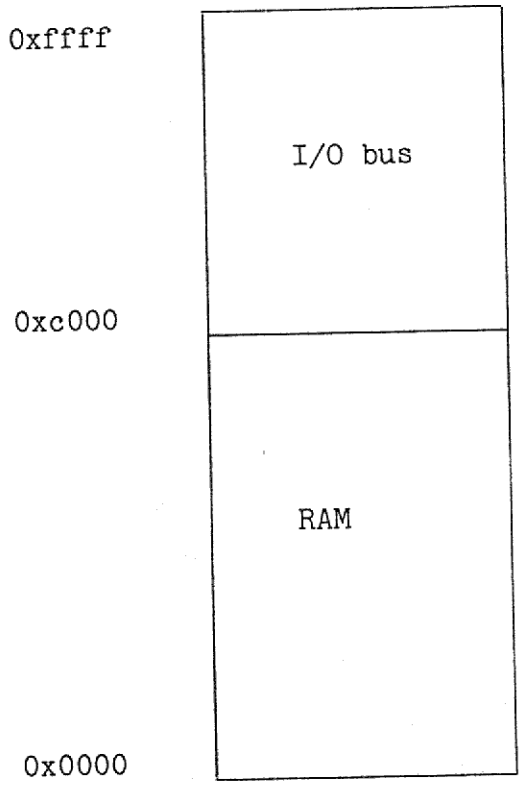


Debug/monitor program.

Bootloader program.

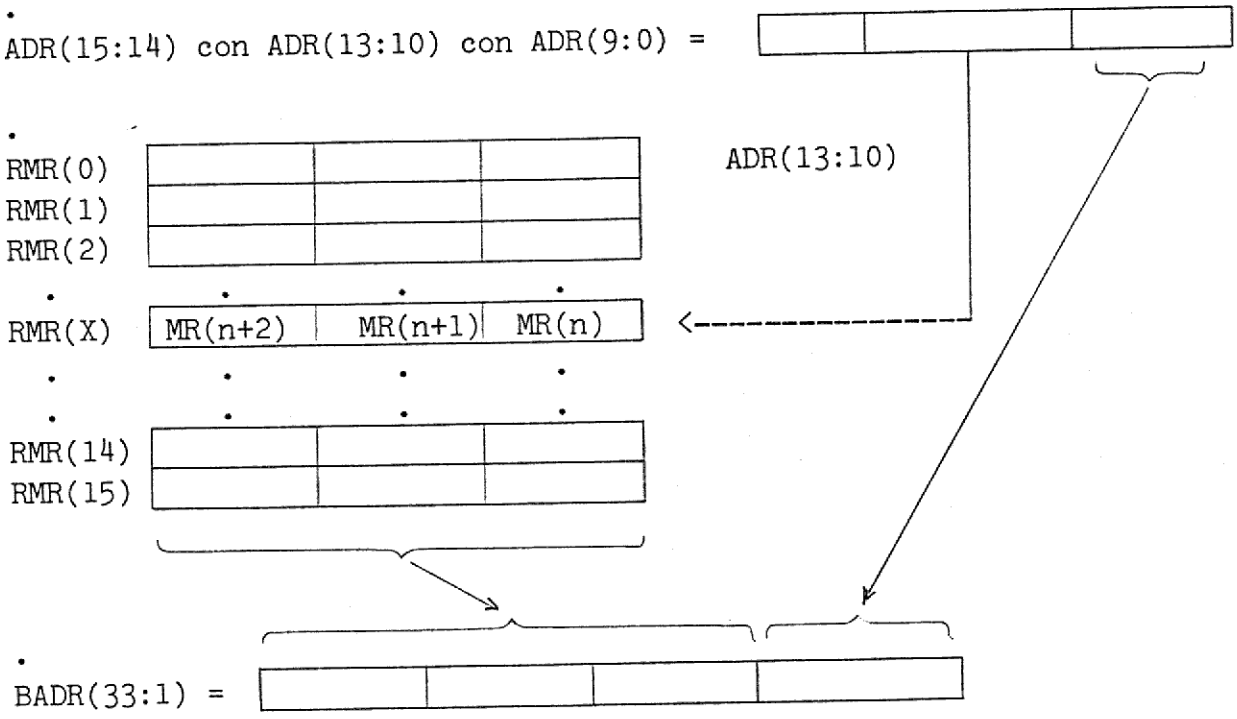
Memory layout for normal use.

AMR(2:0) = 111



5. MEMORY MAPPING UNIT.

When the DIOC is the active part in a I/O bus transfer, the 16 bit 8085 address is expanded through a memory mapping unit. This enables the DIOC to transfer data directly to and from all memory locations connected to the I/O bus. The 8085 address is called ADR(15:0). When ADR(15:14) = 11 and the 8085 performs a memory cycle, the cycle will be a cycle to the I/O bus. (depends of on contents of AMR) ADR(13:10) is used to select one of 16 entries to the memory mapper. Each entry is called a Resulting memory Map Register, RMR. Each RMR consist of three Map Registers, MR. Each map register is 8 bit wide.



The resulting address is the I/O bus address: BADR(33:1)

BADR(33:0) = RMR(X) con ADR(9:0)
BADR(33:0) = MR(n+2)(7:0) con MR(n+1)(7:0) con MR(n)(7:0) con ADR(9:0)

MR(47:0)(7:0), Map Register. 48 map registers, each 8 bits wide.
Access mode: I/O write and I/O read.
Upon power up reset: Contents undefined.

I/O addresses:

	MR(n+2)	MR(n+1)	MR(n)
RMR(0)	0xC2	0xC1	0xC0
RMR(1)	0xC6	0xC5	0xC4
RMR(2)	0xCA	0xC9	0xC8
RMR(3)	0xCE	0xCD	0xCC
RMR(4)	0xD2	0xD1	0xD0
RMR(5)	0xD6	0xD5	0xD4
RMR(6)	0xDA	0xD9	0xD8
RMR(7)	0xDE	0xDD	0xDC
RMR(8)	0xE2	0xE1	0xE0
RMR(9)	0xE6	0xE5	0xE4
RMR(10)	0xEA	0xE9	0xE8
RMR(11)	0xEE	0xEd	0xEC
RMR(12)	0xF2	0xF1	0xF0
RMR(13)	0xF6	0xF5	0xF4
RMR(14)	0xFA	0xF9	0xF8
RMR(15)	0xFE	0xFD	0xFC

An example:

```
        MVI  A,30
        OUT  0C2        ;SETUP MR(2)
        MVI  A,89
        OUT  0C1        ;SETUP MR(1)
        MVI  A,23
        OUT  0C0        ;SETUP MR(0)
        LDA  C056       ;READ A BYTE FROM A UNIT ON THE I/O BUS.
```

The I/O bus address is:

```
00  1100 0010  0010 0100  1000 1100  0101 0110 = 0x0c2248c56
uu  uuaa aaaa  ssss
```

Unit number: 0x3
Address space number: 0x2

segment number: 0x2
address: 0x48c56

6. I/O BUS INTERFACE.

The DIOC contains a full I/O bus interface. When the DIOC acts as the active part in a bus transfer, the 16 bit 8085 address is expanded through the memory mapping unit. This means that the DIOC has full I/O bus addressing capability. Before an active I/O bus cycle, the DIOC has to set up the desired addresses in the memory mapping unit and enable the access to the I/O bus. (Address Mapping Register)
A memory access in address area 0xc000 to 0xffff will be decoded as a I/O bus access. The decoding circuit sends a request to the I/O bus arbitration circuit. After the arbitration, the DIOC drives the address and control lines in the I/O bus. The address specifies another unit connected to the I/O bus, called the passive part. The DIOC gets access to the memory of the passive unit and performs a read or write cycle in the specified memory location. When the address mapping register bit AMR(2), ENBI, is set, the DIOC is able to act in a bus transfer as a passive unit.

The following cycles are implemented:

Active cycles: Byte read and write.

Passive cycles: Byte read and write.
Word read and write.
Read modify write.

The available memory seen from the I/O bus is the 64 kbyte RAM.

Note: It is not possible to run programs in the EPROM simultaneously with passive memory cycles in the RAM.

7. SERVICE PORT.

The service port is a asynchronous RS-232-C line. The port consists of an INTEL 8251A USART and RS-232-C receivers/transmitters. The service port is normally used by diagnostics programs. The port is also useful for program development and debuging. The USART signal Rxrdy is connected to the hardware interrupt RST 5.5. The Rxclk and Txclk are wired together and has one of the following values:

9600 x 16 baud
4800 x 16 baud
2400 x 16 baud
1200 x 16 baud

The effective baud rate depends is programmable. The available speeds are: 9600, 4800, 2400, 1200, 600 and 300 baud. The RS-232-C signals are connected to a 20 pin header. The signals are:

pin	name	
03	Txd	; Transmitter data.
05	Rxd	; Receiver data.
07	RTS	; Modem signals.
09	CTS	
11	DSR	
14	DTR	

Access mode : I/O read and write.
I/O address : 0x60, data.
0x61, control.

8. INTERRUPT.

The five hardware interrupt inputs provided in the 8085 are all used. The general purpose INTR line causes the CPU to fetch an externally placed instruction on the data bus. The instruction is placed by an interrupt and priority unit. The instructions are RST7, RST6....RST0. RST0 has first priority.

External interrupts.

An external interrupt is generated when a unit on the I/O bus performs an active write cycle in the local memory. A specific memory area is used for this purpose. The area is 0x0080 to 0x00FF. The area consists of 8 blocks, each 16 bytes. Total 128 bytes. An active write cycle in block zero, 0x0080 to 0x008F, will activate the INTR line and a RST0 instruction is executed. The interrupt program has to clear this interrupt before enabling new interrupts. The RST0 interrupt is cleared by execution of the instruction OUT 00. A RST1 interrupt is cleared with an OUT 01 instruction etc. The active write cycles that cause an interrupt are: Byte write, word write or a read modify write cycle.

The interrupt unit includes a mask register. With the mask register it is possible to mask out one or several of the eight interrupt levels.

IMR(7:0), Interrupt Mask Register.

Access mode : I/O write.
I/O address : 0xBF
Upon power up reset: Contents undefined.

IMR(0) = 1 : Interrupt level 7 enabled.
IMR(0) = 0 : Interrupt level 7 disabled.

IMR(1) = 1 : Interrupt level 6 enabled.
IMR(1) = 0 : Interrupt level 6 disabled.

IMR(2) = 1 : Interrupt level 5 enabled.
IMR(2) = 0 : Interrupt level 5 disabled.

IMR(3) = 1 : Interrupt level 4 enabled.
IMR(3) = 0 : Interrupt level 4 disabled.

IMR(4) = 1 : Interrupt level 3 enabled.
IMR(4) = 0 : Interrupt level 3 disabled.

IMR(5) = 1 : Interrupt level 2 enabled.
IMR(5) = 0 : Interrupt level 2 disabled.

IMR(6) = 1 : Interrupt level 1 enabled.
IMR(6) = 0 : Interrupt level 1 disabled.

IMR(7) = 1 : Interrupt level 0 enabled.
IMR(7) = 0 : Interrupt level 0 disabled.

Internal interrupts.

The internal interrupts use the four hardware interrupts: TRAP, RST7.5, RST6.5 and RST5.5.

Timer interrupt.

The timer interrupt uses the RST7.5 hardware interrupt. The timer frequency is strapable, and has one of the following values: 0.8, 3.9, 7.8, 39.0, or 79 milliseconds.

Service port interrupt.

The service port uses the RST6.5 hardware interrupt. The USART generates interrupts with the Rxrdy signal. The Txrdy signal is not used.

Disk interface interrupts.

The interrupts from the three disk interfaces are wired together and use the RST5.5 hardware interrupt. The status of the three interrupt lines can be read in the interrupt status register.

ISR(7:0), Interrupt Status Register.

Access mode : I/O write.
I/O address : 0xB2.

ISR(0) = 1 : Interrupt from Winchester disk interface is active.
ISR(0) = 0 : Interrupt from Winchester disk interface is inactive.

ISR(1) = 1 : Interrupt from Streaming tape interface is active.
ISR(1) = 0 : Interrupt from Streaming tape interface is inactive.

ISR(2) = 1 : Interrupt from Floppy disk interface is active.
ISR(2) = 0 : Interrupt from Floppy disk interface is inactive.

ISR(7:3) are not used.

Error detection interrupt.

The error detection hardware uses the non-maskable interrupt line, TRAP. There are eight different interrupt sources. The sources are described later in this manual. The status from the eight sources can be read in the error status register, ESR.

ESR(7:0), Error Status Register.
Access mode : I/O read.
I/O address : 0xB1.

ESR(0) : TOUT, Time OUT.

ESR(0) = 1 : Time out.
ESR(0) = 0 : No time out.

ESR(1) : BEO, BusError Out.

ESR(1) = 1 : Bus error out.
ESR(1) = 0 : No bus error out.

ESR(2) : BEI, Bus error In.

ESR(2) = 1 : Bus error in.
ESR(2) = 0 : No bus error in.

ESR(3) : PER, Parity ERror.

ESR(3) = 1 : Parity error.
ESR(3) = 0 : No parity error.

ESR(4) : ERROR, ERROR signal in I/O bus.

ESR(4) = 1 : Error signal in bus active.
ESR(4) = 0 : Error signal in bus inactive.

ESR(5) : BTOUT, BTU Time OUT.

ESR(5) = 1 : BTU time-out.
ESR(5) = 0 : No-time out.

ESR(6) : BBI, BTU Bus error In.

ESR(6) = 1 : BTU has received a bus error.
ESR(6) = 0 : No bus error.

ESR(7) : DPE, DMA Parity Error.

ESR(7) = 1 : Parity error during DMA cycle.
ESR(7) = 0 : No parity error.

Notice that it is possible to force a non-maskable TRAP interrupt with a switch connected to strap socket 1.

9. DIRECT MEMORY ACCESS.

The DIOC contains a four channels Direct Memory Access Controller. The Controller is a 4 MHz AM9517 device. For further information see the data sheet. The DMA controller performs data transports between the local RAM memory and the three disk interfaces. Three channels are used for this purpose. The fourth channel is used by the Block transport unit, BTU.

Channel 0 : Floppy disk interface.
Channel 1 : Winchester disk interface.
Channel 2 : Streaming tape interface.
Channel 3 : BTU.

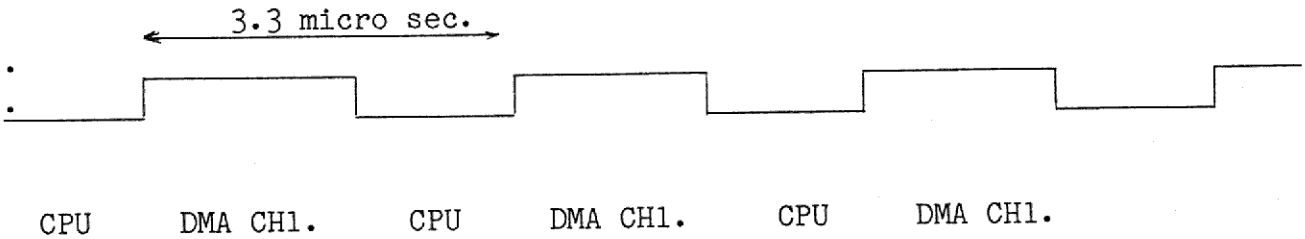
More than one active part is allowed to make transfers to and from the RAM. Therefor an arbitration is made for every memory cycle. The arbitration is made in a manner such that the active parts share the memory cycles evenly. The active parts are: The I/O bus, normal CPU cycles and the four DMA channels.

Because of the arbitration scheme the DMA controller must be programmed for "single byte transfers".

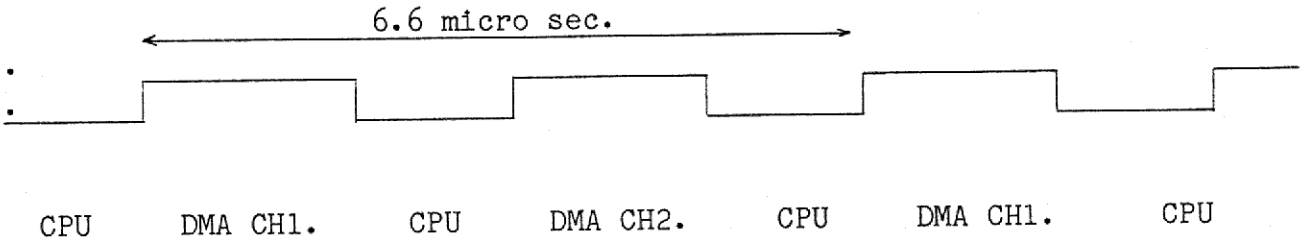
The priority between the four DMA channels depends on the programming of the DMA controller.

The cycle time for one DMA channel is about 3.3 micro sec.

Timing for one DMA channel running:



Timing for two DMA channels running:



DMA Controller, DMAC(7:0).

Access mode : I/O read and write.
I/O addresses: 0xA0 to 0xAF.

10. BLOCK TRANSPORT UNIT.

The Block Transport Unit, BTU, is a device built for high speed data transfers between the local memory and the memories of CPU modules connected to the common I/O bus. The BTU uses 32 bit wide data transfers on the I/O bus. Because of the double word transfers, the load on the I/O bus is minimum. The BTU is always the active part in a bus transfer and runs in either read or write mode. In read mode data is transfered from the main memory to the local memory. The write mode performs data transfers from the 64 kbyte local memory to the main memory. The BTU contains the following basic elements:

* BTU Command Register, BCR.
* BTU Unit number Register, BUR.
* BTU Address space number Register, BAR.
* BTU Address Counter Registers, BACR0, BACR1 and BACR2.
* BTU bidirectional first in first out buffer, FIFO.

BCR(7:0), BTU Command Register.

Access mode : I/O write.
I/O address : 0xBD
Upon power up reset: BCR(7:0) = 0

BCR(0) : START.

BCR(0) = 0 : Start signal is inactive.
BCR(0) = 1 : Start signal is active. The BTU runs until the DMA channel has reached terminal count or until BCR(2) = 0.

BCR(1) : R/W, Read or Write.

BCR(1) = 0 : Write mode transfer.
BCR(1) = 1 : Read mode transfer.

BCR(2) : /CLEAR.

BCR(2) = 0 : The BTU is cleared. If it is running it will stop.
BCR(2) = 1 : The BTU is ready for a command.

BCR(7:3) is not used.

Notice that the command bits may be set only one by one. See the example.

The address on the I/O bus is:

ADR(33:1) = BUR(3:0) con BAR(5:0) con BACR2(7:0) con BACR1(7:0) con BACR0(7:1)

BUR(7:0), BTU unit number address.

Access mode : I/O write.
I/O address : 0xBC
Upon power up reset: Contents of BUR are undefined.

BUR(0) : ADR(30), I/O bus address bit 30.
BUR(1) : ADR(31), I/O bus address bit 31.
BUR(2) : ADR(32), I/O bus address bit 32.
BUR(3) : ADR(33), I/O bus address bit 33.

BUR(7:4) is not used.

BAR(7:0), BTU address space number.

Access mode : I/O write.
I/O address : 0xBB
Upon power up reset: Contents of BAR are undefined.

BAR(0) : ADR(24), I/O bus address bit 24.
BAR(1) : ADR(25), I/O bus address bit 25.
BAR(2) : ADR(26), I/O bus address bit 26.
BAR(3) : ADR(27), I/O bus address bit 27.
BAR(4) : ADR(28), I/O bus address bit 28.
BAR(5) : ADR(29), I/O bus address bit 29.

BAR(7:6) is not used.

BACR2(7:0), BTU address counter register number 2.

Access mode : I/O write.
I/O address : 0xBA
Upon power up reset: Contents of BACR2 are undefined.

BACR2(0) : ADR(16), I/O bus address bit 16.
BACR2(1) : ADR(17), I/O bus address bit 17.
BACR2(2) : ADR(18), I/O bus address bit 18.
BACR2(3) : ADR(19), I/O bus address bit 19.
BACR2(4) : ADR(20), I/O bus address bit 20.
BACR2(5) : ADR(21), I/O bus address bit 21.
BACR2(6) : ADR(22), I/O bus address bit 22.
BACR2(7) : ADR(23), I/O bus address bit 23.

BACR1(7:0), BTU address counter register number 1.

Access mode : I/O write.
I/O address : 0xB9
Upon power up reset: Contents of BACR1 are undefined.

BACR1(0) : ADR(08), I/O bus address bit 8.
BACR1(1) : ADR(09), I/O bus address bit 9.
BACR1(2) : ADR(10), I/O bus address bit 10.
BACR1(3) : ADR(11), I/O bus address bit 11.
BACR1(4) : ADR(12), I/O bus address bit 12.
BACR1(5) : ADR(13), I/O bus address bit 13.
BACR1(6) : ADR(14), I/O bus address bit 14.
BACR1(7) : ADR(15), I/O bus address bit 15.

BACR0(7:0), BTU address counter register number 0.

Access mode : I/O write.
I/O address : 0xB8
Upon power up reset: Contents of BACR0 are undefined.

BACR0(1) : ADR(1), I/O bus address bit 1.

BACR0(2) : ADR(2), I/O bus address bit 2.
BACR0(3) : ADR(3), I/O bus address bit 3.
BACR0(4) : ADR(4), I/O bus address bit 4.
BACR0(5) : ADR(5), I/O bus address bit 5.
BACR0(6) : ADR(6), I/O bus address bit 6.
BACR0(7) : ADR(7), I/O bus address bit 7.

BACR0(0) is not used.

The address count registers must be loaded in the following order: BACR0, BACR1 and BACR0.

FIFO.

The bidirectional fifo is 32 bits wide and has a depth of two.
Access mode : DMA byte read and byte write.

DMA.

The BTU uses DMA channel three.

Functional description.

Read mode:
The main memory address is loaded into the address registers: BUR, BAR, BACR2, BACR1 and BACR0.
DMA channel three is programmed to single byte write transfer. The destination address in the local memory is loaded into the address base registers in DMA channel three. The number of bytes in the block transport is loaded into the word count registers in DMA channel three. The BTU is now ready for a start command. After the start command the BTU requests the I/O bus, addresses a unit on the bus, reads a double word into the FIFO and finishes the bus transfer. The double word is moved one down in the FIFO, and the BTU requests DMA service. The DMA channel moves the four bytes from the FIFO to the local memory, one by one. Simultaneously the BTU increments the I/O bus address and performes a new bus transfer with the new address. The number of transfers is defined in the base word count registers in the

DMA channel. The block transfer is finished when DMA channel three has reached terminal count. The terminal count status can be read in the DMA controller.

Examble: Read transfer.

Transfer from main CPU address 0x0c2248c56 to DIOC local memory address 0x2000. The number of bytes is 0x1000.

```
;
; First set up the I/O bus address.
;
ADR:    MVI     A,56    ; Set up adr: 0x0c2248c56
        OUT     0B8     ; BACR0
        MVI     A,8C    ;
        OUT     0B9     ; BACR1
        MVI     A,24    ;
        OUT     0BA     ; BACR2
        MVI     A,02    ;
        OUT     0BB     ; BAR
        MVI     A,03    ;
        OUT     0BC     ; BUR
;
; Initialize the DMA controller, channel 3.
;
DMAR:   OUT     0AD     ; DMA master clear.
        LXI     H,2000  ; Local buffer start adr.
        LXI     D,1000  ; Number of bytes in transfer.
        MOV     A,L
        OUT     0A6
        MOV     A,H
        OUT     0A6     ; Adr. loaded in base adr. register.
        DCX     D
        MOV     A,E
        OUT     0A7
        MOV     A,D7
        OUT     0A7     ; Adr. loaded in word count register.
        MVI     A,47
```

```
        OUT     0AB     ; Mode set: single transfer and write.
        MVI     A,07
        OUT     0AF     ; Set mask bits.
;
; Start the transfer with a command in the BCR.
;
RBCR:   MVI     A,0
        OUT     0BD     ; The BTU is cleared.
        MVI     A,06
        OUT     0BD     ; Read transfer and clear inactive.
        MVI     A,07
        OUT     0BD     ; Start bit active
;
; Wait until the transport is finished.
;
WAIT:   IN      0A8     ; Get terminal count in the DMA-C.
        ANI     08
        JZ      WAIT    ; Wait until terminal count.
;
; END
;
```

Write mode:

The main memory address is loaded into the address registers. The DMA channel is loaded with the local memory source address and word count. The channel is programmed for single byte transfer, read mode. After a start command the BTU requests a DMA service. The first four bytes are moved into the FIFO, and the double word is moved one down. Now two things run in parallel: The BTU requests the bus, and performs a bus transfer simultaneously with four new DMA transfers into the first level in the FIFO. The DMA transport is finished before the FIFO is empty and it is therefore not sufficient only to ask for terminal count in channel three. The BTU is finished a maximum af 15 micro seconds after the terminal count is reached.

Speed.

The speed depends on the DMA channel. If only one DMA channel is running, the speed is about 300 kbytes/sec.

11. WINCHESTER DISK INTERFACE.

The Winchester disk interface is the Shuggarts Associated Standard Interface, called SASI. The SASI interface contains two data registers, two control registers, parity generating/checking circuit, interrupt generating circuit and some control logic.
Note that the signals in the SASI bus are active low.

SDOR(7:0), SASI Data Out Register.

Access mode : I/O write and DMA I/O write.
I/O address : 0x81.
Upon power up reset the content of SDOR is not defined.

SDOR(0) = 1 : SASI bus signal DB(0) low.
SDOR(0) = 0 : SASI bus signal DB(0) high.

SDOR(1) = 1 : SASI bus signal DB(1) low.
SDOR(1) = 0 : SASI bus signal DB(1) high.

SDOR(2) = 1 : SASI bus signal DB(2) low.
SDOR(2) = 0 : SASI bus signal DB(2) high.

SDOR(3) = 1 : SASI bus signal DB(3) low.
SDOR(3) = 0 : SASI bus signal DB(3) high.

SDOR(4) = 1 : SASI bus signal DB(4) low.
SDOR(4) = 0 : SASI bus signal DB(4) high.

SDOR(5) = 1 : SASI bus signal DB(5) low.
SDOR(5) = 0 : SASI bus signal DB(5) high.

SDOR(6) = 1 : SASI bus signal DB(6) low.
SDOR(6) = 0 : SASI bus signal DB(6) high.

SDOR(7) = 1 : SASI bus signal DB(7) low.
SDOR(7) = 0 : SASI bus signal DB(7) high.

SDIR(7:0), SASI Data In Register.

Access mode : I/O read and DMA I/O read.
I/O address : 0x81.

SDIR(0) = 1 : SASI bus signal DB(0) low.
SDIR(0) = 0 : SASI bus signal DB(0) high.

SDIR(1) = 1 : SASI bus signal DB(1) low.
SDIR(1) = 0 : SASI bus signal DB(1) high.

SDIR(2) = 1 : SASI bus signal DB(2) low.
SDIR(2) = 0 : SASI bus signal DB(2) high.

SDIR(3) = 1 : SASI bus signal DB(3) low.
SDIR(3) = 0 : SASI bus signal DB(3) high.

SDIR(4) = 1 : SASI bus signal DB(4) low.
SDIR(4) = 0 : SASI bus signal DB(4) high.

SDIR(5) = 1 : SASI bus signal DB(5) low.
SDIR(5) = 0 : SASI bus signal DB(5) high.

SDIR(6) = 1 : SASI bus signal DB(6) low.
SDIR(6) = 0 : SASI bus signal DB(6) high.

SDIR(7) = 1 : SASI bus signal DB(7) low.
SDIR(7) = 0 : SASI bus signal DB(7) high.

Parity on the data out register SDOR is always generated.
Parity is checked each time the data in register SDIR is read.

SCR(7:0), SASI Command Register.

Access mode : I/O write.

I/O address : 0x80.
Upon power up reset SCR(7:0) = 0.

SCR(0) : RST, Reset.

SCR(0) = 1 : SASI bus signal RST low.
SCR(0) = 0 : SASI bus signal RST high.

SCR(1) : SEL, Select.

SCR(1) = 1 : SASI bus signal SEL low.
SCR(1) = 0 : SASI bus signal SEL high.

SCR(2) : DEN, DMA Enable.

SCR(2) = 1 : Enable DMA service.
SCR(2) = 0 : Disable DMA service.

SCR(3) : ATN, Attention

SCR(3) = 1 : SASI bus signal ATN low.
SCR(3) = 0 : SASI bus signal ATN high.

SCR(4) : /RPER.

SCR(4) = 1 : Enable parity checking circuit.
SCR(4) = 0 : Reset the parity checking circuit.

SCR(7:5) are not used.

SSR(7:0), SASI Status Register.

Access mode : I/O read.
I/O address : 0x80.

SSR(0) : I/O, I/O signal.

SSR(0) = 1 : SASI bus signal I/O high.
SSR(0) = 0 : SASI bus signal I/O low.

SSR(1) : C/D, Control/data signal.

SSR(1) = 1 : SASI bus signal C/D high.
SSR(1) = 0 : SASI bus signal C/D low.

SSR(2) : BSY, Busy signal.

SSR(2) = 1 : SASI bus signal BSY high.
SSR(2) = 0 : SASI bus signal BSY low.

SSR(3) : MSG, Message signal.

SSR(3) = 1 : SASI bus signal MSG high.
SSR(3) = 0 : SASI bus signal MSG low.

SSR(4) : REQ, Request signal.

SSR(4) = 1 : SASI bus signal REQ high.
SSR(4) = 0 : SASI bus signal REQ low.

SSR(5) : INT, Interrupt.

SSR(5) = 1 : No interrupt.
SSR(5) = 0 : SASI interface has a pending interrupt.

SSR(6) : PER, Parity ERror.

SSR(6) = 1 : No error.
SSR(6) = 0 : Parity checking circuit has detected an error.

SSR(7) is not used.

Control logic.

The control logic activates the interrupt line when the SASI bus signals CD and I/O are low, and REQ goes low. The interrupt is cleared and it is kept cleared when DEN is low. The interface activates the SASI bus signal ACK each time data is transfered to/from the data

registers. The interface requests DMA service when the SASI bus signal C/D is high, the REQ line is low and DEN is high.

12. STREAMING TAPE INTERFACE.

The streaming tape interface is a standard QIC II interface. The interface contains two data registers, three status registers, interrupt generating circuit and some control logic.

TDOR(7:0), Tape Data Out Register.

Access mode : I/O write and DMA I/O write.
I/O address : 0x88.
Upon power up reset the content of TDOR is not defined.

TDOR(0) = 1 : QIC II bus signal DB(0) = 0.
TDOR(0) = 0 : QIC II bus signal DB(0) = 1.

TDOR(1) = 1 : QIC II bus signal DB(1) = 0.
TDOR(1) = 0 : QIC II bus signal DB(1) = 1.

TDOR(2) = 1 : QIC II bus signal DB(2) = 0.
TDOR(2) = 0 : QIC II bus signal DB(2) = 1.

TDOR(3) = 1 : QIC II bus signal DB(3) = 0.
TDOR(3) = 0 : QIC II bus signal DB(3) = 1.

TDOR(4) = 1 : QIC II bus signal DB(4) = 0.
TDOR(4) = 0 : QIC II bus signal DB(4) = 1.

TDOR(5) = 1 : QIC II bus signal DB(5) = 0.
TDOR(5) = 0 : QIC II bus signal DB(5) = 1.

TDOR(6) = 1 : QIC II bus signal DB(6) = 0.
TDOR(6) = 0 : QIC II bus signal DB(6) = 1.

TDOR(7) = 1 : QIC II bus signal DB(7) = 0.
TDOR(7) = 0 : QIC II bus signal DB(7) = 1.

TDIR(7:0), Tape Data In Register.

Access mode : I/O read and DMA I/O read.
I/O address : 0x88.
Upon power up reset the content of TDIR is not defined.

TDIR(0) = 1 : QIC II bus signal DB(0) = 0.
TDIR(0) = 0 : QIC II bus signal DB(0) = 1.

TDIR(1) = 1 : QIC II bus signal DB(1) = 0.
TDIR(1) = 0 : QIC II bus signal DB(1) = 1.

TDIR(2) = 1 : QIC II bus signal DB(2) = 0.
TDIR(2) = 0 : QIC II bus signal DB(2) = 1.

TDIR(3) = 1 : QIC II bus signal DB(3) = 0.
TDIR(3) = 0 : QIC II bus signal DB(3) = 1.

TDIR(4) = 1 : QIC II bus signal DB(4) = 0.
TDIR(4) = 0 : QIC II bus signal DB(4) = 1.

TDIR(5) = 1 : QIC II bus signal DB(5) = 0.
TDIR(5) = 0 : QIC II bus signal DB(5) = 1.

TDIR(6) = 1 : QIC II bus signal DB(6) = 0.
TDIR(6) = 0 : QIC II bus signal DB(6) = 1.

TDIR(7) = 1 : QIC II bus signal DB(7) = 0.
TDIR(7) = 0 : QIC II bus signal DB(7) = 1.

TSR(7:0), Tape Status Register.

Access mode : I/O read.
I/O address : 0x89.

TSR(0) : ACK, Acknowledge.

TSR(0) = 1 : QIC II bus signal /ACK = 0.
TSR(0) = 0 : QIC II bus signal /ACK = 1.

TSR(1) : RDY, Ready.

TSR(1) = 1 : QIC II bus signal /RDY = 0.
TSR(1) = 0 : QIC II bus signal /RDY = 1.

TSR(2) : EXC, Exception.

TSR(2) = 1 : QIC II bus signal /EXC = 0.
TSR(2) = 0 : QIC II bus signal /EXC = 1.

TSR(3) : DIRC, Direction.

TSR(3) = 1 : QIC II bus signal /DIRC = 0.
TSR(3) = 0 : QIC II bus signal /DIRC = 1.

TSR(6) : STA, STAtus.

TSR(6) = 1 : STA = 1.
TSR(6) = 0 : STA = 0.

TSR(7) : INT, interrupt.

TSR(7) = 1 : Interrupt, DMA channel has reached terminal count.
TSR(7) = 0 : No interrupt because of DMA.

TSR(5:4) are not used.

TCR(7:0), Tape Command Register.

Access mode : I/O write.
I/O address : 0x89.
Upon power up reset TCR(7:0) = 0.

TCR(0) : ONL, Online.

TCR(0) = 1 : QIC II bus signal /ONL = 0.
TCR(0) = 0 : QIC II bus signal /ONL = 1.

TCR(1) : REQ, Request.

TCR(1) = 1 : QIC II bus signal /REQ = 0.
TCR(1) = 0 : QIC II bus signal /REQ = 1.

TCR(2) : XFER, Transfer.

TCR(2) = 1 : QIC II bus signal /XFER = 0.
TCR(2) = 0 : QIC II bus signal /XFER = 1.

TCR(3) : RES, Reset.

TCR(3) = 1 : QIC II bus signal /RES = 0.
TCR(3) = 0 : QIC II bus signal /RES = 1.

TCR(7:4) are not used.

TER(7:0), Tape Enable Register.

Access mode : I/O write.
I/O address : 0x8A.
Upon power up reset TER(7:0) = 0.

TER(0) : STA, STAtus.

TER(0) = 1 : STA = 1. Internal status bit, can be read in TSR(6).
TER(0) = 0 : STA = 0. Internal status bit, can be read in TSR(6).

TER(1) : EWDMA, Enable Write DMA.

TER(1) = 1 : The DMA channel is able to write data in TDOR.
TER(1) = 0 : DMA disable.

TER(2) : ERDMA, Enable Read DMA.

TER(2) = 1 : The DMA channel is able to read data in TDIR.
TER(2) = 0 : DMA disable.

TER(3) : EINT, Enable Interrupt.

TER(3) = 1 : Interrupt enable. The interrupt sources are either terminal count from the DMA channel or the QIC II bus signal /EXC.

TER(3) = 0 : Interrupt disable.

TER(7:4) are not used.

Control logic.

If ERDMA and/or EWDMA = 1 the control logic activates the QIC II bus signal XFER according to DMA transfers to/from the two data registers. The logic generates an interrupt when the DMA channel reaches terminal count (EOP), and when the QIC II bus signal EXC goes active. The EOP interrupt is cleared by executing the instruction "IN 0x8A". The interface requests for DMA service if EWDMA or ERDMA = 1.

13. FLOPPY DISK INTERFACE.

The floppy disk interface is built around the Western Digital VLSI device FD 1795. For programming and further information, see the product data sheets. The interface is mounted with components for interface to either a 8 inch or a 5.25 inch floppy disk drive. The interface contains the FD 1795, one control register, and some logic.

FCR(7:0), Floppy disk Control Register.

Access mode : I/O write.
I/O address : 0x94.
Upon power up reset the content of FCR is not defined.

FCR(0) : SEL3, Select no. 3.

FCR(0) = 1 : Floppy disk interface signal /SEL3 = 0.
FCR(0) = 0 : Floppy disk interface signal /SEL3 = 1.

FCR(1) : SEL2, Select no. 2.

FCR(1) = 1 : Floppy disk interface signal /SEL2 = 0.
FCR(1) = 0 : Floppy disk interface signal /SEL2 = 1.

FCR(2) : SEL1, Select no. 1.

FCR(2) = 1 : Floppy disk interface signal /SEL1 = 0.
FCR(2) = 0 : Floppy disk interface signal /SEL1 = 1.

FCR(3) : SEL0, Select no. 0.

FCR(3) = 1 : Floppy disk interface signal /SEL0 = 0.
FCR(3) = 0 : Floppy disk interface signal /SEL0 = 1.

FCR(4) : SIDE, SIDE select.

FCR(4) = 1 : Floppy disk interface signal /SIDE = 0.
FCR(4) = 0 : Floppy disk interface signal /SIDE = 1.

FCR(5) : MOTOR, MOTOR start signal.

FCR(5) = 1 : Floppy disk interface signal /MOTOR = 0.
FCR(5) = 0 : Floppy disk interface signal /MOTOR = 1.

FCR(6) : WCOMP, Write COMPensation.

FCR(6) = 1 : No write compensation.
FCR(6) = 0 : Write compensation enable.

FCR(7) : DDEN, Dual DENsity

FCR(7) = 1 : Input signal to FD 1795 /DDEN = 0.
FCR(7) = 0 : Input signal to FD 1795 /DDEN = 1.

FD 1795.
Access mode : I/O read and write, DMA I/O read and write.
I/O address : 0x90 to 0x93.

The interface uses directly the DMA request and interrupt lines from the FD 1795.

Notice that the 8 inch and 5.25 inch interface buses are not identical. The 5.25 inch interface does not contain the following signals: TG-43, MOTOR and SEL3.

14. ERROR DETECTING AND HANDLING CIRCUIT.

General description.

Time-out.

Local CPU cycles and active bus cycles are monitored by a time-out circuit. A time-out occurs if the CPU executes a HLT instruction, or if the CPU performs an active bus cycle with an illegal destination address. An illegal address is perhaps an address to an unit which is not present. Active bus cycles performed by the BTU are monitored by an other time-out circuit.

Parity error.

A parity bit is generated when a write cycle is made in the local RAM. The parity is checked during all memory read cycles. The parity is generated/checked independent of the type of memory cycle. (CPU, DMA and I/O bus cycles.)

Bus error.

A passive part in a I/O bus cycle is able to answer the active part with one of two signals. If the performed memory cycle is without any errors the answer is DTACK, Data Transfer ACKnowledge. If an error occurs, the passive unit answers with the Bus error signal. The DIOC is able to generate, and to act upon the bus error signal. The BTU part of the DIOC is able to act on the bus error signal.

Error.

The I/O bus signal ERROR indicates that a unit has detected an internal failure. Upon power up reset the DIOC activats the ERROR signal in the I/O bus. The ERROR signal can be activated or deactivated by the program.

Two registers are used for control and diagnosis of errors.

ECR(7:0), Error Command Register.
Access mode : I/O write.
I/O address : 0xBE.
Upon power up reset ECR(7:0) = 0.

ECR(0) : ETOUT, Enable Time OUT.

ECR(0) = 1 : Enable the time-out circuit.
ECR(0) = 0 : No time-out.

ECR(1) : EBO, Enable Bus error Out.

ECR(1) = 1 : Enable bus error out circuit.
ECR(1) = 0 : No bus error out.

ECR(2) : EBI, Enable Bus error In.

ECR(2) = 1 : Enable bus error in circuit.
ECR(2) = 0 : No reaction on a bus error in.

ECR(3) : EPE, Enable Parity Error.

ECR(3) = 1 : Enable parity checking circuit.
ECR(3) = 0 : No parity check.

ECR(4) : SER, Set ERror.

ECR(4) = X : The transition from 0 to 1 sets the error line with the value specifed in ECR(6).

ECR(5) : EPS, Enable Parity Status.

ECR(5) = 1 : Enable the parity status.
ECR(5) = 0 : No parity status.

ECR(6) : ERV, ERror Value.

ECR(6) = 1 : Error signal active.
ECR(6) = 0 : No error.

ECR(7) : EPD, Enable Parity for DMA.

ECR(7) = 1 : Enable the parity checking circuit during DMA cycles.
ECR(7) = 0 : No parity check.

ESR(7:0), Error Status Register.
Access mode : I/O read.
I/O address : 0xB1.

ESR(0) : TOUT, Time OUT.

ESR(0) = 1 : Time-out.
ESR(0) = 0 : No time-out.

ESR(1) : BEO, BusError Out.

ESR(1) = 1 : Bus error out.
ESR(1) = 0 : No bus error out.

ESR(2) : BEI, Bus error In.

ESR(2) = 1 : Bus error in.
ESR(2) = 0 : No bus error in.

ESR(3) : PER, Parity ERror.

ESR(3) = 1 : Parity error.
ESR(3) = 0 : No parity error.

ESR(4) : ERROR, ERROR signal in I/O bus.

ESR(4) = 1 : Error signal in bus active.
ESR(4) = 0 : Error signal in bus inactive.

ESR(5) : BTOUT, BTU Time OUT.

ESR(5) = 1 : BTU time out.
ESR(5) = 0 : No time out.

ESR(6) : BBI, BTU Bus error In.

ESR(6) = 1 : BTU has received a bus error.
ESR(6) = 0 : No bus error.

ESR(7) : DPE, DMA Parity Error.

ESR(7) = 1 : Parity error during DMA cycle.
ESR(7) = 0 : No parity error.

Time out:

Detection: 1. ECR(0) = 1.
2. Active I/O bus cycle is too long.
3. Internal memory cycle is too long.
4. Passive I/O bus cycle in the local memory is too long.

Reaction: 1. Error status register bit ESR(0) = 1.
2. A non-maskable interrupt, TRAP, is generated.
3. Indicator led2 is switched on.

Reset: ECR(0) = 0 deactivates the interrupt line, switches the indictor led2 off and sets ESR(0) = 0.

Bus error out:

Detection: 1. ECR(1) = 1.
2. A parity error occurs during a passive bus cycle.

Reaction: 1. Error status register bit ESR(1) = 1.
2. A non-maskable interrupt, TRAP, is generated.
3. Indicator led5 is switched on.

Reset: ECR(1) = 0 deactivates the interrupt line, switches the indicator led5 off, and sets ESR(1) = 0.

Note: Independent of ECR(1), a unit is answered with a bus error if a parity error is detected.

Bus error in:

Detection: 1. ECR(2) = 1.
2. The DIOC receives a bus error during a active bus cycle.

Reaction: 1. Error status register bit ESR(2) = 1.
2. A non-maskable interrupt, TRAP, is generated.
3. Indicator led3 is switched on.

Reset: ECR(0) = 0 deactivates the interrupt line, switches the indicator led3 off and sets ESR(2) = 0.

Note: If ECR(2) = 0 and the DIOC receives a bus error, the DIOC accepts the data without any warning.

Parity error:

Detection: 1. ECR(3) = 1.
2. ECR(5) = 1.
3. Parity error during an internal memory cycle.

Reaction: 1. Error status register bit ESR(3) = 1.
2. An internal reset signal is generated. This means that the boot prom is enabled, and access to and from the I/O bus is disabled.
3. A non-maskable interrupt, TRAP, is generated during the first executed instruction in the boot prom.
4. Indicator led4 is switched on.
5. The ERROR signal is activated.

Reset: The ERROR signal and ECR(5) are deactivated by ECR(4) and ECR(6).

Note: The programmer has to deactivate the ERROR signal before enable of the parity error checking circuit. If a main CPU activates the ERROR RESET signal, the ERROR signal is deactivated.

DMA parity error.

Detection: 1. ECR(7) = 1.
2. A parity error occurs during a DMA cycle.

Reaction: 1. Error status register bit ESR(7) = 1.
2. A non-maskable interrupt, TRAP, is generated.

Reset: ECR(7) = 0 deactivates the interrupt line and ESR(7) = 0.

Error checking circuit not under control of ECR:

The time-out circuit monitoring the active bus cycles from the BTU runs when the BTU Command Register bit CLEAR is inactive.

BTU time-out:

Detection: 1. /CLEAR = 1.
2. BTU active I/O bus cycle is too long.

Reaction: 1. ESR(5) = 1.
2. A non maskable interrupt, TRAP, is generated.

Reset: /CLEAR = 0 deactivates the interrupt line and ESR(5) = 0.

BTU bus error in:

Detection: 1. /CLEAR = 1.
2. The BTU receives a bus error during an active cycle.

Reaction: 1. ESR(6) = 1.
2. A non-maskable interrupt, TRAP, is generated.

Reset: /CLEAR = 0 deactivates the interrupt line and ESR(6) = 0.

15. INDICATOR LEDS.

Five red light emitting diodes are used to indicate errors and special status.

LED1.

On: The boot prom is enabled.
Off: The boot prom is switched out.
Upon power up: The LED1 is on.

LED2.

On: A time out is pending.
Off: No time out.
Upon power up: The LED2 is off.

LED3.

On: A bus error is received.
Off: No bus error.
Upon power up: The LED3 is off.

LED4.

On: The ERROR line is active. The error line is set by the program or becaurse of parity error.
Off: No error.
Upon power up: The LED4 is on.

LED5.

On: The DIOC has answered with a bus error.
Off: No error.
Upon power up: The LED5 is off.

16. STRAPS.

Strap 1.

Function: Real time clock.

Position: C 3,2

Jumper	Clock
1	0.8 milliseconds
2	3.9 milliseconds
3	7.8 milliseconds
4	39.0 milliseconds
5	78.0 milliseconds

Strap 2.

Function: Baud rate to service port. Connected to both Txclk and Rxclk.

Position: B 7,3

Jumper	Clock
1	9600 x 16 baud.
2	4800 x 16 baud.
3	2400 x 16 baud.
4	1200 x 16 baud.

Strap 3.

Function: Special option for hardware service.

Position: B 4,3

Under normal circumstances, the jumper must be in position two.

Strap socket 1.

Function: Possible to connect two switches: One is able to generate an internal reset pulse and the other is able to generate a hardware interrupt. (TRAP)

Position: C 4,1

Under normal circumstances the strap socket is mounted as follows:

```
    * *=* * * * * *

1.  * *=* * * * * *
```

An internal reset pulse is generated if the connection between pin 2 and 3 is removed, and pins 1 and 2 are connected together.

A non-maskable interrupt TRAP is generated if the connection between pin 14 and 15 is removed, and pins 15 and 16 are connected together.

17. INSTALLATION.

All modules in a SUPERMAX computer system differ in some details.

Unit number.

Each intelligent module connected to the common, I/O bus has an unique address. The address is called the unit number. The unit number is coded in a programable device, called a PAL. The PAL is marked with the text DUXX. XX is the decimal unit number. The unit number PAL is located in position A 4,6.

Priority.

The arbitration scheme used in the commen, I/O bus is based on fixed priorities. The priority is coded in a PAL. Two units connected to the I/O bus cannot use the same priority. The priority PAL is marked DPXX, where XX is the priority. The DIOC module uses two priorities. The PALs are located in position A 1,9 and A 1,10.

18. CABLES.

The connection between the DIOC module and the disks is made with three flat cable connectors.

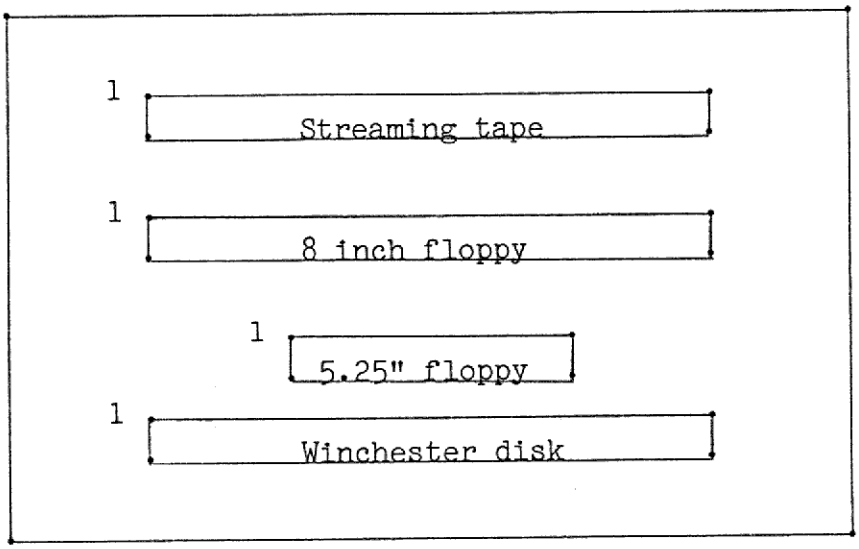
The headers mounted on the PCB are positioned as follows:

Winchester disk: C 1,8.

Floppy disk: C 3,8.

Streaming tape: C 5,8.

The three flat cables are connected to the DIOC back panel The DIOC back panel is mounted on the rear of the SUPERMAX card cabinet.



Card cabinet disk interface panel
Seen from the rear.

The connection to the service port is located in position C 5,3.

19. BOARD SURVEY.