DANSK DATA ELEKTRONIK

ID-7001 8k PROM MODULE

for the

ID-7000 MICROPROCESSOR SYSTEM

june 1976

04420

Generatorvej 6A
DK-2730 Herlev
Denmark

Author: Tom Hertz
rev. 22-2-77 OL

ID-7001 PROM MODULE.

1. Introduction.

The ID-7001 module contains a maximum of 8k-8bit reprogrammable read-only memory. The memory chips used can be either INTEL 2708 or 2704 (8708,8704), containing 1k byte and ½k byte each respectively.

The module may be strapped in 4 different ways:

A) 2k memory consisting of max. 4 2704
B) 4k memory consisting of max. 8 2704
C) 4k memory consisting of max. 4 2708
D) 8k memory consisting of max. 8 2708

Appendix 1 contains a logic schematic of the module.
Appendix 2 is a data sheet of the memory chips.

2. Description.

2.1 Addressbus ADR(15:0).

The addresses are used in the different modes as shown in table 1.

	A	B	C	D	
ADR	8:0	8:0	9:0	9:0	select byte in a PROM-chip
ADR	10:9	11:9	11:10	12:10	select PROM-chip
ADR	15:11	15:12	15:12	15:13	select memory board

table 1

Data from the memory is read if the addressfield that selects the memory module agrees with a manual switch register situated on the module.

2.2 Switchregister S(15:11).

In the upper left corner of the module the manual switchregister is situated. This register determines the module's start address.

1 / 0	11	12	13	14	15	NU
	2	4	8	16	32	k byte

NU=not used

The switches have the following meaning in the different modes:

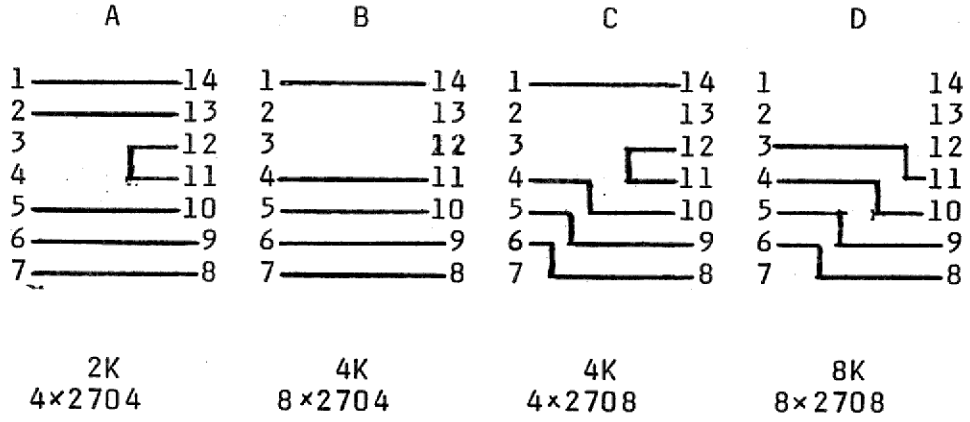
A	B	C	D	
15:11	15:12	15:12	15:13	switches that determine the address.
-	11	11	12:11	switches that have no affect on the address.

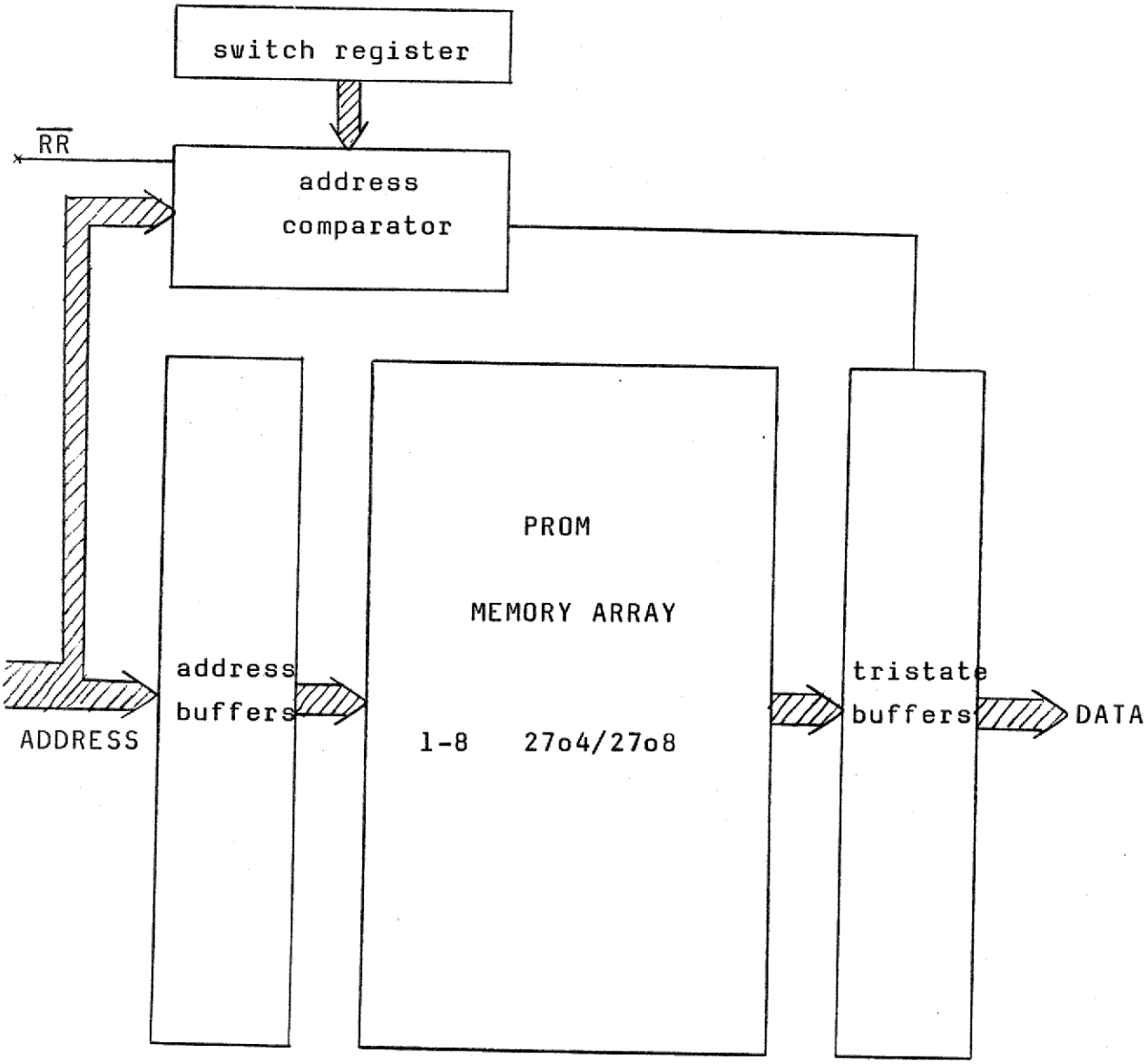
The startaddress will in the 4 modes be a multiplum of

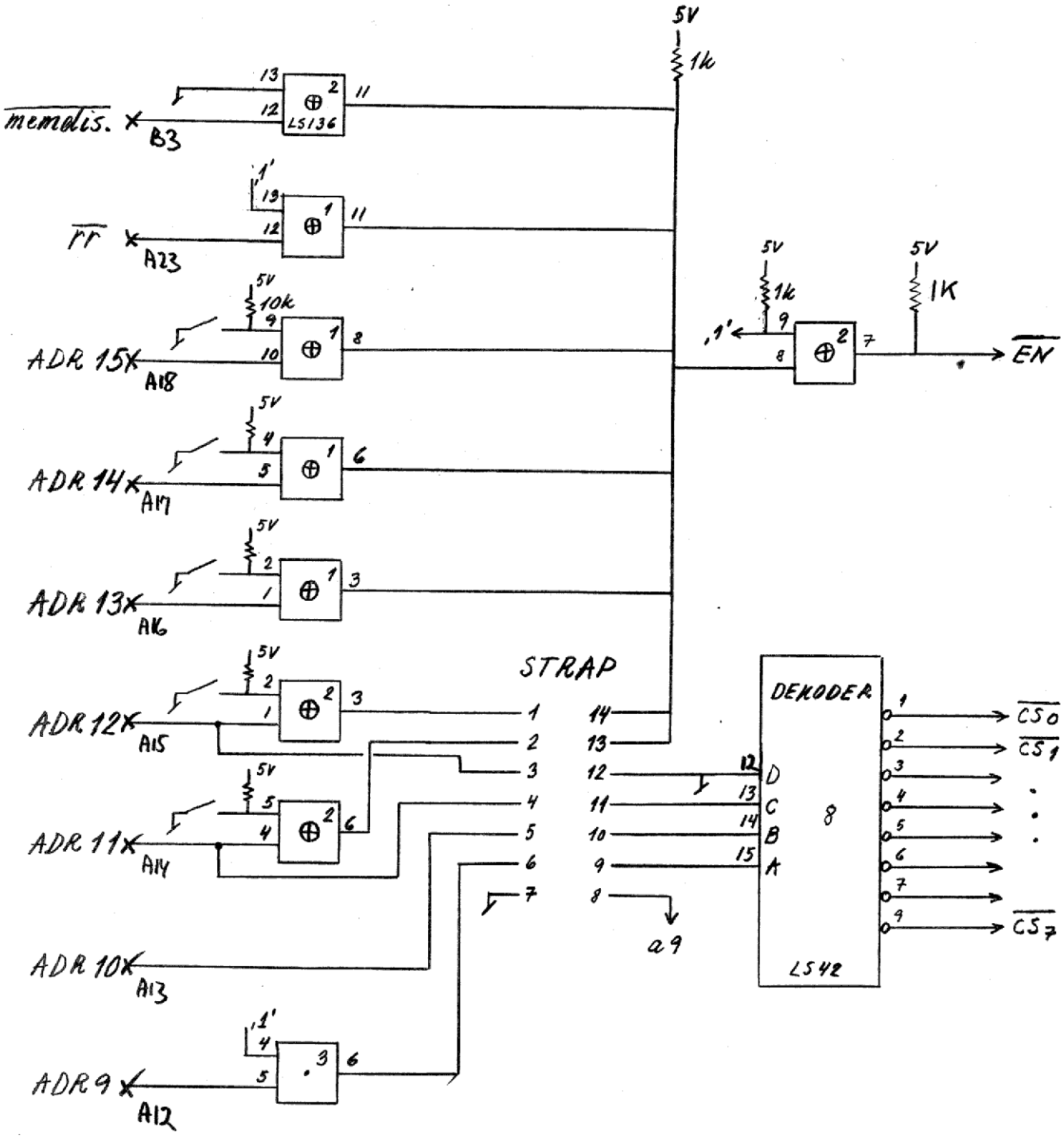
A	B	C	D	
2	4	4	8	k byte

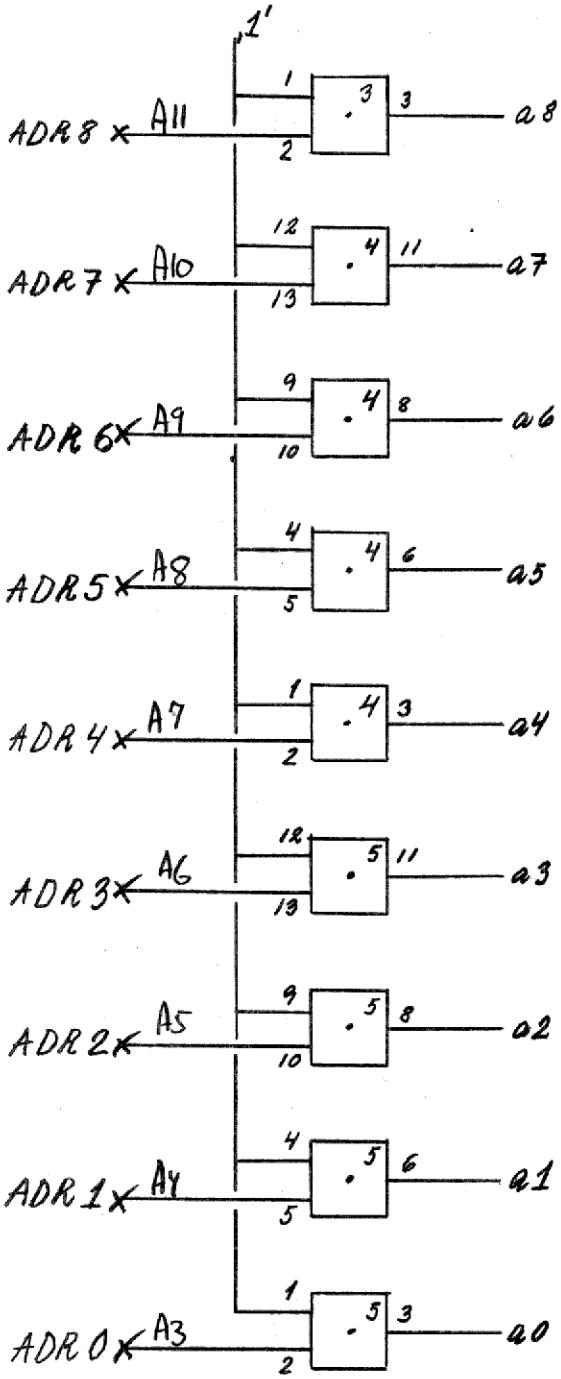
2.3 Strappable options.

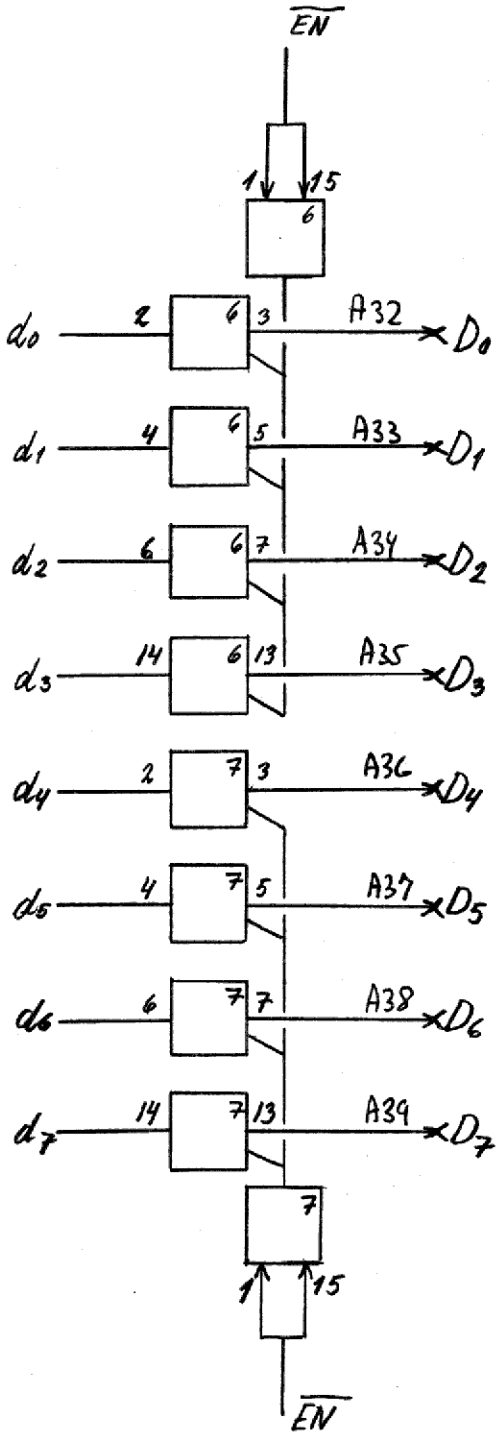
The strap socket situated on the right side of the module, determins the mode as shown in fig 1.

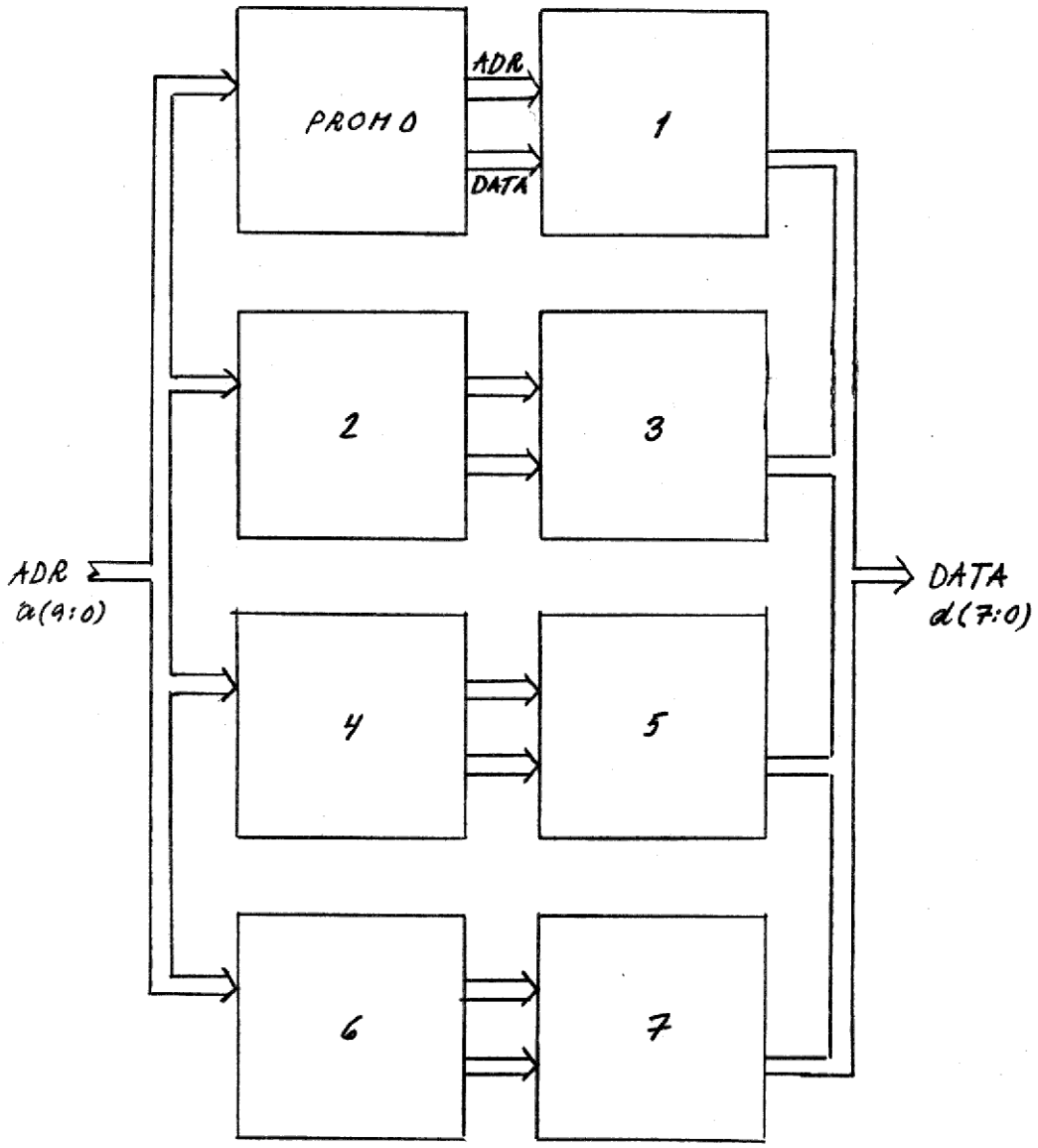


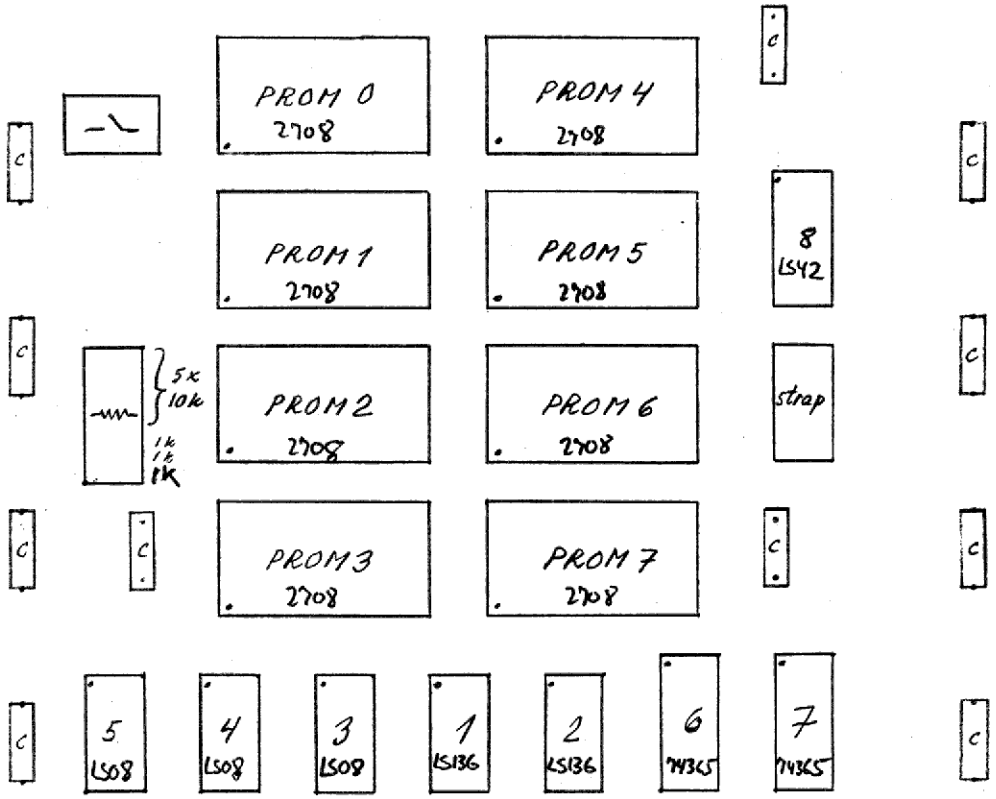

switch register
RR
address
comparator
PROM
MEMORY ARRAY
address
buffers
tristate
buffers
DATA
ADDRESS
1-8 27o4/27o8


5V
1k
memdis.
B3
LS136
'1'
RT
A23
5V
10k
ADR 15X
A18
5V
1k
5V
1K
'1'
EN
ADR 14X
A17
ADR 13X
A16
STRAP
ADR 12X
A15
ADR 11X
A14
ADR 10X
A13
ADR 9X
A12
DEKODER
8
LS42
CS0
CS1
CS7
a9


1'
ADR 8
A11
a8
ADR 7
A10
a7
ADR 6
A9
a6
ADR 5
A8
a5
ADR 4
A7
a4
ADR 3
A6
a3
ADR 2
A5
a2
ADR 1
A4
a1
ADR 0
A3
a0


EN
d0
A32
D0
d1
A33
D1
d2
A34
D2
d3
A35
D3
d4
A36
D4
d5
A37
D5
d6
A38
D6
d7
A39
D7
EN


PROM 0
ADR
DATA
1
2
3
4
5
6
7
ADR
a(9:0)
DATA
d(7:0)


PROM 0
2708
PROM 4
2708
PROM 1
2708
PROM 5
2708
8
LS42
PROM 2
2708
PROM 6
2708
strap
5k
10k
1k
1k
PK
PROM 3
2708
PROM 7
2708
5
LS08
4
LS08
3
LS08
1
LS136
2
LS136
6
74365
7
74365

intel Silicon Gate MOS 2708, 2704

8192/4096 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

- **2708 1024x8 Organization**
- **2704 512x8 Organization**

- **Fast Programming — Typ. 100 sec. For All 8K Bits**
- **Low Power During Programming**
- **Access Time — 500 ns**
- **Standard Power Supplies — +12V, ±5V**
- **Static — No Clocks Required**
- **Inputs and Outputs TTL Compatible During Both Read and Program Modes**
- **Three-State Output — OR-Tie Capability**

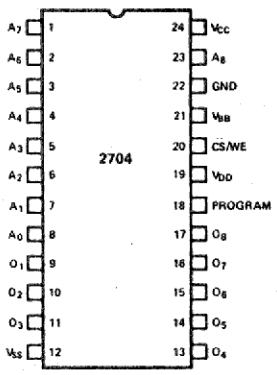
ROMs

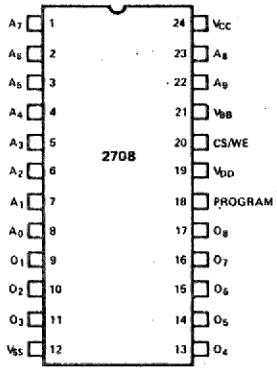
The Intel 2708/2704 are high speed 8192/4096 bit erasable and electrically programmable ROMs.

The 2708/2704 are packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

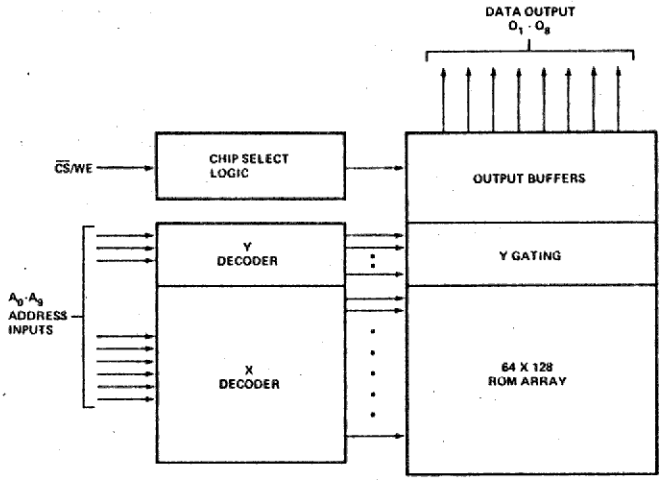
A mask programmable ROM, the Intel 2308, is available for volume production runs of systems initially using the 2708/2704.

PIN CONFIGURATIONS





BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
CS	CHIP SELECT INPUTS