DANSK DATA ELEKTRONIK

ID-7003 INTERRUPT PRIORITY MODULE

for the

ID-7000 MICROPROCESSOR SYSTEM

December 1975

author: Ole Lading

1.Function.

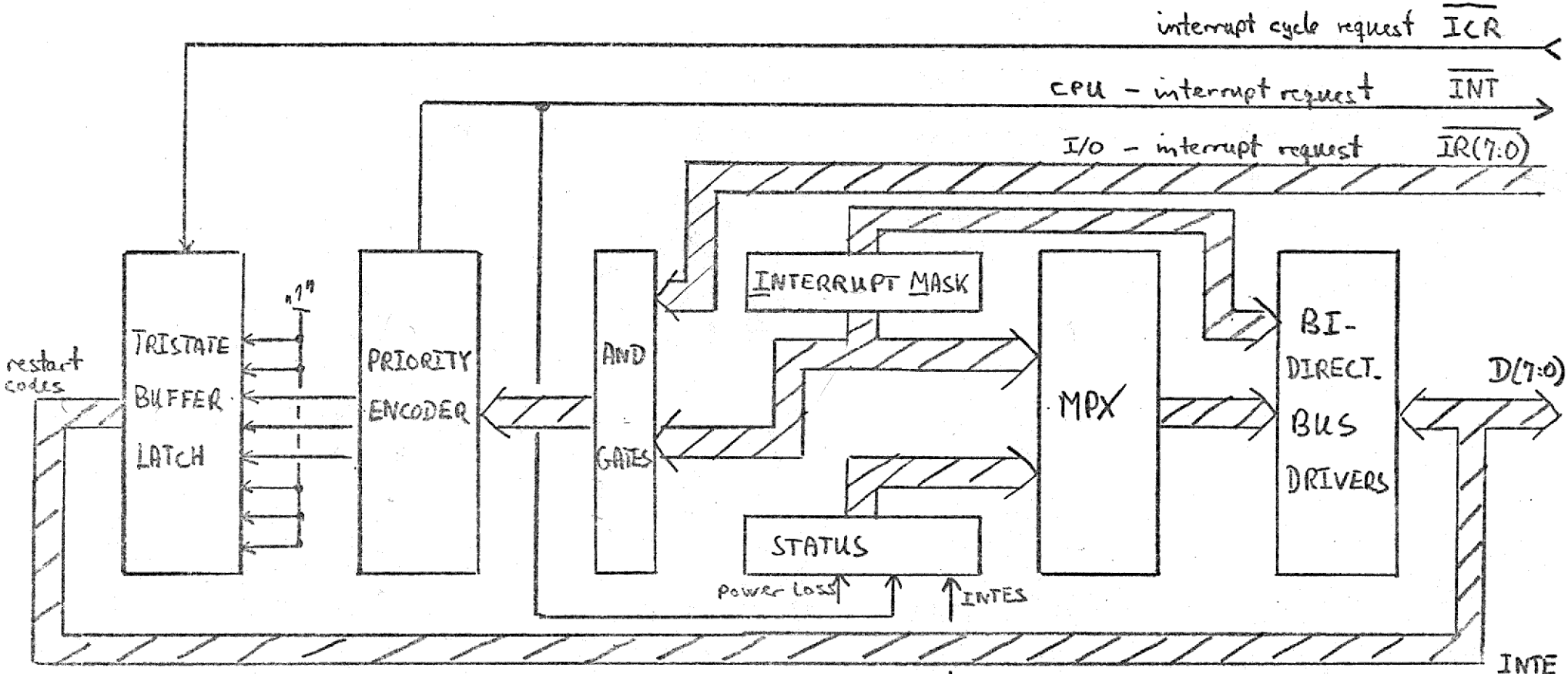
The ID-7003 Interrupt Priority module is used in configurations where I/O-modules must be served by means of interrupts. The module plugs into the ID-7000 bus system at any location. It is able to deal with incoming interrupt request lines $\overline{IR}(7:0)$ at 8 priority levels. The module sends an interrupt request to the CPU-module (via $\overline{INT}$) if at least one enabled interrupt request line is activated. The CPU-module replies to this by executing an interrupt-acknowledge machine cycle. In this cycle, the ID-7003 generates a restart instruction (RST 0,1,...7) corresponding to the interrupt request with highest priority. When the CPU replies to the interrupt request, the internal interrupt enable flip-flop of the 8080A is cleared to prevent more interrupts from being served. Acknowledgement of the interrupting I/O-unit and re-enabling of the interrupt system is under program control.

The ID-7003 Interrupt Priority module contains an interrupt mask register for selective enabling/disabling of the different priority levels. Loading and storing of the interrupt mask register is under program control. The module contains logic to sense the status of the internal interrupt enable flip-flop and the $\overline{powerloss}$ line from the system power-supply.

The drivers of the interrupt request lines, $\overline{IR}(7:0)$, on the different I/O-modules are of the open collector type (with pull-up resistors on the ID-7003 module). This allows for a maximum of 8 interrupt sources to be connected to a single interrupt request line. In this way, the maximum number of direct interrupt sources in the ID-7000 microprocessor system becomes 64.

Figure 1 shows a blocked schematic of the module.

Appendix 1 contains the detailed logic diagram of the module.



OUT 254 :	IM(7:0)	write IM(7:0)
OUT 255 :		Sample INTE
IN 254 :	IM(7:0)	read IM(7:0)
IN 255 :	0 0 0 0 0 POWER LOSS INT INTES	read STATUS

Fig. 1

2. Programming description.

2.1 Interrupt priority: The ID-7003 Interrupt Priority module receives interrupt requests on the 8, active low, interrupt request lines $\overline{IR}(7:0)$ in the bus system. The module generates a RST-instruction corresponding to the activated interrupt request line with highest priority as follows:

$\overline{IR}(0)$: RST 0 instruction, highest priority
$\overline{IR}(1)$: RST 1 instruction
$\overline{IR}(2)$: RST 2 instruction
$\overline{IR}(3)$: RST 3 instruction
$\overline{IR}(4)$: RST 4 instruction
$\overline{IR}(5)$: RST 5 instruction
$\overline{IR}(6)$: RST 6 instruction
$\overline{IR}(7)$: RST 7 instruction, lowest priority

2.2 Interrupt Mask register. The interrupt mask register IM(7:0) controls selective enabling/disabling of the different interrupt request lines (interrupt levels). The interrupt mask register IM(7:0) is loaded from the accumulator of the CPU by the OUT 254 instruction. Execution of the IN 254 instruction transfers the contents of theinterrupt mask register IM(7:0) to the accumulator.

IM(7)	IM(6)	IM(5)	IM(4)	IM(3)	IM(2)	IM(1)	IM(0)
7	6	5	4	3	2	1	0

2.3 Control word. Execution of the OUT 255 instruction (contents of the accumulator irrelevant), causes transfer of the contents in the internal interrupt enable flip-flop,INTE,into a flip-flop, INTES, on the ID-7003 module. The INTES flip-flop is a part of the module status word (see section 2.4). Special logic on the module makes the OUT 255 instruction a non-interruptable instruction. This ensures that the succeeding instruction is always executed.

The purpose of these features is to allow a monitor program to sample the contents of the internal interrupt enable flip-flop before disabling the interrupt system. After this the monitor can read the previous status of the interrupt enable flip-flop, as shown in the following example:

```
MONITOR_ENTRY: OUT 255
               DI
               PUSH PSW
               PUSH B
               PUSH D
               PUSH H
               IN 255
               .
               .
```

2.4 Status word. Execution of the IN 255 instruction transfers the contents of the module's statusword to the accumulator in the CPU. The status word contains the following information:

bit 0: INTES — This status bit indicates the contents of the internal interrupt enable flip-flop of the CPU as sampled by the execution of the latest OUT 255 instruction.
0: Interrupt system was disabled.
1: Interrupt system was enabled.

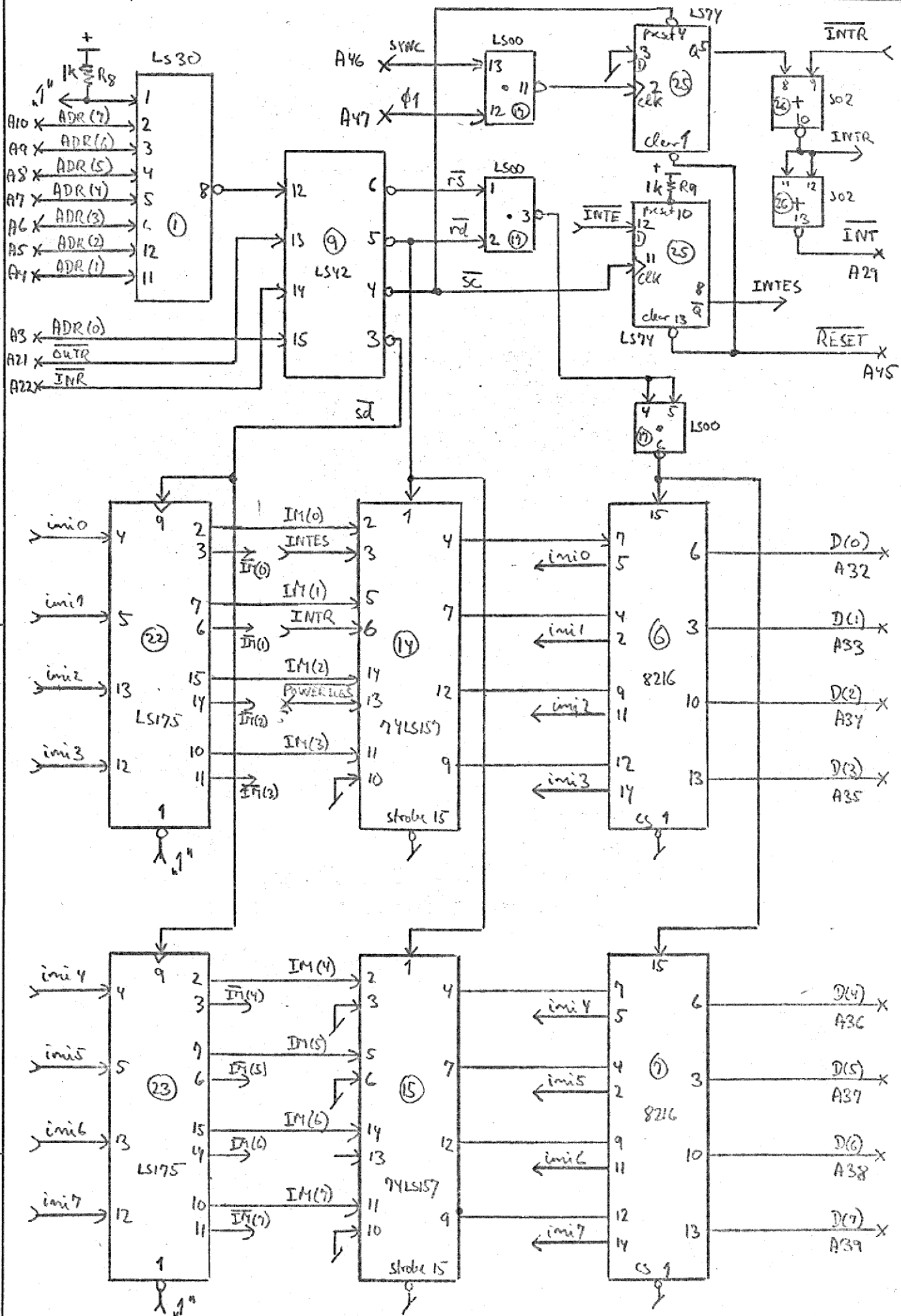
bit 1: INTR — This signal from the interrupt priority logic indicates, when logical one, that at least one IM(i)*IR(i) equals logical one (i=0,1....7).

bit 2:	$\overline{\text{POWERLOSS}}$ *)	This status bit, connected to the $\overline{\text{powerloss}}$ line of the system power supply, indicates the power situation: 0: Powerloss error. 1: Power OK.
bit 3-7		undefined, reserved for future use.

---

*) By means of a strap on the module, the $\overline{\text{powerloss}}$ line may be connected to the $\overline{\text{IR}}(0)$ request line.

Navn	Lb. nr.	Dato	Emne	Fag	Afd.	Side
ID-7003 INTERRUPT PRIORITY module, Logic schematic	Ole Lading	14-6-75	ID-7000 system.	page 1 of 2		



Navn	Lb. nr.	Dato	Emne	Fag	Afd.	Side
ID-7003, INTERRUPT PRIORITY module, Logic Schematic	Ole Lading	14-6-75	ID-7000 system	page 2 of 2