DANSK DATA ELEKTRONIK

ID-7004 ASYNCHRONOUS DATA COMMUNICATION module for the ID-7000 MICROPROCESSOR SYSTEM

December 1975

Ole Lading
rev. 22-2-77

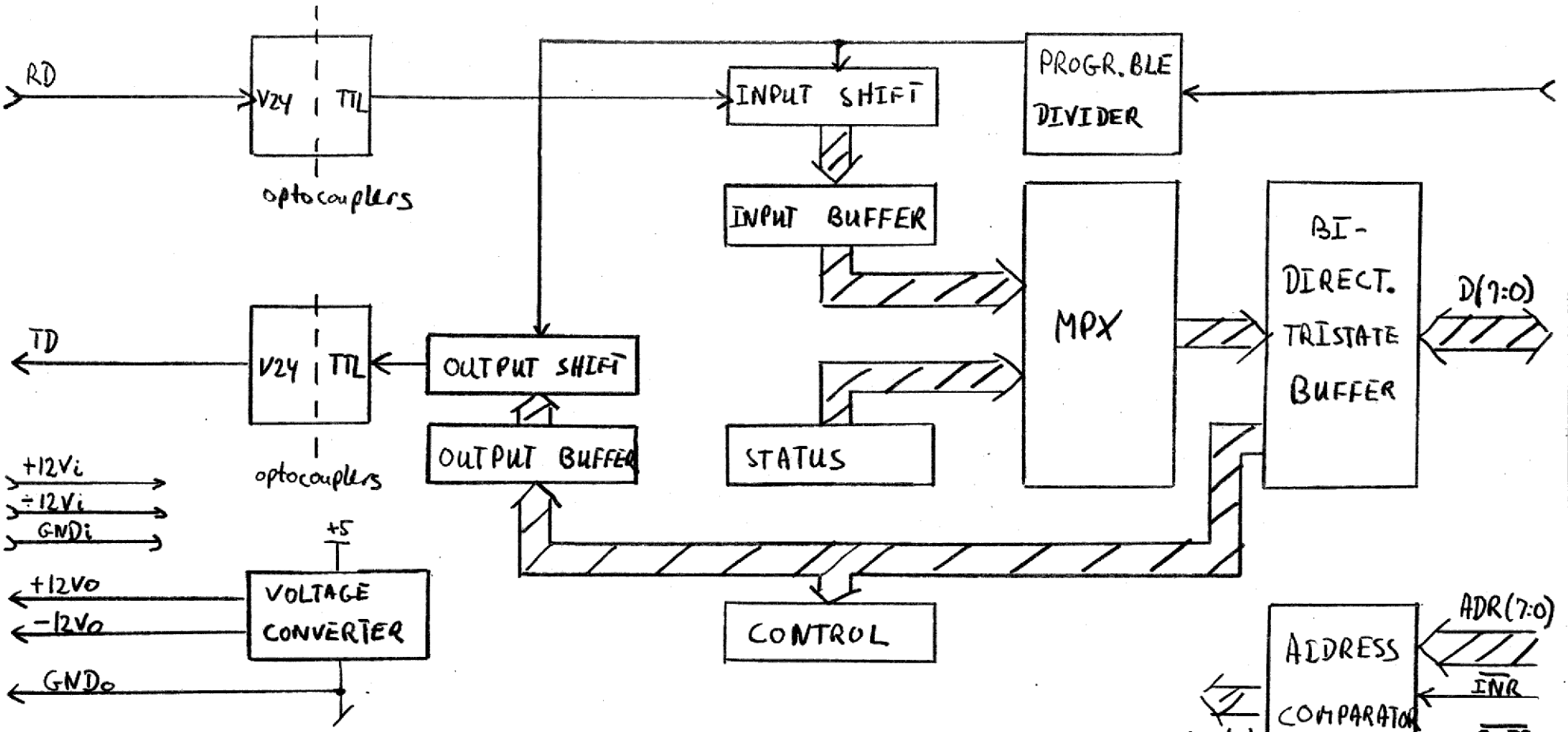
1. Function. The function of the ID-7004 Asynchronous Data Communication module is to connect data communication equipment such as teletypewriters, CRT terminals or modems to the ID-7000 microprocessor system. The module plugs into any position in the bus system. The data communication equipment is connected to the top connector of the module. The interface to the data communication equipment is in accordance to the CCITT V24 (or EIA RS-232) standard and the TTY 20mA current loop standard.

Straps on the module allow a baud rate to be selected in the range from 75 to 9600 bits/sec. By means of a control word from the computer, the module can be programmed to use different character formats.

The data communication interfacing is perfomed by optocouplers, thus achieving total electrical isolation of the communication equipment from the microprocessor system.

Programs can drive the module by utilising the contents of the module's status word,or by means of interrupts. Seperate interrupt flip-flops are provided for read and write operations.

Figure 1 shows a blocked schematic diagram of the module.Appendix 1 contains the detailed logic diagram of the module. Appendix 2 contains a functional description and a data sheet for the universal asynchronous receiver/ transmitter-chip (UAR/T) used on the module.



OUT 2n	WRITE DATA	write data + clear WFF
OUT 2n+1	clear WFF | clear RFF | // | NP | TSB | EPS | NB2 | NB1	write control
IN 2n	READ DATA	read data + clear RFF
IN 2n+1	WFF | RFF | EOC | DA | OR | FE | PE | TBMT	read status

Navn ID 7004. Asynchronous communication module.

Lb. nr.

Dato

Emne

Fag

Afd.

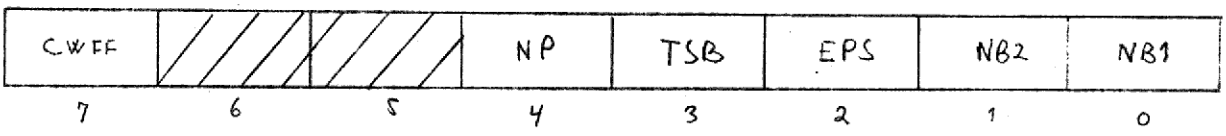
Side 2

2. Programming Description.

2.1 Addressing. The module uses two consecutive I/O addresses. A switch register on the module is used to select the module's base address,which must be an even address. Input and output to the even address of the module transfers a data word between the accumulator of the CPU and the module. Input from the next (odd) address of the module reads the statusword. Output to the odd address transmits a control word to the module.

2.2 Control word. An 8 bit control word determines the characteristics of the received/transmitted serial data to/from the module, and controls the clearing of the write interrupt flip-flop WFF (withour starting a new transmission). The control word is loaded by execution of an OUT-instruction to the odd address of the module.

The specifications of the control word are:



bit 7: CWFF — 1: Write interrupt flip-flop (WFF) is cleared.
0: No change in WFF.

bit 6-5: not used

bit 4: NP — 1: No Parity; parity bit not generated by transmitter and tested by receiver.

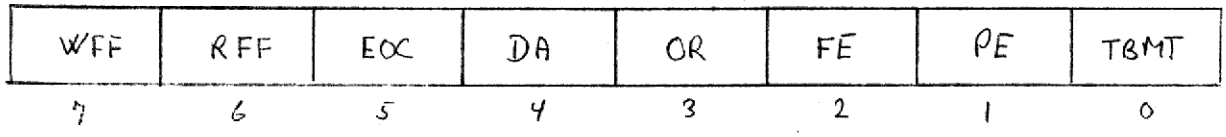
bit 3: TSB — The value of this bit determines the number of stop-bits generated by transmitter and expected by receiver.
0: 1 stop bit
1: 2 stop bits

bit 2: EPS — The value of this bit determines the parity mode used:
1: Even Parity Status
0: Odd Parity Status

bit 1-0:NB2,NB1 — These bits determine the number of data bits
NB2,NB1: 00: 5 data bits/character
01: 6 data bits/character
10: 7 data bits/character
11: 8 data bits/character

2.3 Status word
This 8-bit word contains the status of the module, and can be read by execution of an IN-instruction to the odd address of the module.

The status word contains the following information



bit 7: WFF	The content of the write interrupt flip-flop (see section 2.4)
bit 6: RFF	The content of the read interrupt flip-flop (see section 2.4)
bit 5:EOC	This status bit is o while a character transmission is going on. After this it enters the 1-state.
bit 4:DA	This status bit is set when a full character has been received and transferred to the input buffer register. It is reset when the dataword is fetched by the CPU by an IN-instruction.
bit 3:OR	This status bit is set when a data overun has occurred, i.e. when a new character is received and transferred to the input buffer register before the old character has been fetched by the CPU.
bit 2: FE	This status bit is set when an illegal stop bit state is detected by the receiver.
bit 1: PE	This status bit is set when the parity of the received character does not correspond to the programmed parity mode.
bit 0: TBMT	This status bit is set when the output buffer register may be loaded with a new character from the CPU.

2.4 Data word.

The data bits transmitted by the module are the n least significant bits of the data word,where n is determined by bit 1 and o of the control word (NB2,NB1). The least significant bit is the first transmitted databit. The received characters are right justified in the dataword with the first received bit in the LSB-position. The unused bits in the data word are set to logical 0.

The serial bit format for a single character transmission is shown in fig. 2.

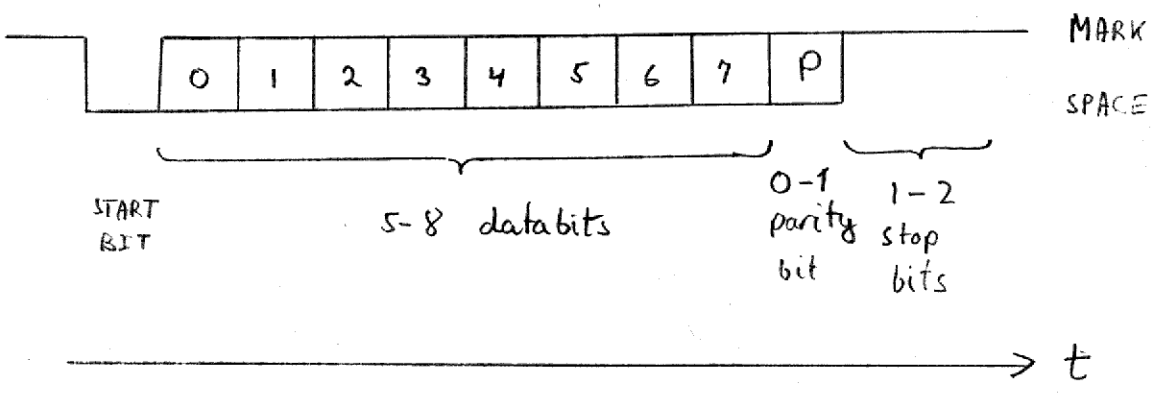


fig.2

2.5 Interrupt.

The module contains two separate interrupt flip-flops for read and write operations, RFF and WFF. By means of a strap socket on the module these interrupt flip-flops can be connected to any of the 8 interrupt request lines on the bus. The output buffers from the flip-flops are open collector, to allow several interrupt flip-flops to share common interrupt request lines.

The read interrupt flip-flop is set, when a character from the data comminication equipment is received and transferred to the input buffer. It is cleared when the contents of the input buffer are transferred to the CPU by an input instruction.

The write-interrupt flip-flop is set, when the output buffer is ready to receive a new character from the CPU. It is cleared when the CPU transfers a new character to the output buffer or when a control word containing a logical 1 in bit 7 is sent.

3. Straps and connections.

3.1 Interrupt strapping. By means of a dual-in-line socket near the bus connector of the module, the read and write interrupt flip-flops of the module can be connected to any of the 8 interrupt request lines in the bus. The connections are made with a component board plugged into the socket. Fig. 3 shows the connections to the socket:

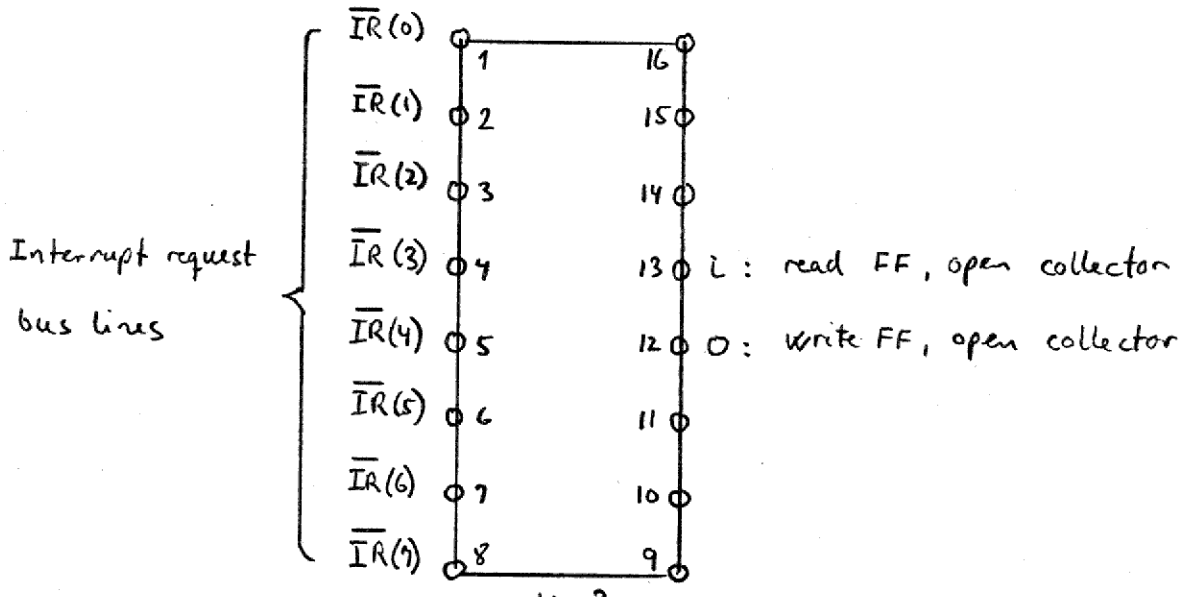


fig. 3

3.2 Baud-rate strapping. By means of a dual-in-line socket near the top connector of the module, a baud rate between 75 bits/sec. and 9600 bits/sec. can be selected for the serial data transmission. Two straps determine the modulus of a programable counter to obtain the two basic baud ranges of 75bits/sec. or 110 bits/sec. Two more straps are used to connect the appropriate outputs from the counter to the clock inputs for the UAR/T chip (TCP and RCP). Fig. 4 shows the connections to the socket:

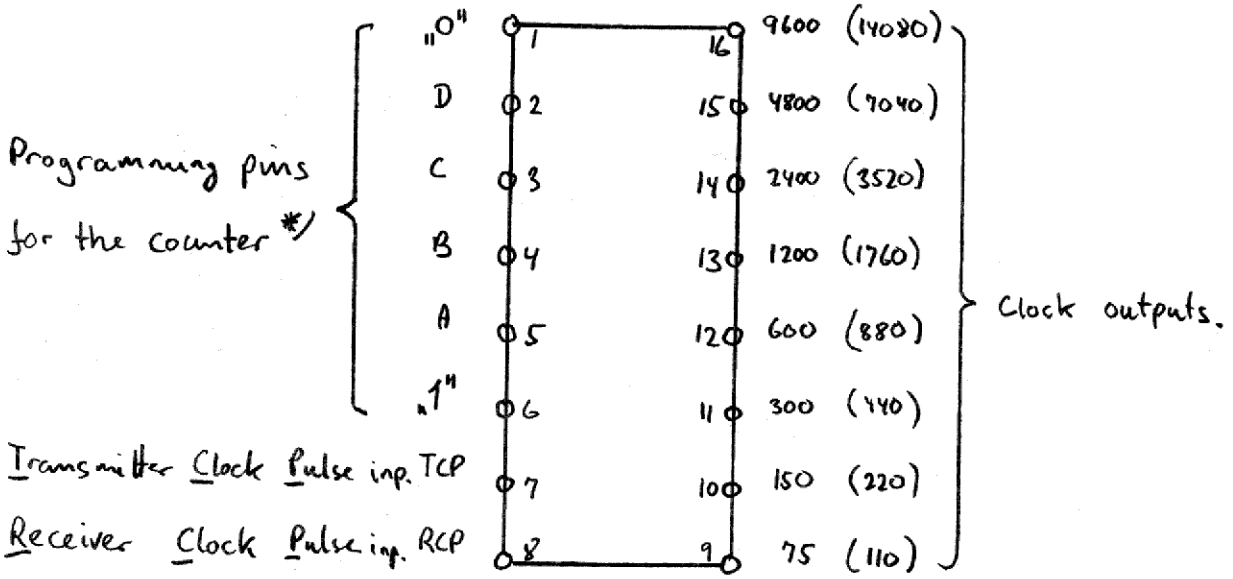


fig. 4

3.3 Communication equipment connection. The connection to the data communication equipment is made via the top connector of the module. The interface is in accordance with the CCITT V24 (or EIA RS-232) standard and the tty 20mA current loop standard. The top connector is connected to the rest of the module through opto-couplers. When the module is supplied from an external ± 12V power supply, total electrical isolation between the communication equipment and the microprocessor system is achieved, but the interface circuits can also be supplied from an on-board ± 12V power supply.

Table 1 gives the pin connections used in the top connector.

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*/ A basic frequency of 75 bits/sec is obtained when DCBA=0011 (pins 1,2,3 strapped together and pins 4,5,6 strapped together.).

A basic frequency of 110 bits/sec is obtained when DCBA=0111 (pins 1,2 strapped together and pins 3,4,5,6 strapped together).

pin nr.	signal name	description.
D	CLI	current loop input
K	GNDI	input ground
M	RDI	read data , V24
N	-12VI	input -12V
R	+12VI	input +12V
T	TDO	transmitted data output , V24
U	+12VO	output +12V
W	-12VO	output -12V
X	GNDO	output gnd
Z	TDI	transmitted data input (for current loop conversion)
b	CLO	current loop output.

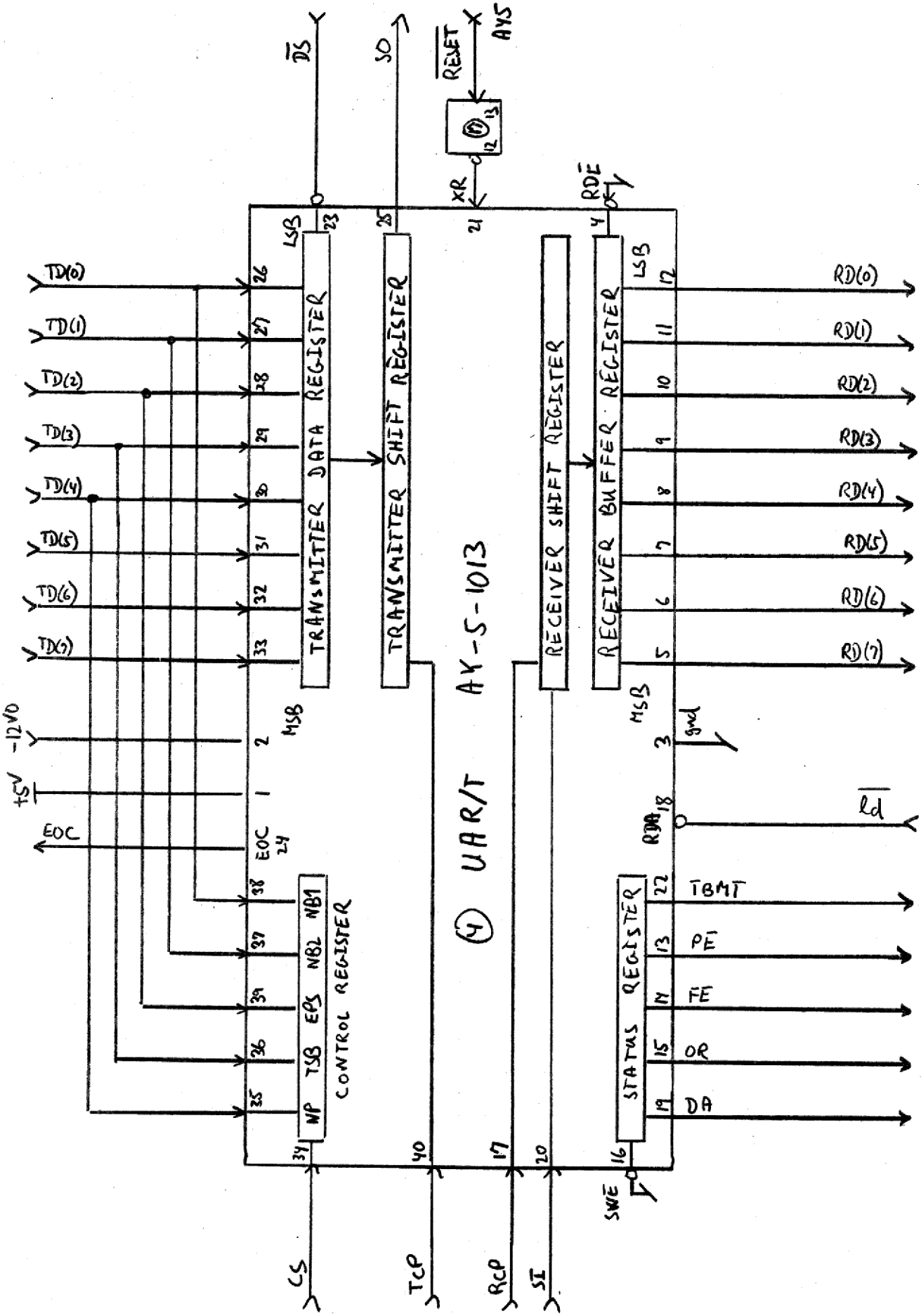
Table 1.

When an external $\pm$ 12 V power supply is used, it is connected to pin K , N and R. When no external power supply is used, connections K→X, N→W and R→U have to be made in the cable connector.

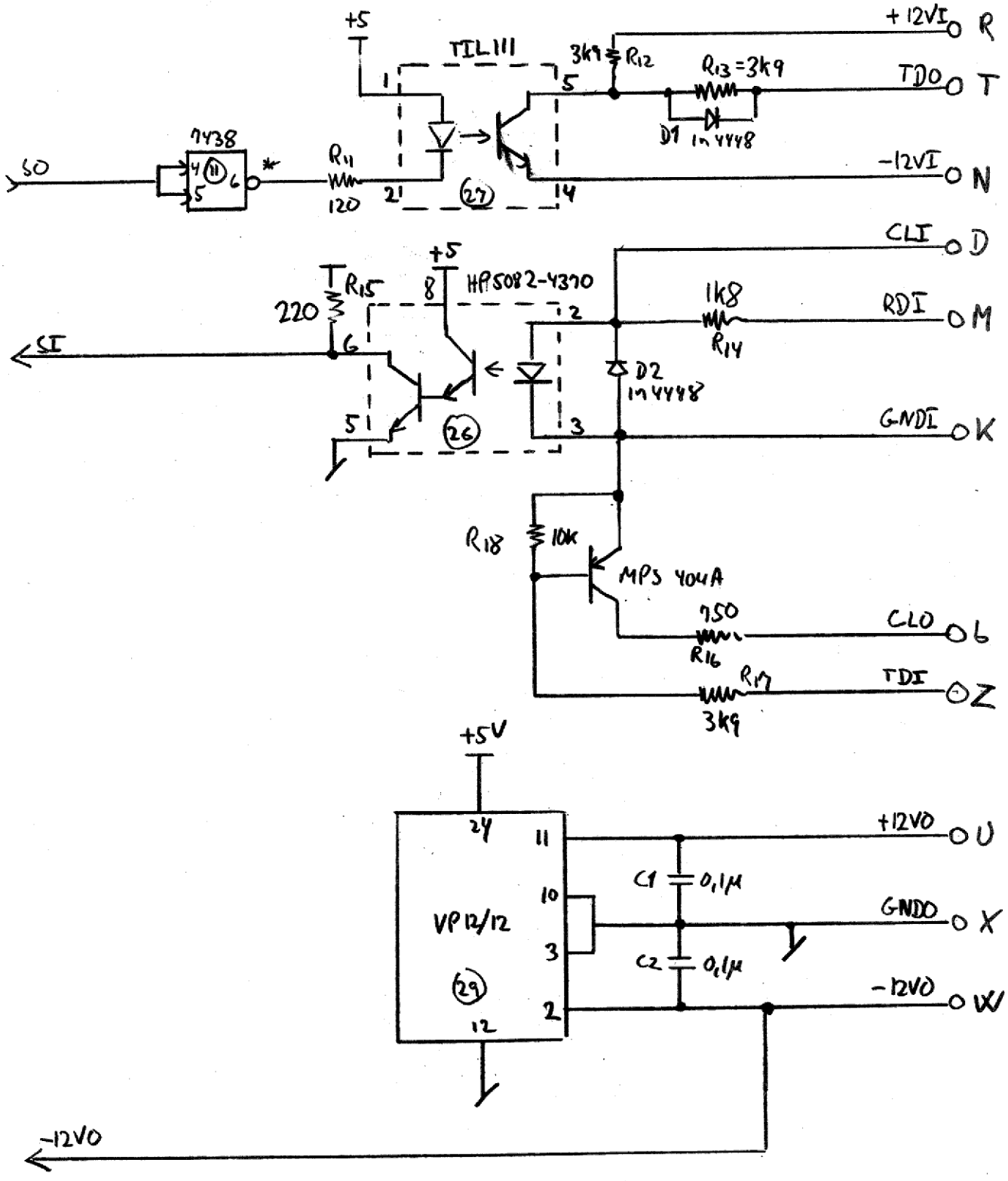
When the V24 standard is used, pins M and T are used for data connections with K (K→X) as common ground

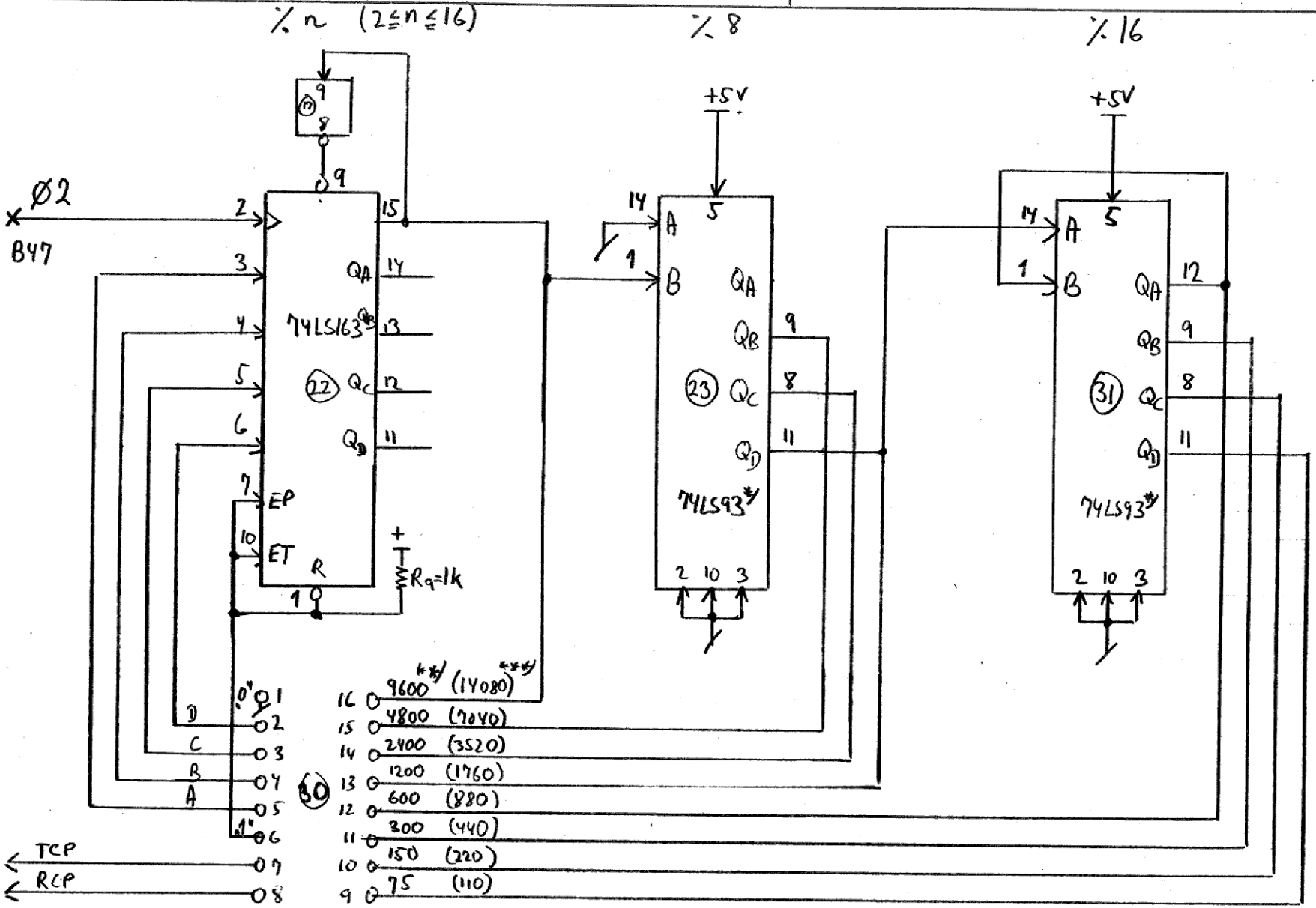
When the current loop (in serial with a 680Ω resistor) standard is used, pin M is connected to the + 12V supply (R or R→U) and pin D is used as the positive current loop input. The negative current loop input is connected to the - supply (W or W→N). The current loop output is obtained by connecting T→Z. The positive current loop output terminal is then b. The negative current loop output terminal is the - 12V supply (N or N→W).

Navn	Lb. nr.	Dato	Emne	Fag	Afd.	Side
ID-7004 Asynchr. com. mod. UART		7-6-75	ID-7000 syst.		OL	A1.1



Navn	Lb. nr.	Dato	Emne	Fag	Afd.	Side
ID-7004 Async. comm. mod. I/O-interface.		7-6-75	ID-7000 syst.			A1.2





*) 74LS93 has Vcc on pin 5 and gnd on pin 10.

**) DCBA = 0011 (divide by 13)

***) DCBA = 0111 (divide by 9)

Navn: ID-7004, Asynchronous comm. module, clock counter

Lb. nr.

Dato

Emne: ID-7000 syst.

Fag

Afd.: OL

Side: A3

Emne: ID-7004 Async. com. module

Addr. comp., busdrivers, interrupt logic

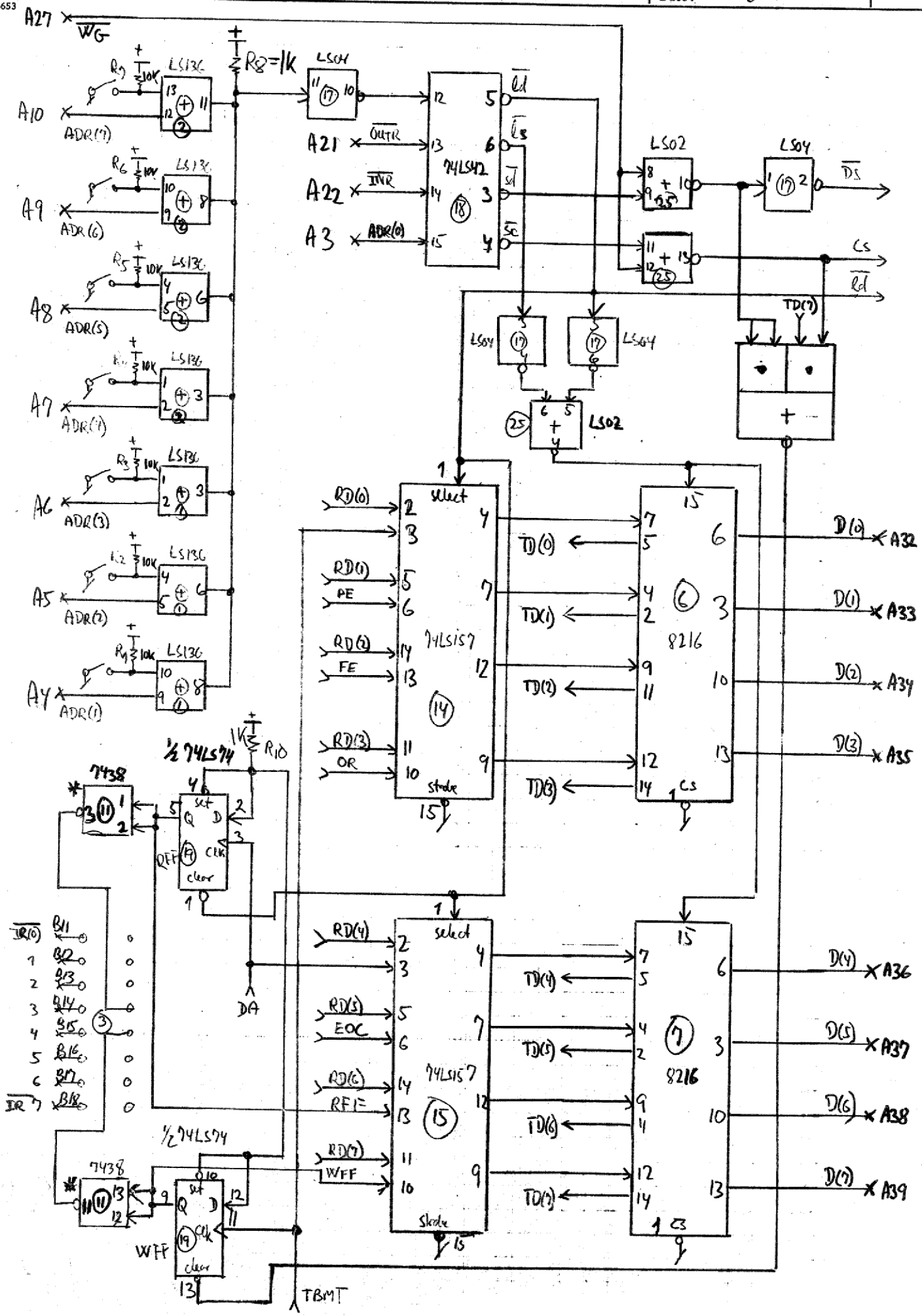
Dok. nr.:

Navn: Ole Lading

Dato: 7-6-75

Side A1.4 ud af sider

Un 04-653



AY-5-1013/AY-5-1013A

UAR/T UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

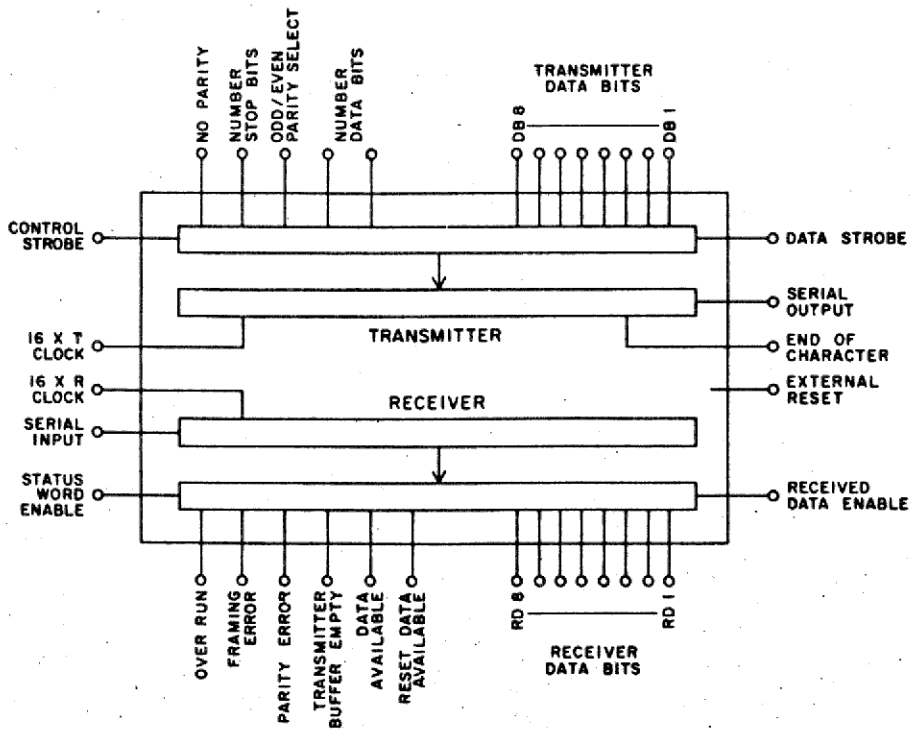
FEATURES

- DTL and TTL Compatible—no interfacing circuits required—drives one TTL load.
- Fully Double Buffered—eliminates need for system synchronization, facilitates high speed operation.
- Full Duplex Operation—can handle multiple baud rates (receiving-transmitting) simultaneously.
- Start Bit Verification—decreases error rate with center sampling.
- The receiver will strobe the input bit within ±4% of the theoretical centre.
- External reset of error flags.
- High Speed Operation—greatest through-put; 40k baud
- Tri-State Outputs—bus structure capability.
- Low Power—minimum power requirements.
- Input Protected—eliminates handling problems.
- Hermetic DIP Package—easy board insertion and mechanical handling.

GENERAL DESCRIPTION

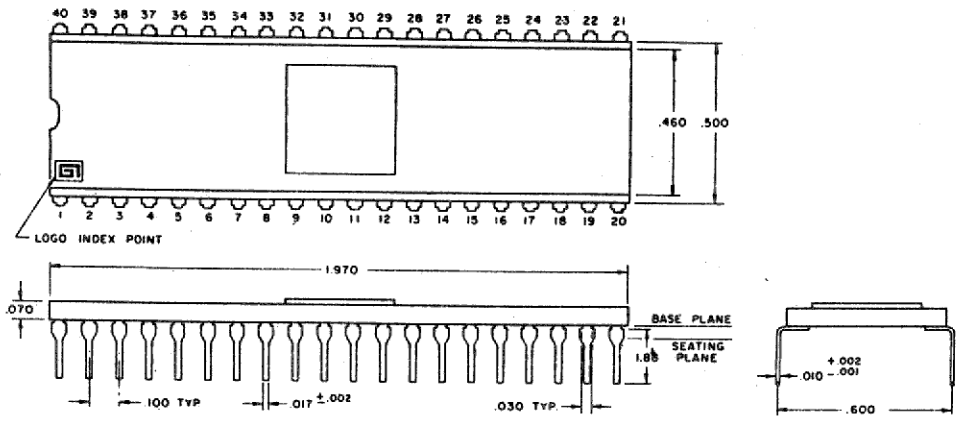
The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits, and either odd/even parity or no parity. In order to make the UAR/T universal, the baud rate, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip utilizing MTNS P-channel enhancement mode transistors. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL logic without the need for interfacing components and with all strobed outputs having tri-state logic.

FIGURE 1
BLOCK DIAGRAM



PIN CONFIGURATION
AY-5-1013

PACKAGE: 40 LEAD DUAL IN-LINE



All dimensions in inches

DESCRIPTION OF PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	V_{CC} Power Supply	V_{CC}	+5V Supply
2	V_{GG} Power Supply	V_{GG}	−12V Supply
3	Ground	V_{GR}	Ground
4	Received Data Enable	$\overline{RDE}$	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits	RD8-RD1	These are the 8 data output lines. Received characters are right justified, the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when RDE is "0" and a high impedance state when RDE is "1". Thus, the data output lines can be bus structure oriented. Unused outputs go to an active "0" when enabled.
13	Receive Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run	OR	This line goes to a logic "1" if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	Status Word Enable	$\overline{SWE}$	A logic "0" on this line places the status word bits (PE, FE, OR, DA, TBMT) onto the output lines. Tri-state.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data Available	$\overline{RDA}$	A logic "0" will reset the DA line. DA FF is only thing that is reset.
19	Receive Data Available	DA	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig. 13.

Pin No.	Name	Symbol	Function
20	Serial Input	SI	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 12, 13.
21	External Reset	XR	Resets shift registers. Sets SO, EOC, and TBMT to a logic "1". Resets DA, and error flags to "O" . Clears input data buffer. Must be tied to logic "O" when not in use.
22	Transmitter Buffer Empty	TBMT	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 29, 21.
23	Data Strobe	$\overline{DS}$	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS. Data must be stable during entire DS.
24	End of Character	EOC	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 18, 20.
25	Serial Output.	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig. 17.
26-33	Data Bit Inputs	DB1-DB8	There are up to 8 data bit input lines available.
34	Control Strobe	CS	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity	NP	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits	TSB	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Bits/Character	NB2, NB1	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character.
39	Odd/Even Parity	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock Line	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

NB1	NB2	Bits/Character
0	0	5
1	0	6
0	1	7
1	1	8

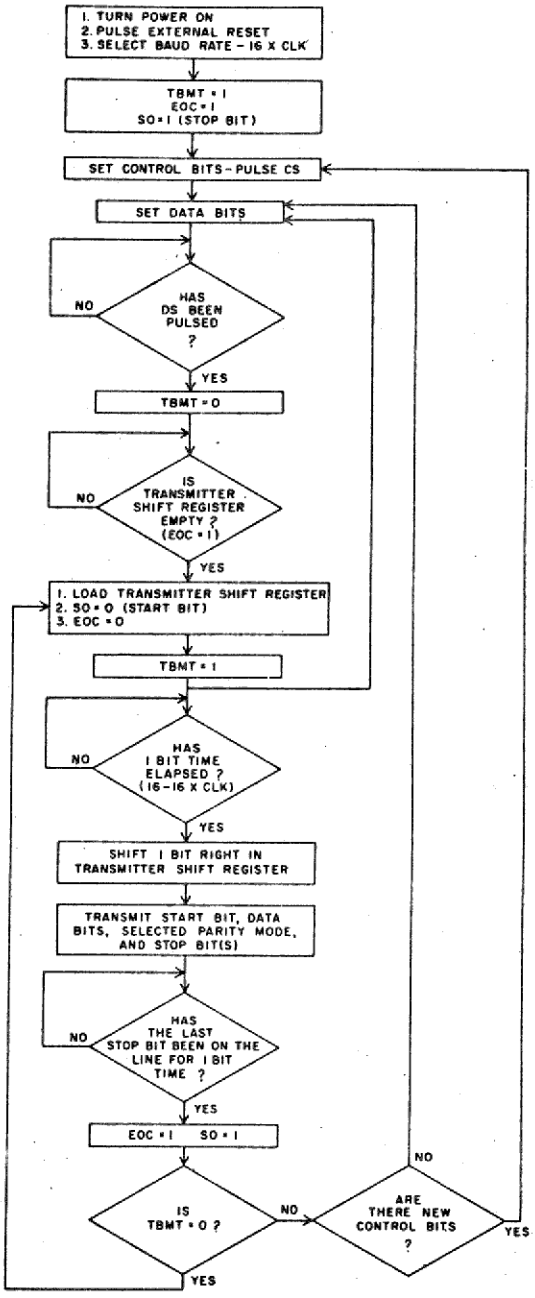
TRANSMITTER OPERATION
FIGURE 2

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occuring before data bits selection. However, one may set both DS and CS simultaneously if minimum pulse width specifications are followed. Once data strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding registar is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.



RECEIVER OPERATION
FIGURE 3

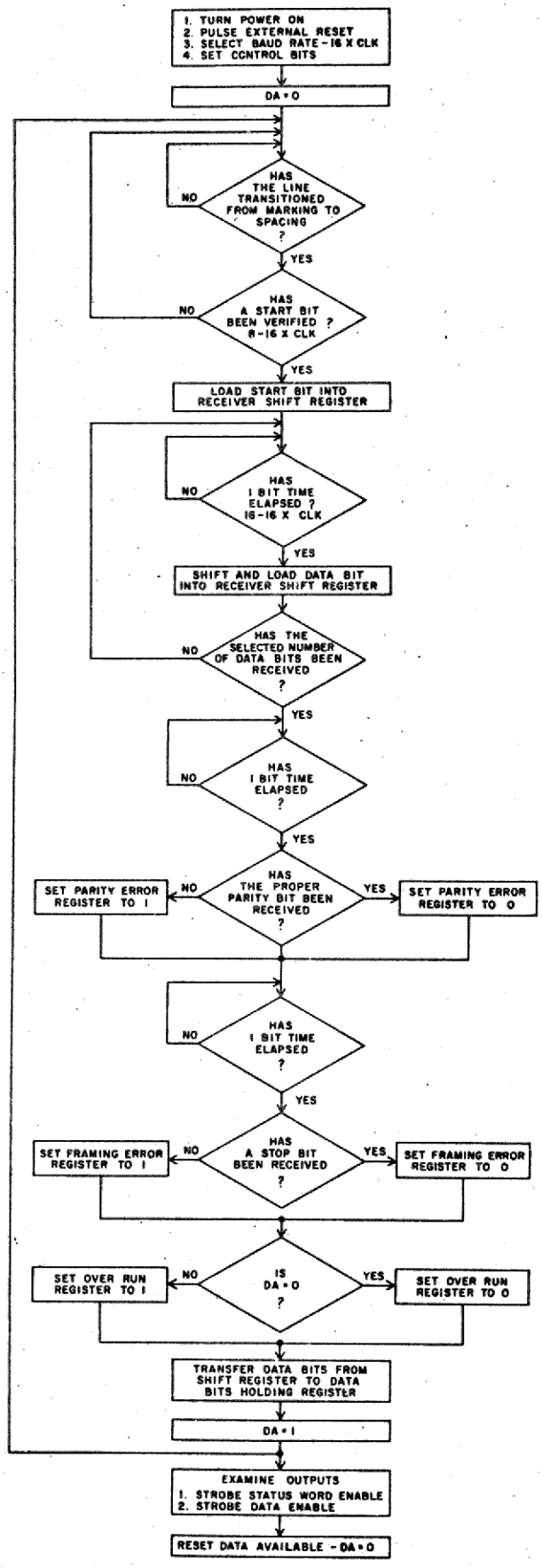
Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DA) to a logic "0".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DA) signal to determine if data has been the read out. If the DA signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DA signal is at a logic "0" the receiver will assume that data has been read out. After DA goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{GG} (with respect to V_{CC}) . . . . . −25 to +0.3V
Clock and logic input voltages (with respect to V_{CC}) . . . . . −25 to +0.3V
Storage Temperature . . . . . −55°C to 150°C
Operation Temperature . . . . . 0°C to 70°C
Lead Temperature (Soldering, 10 sec) . . . . . 330°

STANDARD TEST CONDITIONS

The following characteristics apply for any combination of the following test conditions, unless otherwise noted. All voltages are measured with respect to ground. Positive current is defined as flowing into the referenced pin.

$V_{GG} = -12V \pm 5\%$ $V_{CC} = 5V \pm 5\%$ $0°C < T_A < 70°C$

ELECTRICAL CHARACTERISTICS (see standard conditions)

PARAMETER	CONDITIONS AND COMMENTS	MIN.	TYP.	MAX.	UNITS
Input Logic Levels					
Logic 0	V_{IL} (I_{IL} = −1.6mA)	0	–	0.8	volts
Logic 1	V_{IH} Unit has internal pullup resistors	V_{CC}−1.5	–	V_{CC}+0.3	volts
Input Capacitance					
All Inputs	0 volts bias, f = 1MHz	–	–	20	pF
Leakage Currents					
Tri-State Outputs	0 volts	–	–	1.0	μA
Data Output Levels					
Logic 0	I_{OL} = 1.6mA (sink) V_{CC} max.	–	–	+0.4	volts
Logic 1	I_{OH} = −.3mA (source)	V_{CC}−1.0			volts
Output Capacitance		–	10	15	pF
Short Circuit Current	See Fig. 24			–	
Power Supply Current					
V_{GG} 25°C	See Fig. 26a } All inputs high	–	14	16	mA
V_{CC}	See Fig. 26b }	–	18	20	mA
A.C. CHARACTERISTICS	T_A = 25°C, Output load capacitance 50pF max.				
AY-5-1013					
Maximum Clock Freq.				480	KHz
Maximum Baud Rate				30	K Baud
Minimum Clock Freq.		DC			
AY-5-1013A					
Maximum Clock Freq.				640	KHz
Maximum Baud Rate				40	K Baud
Minimum Clock Freq.		DC			
Pulse Width					
Clock Pulse	See Fig. 10	1.0	–	–	μS
Control Strobe	See Fig. 16	300	–	–	nS
Data Strobe	See Fig. 15	200	–	–	nS
External Reset	See Fig. 14	500	–	–	nS
Status Word Enable	See Fig. 22	500	–	–	nS
Reset Data Available	See Fig. 23	250	–	–	nS
Received Data Enable	See Fig. 22	500	–	–	nS
Set Up & Hold Time					
Input Data Bits	See Fig. 15	>0	–	–	nS
Input Control Bits	See Fig. 16	>0	–	–	nS
Output Propagation Delay					
TPD0	See Fig. 22 & 25		–	500	nS
TPD1	See Fig. 22 & 25 Output Load Capacitance 50 pf		–	500	nS

FIGURE 4 TRANSMITTER–BLOCK DIAGRAM

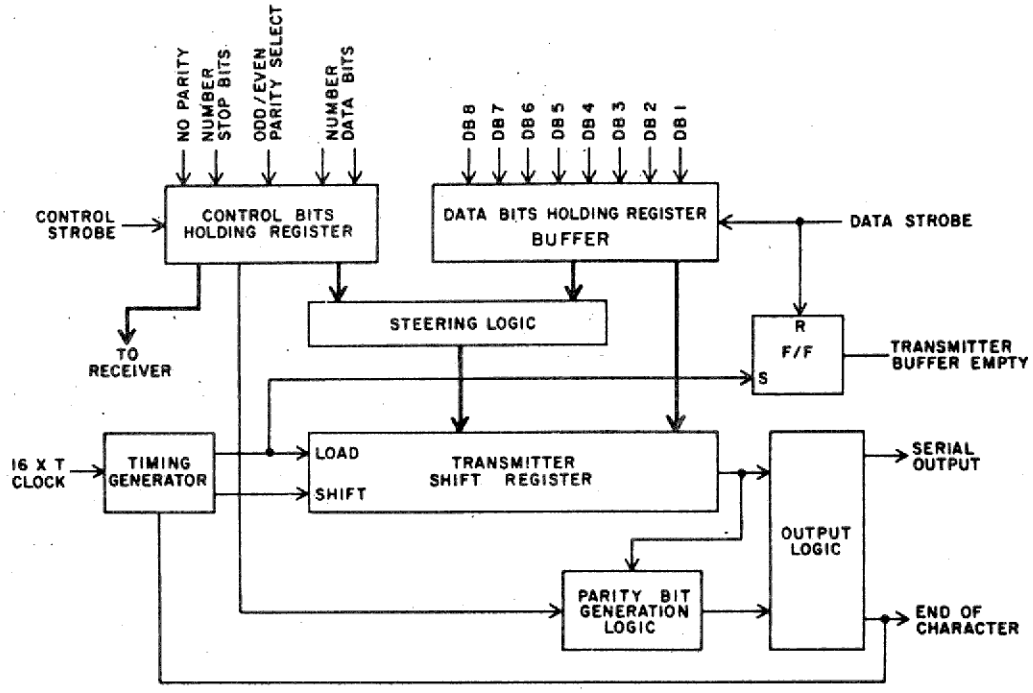


FIGURE 5 RECEIVER–BLOCK DIAGRAM

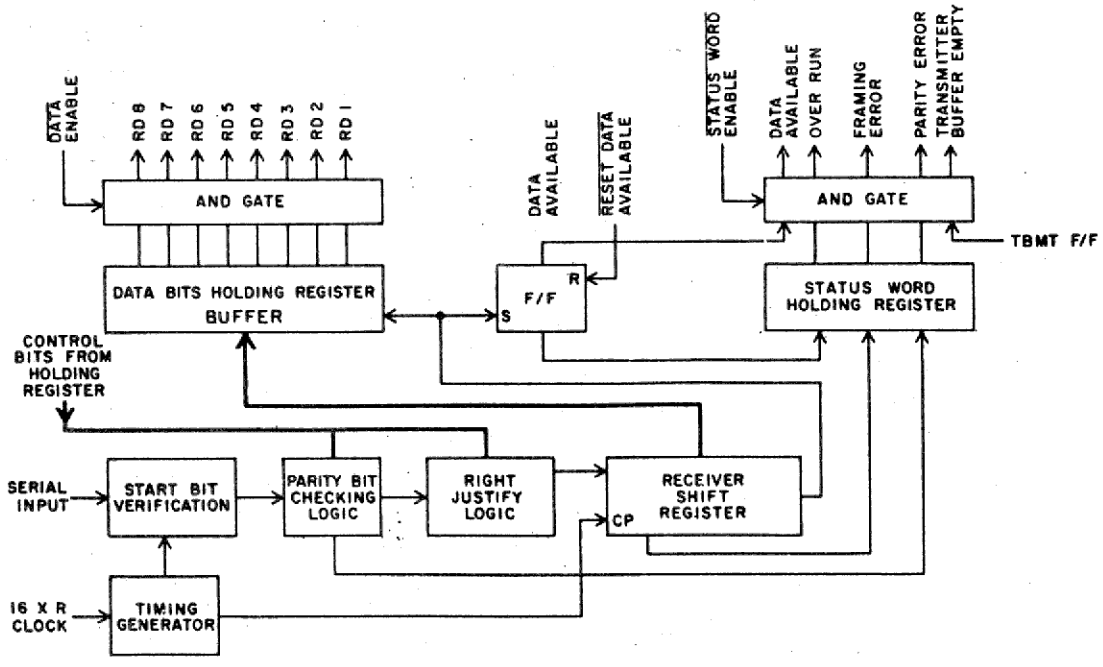
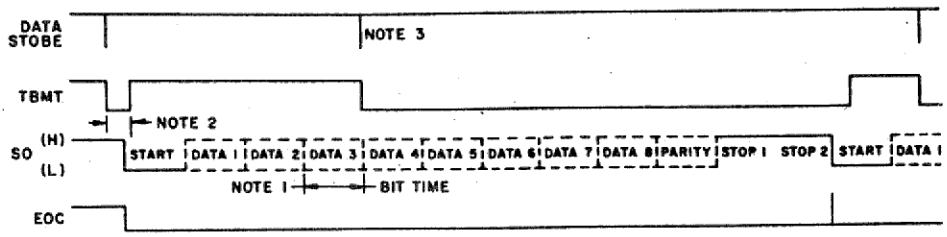


FIGURE 6 UAR/T–TRANSMITTER TIMING



NOTE: SEE FIGURES 7, 8, 9 FOR DETAILS.

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

DETAIL:

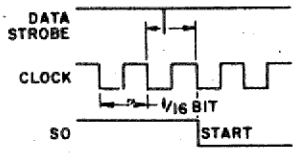


FIGURE 7 TRANSMITTER AT START BIT

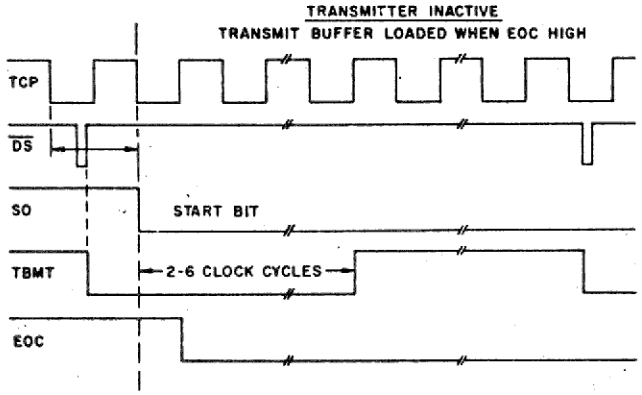


FIGURE 8 TRANSMITTER AT START BIT

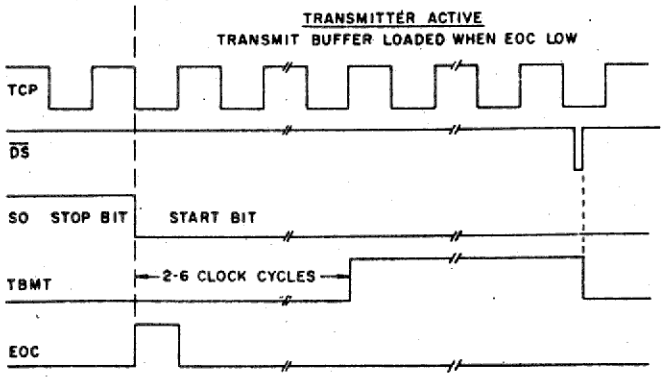


FIGURE 9 ALLOWABLE POINTS TO USE CONTROL STROBE

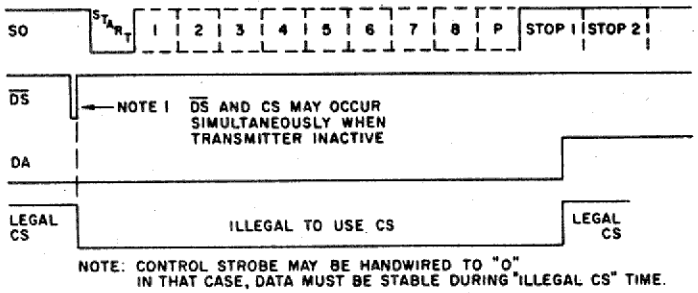


FIGURE 10 ALLOWABLE TCP, RCP

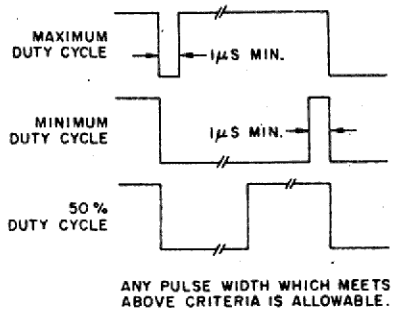
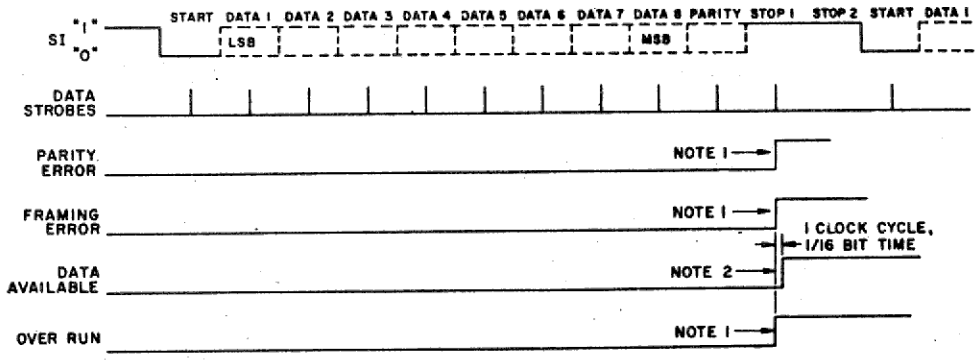


FIGURE 11 UAR/T–RECEIVER TIMING



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE DETECTED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP, FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED;* THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

FIGURE 12

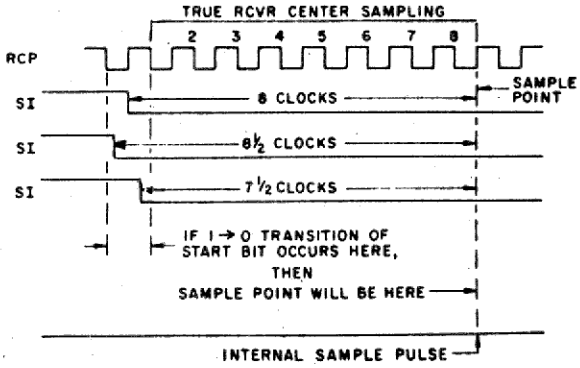


FIGURE 13 RECEIVER DURING 1st STOP BIT

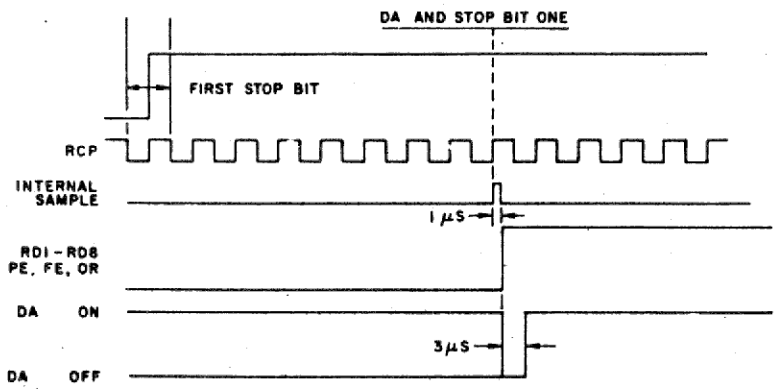
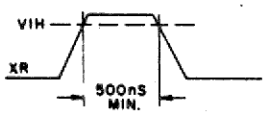


FIGURE 14 XR PULSE



WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER EXCEPT CONTROL REGISTER RECEIVED DATA SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO OV.

FIGURE 15 $\overline{DS}$

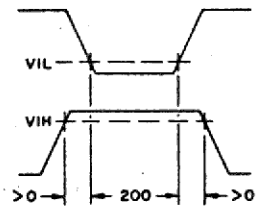


FIGURE 22 $\overline{RDE}$, $\overline{SWE}$

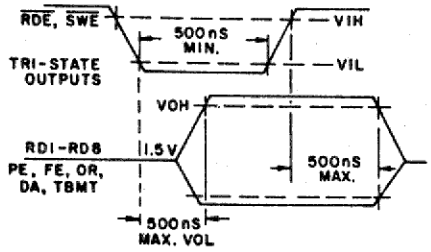


FIGURE 23 $\overline{RDA}$

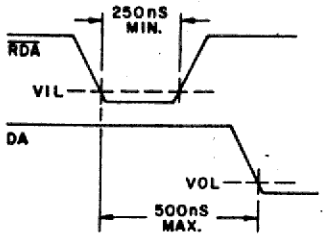


FIGURE 24 SHORT CIRCUIT OUTPUT CURRENT

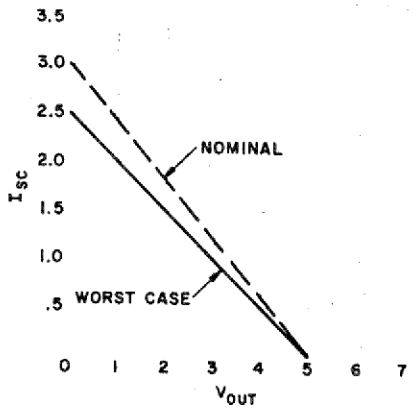


FIGURE 25 RD1–RD8, PE, FE, OR, TBMT, DA

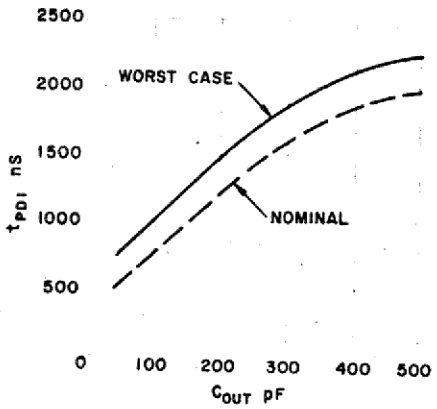


FIGURE 26a –12 VOLT SUPPLY CURRENT

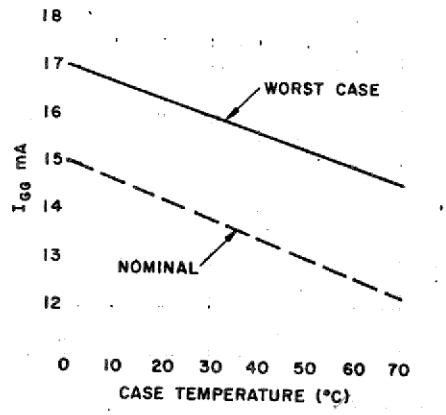
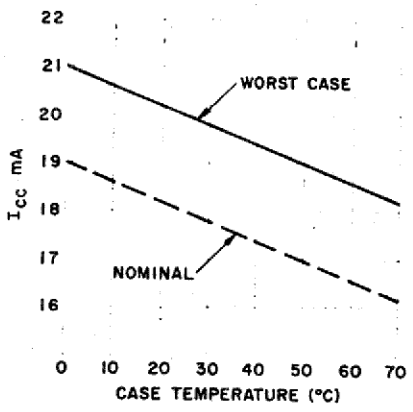


FIGURE 26b +5 VOLT SUPPLY CURRENT



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