DANSK DATA ELEKTRONIK ApS

ID-7oo5 MANUAL CONTROL module for the ID-7ooo MICROPROCESSOR SYSTEM

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1. General description. This module contains logic to perform the manual control functions of the ID-7ooo microprocessor system, such as reset, single cycle execution, single instruction execution, run/stop control and debug call.
Furthermore the module contains drivers for indicators on the ID-7ooo front panel, displaying address, data and interrupt information and different control signals in the bus.

The connection to the ID-7ooo front panel is performed by means of the top edge connector of the module, while the connection to the bus is performed by the bottom edge connector of the board.
The module plugs into any vacant position in the bus system.

Appendix 1 contains logic schematic of the ID-7oo5 manual control module. Appendix 2 shows the ID-7ooo front panel.

2. Manual controls. The ID-7ooo front panel contains 5 switches with the following functions:

RUN/STOP: This control starts and stops the instruction execution of the CPU. When STOP is selected, the program execution is stopped in the TW-state of the current machine cycle. If it is wanted to stop the processor in an M1 machine cycle, a SINGLE INSTRUCTION command should be executed after execution of the STOP command.
When stopped, the indicators on the front panel display the state of the processor (address, data and control signals) corresponding to the current machine cycle.

SC (SINGLE CYCLE): This control switch is only active, when the processor is in the STOP state. When activated, the processor executes the current machine cycle and stops in the succeding machine cycle.

SI (SINGLE INSTRUCTION): This control switch is only active, when the processor is in the STOP state. When activated, the processor executes one machine instruction and stops in the first machine cycle of the succeeding machine instruction.

DC (DEBUG CALL): When this switch is activated, a CALL X.F000 instruction is jammed into the CPU, succeeding the current instruction (and a possible interrupt acknowledge machine cycle). This CALL instruction transfers control to the system DEBUG-program.

NOTE: The switch is not active, when the CPU is in the HALT state (after execution of a HLT instruction). To prevent the CPU from entering a HALT state by cold start, it is recommended to use the control switches in the following order:

1) Enter STOP
2) Enter RES (RESET)
3) Enter DC (DEBUG CALL)
4) Enter RUN.

RES (RESET): When activated, this switch resets the ID-7ooo system.

3. Indicators. The module contains drivers to indicate the following bus signals on the display of the ID-7ooo front panel:

ADDRESS(15:o):	System address bus. ADDRESS(15) is most significant bit.
DATA(7:o):	System data bus. DATA(7) is most significant bit.
INTERRUPT REQUEST(7:o):	Interrupt request lines from I/O modules.

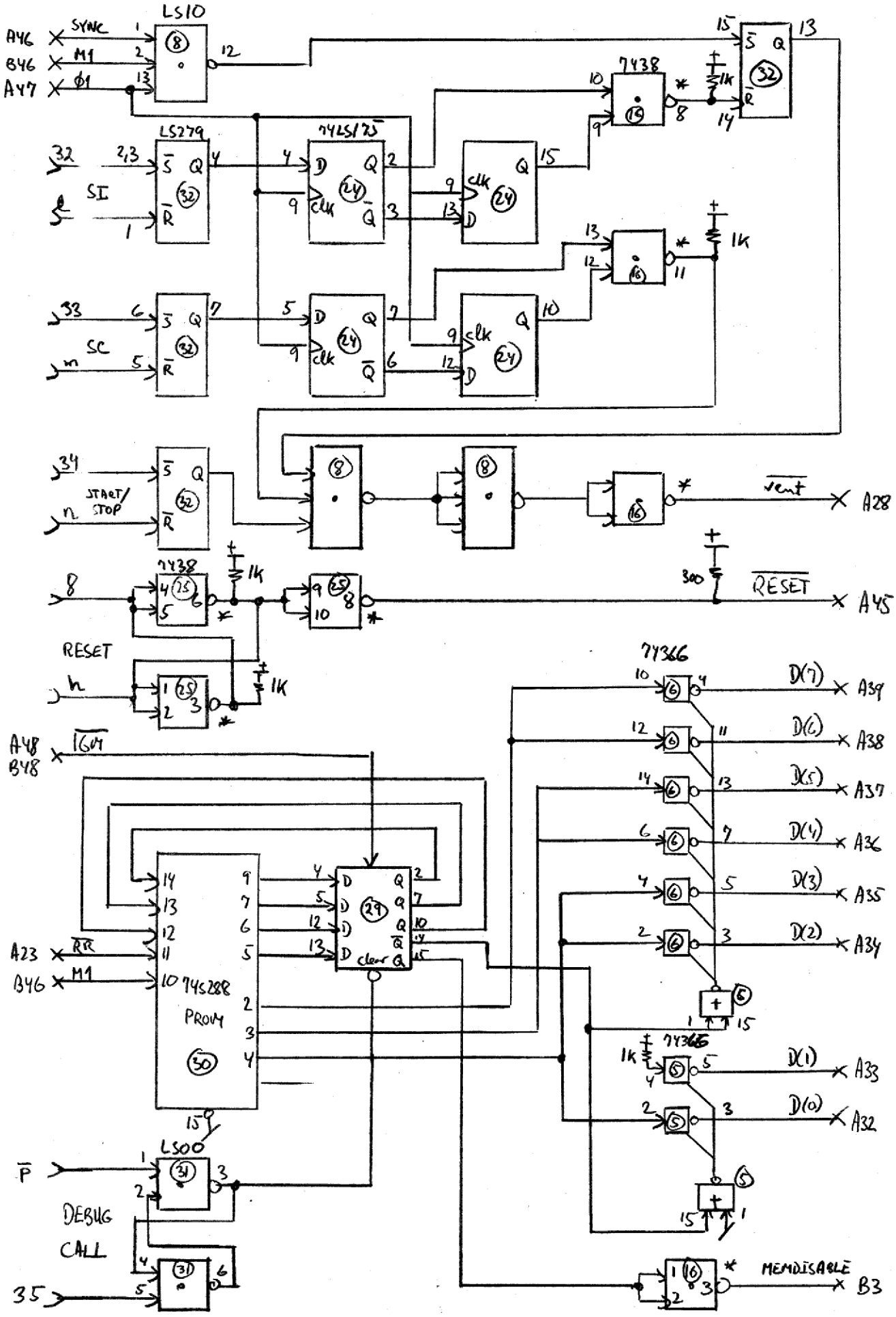
CYCLE INDICATORS: These indicators display the type of the current machine cycle:

- READ: Memory read cycle.
- WRITE: Memory write cycle.
- INPUT: I/O input cycle.
- OUTPUT: I/O output cycle.
- INT: Interrupt acknowledge cycle.

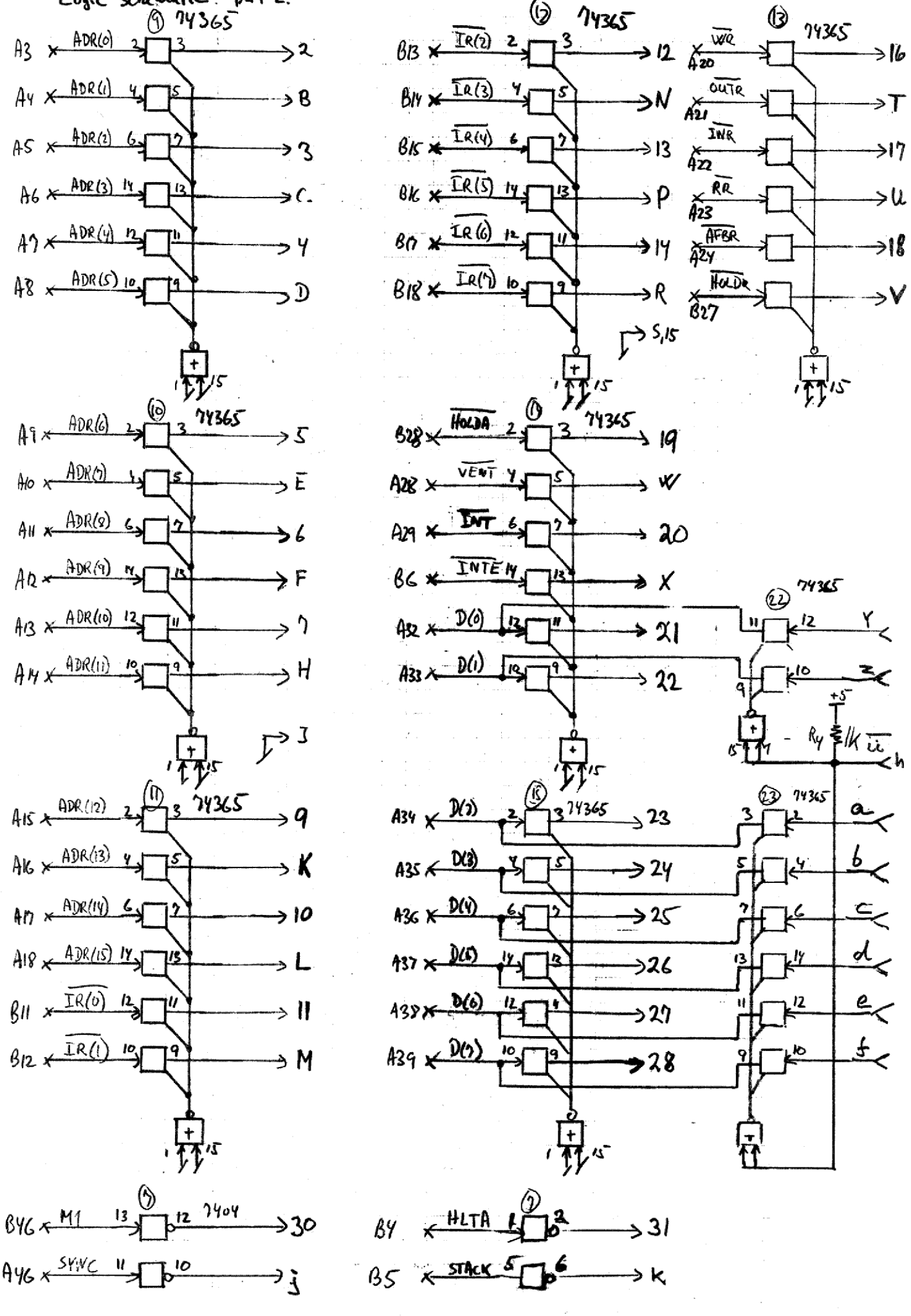
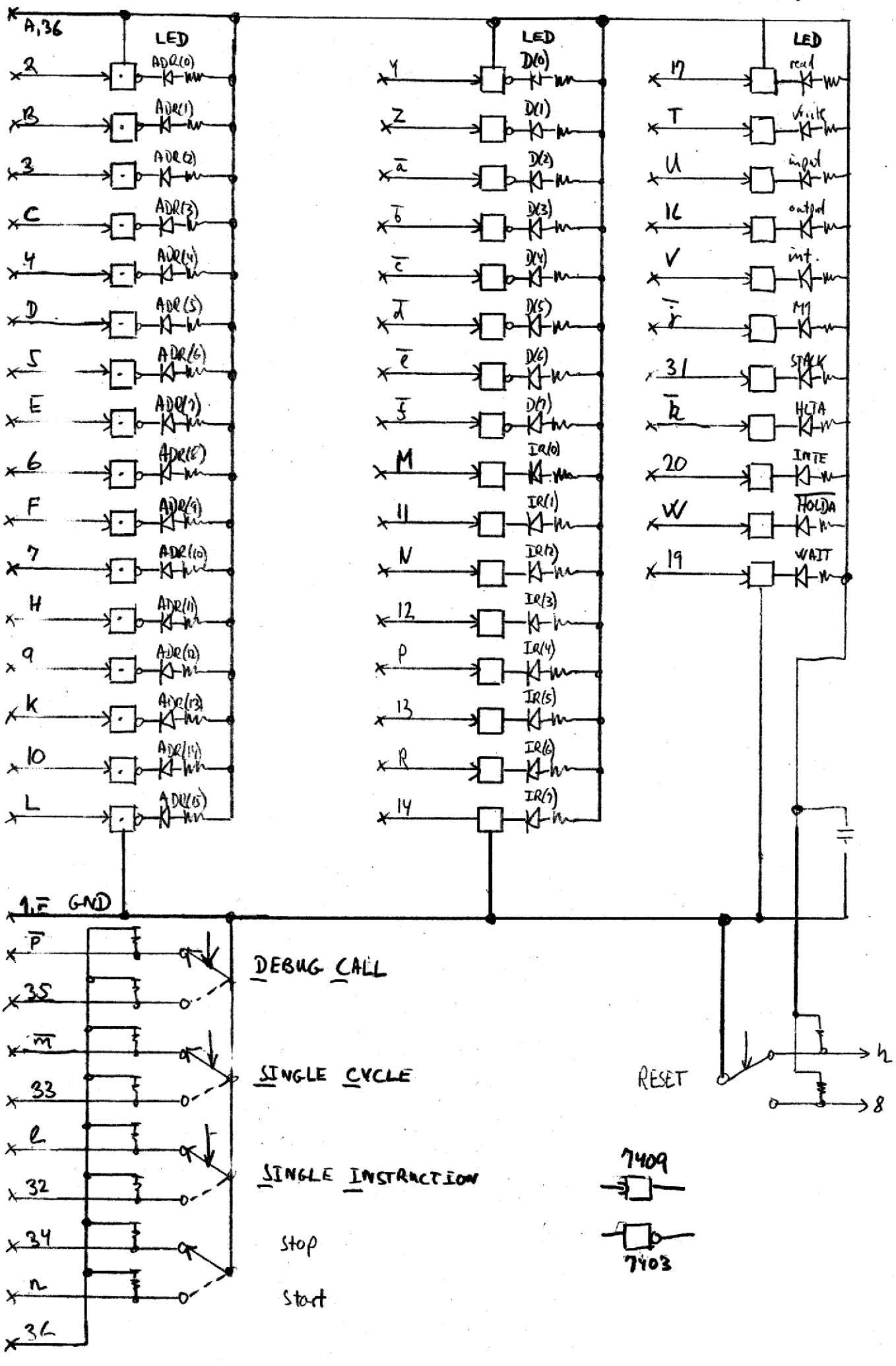
STATUS INDICATORS:

- M1: This indicator indicates a M1 (i.e. instruction fetch) machine cycle.
- ST: Indicates a stack machine cycle (stack read or stack write as indicated by the cycle indicators).
- HLT: Indicates a HALT machine cycle.
- IE: Indicates the state of the internal interrupt enable flip-flop of the CPU.
- $\overline{HA}$: Indicates the state of the HOLD ACKNOWLEDGE control line from the CPU.
- WT: Indicates the state of the vent control line to the CPU.

Navn	Lb. nr.	Dato	Emne	Fag	Afd.	Side
ID-7005 Manual Control mod. Logic schematic. part1					Appendix 1	1



ID-7005 Manual control mod.
Logic Schematic. part 2.



ID-7000 FRONT PANEL, logic schematic: