DANSK DATA ELEKTRONIK

ID-7009 DMA CONTROLLER MODULE

for the

ID-7000 MICROPROCESSOR SYSTEM

NOVEMBER 1978

Author: Knud Arne Nielsen

ID-7009 DMA CONTROLLER MODULE

1. GENERAL DESCRIPTION.

The 7009 module uses two AMD 9517 DMA controllers. The DMA controllers are described in appendix 1, while appendix 2 is a logic schematic of the module.

Each DMA controller has four DMA channels and the 7009 module has a total of eight DMA channels.

The 7009 module does not use the cascade capability of the DMA controllers. Instead it contains control logic that arbitrates between requests from the two controllers. Furthermore the module contains data and address bus drivers/receivers and control logic for these.

2. ADDRESSING.

The module uses 32 addresses. ADR(4) selects one of the two DMA controllers. ADR(3:0) selects different registers or control functions in the selected DMA controller as described in appendix 1.

The address of the module is selected by a switch register on the module. ADR(7:3) is compared with the switch register and if there is a match the card select signal is generated.

3. DMA CONTROL SIGNALS.

$\overline{\text{DMAREQ}}$(7:0)

The signals are open collector active low. The 7009 module has the pull up resistors for the signals and converts them to active high before they are connected to the DMA controllers.

$\overline{\text{DMAACK(7:0)}}$

The signals are active low open collector without pull up resistors. Pull up resistors should be placed on the modules that use the signals. The signals are not inverted on the 7009 module.

$\overline{\text{INDMA}}$, $\overline{\text{OUTDMA}}$

These signals are active low signals that control reading and writing respectively in a DMA IO unit during a DMA cycle.

EOPIN, EOPOUT

These signals are input and output to the tristate EOP signal from the DMA controllers. The EOP signal is described in appendix 1. The signals are not inverted on the module.

4. PROGRAMMING CONSIDERATIONS.

See appendix 1 page 6: command register.

The controllers should be initialized so they use normal timing (bit 3) and late write (bit 5).

DREQ should be active high (bit 6) and DACK should be active low (bit 7).

Am9517A

Multimode DMA Controller

Advanced Micro Devices
Advanced MOS/LSI

DISTINCTIVE CHARACTERISTICS

- Four independent DMA channels, each with separate registers for Mode Control, Current Address, Base Address, Current Word Count and Base Word Count.
- Transfer modes: Block, Demand, Single Word, Cascade
- Independent autoinitialization of all channels
- Memory-to-memory transfers
- Memory block initialization
- Address increment or decrement
- Master system disable
- Enable/disable control of individual DMA requests
- Directly expandable to any number of channels
- End of Process input for terminating transfers
- Software DMA requests
- Independent polarity control for DREQ and DACK signals
- Compressed timing option speeds transfers – up to 2M words/second
- +5 volt power supply
- Advanced N-channel silicon gate MOS technology
- 40 pin Hermetic DIP package
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

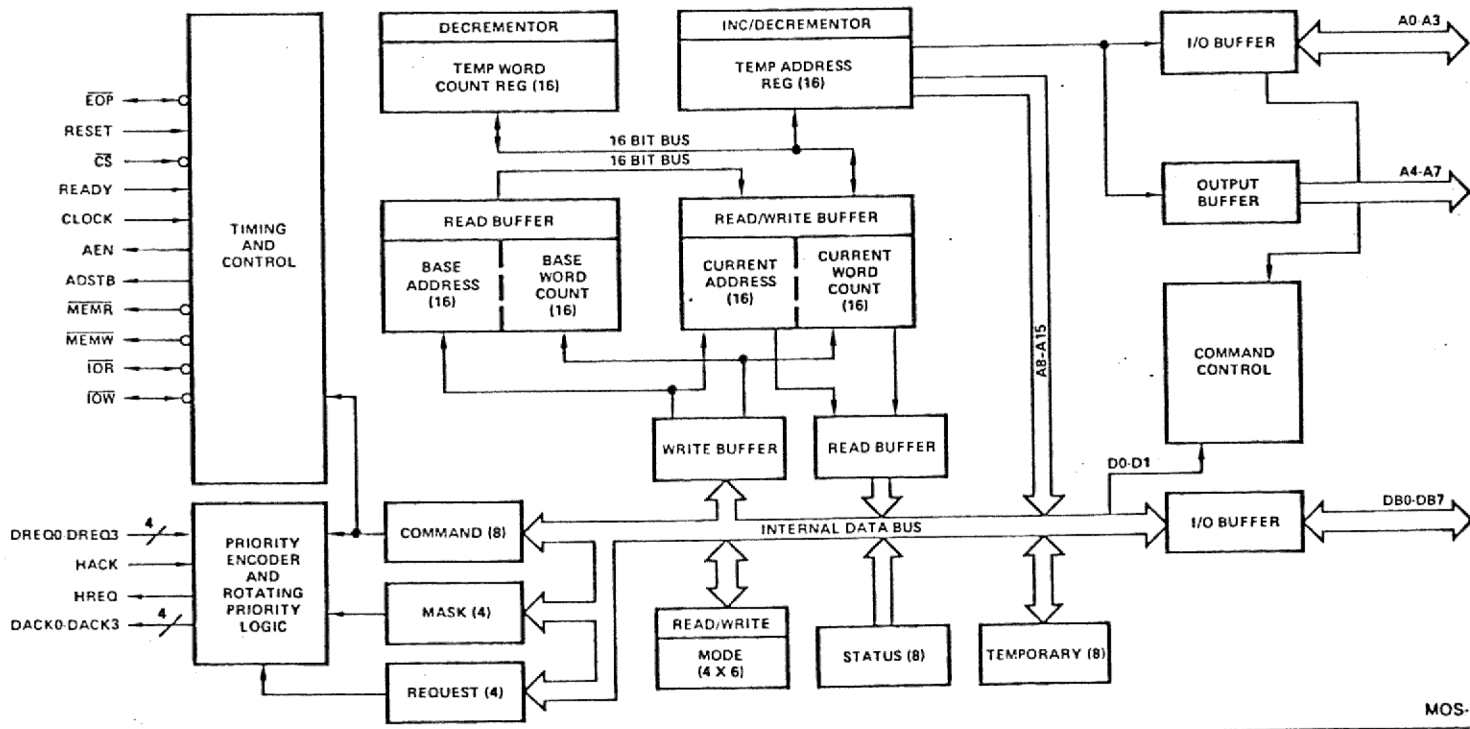
The Am9517A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information to or from the system memory. Memory-to-memory transfer capability is also provided. The Am9517A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The Am9517A is designed to be used in conjunction with an external 8-bit address register such as the Am74LS373. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process ($\overline{EOP}$).

Each channel has a full 64K address and word count capability. An external $\overline{EOP}$ signal can terminate a DMA or memory-to-memory transfer. This is useful for block search or compare operations using external comparators or for intelligent peripherals to abort erroneous services.

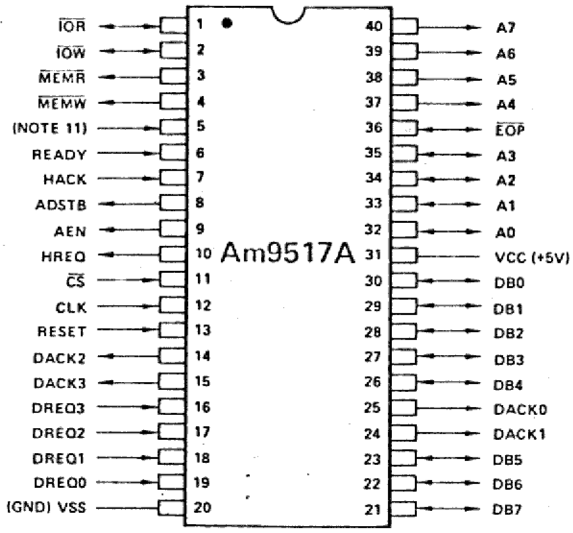
BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Ambient Temperature	Maximum Clock Frequency	
		3MHz	4MHz
Hermetic DIP/ Molded DIP	$0°C \leq T_A \leq +70°C$	AM9517ADC/PC AM9517A-1DC/PC	AM9517A-4DC/PC
Hermetic DIP	$-55°C \leq T_A \leq +125°C$	AM9517ADM	

CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

Figure 1.

MOS-034

INTERFACE SIGNAL DESCRIPTION

VCC: +5 Volt Supply
VSS: Ground

CLK (Clock, Input)

This input controls the internal operations of the Am9517A and its rate of data transfers. The input may be driven at up to 3MHz for the standard Am9517A and up to 4MHz for the Am9517A-4.

$\overline{\text{CS}}$ (Chip Select, Input)

Chip Select is an active low input used to select the Am9517A as an I/O device during an I/O Read or I/O Write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the Am9517A by the host CPU, $\overline{\text{CS}}$ may be held low providing $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$ is toggled following each transfer.

RESET (Reset, Input)

Reset is an asynchronous active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.

READY (Ready, Input)

Ready is an input used to extend the memory read and write pulses from the Am9517A to accommodate slow memories or I/O peripheral devices.

HACK (Hold Acknowledge, Input)

The active high Hold Acknowledge from the CPU indicates that control of the system buses has been relinquished.

DREQ0-DREQ3 (DMA Request, Input)

The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. Polarity of DREQ is programmable. Reset initializes these lines to active high.

DB0-DB7 (Data Bus, Input/Output)

The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled during the I/O Read by the host CPU, permitting the CPU to examine the contents of an Address register, the Status register, the Temporary register or a Word Count register. The Data Bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the Am9517A control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the Am9517A's Temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the Temporary register data into the destination memory location.

$\overline{\text{IOR}}$ (I/O Read, Input/Output)

I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the Am9517A to access data from a peripheral during a DMA Write transfer.

$\overline{\text{IOW}}$ (I/O Write, Input/Output)

I/O Write is a bidirectional active low three-state line. In the Idle cycle it is an input control signal used by the CPU to load information into the Am9517A. In the Active cycle it is an output control signal used by the Am9517A to load data to the peripheral during a DMA Read transfer.

Write operations by the CPU to the Am9517A require a rising $\overline{\text{WR}}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{\text{IOW}}$ pin low and toggle $\overline{\text{CS}}$.

$\overline{\text{EOP}}$ (End of Process, Input/Output)

$\overline{\text{EOP}}$ is an active low bidirectional open-drain signal providing information concerning the completion of DMA service. When a channel's Word Count goes to zero, the Am9517A pulses $\overline{\text{EOP}}$ low to provide the peripheral with a completion signal. $\overline{\text{EOP}}$ may also be pulled low by the peripheral to cause premature completion. The reception of $\overline{\text{EOP}}$, either internal or external, causes the currently active channel to terminate the service, to set its TC bit in the Status register and to reset its request bit. If Autoinitialization is selected for the channel, the current registers will be updated from the base registers. Otherwise the channel's mask bit will be set and the register contents will remain unaltered.

During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ always applies to the channel with an active DACK; external $\overline{EOPS}$ are disregarded in DACK0-DACK3 are all inactive.

Because $\overline{EOP}$ is an open-drain signal, an external pullup resistor is required. Values of 3.3K or 4.7K are recommended; the $\overline{EOP}$ pin can not sink the current passed by a 1K pullup.

A0-A3 (Address, Input/Output)

The four least significant address lines are bidirectional 3-state signals. During DMA Idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the lower 4-bits of the output address.

A4-A7 (Address, Output)

The four most significant address lines are three-state outputs and provide four bits of address. These lines are enabled only during DMA service.

HREQ (Hold Request, Output)

The Hold Request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the Am9517A to issue HREQ.

DACK0-DACK3 (DMA Acknowledge, Output)

The DMA Acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.

AEN (Address Enable, Output)

Address Enable is an active high signal used to disable the system bus during DMA cycles to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HACK and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The Am9517A automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.

ADSTB (Address Strobe, Output)

The active high Address Strobe is used to strobe the upper address byte from DB0-DB7 into an external latch.

$\overline{MEMR}$ (Memory Read, Output)

The Memory Read signal is an active low three-state output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 2. Am9517A Internal Registers.

$\overline{MEMW}$ (Memory Write, Output)

The Memory Write signal is an active low three-state output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.

FUNCTIONAL DESCRIPTION

The Am9517A block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The Am9517A contains 344 bits of internal memory in the form of registers. Figure 2 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

The Am9517A contains three basic blocks of control logic. The Timing Control block generates internal timing and externa control signals for the Am9517A. The Program Command Control block decodes the various commands given to the Am9517A by the microprocessor prior to servicing a DMA Request. It also decodes each channel's Mode Control word. The Priority Encoder block resolves priority contention among DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In Am9080A systems this input will usually be the $\phi 2$ TTL clock from an Am8224. However, any appropriate system clock will suffice.

DMA Operation

The Am9517A is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The Am9517A can assume seven separate states, each composed of one full clock period. State 1 (S1) is the inactive state. It is entered when the Am9517A has no valid DMA requests pending. While in S1, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The Am9517A has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wa states (SW) can be inserted before S4 by the use of the Read line on the Am9517A.

Memory-to-memory transfers require a read-from and write-to-memory to complete each transfer. The states, whic resemble the normal working states, use two digit numbers fo identification. Eight states are required for each complet transfer. The first four states (S11, S12, S13, S14) are used fo the read-from-memory half and the last four states (S21, S22 S23 and S24) for the write-to-memory half of the transfer. Th Temporary Data register is used for intermediate storage of th memory byte.

IDLE Cycle

When no channel is requesting service, the Am9517A will ente the Idle cycle and perform "S1" states. In this cycle th Am9517A will sample the DREQ lines every clock cycle to de termine if any channel is requesting a DMA service. The devic will also sample $\overline{CS}$, looking for an attempt by the microproces sor to write or read the internal registers of the Am9517A. Whe $\overline{CS}$ is low and HACK is low the Am9517A enters the Progra Condition. The CPU can now establish, change or inspect th internal definition of the part by reading from or writing to th internal registers. Address lines A0-A3 are inputs to the devic and select which registers will be read or written. The $\overline{IOR}$ ar $\overline{IOW}$ lines are used to select and time reads or writes. Due to th number and size of the internal registers, an internal flip/flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip/flop is reset by Master Clear or Reset. A separate software command can also reset this flip/flop.

Special software commands can be executed by the Am9517A in the Program Condition. These commands are decoded as sets of addresses when both $\overline{CS}$ and $\overline{IOW}$ are active and do not make use of the data bus. Functions include Clear First/Last Flip/Flop and Master Clear.

ACTIVE CYCLE

When the Am9517A is in the Idle cycle and a channel requests a DMA service, the device will output a HREQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode: In Single Transfer mode, the Am9517A will make a one-byte transfer during each HREQ/HACK handshake. When DREQ goes active, HREQ will go active. After the CPU responds by driving HACK active, a one-byte transfer will take place. Following the transfer, HREQ will go inactive, the word count will be decremented and the address will be either incremented or decremented. When the word count goes to zero a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.

To perform a single transfer, DREQ must be held active only until the corresponding DACK goes active. If DREQ is held continuously active, HREQ will go inactive following each transfer and then will go active again and a new one-byte transfer will be made following each rising edge of HACK. In 8080A/9080A systems this will ensure one full machine cycle of execution between DMA transfers. Details of timing between the Am9517A and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode: In Block Transfer mode, the Am9517A will continue making transfers until a TC (caused by the word count going to zero) or an external End of Process ($\overline{EOP}$) is encountered. DREQ need be held active only until DACK becomes active. An autoinitialize will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode: In Demand Transfer mode the device will continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus, the device requesting service may discontinue transfers by bringing DREQ inactive. Service may be resumed by asserting an active DREQ once again. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count may be read from the Am9517A Current Address and Current Word Count registers. Autoinitialization will only occur following a TC or $\overline{EOP}$ at the end of service. Following Autoinitialization, an active-going DREQ edge is required to initiate a new DMA service.

Cascade Mode: This mode is used to cascade more than one Am9517A together for simple system expansion. The HREQ and HACK signals from the additional Am9517A are connected to the DREQ and DACK signals of a channel of the initial Am9517A. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel in the initial device is used only for prioritizing the additional device, it does not output any address or control signals of its own. These would conflict with the outputs of the active channel in the added device. The Am9517A will respond to DREQ with DACK but all other outputs except HREQ will be disabled.

Figure 3 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More Am9517As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices forming a third level.

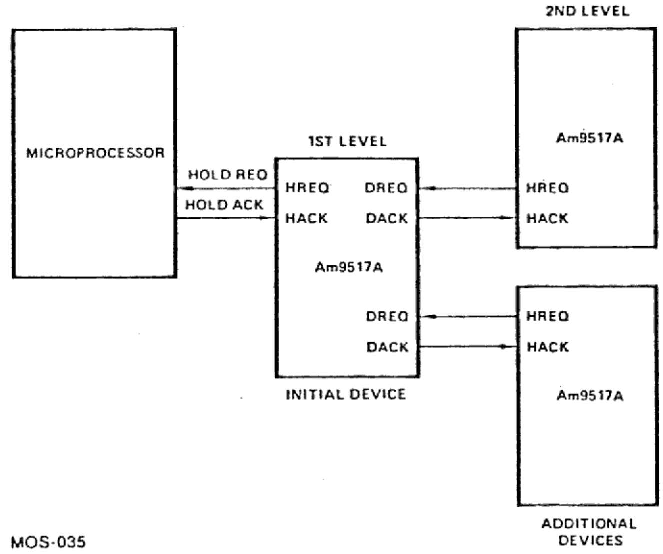


Figure 3. Cascaded Am9517As.

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{IOR}$ and $\overline{MEMW}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers; the Am9517A operates as in Read or Write transfers generating addresses, responding to $\overline{EOP}$, etc., however, the memory and I/O control lines remain inactive.

Memory-to-Memory: The Am9517A includes a block move capability that allows blocks of data to be moved from one memory address space to another. When Bit C0 in the Command register is set to a logical 1, channels 0 and 1 will operate as memory-to-memory transfer channels. Channel 0 forms the source address and channel 1 forms the destination address. The channel 1 word count is used. A memory-to-memory transfer is initiated by setting a software DMA request for channel 0. Block Transfer Mode should be used for memory-to-memory. When channel 0 is programmed for a fixed source address, a single source word may be written into a block of memory.

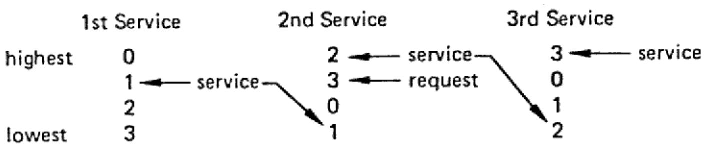
When setting up the Am9517A for memory-to-memory operation, it is suggested that both channels 0 and 1 be masked out. Further, the channel 0 word count should be initialized to the same value used in channel 1. No DACK outputs will be active during memory-to-memory transfers.

The Am9517A will respond to external $\overline{EOP}$ signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers may be found in Timing Diagram 4.

Autointialize: By programming a bit in the Mode register a channel may be set up for an Autoinitialize operation. During Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set by $\overline{EOP}$ when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to repeat its service without CPU intervention.

Priority: The Am9517A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.



The priority encoder selects the highest priority channel requesting service on each active-going HACK edge. Once a channel is started, its operation will not be suspended if a request is received by a higher priority channel. The high priority channel will only gain control after the lower priority channel releases HREQ. When control is passed from one channel to another, the CPU will always gain bus control. This ensures generation of rising HACK edge to be used to initiate selection of the new highest-priority requesting channel.

Compressed Timing: In order to achieve even greater throughput where system characteristics permit, the Am9517A can compress the transfer time to two clock cycles. From Timing Diagram 3 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Timing Diagram 6.

Address Generation: In order to reduce pin count, the Am9517A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a 3-state enable. The lower order address bits are output by the Am9517A directly. Lines A0-A7 should be connected to the address bus. Timing Diagram 3 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode services which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the Am9517A executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

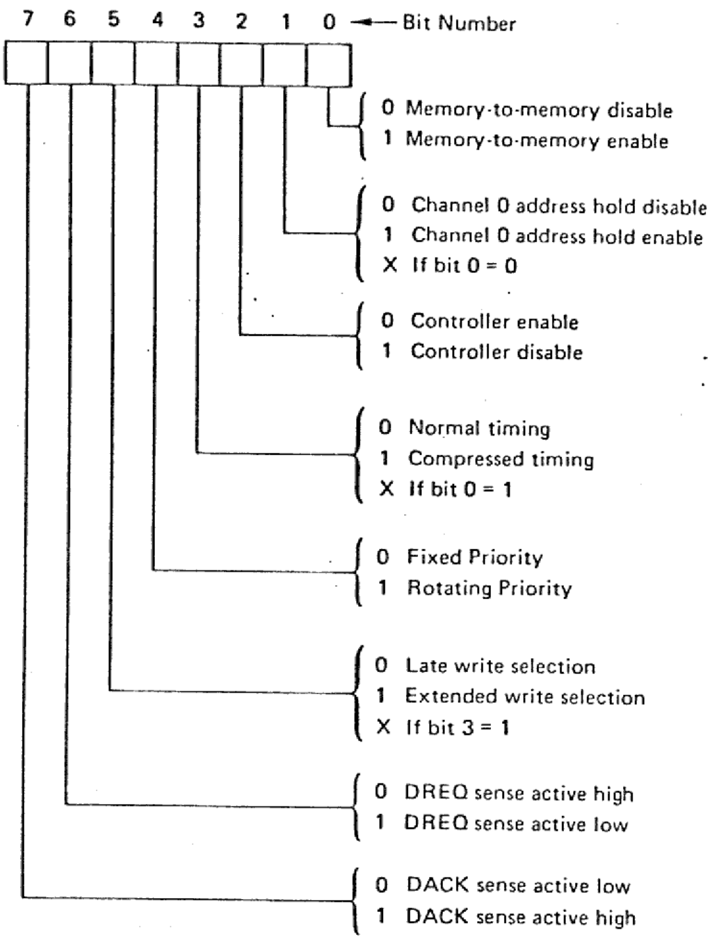
REGISTER DESCRIPTION

Current Address Register: Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialization takes place only after an $\overline{EOP}$.

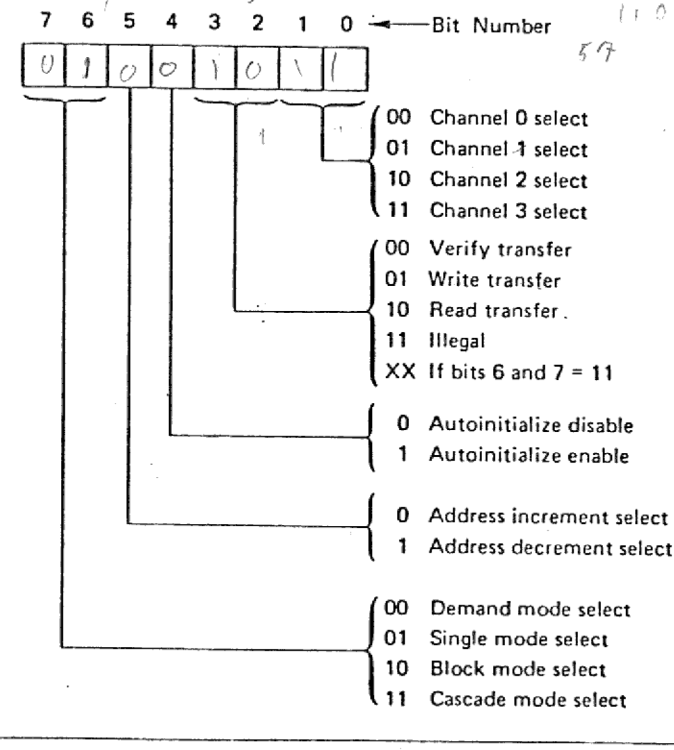
Current Word Count Register: Each channel has a 16-bit Current Word Count register. This register should be programmed with, and will return on a CPU read, a value one less than the number of words to be transferred. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize can occur only when an $\overline{EOP}$ occurs. Note that the contents of the Word Count register will be FFFF (hex) following on internally generated $\overline{EOP}$.

Base Address and Base Word Count Registers: Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original values of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes during DMA programming by the microprocessor. Accordingly, writing to these registers when intermediate values are in the Current registers will overwrite the intermediate values. The Base registers cannot be read by the microprocessor.

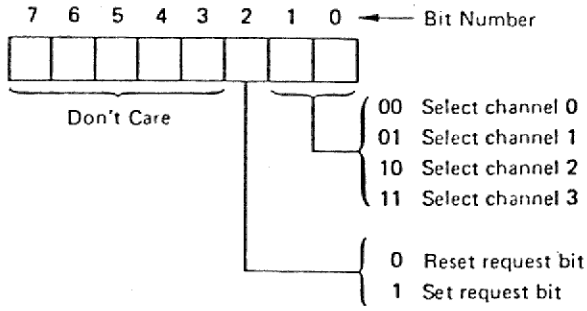
Command Register: This 8-bit register controls the operation of the Am9517A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset. The following table lists the function of the command bits. See Figure 4 for address coding.



Mode Register: Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register it to be written.

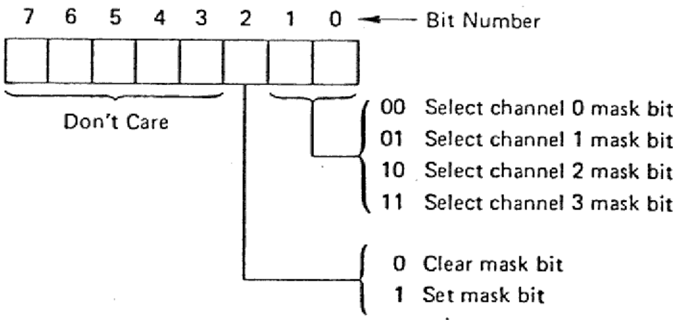


Request Register: The Am9517A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 4 for address coding.

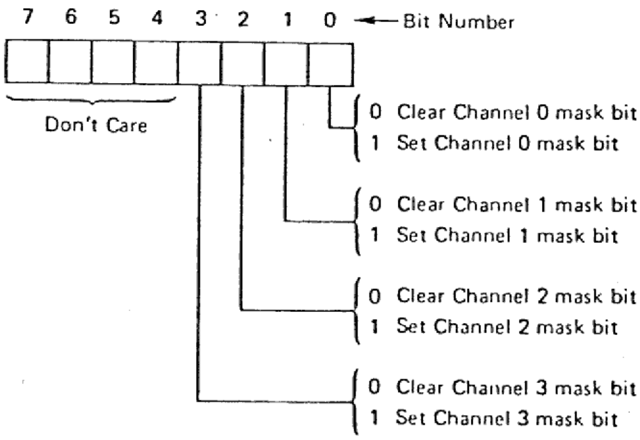


Software requests will be serviced only if the channel is in Block mode. When initiating a memory-to-memory transfer, the software request for channel 0 should be set.

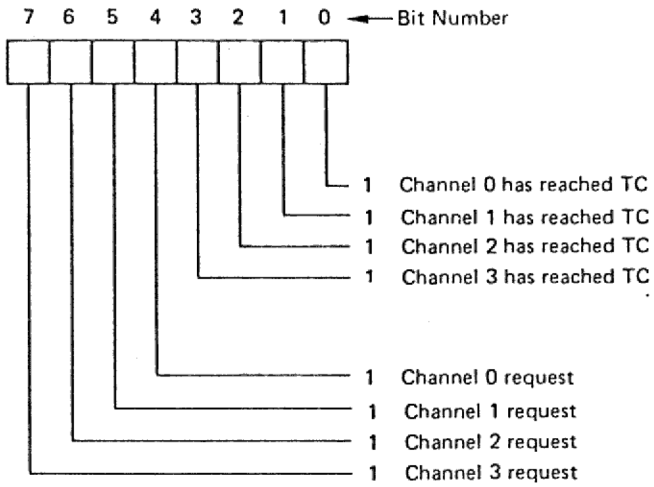
Mask Register: Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 4 for instruction addressing.



All four bits of the Mask Register may also be written with a single command.



Status Register: The Status registers may be read out of the Am9517A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set each time a TC is reached by that channel, including after each Autoinitialization. These bits are cleared by Reset and each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.



Temporary Register: The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands: There are two special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The two software commands are:

Clear First/Last Flip/Flop: This command may be issued prior to writing or reading Am9517A address or word count information. This initializes the flip/flop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary and Internal First/Last Flip/Flop registers are cleared and the Mask register is set. The Am9517A will enter the Idle cycle.

Figure 4 lists the address codes for the software commands.

	Interface Signals						
	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	Operation
28	1	0	0	0	0	1	Read Status Register
8	1	0	0	0	1	0	Write Command Register
9	1	0	0	1	0	1	Illegal
9	1	0	0	1	1	0	Write Request Register
A	1	0	1	0	0	1	Illegal
A	1	0	1	0	1	0	Write Single Mask Register Bit
B	1	0	1	1	0	1	Illegal
B	1	0	1	1	1	0	Write Mode Register
C	1	1	0	0	0	1	Illegal
C	1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
D	1	1	0	1	0	1	Read Temporary Register
D	1	1	0	1	1	0	Master Clear
E	1	1	1	0	0	1	Illegal
E	1	1	1	0	1	0	Illegal
2F	1	1	1	1	0	1	Illegal
2F	1	1	1	1	1	0	Write All Mask Register Bits

Figure 4. Register and Function Addressing.

Channel	Register	Operation	Signals							Internal Flip/Flop	Data Bus DB0–DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base & Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base & Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base & Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base & Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

Figure 5. Word Count and Address Register Command Codes.

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avo exposure to excessive voltages.

OPERATING RANGE

Part Number	T_A	VCC
Am9517ADC/PC	0°C to +70°C	5.0V ±5%
Am9517A-1DC/PC	0°C to +70°C	5.0V ±5%
Am9517A-4DC/PC	0°C to +70°C	5.0V ±5%
Am9517ADM	−55°C to +125°C	5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
VOH	Output HIGH Voltage	IOH = −200μA	2.4			Volts
		IOH = −100μA, (HREQ Only)	3.3			
VOL	Output LOW Voltage	IOL = 3.2mA			0.4	Volts
VIH	Input HIGH Voltage		2.0		VCC+0.5	Volts
VIL	Input LOW Voltage		−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VI ≤ VCC	−10		+10	μA
IOZ	Output Leakage Current	VCC ≤ VO ≤ VSS+.40	−10		+10	μA
ICC	VCC Supply Current	T_A = +25°C		65	130	mA
		T_A = 0°C		75	150	
		T_A = −55°C			175	
CO	Output Capacitance	fc = 1.0MHz, Inputs = 0V		4	8	pF
CI	Input Capacitance			8	15	pF
CIO	I/O Capacitance			10	18	pF

NOTES:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. Input timing parameters assume transition times of 20ns or less. Waveform measurement points for both input and output signals are 2.0V for High and 0.8V for Low, unless otherwise noted.
3. Output loading is 1 Standard TTL gate plus 50pF capacitance unless noted otherwise.
4. The new $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be TCY-100ns and for extended write will be 2TCY-100ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY-50ns and for compressed read will be TCY-50ns.
5. TDQ is specified for two different output HIGH levels. TDQ1 is measured at 2.0V. TDQ2 is measured at 3.3V. The value for TDQ2 assumes an external 3.3kΩ pull-up resistor connected from HREQ to VCC.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. Output loading on the data bus is 1 Standard TTL gate plu 15pF for the minimum value and 1 Standard TTL gate plu 100pF for the maximum value.
9. Successive read and/or write operations by the extern processor to program or examine the controller must b timed to allow at least 600ns for the Am9517A Am9517A-1 and at least 450ns for the Am9517A-4 as r covery time between active read or write pulses.
10. Parameters are listed in alphabetical order.
11. Pin 5 is an input that should always be at a logic high leve An internal pull-up resistor will establish a logic high whe the pin is left floating. Alternatively, pin 5 may be tied VCC.
12. Signals $\overline{READ}$ and $\overline{WRITE}$ refer to $\overline{IOR}$ and $\overline{MEMW}$ respe tively for peripheral-to-memory DMA operations and $\overline{MEMR}$ and $\overline{IOW}$ respectively for memory-to-periphe DMA operations.
13. If N wait states are added during the write-to-memory half a memory-to-memory transfer, this parameter will increa by N (TCY).

SWITCHING CHARACTERISTICS

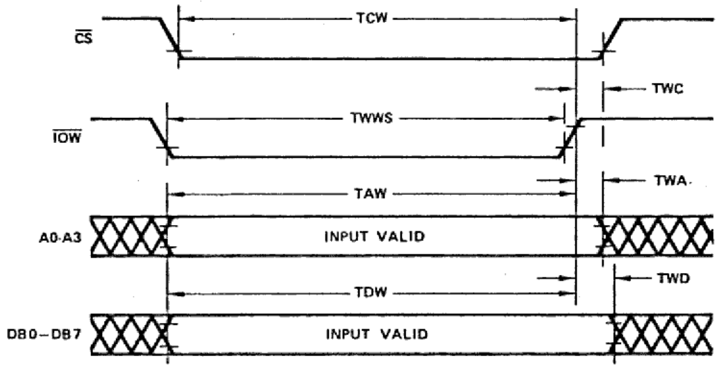
ACTIVE CYCLE (Notes 2, 3, 10, 11 and 12)

Parameter	Description	Am9517A Min	Am9517A Max	Am9517A-1 Min	Am9517A-1 Max	Am9517A-4 Min	Am9517A-4 Max	Unit
TAEL	AEN HIGH from CLK LOW (S1) Delay Time		300		300		225	ns
TAET	AEN LOW from CLK HIGH (S1) Delay Time		200		200		150	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		150		150		120	ns
TAFC	READ or WRITE Float from CLK HIGH		150		150		120	ns
TAFDB	DB Active to Float Delay from CLK HIGH		250		250		190	ns
TAHR	ADR from READ HIGH Hold Time	TCY-100		TCY-100		TCY-100		ns
TAHS	DB from ADSTB LOW Hold Time	50		50		40		ns
TAHW	ADR from WRITE HIGH Hold Time	TCY-50		TCY-50		TCY-50		ns
TAK	DACK Valid from CLK LOW Delay Time		280		280		220	ns
	EOP HIGH from CLK HIGH Delay Time		250		250		190	ns
	EOP LOW to CLK HIGH Delay Time		250		250		190	ns
TASM	ADR Stable from CLK HIGH		250		250		190	ns
TASS	DB to ADSTB LOW Setup Time	100		100		100		ns
TCH	Clock High Time (Transitions ≤ 10ns)	120		120		100		ns
TCL	Clock Low Time (Transitions ≤ 10ns)	150		150		110		ns
TCY	CLK Cycle Time	320		320		250		ns
TDCL	CLK HIGH to READ or WRITE LOW Delay (Note 4)		270		270		200	ns
TDCTR	READ HIGH from CLK HIGH (S4) Delay Time (Note 4)		270		270		210	ns
TDCTW	WRITE HIGH from CLK HIGH (S4) Delay Time (Note 4)		200		200		150	ns
TDQ1	HREQ Valid from CLK HIGH Delay Time (Note 5)		160		160		120	ns
TDQ2			250		250		190	ns
TEPS	EOP LOW from CLK LOW Setup Time	60		60		45		ns
TEPW	EOP Pulse Width	300		300		225		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		250		250		190	ns
TFAC	READ or WRITE Active from CLK HIGH		200		200		150	ns
TFADB	DB Float to Active Delay from CLK HIGH		300		300		225	ns
THS	HACK valid to CLK HIGH Setup Time	100		100		75		ns
TIDH	Input Data from MEMR HIGH Hold Time	0		0		0		ns
TIDS	Input Data to MEMR HIGH Setup Time	250		250		190		ns
TODH	Output Data from MEMW HIGH Hold Time	20		20		20		ns
TODV	Output Data Valid to MEMW HIGH (Note 13)	200		200		125		ns
TQS	DREQ to CLK LOW (S1, S4) Setup Time	120		120		90		ns
TRH	CLK to READY LOW Hold Time	20		20		20		ns
TRS	READY to CLK LOW Setup Time	100		100		60		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		200		200		150	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		140		140		110	ns

SWITCHING CHARACTERISTICS
PROGRAM CONDITION (IDLE CYCLE)
(Notes 2, 3, 10, 11 and 12)

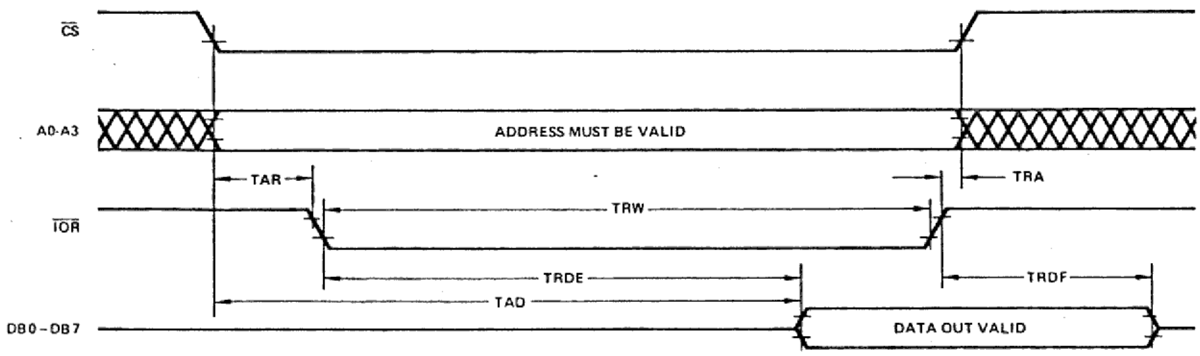
Parameter	Description	Am9517A Min.	Am9517A Max.	Am9517A-1 Min.	Am9517A-1 Max.	Am9517A-4 Min.	Am9517A-4 Max.	Unit
TAR	ADR Valid or $\overline{\text{CS}}$ LOW to $\overline{\text{READ}}$ LOW	50		50		50		ns
TAW	ADR Valid to $\overline{\text{WRITE}}$ HIGH Setup Time	200		200		150		ns
TCW	$\overline{\text{CS}}$ LOW to $\overline{\text{WRITE}}$ HIGH Setup Time	200		200		150		ns
TDW	Data Valid to $\overline{\text{WRITE}}$ HIGH Setup Time	200		200		150		ns
TRA	ADR or $\overline{\text{CS}}$ Hold from $\overline{\text{READ}}$ HIGH	0		0		0		ns
TRDE	Data Access from $\overline{\text{READ}}$ LOW (Note 8)		300		200		200	ns
TDRF	DB Float Delay from $\overline{\text{READ}}$ HIGH	20	150	20	100	20	100	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		500		500		μs
TRSTS	RESET to First $\overline{\text{IOWR}}$	2		2		2		TCY
TRSTW	RESET Pulse Width	300		300		300		ns
TRW	$\overline{\text{READ}}$ Width	300		300		250		ns
TWA	ADR from $\overline{\text{WRITE}}$ HIGH Hold Time	20		20		20		ns
TWC	$\overline{\text{CS}}$ HIGH from $\overline{\text{WRITE}}$ HIGH Hold Time	20		20		20		ns
TWD	Data from $\overline{\text{WRITE}}$ HIGH Hold Time	30		30		30		ns
TWWS	Write Width	200		200		200		ns
TAD	Data Access from ADR Valid, $\overline{\text{CS}}$ LOW		350		300		300	ns

SWITCHING WAVEFORMS



Timing Diagram 1. Program Condition Write Timing (Note 9).

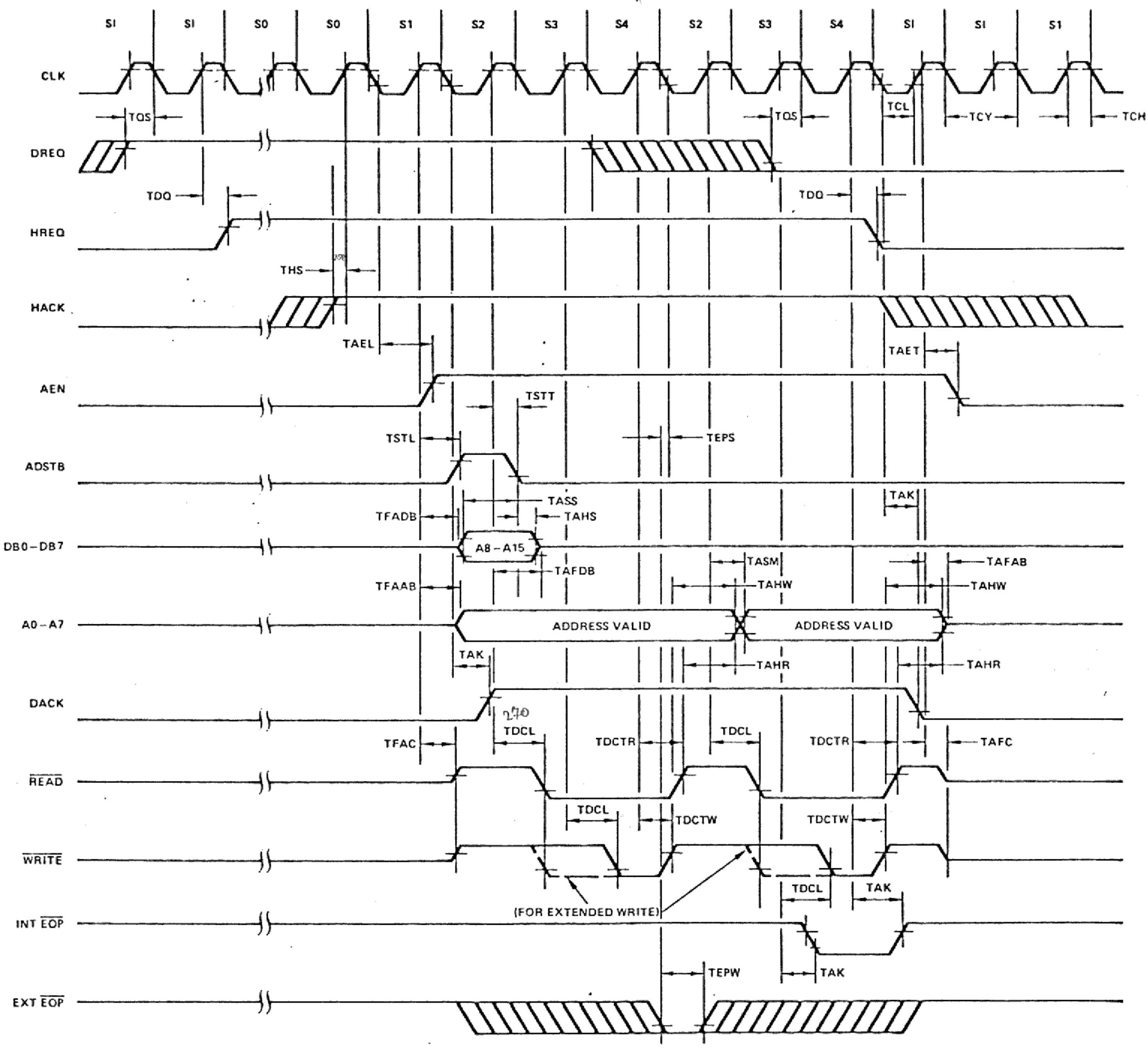
MOS-036



Timing Diagram 2. Program Condition Read Cycle (Note 9).

MOS-037

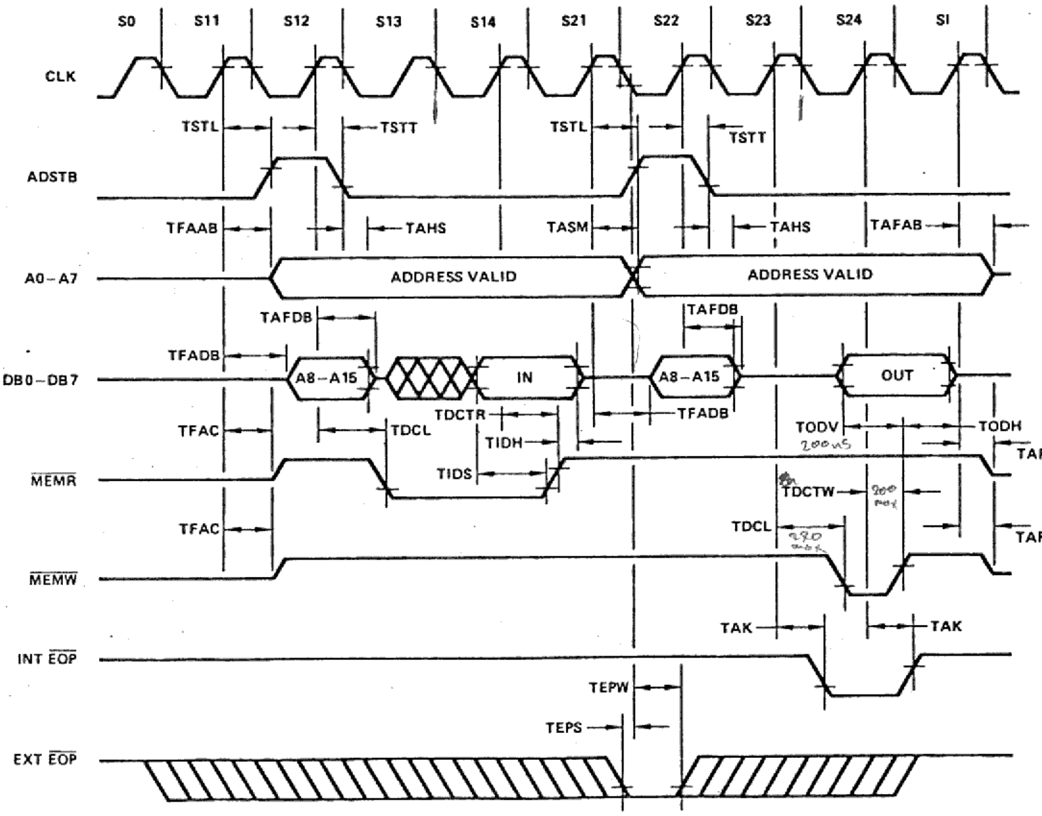
SWITCHING WAVEFORMS (Cont.)



Timing Diagram 3. Active Cycle Timing Diagram.

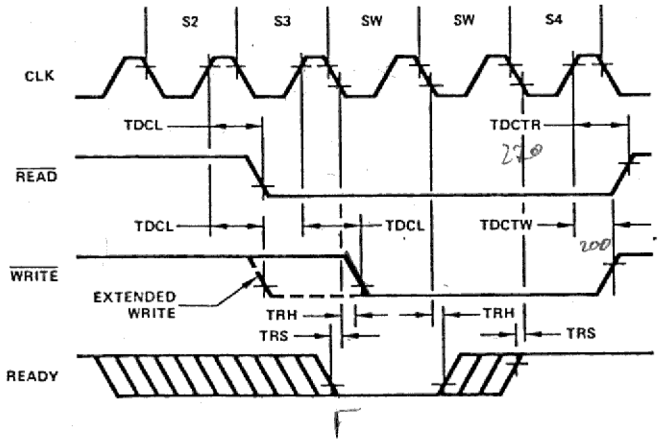
MOS-038

SWITCHING WAVEFORMS (Cont.)



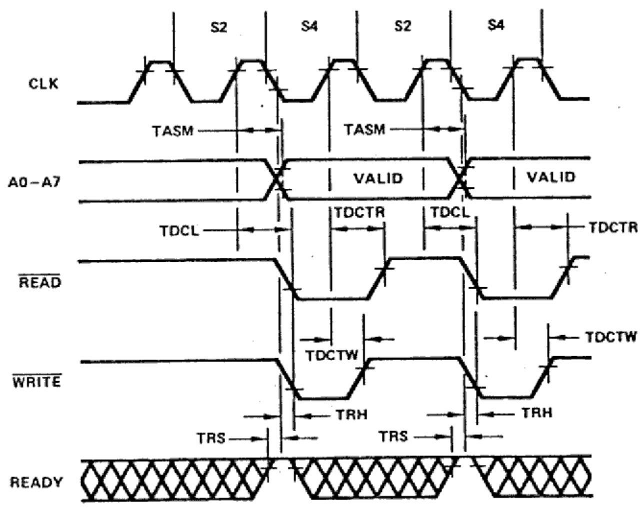
Timing Diagram 4. Memory-to-Memory.

MOS-039



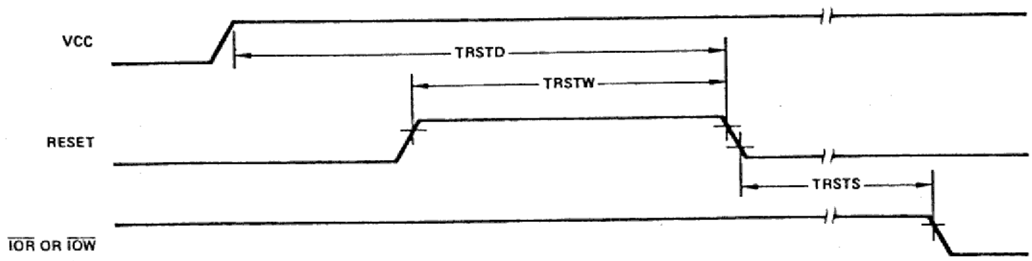
Timing Diagram 5. Ready Timing.

MOS-040



Timing Diagram 6. Compressed Timing.

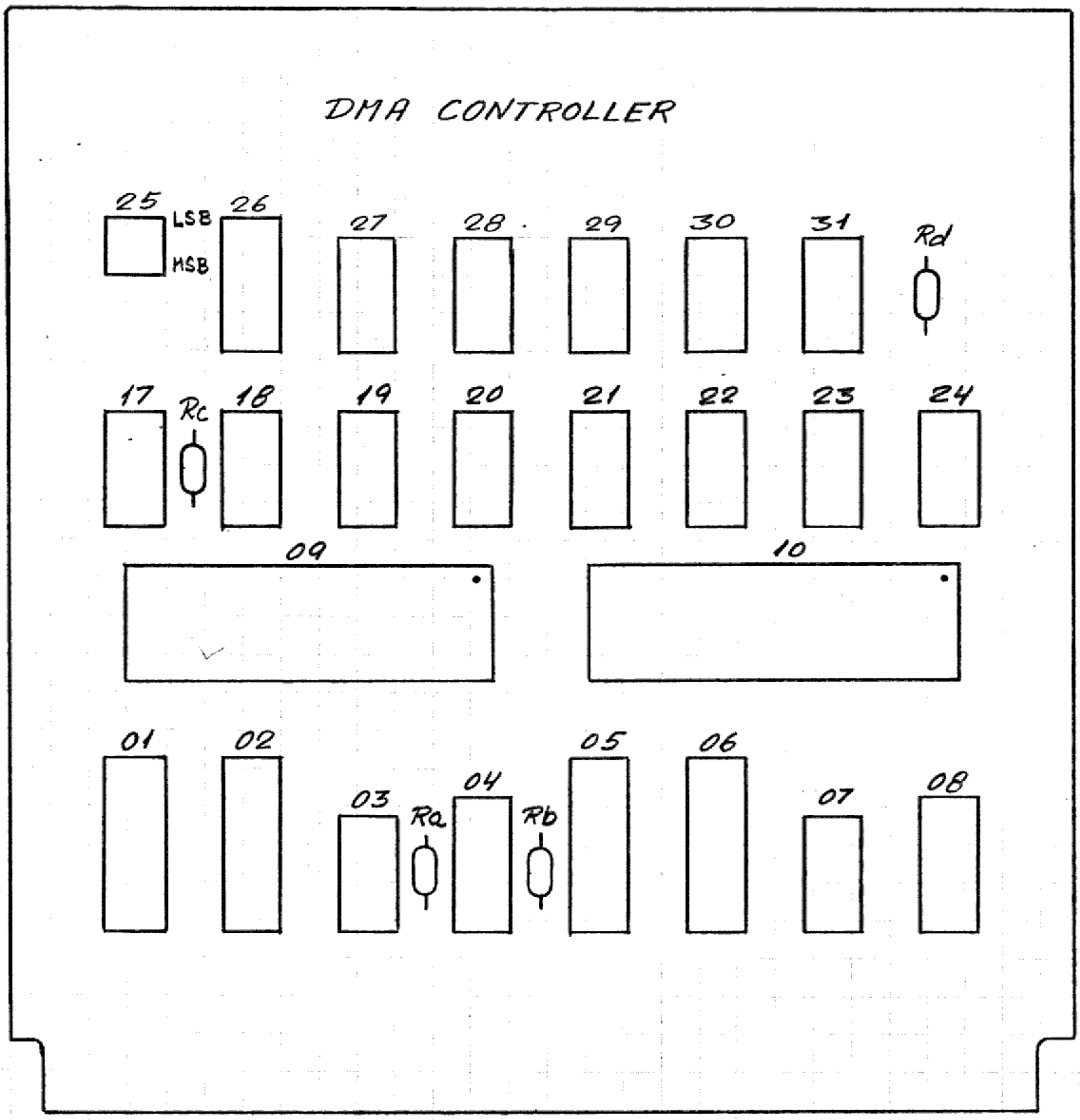
MOS-041

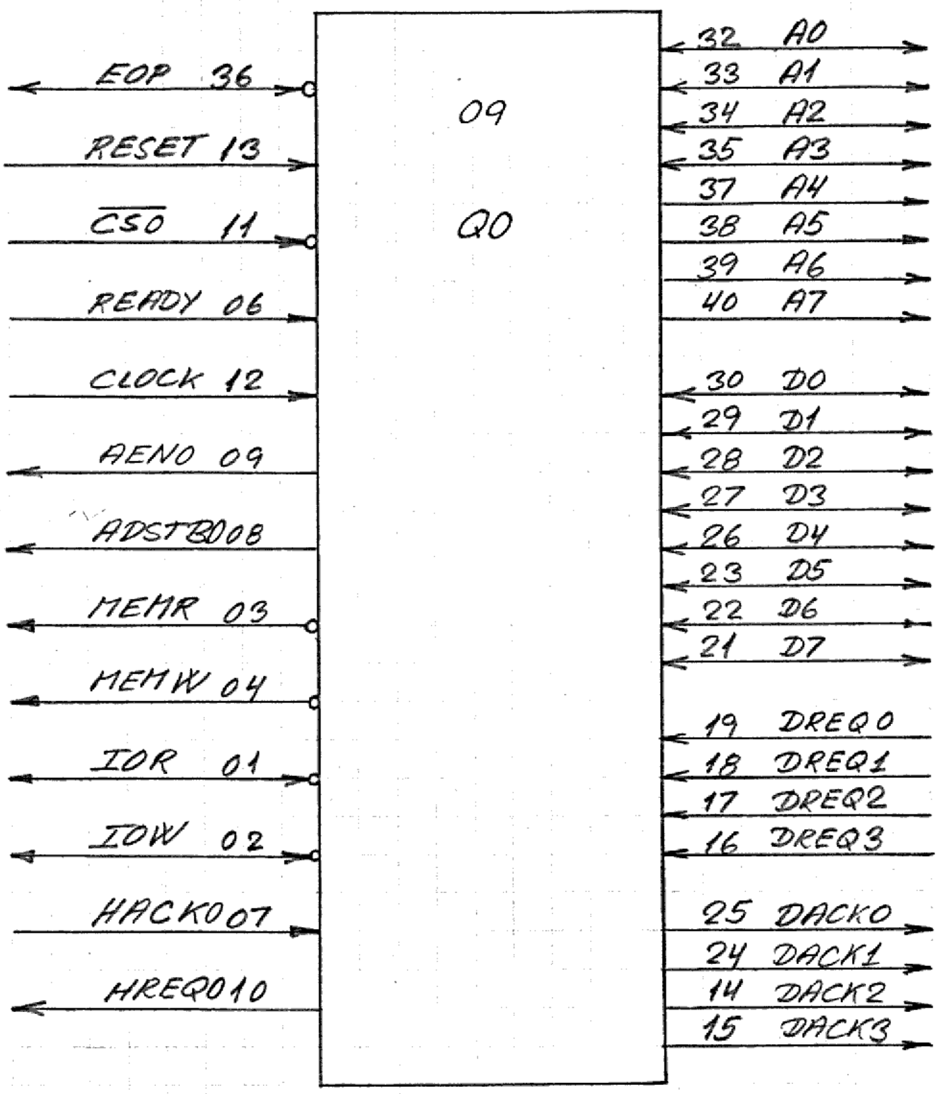


Timing Diagram 7. Reset Timing.

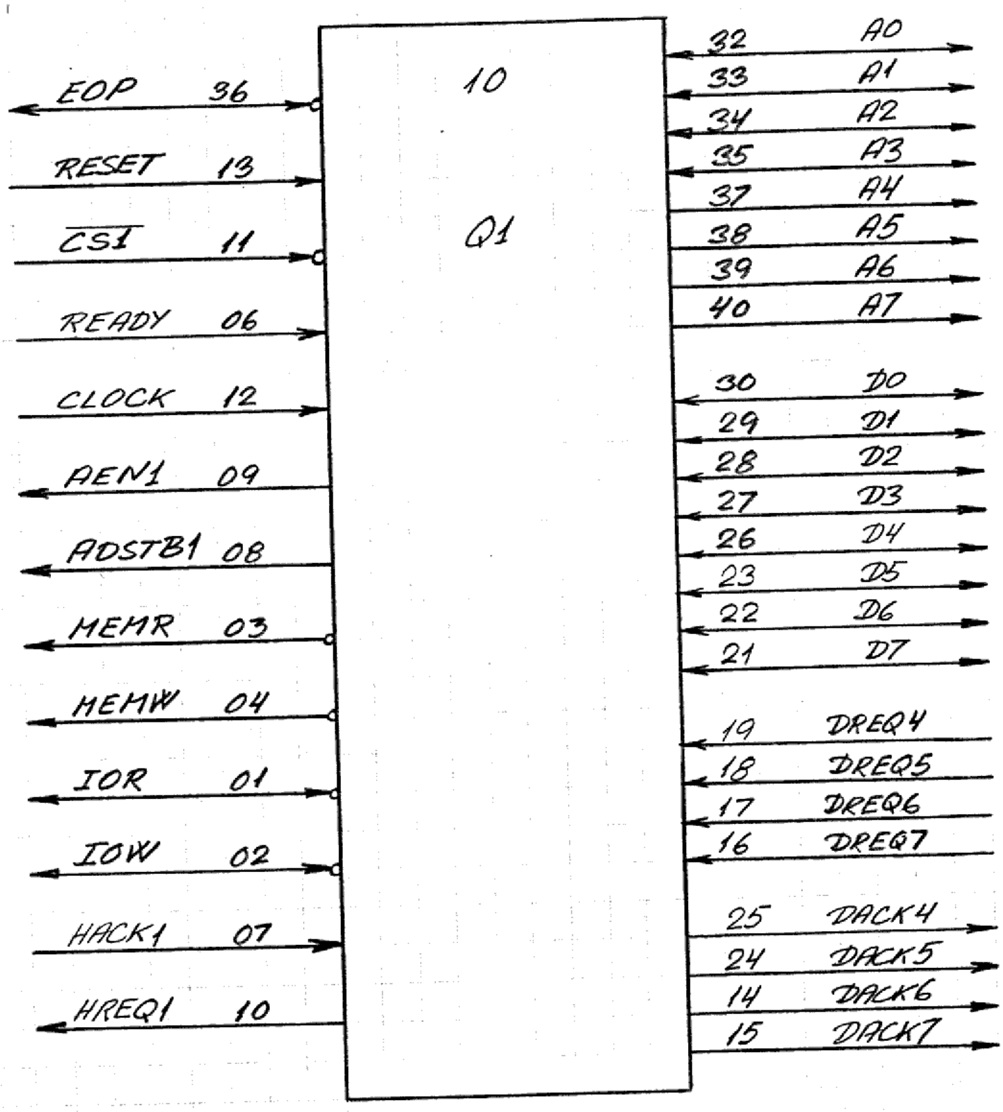
MOS-0

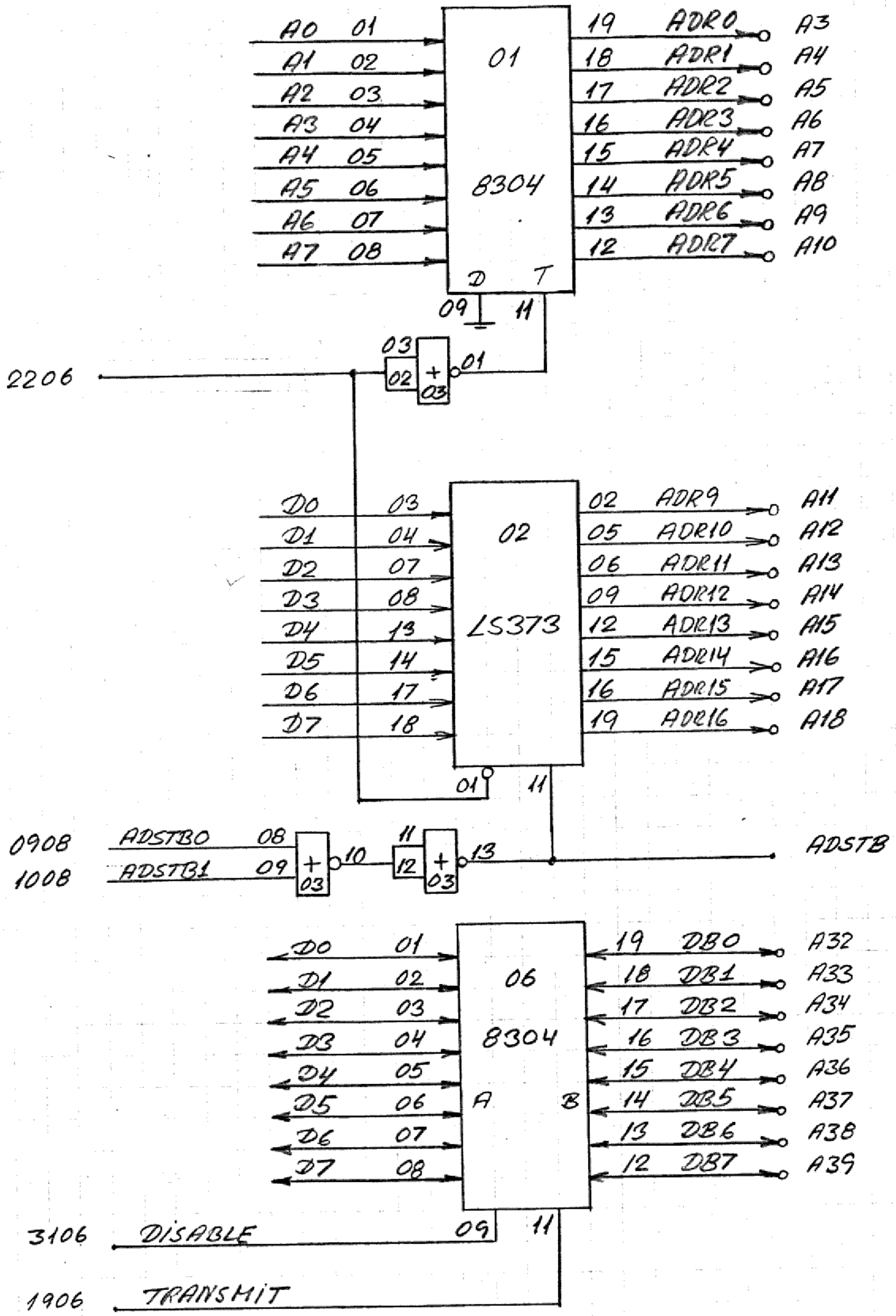
Appendix 2	Initialer/dato: KAN 781124	Side: 1
	Revideret	Projekt: 7009



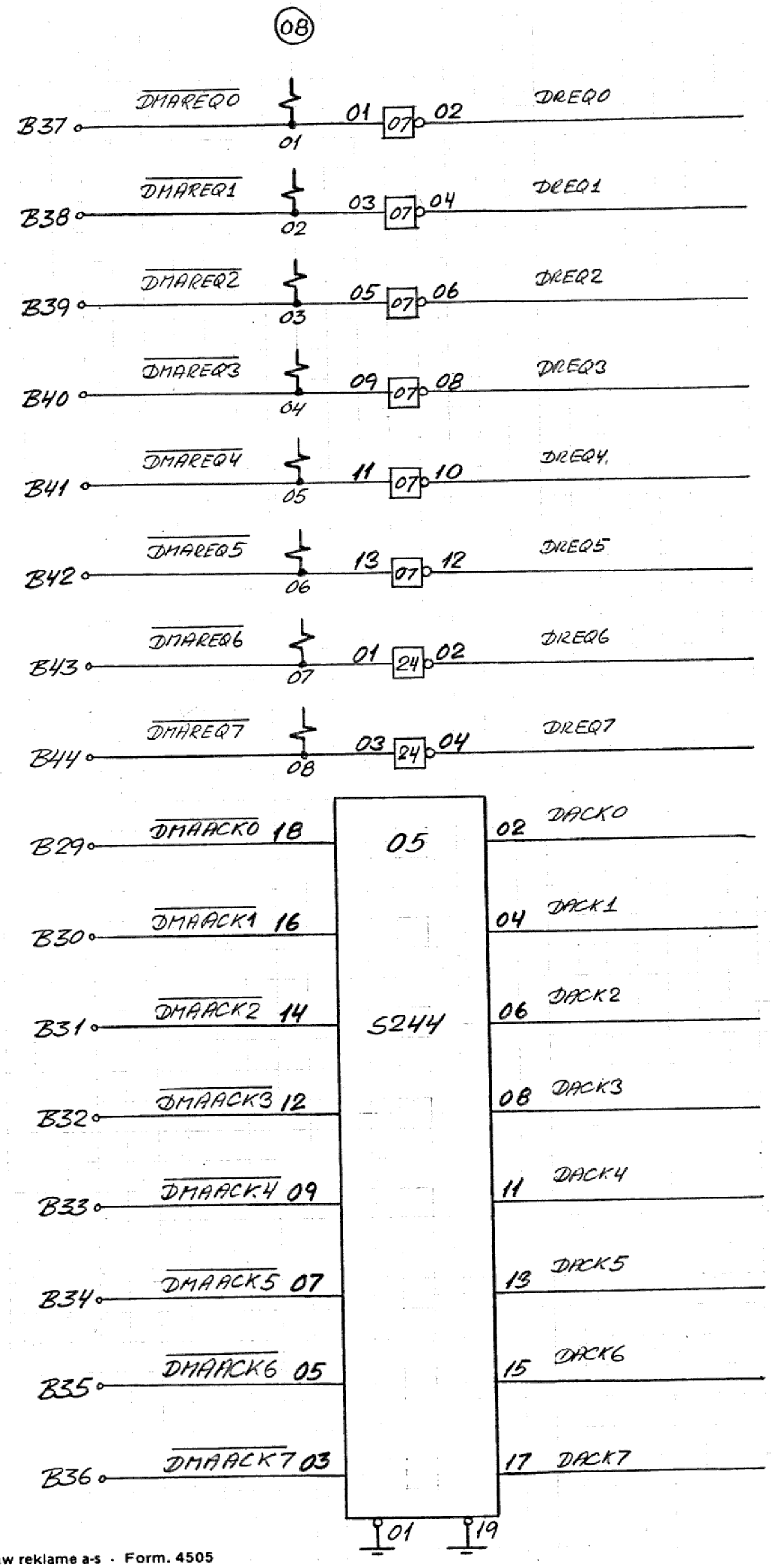


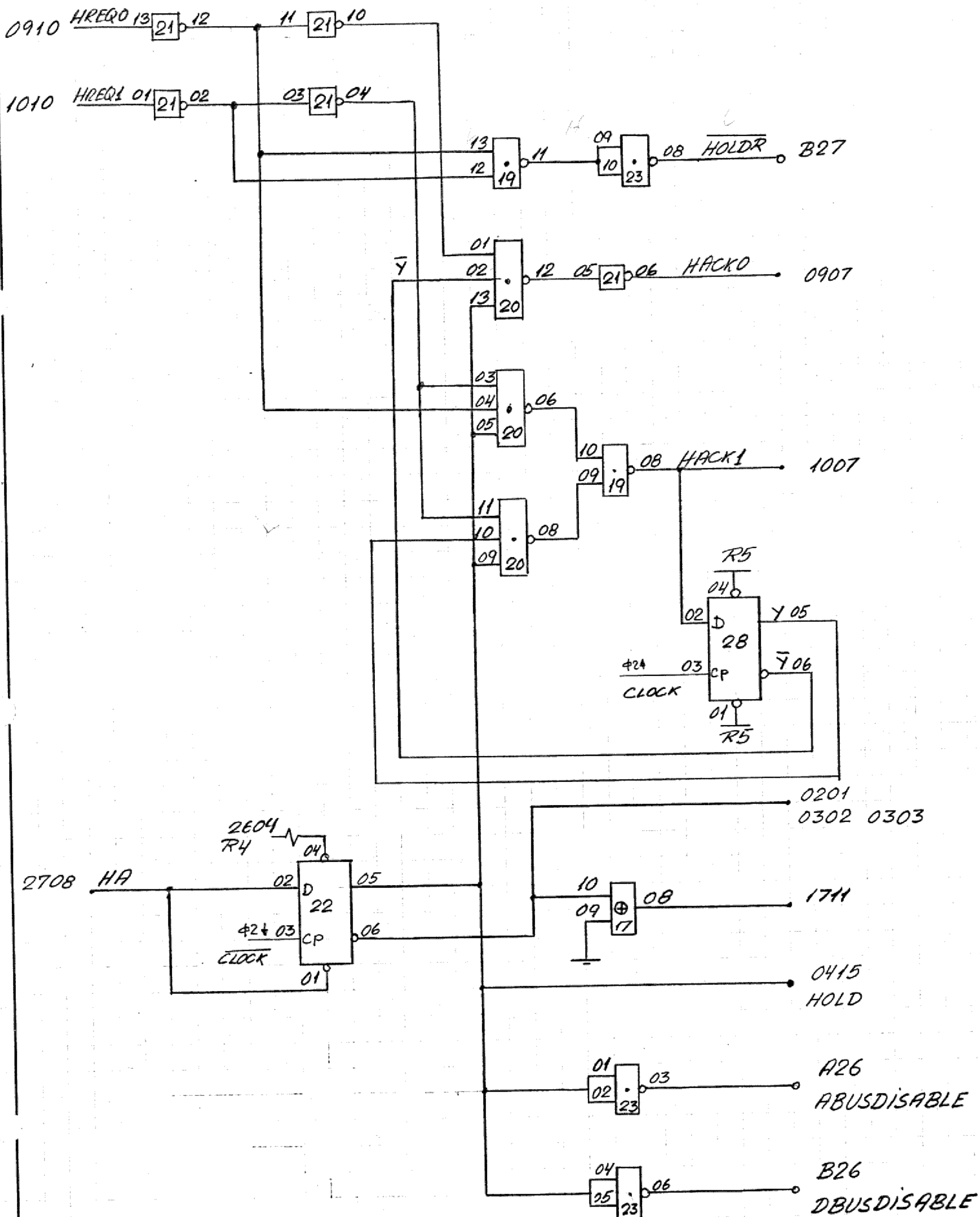
09
Q0
EOP 36
RESET 13
CSO 11
READY 06
CLOCK 12
AENO 09
ADSTB008
MEMR 03
MEMW 04
IOR 01
IOW 02
HACK007
HREQ010
32 A0
33 A1
34 A2
35 A3
37 A4
38 A5
39 A6
40 A7
30 D0
29 D1
28 D2
27 D3
26 D4
23 D5
22 D6
21 D7
19 DREQ0
18 DREQ1
17 DREQ2
16 DREQ3
25 DACK0
24 DACK1
14 DACK2
15 DACK3


10
Q1
EOP 36
RESET 13
CS1 11
READY 06
CLOCK 12
AEN1 09
ADSTB1 08
MEMR 03
MEMW 04
IOR 01
IOW 02
HACK1 07
HREQ1 10
32 A0
33 A1
34 A2
35 A3
37 A4
38 A5
39 A6
40 A7
30 D0
29 D1
28 D2
27 D3
26 D4
23 D5
22 D6
21 D7
19 DREQ4
18 DREQ5
17 DREQ6
16 DREQ7
25 DACK4
24 DACK5
14 DACK6
15 DACK7

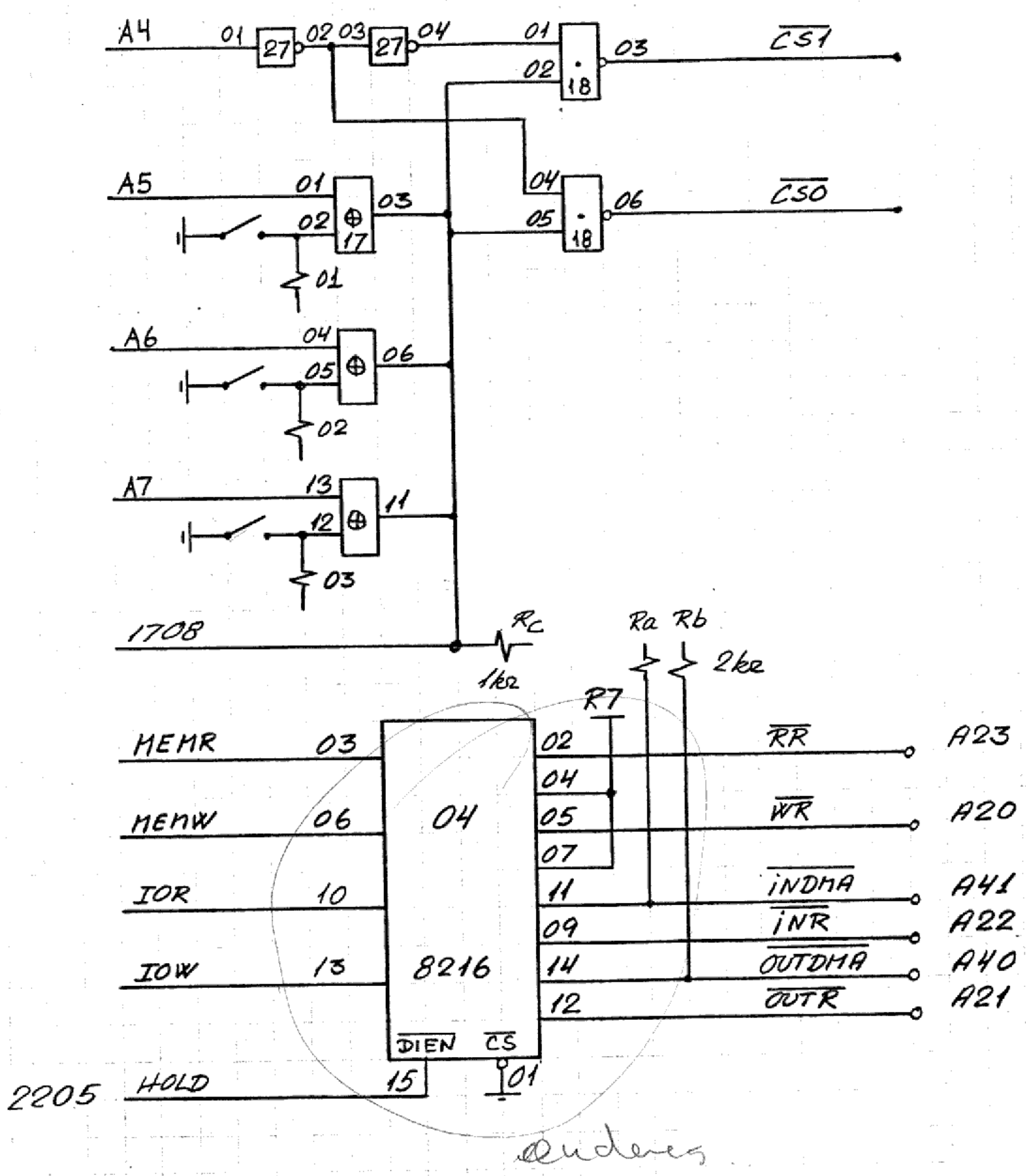


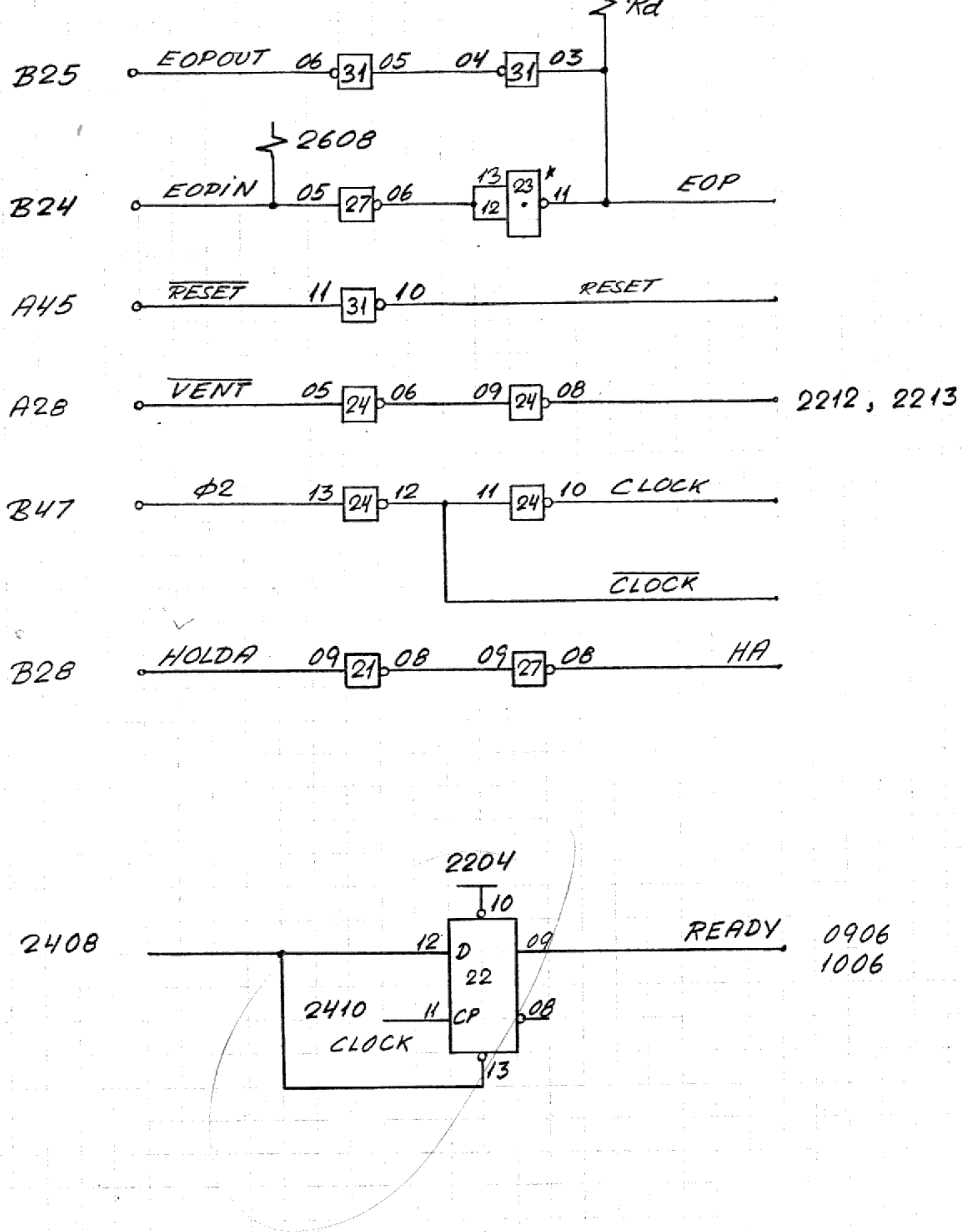
A0 01
A1 02
A2 03
A3 04
A4 05
A5 06
A6 07
A7 08
01
8304
D T
09 11
19 ADR0 A3
18 ADR1 A4
17 ADR2 A5
16 ADR3 A6
15 ADR4 A7
14 ADR5 A8
13 ADR6 A9
12 ADR7 A10
2206
03 02 03 01
D0 03
D1 04
D2 07
D3 08
D4 13
D5 14
D6 17
D7 18
02
LS373
01 11
02 ADR9 A11
05 ADR10 A12
06 ADR11 A13
09 ADR12 A14
12 ADR13 A15
15 ADR14 A16
16 ADR15 A17
19 ADR16 A18
0908 ADSTB0 08
1008 ADSTB1 09
03 10 11 12 03 13
ADSTB
D0 01
D1 02
D2 03
D3 04
D4 05
D5 06
D6 07
D7 08
06
8304
A B
19 DB0 A32
18 DB1 A33
17 DB2 A34
16 DB3 A35
15 DB4 A36
14 DB5 A37
13 DB6 A38
12 DB7 A39
3106 DISABLE 09 11
1906 TRANSMIT


08
B37 DMAREQ0 01 01 07 02 DREQ0
B38 DMAREQ1 02 03 07 04 DREQ1
B39 DMAREQ2 03 05 07 06 DREQ2
B40 DMAREQ3 04 09 07 08 DREQ3
B41 DMAREQ4 05 11 07 10 DREQ4
B42 DMAREQ5 06 13 07 12 DREQ5
B43 DMAREQ6 07 01 24 02 DREQ6
B44 DMAREQ7 08 03 24 04 DREQ7
05
S244
B29 DMAACK0 18 02 DACK0
B30 DMAACK1 16 04 DACK1
B31 DMAACK2 14 06 DACK2
B32 DMAACK3 12 08 DACK3
B33 DMAACK4 09 11 DACK4
B34 DMAACK5 07 13 DACK5
B35 DMAACK6 05 15 DACK6
B36 DMAACK7 03 17 DACK7
01
19



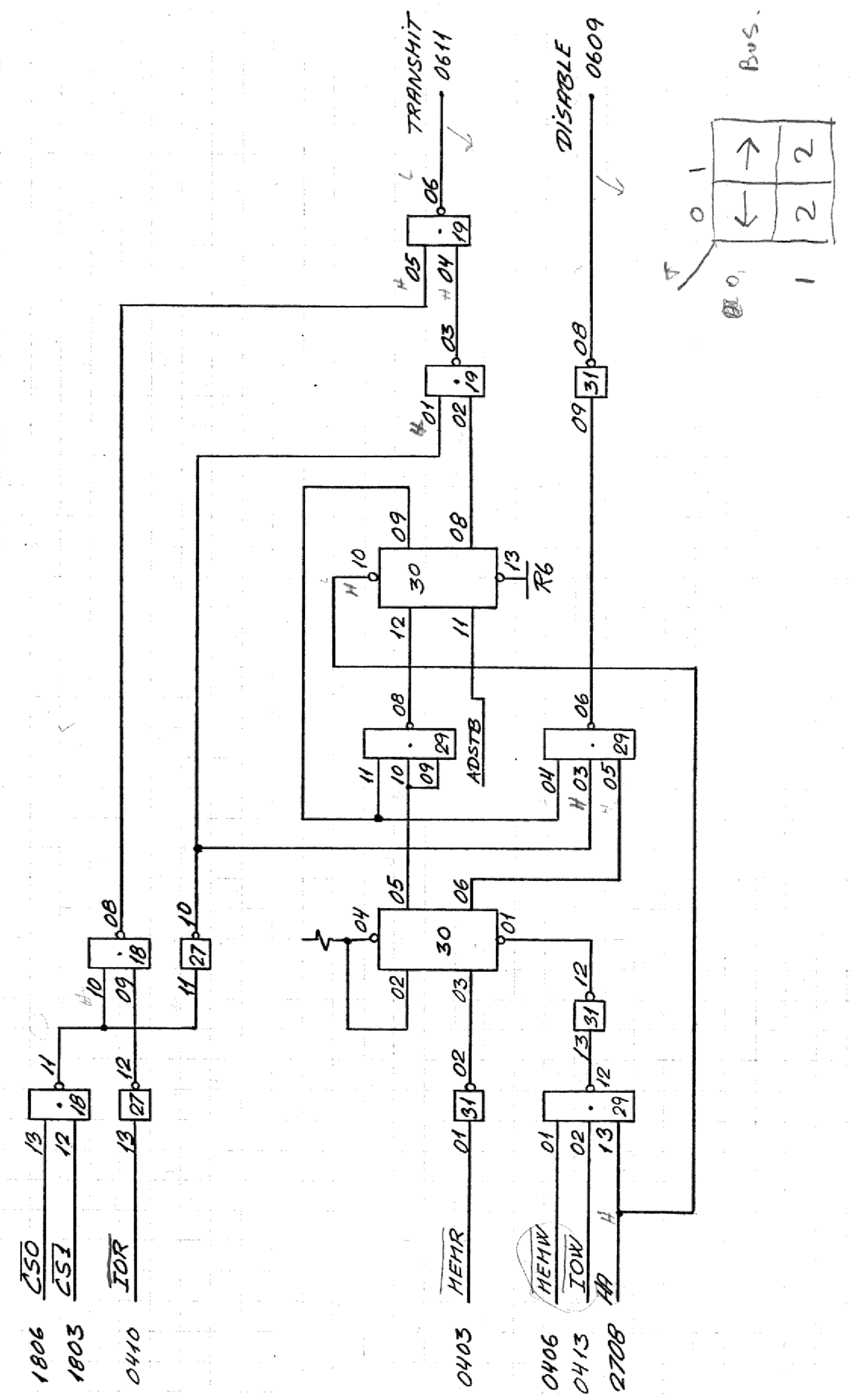
0910
HREQ0
1010
HREQ1
HOLDR
B27
HACK0
0907
HACK1
1007
R5
D
28
CP
CLOCK
0201
0302 0303
2E04
R4
2708
HA
22
1711
0415
HOLD
A26
ABUSDISABLE
B26
DBUSDISABLE


A4
01
27
02
03
27
04
01
02
03
18
CS1
A5
01
02
03
17
04
05
06
18
CS0
01
A6
04
05
06
02
A7
13
12
11
03
1708
Rc
1kΩ
Ra
Rb
2kΩ
R7
MEMR
03
MEMW
06
IOR
10
IOW
13
04
8216
02
04
05
07
11
09
14
12
DIEN
CS
15
01
RR
A23
WR
A20
INDMA
A41
INR
A22
OUTDMA
A40
OUTR
A21
2205
HOLD
ændres


Rd
B25
EOPOUT
06
31
05
04
31
03
2608
B24
EOPIN
05
27
06
13
12
23
11
EOP
A45
RESET
11
31
10
RESET
A28
VENT
05
24
06
09
24
08
2212, 2213
B47
φ2
13
24
12
11
24
10
CLOCK
CLOCK
B28
HOLDA
09
21
08
09
27
08
HA
2204
10
2408
12
D
22
09
READY
0906
1006
2410
CLOCK
11
CP
08
13

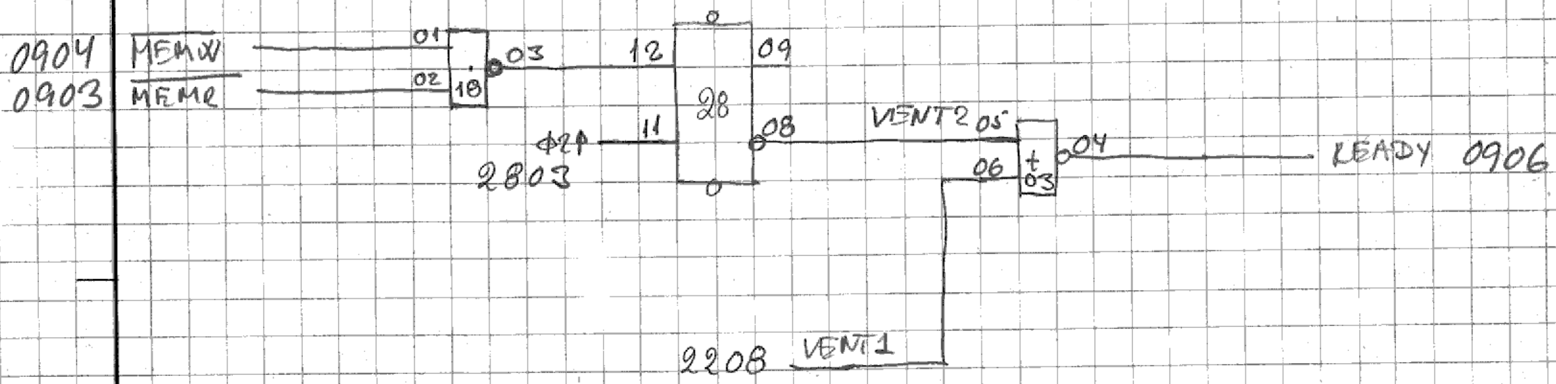
dansk data elektronik aps

Initialer/dato	Side
KAN 781124	9
Revideret	**Projekt**
	7009



dde dansk data elektronik aps

Initialer/dato	Side
Revideret	Projekt



rettelse af hensyn til 8530 (5MHz CPU)