DANSK DATA ELEKTRONIK

ID-7011 PROM-WRITER MODULE

for the

ID-7000 MICROPROCESSOR SYSTEM

December 1975.

Written by Ole Lading.

1. General description.

This module is used to program the INTEL N-channel erasable PROM's 2704 and 2708. The module contains a 10 bit address buffer register and an 8 bit data buffer register for the PROM to be programmed. These registers are loaded from the CPU by execution of OUT-instructions. Input instructions transfer a status word from the module and the contents of the PROM to the CPU.

The PROM to be programmed may be plugged into a socket placed on the module, or into a socket in a box connected to the module via the top connector.

The module is used in combination with the PROM-writer facility, which is a part of the ID-7000 Debug program. For use of the PROM writer facility, refer to the ID-7000 DEBUG description.

Fig. 1 shows a blocked schematic of the module.

Appendix 1 is a complete logic schematic of the module.

Appendix 2 is a data sheet of the 2704/2708 PROM's.

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2. Programming description.

The module uses four consecutive I/O-addresses, starting at a base address determined by a 6 bit switch register on the module. The four addresses are used as follows:

OUT 4n : Loads the 8 least significant bits of the address buffer register:

A7	A6	A5	A4	A3	A2	A1	A0
7	6	5	4	3	2	1	0

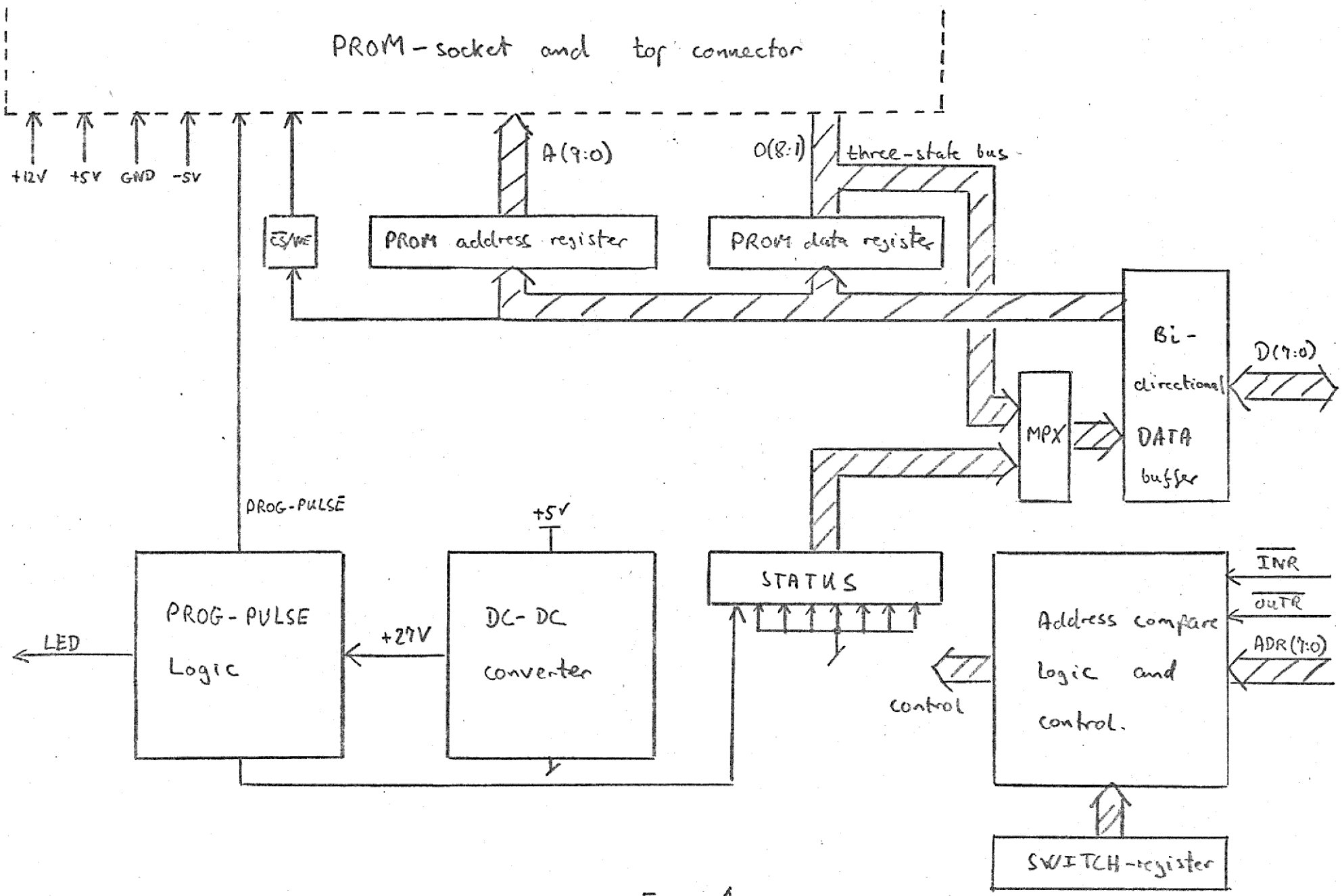

Fig. 1

Navn: ID-7011, PROM-writer module, blocked schematic.
Lb. nr.
Dato
Emne
Fag
Afd.
Side 2

OUT 4n + 1 : Loads the 2 most significant bits of the address buffer register, and determines the mode of the module (WRITE/READ mode):

WRITE						A9	A8

OUT 4n + 2 : Loads the data buffer register.

08	07	06	05	04	03	02	01

OUT 4n + 3 : The transferred data of this OUT-instruction is irrelevant. Execution of this OUT-instruction generates one programming pulse (1 msec) to the PROM.

IN 4n : not used.

IN 4n + 1 : not used.

IN 4n + 2 : Transfers the contents of the PROM word adressed by the address buffer registqr to the accumulator of the CPU:

08	07	06	05	04	03	02	01

IN 4n + 3 : Transfers the module status word to the accumulator of the CPU. Only one bit of the status word is used, to indicate whether the programming pulse is still on, or whether the module is ready:

READY	0	0	0	0	0	0	0

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3. PROM-interface.

The PROM to be programmed may be plugged into a 24 pin dual-in-line socket on the module, or alternatively into a box connected to the module via the top connector. The module needs no external power supplies.

The connections to the socket and the top connector are shown in table 1. The electrical characteristics of the different signals are in accordance with the requirements given in the 2704/2708 data sheet (appendix 2).

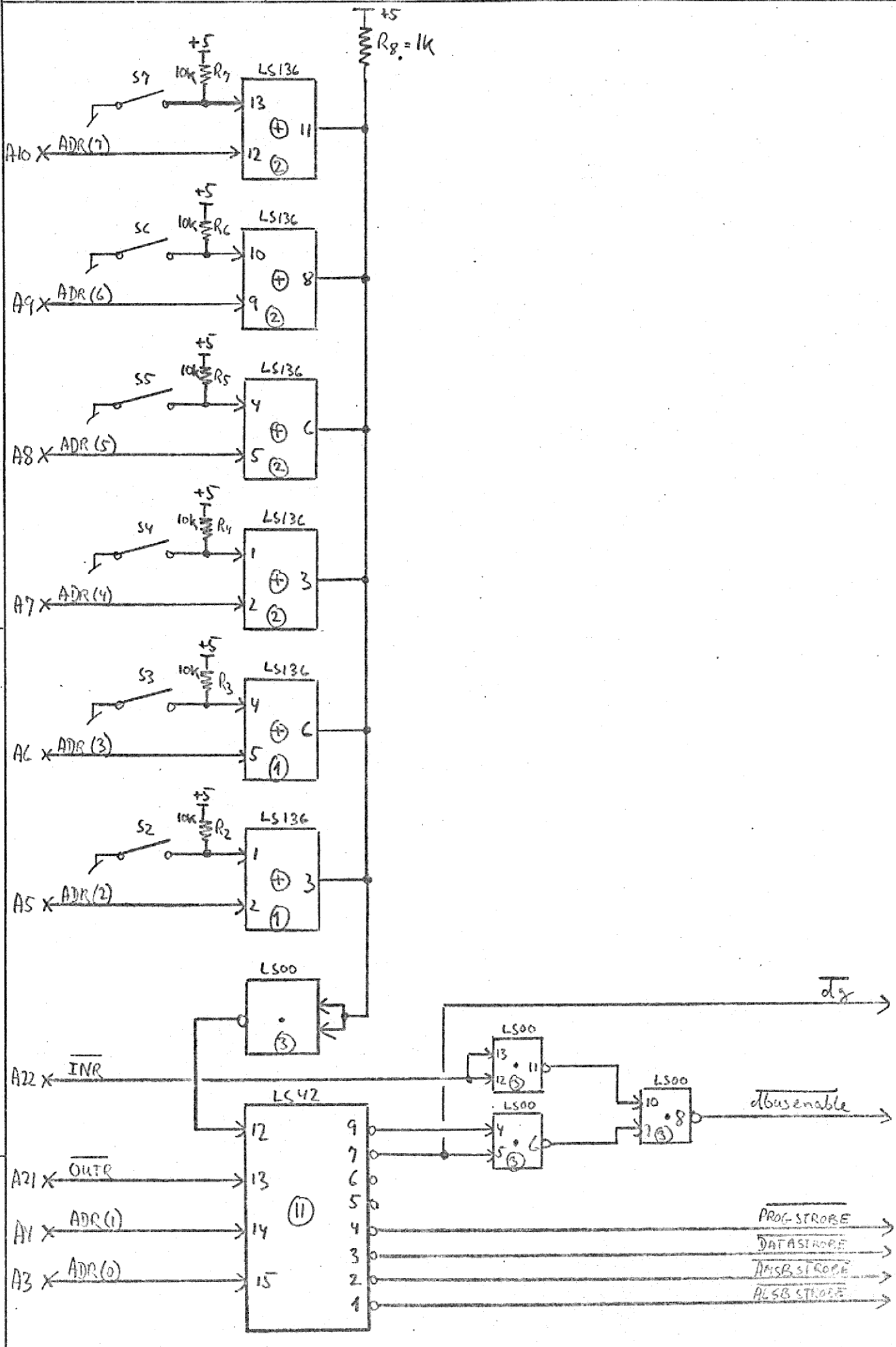
One pin in the top connector may be used for connection of a LED-indicator. The pin is at a low level, when the module is in read mode. The output has a serial resistance of 300 ohms. The LED-indicator may be connected directly between this pin and the +5 V supply.

Table 1. PROM-interface

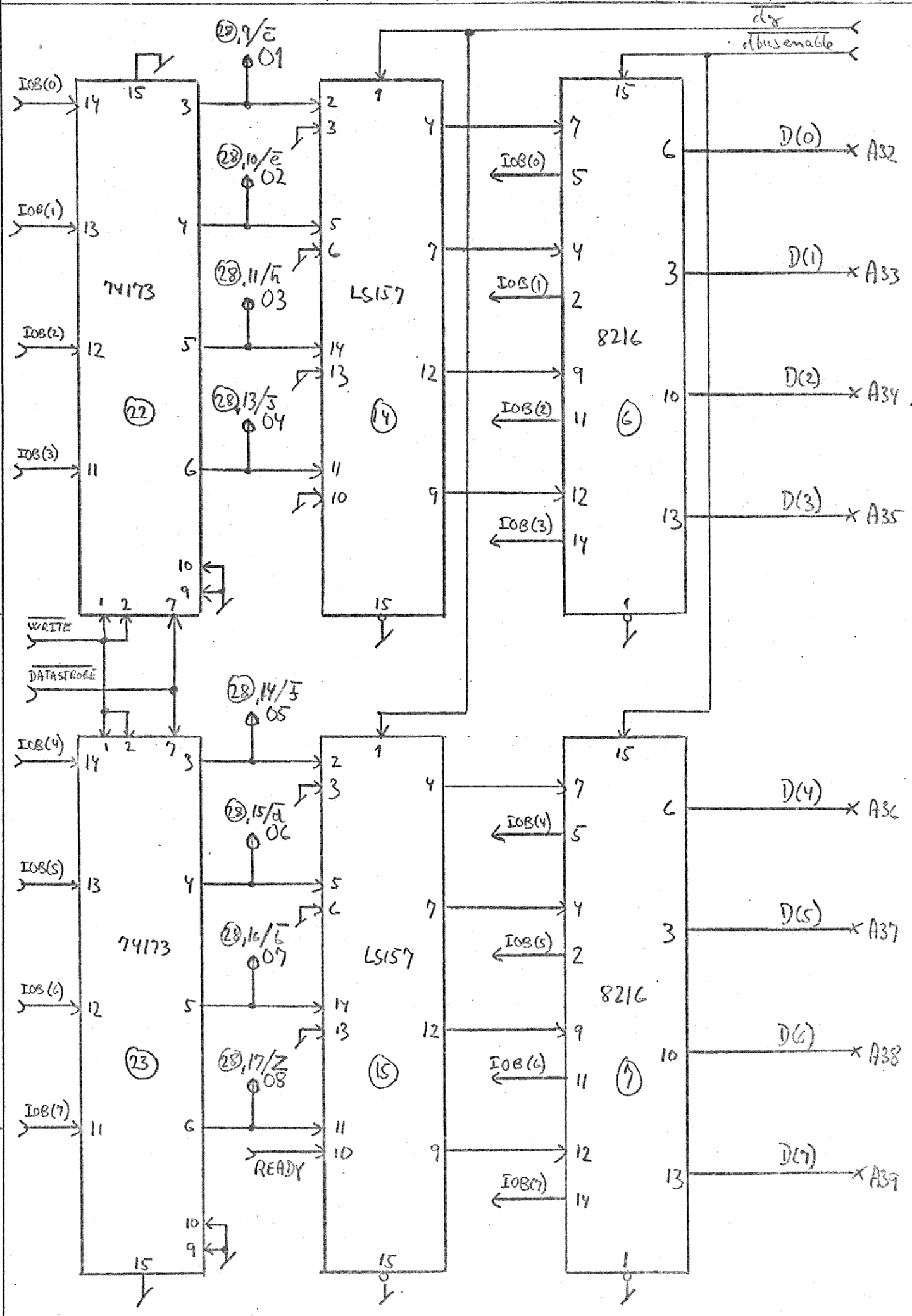
Signal name	description	pin nr. socket	pin nr. topconn.
A7	PROM-address bit 7	1	K
A6	" bit 6	2	M
A5	" bit 5	3	P
A4	" bit 4	4	S
A3	" bit 3	5	U
A2	" bit 2	6	W
A1	" bit 1	7	Y
A0	" bit 0	8	a
O1	PROM-data bit 1 */	9	c
O2	" bit 2	10	e
O3	" bit 3	11	h
GND		12	1
O4	PROM-data bit 4	13	j
O5	" bit 5	14	f
O6	" bit 6	15	d
O7	" bit 7	16	b
O8	" bit 8	17	Z
PROG PULSE	PROM-programming pulse	18	X
+12V		19	V
$\overline{CS}/WE$	$\overline{\text{chip select}}$/write enable	20	T
-5V		21	R
A9	PROM-address bit 9	22	N
A8	" bit 8	23	L
+5V		24	A
LED	LED-indicator	—	J

*/ The PROM-data bits are numbered 1-8 according to the datasheet.

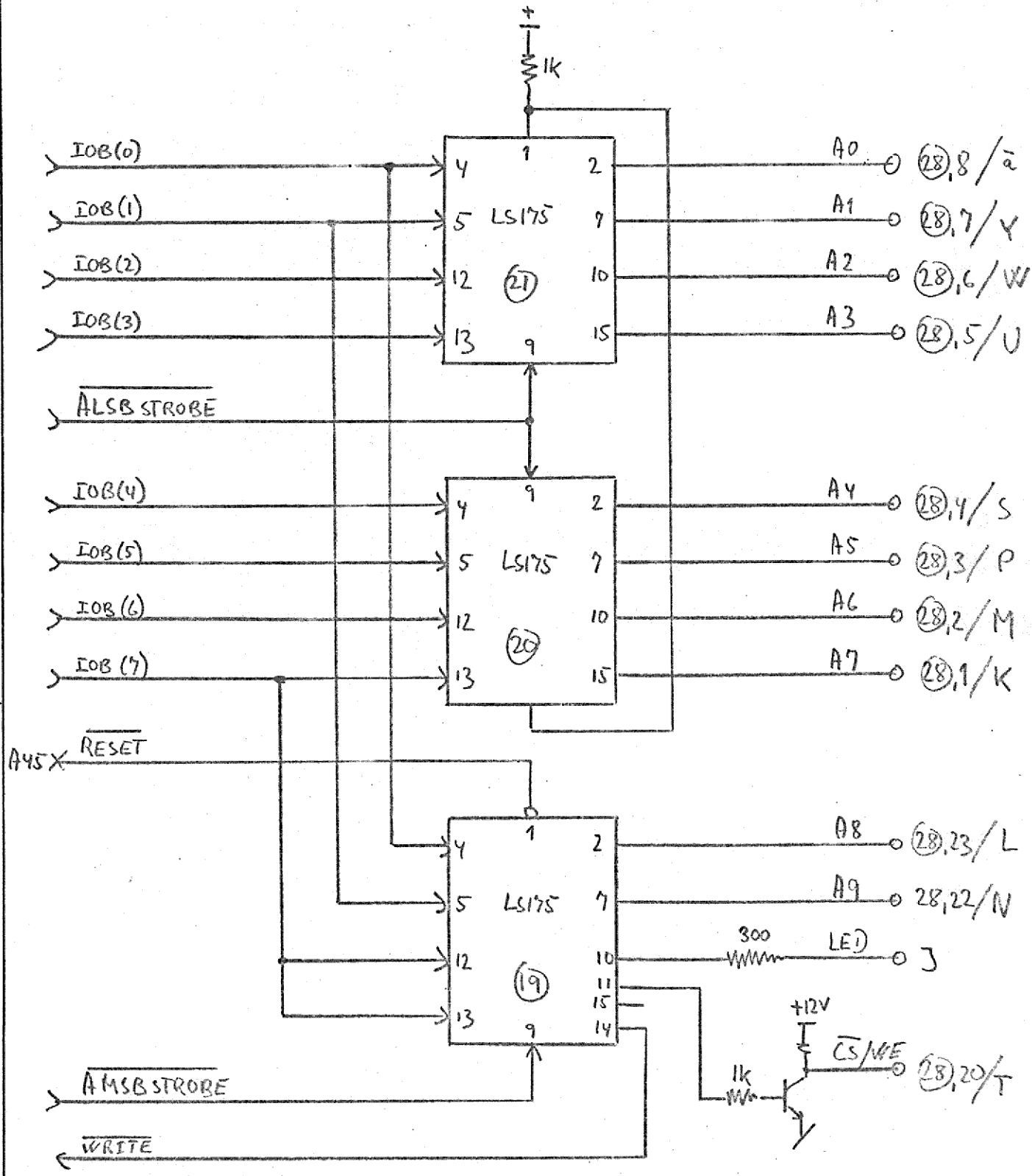
Navn	Lb. nr.	Dato	Emne	Fag	Ald.	Side
ID-7011. PROM-writer module Logic schematic: Addr. comp + contr.	A1.1	dec 75			O.L	



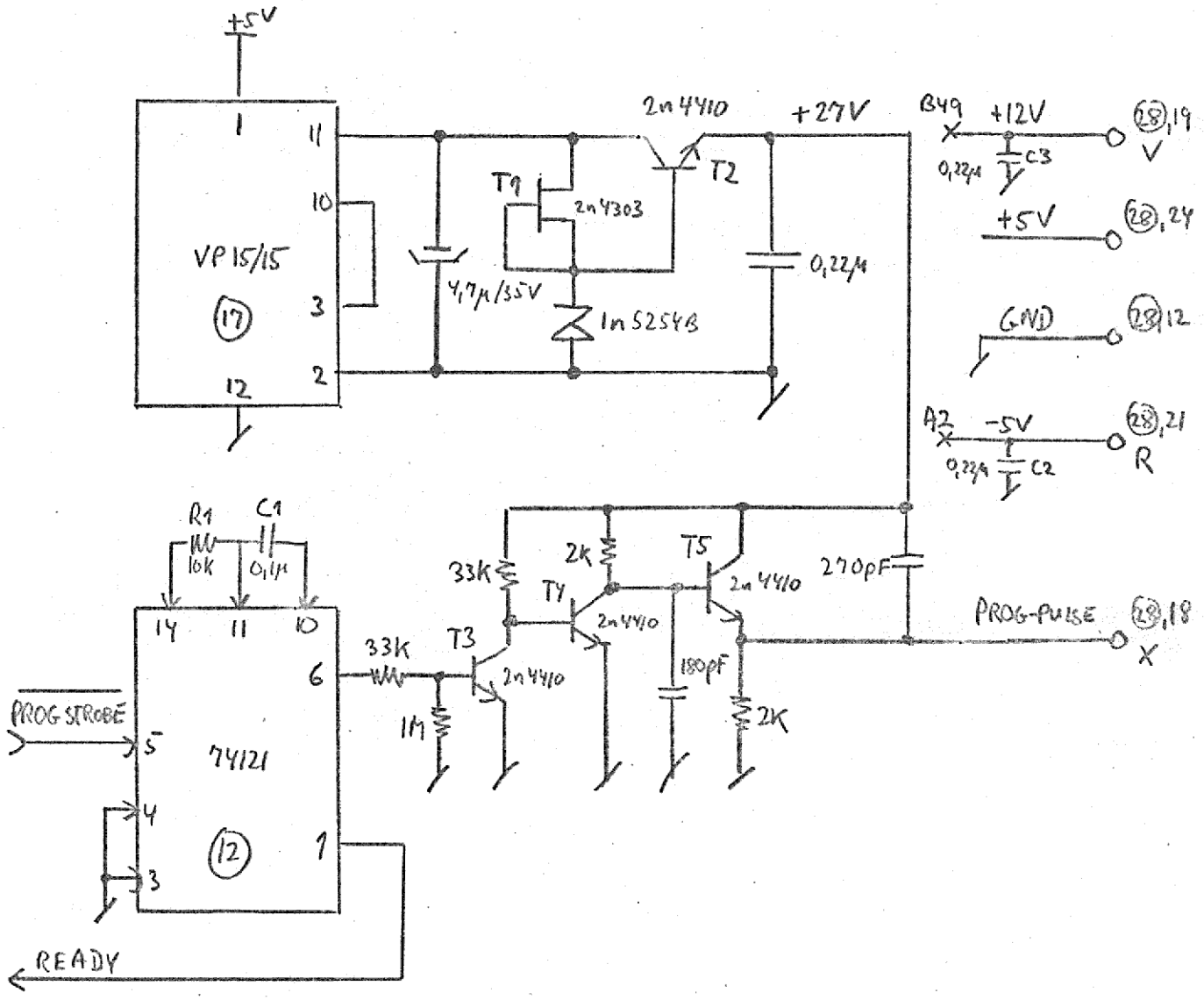
Navn	Lb. nr.	Dato	Emne	Fag	Afd.	Side
ID-7011 PROM-writer module Logic schematic: Busdrivers, MPX, Data reg.	A1.2	dec 75			OL	

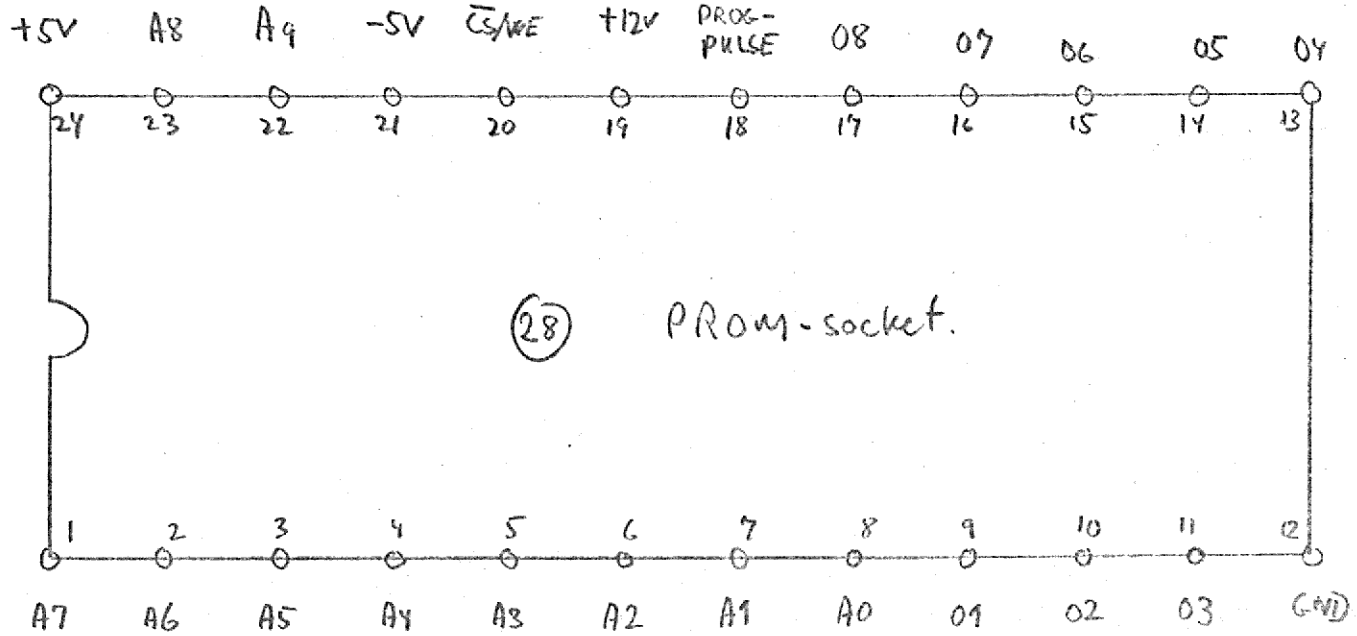


Navn	Lb. nr.	Dato	Emne	Fag	Afd.	Side
ID-7011 PROM-writer module logic schematic: PROM-adr. reg. + $\overline{CS}$/$\overline{WE}$-flip-flop	A1.3	dec 75			OL	



Navn	Lb. nr.	Dato	Emne	Fag	Afd.	Side
TD-9011 PROM-writer module Logic schematic: DC-DC-conv. + PROG-PULSE logic	A9.4	dec 75			OL	





Silicon Gate MOS 8708/8704

8192/4096 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

- 8708 1024x8 Organization
- 8704 512x8 Organization

- Fast Programming — Typ. 100 sec. For All 8K Bits
- Low Power During Programming
- Access Time — 450 ns
- Standard Power Supplies — +12V, ±5V
- Static — No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Three-State Output — OR-Tie Capability

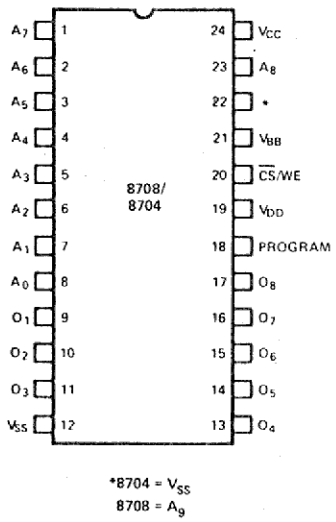
The Intel® 8708/8704 are high speed 8192/4096 bit erasable and electrically reprogrammable ROM's (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

The 8708/8704 are packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices.

A pin for pin mask programmed ROM, the Intel® 8308, is available for large volume production runs of systems initially using the 8708.

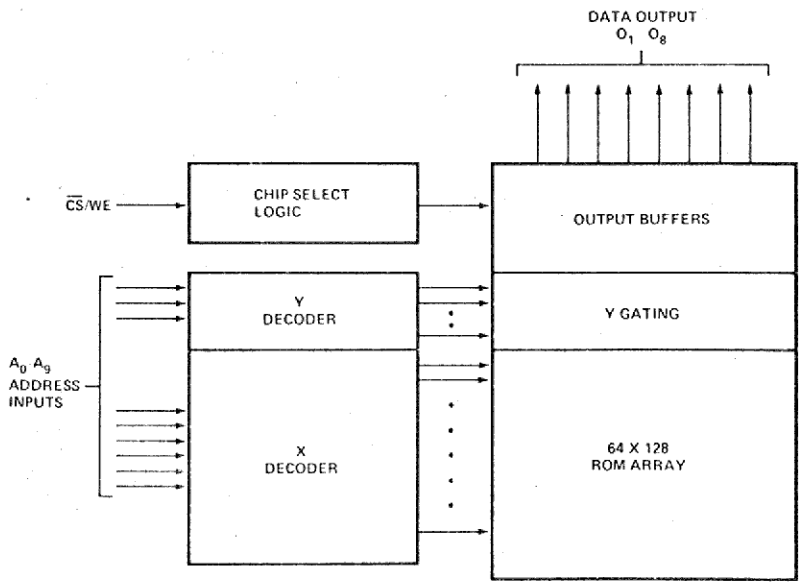
The 8708/8704 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATIONS



*8704 = V_{SS}
8708 = A_9

BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1 O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +125°C
All Input or Output Voltages with Respect to V_{BB}
(except Program) . . . . . +15V to -0.3V
Program Input to V_{BB} . . . . . +35V to -0.3V
Supply Voltages V_{CC} and V_{SS} with Respect to V_{BB} . . . . . +15V to -0.3V
V_{DD} with Respect to V_{BB} . . . . . +20V to -0.3V
Power Dissipation 1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V
I_{DD}	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. The program input (Pin 18) may be tied to V_{SS} or V_{CC} during the read mode.

A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
$t_{\overline{CO}}$	Chip Select to Output Delay			120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance[1] $T_A = 25°C$, f = 1MHz

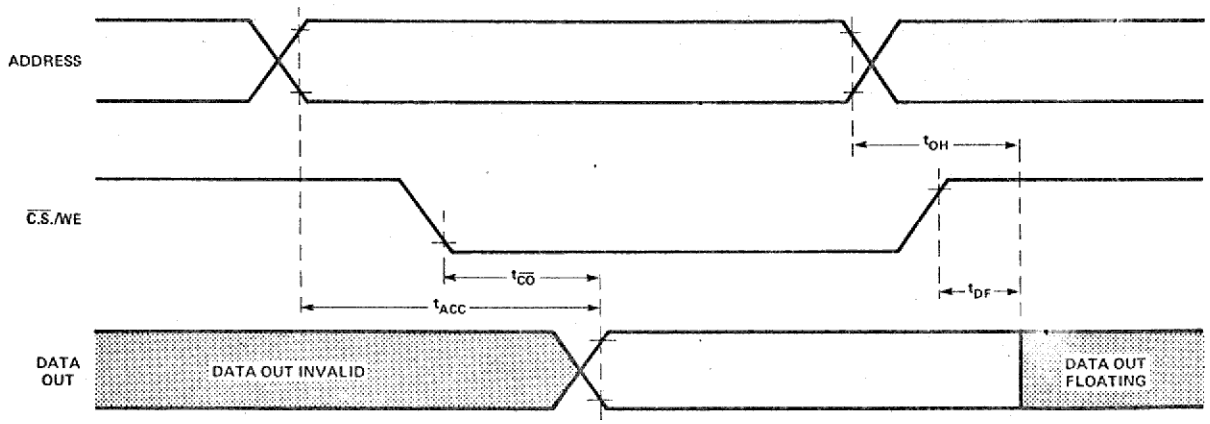
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN}=0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT}=0V$

Note 1. This parameter is periodically sampled and not 100% tested.

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤20ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

Waveforms



PROGRAMMING OPERATION

Description

Initially, and after each erasure, all bits of the 8708/8704 are in the "1" state (Output High). Information is introduced by selectively programming "0" into the desired bit locations.

The circuit is set up for programming operation by raising the $\overline{CS}$/WE input (Pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8-bits in parallel, to the data output lines (O_1-O_8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up one program pulse (V_P) per address is applied to the program input (Pin 18). One pass through all addresses to be programmed is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to $N \times t_{PW} \geqslant 100$ ms.

For program verification, program loops and read loops may be alternated as shown in waveform B.

Program Characteristics

$T_A = 25°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, $\overline{CS}$/WE = +12V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	$\overline{CS}$/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	$\overline{CS}$/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	.5		2.0	μs
I_P	Programming Current		10	20	mA
V_P	Program Pulse Amplitude	25		27	V

NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

Erasing Procedure

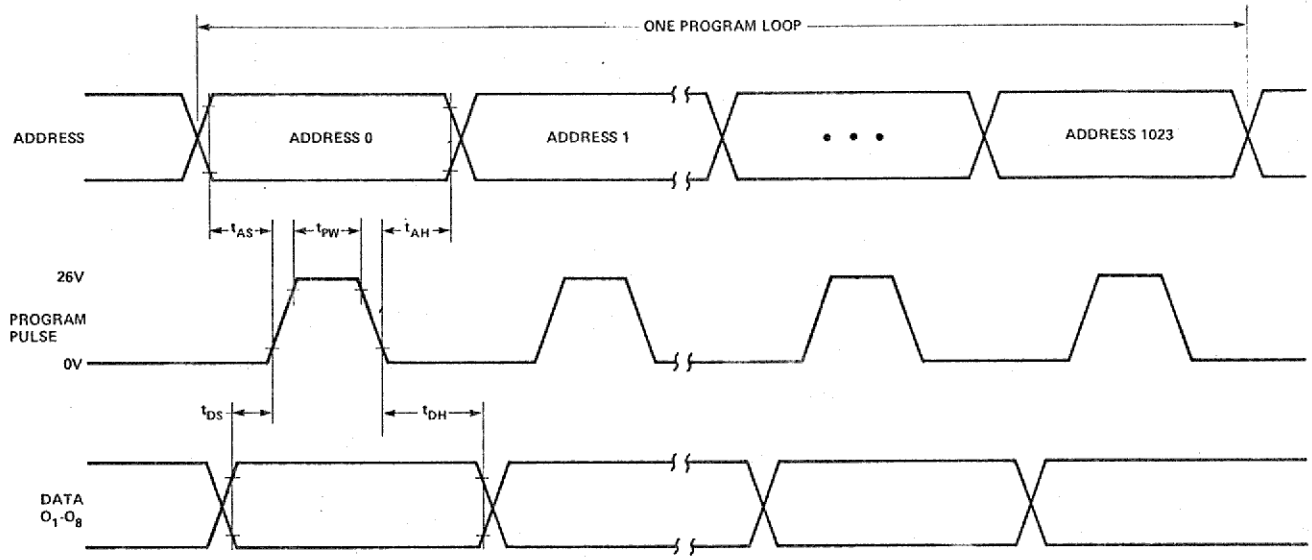
The 8708/8704 may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose. (i.e., UV intensity x exposure time) is 10W-sec/cm^2. Examples of ultraviolet sources which can erase the 8708/8704 in 20 to 30 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the 8708/8704 to be erased should be placed about one inch away from the lamp tubes.

Waveforms

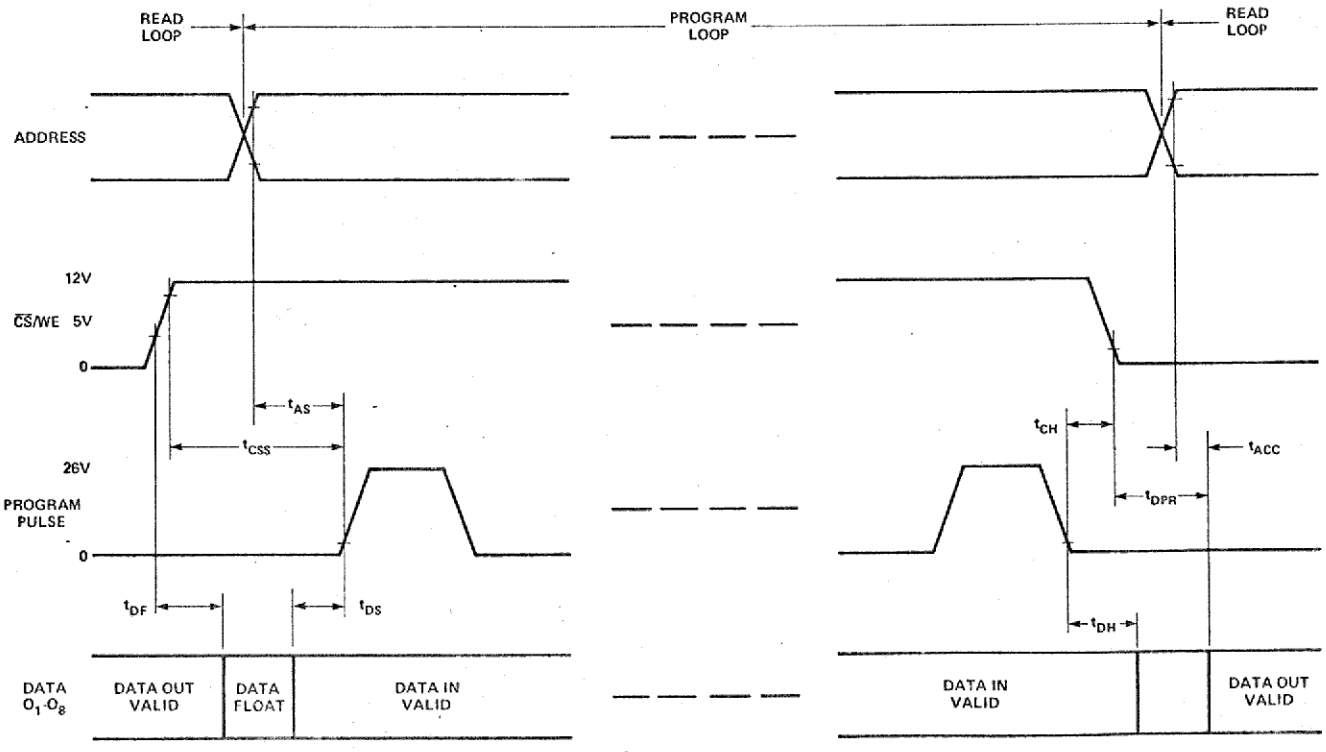
(Logic levels and timing reference levels same as in the Read Mode unless noted otherwise.)

A) Program Mode

$\overline{CS}$/WE = +12V

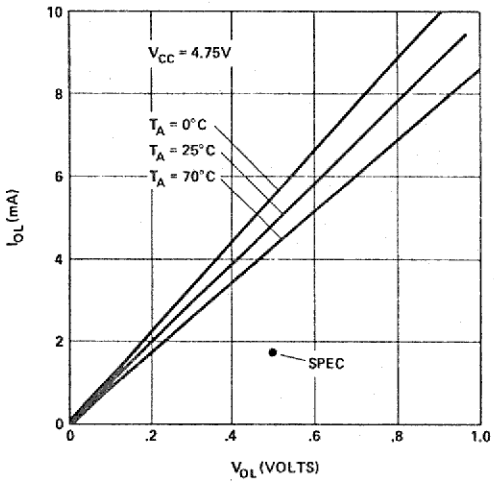


B) Read/Program/Read Transitions

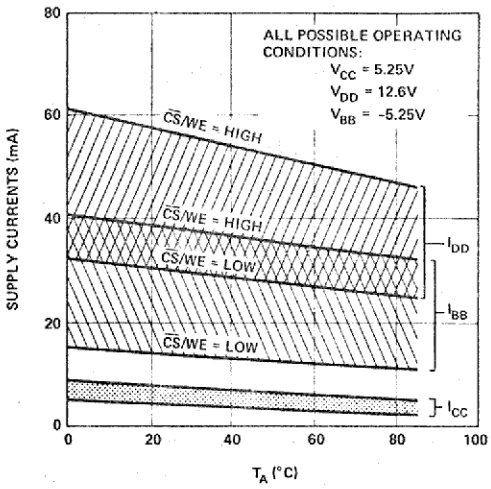


Typical Characteristics (Nominal supply voltages unless otherwise noted):

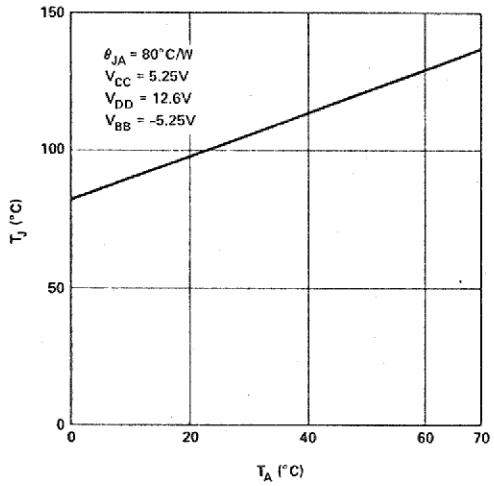
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE



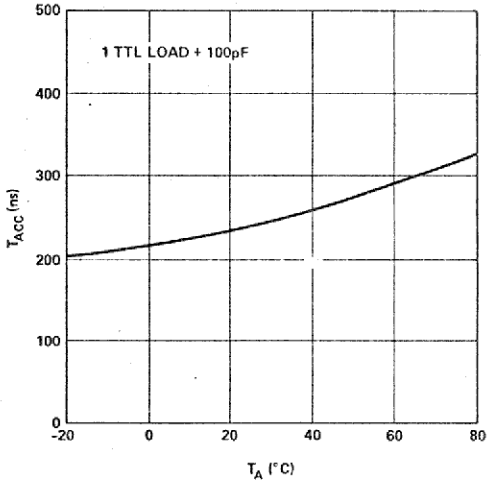
RANGE OF SUPPLY CURRENTS
VS. TEMPERATURE



MAXIMUM JUNCTION TEMPERATURE
VS. AMBIENT TEMPERATURE



ACCESS TIME VS. TEMPERATURE



ACCESS TIME
VS. LOAD CAPACITANCE