Dansk Data Elektronik ApS

# ID-7016 A/D-Conversion Module for the ID-7000 Microprocessor System

December 1976.

Author: Ole Lading.

# ID-7016 ANALOG/DIGITAL CONVERSION MODULE

1. Introduction. This module is used for connection of analog input signals to the ID-7000 microprocessor system. A maximum of 8 differential analog inputs can be connected to the module. A 3 bit channel selector register determines which input to be selected . The gain of the individual channels can be set in the range from 1-20 times by means of 8 trimpots on the module. A sample/hold circuit keeps the analog signal to the A/D-converter stable during conversion. The monolithic A/D-converter on the module - available in 8-bit and 10-bit versions-has a 40 µsec conversion time (for 10 bit operation). Basic input levels (with unity gain in instrumentation amplifier) is 0 to 10V differential (unipolar operation) or ÷10V to +10V differential (bipolar operation).

The module must be supplied by +15V/÷15v analog supply voltages. An ID-7022 analog power-supply module plugged into the bus can be used.

Fig. 1 shows a blocked schematic of the module. Appendix 1 is a complete diagram of the module. Appendix 2 contains datasheets for the analog components on the board.

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2. Description. This section contains a description of the module from a programming point of wiev.

2.1 Addressing. The module uses to consecutive addresses of the possible 256 addresses for I/O-units. The address of the module is set by a 7 bit switchregister on the module. The two addresses are used as described in the following sections.

2.2 Data input. When reading from the even address of the module, the CPU transfers the 8 most significant bits of the converted data to the accumulator:

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| IN 2n | CD9 | CD8 | CD7 | CD6 | CD5 | CD4 | CD3 | CD2 |
| | 7 | 6 | 5 | 4 | 3 | 2 | I | 0 |

If an 8 bit converter is used, this data word contains all the converted data. When bipolar operation is used, the result is in modified 2's complement notation with CD9 as a complemented sign bit.

Navn: LD 7016 A/D-conversion mod. Blocked schematic

Dato: 31-10-75

Afd.: O. Lauritzen

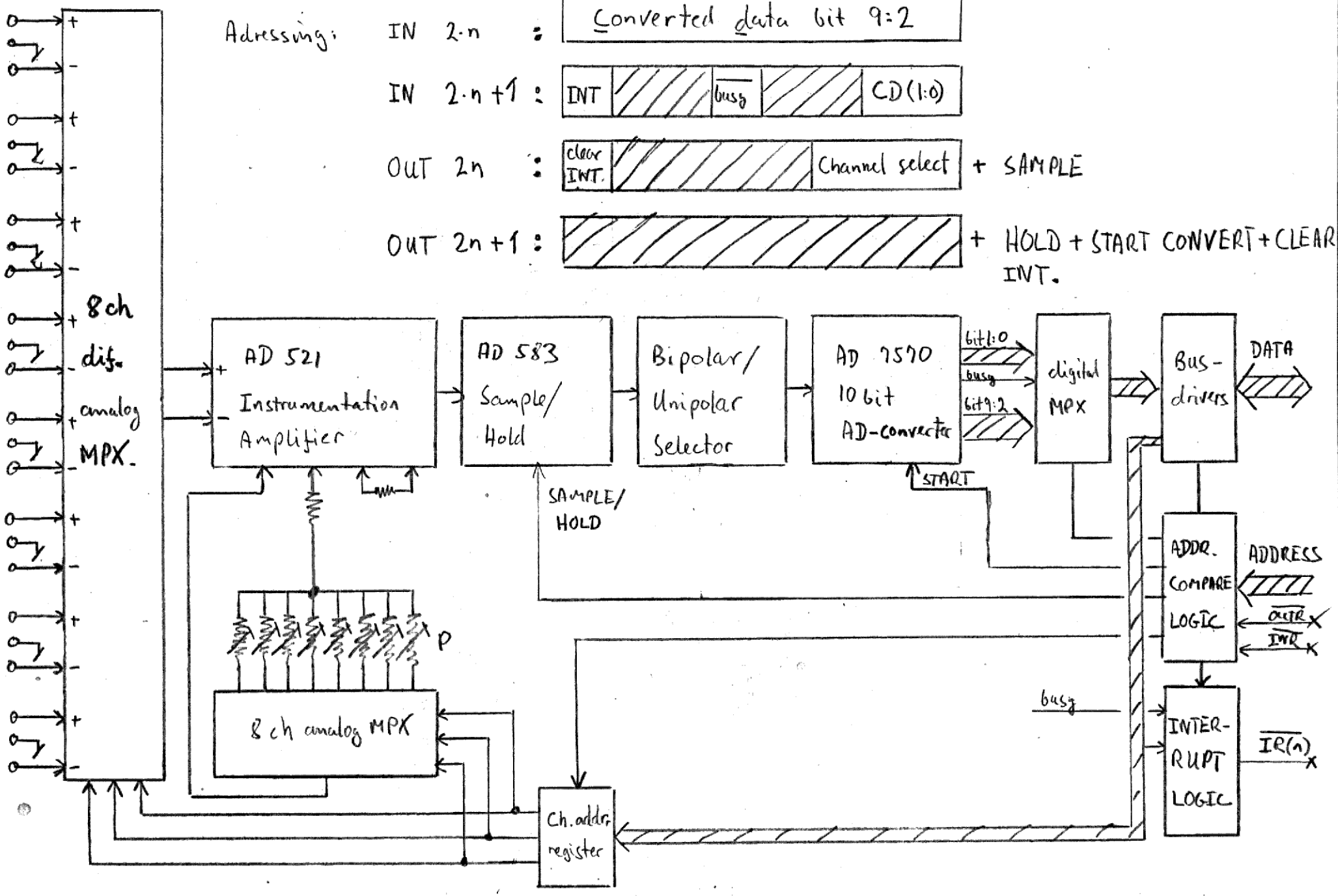
Adressing:

IN 2·n : Converted data bit 9:2

IN 2·n+1 : INT | busy | CD(1:0)

OUT 2n : clear INT. | Channel select + SAMPLE

OUT 2n+1 : + HOLD + START CONVERT + CLEAR INT.



2.2 Status input. When reading from the odd address of the module, the CPU transfers the 2 least significant bits of the converted data and some status information to the accumulator.

| IN 2n+1 | INT | 0 | 0 | READY | 0 | 0 | CD1 | CD0 |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

If an 8 bit converter is used, bit 0 and bit 1 in the status word are irrelevant.

bit 4: READY
0: the module is converting data, while the sample/hold circuit is in the HOLD state.
1: the module keeps converted data in the buffer, and the sample/hold circuit is in the SAMPLE state.

bit 7: INT
this bit in the status word is the interrupt flip-flop of the module. This bit can be used, when more than one interrupt source is connected to the same interrupt request line.

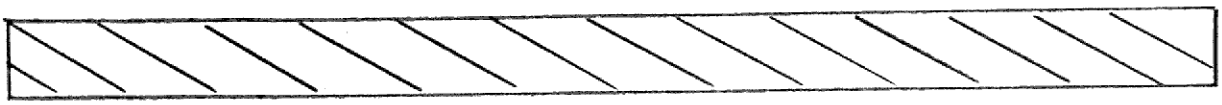
2.3 Data output. When writing to the even address of the module, the CPU loads the channel address register. One bit in the data word is used to clear the interrupt flip-flop of the module.

| OUT 2n | clear INT | | | | | CH(2) | CH(1) | CH(0) |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

bit 2-0: CH(2:0)
The channel address for the analog input multiplexor and the gain-selector multiplexor.

bit 7 clear INT
0: The content of the interrupt flip-flop is not affected.
1: The interrupt flip-flop is cleared. This can be used to passivate the module after a serie of conversions, to allow other interrupt sources to use the same interrupt request line.

2.4 Control output. When writng to the odd address of the module, the sample/hold circuit enters the HOLD state and an A/D conversion is started. This output instruction clears the interrupt flip-flop of the module. The output information is irrelevant:

OUT 2n+1 

2.5 Interrupt. The module contains one interrupt flip-flop. As described above, the interrupt flip-flop is cleared whwn a new conversion is started or a data word containing a logic 1 in bit 7 is send to the module. The interrupt flip-flop is set by the module, when an A/D-conversion is concluded and converted data are ready in the buffer.

By means of a strap on the module, the interrup request line (i.e. interrupt level) to be used by the module, is determined.

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3. Connections. This section describes the pin connections in the top edge connector of the module.

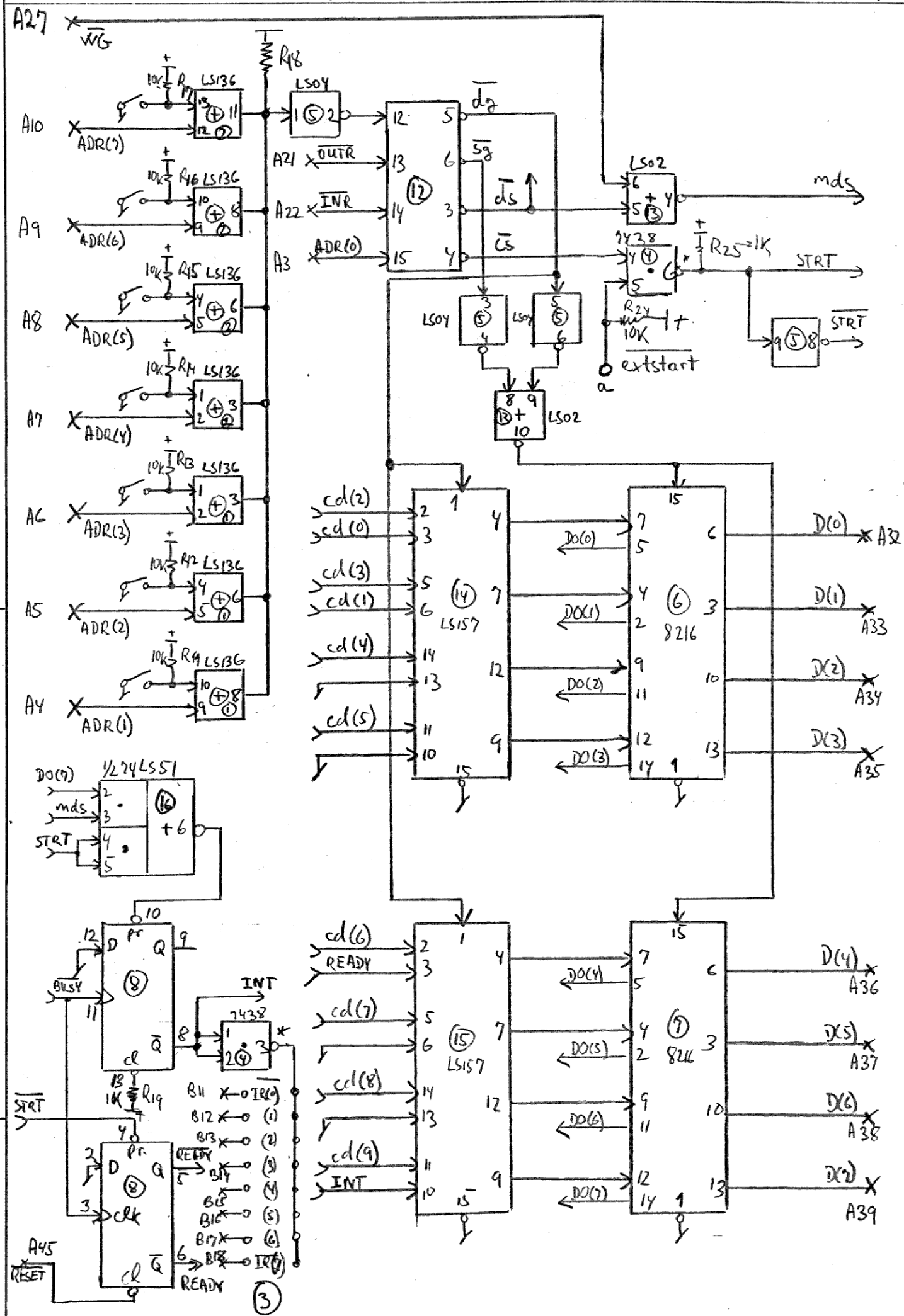
| | | |
|---|---|---|
| pin A | : | + 5 Volt supply. |
| pin 1 | : | digital gnd. |
| pin B | : | channel 0 positive input. |
| pin C | : | channel 0 negative input. |
| pin D | : | channel 1 positive input. |
| pin E | : | channel 1 negative input. |
| pin F | : | channel 2 positive input. |
| pin H | : | channel 2 negative input. |
| pin J | : | channel 3 positive input. |
| pin K | : | channel 3 negative input. |
| pin L | : | channel 4 positive input. |
| pin M | : | channel 4 negative input. |
| pin N | : | channel 5 positive input. |
| pin P | : | channel 5 negative input. |
| pin R | : | channel 6 positive input. |
| pin S | : | channel 6 negative input. |

| | | | |
|---|---|---|---|
| pin T | : | channel 7 positive input. | |
| pin U | : | channel 7 negative input. | |
| pin 2-17 incl | : | analog gnd. | |
| | | | These pins can be used to supply |
| pin W | : | +15V | the module from an external power |
| pin X,20 | : | analog gnd | supply or to supply external equip- |
| pin Y | : | +15V | ment (transducers) when an ID-7022 analog power supply is used. |
| pin a | : | $\overline{\text{EXTSTART}}$ | This input can be used to make an external start of the A/D-conversion. |
| pin b | : | $\overline{\text{SRO}}$ | This line contains complemented serial data from the A/D-converter during conversion.The information must be strobed at the negative edges of the SYNC-line (pin c). |
| pin c | : | $\overline{\text{SYNC}}$ | Synchronization line for the serial data (pin b). |
| pin d | : | $\overline{\text{READY}}$ | This line goes high when A/D-conversion is in progress. |
| pin 1 | : | analog out | This pin contains the analog data to the A/D-converter. |
| pin ρ | : | +10V ref. | |
| pin r | : | digital gnd | |
| pin 36 | : | +5V supply. | |

Pin a,b,c,d, ℓ and ρ are primary used for test and adjustment purposes.

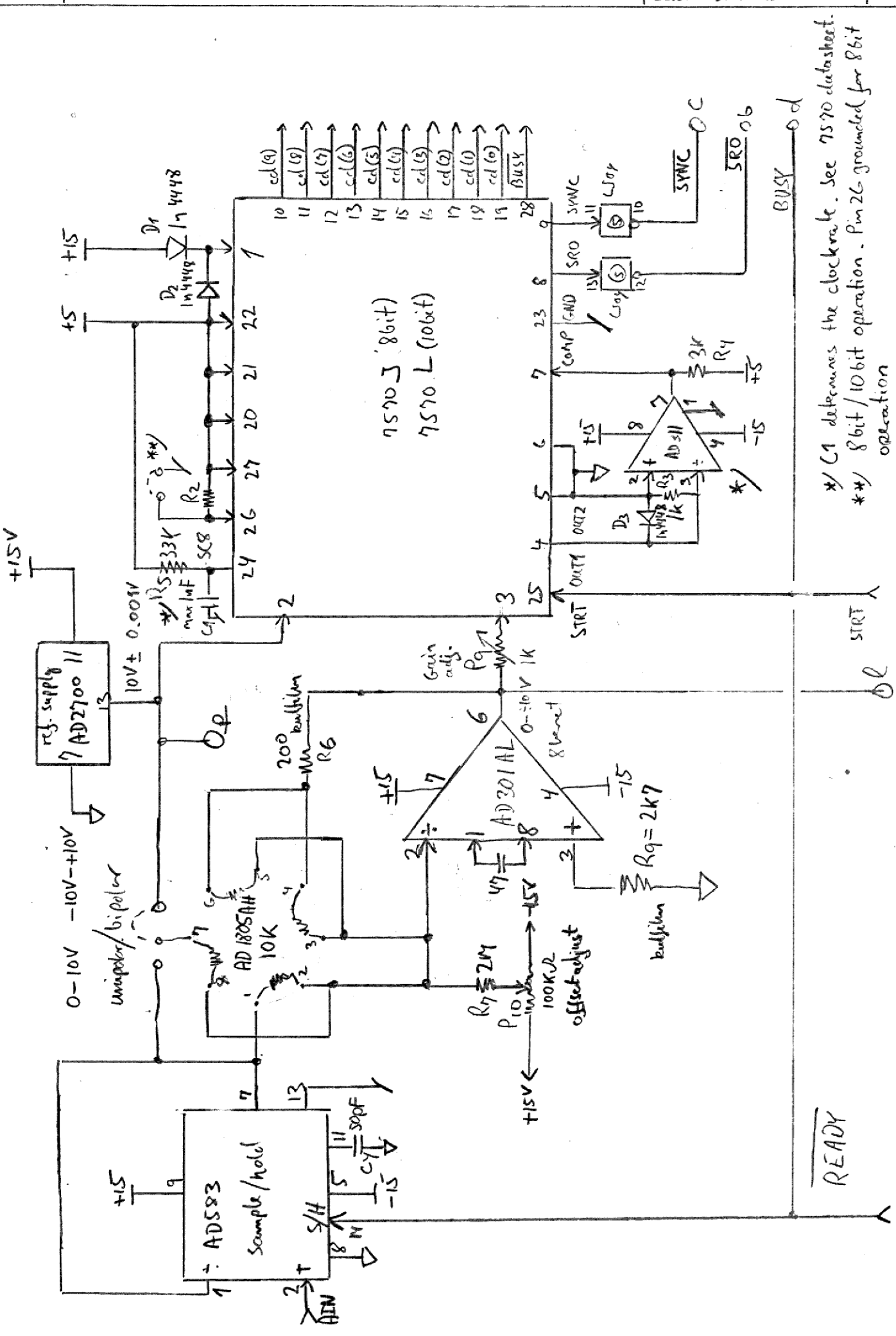
---

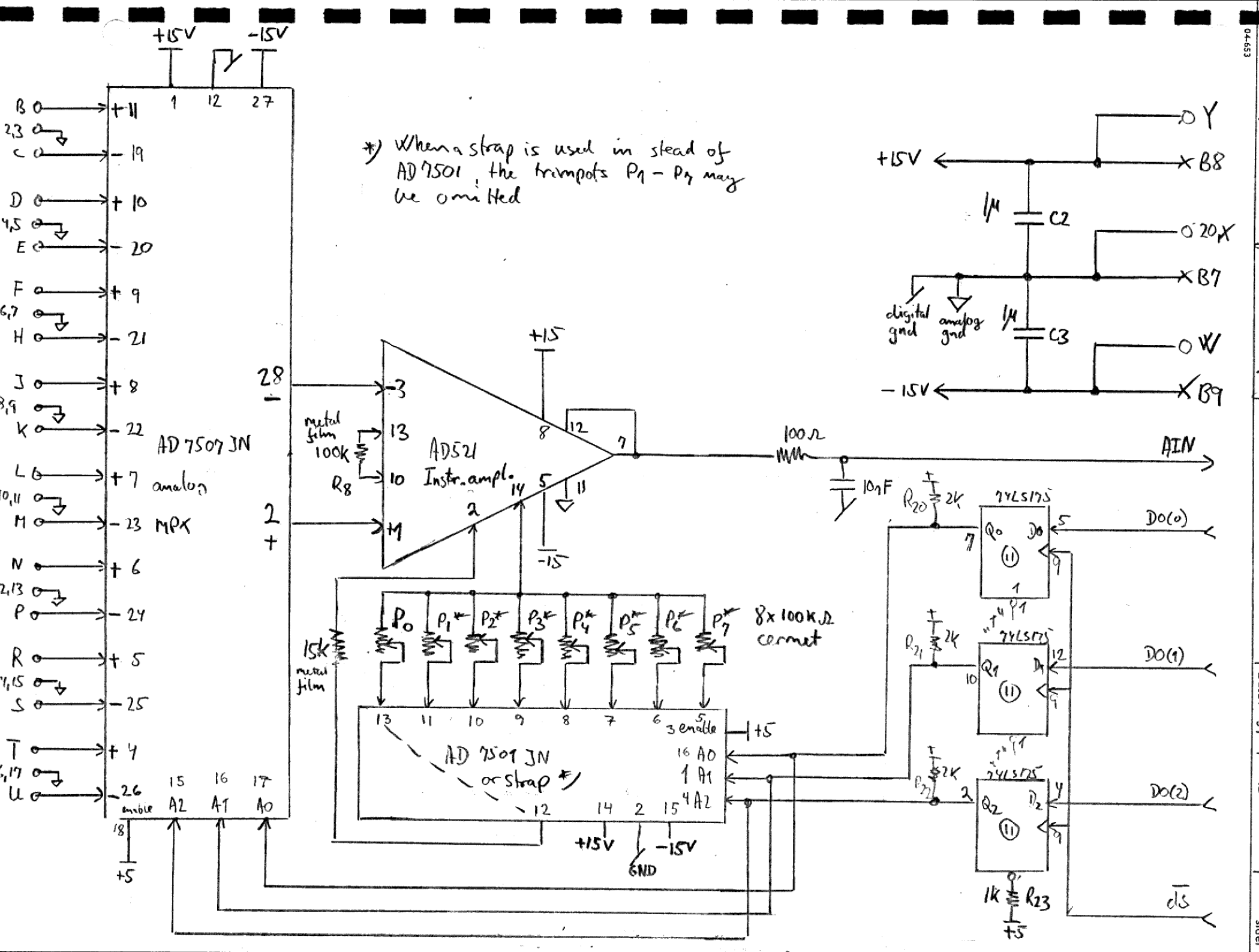
| Navn | Lb. nr. | Dato | Emne | Fag | Afd. | Side |
|---|---|---|---|---|---|---|
| ID 7016 A/D-conversion module | | 31-10-75 | | A1.1 | O. Lading | 1 |



| Emne: ID 7016 A/D-conversion module | Dok. nr.: | Side A1.2 |
|---|---|---|
| | Navn: Ole Ladegaard | ud af |
| | Dato: 31-10-75 | sider |

04-653




+15V
-15V
AD 7507 JN
analog MPX
*) When a strap is used in stead of AD 7501, the trimpots P1 – P7 may be omitted
AD521 Instr.ampl.
metal film 100k
R8
100Ω
AIN
10nF
15k metal film
P0 P1* P2* P3* P4* P5* P6* P7*
8x 100kΩ cermet
AD 7501 JN or strap *)
enable
A2 A1 A0
+5
GND
C2
C3
digital gnd
analog gnd
74LS175
R20 2K
R21 2K
R22 2K
R23 1k
DO(0)
DO(1)
DO(2)
ds
Y
B8
20X
B7
W
B9
Emne: ID 7016 A/D-conversion module
Analog MPX + amplifier
Dok. nr.:
Navn: Ole Ladin
Dato: 3/-10-23
Side A1.3
ud af
sider

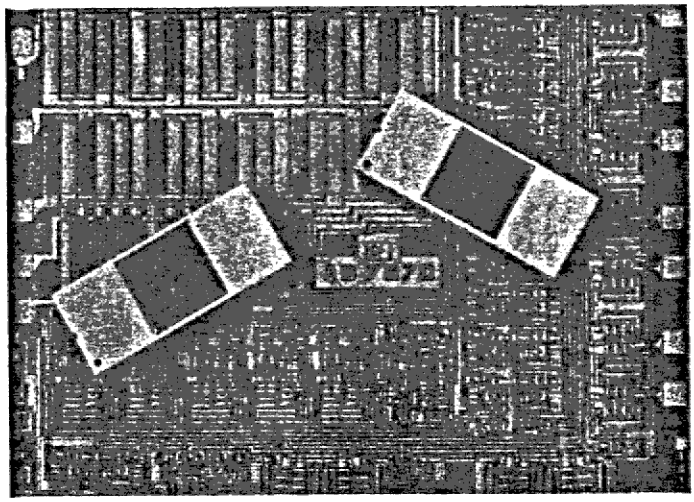
ANALOG DEVICES

# CMOS 10-Bit Monolithic A/D Converter

# AD7570

## FEATURES

- 8 and 10-Bit Resolution
- 20μsec Conversion Time
- Microprocessor Compatibility
- Very Low Power Dissipation
- Parallel and Serial Outputs
- Ratiometric Operation
- TTL/DTL/CMOS Logic Compatibility
- CMOS Monolithic Construction



## GENERAL DESCRIPTION

The AD7570 is a monolithic CMOS 10-bit successive approximation A/D converter on a 120 by 135 mil chip, requiring only an external comparator, reference and passive clocking components. Ratiometric operation is inherent, since an extremely accurate multiplying DAC is used in the feedback loop.

The AD7570 parallel output data lines and Busy line utilize three-state logic to permit bussing with other A/D output and control lines or with other I/O interface circuitry. Two enables are available, one controls the two MSB's, the second controls the remaining 8 LSB's. This feature provides the control interface for most microprocessors which can accept only an 8-bit byte.

The AD7570 also provides a serial data output line to be used in conjunction with the serial synchronization line. The clock can be driven externally or, with the addition of a resistor and a capacitor, can run internally as high as 0.6 MHz allowing a total conversion time (8-bits) of typically 20μsec. An 8-bit short cycle control pin stops the clock after exercising 8 bits, normally used for the "J" version (8-bit resolution).

The AD7570 requires two power supplies, a +15V main supply and a +5V (for TTL/DTL logic) to +15V (for CMOS logic) supply for digital circuitry. Both analog and digital grounds are available.

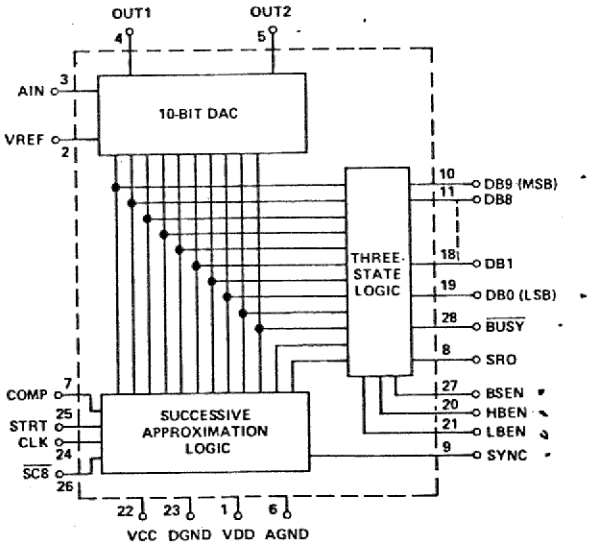
The AD7570 is a monolithic device using a proprietary CMOS process featuring a double layer metal interconnect, on-chip thin-film resistor network and silicon nitride passivation ensuring high reliability and excellent long term stability.

## ORDERING INFORMATION

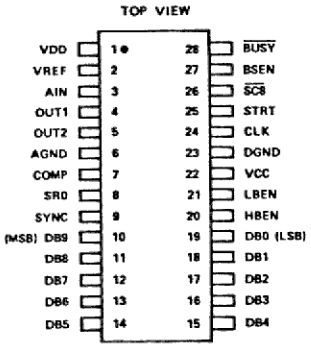
| Resolution | Temperature Range |
|---|---|
| | 0 to +75°C |
| 8-Bit | AD7570J |
| 10-Bit | AD7570L |

Suffix D: Ceramic Package

## FUNCTIONAL DIAGRAM




## PIN CONFIGURATION






Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: (617) 329-4700 Telex: 924491
Cable: ANALOG NORWOODMASS

# SPECIFICATIONS (VDD = +15V, VCC = +5V, VREF = ±10V unless otherwise noted)

| PARAMETER[1] | VERSION | TA = +25°C | | | OVER SPECIFIED TEMP. RANGE | | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | MAX | | |
| **ACCURACY** | | | | | | | | |
| Resolution | J | 8 | | | 8 | | Bits | $\overline{SC8}$ = Logic 0 |
| | L | 10 | | | 10 | | Bits | $\overline{SC8}$ = Logic 1 |
| Quantization Uncertainty | J, L | | | ±1/2 | | ±1/2 | LSB | |
| Relative Accuracy | J, L | | | ±1/2 | | ±1/2 | LSB | FCLK = 100 kHz |
| Differential Nonlinearity | J, L | | | ±1/2 | | ±1/2 | LSB | See Figure 5 on Page 4 |
| Gain Error | J, L | | 0.3 | | | | % Reading | |
| Gain Temperature Coefficient | J, L | | 5 | | | 10 | ppm Reading per °C | |
| **ANALOG INPUTS** | | | | | | | | |
| Analog Input Resistance | J, L | - | 10 | | 5 | 20 | kΩ | |
| Analog Input Resistance Tempco | J, L | | −150 | | | | ppm/°C | |
| Reference Input Resistance | J, L | | 10 | | 5 | 20 | kΩ | |
| Reference Input Resistance Tempco | J, L | | −150 | | | | ppm/°C | |
| **ANALOG OUTPUTS** | | | | | | | | |
| Output Leakage Current (IOUT1, IOUT2) | J, L | | 10 | | | 200 | nA | VOUT1, 2 = 0V |
| Output Capacitance COUT1 | J, L | | 120 | | | | pF | DB0 through DB9 = Logic 1 |
| COUT2 | J, L | | 40 | | | | pF | |
| COUT1 | J, L | | 40 | | | | pF | DB0 through DB9 = Logic "0" |
| COUT2 | J, L | | 120 | | | | pF | |
| **DIGITAL INPUTS** | | | | | | | | |
| VINL[2] | J, L | | +1.4 | +0.8 | | +0.8 | V | VCC = +5V |
| VINH[2] | J, L | +2.4 | +1.4 | | +2.4 | | V | |
| VINL[2] | J, L | | | +1.5 | | +1.5 | V | VCC = +15V |
| VINH[2] | J, L | +13.5 | | | +13.5 | | V | |
| IINL, IINH[3] | J, L | | ±0.1 | ±10 | | | μA | VIN = 0 to VCC |
| CLK Input Current | J, L | | +0.4 | +1 | | | mA | During Conversion VCC = +5V; 2.4V ≤ VIN ≤ VCC |
| CLK Input Current | J, L | | +1.7 | +3 | | | mA | During Conversion VCC = +15V; 10V ≤ VIN ≤ VCC |
| CLK Input Current | J, L | | ±1 | | | | μA | VCC = +5V to +15V Conversion Complete or CLK IN ≤ VINL |
| CIN | J, L | | 2 | | | | pF | |
| **DIGITAL OUTPUTS** | | | | | | | | |
| VOUTL | J, L | | | +0.5 | | +0.8 | V | VCC = +5V, ISINK = 1.6 mA |
| VOUTH | J, L | +2.4 | | | +2.4 | | V | VCC = +5V, ISOURCE = 40μA |
| VOUTL | J, L | | | +1.5 | | +1.5 | V | VCC = +15V, ISINK = 3 mA |
| VOUTH | J, L | +13.5 | | | +13.5 | | V | VCC= +15V, ISOURCE = 1 mA |
| COUT (Floating) (SYNC, SRO, $\overline{BUSY}$, and DB0 through DB9) | J, L | | 5 | | | | pF | VCC = +5V to +15V SRO and SYNC; Conversion Complete $\overline{BUSY}$; BSEN = Logic "0" DB0–DB9; HBEN, LBEN = Logic "0" |
| ILKG (Floating) (SYNC, SRO, $\overline{BUSY}$ and DB0 through DB9) | | | ±5 | | | | nA | VCC = +5V to +15V SRO and SYNC; Conversion Complete $\overline{BUSY}$; BSEN = Logic "0" DB0–DB9; HBEN, LBEN = Logic "0" VOUT = 0V and VCC |

# SPECIFICATIONS (continued)

| PARAMETER[1] | VERSION | TA = +25°C | | | OVER SPECIFIED TEMP. RANGE | | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | MAX | | |
| DYNAMIC PERFORMANCE | | | | | | | | |
| Conversion Time | J | | 20 | 40 | | 40 | µs | See Figure 5 on Page 4 |
| | L | | 40 | 120 | | 120 | µs | |
| Internal CLK Frequency | J, L | | 100 | | | | kHz | VCC = +5V; CLK Duty Cycle = 50%, R = 33k, C = 760 pF |
| (See Figure 2, Page 4 and Section 6, Page 5) | J, L | | 100 | | | | kHz | VCC = +15V, CLK Duty Cycle = 50%, R = 10k; C = 2500 pF |
| LBEN, HBEN Propagation Delay | | | | | | | | VCC = +5V |
| tON(EN) | J, L | | 650 | | | | ns | LBEN, HBEN = 0V to +3V |
| tOFF(EN) | J, L | | 200 | | | | ns | Data Bit Load = 5k, 16 pF<br>Measured from 50% of Enable Input to 50% Point of Data Bit Output |
| BSEN Propagation Delay | | | | | | | | VCC = +5V |
| tON(BSEN) | J, L | | 450 | | | | ns | BSEN = 0V to +3V |
| tOFF(BSEN) | J, L | | 200 | | | | ns | $\overline{BUSY}$ Loud = 5k, 16 pF<br>Measured from 50% Point of BSEN Input Waveform to 50% Point of $\overline{BUSY}$ Output Waveform |
| Convert Start (STRT)[4] Pulse Duration Requirement | J, L | 0.5 | | | | | µs | |
| POWER SUPPLIES | | | | | | | | |
| VDD | J, L | | +5 to +15 | | | | V | See Figures 3 and 4, Page 4 |
| VCC | J, L | | +5 to VDD | | | | V | |
| IDD | J, L | | 0.2 | 2 | | | mA | VDD = +15V, fCLK = 0 to 100 kHz Continuous Conversion (80% Duty Cycle) |
| ICC | J, L | | 0.02 | 2 | | | mA | VCC = +5V, fCLK = 0 to 100 kHz Continuous Conversion (80% Duty Cycle) |
| | J, L | | 0.1 | 2 | | | mA | VCC = +15V; fCLK = 0 to 100 kHz Continuous Conversion (80% Duty Cycle) |

Specifications subject to change without notice.
[1] "J" version parameters specified for $\overline{SC8}$ = 0.
[2] VINL and VINH specifications applicable to all digital inputs except COMP. COMP terminal must be driven with CMOS levels (i.e., comparator output pullup must be tied to VCC).
[3] IINL, IINH specifications not applicable to CLK terminal. See "CLK input current" in specification table.
[4] STRT falling edge should not coincide with CLK in falling edge.

## ABSOLUTE MAXIMUM RATINGS

VDD to GND . . . . . +17V
VCC to GND . . . . . +17V
VCC to VDD . . . . . +0.4V
VREF to GND . . . . . ±25V
Analog Input to GND . . . . . ±25V
Digital Input Voltage Range . . . . . VDD to GND

$I_{OUT1}$, $I_{OUT2}$ . . . . . ±5 mA
Power Dissipation (package)
up to +50°C . . . . . 1000 mW
Derate above +50°C by . . . . . 10 mW/°C
Operating Temperature . . . . . 0°C to +75°C
Storage Temperature . . . . . −65°C to +150°C

*CAUTION:*

1. Do not apply voltages higher than VCC or less than GND to any input/output terminal except VREF or AIN.
2. The digital control inputs are zener protected, however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
3. VCC should never exceed VDD by more than 0.4V, especially during power ON or OFF sequencing.

# Typical Performance Characteristics

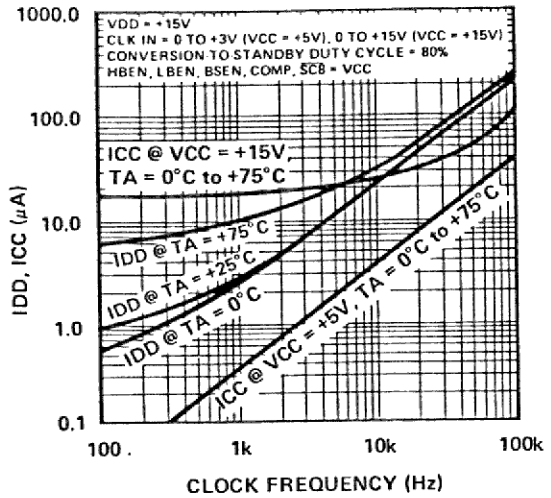



*Figure 1. IDD, ICC vs. fCLK at Different Temperatures*

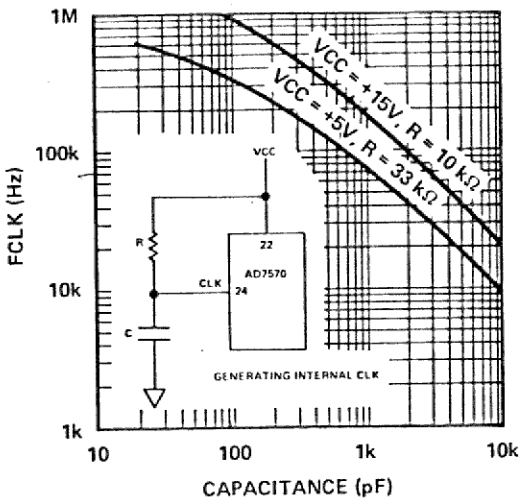



*Figure 2. fCLK vs. R and C at VCC = +5V, +15V*

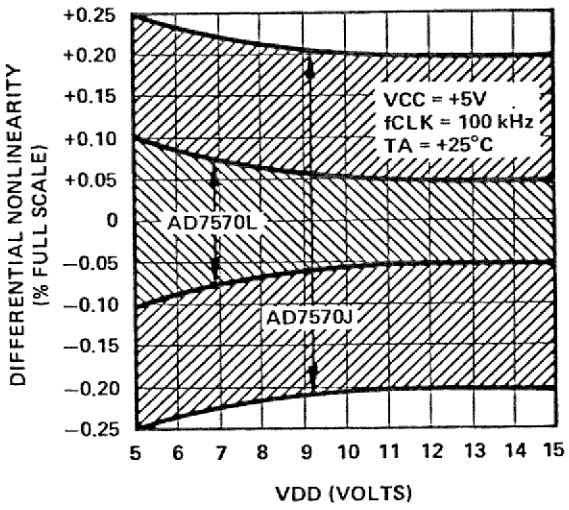



*Figure 3. Differential Nonlinearity vs. VDD*

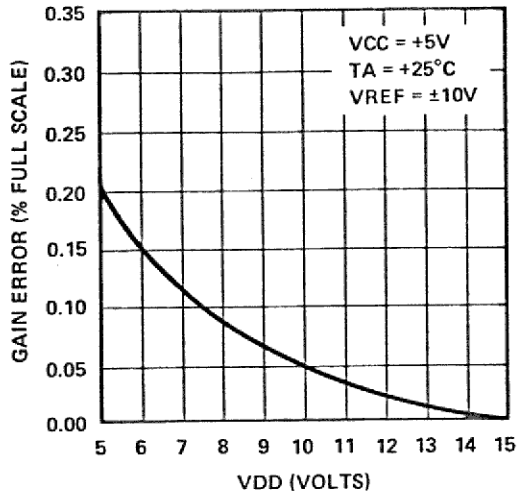



*Figure 4. Gain Error vs. VDD (Normalized for VDD = 15V)*

# Test Circuits

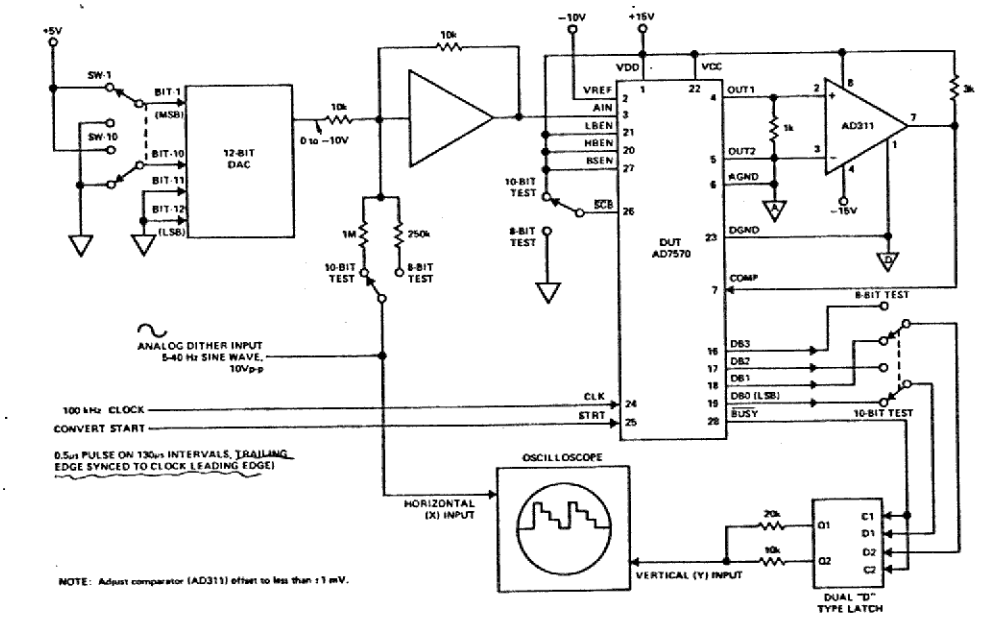
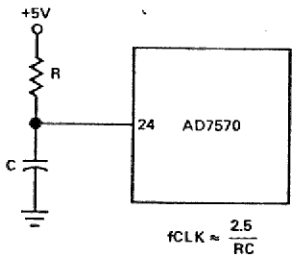



*Figure 5. Dynamic Crossplot Accuracy Test*

# Pin Function Description

## INPUT CONTROLS

1. Convert Start (pin 25 – STRT)
   When the start input goes to logical 1, the MSB data latch is set to logic 1 and all other data latches are set to logic 0. When the start input returns low, the conversion sequence begins. The start command must remain high for at least 500 nanoseconds. If a start command is reinitiated *during* conversion, the conversion sequence starts over.
2. High Byte Enable (pin 20 – HBEN)
   This is a three-state enable for the bit-9 (MSB) and bit 8. When the control is low, the output data lines for bits 9 and 8 are floating. When the control is high, digital data from the latches appears on the data lines.
3. Low Byte Enable (pin 21 – LBEN)
   Same as High Byte Enable pin, but controls bits 0 (LSB) through 7.
4. Busy Enable (pin 27 – BSEN)
   This is an interrogation input which requests the status of the converter, i.e., conversion in process or convert complete. The converter status is addressed by applying a logic 1 to the Busy Enable. (See Busy under Output Functions.)
5. Short Cycle 8-Bits (pin 26 – $\overline{SC8}$)
   With a logic 0 input, the conversion stops after 8 bits reducing the conversion time by 2 clock periods. This control should be exercised for proper operation of the "J" version. When a logic 1 is applied, a complete 10-bit conversion takes place ("L" version).
6. Clock(pin 24 – CLK)
   With an external RC connected, as shown in the Figure below, clock activity begins upon receipt of a Convert-Start command to the A/D, and ceases upon completion of conversion. An external clock (CMOS or TTL/DTL levels) can directly drive the clock terminals, if required.




*Generating Internal Clock Frequency*

The clock frequency vs. R and C is given in Figure 2.

7. VDD (pin 1)
   VDD is the positive supply for all analog circuitry plus some digital logic circuits that are not part of the TTL compatible input/output lines (back-gates to the P-channel devices). Nominal supply voltage is +15V.
8. VCC (pin 22)
   VCC is the logic power supply. If +5V is used, all control inputs/outputs (with the exception of comparator terminal) are DTL/TTL compatible. If +15V is applied, control inputs/outputs are CMOS compatible.

## OUTPUT FUNCTIONS

1. Busy (pin 28 – $\overline{BUSY}$)
   The Busy line indicates whether conversion is complete or in process. Busy is a three-state output and floats until the Busy-Enable line is addressed with a logic 1. When addressed, Busy will indicate either a 1 (conversion complete) or a 0 (conversion in process).
2. Serial Output (pin 8 – SRO)
   Provides output data in serial format. Data is available only during conversion. When the A/D is not converting, the Serial Output line "floats." The Serial Sync (see next function) *must* be used, along with the Serial Output terminal to avoid misinterpreting data.
3. Serial Synchronization (pin 9 – SYNC)
   Provides 10 positive edges, which are synchronized to the Serial Output pin. Serial Sync is floating if conversion is not taking place.

Note that all digital inputs/outputs are TTL/DTL compatible when VCC is +5V, and CMOS compatible when VCC is +15V.

*Table 1. Function Table*

| PIN NO. | MNEMONIC | FUNCTION |
|---|---|---|
| 1 | VDD | Positive Supply (+15V) |
| 2 | VREF | Voltage REFerence (±10V) |
| 3 | AIN | Analog INput |
| 4 | OUT1 | DAC Current OUTput 1 |
| 5 | OUT2 | DAC Current OUTput 2 |
| 6 | AGND | Analog GrouND |
| 7 | COMP | COMParator |
| 8 | SRO | SeRial Output |
| 9 | SYNC | Serial SYNChronization |
| 10 | DB9 | Data Bit 9 (MSB) |
| 11 | DB8 | Data Bit 8 |
| 12 | DB7 | Data Bit 7 |
| 13 | DB6 | Data Bit 6 |
| 14 | DB5 | Data Bit 5 |
| 15 | DB4 | Data Bit 4 |
| 16 | DB3 | Data Bit 3 |
| 17 | DB2 | Data Bit 2 |
| 18 | DB1 | Data Bit 1 |
| 19 | DB0 | Data Bit 0 (LSB) |
| 20 | HBEN | High Byte ENable |
| 21 | LBEN | Low Byte ENable |
| 22 | VCC | Logic Supply (+5V to +15V) |
| 23 | DGND | Digital GrouND |
| 24 | CLK | CLocK |
| 25 | STRT | STaRT |
| 26 | $\overline{SC8}$ | Short Cycle 8 Bits |
| 27 | BSEN | BuSy ENable |
| 28 | $\overline{BUSY}$ | BUSY |

# Functional Analysis

## BASIC DESCRIPTION

The AD7570 is a monolithic CMOS A/D converter which uses the successive approximations technique to provide up to 10 bits of digital data in a serial and parallel format. Most A/D applications require the addition of only a comparator and a voltage or current reference.

In the successive approximations technique, successive bits, starting with the most significant bit (DB9) are applied to the input of the D/A converter. The DAC output is then compared to the unknown analog input voltage (AIN) using a zero crossing detector (comparator). If the DAC output is greater than AIN, the data latch for the trial bit is reset to zero, and the next smaller data bit is tried. If the DAC output is less than AIN, the trial data bit stays in the "1" state, and the next smaller data bit is tried.

Each successive bit is tried, compared to AIN, and set or reset in this manner until the least significant bit (DB0) decision is made. At this time, the AD7570 output is a valid digital representation of the analog input, and will remain in the data latches until another convert start (STRT) is applied.

## TIMING DESCRIPTION

Figure 6 is the AD7570 timing diagram, showing the successive trials and decisions for each data bit. When convert start (STRT) goes HIGH, the MSB(DB9) is set to the logic "1" state, while DB0 through DB8 are reset to the "0" state.

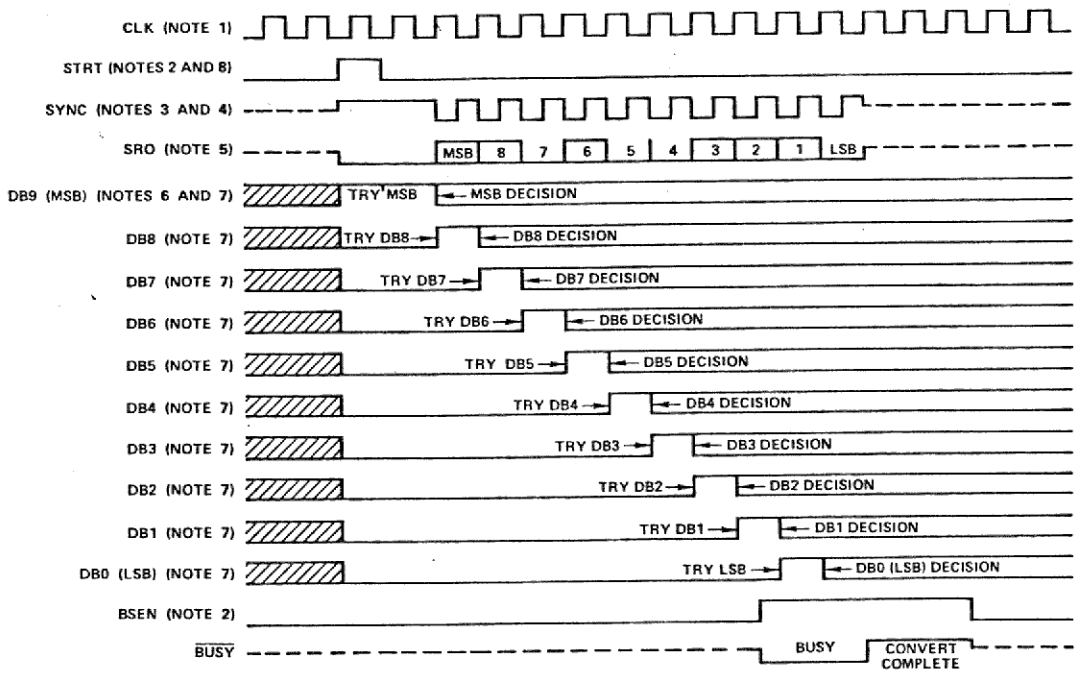
Two clock *pulses* plus 200 ns after STRT returns LOW, the MSB decision is made, and DB8 is tried. Each succeeding trial and decision is made at tCLK + 200 ns.

Serial NRZ data is available during conversion at the SRO terminal. SYNC provides 10 positive edges which occur in the middle of each serial output bit. SYNC out must be used in conjunction with SRO to avoid misinterpretation of data. Both SYNC and SRO "float" when conversion is not taking place.

## 8-BIT SHORT CYCLE NOTES

If the AD7570 is short cycled to 8 bits ($\overline{SC8}$ = 0V), the following will occur:

1. The SYNC terminal will provide 8, instead of 10, positive output pulses.
2. DB1 goes "high" coincident with the LSB (DB2 is the LSB when short cycled to 8 bits) decision, and remains high until another STRT is initiated. DB0 remains in the "0" state.
3. $\overline{BUSY}$ goes "high" one clock period after the DB2 (DB2 is the LSB when short cycled) decision is made.




NOTES:
1. Internal Clock Runs Only During Conversion Cycle (External Clock Shown).
2. Externally Initiated.
3. Serial Sync Lags Clock by ≈ 200 ns.
4. Dotted Lines Indicate "Floating" State.
5. For Illustrative Purposes, Serial Out Shown as 1101001110.
6. Cross Hatching Indicates "Don't Care" State.
7. Set and Reset of Output Data Bits Lags Clock Positive Edge by ≈ 200 ns.
8. Trailing edge of STRT Should be Externally Synchronized to Leading Edge of CLK.
9. Shown for $\overline{SC8}$ = 1.

*Figure 6. AD7570 Conversion Timing Sequence*

## DYNAMIC PERFORMANCE

The upper clock frequency limitation (hence the conversion speed limitation) of the AD7570 is due to the output settling characteristics of the current weighting DAC in conjunction with the propagation delay of the comparator, not to speed limitations in the digital logic.

## DAC EQUIVALENT CIRCUIT

The D/A converter section of the AD7570 is a precision 10-bit multiplying DAC. The simplified DAC circuit, shown in Figure 7, consists of ten single-pole-double-throw current steering switches and an "inverted" R-2R current weighting network. (For a complete description of the DAC, refer to the AD7520 data sheet.)

The output resistance and capacitance at OUT1 (and OUT2) are code dependent, exhibiting resistive variations from 0.5 "R" to 0.75 "R," and capacitive variations from 40 pF to 120 pF.

## SETTLING TIME ANALYSIS

Due to the changing COUT1 and ROUT1, the time constant on OUT1 falls anywhere between 250 and 900 nanoseconds, depending on the instantaneous state of the AD7570 digital output code.

Worst case settling requirements occur when a trial bit causes the OUT1 terminal to charge towards a final value which is precisely 1/2 LSB beyond zero crossing. When this occurs, the trial bit must settle and remain within 1/2 LSB of final value, or an incorrect decision will be made by the comparator.

For 10-bit accuracy, the first MSB must settle to within 0.1% of final value; the second MSB to within 0.2%. The LSB settling requirement is only 50% of the LSB value. Figure 8 illustrates the settling time available during a given clock period. The pulse shown on the OUT1 terminal falling midway between t0 and t3 is a feedthrough from internal clock mechanisms, and is due primarily to bonding wire and header capacitance. Two methods may be used to reduce the OUT1 settling time:

1. Load OUT1 with a 1k resistor. This reduces the time constant by a factor of 10. Further reduction of the 1kohm load reduces the amount of comparator overdrive, thus increasing the comparator propagation delay, resulting in a reduction of available settling time (t1 - t0 on Figure 8).
2. Use a zero input impedance comparator. Figure 9 illustrates a comparator circuit which has an input impedance of approximately 26 ohms. Proper circuit layout will provide 10-bit accuracy for clock frequencies greater than 500 kHz.

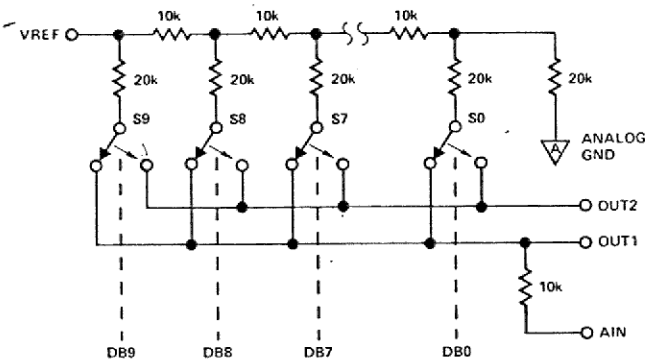
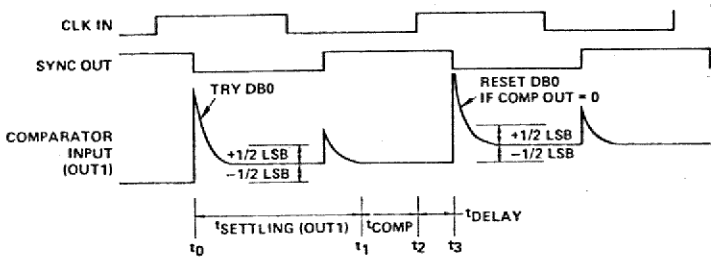



*Figure 7. DAC Circuit*




NOTES:
1. "tsettling" (t1 - t0) is the time required for the OUT1 terminal to settle within ± 1/2LSB of the final value.
2. "tcomp" (t2 - t1) is the comparator switching time.
3. "tdelay" (t3 - t2) is an internally generated time delay equal to approximately 400 nanoseconds.

*Figure 8. Expanded Timing Diagram*

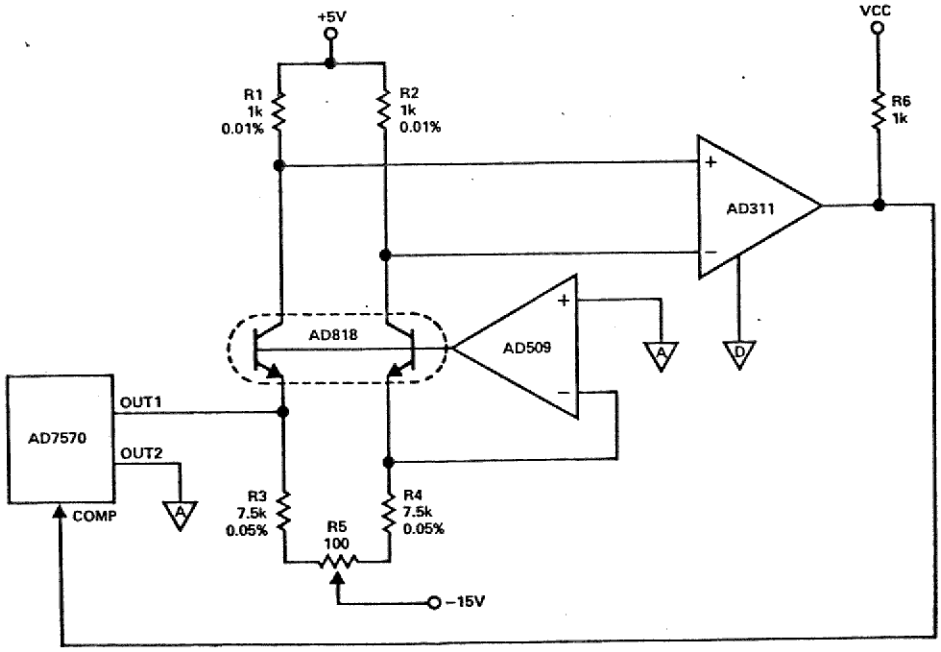



*Figure 9. Current Comparator With Low Input Impedance*

## UNIPOLAR BINARY OPERATION

Figure 10 shows the circuit connections required for unipolar analog inputs. If *positive* analog inputs are to be quantized, VREF must be *negative*, and the OUT1 (pin 4) terminal of the AD7570 must be connected to the "+" comparator input. For *negative* analog inputs, VREF must be *positive*, and the OUT1 terminal connected to the "−" input of the comparator.

For clarity, the digital control functions have been omitted from the diagram. For proper use of the digital input/output control functions, refer to the pin function descriptions on page 5.

The input voltage/output code relationship for unipolar operation is shown in Table 2. Due to the inherent multiplying capability of the internal D/A converter, the AD7570 can accurately quantize full scale ranges of 10V to 1V. It should be noted, however, that for smaller full scale ranges, the resolution and speed limitations of the comparator impose a limitation on the maximum conversion rate.

## BIPOLAR (OFFSET BINARY) OPERATION

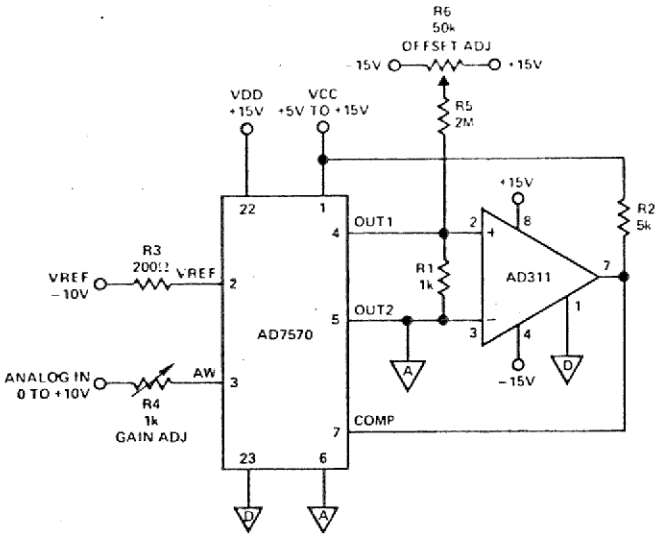
Figure 11 shows the AD7570 configured for offset binary (modified 2's complement) operation. Input voltage/output codes are shown in Table 3.

Amplifier A1, in conjunction with resistors R1, R2, and R3, offsets the bipolar analog input by full scale, and reduces its gain by a factor of 2. The analog signal applied to the AIN terminal is, therefore, a unipolar signal of 0 to +V or 0 to −V, depending on the polarity of VREF. Note that the offset (as well as the scale factor) changes if VREF drifts.

## ADJUSTMENT PROCEDURES UNIPOLAR OPERATION

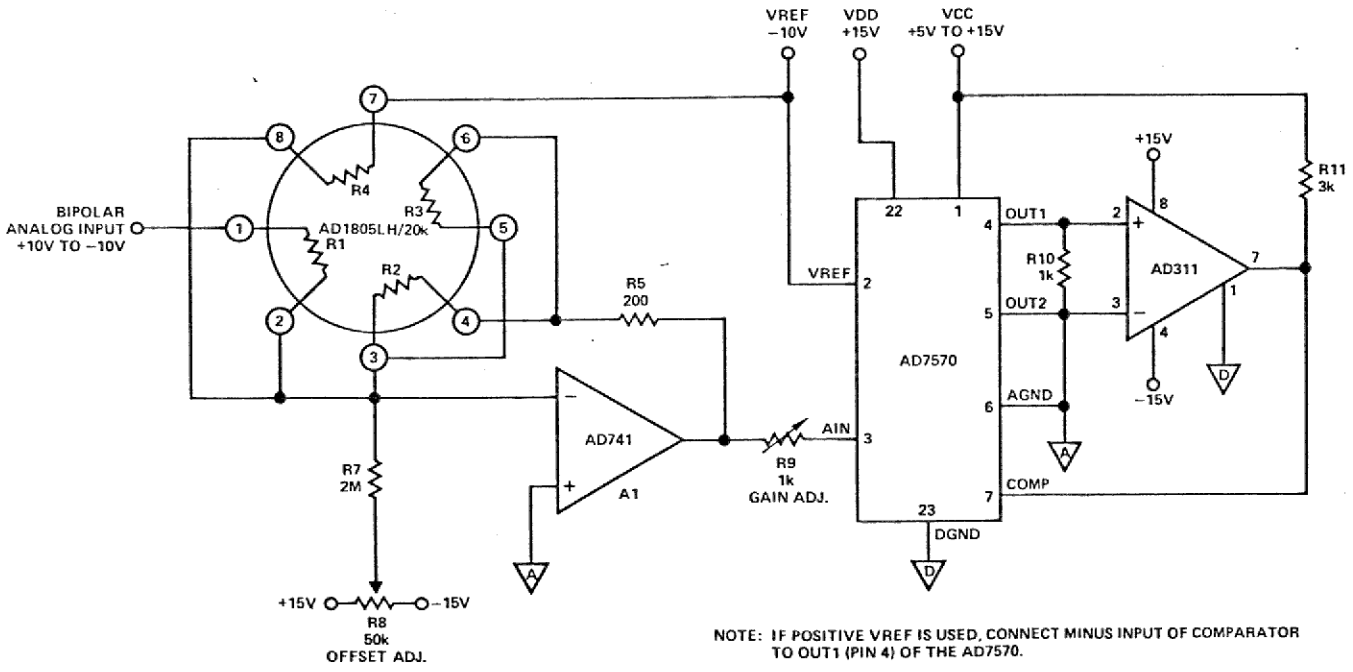
### Zero Offset Adjustment

1. Apply continuous STRT command to the AD7570 STRT input. *Note:* STRT must be at intervals long enough to allow a complete conversion.
2. Apply 0 + 1/2LSB (0 − 1/2LSB if positive VREF is used) to the AIN terminal.
3. Observe the SRO output line (synchronize oscilloscope to SYNC terminal of AD7570). Adjust the offset potentiometer (R6) until the LSB flickers between 0 and 1, and all other data bits are logic "0." (See Figure 6, timing diagram, for correlation of SRO and SYNC.)




NOTE:
IF POSITIVE VREF IS USED, THE ANALOG INPUT RANGE IS 0 TO −VREF, AND THE COMPARATOR'S (−) INPUT SHOULD BE CONNECTED TO OUT1 (PIN 4) OF THE AD7570.

*Figure 10. Unipolar Operation*




NOTE: IF POSITIVE VREF IS USED, CONNECT MINUS INPUT OF COMPARATOR TO OUT1 (PIN 4) OF THE AD7570.

*Figure 11. Bipolar Operation*

## Operation Guidelines cont'd

*Table 2. Unipolar Operation*

| ANALOG INPUT (AIN) NOTES 1, 2, 3 | DIGITAL OUTPUT CODE MSB LSB |
|---|---|
| FS – 1LSB | 1 1 1 1 1 1 1 1 1 1 |
| FS – 2LSB | 1 1 1 1 1 1 1 1 1 0 |
| 3/4 FS | 1 1 0 0 0 0 0 0 0 0 |
| 1/2 FS + 1LSB | 1 0 0 0 0 0 0 0 0 1 |
| 1/2 FS | 1 0 0 0 0 0 0 0 0 0 |
| 1/2 FS – 1LSB | 0 1 1 1 1 1 1 1 1 1 |
| 1/4 FS | 0 1 0 0 0 0 0 0 0 0 |
| 1LSB | 0 0 0 0 0 0 0 0 0 1 |
| 0 | 0 0 0 0 0 0 0 0 0 0 |

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale, i.e., (–VREF).
3. For 8-bit operation, 1LSB equals (–VREF) $(2^{-7})$; for 10-bit operation, 1LSB equals (–VREF) $(2^{-9})$.
4. Code relationship is shown for circuit of Figure 21. If circuit of Figure 22 is used, the output codes shown above will be complemented.

*Table 3. Bipolar Operation*

| ANALOG INPUT (AIN) NOTES 1, 2, 3 | DIGITAL OUTPUT CODE MSB LSB |
|---|---|
| +(FS – 1LSB) | 1 1 1 1 1 1 1 1 1 1 |
| +(FS – 2LSB) | 1 1 1 1 1 1 1 1 1 0 |
| +(1/2 FS) | 1 1 0 0 0 0 0 0 0 0 |
| +(1LSB) | 1 0 0 0 0 0 0 0 0 1 |
| 0 | 1 0 0 0 0 0 0 0 0 0 |
| –(1LSB) | 0 1 1 1 1 1 1 1 1 1 |
| –(1/2 FS) | 0 1 0 0 0 0 0 0 0 0 |
| –(FS – 1LSB) | 0 0 0 0 0 0 0 0 0 1 |
| –FS | 0 0 0 0 0 0 0 0 0 0 |

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale; i.e., (VREF).
3. For 8-bit operation, 1LSB equals (–VREF) $(2^{-8})$; for 10-bit operation, 1LSB equals (–VREF) $(2^{-10})$.

Gain Adjustment

1. Apply continuous start commands to the STRT input of the AD7570.
2. Apply full scale minus 1-1/2LSB to AIN.
3. Observe the SRO terminal as described under zero offset procedure above, and adjust the gain potentiometer (R4) until the LSB flickers between 0 and 1, and all other data bits equal "1." An alternate method is to adjust VREF instead of using R4.

### ADJUSTMENT PROCEDURES BIPOLAR OPERATION

Zero Offset Adjustment

1. Apply continuous start commands to the STRT input of the AD7570. *Note:* STRT must be at intervals long enough to allow a complete conversion.
2. Apply 1/2LSB less than negative full scale (–FS = –VREF) to the bipolar analog input shown in Figure 11.
3. Observe the SRO terminal (synchronize oscilloscope to the AD7570 SYNC terminal). Adjust the offset potentiometer (R8) until the LSB flickers between 1 and 0, and all other data bits are logic "0." (See timing diagram of Figure 6.)

Gain Adjustment

1. Apply continuous start commands to the STRT input of the AD7570.
2. Apply 1-1/2LSB less than positive full scale (FS = VREF) to the bipolar analog input of Figure 11.
3. Trim the gain potentiometer (R9) for a flickering LSB, and all other data bits equal to logic "1." Observe the SRO terminal, as described in zero offset procedure above.

### APPLICATION HINTS

1. Unused CMOS digital inputs should be tied to their appropriate logic level, and not left floating. Open digital inputs may cause undesired digital activity in the presence of noise.
2. Analog and digital grounds should have separate returns.
3. Load the OUT1 terminal with a 1k resistor to reduce the time constant when operating at clock frequencies greater than 50 kHz.
4. For 10-bit operation, the comparator offset should be adjusted to less than 1mV. Each millivolt of comparator offset will cause approximately 0.015% of differential nonlinearity when a 10V reference is used.
5. The comparator input and output should be isolated to prevent oscillations due to stray capacitance. (See layout on page 10.)
6. If an external clock is used, the negative transition of STRT should not coincide with the trailing edge of the clock input.

### OPERATING PRECAUTIONS

1. Do not allow VCC to exceed VDD. In cases where VCC could exceed VDD, the diode protection scheme in Figure 12 is recommended.
2. Do not apply voltages greater than VCC or lower than ground to any digital *output* from sources which can supply more than 20 mA.
3. Do not apply voltages (from a source which can supply more than 5 mA) lower than ground to the OUT1 or OUT2 terminal. (See Figure 12 Diode Protection Scheme.)

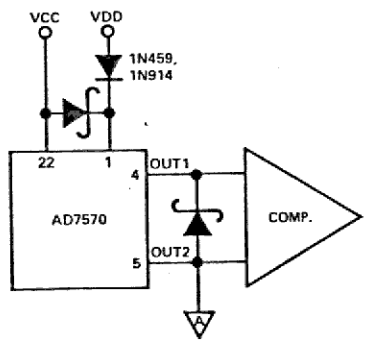



*Figure 12. Diode Protection Scheme*

A2.10

ANALOG DEVICES

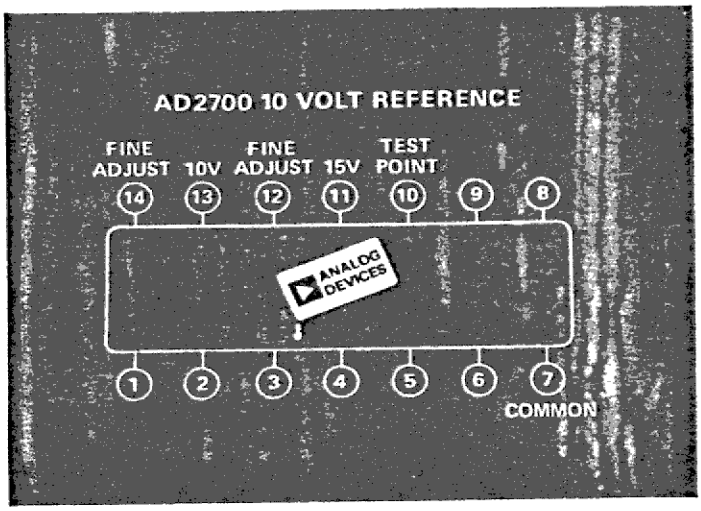
# 10.000 ± .001 Volt Precision Reference

# AD2700

PRELIMINARY TECHNICAL DATA

FEATURES

- 3-Terminal Device:
  - Voltage In/Voltage Out
- Total Output Error at
  - $T_{MAX}$ to: 2mV
- Excellent Long Term Stability:
  - To 50ppm/yr.
- Small IC Package: 14 Pin Dip
- 20mA Current Output Capability
- Available Screened to MIL-STD-883A
- Use with AD7520, AD7570, AD562
- Short Circuit Protected

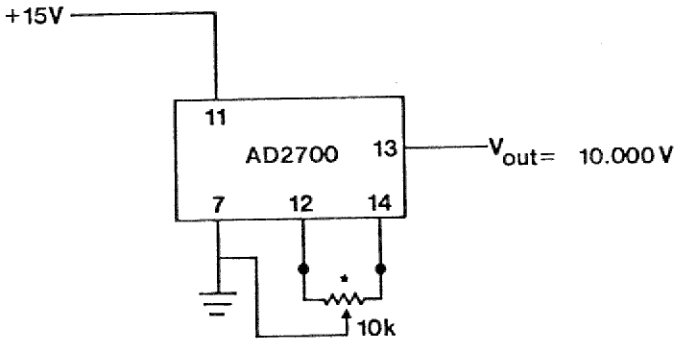



## PRODUCT DESCRIPTION

The AD2700 is a medium cost, high stability, temperature compensated voltage reference source. The reference output is accurately fixed at 10V. With excellent termperature stability and long term stability of 50ppm/year, the AD2700 offers a convenient solution to regulated voltage requirements which may previously have been met with bulky power supplies or elaborate diodes and ovens. This product is made possible by the combination of the best available semiconductor technology with high precision thin film resistors which are functionally trimmed.

The AD2700 is recommended for use in 10- or, 12-bit A/D, and D/A converter circuits and other precise analog circuits. Its small size and hermetic seal make it adaptable to essentially any application or environment.

The operation of the AD2700 is 3 terminal, voltage in/voltage out. No external components are required. Offset adjustment terminals are provided for optional use if accuracy of better than 1mV is desired.




*External 10k potentiometer provides ±30mV output offset adjust. Temperature effect is ±4μV/°C per mV of offset correction.

*(External Adjustment Optional)*



P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Telex: 924491 Cables: ANALOG NORWOODMASS

# SPECIFICATIONS

(typical at 25°C and $V_{in}$ = +15V unless otherwise specified)

ABSOLUTE MAX RATINGS

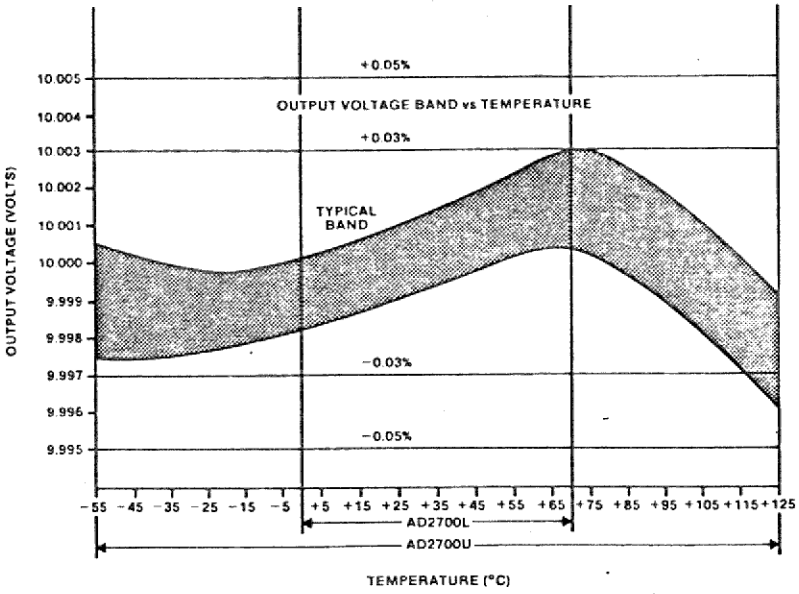
| | |
|---|---|
| Input Voltage | 20VDC |
| Power Dissipation @ +25°C | 400 mW |
| Derate Above 25°C | 1mW/°C |
| Storage Temperature Range | -65 to +150°C |
| Lead Temperature (soldering, 10 sec) | 250°C |
| Operating Temperature Range – AD2700/L | 0 to 70°C |
| – AD2700/U | -55 to +125°C |
| Short Circuit Protection | Continuous |

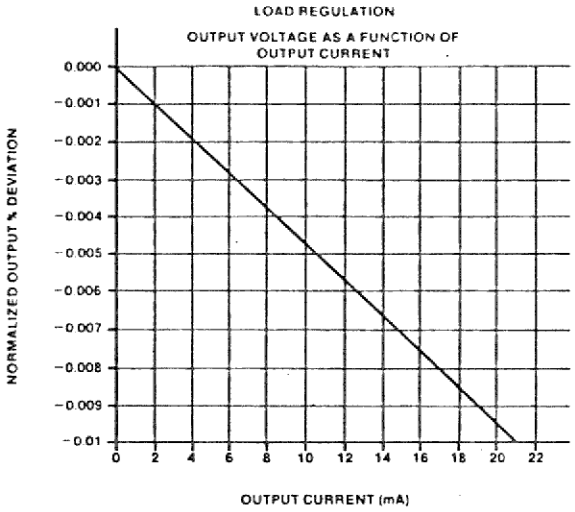
| ELECTRICAL CHARACTERISTICS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| Output Voltage @ 25°C, No Load | 9.999 | 10.000 | 10.001 | V |
| Output Current | | ±18 | ±20 | mA |
| Total Output Error Over Operating Temperature Range (see graph, page 4) | | | | |
| – AD2700L | | ±.02 | ±.03 | % |
| – AD2700U | | ±.03 | ±.05 | % |
| Input Regulation/Power Supply Rejection ($V_{in}$ = 12 to 18 V) | | .0003 | .0005 | %/% |
| Load Regulation 0 to ±10mA (see graph, page 4) | | | ±.005 | % |
| Input Voltage, Operating | 12 | 15 | 18 | V |
| Input Current, No Load | | | 12 | mA |
| *Noise (0.1 to 10Hz) | | | 50 | μVp.p |
| *Long Term Stability | | | 50 | ppm/yr |
| *Output Resistance | | | .1 | Ω |
| *Ripple Rejection | | | .01 | %/V |
| *Offset Adjust Range (see schematic, page 1) | | | ±30 | mV |
| *Offset Adjust Temperature Effect | | | ±4 | μV/°C per mV of adjust |

OPTION 883 (designated as AD2700/U/883) per MIL-STD-883A, Method 5004.2, Class B

| PRICES | AD2700/L | AD2700/U | AD2700/U/883 |
|---|---|---|---|
| 1-9 | | | |
| 10-24 | | | |
| 25-99 | | | |

*Guaranteed by design, not tested.

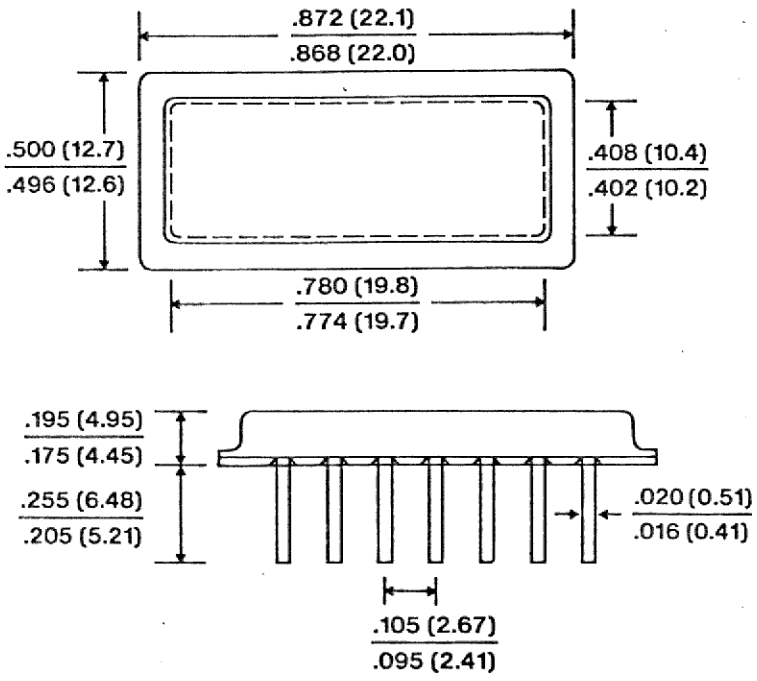


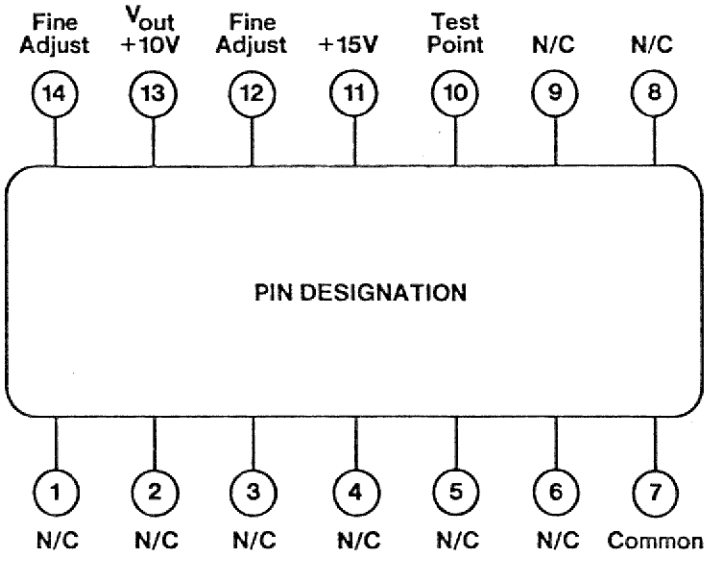

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

### 14-PIN DUAL-IN-LINE




### AD2700 10 VOLT REFERENCE



A2.13

ANALOG DEVICES

# High Accuracy Low Cost IC Operational Amplifier

## AD301AL

### FEATURES

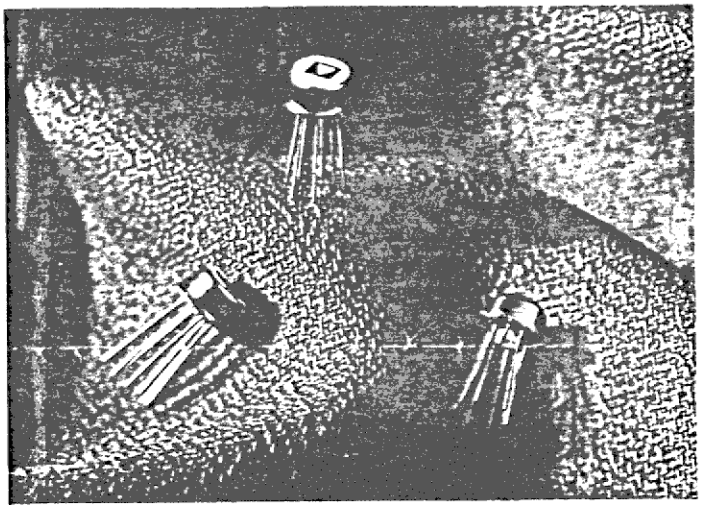
Precision Input Characteristics
- Low $V_{os}$: 0.5mV max
- Low $V_{os}$ Drift: 5μV/°C max
- Low $I_{os}$: 5nA max
- Low $I_b$: 30nA max
- High $A_{ol}$: 80,000 min

External Compensation Flexibility

Small Signal Bandwidth
- 1MHz to 10MHz

Full Power Response
- 6kHz to 100kHz

Slew Rate
- 0.25V/μsec to 9V/μsec



### GENERAL DESCRIPTION

The Analog Devices AD301AL is the highest accuracy version of the popular AD101A, AD201A, AD301A series of operational amplifiers. Improved processing and additional electrical testing allow the user to achieve precision performance at low cost. The AD301AL provides substantially increased accuracy by reducing the errors due to offset voltage (0.5mV max), offset voltage drift (5.0μV/°C max), bias current (30nA max), offset current (5nA max), voltage gain (80,000 min), PSRR (90dB min), and CMRR (90dB min).

In simple ac applications, the AD301AL is unity gain stable with a 30pF capacitor. In more complex situations, the user may tailor the frequency compensation to his particular application. For example, in low frequency applications, the devices may be over-compensated for increased stability margin. Likewise, the compensation can be optimized to give more than a factor of 10 improvement in high frequency performance.

All devices feature full short circuit protection, and are free of latch up when the common mode range is exceeded. The AD301AL is specified for operation from 0°C to +70°C, and is available in both the TO-99 and mini-DIP packages.

### GUARANTEED ACCURACY

The vastly improved performance of the AD301AL provides the user with an ideal choice when precision and flexibility are needed and economy is a necessity. The error budget calculated for the AD301A, AD201A and the AD301AL (see page 3) makes it apparent that this selected version offers substantial improvement over the other two industry-standard amplifiers at +25°C and for 0°C to +70°C applications. A typical circuit configuration (see Figure 1) is assumed, and the various errors are computed using maximum values at both +25°C and +70°C. The results indicate a factor of greater than 4 improvement of the AD301AL over the AD301A and a 30% improvement over the AD201A. Note that the error has been determined as a sum of component errors, but that in actuality the total error will be less, and resemble a root mean square sum.

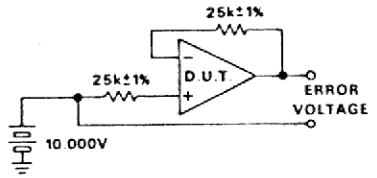



*Figure 1. Error Budget Analysis Circuit*



Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577

# SPECIFICATIONS (typical @ +25°C and ±15VDC, unless otherwise specified)

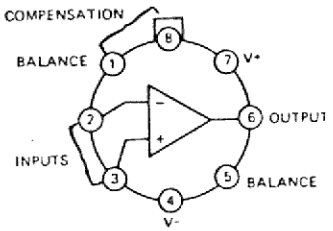
| MODEL | AD301AL |
|---|---|
| OPEN LOOP GAIN | |
| $V_O$ = ±10V, $R_L \geq 2k\Omega$ | 80,000 min (300,000 typ) |
| @ $T_A$ = 0°C to +70°C | 40,000 min (100,000 typ) |
| OUTPUT CHARACTERISTICS | |
| Voltage, $R_L \geq 10k\Omega$, $T_A$ = 0°C to +70°C | ±12V min (±14V typ) |
| $R_L \geq 2k\Omega$, $T_A$ = 0°C to +70°C | ±10V min (±13V typ) |
| Short Circuit Current | 25mA |
| FREQUENCY RESPONSE | |
| Unity Gain, Small Signal, $C_C$ = 30pF | 1MHz |
| Feedforward | 10MHz |
| Full Power Response, $C_C$ = 30pF | 6kHz |
| Feedforward | 150kHz |
| Slew Rate, Unity Gain, $C_C$ = 30pF | 0.25V/μsec |
| Feedforward | 9V/μsec |
| INPUT OFFSET VOLTAGE | |
| Initial, $R_S < 50k\Omega$ | 0.5mV max (0.3mV typ) |
| vs. Temperature, $T_A$ = 0°C to +70°C | 5μV/°C max (2μV/°C typ) |
| vs. Supply | 90dB min (100dB typ) |
| @ $T_A$ = 0°C to +70°C | 80dB min (96dB typ) |
| INPUT OFFSET CURRENT | |
| Initial | 5nA max (3nA typ) |
| @ $T_A$ = 0°C to +70°C | 10nA max |
| vs. Temperature, 25°C < $T_A$ < 70°C | 0.1nA/°C max |
| 0°C < $T_A$ < 25°C | 0.1nA/°C max |
| INPUT BIAS CURRENT | |
| Initial | 30nA max (15nA typ) |
| @ $T_A$ = 0°C to +70°C | 45nA max |
| INPUT VOLTAGE NOISE | |
| f = 10Hz | 22nV/√Hz |
| f = 100Hz | 18nV/√Hz |
| f = 1kHz | 13nV/√Hz |
| INPUT IMPEDANCE | 1.5MΩ min (4MΩ typ) |
| INPUT VOLTAGE RANGE | |
| Differential, Max Safe | ±30V |
| Common Mode, Max Safe | $\pm V_S$, $V_S \leq 15V$ |
| Common Mode Rejection Ratio | 90dB min (100dB typ) |
| @ $T_A$ = 0°C to +70°C | 80dB min (90dB typ) |
| POWER SUPPLY | |
| Rated Performance | ±15V |
| Operating | ±18V |
| Quiescent Current | 3mA max (1.8mA typ) |
| TEMPERATURE RANGE | |
| Operating, Rated Performance | 0°C to +70°C |
| Storage | −65°C to +150°C |

Specifications subject to change without notice.

## CONNECTION DIAGRAMS
(Top View)

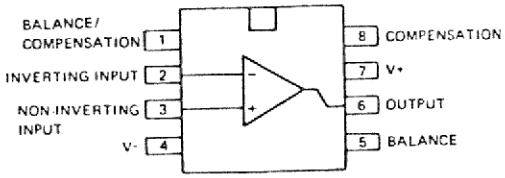
'H' Package

TO-99




'N' Package

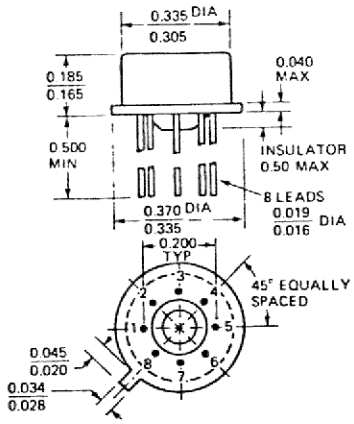
Mini-DIP




## PHYSICAL DIMENSIONS
(In Inches)

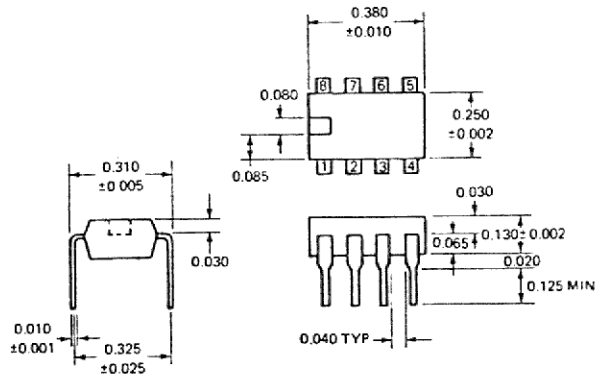
'H' Package

TO-99




'N' Package

Mini-DIP



## ERROR BUDGET ANALYSIS

Op amp accuracy is a confusing term, often subject to misinterpretation. The total output error of an op amp accrues from a number of error sources, whose relative contributions may vary appreciably with different applications, as well as variations in operating temperatures.

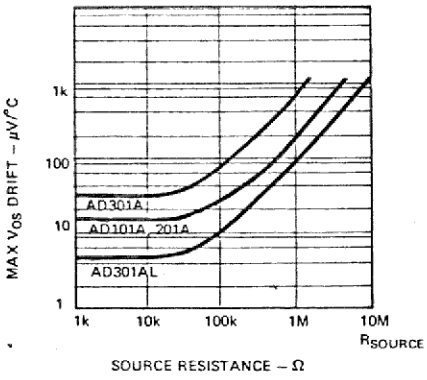
The Error Budget Analysis, which reveals all significant error contributions, is a useful figure of merit of an op amp when used in a particular application. The error contributions are established from the min or max values, both at room temperature and at +70°C. A unity gain non-inverting configuration is assumed for simplicity. While this configuration is only one of a multitude of possible applications, it effectively demonstrates the great improvement in overall accuracy achievable at relatively low cost using the AD301AL.

### ERROR BUDGET ANALYSIS

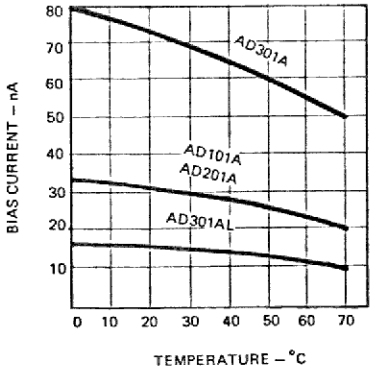
| PARAMETER | ERROR | SPEC ERROR AD301AL $T_A$ = +25°C | | SPEC ERROR AD201A $T_A$ = +25°C | | SPEC ERROR AD301A $T_A$ = +25°C | | SPEC ERROR AD301AL $T_A$ = +70°C | | SPEC ERROR AD201A $T_A$ = +70°C | | SPEC ERROR AD301A $T_A$ = +70°C | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Gain | $10V_{in}/G$ | 80,000 | 125μV | 50,000 | 200μV | 25,000 | 400μV | 40,000 | 250μV | 25,000 | 400μV | 15,000 | 665μV |
| $I_b$ (nA) | $I_b$ x resistor mismatch | 30 | 15μV | 75 | 38μV | 250 | 125μV | 45 | 23μV | 100 | 50μV | 300 | 150μV |
| $I_{os}$ (nA) | $I_{os}$ x 25kΩ | 5 | 125μV | 10 | 250μV | 50 | 1250μV | 10 | 250μV | 20 | 500μV | 70 | 1750μV |
| $\Delta V_{os}/\Delta T$ (μV/°C) | $(\Delta V_{os}/\Delta T) \cdot \Delta T$ | – | – | – | – | – | – | 5 | 225μV | 15 | 675μV | 30 | 1350μV |
| CMRR (dB) | 10V/CMRR | 90 | 330μV | 90 | 330μV | 80 | 1000μV | 80 | 1000μV | 80 | 1000μV | 70 | 3300μV |
| PSRR (dB) | Assume a ±5% power supply variation | 90 | 96μV | 90 | 96μV | 80 | 330μV | 80 | 330μV | 80 | 300μV | 70 | 960μV |
| TOTAL | | | 691μV | | 914μV | | 3075μV | | 2048μV | | 2925μV | | 8175μV |

## INPUT CHARACTERISTICS

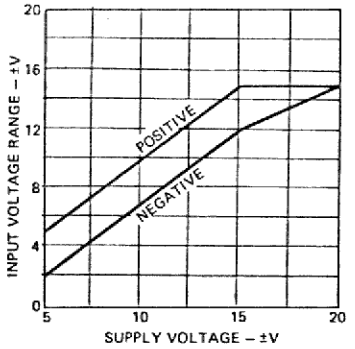
### MAX EQUIVALENT INPUT OFFSET DRIFT VS. SOURCE RESISTANCE



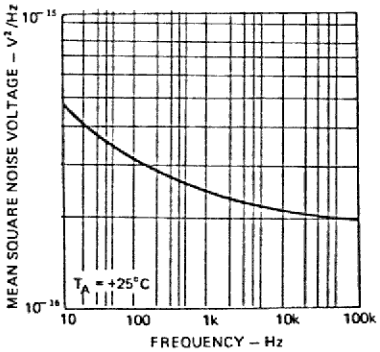

### BIAS CURRENT VS. TEMPERATURE



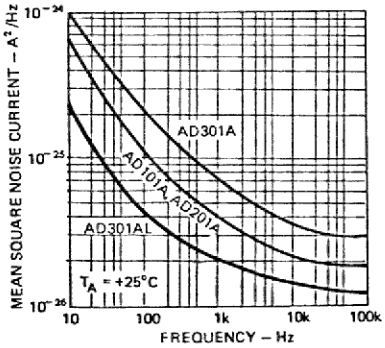

### INPUT VOLTAGE RANGE VS. SUPPLY



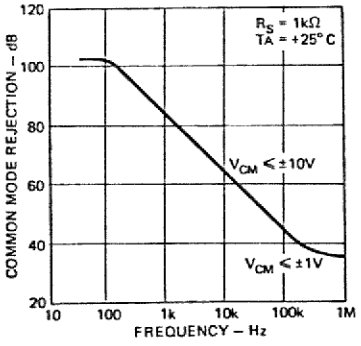

### INPUT NOISE VOLTAGE VS. FREQUENCY




### INPUT NOISE CURRENT VS. FREQUENCY

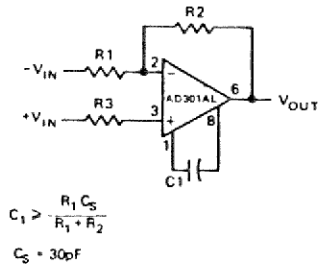



### COMMON MODE REJECTION VS. FREQUENCY

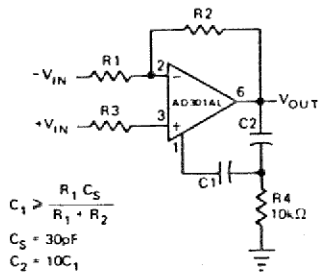


## DYNAMIC PERFORMANCE

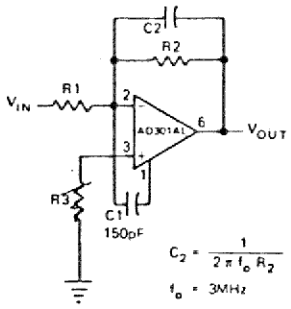
### SINGLE-POLE COMPENSATION



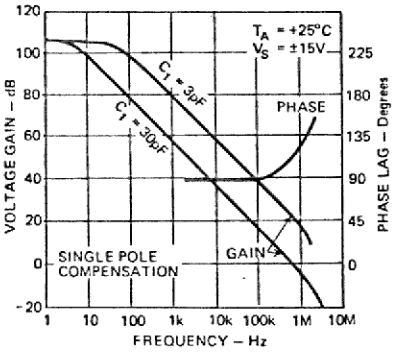

### TWO-POLE COMPENSATION



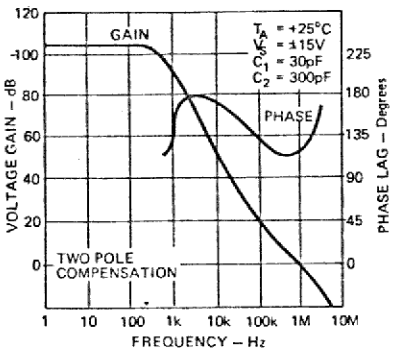

### FEEDFORWARD COMPENSATION



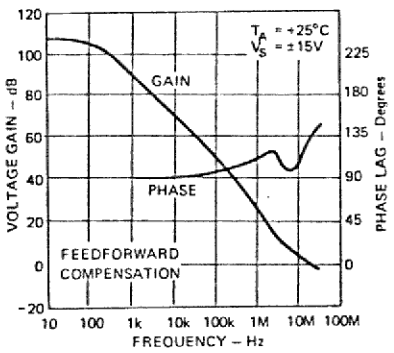

### Open Loop Frequency Response



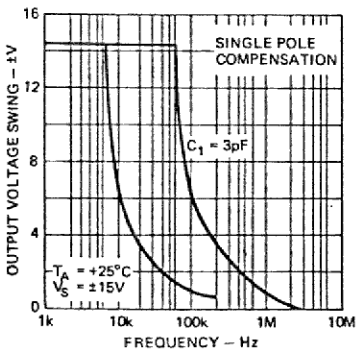

### Open Loop Frequency Response



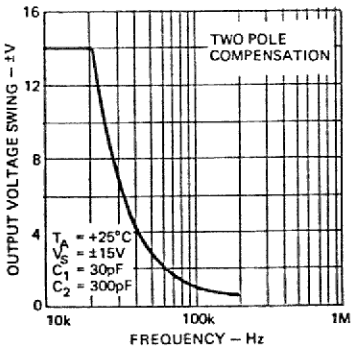

### Open Loop Frequency Response



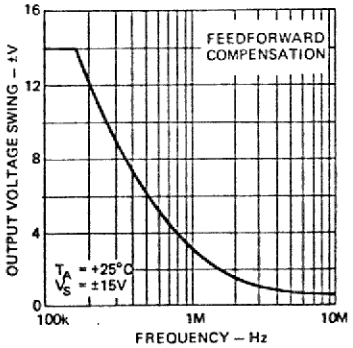

### Large Signal Frequency Response




### Large Signal Frequency Response




### Large Signal Frequency Response




## ORDERING GUIDE

| MODEL | TEMP RANGE | ORDER NUMBER |
|---|---|---|
| AD301AL | 0°C to +70°C | AD301AL* |
| AD201A | −25°C to +85°C | AD201A* |
| AD301A | 0°C to +70°C | AD301A* |
| AD101A | −55°C to +125°C | AD101AH |
| AD101A | −55°C to +125°C | AD101AF |
| §AD101A/883 | −55°C to +125°C | AD101AF/883 |

* Add package type letter: H = TO-99, N = Mini-DIP, F = Flat Pack.

§ Standard AD101A in a 10-lead, hermetically-sealed flat pack (TO-91) processed to MIL-STD-883, Method 5004, Level B.

† Minimum order...10 pieces.

For information on AD101A, AD201A, AD301A, see separate data sheet previously published for these products.

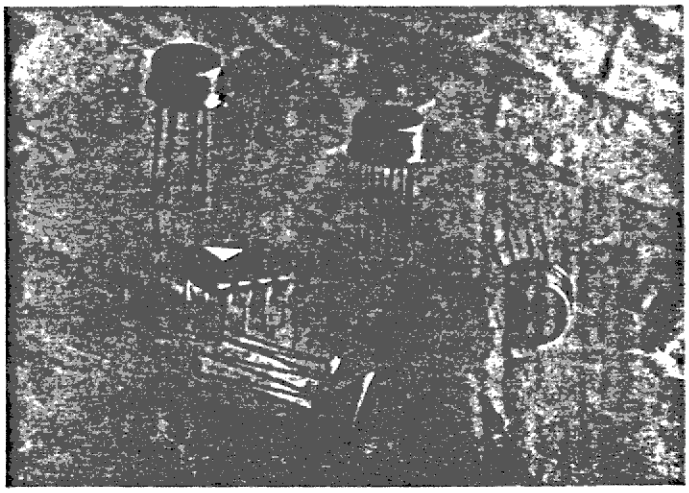
A2.17

ANALOG DEVICES

# Precision Comparators

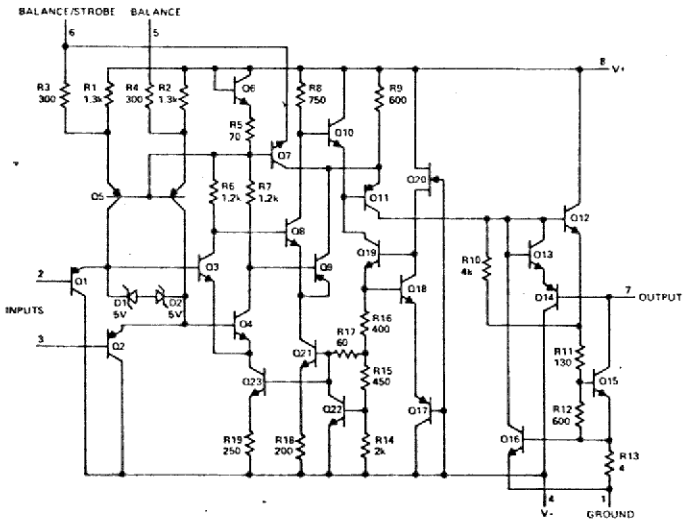
# AD111/211/311

FEATURES
Differential Input Voltage Range: ±30V
Common Mode Input Voltage Range: ±14V
Supply Voltage: From +5V to ±18V
Input Offset Voltage: 3mV max
Input Bias Current: 100nA max
Output: 35V, 50mA TTL Compatible
Strobed Output
Input Offset Adjustable



PRODUCT DESCRIPTION

The AD111, AD211, and AD311 are precision voltage comparators designed for low level signal detection and high level output drive capability. Offering significant improvement over the earlier 710-type comparator in terms of bias currents and gain, the AD111 series operates on supply voltages from +5V (single ended) up to ±18V. TTL strobe capability is available with the addition of two external components. The AD311 is specified from 0 to +70°C, the AD211 from -25°C to +85°C and the AD111 over the full military temperature range -55°C to +125°C. All versions are available in the TO-99 can; the AD311 is also available in the 8 pin mini dip.




*Schematic Diagram*

PRODUCT HIGHLIGHTS

1. Differential voltages up to the supply voltage (30V where $V_S = \pm 15V$) are permitted so long as either positive or negative input voltages remain below the supply voltages.
2. The AD211 series operates on supply voltages from ±18V down to a single supply of only +5V.
3. The AD111 series can deliver a 50mA output current or 35V of output voltage. They can drive TTL, RTL, DTL, and MOS loads as well as lamps and relays. The outputs can be wire OR ed for window or threshold detectors.
4. Where excessive noise is present or an additional logic input is desired, the AD111 series provide TTL strobing with the addition of two external components.
5. The AD111 series offer bias currents below 100nA and gains of 200,000, thus providing the user with greater accuracy and versatility over the earlier 710-type comparators.



P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Telex: 924491 Cables: ANALOG NORWOODMASS

A2.18

# SPECIFICATIONS (typical @ $V_S$ = ±15V, $V_D$ = 5V, $R_L$ = 500Ω and $T_A$ = +25°C unless otherwise specified)

| Model | AD311 | AD211 | AD111 |
|---|---|---|---|
| OPERATING TEMPERATURE RANGE | 0 to +70°C | -25°C to +85°C | -55°C to +125°C |
| VOLTAGE GAIN | 200V/mV | • | • |
| INPUT CHARACTERISTICS | | | |
| Maximum Input Voltage (Note 1) | ±15V | • | • |
| Over Operating Temperature Range | ±14V | • | • |
| Offset Voltage (Note 2) | 2.0mV typ (7.5mV max) | 0.7mV typ (3.0mV max) | •• |
| Over Operating Temperature Range | 10.0mV max | 4.0mV max | •• |
| Bias Current (Note 3) | 100nA typ (250nA max) | 60nA typ (100nA max) | •• |
| Over Operating Temperature Range | 300nA max | 150nA max | •• |
| Offset Current (Note 2) | 6nA typ (50nA max) | 4nA typ (10nA max) | •• |
| Over Operating Temperature Range | 70nA max | 20nA max | •• |
| OUTPUT CHARACTERISTICS | | | |
| Maximum Output to Negative Supply Voltage ($V_{7,4}$) | 50V | • | • |
| Maximum Ground to Negative Supply Voltage ($V_{1,4}$) | 30V | • | • |
| Leakage Current (Note 4) | 0.2nA typ (50nA max) | 0.2nA typ (10nA max) | •• |
| Over Operating Temperature Range | 0.1μA typ | 0.1μA typ (0.5μA max) | •• |
| Saturation Voltage (Note 5) | 0.75V typ (1.5V max) | • | • |
| Over Operating Temperature Range (Note 6) | 0.23V typ (0.4V max) | • | • |
| Short Circuit Duration | 10 sec | • | • |
| POWER SUPPLIES | | | |
| Total Supply Voltage ($V_{8,4}$) | 5V min (36V max) | • | • |
| Positive Supply Current | 5.1mA typ (7.5mA max) | 5.1mA typ (6mA max) | •• |
| Negative Supply Current | 4.1mA typ (5mA max) | • | • |
| RESPONSE TIME (Note 7) | 200ns | • | • |
| STROBE ON CURRENT (Note 8) | 3mA | • | • |
| THERMAL CHARACTERISTICS | | | |
| Power Dissipation | 500mW max | • | • |
| Maximum Junction Temperature | +85°C | +110°C | +150°C |
| Thermal Resistance | | | |
| Junction-to-Ambient | | | |
| TO-99 Package | 150°C/W | • | • |
| Mini-DIP Package | 210°C/W | — | — |
| Junction-to-Case | | | |
| TO-99 Package | 45°C/W | • | • |
| Mini-DIP Package | 80°C/W | — | — |
| Storage Temperature Range | -65°C to +150°C | • | • |
| Lead Temperature (Soldering, 10 sec) | +300°C | • | • |

*Specifications same as AD311.
**Specifications same as AD211
Prices and specifications subject to change without notice.

Note 1. This rating applies for ±15V supplies. The positive voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance. Offset voltage is specified with an input source resistance of 50k or less.

Note 3. Input bias current for this product is defined as the average of the two input currents.

Note 4. The conditions for this specification are $V_S$ = ±15V, Pin 1 at ground, 5mV input voltage to the 111/211 or 10mV input voltage to the 311 and the output Pin 7 pulled up to +35V.

Note 5. The conditions for this specification are $V_S$ = ±15V, Pin 1 at ground, 5mV input voltage to the 111/211 or 10mV input voltage to the 311 and the output Pin 7 sinking 50mA.

Note 6. The conditions for this specification are $V_S$ = ±15V, Pin 1 at ground, 6mV input to the 111/211 or 10mV input voltage to the 311 and the output Pin 7 sinking 8mA.

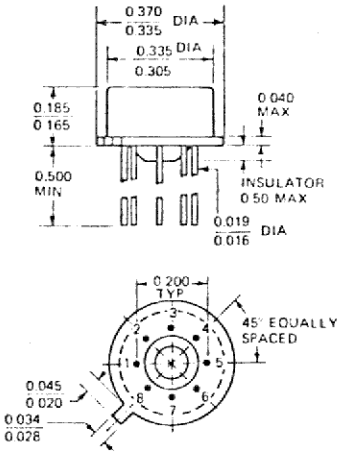
Note 7. The response time specified is for a 100mV input step with 5mV of overdrive "Response Time" is the interval between the application of an input step function and the time when the output crossed the TTL logic threshold.

Note 8. Strobe on current is the current that must be drawn out of the strobe terminal to disable the comparator, not the current that will flow out of the strobe terminal if it is grounded. We recommend using at least a 1kΩ resistor in series with strobe terminal.

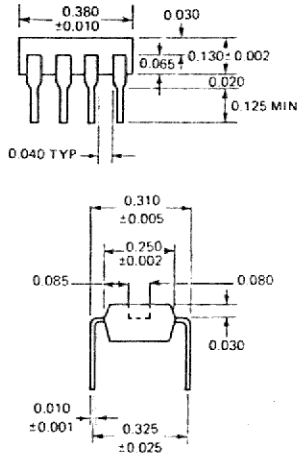
## OUTLINE DIMENSIONS

Dimensions shown in inches

### TO-99

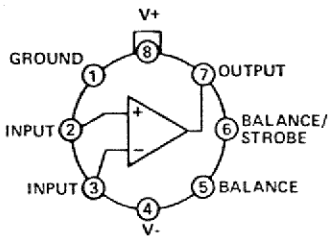



### MINI-DIP

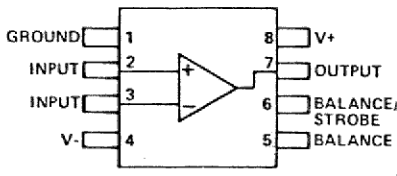


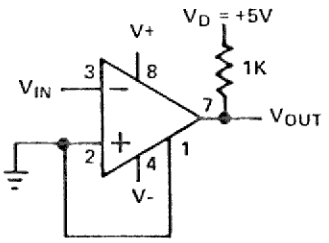

## CONNECTION DIAGRAMS

### TO-99
Top View

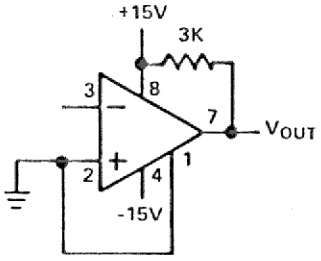



### MINI-DIP
Top View

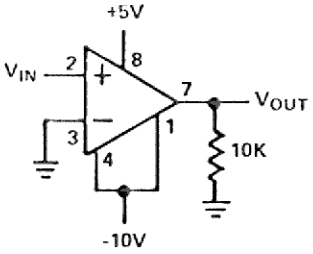




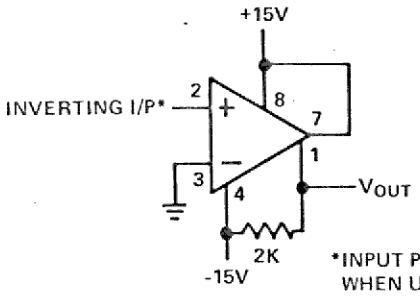

*TTL Compatible Output Swing*



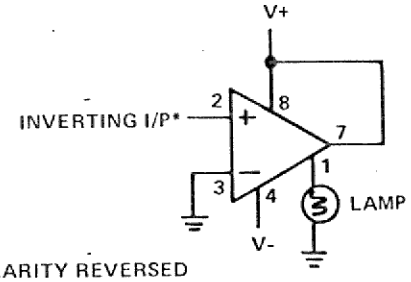

*High Level TTL Compatible Output Swing*




*MOS Logic Compatible Output Swing*

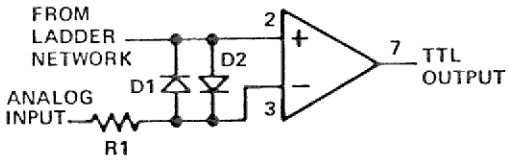



*Obtaining ±15 Volt Output Swing*

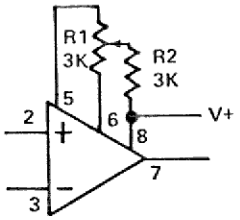



*Driving Ground-Referred Load*

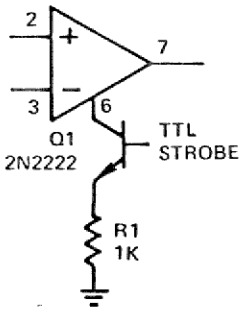
*INPUT POLARITY REVERSED WHEN USING PIN 1 AS OUTPUT



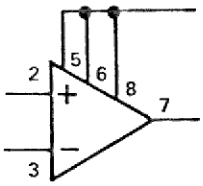

*Using Clamp Diodes To Improve Response*




*Offset Balancing*

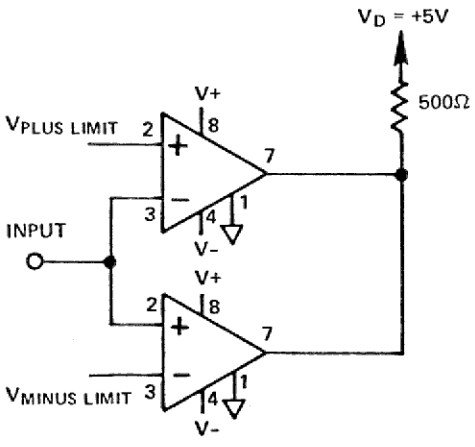



*Strobing*

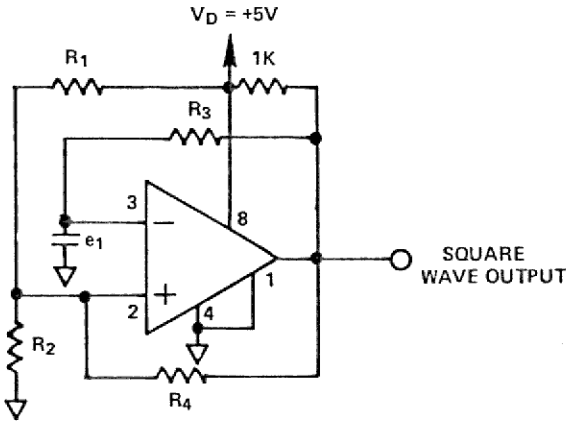


*INCREASES TYPICAL COMMON MODE SLEW FROM 7.0V/μs TO 18V/μs

*Increasing Input Stage Slew Rate**

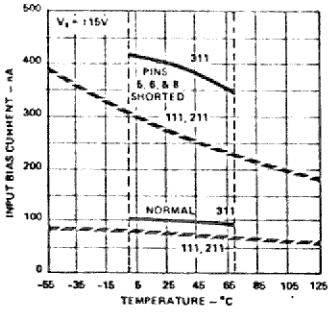



*Window Detector*

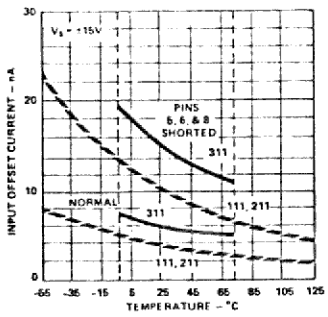



*Free-Running Multivibrator*

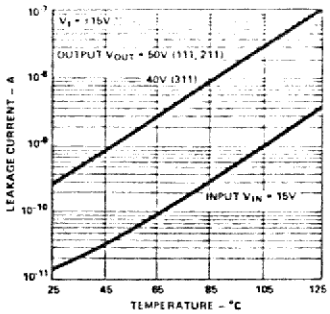
## TYPICAL PERFORMANCE



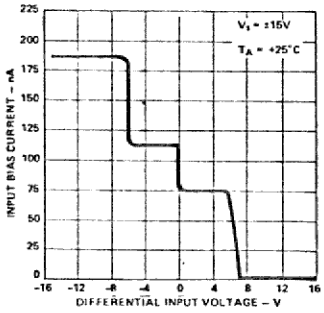

*Input Bias Current*



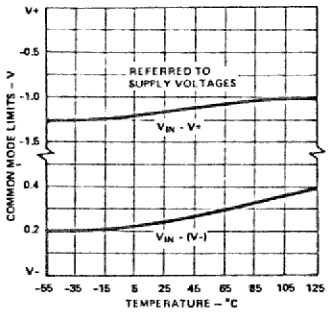

*Input Offset Current*



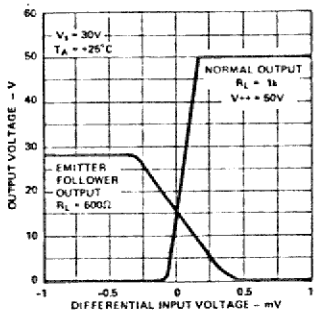

*Leakage Currents*



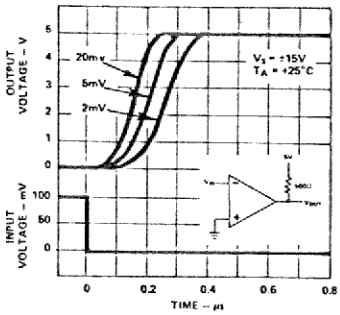

*Input Characteristics*



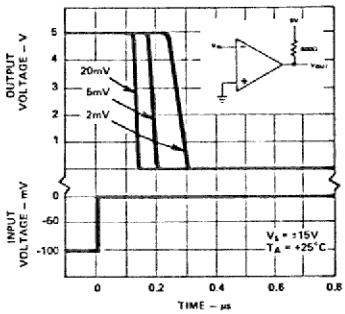

*Common Mode Limits*



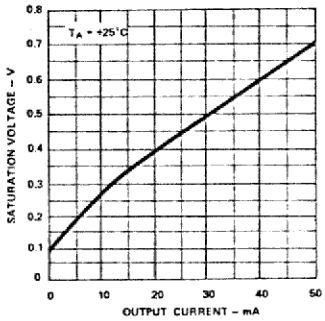

*Transfer Function*



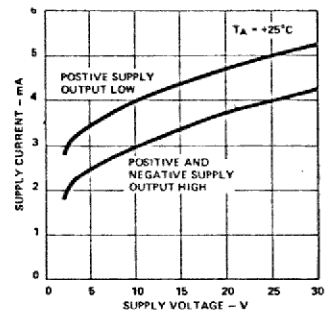

*Response Time For Various Input Overdrives*



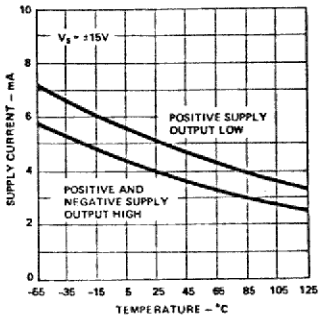

*Response Time For Various Input Overdrives*



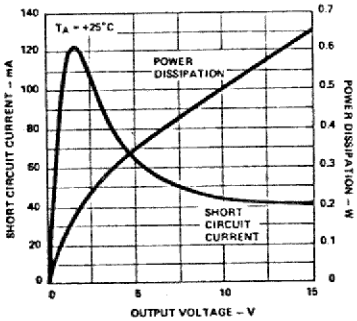

*Output Saturation Voltage*



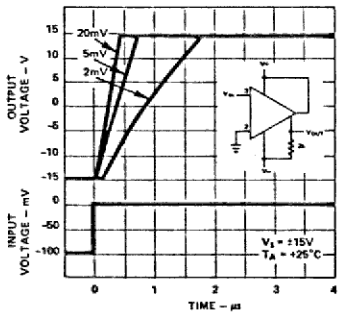

*Supply Current*



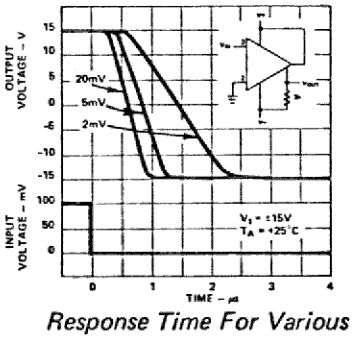

*Supply Current*




*Output Limiting Characteristics*




*Response Time For Various Input Overdrives*




*Response Time For Various Input Overdrives*

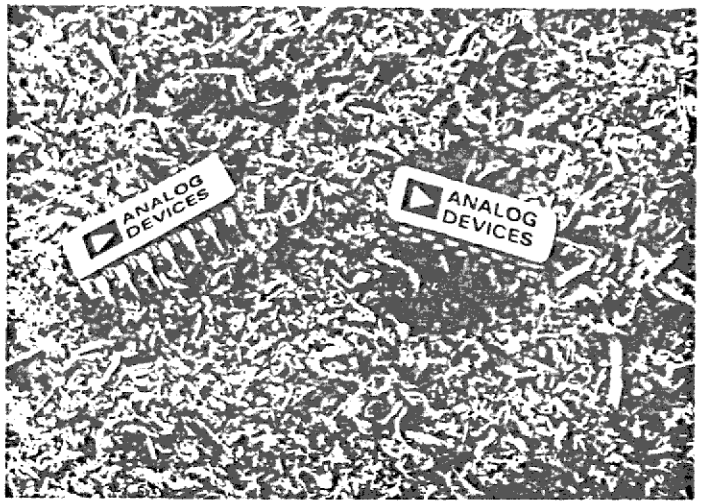
A2.21

ANALOG DEVICES

# IC Sample and Hold Gated Op Amp

# AD583

FEATURES
High Sample-to-Hold Current Ratio: $10^6$
High Slew Rate: 5V/μsec
High Bandwidth: 2MHz
Low Aperture Time: 50ns
Low Charge Transfer: 10pC
DTL/TTL Compatible
May Be Used as Gated Op Amp

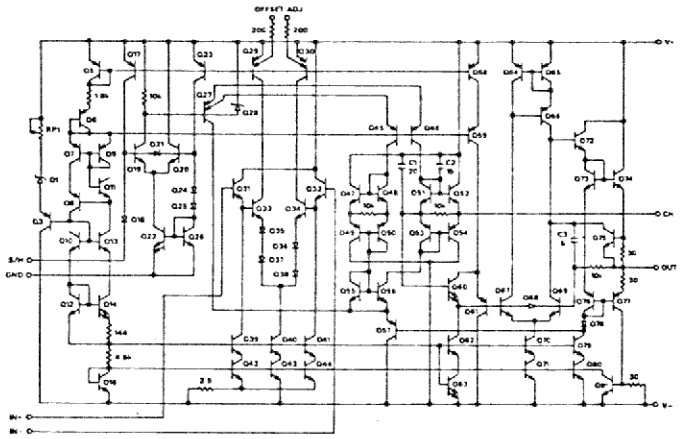



## PRODUCT DESCRIPTION

The AD583 is a monolithic sample and hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier. An external holding capacitor, connected to the switch output, completes the sample-and-hold or track-and-hold function.

With the analog switch closed, the AD583 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open the capacitor holds the output at its previous level.

The AD583 may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.



*Schematic Diagram*

## PRODUCT HIGHLIGHTS

1. Sample-and-hold operation is obtained with the addition of one external capacitor.
2. Low charge transfer (10pC) and high sample-to-hold current ratio insure accurate tracking.
3. Any gain or frequency response is available using standard op amp feedback networks.
4. High slew rate and low aperature time permit sampling of rapidly changing signals.
5. Output, gated through a low leakage analog switch, also makes the AD583 useful for applications such as analog switches, peak holding circuits, etc.



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A2.22a

# SPECIFICATIONS (typical @ +25°C and ±15VDC unless otherwise specified)

| MODEL | AD583K |
|---|---|
| OPEN LOOP GAIN<br>$R_L$ = 2kΩ, $T_{min}$ to $T_{max}$ | 25k min (50k typ) |
| OUTPUT VOLTAGE SWING<br>$R_L$ = 2kΩ, $T_{min}$ to $T_{max}$ | ±10V min |
| OUTPUT CURRENT | ±10mA min |
| OUTPUT RESISTANCE | 5Ω |
| OFFSET VOLTAGE<br>$T_{min}$ to $T_{max}$ | 6mV max (3mV typ)<br>8mV max (4mV typ) |
| BIAS CURRENT<br>$T_{min}$ to $T_{max}$ | 200nA max (50nA typ)<br>400nA max |
| OFFSET CURRENT<br>$T_{min}$ to $T_{max}$ | 50nA max (10nA typ)<br>100nA max |
| INPUT RESISTANCE | 5MΩ min (10MΩ typ) |
| COMMON MODE RANGE | ±10V min |
| COMMON MODE REJECTION<br>$T_{min}$ to $T_{max}$ | 74dB min (90dB typ) |
| GAIN BANDWIDTH PRODUCT | 2MHz |
| SLEW RATE<br>Av = +1, $R_L$ = 2kΩ, $C_L$ = 50pF,<br>$V_{out}$ = ±10V p-p | 5V/μsec |
| RISE TIME<br>Av = +1, $R_L$ = 2kΩ, $C_L$ = 50pF,<br>$V_{out}$ = 400mV p-p | 100nsec |
| OVERSHOOT<br>Av = +1, $R_L$ = 2kΩ, $C_L$ = 50pF,<br>$V_{out}$ = 400mV p-p | 20% |
| DIGITAL INPUT CURRENT<br>$V_{in}$ = 0, $T_{min}$ to $T_{max}$<br>$V_{in}$ = +5.0V, $T_{min}$ to $T_{max}$ | <br>0.8mA max<br>20μA max |
| DIGITAL INPUT VOLTAGE<br>Low $T_{min}$ to $T_{max}$<br>High $T_{min}$ to $T_{max}$ | <br>0.8V max<br>2.0V min |
| ACQUISITION TIME<br>Av = +1, $R_L$ = 2kΩ, $C_L$ = 50pF<br>to 0.1% of final value | 4μsec |
| APERTURE TIME | 50nsec |
| DRIFT CURRENT<br>$T_{min}$ to $T_{max}$ | 50pA max (5pA typ)<br>1.0nA max (0.05nA typ) |
| CHARGE TRANSFER | 20pC max (10pC typ) |
| SUPPLY CURRENT | 5.0mA max (2.5mA typ) |
| POWER SUPPLY REJECTION | 74dB min (90dB typ) |
| OPERATING TEMP | 0 to +70°C |
| STORAGE TEMP | -65 to +150°C |

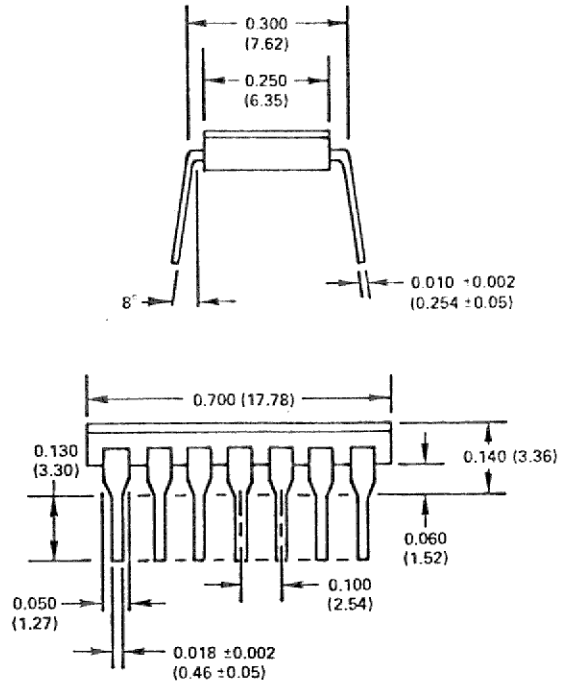
Specifications subject to change without notice.

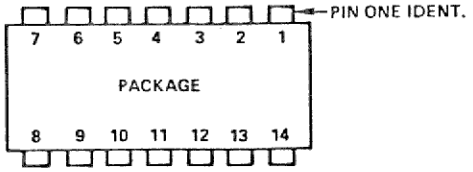
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Voltage between V+ and V- Terminals | 40V |
| Differential Input Voltage | ±30V |
| Digital Voltage (Pin 14) | +8V, -15V |
| Output Current | Short Circuit Protected |
| Internal Power Dissipation | 30mW (Derate power dissipation by 4.3mW/°C above +150°C ambient temperature) |

## OUTLINE DIMENSIONS

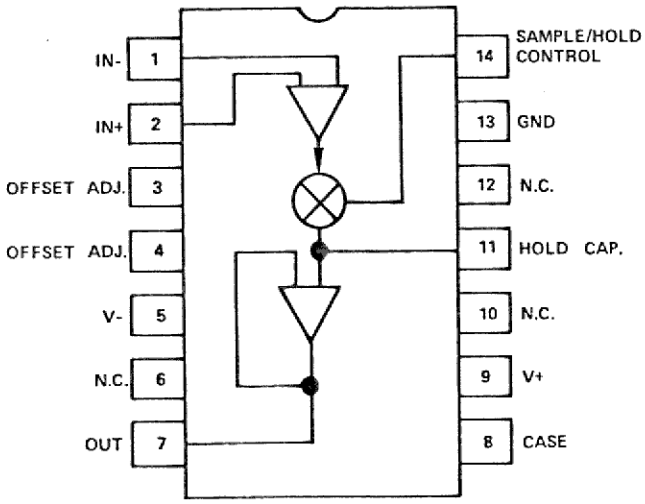
Dimensions shown in inches and (mm)



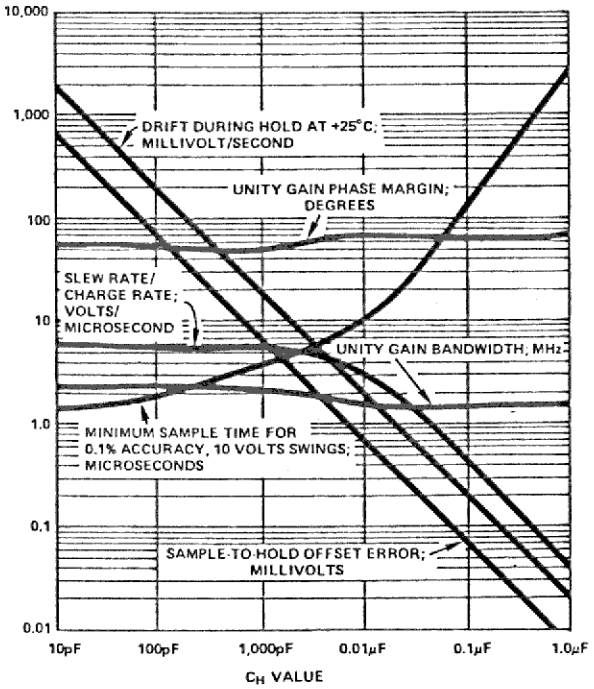

ALL DIMENSIONS ±0.010 UNLESS OTHERWISE SHOWN

## PIN CONFIGURATION

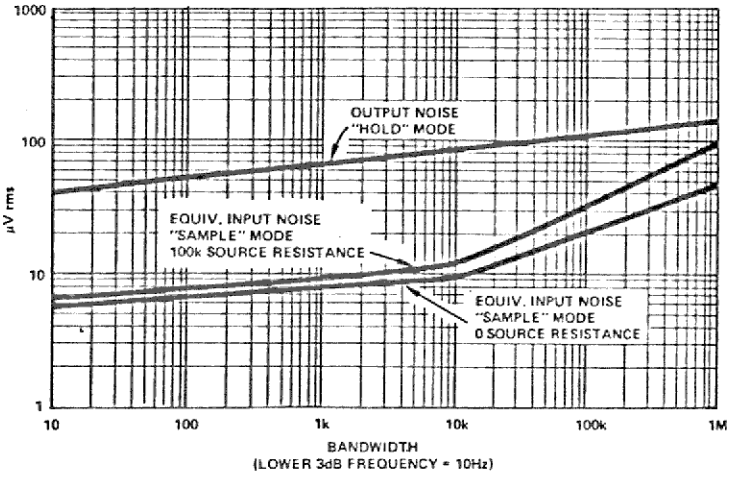


# Performance Curves

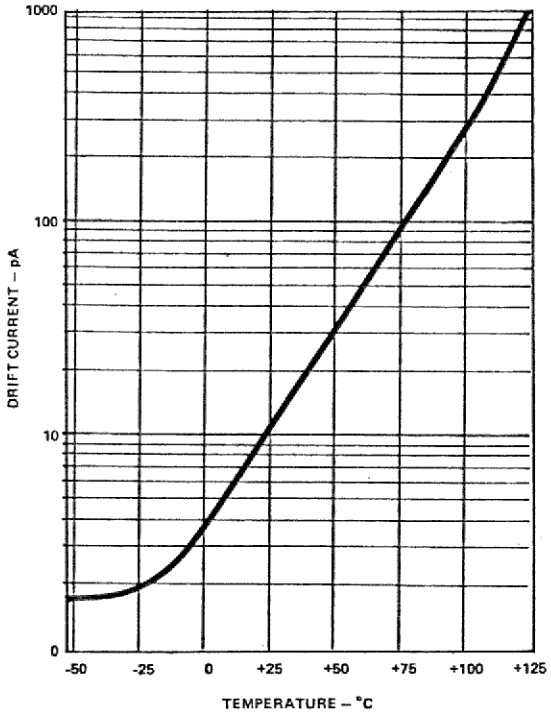
$V_{SUPPLY}$ = ±15VDC, $T_A$ = +25°C, $C_H$ = 1,000pF unless otherwise specified



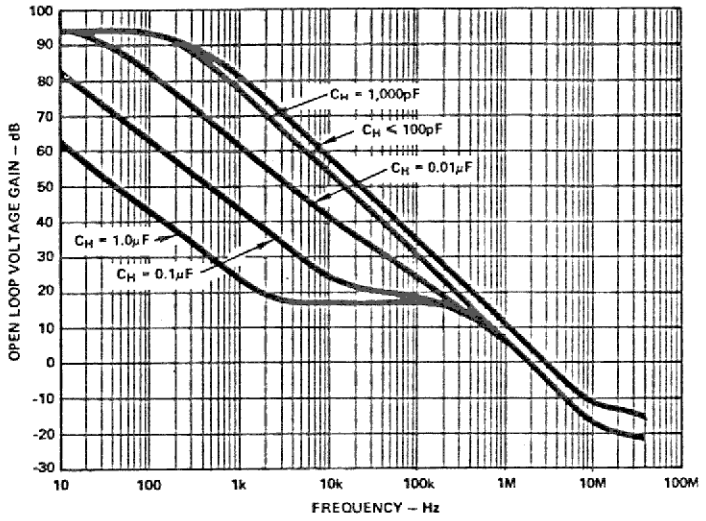

*Typical Sample-and-Hold Performance as a Function of Holding Capacitance*



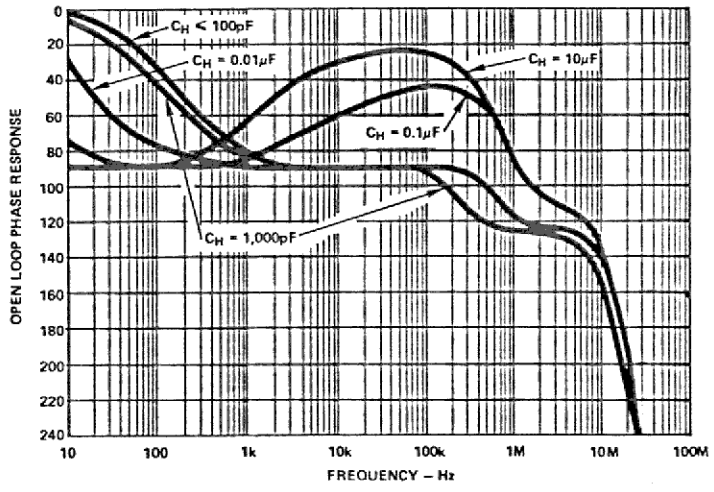

*Broadband Noise Characteristics*




*Drift Current vs. Temperature*




*Open Loop Frequency Response*




*Open Loop Phase Response*

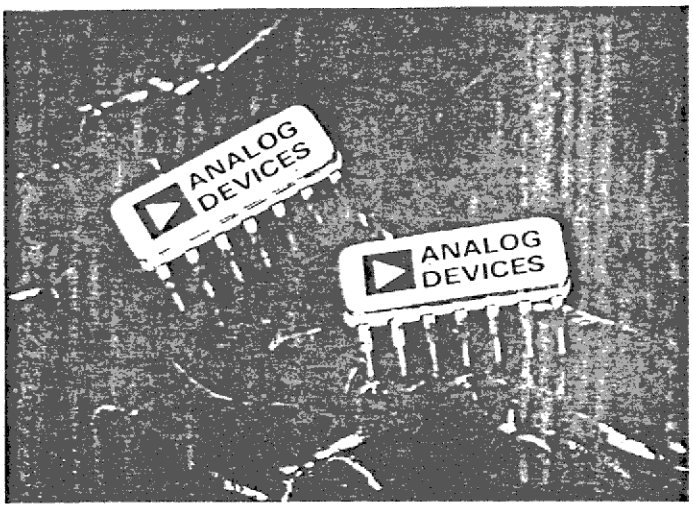
A223

ANALOG DEVICES

# Integrated Circuit Precision Instrumentation Amplifier

## PRELIMINARY TECHNICAL DATA

FEATURES
Programmable Gains from 0.1 to 1000
Floating Differential Inputs
High CMRR: 110dB min
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Low Noise: 0.5$\mu$V p-p (0.1 to 10Hz)
Extremely Low Cost:




### PRODUCT DESCRIPTION

The AD521 is the second generation, low cost, monolithic I.C. instrumentation amplifier developed by Analog Devices. A true instrumentation amplifier, the AD521 is a controlled gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521, like its predecessor the AD520, should not be confused with an operational amplifier, even though several manufacturers (including Analog Devices) offer op amps that can be used as building blocks in variable gain instrumentation amplifier circuits. An op amp is merely a high gain component requiring the addition of external feedback to complete the amplification function. Because of the limitations of resistor matching in the external feedback circuit and the relatively low input impedance resulting from the input resistors, an instrumentation amplifier circuit designed around op amps frequently provides less than satisfactory performance. Since the AD521 is a complete amplification circuit which does not depend upon external resistor matching for input/output isolation it maintains its high CMRR (110dB min) in any application. In addition, the high impedance inputs are fully protected against over voltages up to 15V greater than the supply voltage.

The AD521 can be operated at gains from 0.1 to greater than 1000 with the addition of only two programming resistors. Excellent d.c. characteristics are realized through the device's inherently low offset and gain drift and optional one-pot nulling. Dynamic performance is also outstanding with a gain bandwidth product of 40MHz, full peak response of 100kHz and a 10V/$\mu$sec slew rate.

The AD521 I.C. instrumentation amplifier is available in three different versions, depending on accuracy and operating temperature range: the economical "J" specified from 0°C to +70°C, the low drift "K", also specified from 0°C to +70°C and the "S" guaranteed over the full MIL-temperature range, -55°C to +125°C. All versions are packaged in a hermetically-sealed 14 pin DIP.

### PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
3. The AD521 is fully protected for input levels up to 15V beyond the supply voltage and 30V differential at the inputs.
4. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
5. Offset nulling can be achieved with an optional trim pot.
6. The AD521 offers superior dynamic performance with a gain bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5$\mu$sec to 0.1% of a 10V step.
7. Every AD521 is baked for 40 hours at +150°C and temperature cycled ten times from -65°C to +150°C.

Note: this data sheet includes "Preliminary Technical Data" describing a new product. Though highly unlikely, it may be necessary to alter the specifications to reflect life data collected during the initial months of the product's use.



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**Telex: 924491 Cables: ANALOG NORWOODMASS**

# SPECIFICATIONS (typical @ $V_S$ = ±15V, $R_L$ = 2kΩ and $T_A$ = 25°C unless otherwise specified)

| MODEL | AD521J | AD521K | AD521S |
|---|---|---|---|
| GAIN | | | |
| Range (For Specified Operation. Note 1.) | 1 to 1000 | • | • |
| Equation | $G = R_S/R_G V/V$ | • | • |
| Error from Equation | (±0.25–0.004G)% | • | • |
| Nonlinearity (Note 2) | | | |
| 1≤G≤1000 | 0.1% max | • | • |
| Gain Temperature Coefficient | ±(3 ±0.05G)ppm/°C | • | ±(15 ±0.4G)ppm/°C |
| OUTPUT CHARACTERISTICS | | | |
| Rated Output | ±10V, ±10mA min | • | • |
| Output at Maximum Operating Temperature | ±10V @ 5mA min | • | • |
| Impedance | 0.1Ω | • | • |
| DYNAMIC RESPONSE | | | |
| Small Signal Bandwidth (±3dB) | | | |
| G = 1 | >2MHz | • | • |
| G = 10 | 300kHz | • | • |
| G = 100 | 200kHz | • | • |
| G = 1000 | 40kHz | • | • |
| Small Signal, ±1.0% Flatness | | | |
| G = 1 | 75kHz | • | • |
| G = 10 | 26kHz | • | • |
| G = 100 | 24kHz | • | • |
| G = 1000 | 6kHz | • | • |
| Full Peak Response (Note 3) | 100kHz | • | • |
| Slew Rate, 1≤G≤1000 | 10V/μsec | • | • |
| Settling Time (any 10V step to within 10mV of Final Value) | | | |
| G = 1 | 7μsec | • | • |
| G = 10 | 5μsec | • | • |
| G = 100 | 10μsec | • | • |
| G = 1000 | 35μsec | • | • |
| Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4) | | | |
| G = 1000 | 50μsec | • | • |
| Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5) | | | |
| G = 1000 | 10μsec | • | • |
| VOLTAGE OFFSET (may be nulled) | | | |
| Input Offset Voltage ($V_{os_1}$) | 3mV max (2mV typ) | 1.5mV max (0.5mV typ) | •• |
| vs. Temperature | 15μV/°C max (7μV/°C typ) | 5μV/°C max (1.5μV/°C typ) | •• |
| vs. Supply | 3μV/% | • | • |
| Output Offset Voltage ($V_{os_0}$) | 400mV max (200mV typ) | 200mV max (30mV typ) | •• |
| vs. Temperature | 400μV/°C max (150μV/°C typ) | 150μV/°C max (50μV/°C typ) | •• |
| vs. Supply (Note 6) | $0.005V_{os_0}$/% | • | • |
| INPUT CURRENTS | | | |
| Input Bias Current (either input) | 80nA max | 40nA max | •• |
| vs. Temperature | 1nA/°C max | 500pA/°C max | •• |
| vs. Supply | 2%/V | • | • |
| Input Offset Current | 20nA max | 10nA max | •• |
| vs. Temperature | 250pA/°C max | 125pA/°C max | •• |
| INPUT | | | |
| Differential Input Impedance (Note 7) | $3 \times 10^9 \Omega \| 1.8pF$ | • | • |
| Common Mode Input Impedance (Note 8) | $6 \times 10^{10} \Omega \| 3.0pF$ | • | • |
| Input Voltage Range for Specified Performance | ±10V | • | • |
| Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9) | 30V | • | • |
| Voltage at either input (Note 10) | $V_S$ ±15V | • | • |
| Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance | | | |
| G = 1 | 70dB min (74dB typ) | 74dB min (80dB typ) | •• |
| G = 10 | 90dB min (94dB typ) | 94dB min (100dB typ) | •• |
| G = 1000 | 100dB min (104dB typ) | 104dB min (114dB typ) | •• |
| G = 1000 | 100dB min (110dB typ) | 110dB min (120dB typ) | •• |
| NOISE | | | |
| Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10) | $\sqrt{(0.5G)^2 + (150)^2}\,\mu V$ | • | • |
| RMS RTO, 10Hz to 10kHz | $\sqrt{(1.2G)^2 + (30)^2}\,\mu V$ | • | • |
| Input Current, rms, 10Hz to 10kHz | 15pA(rms) | • | • |
| REFERENCE TERMINAL | | | |
| Bias Current | 3μA | • | • |
| Input Resistance | 10MΩ | • | • |
| Voltage Range | ±10V | • | • |
| Gain to Output | 1 | • | • |
| POWER SUPPLY | | | |
| Operating Voltage Range | ±5 to ±18 | • | • |
| Quiescent Supply Current | 5mA max | • | • |
| TEMPERATURE RANGE | | | |
| Specified Performance | 0 to +70°C | • | -55 to +125°C |
| Operating | -25 to +85°C | • | -55 to +125°C |
| Storage | -65 to +150°C | • | • |

*Specification same as AD521J.
**Specification same as AD521K.

Specifications and prices subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, input voltage should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output of ±9 volts to 18 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.2%.

3. Full Peak Response is the typical frequency below which the amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μsec pulse at a 1kHz rate.(When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, and an added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is a 30V, 10μsec pulse at a 1kHz rate. (When a common mode signal greater than $V_S$ - 0.5V) is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, and an added thermal time constant, but will not damage the device.)

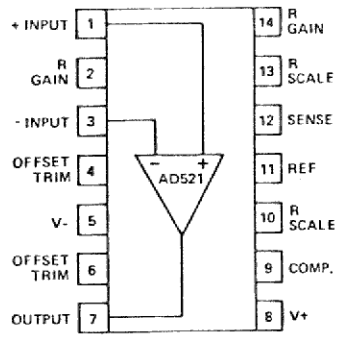
6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when $V_S$ = 0) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 6.




TOP VIEW

*Figure 1. AD521 Pin Configuration*

**TO-116**

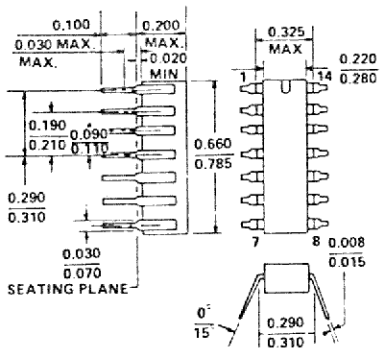



*Figure 2. Physical Dimensions*

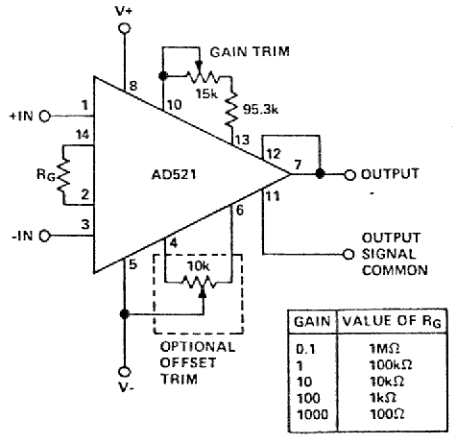



*Figure 3. Operating Connections for AD521*

## INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output under any gain or circuit configuration. An op amp with 1mV of input offset voltage, for exampl would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain, can be classi-

fied as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error with respect to either the input or output by the following formulae:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

As shown in Figure 4, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, $R_S/R_G$). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by $R_1$ and $R_2$. This gain factor is $1 + R_2/R_1$.

Where offset errors are critical, a resistor equal to the parallel combination of $R_1$ and $R_2$ should be placed between pin 11 and $V_{REF}$. This minimized the offset errors resulting from the input currents at the sense terminal flowing in $R_1$ and $R_2$. Note that gain changes introduced by changing the $R_1/R_2$ attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, $V_{REF}$ can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 4.

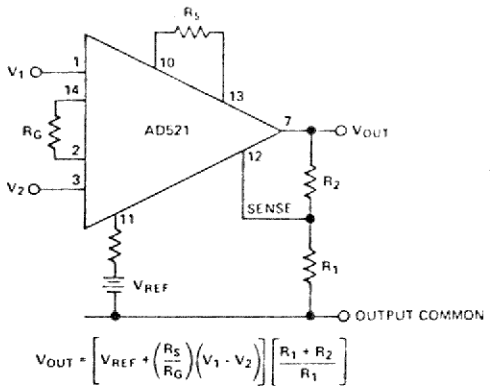



*Figure 4. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing $R_1$ and $R_2$ will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.*

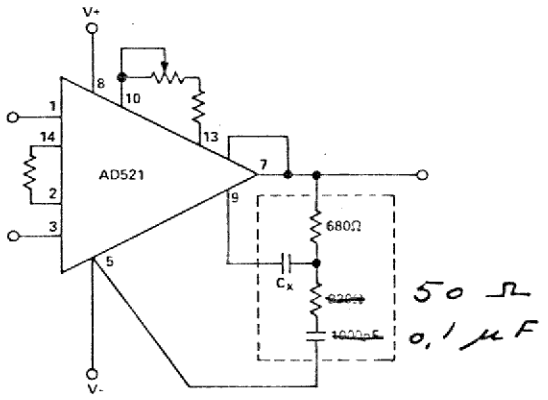



*Figure 5. Optional bandwidth control. $C_X$ is determined by the following relationship: $C_X = \frac{1}{2}\pi 50k\Omega\, f_t$ when $f_t$ is the desired bandwidth.*

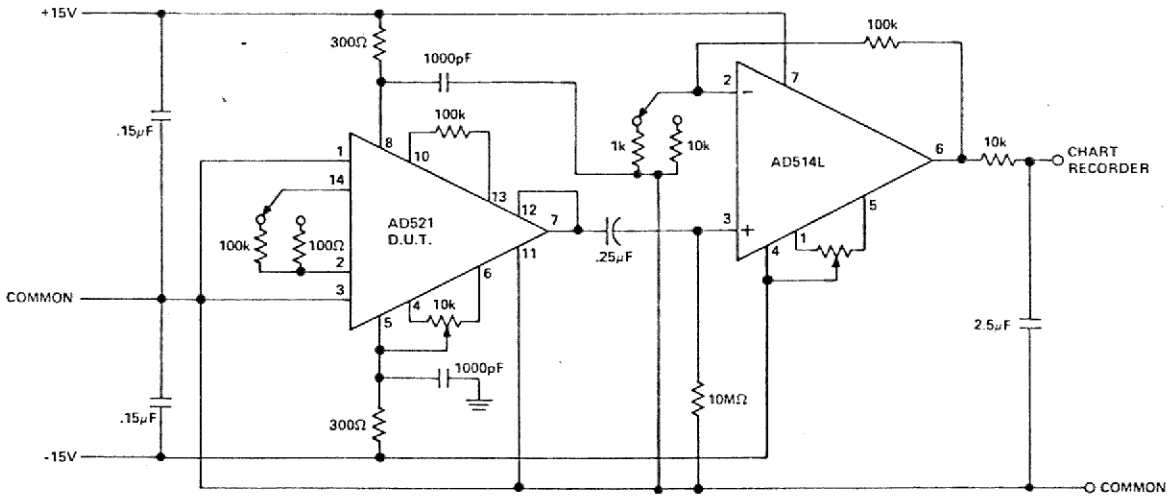



*Figure 6. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.*

A2.27

ANALOG DEVICES

# CMOS 8 and 16 Channel Analog Multiplexers

PRELIMINARY DATA SHEET

# AD7506/AD7507

## FEATURES

| | |
|---|---|
| $R_{ON}$ | 300Ω |
| Power Dissipation | 1.5 mW |

TTL/DTL/CMOS Compatible
Break Before Make Switching
Silicon Nitride Passivation
Replaces DG506/DG507

## GENERAL DESCRIPTION

The AD7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable". The AD7507 is identical to the AD7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable".

The AD7506 and AD7507 are excellent examples of a high breakdown CMOS process combined with a double layer interconnect for high density. Both units are silicon/nitride passivated featuring increased stability and reliability.

## ORDERING INFORMATION

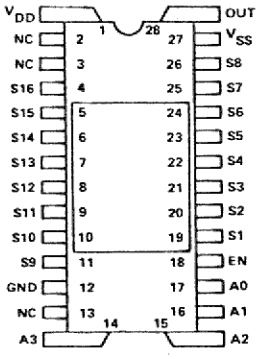
| | | |
|---|---|---|
| AD7506J | : | 0°C to +75°C |
| AD7506K | : | 0°C to +75°C |
| AD7506S | : | −55°C to +125°C |
| AD7506T | : | −55°C to +125°C |
| AD7507J | : | 0°C to +75°C |
| AD7507K | : | 0°C to +75°C |
| AD7507S | : | −55°C to +125°C |
| AD7507T | : | −55°C to +125°C |

## PACKAGE VERSIONS

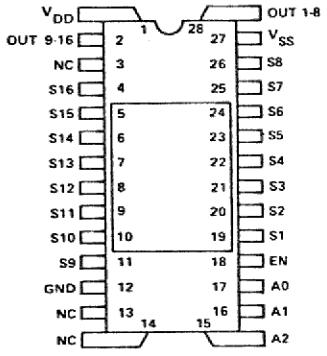
Suffix "D": 28-pin Ceramic DIP

## PIN CONFIGURATION (TOP VIEW)

AD7506

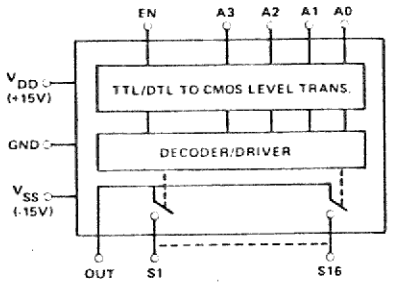



AD7507

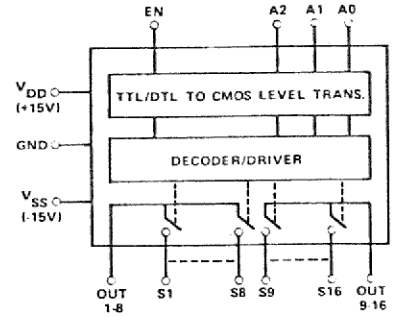



## FUNCTIONAL DIAGRAMS

AD7506




AD7507




## TRUTHTABLE

AD7506

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | EN | ON SWITCH |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 2 |
| 0 | 0 | 1 | 0 | 1 | 3 |
| 0 | 0 | 1 | 1 | 1 | 4 |
| 0 | 1 | 0 | 0 | 1 | 5 |
| 0 | 1 | 0 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 | 1 | 7 |
| 0 | 1 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 0 | 1 | 9 |
| 1 | 0 | 0 | 1 | 1 | 10 |
| 1 | 0 | 1 | 0 | 1 | 11 |
| 1 | 0 | 1 | 1 | 1 | 12 |
| 1 | 1 | 0 | 0 | 1 | 13 |
| 1 | 1 | 0 | 1 | 1 | 14 |
| 1 | 1 | 1 | 0 | 1 | 15 |
| 1 | 1 | 1 | 1 | 1 | 16 |
| X | X | X | X | 0 | NONE |

AD7507

| $A_2$ | $A_1$ | $A_0$ | EN | ON SWITCH PAIR |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 & 9 |
| 0 | 0 | 1 | 1 | 2 & 10 |
| 0 | 1 | 0 | 1 | 3 & 11 |
| 0 | 1 | 1 | 1 | 4 & 12 |
| 1 | 0 | 0 | 1 | 5 & 13 |
| 1 | 0 | 1 | 1 | 6 & 14 |
| 1 | 1 | 0 | 1 | 7 & 15 |
| 1 | 1 | 1 | 1 | 8 & 16 |
| X | X | X | 0 | NONE |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{DD}$ (to GND) | +17 V |
| $V_{SS}$ (to GND) | −17 V |
| Switch Voltage (to $V_{SS}$) | +27 V |
| Digital Input Voltage Range | $V_{DD}$ to GND |
| Switch Current | 10 mA |
| Power Dissipation (Package) | |
| To +70°C | 1200 mW |
| Derate Above +70°C by | 10 mW/°C |
| Operating Temperature | −55°C to +125°C |
| Storage Temperature | −65°C to +150°C |



Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062

# SPECIFICATIONS ($V_{DD}$ = +15 V, $V_{SS}$ = −15 V unless otherwise noted)

| PARAMETER | | VERSION | SWITCH CONDITION | @ 25°C | | | Over Specified Temp. Range | | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | | |
| **ANALOG SWITCH** | | | | | | | | | | |
| $R_{ON}$ | | J, K | ON | | 300 | 450 | | 550 | | $V_S$ = −10 V to +10 V, $I_S$ = 1 mA |
| | | S, T | ON | | | 400 | | 500 | | |
| $R_{ON}$ vs. $V_S$ | | All | ON | | 15 | | | | % | |
| $R_{ON}$ vs. Temperature | | All | ON | | 0.5 | | | | %/°C | $V_S$ = 0 V, $I_S$ = 1 mA |
| $R_{ON}$ Between Switches | | All | ON | | 4 | | | | % | |
| $R_{ON}$ Between Switches vs. Temperature | | All | ON | | 0.05 | | | | %/°C | |
| $I_S$ | | J, K | OFF | | 0.05 | 5 | | 50 | nA | $V_S$ = −10 V, $V_{OUT}$ = +10 V and $V_S$ = +10 V, $V_{OUT}$ = −10 V "Enable" Low |
| | | S, T | OFF | | 0.05 | 1 | | 50 | nA | |
| $I_{OUT}$ | AD7506 | J, K | OFF | | 0.3 | 20 | | 500 | nA | |
| | | S, T | OFF | | 0.3 | 10 | | 500 | nA | |
| | AD7507 | J, K | OFF | | 0.3 | 10 | | 250 | nA | |
| | | S, T | OFF | | 0.3 | 5 | | 250 | nA | |
| $I_{OUT} - I_S$ | AD7506 | J, K | ON | | 0.3 | 20 | | 500 | nA | $V_S$ = 0 |
| | | S, T | ON | | 0.3 | 10 | | 500 | nA | |
| | AD7507 | J, K | ON | | 0.3 | 10 | | 250 | nA | |
| | | S, T | ON | | 0.3 | 5 | | 250 | nA | |
| **DIGITAL CONTROL** | | | | | | | | | | |
| $V_{INL}$ | | | | | | | | 0.8 | V | Note 2 |
| $V_{INH}$ | | J, S | | | | | 3.0 | | V | |
| | | K, T | | | | | 2.4 | | V | |
| $I_{INL}$ or $I_{INH}$ | | All | | | | 10 | | 30 | μA | |
| $C_{IN}$ | | All | | | 3 | | | | pF | |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | | |
| $t_{transition}$ | | J, S | | | 700 | | | | ns | $V_{IN}$: 0 to 3.0 V |
| | | K, T | | | 700 | 1000 | | | ns | |
| $t_{open}$ | | All | | | 100 | | | | ns | |
| $t_{on(En)}$ | | J, S | | | 0.8 | | | | μs | $V_{EN}$: 0 to 3.0 V |
| | | K, T | | | | 1.5 | | | μs | |
| $t_{off(En)}$ | | J, S | | | 0.8 | | | | μs | |
| | | K, T | | | | 1 | | | μs | |
| "OFF" Isolation | | All | | | 70 | | | | dB | $V_{EN}$ = 0, $R_L$ = 200 Ω, $C_L$ = 3.0 pF, $V_S$ = 3.0 VRMS, f = 500 kHz |
| $C_S$ | | All | OFF | | 5 | | | | pF | |
| $C_{OUT}$ | | All | OFF | | 40 | | | | pF | |
| $C_{S-OUT}$ | | All | OFF | | 0.5 | | | | pF | |
| $C_{SS}$ Between Any Two Switches | | All | OFF | | 0.5 | | | | pF | |
| **POWER SUPPLY** | | | | | | | | | | |
| $I_{DD}$ (Standby) | | J, K | OFF | | 0.05 | 1 | | | mA | All Digital Inputs Low |
| | | S, T | OFF | | 0.05 | 1 | | 2 | mA | |
| $I_{SS}$ (Standby) | | J, K | OFF | | 0.05 | 1 | | | mA | |
| | | S, T | OFF | | 0.05 | 1 | | 2 | mA | |
| $I_{DD}$ | | J, K | ON | | 0.3 | 1 | | | mA | All Digital Inputs High |
| | | S, T | ON | | 0.3 | 1 | | 2 | mA | |
| $I_{SS}$ | | J, K | ON | | 0.05 | 1 | | | mA | |
| | | S, T | ON | | 0.05 | 1 | | 2 | mA | |

NOTES:

1. Specifications subject to change without notice.
2. A pull-up resistor, typically 1−2 kΩ is required to make the J and S versions compatible with TTL/DTL. The maximum value is determined by the output leakage curre of the driver gate when in the high state.

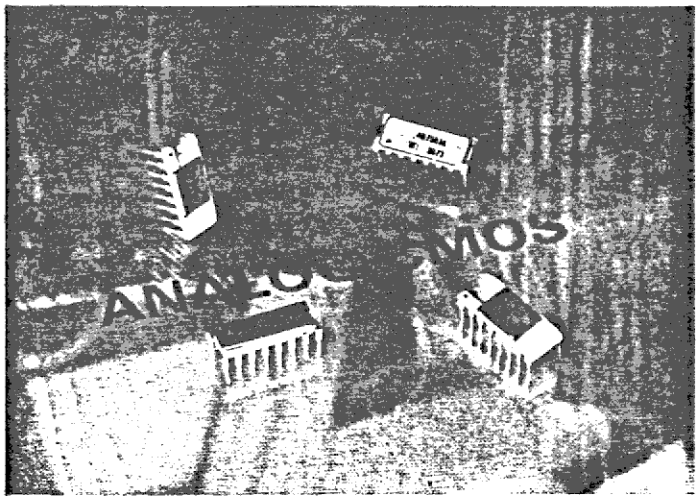
A2.29

ANALOG DEVICES

# CMOS 8 and 4 Channel Analog Multiplexers

# AD7501/AD7502

FEATURES
TTL/DTL/CMOS Compatible
Max. Quiescent Power Dissipation: 30μW
"ON" Resistance: 170Ω
Leakage Current: 200pA
Analog Signal Range: +12, -15V
Output Enable Control
Silicon Nitride Passivation



## GENERAL DESCRIPTION

The AD7501 is an 8 channel analog multiplexer which switches one output to one of 8 inputs depending on the state of 3 binary inputs. An "enable" control allows for disconnecting the output regardless of the digital input states. The AD7502 is identical to the AD7501 except it has 2 outputs switched to two of 8 inputs depending on 2 binary inputs.

Both units are specified over a ±10V range with a +12 to -15V operating range and without latch-up problems over the ±15V range (±15V supplies). The digital inputs are TTL/DTL and CMOS logic compatible.

An extremely low quiescent power dissipation (30μW) is achieved by combining unique CMOS (Complementary MOS) technology using the state-of-the-art double layer of interconnect and silicon nitride passivation techniques resulting in a highly reliable product.

The AD7501 and AD7502 are ideal for multiplexing single and differential analog data channels in data acquisition systems used in the process control and minicomputer industries. Their ultra low power dissipation also makes them an excellent choice in avionic and portable systems.

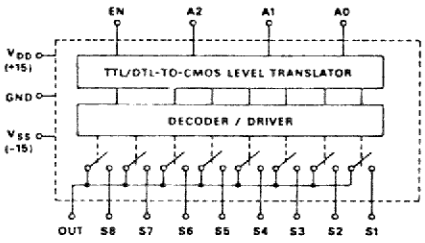
## TRUTH TABLES

| AD7501 | | | | |
|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $E_N$ | ON |
| L | L | L | H | 1 |
| L | L | H | H | 2 |
| L | H | L | H | 3 |
| L | H | H | H | 4 |
| H | L | L | H | 5 |
| H | L | H | H | 6 |
| H | H | L | H | 7 |
| H | H | H | H | 8 |
| X | X | X | L | NONE |

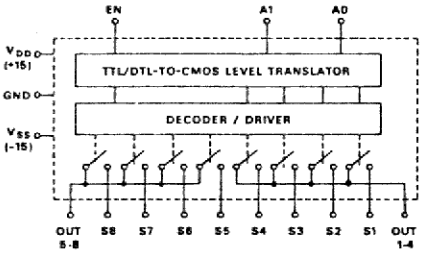
| AD7502 | | | |
|---|---|---|---|
| $A_1$ | $A_0$ | $E_N$ | ON |
| L | L | H | 1 & 5 |
| L | H | H | 2 & 6 |
| H | L | H | 3 & 7 |
| H | H | H | 4 & 8 |
| X | X | L | NONE |

## FUNCTIONAL DIAGRAMS

AD7501




AD7502






P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Telex: 924491 Cables: ANALOG NORWOODMASS

# SPECIFICATIONS ($V_{DD}$ = +15V, $V_{SS}$ = -15V unless otherwise noted)

| PARAMETER (NOTE 1) | | | SWITCH | $T_A$ (°C) | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | | | | | |
| $R_{ON}$ | | | ON | +25 | | 170 | 300 | Ω | -10V ≤ $V_S$ ≤ +10V<br>$I_S$ = 1mA |
| $R_{ON}$ vs. $V_S$ | | | ON | +25 | | 20 | | % | $V_S$ = -10V to +10V<br>$I_S$ = 1mA |
| $R_{ON}$ vs. Temperature | | | ON | | | 0.5 | | %/°C | |
| $\Delta R_{ON}$ between Switches | | | ON | +25 | | 4 | | % | $V_S$ = 0V<br>$I_S$ = 1mA |
| $R_{ON}$ vs. Temperature between Switches | | | ON | | | ±0.01 | | %/°C | |
| $I_S$ | | Commercial | OFF | +25 | | 0.2 | 2 | nA | $V_S$ = -10V, $V_{OUT}$ = +10V and $V_S$ = +10V, $V_{OUT}$ = -10V |
| | | | OFF | 0 to +75 | | | 50 | nA | |
| | | Military | OFF | +25 | | | 0.5 | nA | |
| | | | OFF | -55 to +125 | | | 50 | nA | |
| $I_{OUT}$ | AD7501 | Commercial | OFF | +25 | | 1.0 | 10 | nA | $V_S$ = -10V, $V_{OUT}$ = +10V and $V_S$ = +10V, $V_{OUT}$ = -10V "enable" low |
| | | | OFF | 0 to +75 | | | 250 | nA | |
| | | Military | OFF | +25 | | | 5 | nA | |
| | | | OFF | -55 to +125 | | | 250 | nA | |
| | AD7502 | Commercial | OFF | +25 | | 0.6 | 5 | nA | |
| | | | OFF | 0 to +75 | | | 125 | nA | |
| | | Military | OFF | +25 | | | 3 | nA | |
| | | | OFF | -55 to +125 | | | 125 | nA | |
| $\|I_{OUT} - I_S\|$ | | | ON | +25 | | | 5 | nA | $V_S$ = 0 |
| DIGITAL CONTROL | | | | | | | | | |
| $V_{INL}$ | | | | +25 | | | 0.8 | V | |
| $V_{INH}$ | AD7501J<br>AD7502J | | | +25 | 4 | | | V | SEE NOTE 2 |
| | AD7501K<br>AD7501S<br>AD7502K<br>AD7502S | | | +25 | 2.4 | | | V | |
| $I_{INL}$ or $I_{INH}$ | | Commercial | | +25 | | 10 | | nA | |
| | | | | 0 to +75 | | 100 | | nA | |
| | | Military | | -55 to +125 | | 1 | | µA | |
| $C_{IN}$ | | | | +25 | | 3 | | pF | |
| DYNAMIC CHARACTERISTICS | | | | | | | | | |
| $T_{ON}$ | | | | +25 | | 0.8 | | µs | SEE TEST |
| $T_{OFF}$ | | | | +25 | | 0.8 | | µs | CIRCUIT 2 |
| $C_S$ | | | OFF | +25 | | 5 | | pF | |
| $C_{OUT}$ | | | OFF | +25 | | 30 | | pF | |
| $C_{S,OUT}$ | | | OFF | +25 | | 0.5 | | pF | |
| $C_{SS}$ between any two switches | | | OFF | +25 | | 0.5 | | pF | |
| POWER SUPPLY | | | | | | | | | |
| $I_{DD}$ (Quiescent) | | | OFF | +25 | | 0.01 | 100 | µA | ALL DIGITAL |
| $I_{SS}$ (Quiescent) | | | OFF | +25 | | 0.01 | 100 | µA | INPUTS LOW |
| $I_{DD}$ | | | ON | +25 | | 0.2 | 0.5 | mA | ALL DIGITAL |
| $I_{SS}$ | | | ON | +25 | | 0.01 | 100 | µA | INPUTS HIGH |

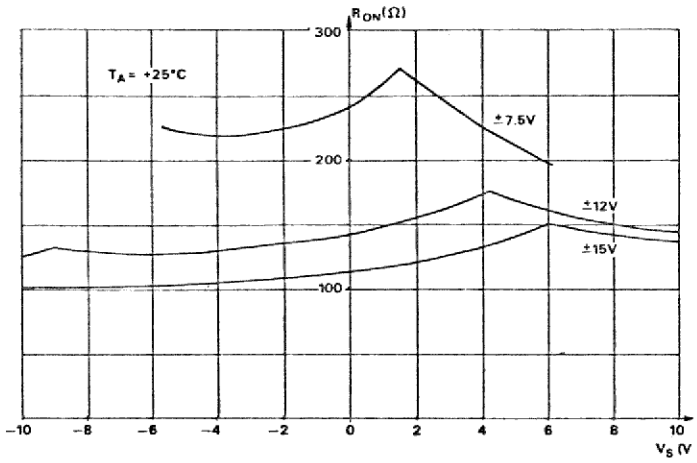
NOTE 1: See "Terminology" on page 6.

NOTE 2: A pull-up resistor, typically 1-2kΩ, is required to make the AD7501J and AD7502J compatible with TTL/DTL levels. The maximum value is determined by the output leakage current of the driver gate when in the high state.

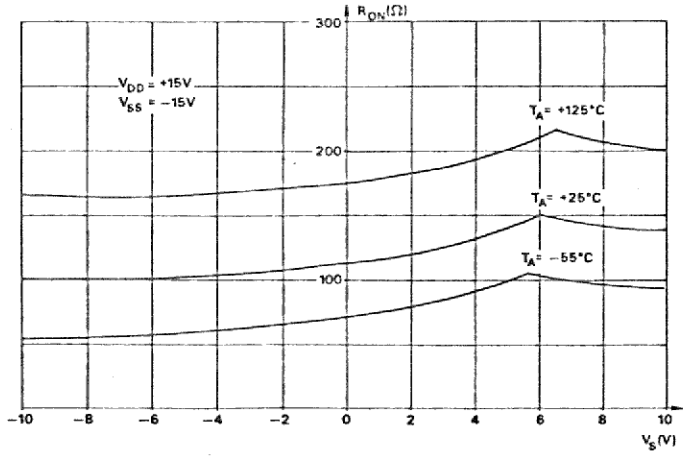
Specifications subject to change without notice.

## TYPICAL PERFORMANCE CURVES

### 1. $R_{ON}$ AS A FUNCTION OF SWITCH VOLTAGE ($V_S$)

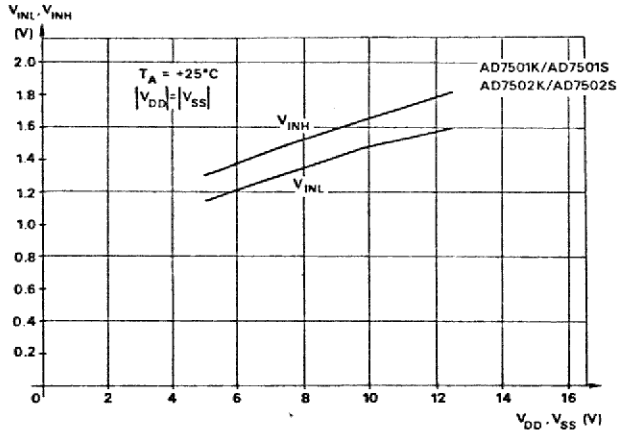



*At Different Power Supplies*

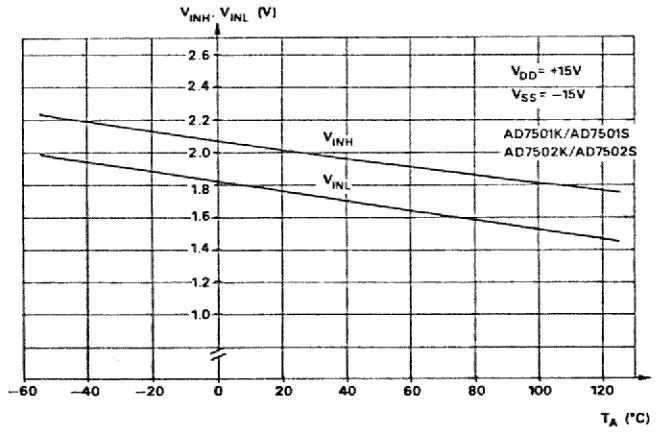



*At Different Temperatures*

### 2. DIGITAL THRESHOLD VOLTAGE ($V_{INH}$, $V_{INL}$)

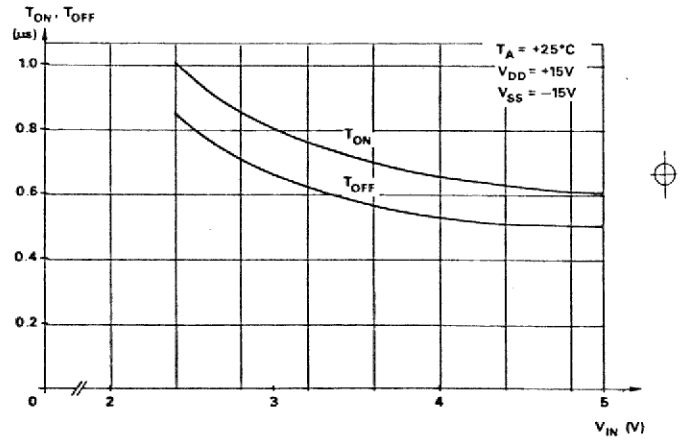



*Vs. Power Supply*



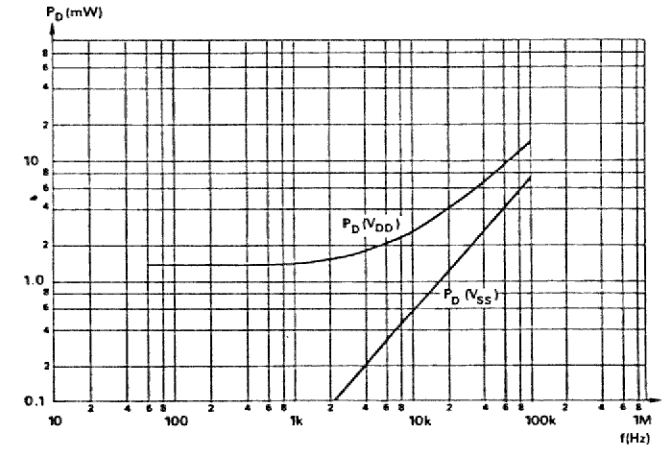

*Vs. Temperature*

### 3. $T_{ON}$, $T_{OFF}$




*Vs. Digital Input Voltage*

### 4. POWER DISSIPATION

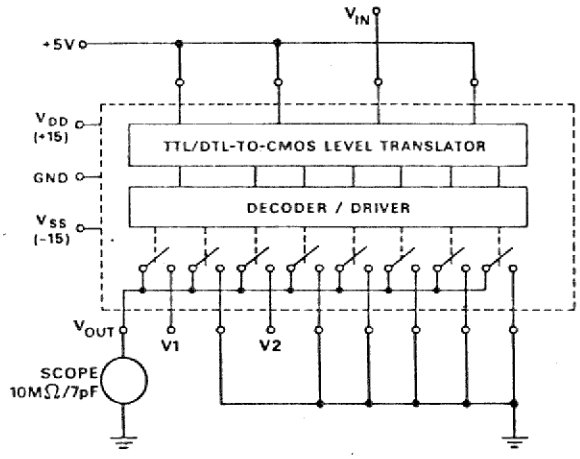


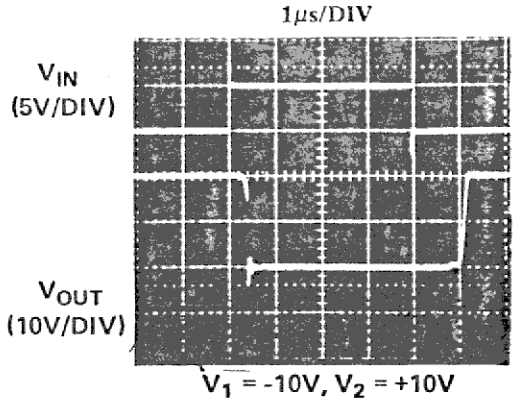

*Vs. Logic Frequency (50% Duty Cycle)*

TYPICAL PERFORMANCE CURVES (Continued)

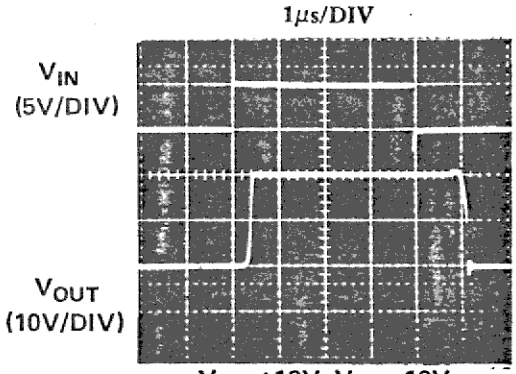
## SWITCHING CHARACTERISTICS

### TEST CIRCUIT 1




$V_1$ = -10V, $V_2$ = +10V




$V_1$ = +10V, $V_2$ = -10V

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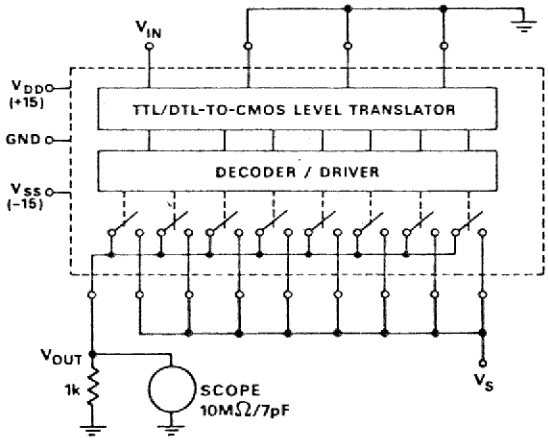
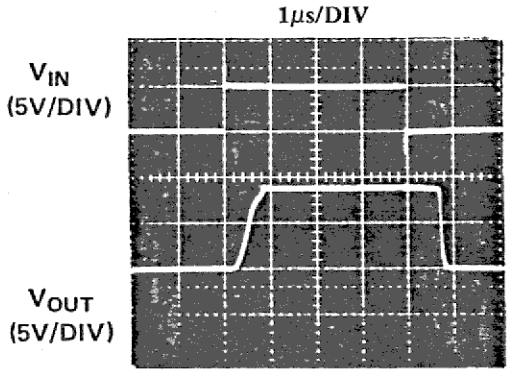
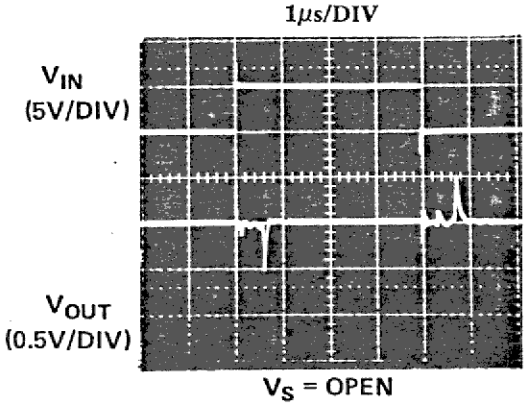
### TEST CIRCUIT 2

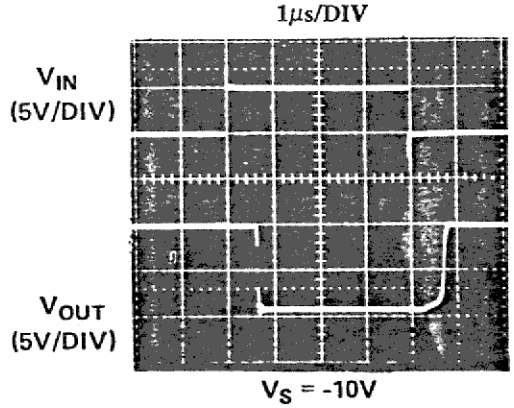



$V_S$ = +10V




$V_S$ = OPEN




$V_S$ = -10V

## APPLICATIONS

The basic applications for the AD7501 and AD7502 are in single and differential signal multiplexing and demultiplexing circuits.

Most data acquisition systems have multiple data inputs coming from various transducers, signal conditioners, etc. This analog data is normally converted into digital format using A/D converters for further processing. Multiplexing the various data channels into one channel reduces the number of digital conversion products needed and saves space, power and money.

Figure 1 shows how eight data channels are reduced to a single channel which subsequently is converted into digital language using a sample/hold amplifier and an A/D converter. Additional channels can be multiplexed by using two or more AD7501's using the "enable" line to disconnect the output of those multiplexers which are not addressed.

Figure 2 shows the AD7502 multiplexing balanced data channels. Using an instrumentation amplifier such as the AD520 converts the differential signal into a single ended output. A sample/hold amplifier and A/D converter can subsequently be used for digitizing the analog information.

The AD7501/AD7502 are designed for the "analog world" where the standard power supplies are ±15V and the signal range is ±10V coming from op amps or other signal sources. The digital interface does not need any additional parts (K and S versions) and is directly compatible with standard TTL/DTL and CMOS gates, simplifying the circuit design.

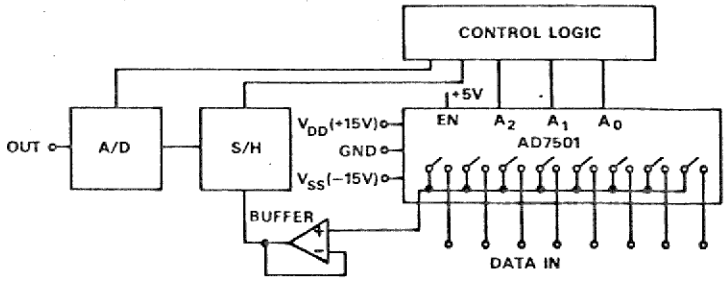



*Figure 1. 8-Channel Data Acquisition System*

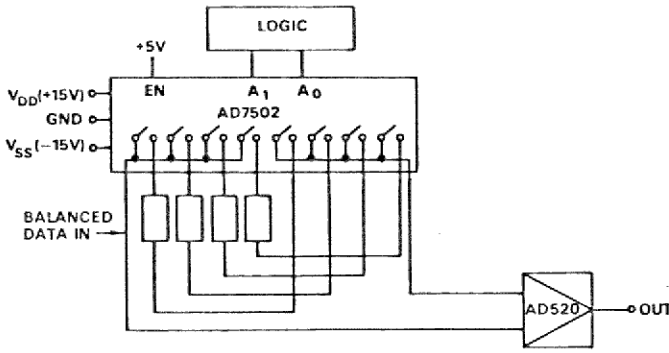
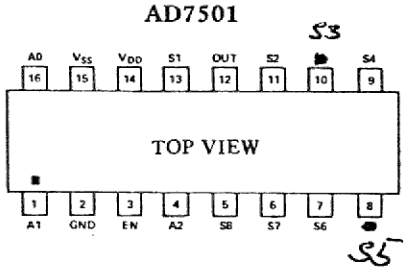


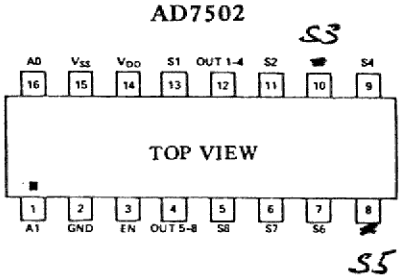

*Figure 2. 4-Channel Differential Multiplexer*

## PIN CONFIGURATION

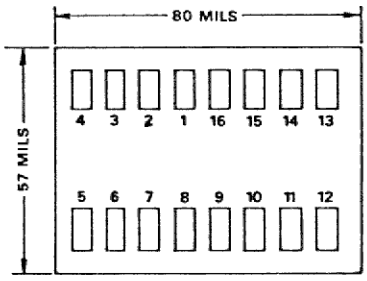
**AD7501**




**AD7502**




## BONDING DIAGRAM




NOTE: Please consult the factory for additional chip information.

## ABSOLUTE MAXIMUM RATINGS

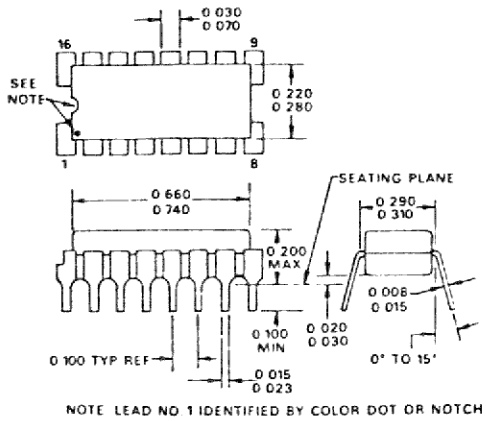
| | |
|---|---|
| $V_{DD}$ – (to Gnd) | +17V |
| $V_{SS}$ – (to Gnd) | -17V |
| Switch Voltage (to $V_{SS}$) | +27V |
| Switch Current | 10mA |
| Digital Input Voltage Range | $V_{DD}$ to $V_{SS}$ |
| Power Dissipation (package) | |
| up to +75°C | 450mW |
| derates above +75°C at | 6mW/°C |
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |

**CAUTION:**

1. Do not apply voltages higher than $V_{DD}$ and $V_{SS}$ on any other terminal, especially when $V_{SS} = V_{DD} = 0V$ all other pins should be at 0V.
2. The digital control inputs are zener protected. However, permanent damage can occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

## OUTLINE DIMENSIONS

16 PIN CERAMIC DIP




## TERMINOLOGY

| | |
|---|---|
| $R_{ON}$: | Ohmic resistance between the output and an addressed input. |
| $R_{ON}$ vs. Temperature: | $R_{ON}$ drift over the temperature range. |
| $\Delta R_{ON}$ between Switches: | Difference between the $R_{ON}$ of any two switches. |
| $R_{ON}$ vs. Temperature between Switches: | Difference between the $R_{ON}$ drift of any two switches. |
| $I_S$: | Current at any switch input S1 through S8. This is a leakage current when the switch is open. |
| $I_{OUT}$: | Current at the output. This is a leakage current when all switches are open (enable low). |
| $I_{OUT} - I_S$: | Difference between the current going into terminal "S" and the current going out of terminal "out" when terminal "S" is addressed. |
| $V_{INL}$: | Digital threshold voltage for the low state. |
| $V_{INH}$: | Digital threshold voltage for the high state. |
| $C_S$: | Capacitance between any open terminal "S" and ground. |
| $C_{OUT}$: | Capacitance between the output terminal and ground with all switches open (enable low). |
| $C_{S\text{-}OUT}$: | Capacitance between any open terminal "S" and the output terminal. |
| $C_{SS}$: | Capacitance between any two "S" terminals. |

## ORDERING INFORMATION

| | |
|---|---|
| AD7501J: | 0 – +75°C |
| AD7501K: | 0 – +75°C |
| AD7501S: | -55°C – +125°C |
| AD7502J: | 0 – +75°C |
| AD7502K: | 0 – +75°C |
| AD7502S: | -55°C – +125°C |