DANSK DATA ELEKTRONIK

ID-7017 DIGITAL/ANALOG CONVERSION MODULE

for the

ID-7000 MICROPROCESSOR SYSTEM

June 1976

Generatorvej 6A
DK-2730 Herlev
Denmark

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ID-7o17 DIGITAL/ANALOG CONVERTION MODULE.

1. Introduction.

This module is used for generation of analog output signals from the ID-7ooo microprocessor system. A maximum of 4 different analog outputs can be generated by the module. The monolithic D/A converters on the module- available in 8 bit and lo bit versions - have a 6 usec coversion time. The module is available in two versions for output range 0-+10 V or 0-÷10V.

The module only works in ID-7ooo systems with +/÷15V power supply.

Fig. 1 shows a blocked schematic of the module.Appendix 1 is a complete diagram. Appendix 2 contains datasheets for the analog components on the board.

2. Description.

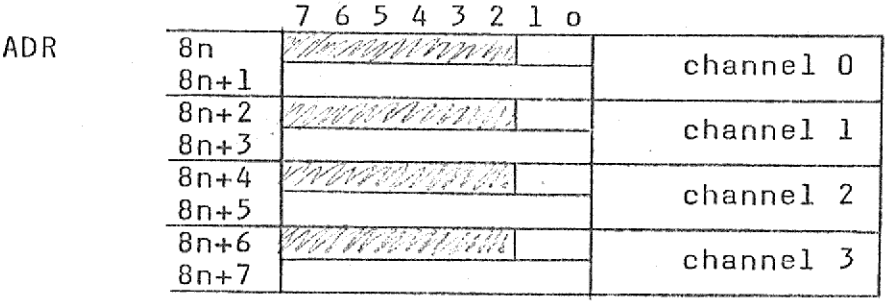
This section containa a description of the module from a programming point of view.

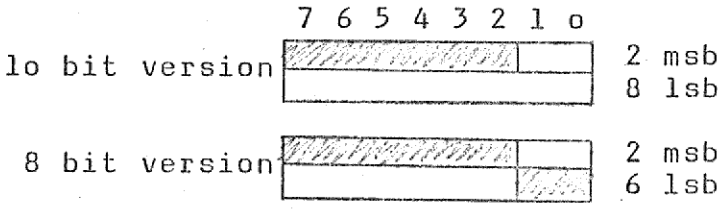
2.1 Addressing.

The module uses 8 consecutive addresses of the possible 256 addresses for I/O-units.The address of the module is set by a 5 bit switch register on the module.

2.2 Data output.

Data to the module is always sent in two parts. First the two most significant bits, and then the 6 (in 8 bit version) or 8 (in lo bit version) least significant bits. Data is interpreted as a true binary number without sign-bit.





msb = most significant bits
lsb = least significant bits

The analog outputs are not changed if the 2 most significant bits are altered. The change in analog value occurs shortly after the 8 (6) least significant bits are sent to the module.

2.3 Vent.

The module makes use ot the $\overline{\text{vent}}$ signal to delay the microcomputer in order to provide the necessary setup time for data to the D/A-chips. Each time the module is addressed the microprocessor id delayed 5 usec.

3. Connections.

At the top-connector the different signals are found as follow:

pin F	channel 0
pin 5	analog ground
pin N	channel 1
pin 1o	analog ground
pin Z	channel 2
pin 21	analog ground
pin $\overline{\text{m}}$	channel 3
pin 31	analog ground
pin $\overline{\text{f}}$	+15V
pin $\overline{\text{h}}$	-15V

4. Adjustment.

The datasheet for the digital-analog converter AD7522 (in appendix 2) describes the adjustment of the converter.

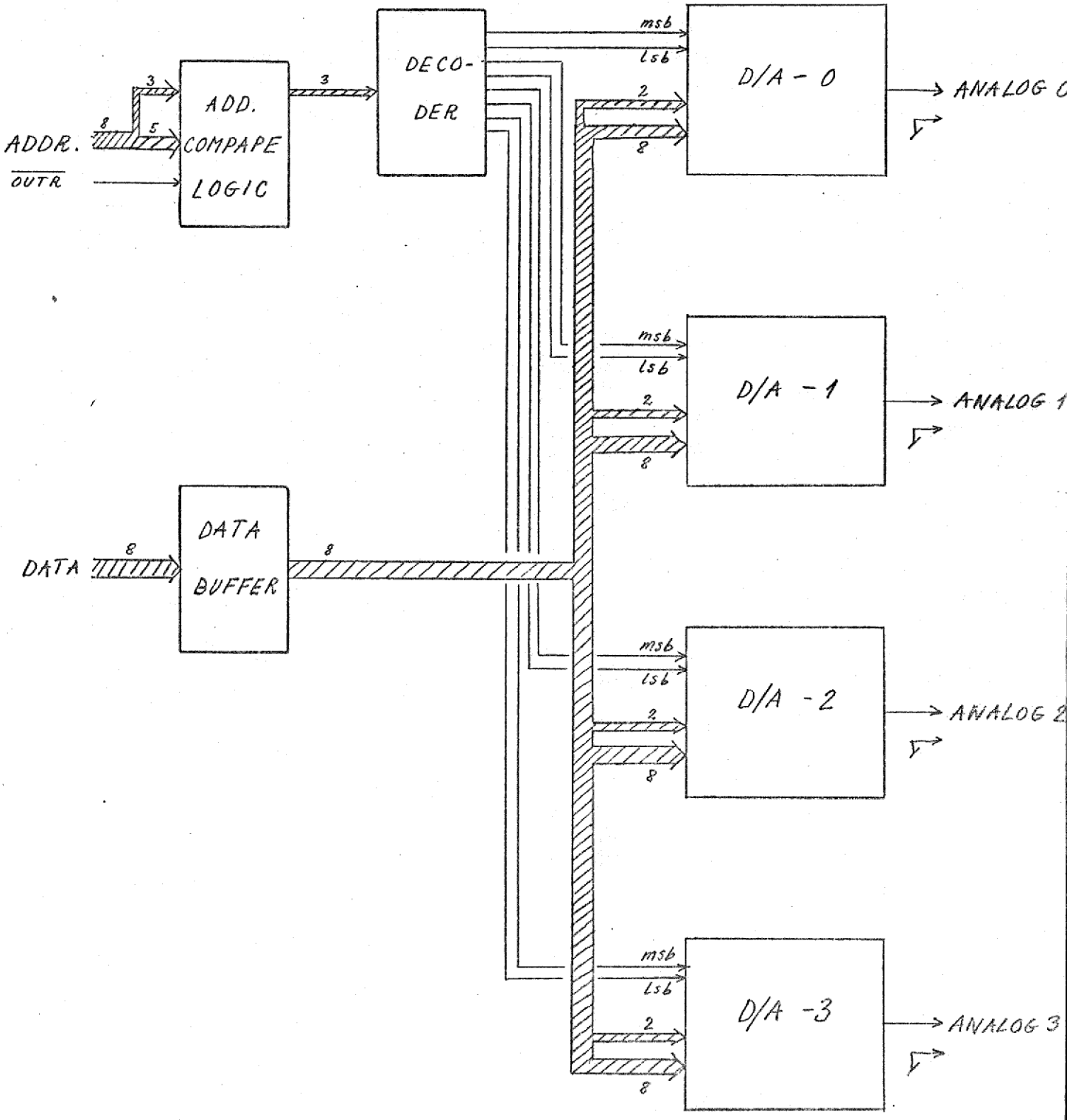
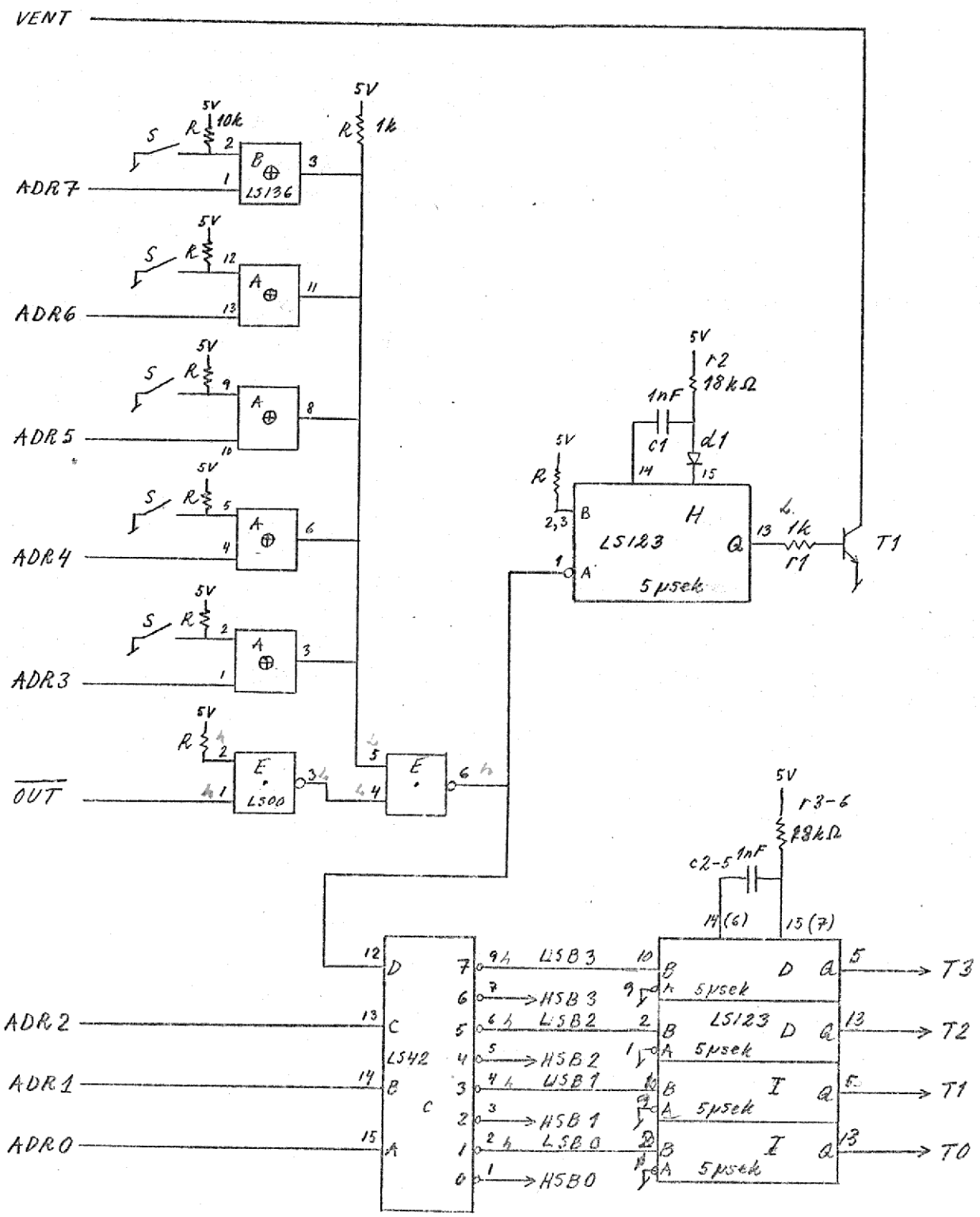
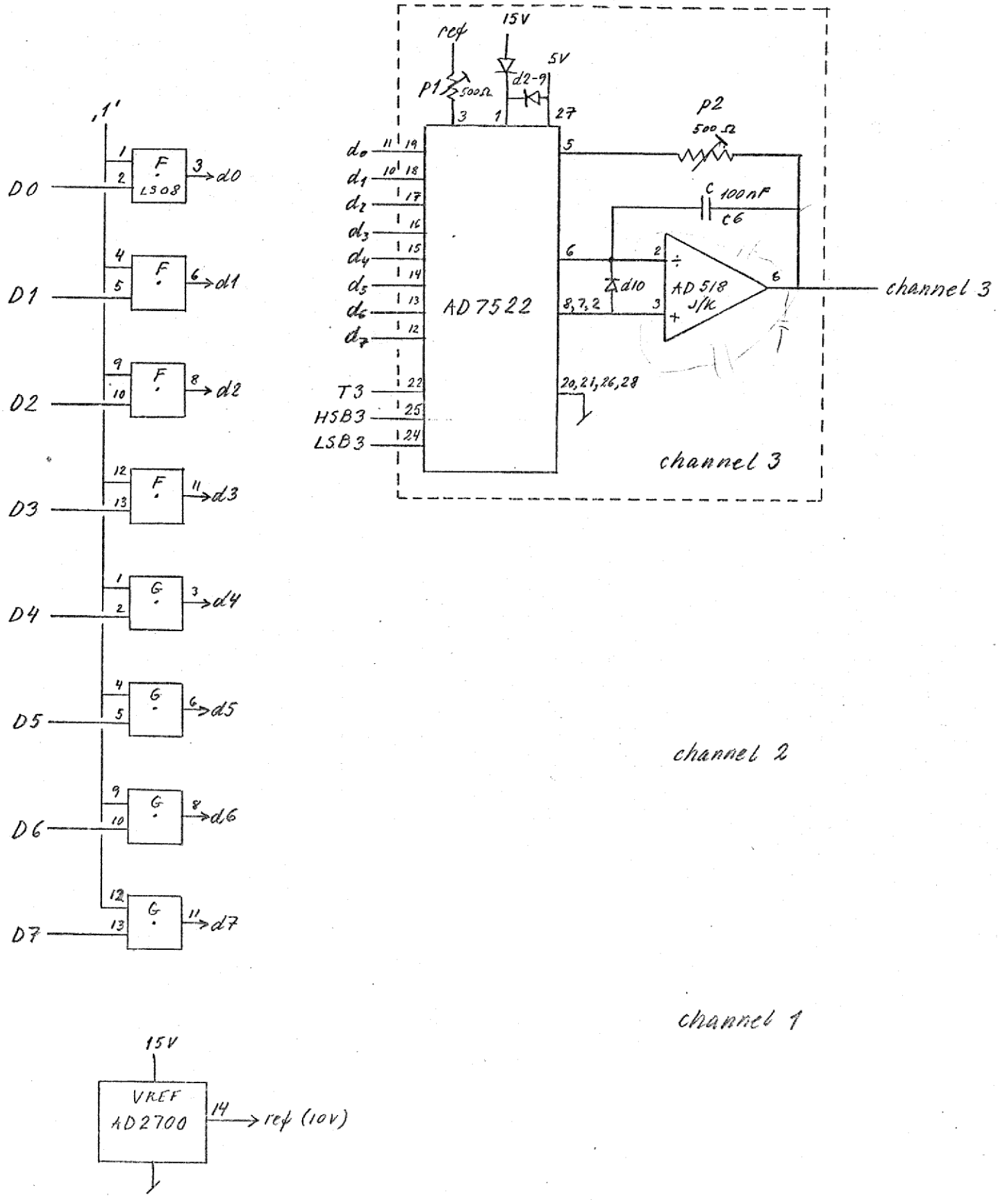
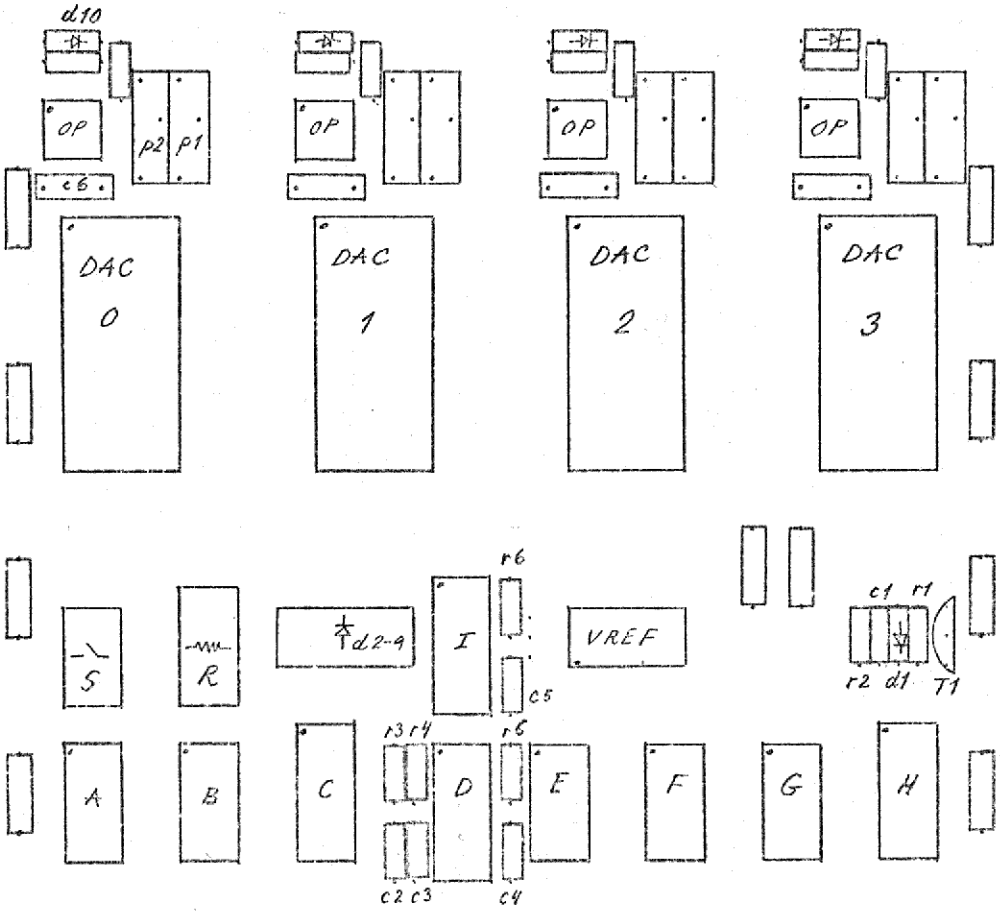

ADDR.
OUTR
3
8
5
ADD. COMPAPE LOGIC
3
DECO-DER
msb
lsb
2
8
D/A - 0
ANALOG 0
D/A - 1
ANALOG 1
DATA
8
DATA BUFFER
8
D/A -2
ANALOG 2
D/A -3
ANALOG 3

Fig. 1


VENT
5V
R 10k
R 1k
S
ADR7
ADR6
ADR5
ADR4
ADR3
OUT
LS136
LS00
5V
r2 18kΩ
1nF
c1
d1
R
H
LS123
5 µsek
r1 1k
T1
5V
r3-6 18kΩ
c2-5 1nF
LSB3
HSB3
LSB2
HSB2
LSB1
HSB1
LSB0
HSB0
ADR2
ADR1
ADR0
LS42
LS123
5 µsek
T3
T2
T1
T0


'1'
D0
D1
D2
D3
D4
D5
D6
D7
F
LS08
G
d0
d1
d2
d3
d4
d5
d6
d7
ref
15V
5V
P1
500Ω
d2-9
P2
500 Ω
C 100nF
C6
AD7522
AD518
J/K
d10
T3
HSB3
LSB3
20,21,26,28
channel 3
channel 2
channel 1
channel 0
VREF
AD2700
14
ref (10V)


d10
OP
p2
p1
c6
DAC
0
DAC
1
DAC
2
DAC
3
S
R
d2-9
I
r6
c5
VREF
c1
r1
r2
d1
T1
A
B
C
r3
r4
D
r6
E
F
G
H
c2
c3
c4

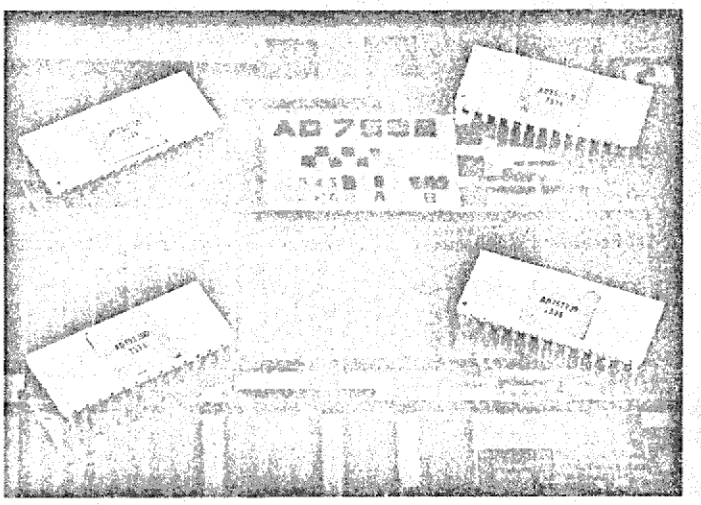
ANALOG DEVICES

CMOS 10-Bit, Buffered Multiplying D/A Converter

AD7522

FEATURES

- 10-Bit Resolution
- 8, 9, & 10-Bit Linearity
- Microprocessor Compatible
- Double Buffered Inputs
- Serial or Parallel Loading
- DTL/TTL/CMOS Direct Interface
- Nonlinearity Tempco: 2ppM of FSR/°C
- Gain Tempco: 10ppM of FSR/°C
- Very Low Power Dissipation
- Very Low Feedthrough



GENERAL DESCRIPTION

The AD7522 is a monolithic CMOS 10-bit multiplying D/A converter, with an input buffer and a holding register, allowing direct interface with microprocessors. Most applications require the addition of only an operational amplifier and a reference voltage.

The key to easy interface to a data bus is the AD7522's ability to load the input buffer in two bytes (an 8-bit and a 2-bit byte), and subsequently move this data to a holding register, where the digital word is converted into an analog current or voltage (with external operational amplifier). The input loading of either 8 or 10 bits can be done in a parallel or serial mode.

The AD7522 is packaged in a 28-pin DIP, and operates with a +15V main supply at 2mA max, and a logic supply of +5V for TTL interface, or +10 to +15V for CMOS interface.

A thin film on high density CMOS process, using silicon nitride passivation, ensures high reliability and excellent stability.

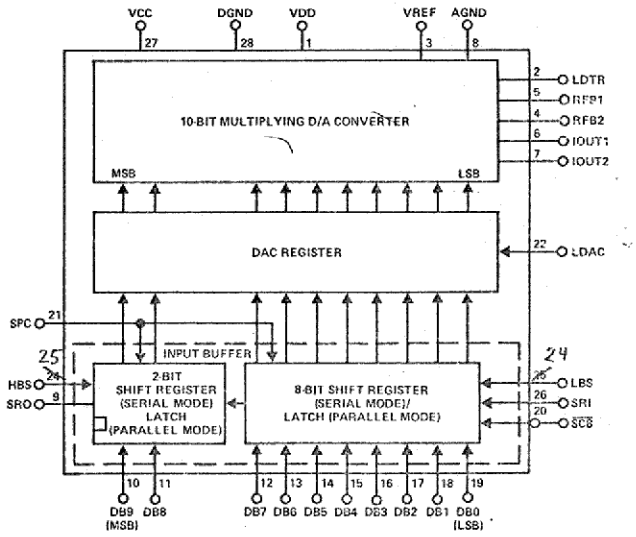
ORDERING INFORMATION

Nonlinearity	Temperature Range	
	0°C to +75°C	−55°C to +125°C
0.2% FSR (8-Bit)	AD7522JD AD7522JN	AD7522SD
0.1% FSR (9-Bit)	AD7522KD AD7522KN	AD7522TD
0.05% FSR (10-Bit)	AD7522LD AD7522LN	AD7522UD

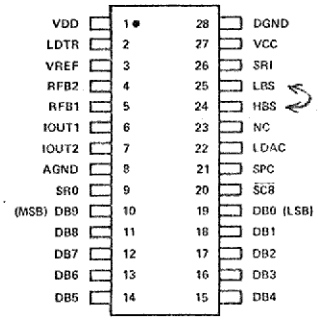
PACKAGE IDENTIFICATION

Suffix "D": Ceramic DIP Package
Suffix "N": Plastic DIP Package

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



OMBYTTET!

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: (617) 329-4700 Telex: 924491
Cable: ANALOG NORWOODMASS

SPECIFICATIONS (VDD = +15V, VCC = +5V, VREF = ±10V, TA = +25°C unless otherwise noted)

PARAMETER[1]	VERSION	TA = 25°C			OVER SPECIFIED TEMP. RANGE		UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	MAX		
STATIC ACCURACY								SC8 = "1"
Resolution	All	10			10		Bits	
Differential Nonlinearity	J			±0.2			% FSR	
	S			±0.2		±0.2	% FSR	
	K			±0.1			% FSR	
	T			±0.1		±0.1	% FSR	
	L			±0.05			% FSR	
	U			±0.05		±0.05	% FSR	
Nonlinearity	J			±0.2			% FSR	
	S			±0.2		±0.2	% FSR	
	K			±0.1			% FSR	
	T			±0.1		±0.1	% FSR	−10V ≤ VREF ≤ +10V
	L			±0.05			% FSR	
	U			±0.05		±0.05	% FSR	
Nonlinearity Tempco[2]	J, K, L		±1			±2	ppm FSR/°C	
	S, T, U					±2	ppm FSR/°C	
Gain Error	J, K, L		±0.3				% Reading	
Gain Error Tempco[2]	J, K, L		±5			±10	ppm of Reading/°C	
	S, T, U					±10	ppm of Reading/°C	
Output Leakage Current at IOUT1 or IOUT2	All					200	nA	IOUT1: DB0 through DB9 = 0 IOUT2: DB0 through DB9 = 1
Power Supply Rejection	J, K, L		50				ppm of Reading/%	
AC ACCURACY								
Feedthrough Error[2]	All		1	10			mV p-p	VREF = 20V p-p; 10 kHz
Output Current Settling Time	J, K, L		500				ns	To 0.05% of FSR for a FSR Step. HBS and LBS Low to High LDAC = 1
REFERENCE INPUT								
Input Resistance	All	5		20			kΩ	
ANALOG OUTPUT								
Output Capacitance								
C_{OUT1}	J, K, L		120				pF	All Data Inputs High
C_{OUT2}	J, K, L		40				pF	
C_{OUT1}	J, K, L		40				pF	All Data Inputs Low
C_{OUT2}	J, K, L		120				pF	
DIGITAL INPUTS								
Low State Threshold	J, K, L			0.8			V	
	S, T, U			0.8		0.8	V	
High State Threshold	J, K, L	2.4					V	
	S, T, U	2.4			2.4		V	
Input Current	J, K, L		1				μA	
LDAC Pulse Width Requirement[3]	All	5					μs	LDAC: 0 to +3V
HBS, LBS Pulse Width Requirement[3]	All	5					μs	HBS, LBS: 0 to +3V
Serial Clock Frequency[3]	All			200			kHz	

Notes
[1] Specifications subject to change without notice.
[2] Guaranteed by design. Not tested.
[3] Sample tested.

SPECIFICATIONS (continued)

PARAMETER[1]	VERSION	TA = +25°C			OVER SPECIFIED TEMP. RANGE		UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	MAX		
POWER REQUIREMENTS								
IDD	All			2			mA	
ICC	All			2			mA	

ABSOLUTE MAXIMUM RATINGS

VREF to GND . . . . . ±25V
VDD to GND . . . . . +17V
VCC to GND . . . . . +17V
VCC to VDD . . . . . +0.4V
IOUT1, IOUT2 . . . . . ±5 mA
Operating Temperature . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C

Power Dissipation (Package)
Up to +50°C:
Plastic (Suffix N) . . . . . 1200 mW
Ceramic (Suffix D) . . . . . 1000 mW
Derate Above +50°C by
Plastic (Suffix N) . . . . . 12 mW/°C
Ceramic (Suffix D) . . . . . 10 mW/°C
Digital Input Voltage Range . . . . . VDD to GND

CAUTION:

1. Do not apply voltages higher than VCC to SRO.
2. Do not apply voltages higher than VDD or less than GND to any other input/output terminal except VREF, RFB1 or RFB2.
3. The digital control inputs are zener protected, however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
4. VCC should never exceed VDD by more than 0.4V, especially during power ON or OFF sequencing.

Terminology

RESOLUTION

Value of the LSB. For example, a unipolar n-bit converter has a resolution of (2^{-n}) (VREF). A bipolar n-bit converter has a resolution of $[2^{-(n-1)}]$ [VREF]. Resolution in no way implies linearity.

NONLINEARITY

Error contributed by deviation of the DAC transfer function from a best straight line function. For a multiplying DAC, the nonlinearity should be independent of the sign or magnitude of VREF. Nonlinearity is normally expressed as a percentage of full scale range (% FSR).

DIFFERENTIAL NONLINEARITY

In a DAC, differential linearity error describes the variation in the analog output transitions between adjacent pairs of digital input numbers, over the full range of digital inputs. If each transition is equal to its neighbors' (i.e., 1 LSB), the "differential nonlinearity" is zero. If a transition differs from the ideal by more than 1 LSB, a D/A converter can be "nonmonotonic." A specific maximum differential nonlinearity of ±1/2LSB at +25°C ensures that monotonic behavior will exist over a tangible range of temperatures.

GAIN

The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is a linear error which can be externally adjusted. (See gain adjustment on page 6.)

OUTPUT LEAKAGE CURRENT

Current which appears on the OUT1 terminal when the DAC register is loaded with all "0's" or on the OUT2 terminal when the DAC register is loaded with all "1's."

Pin Function Description

PIN	MNEMONIC	DESCRIPTION
1	VDD	+15V (nominal) Main Supply.
2	LDTR	R-2R Ladder Termination Resistor. Normally grounded for unipolar operation or terminated at IOUT2 for bipolar operation.
3	VREF	Reference Voltage Input. Since the AD7522 is a multiplying DAC, VREF may vary over the range of ±10V.
4	RFB2	Rfeedback ÷ 2; gives full scale equal to VREF/2.
5	RFB1	Rfeedback, used for normal unity gain (at full scale) D/A conversion.
6	IOUT1	DAC Current OUT-1 Bus. Normally terminated at virtual ground of output amplifier.
7	IOUT2	DAC Current OUT-2 Bus, terminated at ground for unipolar operation, or virtual ground of op amp for bipolar operation.
8	AGND	Analog Ground. Back gate of DAC N-channel SPDT current steering switches.
9	SRO	Serial Output. An auxiliary output for recovering data in the input buffer.
10	DB9	Data Bit 9. Most significant parallel data input.
11	DB8	Data Bit 8.
12	DB7	Data Bit 7.
13	DB6	Data Bit 6.
14	DB5	Data Bit 5.
15	DB4	Data Bit 4.
16	DB3	Data Bit 3.
17	DB2	Data Bit 2.
18	DB1	Data Bit 1.
19	DB0	Data Bit 0. Least significant parallel data input.
20	$\overline{SC8}$	8-Bit Short Cycle Control. When in serial mode, if $\overline{SC8}$ is held to logic "0," the two least significant input latches in the input buffer are bypassed to provide proper serial loading of 8-bit serial words. If $\overline{SC8}$ is held to logic "1," the AD7522 will accept a 10-bit serial word. Data bits 0(LSB) and $\overline{DB1}$ are in a parallel load mode when $\overline{SC8}$ = 0, and should be tied to a logic low state to prevent false data from being loaded.

Note 1

PIN	MNEMONIC	DESCRIPTION
21	SPC	Serial/Parallel Control. If SPC is a logic "0," the AD7522 will load parallel data appearing on DB0 through DB9 into the input buffer when the appropriate strobe inputs are exercised (see HBS and LBS). If SPC is a logic "1," the AD7522 will load serial data appearing on Pin 26 into the input buffers. Each serial data bit must be "strobed" into the buffer with the HBS and LBS.
22	LDAC	Load DAC: When LDAC is a logic "0," the AD7522 is in the "hold" mode, and digital activity in the input buffer is locked out. When LDAC is a logic "1," the AD7522 is in the "load" mode, and data in the input buffer loads the DAC register.
23	NC	No Connection.
24	HBS	High Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB9 (MSB) and DB8 data inputs will be "clocked" into the input buffer on the positive going edge of HBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edges of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
25	LBS	Low Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB0 (LSB) through DB7 inputs will be "clocked" into the input buffer on the positive going edge of the LBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edge of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
26	SRI	Serial Input.

Pin Function Description cont'd

PIN	MNEMONIC	DESCRIPTION
27	VCC	Logic Supply. If +5V is applied, all digital inputs/outputs are TTL compatible. If +10V to +15V is applied, digital inputs/outputs are CMOS compatible.

PIN	MNEMONIC	DESCRIPTION
28	DGND	Digital Ground.

Note 1: Logic "1" applied to a data bit steers that bit's current to the IOUT1 terminal.

DAC Circuit Description

GENERAL CIRCUIT INFORMATION

The AD7522's DAC functional block consists of a highly stable Silicon Chromium thin film R-2R ladder, and ten SPDT N-channel current steering switches. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used — that is, the binarily weighted currents are switched between the IOUT1 and IOUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

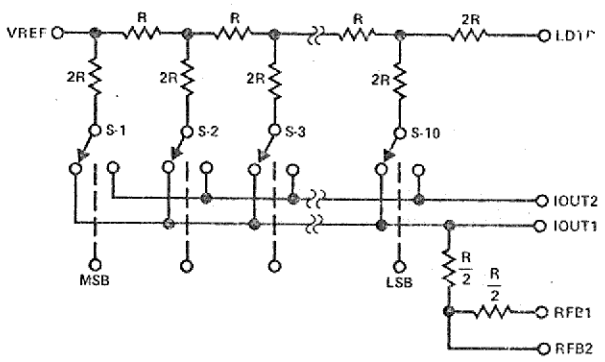


Figure 1. DAC Functional Diagram

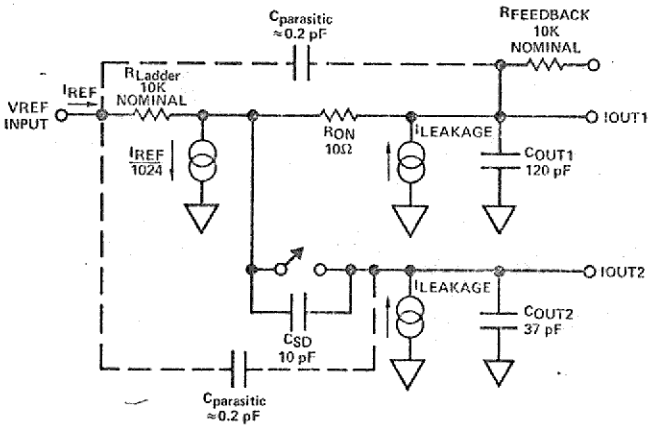


Figure 2. Equivalent Circuit (Shown for all Digital Inputs High)

EQUIVALENT CIRCUIT

The DAC equivalent circuit is shown in Figure 2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the $I_{REF}/1024$ current source represents the 1LSB of current lost through the ladder termination resistor to ground. The C_{OUT1} and C_{OUT2} output capacitances are as shown when the DAC latches feed the DAC with all "1's." If the DAC latches are loaded with all "0's," C_{OUT1} is 37 pF, while C_{OUT2} is 120 pF. In addition, C_{SD} is shunted by 10 ohms, and the 10 ohm R_{ON} in IOUT1 is replaced by a C_{SD} of 10 pF. When fast amplifiers are used, it will be necessary to provide phase compensation (in the form of feedback capacitance) to cancel the pole formed by $R_{FEEDBACK}$ and C_{OUT} if stability is to be maintained.

UNIPOLAR OPERATION

Figure 3 shows the analog circuit connections required for unipolar operation. The input code/output voltage relationship is shown in Table 1.

Zero Offset Adjustment

1. Adjust the op amp's offset potentiometer for < 1 mV on the amplifier junction. (Each millivolt of amplifier V_{OS} causes ±0.66 mV of differential nonlinearity which adds to the ladder nonlinearity.)

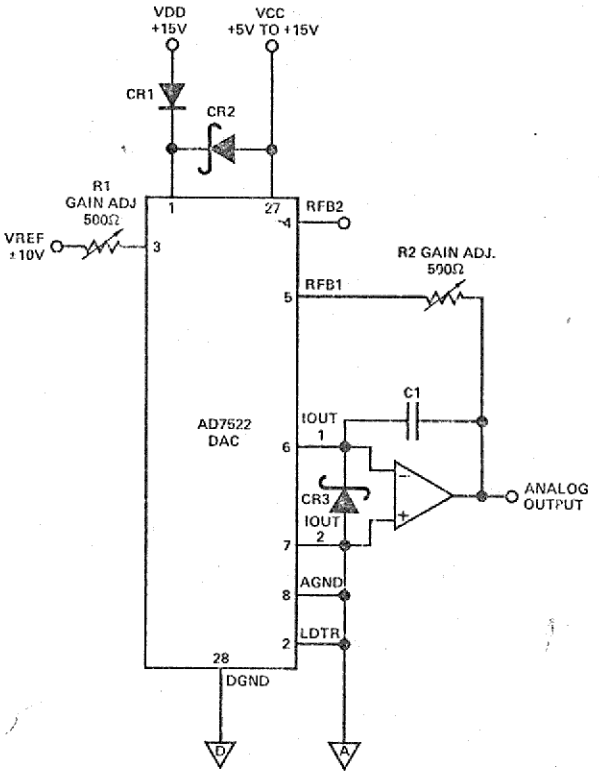


Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

Gain Adjustment

1. Set R1 and R2 to 0Ω. Load the DAC register with all "1's."
2. If analog out is greater than −VREF, increase R1 for required full scale output. If analog out is less than −VREF, increase R2 for required full scale output.

TABLE 1
UNIPOLAR CODE TABLE

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-VREF\ (1 - 2^{-10})$
1000000001	$-VREF\ (1/2 + 2^{-10})$
1000000000	−VREF/2
0111111111	$-VREF\ (1/2 - 2^{-10})$
0000000001	$-VREF\ (2^{-10})$
0000000000	0

TABLE 2
BIPOLAR CODE TABLE

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-VREF\ (1 - 2^{-9})$
1000000001	$-VREF\ (2^{-9})$
1000000000	0
0111111111	$VREF\ (2^{-9})$
0000000001	$VREF\ (1 - 2^{-9})$
0000000000	VREF

BIPOLAR OPERATION

Figure 4 shows the analog circuit connections required for bipolar operation. The input code/output voltage relationship is shown in Table 2.

Zero Offset Adjustment

1. Adjust the offset potentiometer of amplifier A1 and A2 for < 1 mV on the respective summing junctions. If the analog out for code 1000000000 is not zero, sum current into or out of the summing junction of A1 for 0V at analog out.

Gain Adjustment

1. Load the DAC register with all "0's." Set R1 and R2 to 0Ω.
2. If analog out is greater than +VREF, increase R2 until it reads precisely +VREF. If analog out is less than +VREF, increase R1 until it reads precisely VREF.

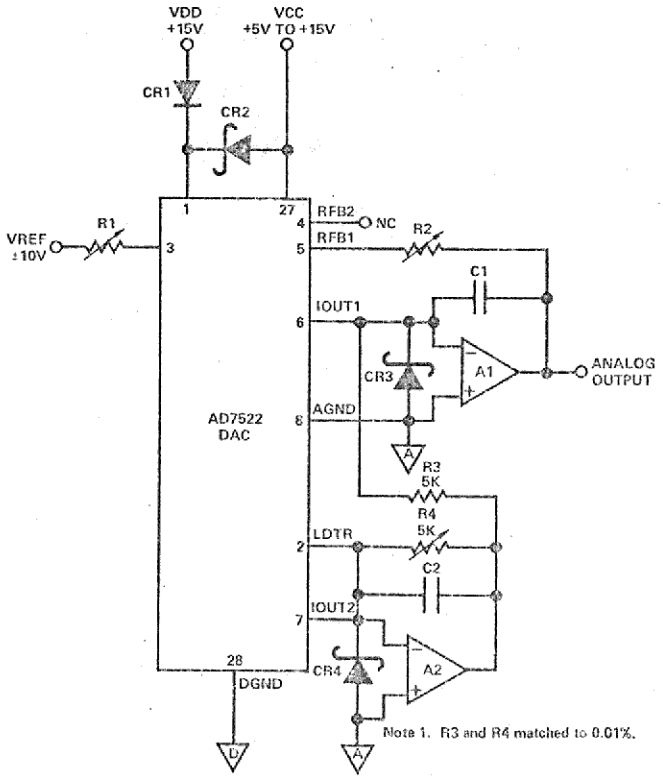


Figure 4. Bipolar Operation

SINGLE BYTE PARALLEL LOADING

Figure 5 illustrates the logic connections for loading single byte parallel data into the input buffer. DB0 should be grounded on "K" and "T" versions, and DB0 and DB1 should be grounded on "J" and "S" versions for monotonic operation of the DAC. DB9 is always the MSB, whether 8-bit, 9-bit, or 10-bit linear AD7522's are used.

When data is stable on the parallel inputs (DB0-DB9), it can be transferred into the input buffer on the positive edge of the strobe pulse.

Data is transferred from the input buffer to the DAC register when LDAC is a logic "1." LDAC is a level-actuated (versus edge-triggered) function, and must be held "high" at least 3μs for data transfer to occur.

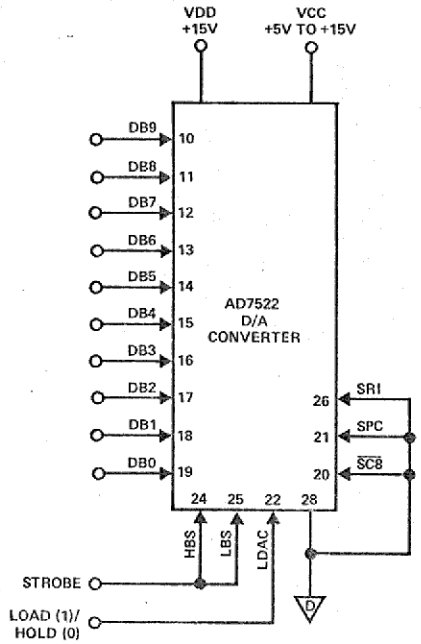


Figure 5. Single Byte Parallel Loading

TWO BYTE PARALLEL LOADING

Figures 6 and 7 show the logic connections and timing requirements for interfacing the AD7522 to an 8-bit data bus for two byte loading of a 10-bit word.

First, the least significant data byte (DB0 through DB7) is loaded into the input buffer on the positive edge of LBS. Subsequently, the data bus is used for status indication and instruction fetching by the CPU. When the most significant data byte (DB8 and DB9) is available on the bus, the input buffer is loaded on the positive edge of HBS. The DAC register updates to the new 10-bit word when LDAC is "high." LDAC may be exercised coincident with, or at any time after HBS loads the second byte of data into the input buffer.

SERIAL LOADING

Figure 8 and Figure 9 show the connections and timing diagram for serial loading.

To load a 10-bit word ($\overline{SC8}$ = 1), HBS and LBS must be strobed simultaneously with exactly 10 positive edges to clock the serial data into the input buffer. For 8-bit words ($\overline{SC8}$ = 0), only 8 positive edges are required.

The DAC register can now be loaded by holding LDAC "high."

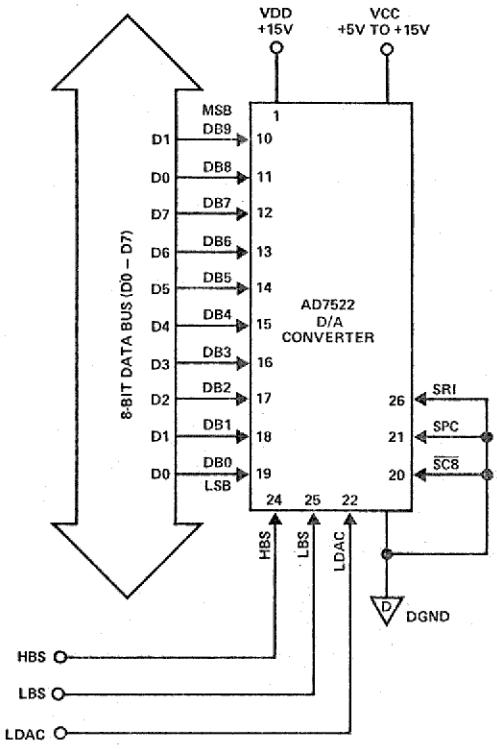


Figure 6. Two Byte Parallel Loading

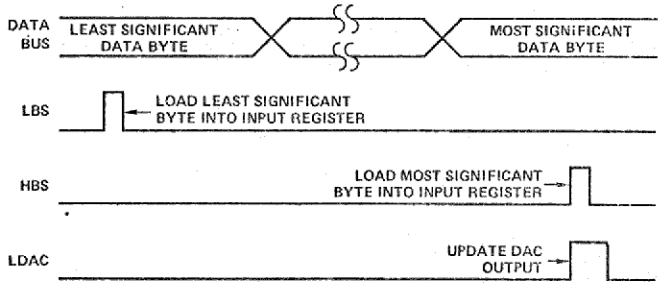


Figure 7. Timing Diagram

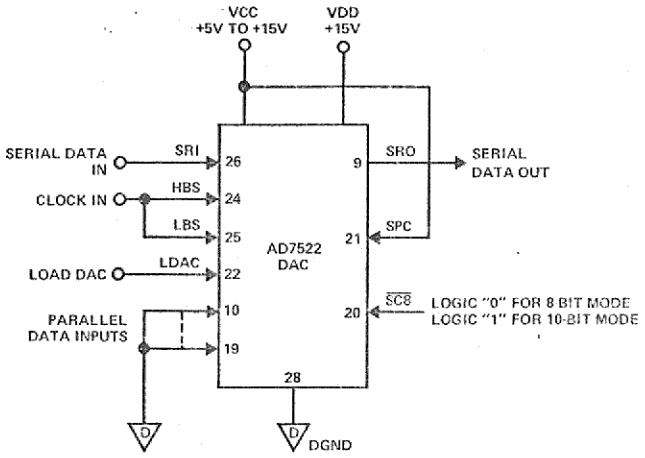


Figure 8. Serial 8- and 10-Bit Loading (Analog Outputs Not Shown for Clarity)

Applications cont'd

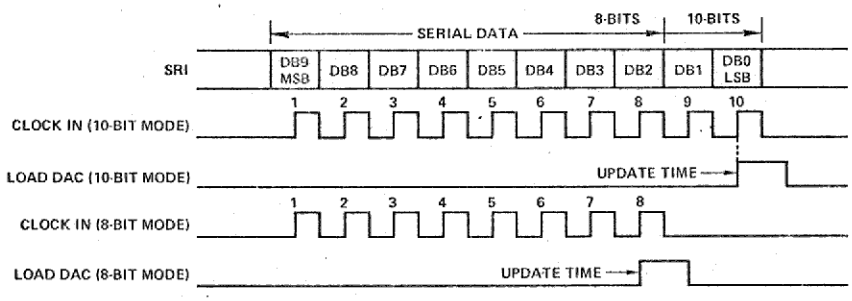


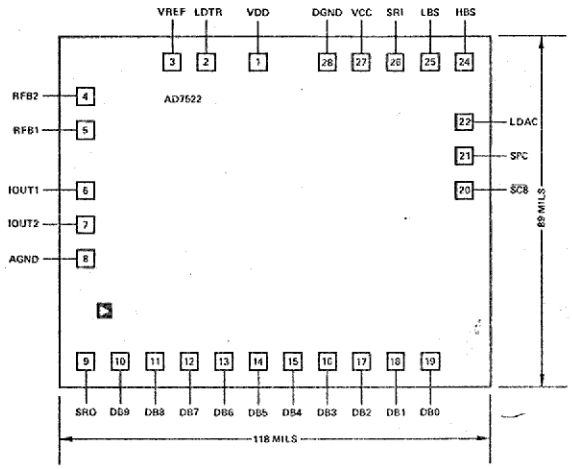
Figure 9. Timing Diagram for Serial 8- and 10-Bit Loading

APPLICATION HINTS

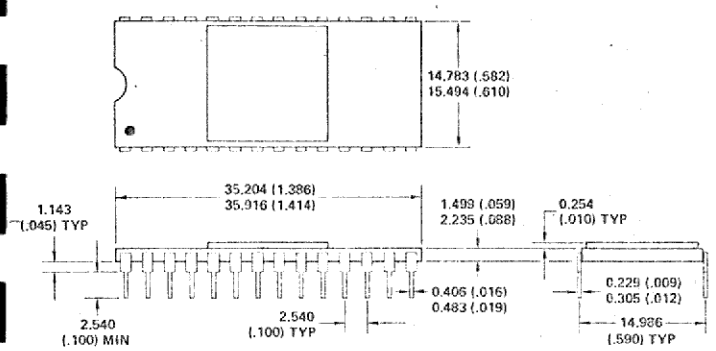
1. CR1 and CR2 on Figures 3 and 4 protect the AD7522 against latch-up if VCC exceeds VDD, and may be omitted if VDD and VCC are driven from the same voltage.
2. Diodes CR3 on Figure 3 and CR3 and CR4 on Figure 4 clamp the amplifier junction to −300 mV if they attempt to swing negative during power up or power down. The input structures of some high-speed op amps can supply substantial current under the transient conditions encountered during power sequencing. It is recommended that the PC layout be able to accommodate the diodes.
3. Fast op amps will require phase compensation for stability due to the pole formed by C_{OUT1} or C_{OUT2} and $R_{FEEDBACK}$.
4. During serial loading, all data inputs (DB0 through BD9), should be grounded.

Mechanical Information

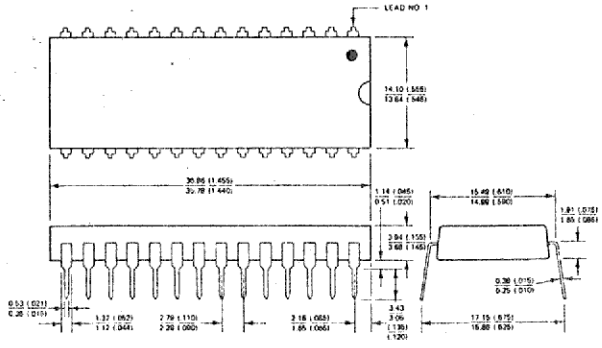
BONDING DIAGRAM



28 PIN CERAMIC DIP



28 PIN PLASTIC DIP



1. Lead no. 1 identified by dot or notch.
2. Dimensions in millimeters (inches).

C357–10–8/75

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ANALOG DEVICES

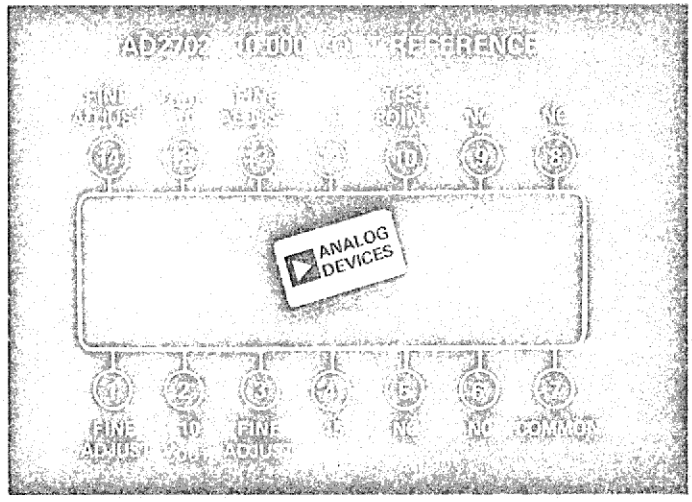
± 10.000 ± .001 Volt Precision Reference

AD2700 AD2701 AD2702

PRELIMINARY TECHNICAL DATA

FEATURES

- 3-Terminal Device:
  Voltage In/Voltage Out
- Total Output Error at
  T_{MAX} to: 2mV
- Excellent Long Term Stability:
  To 50ppm/yr.
- OP. Range: -55°C to +125°C
- 20mA Current Output Capability
- Available Screened to MIL-STD-883A
- Use with AD7520, AD7570, AD562
- Short Circuit Protected

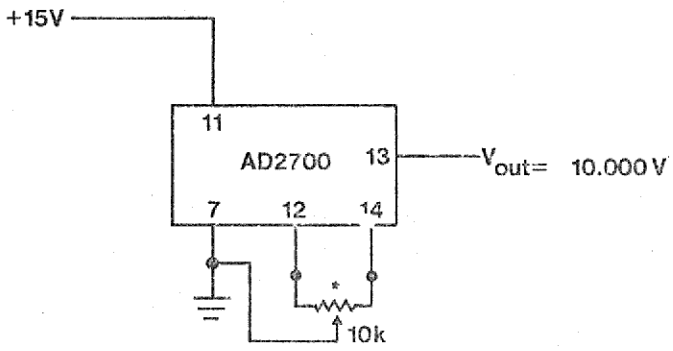


PRODUCT DESCRIPTION

The AD2700 is a medium cost, high stability, temperature compensated voltage reference source. The reference output is accurately fixed at 10V. With excellent termperature stability and long term stability of 50ppm/year, the AD2700 offers a convenient solution to regulated voltage requirements which may previously have been met with bulky power supplies or elaborate diodes and ovens. This product is made possible by the combination of the best available semiconductor technology with high precision thin film resistors which are functionally trimmed.

The AD2700 is recommended for use in 10- or, 12-bit A/D, and D/A converter circuits and other precise analog circuits. Its small size and hermetic seal make it adaptable to essentially any application or environment.

The operation of the AD2700 is 3 terminal, voltage in/voltage out. No external components are required. Offset adjustment terminals are provided for optional use if accuracy of better than 1mV is desired.



*External 10k potentiometer provides ±30mV output offset adjust. Temperature effect is ±4μV/°C per mV of offset correction.

(External Adjustment Optional)

MODEL	OUTPUT
AD2700	+10.000V
AD2701	−10,000V
AD2702	±10.000V

P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Telex: 924491 Cables: ANALOG NORWOODMASS

SPECIFICATIONS (typical at 25°C and V_{in} = +15V unless otherwise specified)

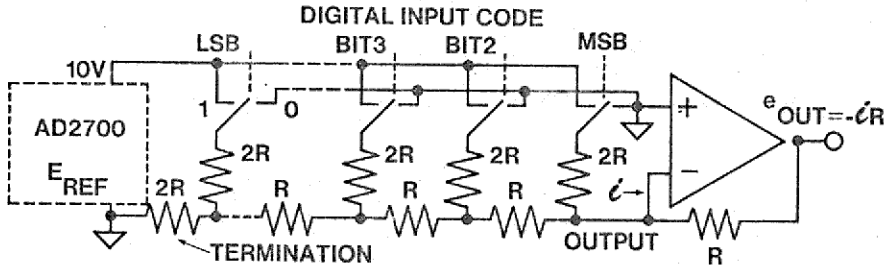
ABSOLUTE MAX RATINGS

Input Voltage	20VDC
Power Dissipation @ +25°C	400 mW
Derate Above 25°C	1mW/°C
Storage Temperature Range	-65 to +150°C
Lead Temperature (soldering, 10 sec)	250°C
Operating Temperature Range – L & U	-55°C to +125°C
Short Circuit Protection	Continuous

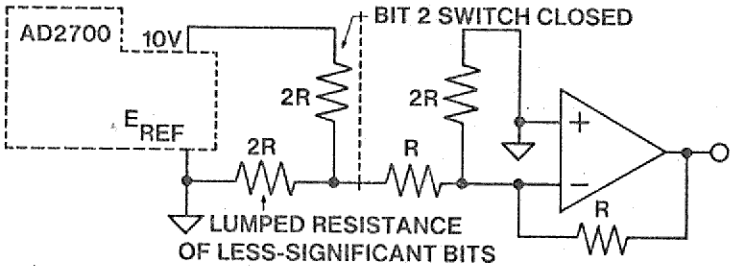
ELECTRICAL CHARACTERISTICS		MIN	TYP	MAX	UNITS
Output Voltage @ 25°C, No Load	−2700	+9.999	+10.000	+10.001	
	−2701	−10.001	−10.000	−9.999	
	−2702	±9.999	±10.000	±10.001	
Output Current			±18	±20	mA
Total Maximum Output Error	@−55° C		±0.02	±0.03	%
(Including Initial Offset)	−25° C		±0.02	±0.03	%
" L " Guarnateed −25° C to +85° C	0° C		±0.02	±0.02	%
" U " Guaranteed −55° C to +125° C	+25° C		±0.005	±0.01	%
	+70° C		±0.02	±0.03	%
	+85° C		±0.02	±0.03	%
	+125° C		±0.03	+0.03 −0.05	%
Input Regulation/Power Supply Rejection (V_{in} = 12 to 18 V)			.0003	.0004	%/%
Load Regulation:					
AD 2700/01	0 to ± 10mA		.0015	.002	%
AD 2702	0 to ± 5mA		.015	.02	%
(See Graphs Page 4)					
Input Voltage, Operating		12	15	18	V
Input Current, No Load				12	mA
*Noise (0.1 to 10Hz)				50	μVp-p
*Long Term Stability				50	ppm/yr
Output Resistance AD2700/01				0.02	Ω
*Ripple Rejection				.01	%/V
*Offset Adjust Range (see schematic, page 1)				±30	mV
*Offset Adjust Temperature Effect				±4	μV/°C per mV of adjust
OPTION 883 (designated as U/883) per MIL-STD-883A, Method 5004.2, Class B					

*Guaranteed by design, not tested.

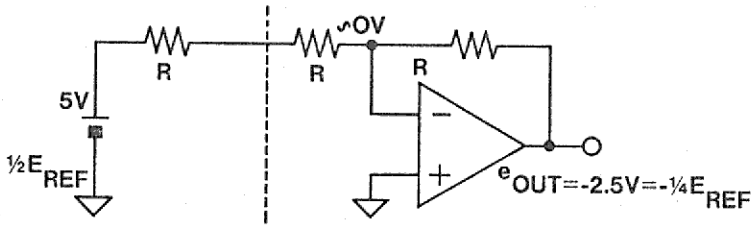
USING THE AD2700 VOLTAGE REFERENCE WITH D/A CONVERTER USING R-2R LADDER NETWORK IN CURRENT MODE



a. Basic Circuit



b. Example: Contribution of Bit 2; All Other Bits "0"



c. Simplified Equivalent of Circuit (b)

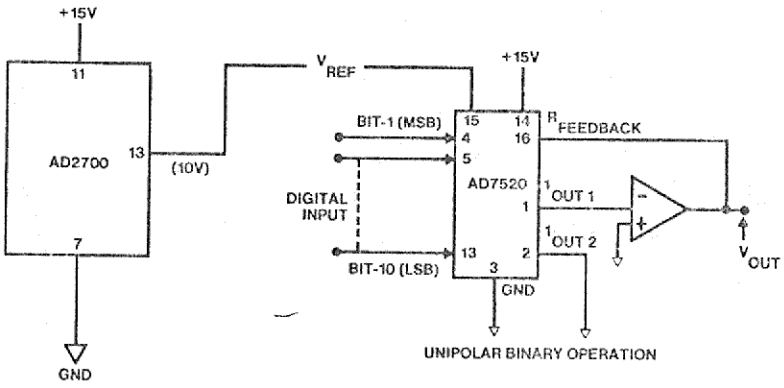
An AD2700 Voltage Reference used with an inverting operational amplifier and an AD855 R-2R ladder. If all bits but the MSB are off (i.e., grounded), the output voltage is $(-R/2R)E_{REF}$. If all bits but Bit 2 are off, it can be shown that the output voltage is $\frac{1}{2}(-R/2R)E_{REF} = 1/4\ E_{REF}$. The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is 2R; the Thévenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance 2R; since the grounded MSB series resistance, 2R, has virtually no influence – because the amplifier summing point is at virtual ground – the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the nth bit produces an increment of output equal to $2^{-n}\ E_{REF}$.

USING AD2700 REFERENCE WITH THE AD7520 AND AN IC AMPLIFIER TO BUILD A DAC.

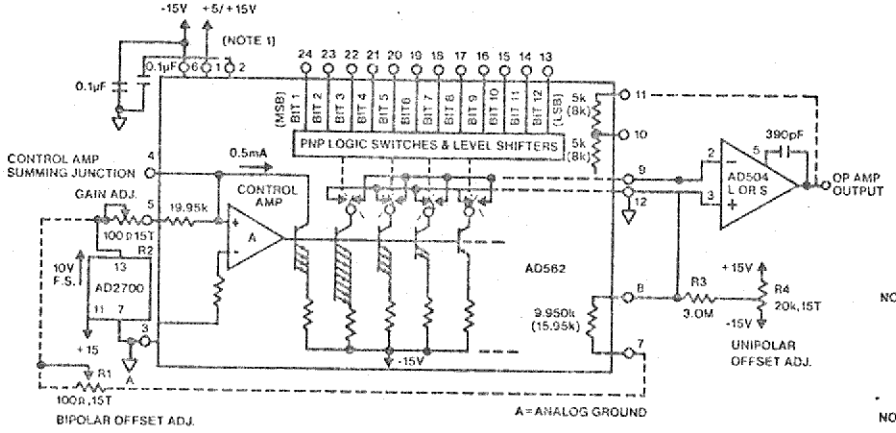
CODE TABLE – UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-10})$
1000000001	$-V_{REF}\ (1/2 + 2^{-10})$
1000000000	$\frac{-V_{REF}}{2}$
0111111111	$-V_{REF}\ (1/2 - 2^{-10})$
0000000001	$-V_{REF}\ (2^{-10})$
0000000000	0

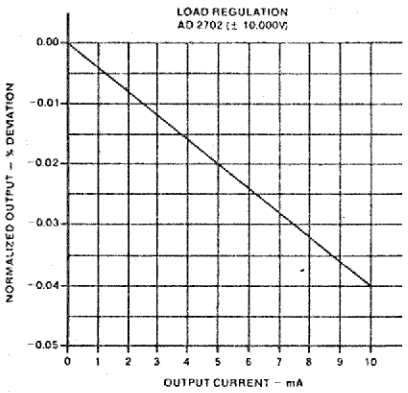
NOTE: $1LSB = 2^{-10} V_{REF}$

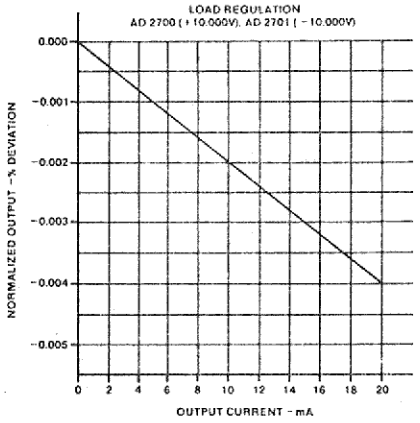


USING AD2700 REFERENCE WITH THE AD562

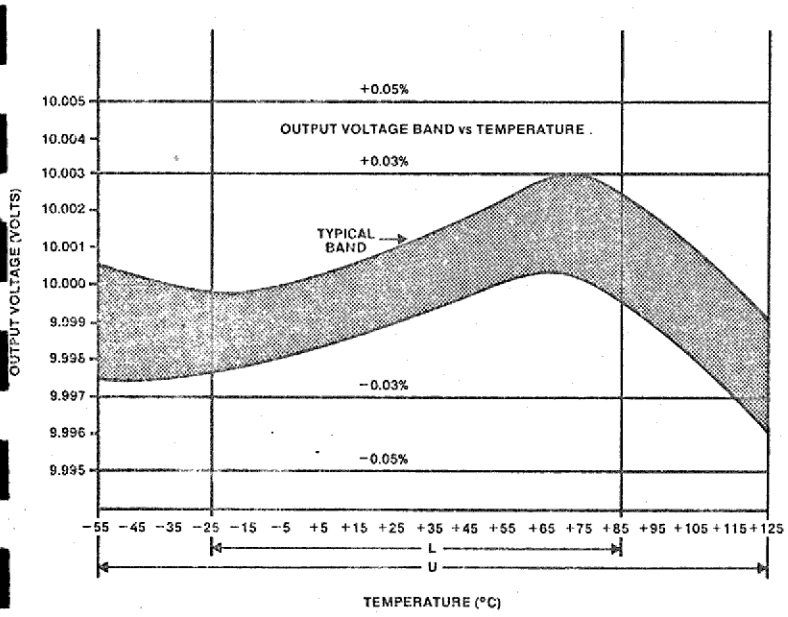


NOTE 1.
A. FOR TTL AND DTL COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND LEAVE PIN 2 OPEN.
B. FOR LOW VOLTAGE CMOS COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.
C. FOR HIGH VOLTAGE CMOS COMPATIBILITY, CONNECT +15 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.
NOTE 2. RESISTOR VALUES IN PARENTHESES ARE FOR BCD VERSION.

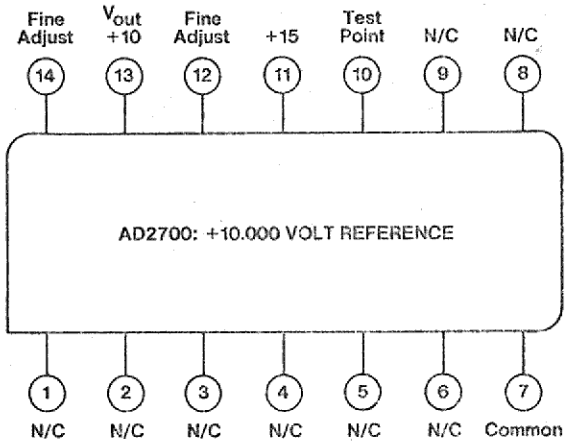


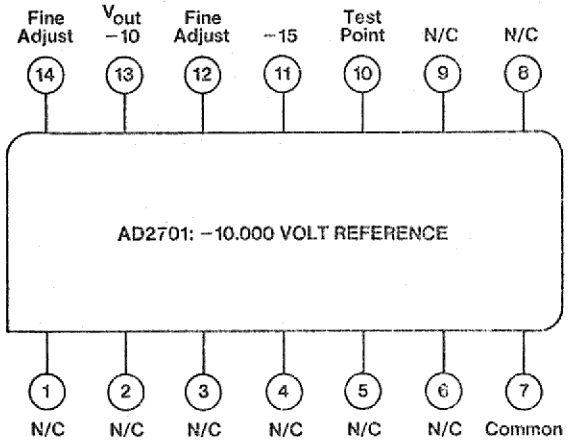


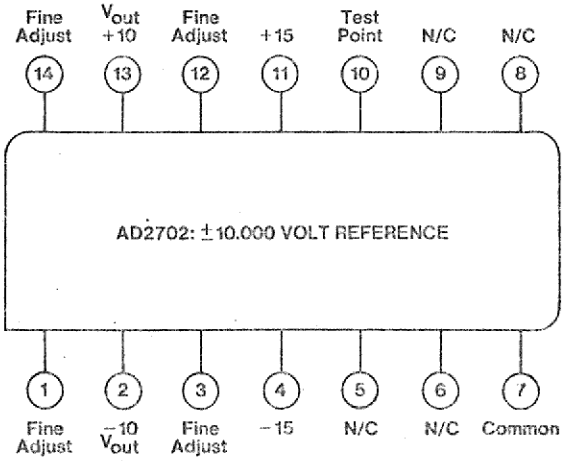
OUTPUT VOLTAGE VS. TEMPERATURE



PIN DESIGNATION



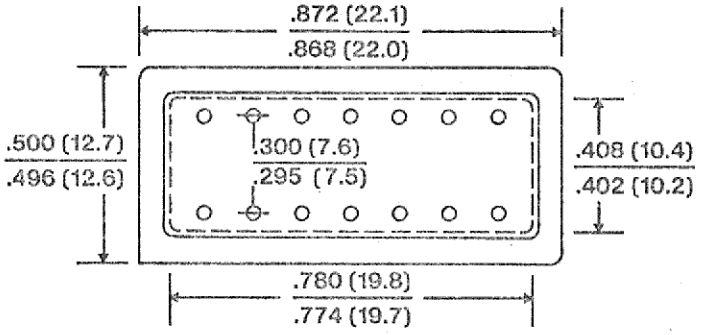


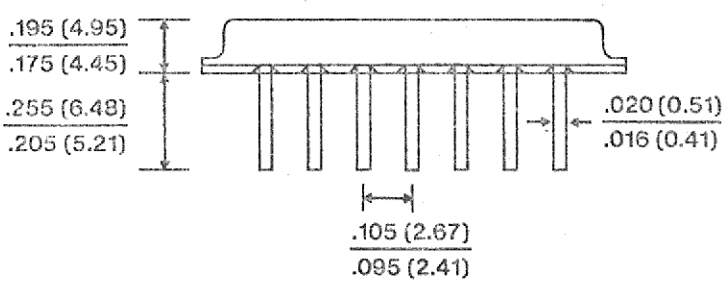


OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

14-PIN DUAL-IN-LINE





C364–10–10/75
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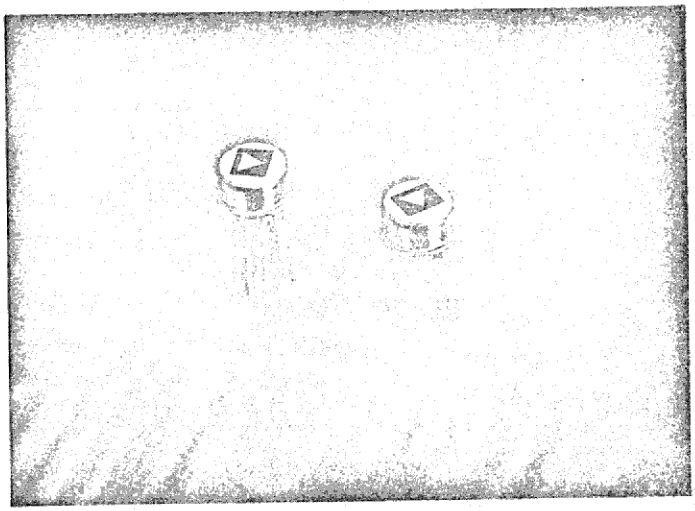
ANALOG DEVICES

Low Cost, High Speed, IC Operational Amplifier

AD518

FEATURES

- High Slew Rate: 70V/μsec
- Wide Bandwidth: 12MHz
- 60° Phase Margin (At Unity Gain Crossover)
- Drives 300pF Load
- Guaranteed Low Offset Drift:
  - 15μV/°C Max (AD518K)
- Pin Compatible With 118-Type Op Amp Series
- MIL-STD-883 Availability



PRODUCT DESCRIPTION

The AD518J, AD518K, and AD518S are high speed precision monolithic operational amplifiers designed for applications where slew rate and wide bandwidth are required, but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a 60° phase margin to insure stability, a minimum unity gain slew rate of 50V/μsec, and a typical bandwidth of 12MHz. In addition, in inverting applications external feedforward compensation may be added to increase the slew rate to over 100V/μsec, and nearly double the bandwidth. If desired, settling time to 0.1% can be reduced to under 1μsec with a single external capacitor.

The AD518's dc performance is consistent with its precision dynamic characteristics. The devices feature offset voltages below 2mV, maximum offset drifts of 15μV/°C, and offset currents below 50nA max.

The high slew rate, fast settling time, ease of use, and low cost of the AD518 make it ideal for use with D/A and A/D converters, as well as active filters, sample-and-hold circuits, and as a general purpose, fast, wideband amplifier. The AD518 is supplied in the TO-99 package. The AD518J and AD518K are specified for operation over the 0 to +70°C temperature range; the AD518S for operation from −55 to +125°C.

PRODUCT HIGHLIGHTS

1. The AD518 offers the user high speed performance and flexibility previously unavailable at low cost . . . . . .
   - Internal compensation for unity gain applications
   - Capability to increase slew rate to over 100V/μsec and double the bandwidth by an external feedforward technique
   - Capability to reduce settling time to under 1μsec to 0.1% with a single external capacitor
   - Differential input capability
2. The phase margin of the AD518, uncompensated at the unity gain crossover frequency, is 60°, providing unconditional stability for all conditions. This conservative phase margin represents a clear improvement over that of the 118 series IC op amps currently available.
3. The static performance of the AD518 is consistent with its excellent dynamic performance, providing offset voltage drift under 15μV/°C, CMRR of 80dB, and offset current below 50nA.
4. Every AD518 is stored for 40 hours at +200°C, temperature cycled 10 times from −65 to +150°C, and subjected to a high g shock test to insure reliability and long-term stability.

P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Telex: 924491 Cables: ANALOG NORWOODMASS

SPECIFICATIONS (typical @ +25°C and V_S = ±15VDC unless otherwise specified)

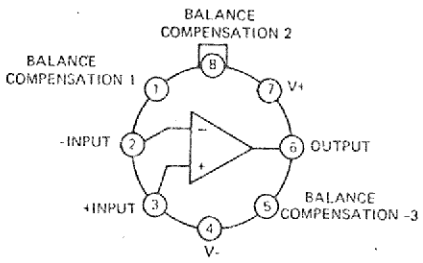
PARAMETER	AD518J	AD518K	AD518S
OPEN LOOP GAIN			
$R_L \geq 2k\Omega$, V_O = ±10V	25,000 min (100,000 typ)	50,000 min (100,000 typ)	50,000 min (100,000 typ)
@ T_A = min to max	20,000 min	25,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ $R_L \geq 2k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*
Current @ V_O = ±10V	±10mA	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	12MHz	*	*
Slew Rate, Unity Gain	50V/µsec min (70V/µsec typ)	*	*
Settling Time to 0.1% (Single Capacitor Compensation)	800nsec	*	*
Phase Margin, Uncompensated at Unity Gain Crossover Frequency	60°	*	*
INPUT OFFSET VOLTAGE			
Initial, $R_S \leq 10k\Omega$	10mV max (4mV typ)	4mV max (2mV typ)	4mV max (2mV typ)
@ T_A = min to max	15mV max	6mV max	6mV max
Avg vs. Temp, T_A = min to max	10µV/°C	15µV/°C max (5µV/°C typ)	20µV/°C max (10µV/°C typ)
Avg vs. Supply, T_A = min to max	65dB min (80dB typ)	80dB min (90dB typ)	80dB min (90dB typ)
INPUT BIAS CURRENT			
Initial	500nA max (120nA typ)	250nA max (120nA typ)	250nA max (120nA typ)
@ T_A = min to max	750nA max	400nA max	400nA max
INPUT OFFSET CURRENT			
Initial	200nA max (30nA typ)	50nA max (6nA typ)	50nA max (6nA typ)
@ T_A = min to max	300nA max	100nA max	100nA max
INPUT IMPEDANCE			
Differential	0.5MΩ min (3.0MΩ typ)	*	*
INPUT VOLTAGE RANGE †			
Common Mode, max safe	$\pm V_S$	*	*
Operating, V_S = ±15V	±11.5V	*	*
Common Mode Rejection Ratio	70dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	10mA max (5mA typ)	7mA max (5mA typ)	7mA max (5mA typ)
TEMPERATURE RANGE			
Rated Performan.	0 to +70°C	*	−55 to +125°C
Storage	−65 to +150°C	*	*

† The inputs are shunted with back-to-back diodes; if the differential input may exceed ±1 volt, a resistor should be used to limit the input current to 10mA.

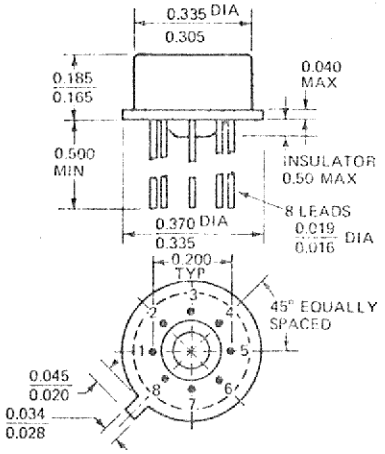
*Specifications same as AD518J.

Specifications and prices subject to change without notice.

PIN CONFIGURATION
Top View



OUTLINE DIMENSIONS
Dimensions shown in inches



HIGHER BANDWIDTH OR HIGHER SLEW RATE APPLICATIONS

For applications where higher bandwidth is desired, the bandwidth of the AD518 may be increased to nearly 25MHz by using the feedforward technique shown in Figure 4.

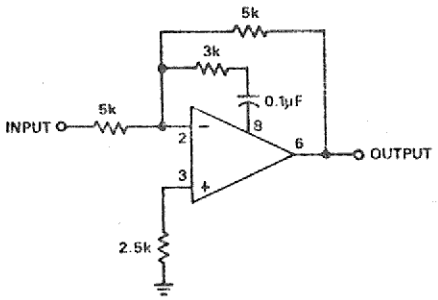


Figure 4. High Bandwidth Configuration

For applications where higher slew rate is desired, the slew rate of the AD518 may be nearly doubled using the technique shown in Figure 5.

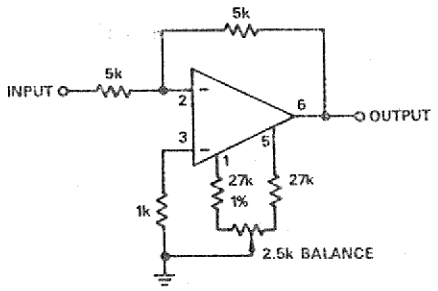


Figure 5. High Slew Rate Configuration

Note that the techniques of Figures 4 and 5 may be used in conjunction with each other to both double the bandwidth to 25MHz and increase the slew rate to 100–140V/μsec.

USING THE AD518

The connection scheme employed when using the AD518 is considerably more important than for low frequency, general purpose amplifiers. The primary purpose of the 0.1μF bypass capacitors shown in Figure 6 is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V– 0.1μF capacitor equalizes the supply grounds, while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. This signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal. In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

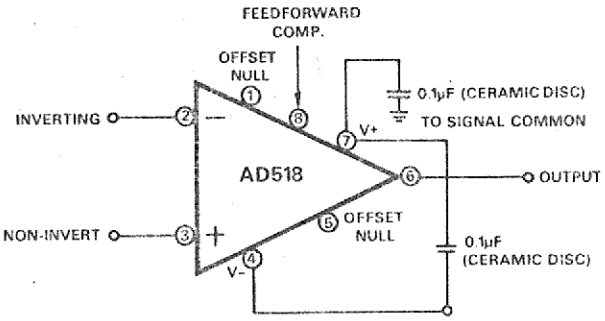
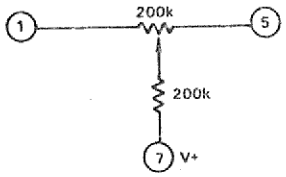


Figure 6. General Purpose Connection Diagram

NULLING THE AD518



OTHER IC HIGH SPEED AMPLIFIERS AVAILABLE

AD505	Slew Rate of 120V/μsec min Bias Current of 25nA max Offset Voltage Drift of 15μV/°C max
AD507	35MHz Gain Bandwidth Slew Rate of 25V/μsec min Bias Current of 15nA max Offset Voltage Drift of 15μV/°C max
AD509	Settles to 0.01% in 1μsec Settles to 0.1% in 200nsec Slew Rate of 100V/μsec min

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