ID-7024 2K static
NON-VOLATILE RAM Module

Dansk Data Elektronik ApS

ID-7o24 2k STATIC NON-VOLATILE RAM MODULE

for the

ID-7ooo MICROPROCESSOR SYSTEM

August 1977

Author: Peter Kyllesbeck

ID-7o24 2k STATIC NON-VOLATILE RAM MODULE

1. Introduction

ID-7o24 is a 2k-8bit static writeable memory module. The memory
chips used are INTERSIL IM6518. The contents of the memory can
be writeprotected by means of a switch on the module or by a
software instruction. The module contains power down protect
logic which write protects the memory module 2 ms after an active
signal on the power-loss line. When power returns the system
generates a RESET signal, which makes it posible to open or
close the memory module for writing by a software instruction.
The module contains Ni-Cd batteries which can supply the memory
for about 8o hours, and the module contains a charger which can
recharge the batteries in about 2 hours.

2. Description

2.1 Addressing the module

This module uses 2k consecutive addresses of the possible 64k
memory. The address of the module is set by a 5bit switch regi-
ster on the board.
   The bits on the address bus are used in the follewing manner.

ADR(15:11)   determine if the actual memory board is
                    selected. This happens if ADR(15:11) and
                    the manual switch register are identical.

ADR(lo)   selects one of two 1k memory banks

ADR(9:o)   select one 8bit word from the addressed
                    memory board

2.2 Writeability of memory

The memory can be write protected by means of a switch on the
module. This way of protection overrides a software instruction
which would open the memory for writing. If writing is enabled
by the switch, the writeability is controlled by a flip-flop
set by an OUT-instruction. The controlling bit is DATA(o).
A DATA(o) = 1 opens the memory for writing. The setting of the
flip-flop is lost during power off. Therefore, the flip-flop
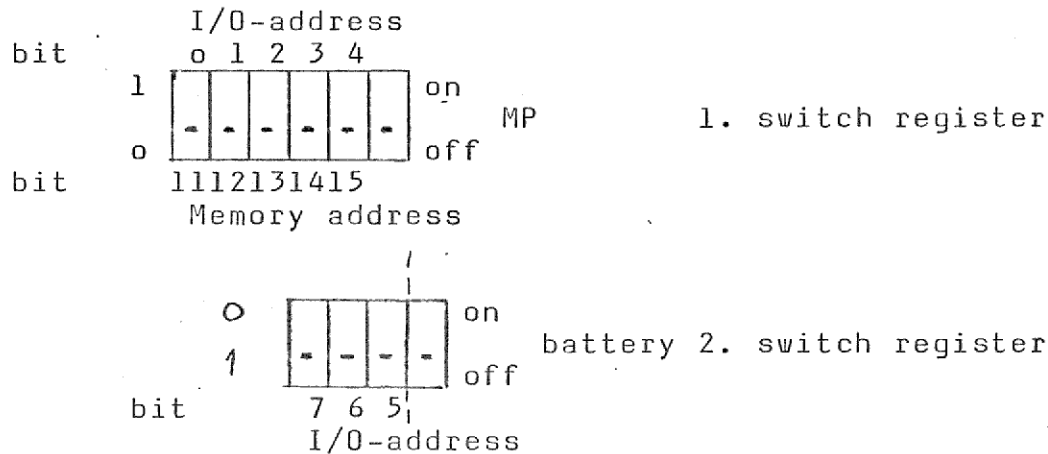must be set to the desired value after power- up.
   When AC power is lost the power supply can deliver power for
some ms in order to allow time for the system to shut down.
The AC power loss is signalized by the bus line POWER LOSS
and this line must be connected to the interrupt system in order
to activate the software routines that can store registers and
data in the non-volatile portion of memory. The POWER LOSS signal
is used on the module to close the memory for writing 2 ms after
the signal. This is done to prevent destruction of the content
of the memory by false signals on the bus when power drops below
4.75V. This security protection disapears 2 us after the power-up
RESET signal is deactivated.

2.3 Addressing the memory protect flip-flop

As described in 2.2 the memory can be write protected by means
of an OUT- instruction. The I/O-address of the module is set
by two sets of switch registers. A complete I/O-address requires
a specification of 8 bits, but to reduce the number of switches
a special way of setting the I/O-address is used:
  The 5 LSB of the I/O-address are taken from the switch register
specifying the 5 MSB of the memory address, and the 3 MSB of the
I/O-address are set by the second switch register.

2.4 Switch registers

```
                I/O-address
  bit           o 1 2 3 4
        1       ┌─┬─┬─┬─┬─┐    on
                │ │ │ │ │ │         MP      1. switch register
                │-│-│-│-│-│
        o       └─┴─┴─┴─┴─┘    off
  bit           1112131415
                Memory address


                            ╱│
        O       ┌─┬─┬─┬─┐   on
                │ │ │ │ │              battery 2. switch register
        1       │-│-│-│-│
                └─┴─┴─┴─┘   off
  bit            7 6 5│
                I/O-address
```

The switch registers are situated in the upper middle of the module.
The 1. switch register determines which 2k addresses of memory the
module incorporates and the 5 LSB of the I/O-address. The 2. switch
register determines the 3 MSB of the I/O-address. The memory
protect switch is situated to the right of the 1. switch register.
To the right of the 2. switch register a switch for the battery
is placed. The switch should be in the off position when the module
is not in use.

2.5 Batteries and charger

The module contains 4 Ni-Cd cells which can supply the memory for
about 8o hours. The charger can recharge the batteries in about
2 hours and the batteries are kept fully charged as long as power
is supplied to the module. The chargers characteristics, e.g.
recharge current and maximum battery voltage are set by two poten-
tiometers in the upper left corner of the module. The one to the
left is controlling the maximum battery voltage which is 6.oV,
and the other controls the charge current which is loo mA. The
charging is stopped when the voltage is 6.o V and it starts when
the voltage has dropped to 5.6 V.

PCB component layout diagram. Labeled components include:

- 25k, 10Ω (top left)
- MPS 5646
- 100nF
- 6.8k, 3.6k, N (resistor block)
- R16, R17, R18, R19, R20, R21, R22, R23, R24 (resistor row)
- RS180 (×4, right side blocks)
- 5.0R, N, R, R15, 2.7k, 6.8k (resistor block)
- 741
- N, 5.6k, 4.7k (resistor block)
- 47µF, 20R, N
- R14, 50nF, R13, R12, R11, R10
- M10, M11, M12, M13, M14, M15, M16, M17 (top IC row)
- M00, M01, M02, M03, M04, M05, M06, M07 (middle IC row)
- K9, K6 (small vertical labels)
- 13, 11, 12, 9, 10 (numbered blocks)
- R8, R7 (vertical labels)
- R4
- R1, R3, R2, R5 (small labels)
- 1, 2, 3, 4, 5, 6, 7, 8 (numbered blocks, bottom row)
- 100nF (vertical label, bottom right)