ID 7034 & 35 R
Video display modules

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1. General description.

The ID 7034 & 35 R modules provide an output-only facility adjustable to individual purposes, as they are based on a programmable CRT-controller.

The ID 7034 R two-board set produces a standard video black & white output, and adding the ID 7035 R brings colour into the display, producing either a 0.7 Vpp output for high impedance monitors or a 4 Vpp inverted output for 75 ohm monitors.

The modules contain their own 4K bank-switchable memory blocks to obtain the lowest possible updating time. The standard version provides an EPROM´ed character generator of a 128 character set (5*7 dot matrix), with options for a 256 character set, and or 7*9 dot matrix or even a RAM character generator (on separate board). The maximum characters per frame is 32 rows of 80 characters each with a total of 2560 characters.

It is advisable to use high-rem type monitors when more than 64 characters/line output is wanted, as normal TV-monitors do not have the required resolution for the high shifting frequency thus produced.

2. Frame build-up.

The frame is build up of space-matrices (min. 8*6 dots, max. 8*16 dots). The space-matrices are adjacent, and all dots within a space-matrix are contained in the character-generator, which means that semi-graphic displaying can be obtained. Still the actual character-matrix should be inside the space-matrix to assure spacing between numerals (vertical and horizontal) of at least one dot.

With the optional 256 character set, for example it is possible to mix 5*7 and 7*9 character matrices inside a 8*12 space-matrix.

3. Memory organization.

The local memory is organized as 4 K switchable banks. Switching in or out takes approx. 3 microseconds (one OUT-instruction). When switched in, the memory seen from the CPU looks like any other memory and the ordinary move-to-memory instructions etc. can be executed with no extra delay. In this time the displaying is off (black screen).

Bank 1 contains ASCII codes for the characters, i.e. input to the character generator. This means that one byte determines the look of a whole space matrix.

The memory is addressed consecutively by the CRT-control, row by row. The address of the first character to be displayed is a programmed value. As a total of 80*32=2560 characters only require 2.5 K, a dynamic use of first-address loading enables some roll-up/roll-down.

Using a 128 character set only requires 7 bits of code and the 8th bit (bit 7) then determines blink/non blink on the specified character. The blink frequency can be strapped to either 3.2, 1.6, 0.8 or 0.4 Hz (see figure 2.A), and the character blink is independent of an eventual cursor blink (programmed, see appendix 1). When a 256 character set is used, the blink facility of course is lost.

Bank 2 (only when a 7035 R module is added) contains the colour information. Bank 2 is addressed in parrallel to bank 1 during display and also occupies the same memory area when CPU-controlled, i.e. the same location on the two banks contains the character and colour information on the same space-matrix.

Passive colour				Active colour			
F/H	B	G	R	F/H	B	G	R
D_7							D_0

The colour information consists of two independant 4 bit codes, one (the 4 least significant bits) determines the active colour, i.e. the colour of dots being white in a b/w display, and one (the 4 most significant bits) determines the passive colour, i.e. the colour of the dots inside the space matrix that would be black in a b/w display.

The same 16 colour combinations are possible for passive and active dots, in any mixture.
Of the 4 bits the most significant (bit 3 or bit 7) determines full (=1) or half (=0) illuminance, and the 3 least significant bits (bits 0 to 2 or 4 to 6) includes(=1)/excludes(=0) the colour composants red, green and blue respectively.

Bank 3 (only when a RAM character generator board is added) also holds it´s own 4 K memory bank, occupying the same memory locations as bank 1 and 2 when switched in.
This bank is organized equally to the EPROM-generator (see section 8).

4. Light pen circuit.

The A-board (7034 set) contains space for mounting of a light pen amplifying circuit; and some logic for light pen control is already on the board, expecting a start strobe and a light pen strobe on TTL-level. Using a light pen, the internal address of the space pointed out will be latched into the CRT-controller and can be read by the CPU with an IN-instruction (see section 7 and appendix 1).

5. Interrupts.

The ID 7034 R produces two interrupts that can be strapped to any of the eight interrupt lines (see figure 1).
One interrupt occurs when a legal light pen strobe has been detected. And one interrupt follows the start of the vertical sync. pulse. When this interrupt occurs, there will be approximately 3.2 millisecond to the start of the next display period, and this interval can be used to updating of the frame without any loss of display time.
The interrupts are cleared by IN-instructions (see sect. 7).

6. Adressing.

The basic memory address (the 4 MSB of all addresses) are set on a 4-bit switch on the A-board, see figure 2.

The ID 7034/35 R modules use eight input/output adrresses. The basic address is set on a 5-bit switch on the A-board, see figure 3.

7. Instructions.

Instruction set (BA = basic I/O-address):

OUT (BA+0) : DISPLAY ON and no banks CPU-controlled (1)
OUT (BA+1) : DISPLAY OFF and BANK 1 under CPU-control (1,2)
OUT (BA+2) : DISPLAY OFF and BANK 2 under CPU-control (1,2)
OUT (BA+3) : DISPLAY OFF and BANK 3 under CPU-control (2)
OUT (BA+4) : WRITE CRT ADDRESS REGISTER
The data word is loaded into the CRT address register (3)
OUT (BA+5) : WRITE CRT DATA REGISTER
The data word is loaded into the CRT data register pointed out by the CRT addr.register (3).
OUT (BA+6) : SELECT 80*8 BIT ROW (4)
OUT (BA+7) : SELECT 40*8 BIT ROW (4)

IN (BA+0) : RESET VSYNC INTERRUPT
IN (BA+1) : RESET VSYNC INTERRUPT
IN (BA+2) : RESET LIGHT PEN INTERRUPT
IN (BA+3) : RESET LIGHT PEN INTERRUPT
IN (BA+7) : READ CRT DATA REGISTER
The content of CRT data register pointed out by the CRT address register is fetched to the CPU accumulator (3).
IN (BA+4) to IN (BA+6) have no effect.

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1) These instructions do not affect and do not use the data word, which means that the data word to be written into the bank can already be placed i the CPU´s A-register before connecting the bank, i.e. updating of one character can be done in 3 instructions

OUT (BA+1); MOV M,A; OUT (BA)
setting display off for less than 8 microseconds.

2) When the ID 7035 R / RAM ch.gen board is not used, no banks are connected, but display still goes off.

3) See appendix 1 (CRT controller description).

4) RESET equals an OUT (BA+6) instruction.

8. Character generation.

The displayed character is generated from the contents of 6 to 16 memory locations (in the EPROM or optional BANK 3).
One scan line of the character is contained in one 8 bit word with a "1" representing a white (active coloured) dot and a "0" representing a black (passive coloured) dot, and shifted out most significant bit first (leftmost) onto the screen.

Regardless of the number of scan lines per character, used, the character generator expects 16 lines, as to the organization of the locations.
Location no. 0 in the EPROM/RAM contains scan line 0 for the character with ASCII code 0, location 1 contains scan line 1 for ASCII 0, ... location 15 contains scan line 15 for ASCII 0, location 16 contains scan line 0 for ASCII 1 etc.
This means that in case a 8*8 space matrix is used, half of the locations are never addressed and left as "holes" (programmed as blanks), and this enables optional spacing between lines without change of character generator.

Some examples are shown in figures 4 through 6 and a complete listing of the content of the standard EPROM is given in appendix 3.

9. Initialization.

At any RESET (program start) the CRT-controller needs initialization depending on the format used; and a format change can be obtained during run by reinitializing the controller. The initial values depend on the format chosen in relation primarily to the basic character frequency. TABLE 1 gives the initial values for some formats usable in the standard version and appendix 2 is an example of an initialization subroutine.

10. Options.

Apart from the already mentioned options for character generation and colouring, the ID 7034 & 35 R modules can be delivered with a different basic clock crystal to obtain optional characters per row values. For instance a crystal clock frequency of 8.00 MHz will give 48 characters per row. This option would result in an output frequency within the band-width of a normal CTV-set (when output is connected directly to the colour cannons, and DDE has developed a kit for rebuilding of a B&O CTV into a display monitor for the 7034 & 35 R modules.

The RAM-character generator is delivered as a separate PCBA. It interconnects with the ID 7034R-B via to flat-cables. The function is already discussed in section 3.

Space is provided on the ID 7034R-A board for mounting of a small light-pen cicutry, on the upper rigth part of the board. Figure 7.A shows the circuitry´s connections outwards and to the ID 7034. A negative going pulse on input D will start a white-sweep on the screen, and a negative pulse on input C will latch the current frame address into the CRTC´s light pen register. The Component Placing of ID 7034R-A shows the

space provided - for one 8-pin IC, 1 transistor, and three resistors. When the board-set is delivered without a RAM-character generator, inputs C and D are strapped to GROUND.

11. Other strappings and adjustments.

The choice between a 256 character PROM or a 128 character PROM and blink also calls for different strappings. This strap is situated on ID 7034R-B (see the component placing figure), and the two different ways of strapping is shown of figures 7.B and 7.C.

Depending on the number of characters per line, a different delay of data relative to colour-shift is required. This is strapped on board ID 7035R (see component placing).

Finally it is possible to adjust the half-colours (low luminance colours). This is done on one of two sets of resistors (depending on the output driver used), see the component placing figure.

TABLE 1

Initial register values for some values of (characters * character-lines)

	80*32		80*25		80*20		80*16		40*16(1)		48*32(2)		64*32(3)	
Space matrix	8*8		8*10		8*12		8*16		8*16		8*8		8*8	
Char. matrix	5*7		5*7 /7*9		5*7 &/7*9		5*7 &/7*9		5*14/2		5*7		5*7	
R0	107	6B	107	6B	107	6B	107	6B	53	35	63	3F	79	4F
R1	80	50	80	50	80	50	80	50	40	28	48	2F	64	40
R2	88	58	88	58	88	58	88	58	44	2C	53	34	66	42
R3	10	0A	10	0A	10	0A	10	0A	05	05	06	06	07	07
R4	38	26	31	1F	26	1A	19	13	19	13	38	26	38	26
R5	0	0	2	2	0	0	8	8	8	8	0	0	0	0
R6	32	20	25	19	20	14	16	10	16	10	32	20	32	20
R7	34	22	28	1C	23	17	17	11	17	11	35	23	34	22
R9	7	7	9	9	11	0B	15	0F	15	0F	7	7	7	7
	dec	hex	dec	hex	dec	hex	dec	hex	dec	hex	dec	hex	dec	hex

Mode can be either interlaced or non interlaced, but not interlaced and sync. Cursor can be chosen as described in app. 1.

1) In this mode dots have double width but the same hight and initialization includes an OUT (BA+7) instruction.
2) This demands an optional clock crystal of 8.00 Mhz.
3) This demands an optional clock crystal of 10.00 Mhz.

/ = or
&/ = and/or

TABLE 2

The standard character set.

The generated characters and their ASCII codes (hex.).

00		10		20		30	0	40	@	50	P	60		70	p
01		11		21	!	31	1	41	A	51	Q	61	a	71	q
02		12		22	"	32	2	42	B	52	R	62	b	72	r
03		13		23	#	33	3	43	C	53	S	63	c	73	s
04		14		24	$	34	4	44	D	54	T	64	d	74	t
05		15		25	%	35	5	45	E	55	U	65	e	75	u
06		16		26	&	36	6	46	F	56	V	66	f	76	v
07		17		27	'	37	7	47	G	57	W	67	g	77	w
08		18		28	(	38	8	48	H	58	X	68	h	78	x
09		19		29	)	39	9	49	I	59	Y	69	i	79	y
0A		1A		2A	*	3A	:	4A	J	5A	Z	6A	j	7A	z
0B		1B	→	2B	+	3B	;	4B	K	5B	Æ	6B	k	7B	æ
0C		1C		2C	,	3C	<	4C	L	5C	ø	6C	l	7C	ø
0D		1D		2D	-	3D	=	4D	M	5D	Å	6D	m	7D	å
0E		1E		2E	.	3E	>	4E	N	5E		6E	n	7E	
0F		1F		2F	/	3F	?	4F	O	5F	_	6F	o	7F	

FIGURES

Refer also to component placing figures (next pages).

Figures 1-3 - see component placings.

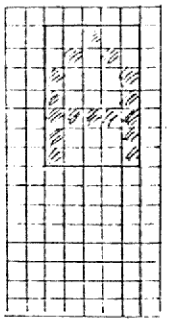


Figure 4

Placing of ch. matrix in max. space matrix allowing optional spacing between ch. lines

Figure 5

Optional placing allowing mixture of 5*7 on 7*9 character matrices. (space matrix = 8*12)

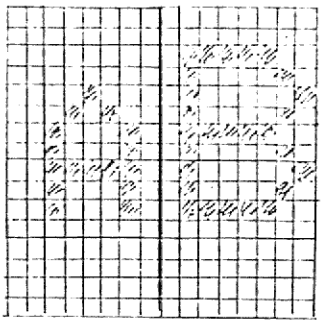
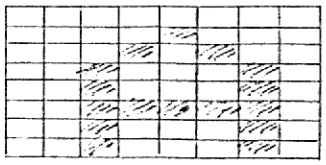


Figure 6

When a 40 character row is selected, the dots have double width but the same hight. Therefore a 8*16 space-matrix should be chosen. But not neccesarily.



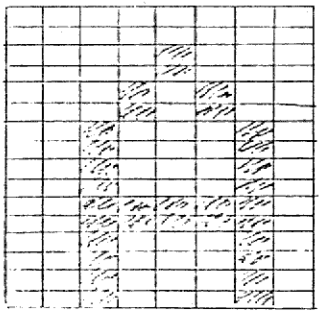


Figure 7A

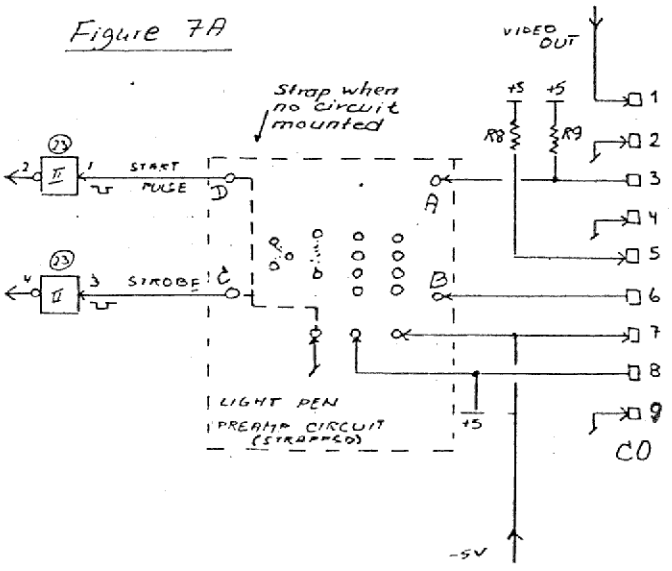
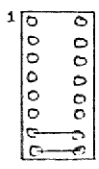
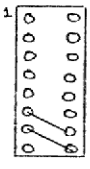


Figure 7.B 7.C

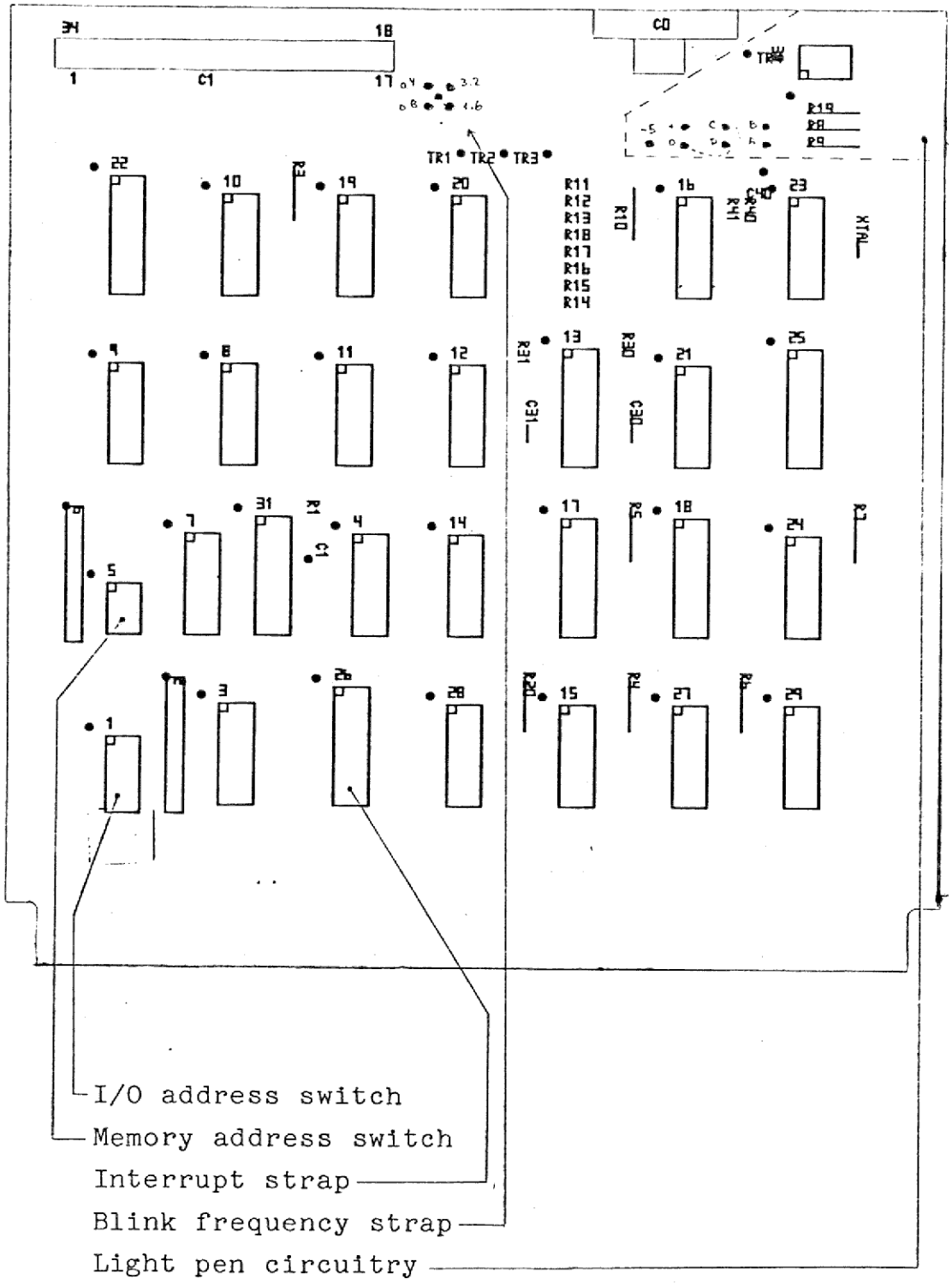


128 ch.s and blink

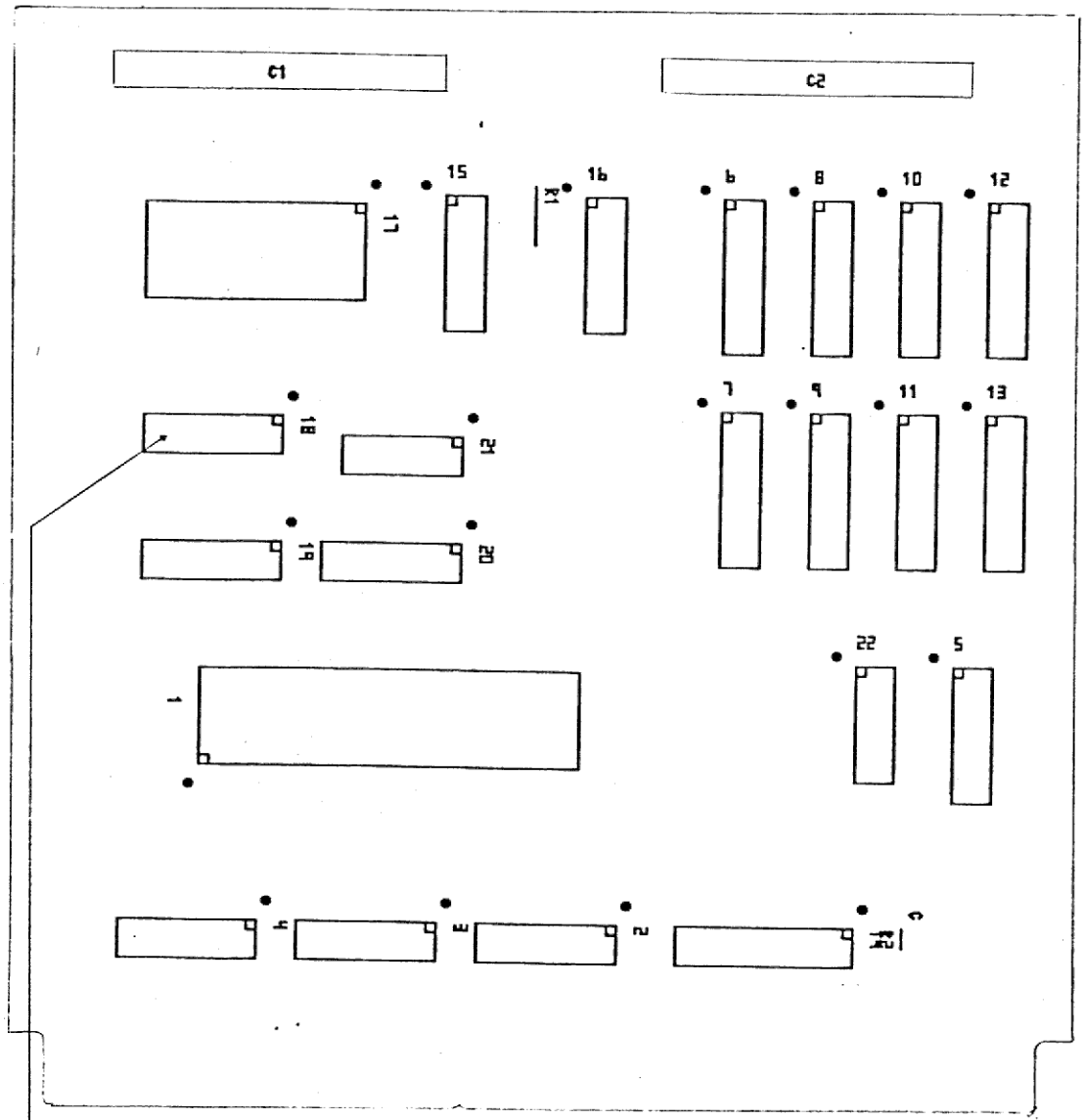


256 ch.s

Component placing, ID 7034R-A.



Component placing, ID 7034R-B.



Component placing, ID 7035R.