DANSK DATA ELEKTRONIK

ID-7037 32/16 K DYNAMIC RAM MODULE

for the

ID-7000 MICROPROCESSOR SYSTEM

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1. INTRODUCTION.

The ID-7037 Dynamic RAM Module contains 32 k words of 8 bits divided into two independent memory banks of 16 K words each.

2. DESCRIPTION.

2.1 BANK SWITCHING.

In order to expand the addressing capabilities af 8080/8085 the memory module is equipped with the bank switching facillity. This facillity allows a bank to be enabled or disabled. When a bank is enabled it occupies space in the memory space and can be accessed by the CPU and various DMA units. When a bank is disabled it does not occupy space in the memory space and it cannot be accessed.

A memory bank is identified by a bank control address which is FC or FD and a bit number between 0 and 7. In this way it is possible to differentiate between 16 different memory banks.

A memory bank with bank control address AA and bit number n is enabled when the CPU performs an OUT AA instruction and bit number n in the data word is one. The bank is disabled if the bit number n is zero.

The control address and the bit number is called the bank address and should not be confused with the memory starting address of the bank.

A memory bank on the ID-7037 module contains 16 K words. Thus a bank can be placed four different places in the 64 K memory space of the 8080/8085.

The two memory banks are called bank 0 and bank 1. The memory starting address off the banks and the bank addresses are selected by means of two switch registers which are described below.

2.2 THE SWITCH REGISTERS.

A survey of the switch registers is shown in fig. 2. A switch is ON or a logic one when the red dot is visible.

2.2.1. DESCRIPTION OF SWITCH POS. 15.

The upper four bits control bank 0 and have the following functions:

BLD0: Bank logic disable.
When the switch is ON the bank switching logic is disabled which means that the bank is enabled, unless it is disabled by the following switch DISAB0.

DISAB0: Bank disable.
When the switch is ON the bank is disabled. When a bank is not installed on the module it should be disabled.

ADR(15:14): Memory starting address of the bank.
The bits select the memory starting address of the bank

The lower four switches in position 15 control bank 1 in the same way.

2.2.2. DESCRIPTION OF SWITCH POS 17.

The switch in pos 17 controls the functions that are common to both banks.

BPR: Controls whether the banks are enabled or disabled after RESET. When the switch is ON both banks are disabled after RESET. Notice: after POWER UP both banks are disabled, and they cannot be enabled until 20 ms after POWER UP.

ADR(0): When the switch is ON the bank control address is FD. When the switch is OFF the bank control address is FC.

BITSEL(1:0): The two switches select two consecutive bits which enable/disable bank 0 and bank 1. In the table below is shown which bit controls bank 0 and which bit controls bank 1 for all four possibilities of BITSEL(1:0).

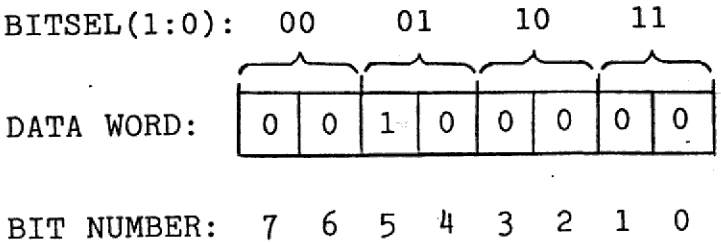
BITSEL(1:0)	bank 1	bank 0
00	7	6
01	5	4
10	3	2
11	1	0

Example:

Suppose ADR(0) is ON and BITSEL(1:0)=01.
The instructions

```
MVI     A,20
OUT     FD
```

will disable bank 0 and enable bank 1.



Bank 0 is enabled/disabled by an even numbered bit.
Bank 1 is enabled/disabled by an odd numbered bit.

3. THE HARDWARE.

ID-7037 is a dynamic memory module and demands some sort of refresh. This is usually done by ID-7038. The ID-7038 refreshes all the ID-7037 modules that are connected to the system bus.

Refresh is done every 14 microsecond. Each ID-7037 has its own refresh address counter while ID-7038 generates all the necessary control signals.

NOTICE: when the CPU is stopped the ID-7038 cannot refresh the memory, so do not stop the system when the dynamic memory should be refreshed by ID-7038.

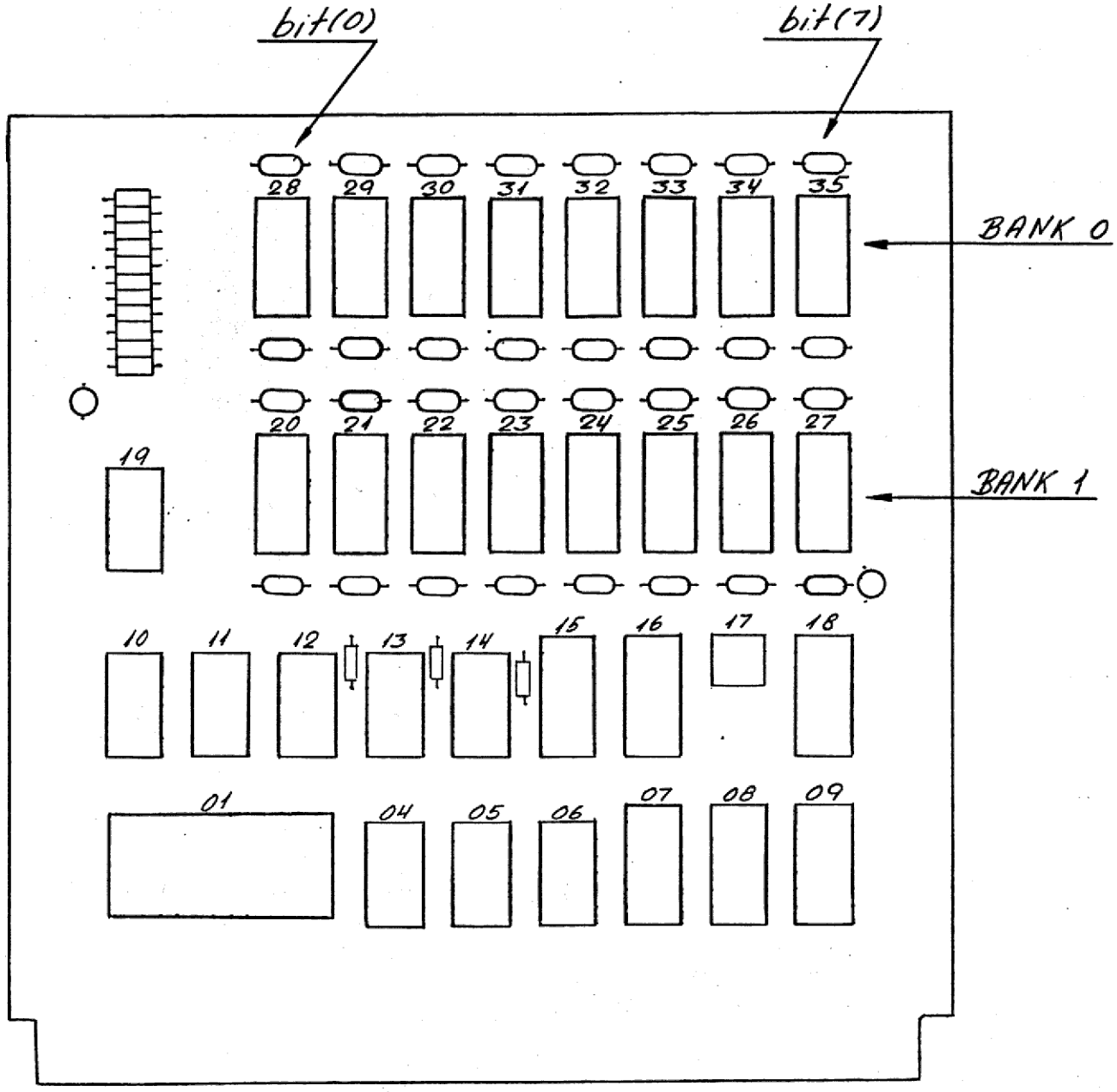

bit(0)
bit(7)
28
29
30
31
32
33
34
35
BANK 0
20
21
22
23
24
25
26
27
BANK 1
19
10
11
12
13
14
15
16
17
18
01
04
05
06
07
08
09

Figure 1

SWITCH SURVEY

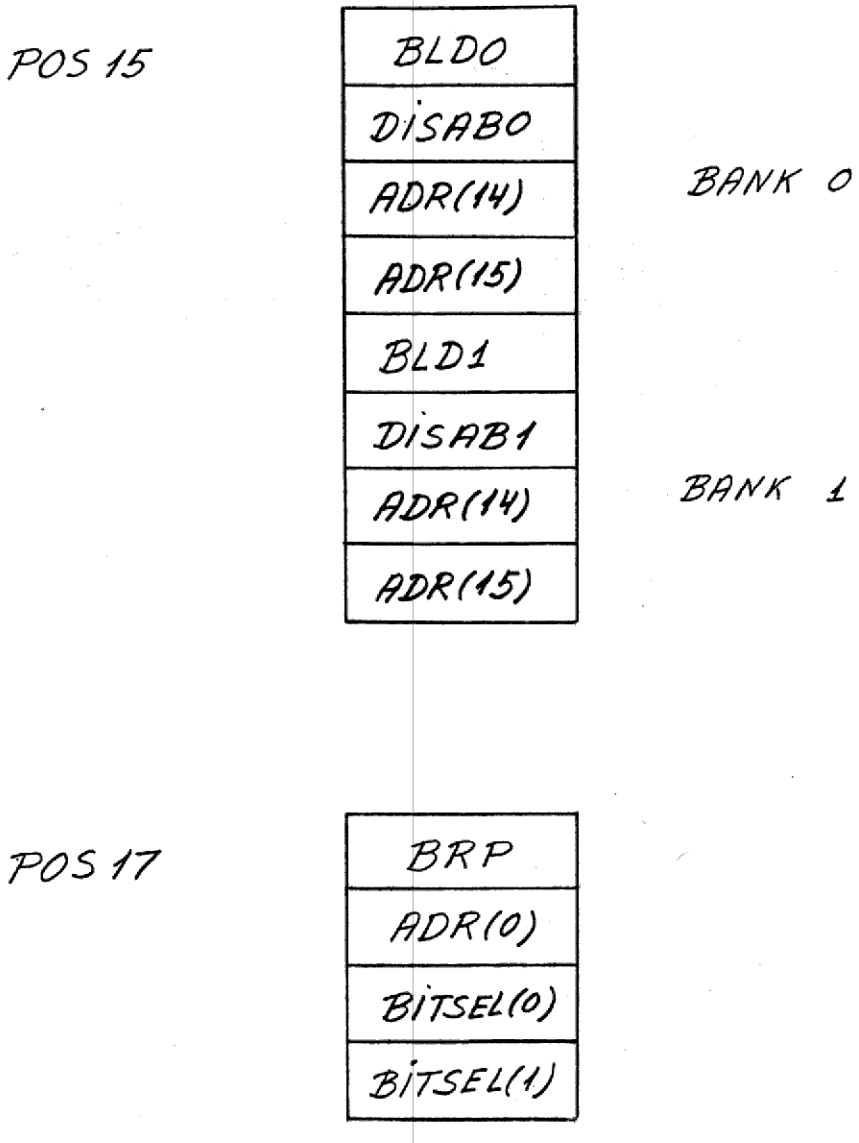
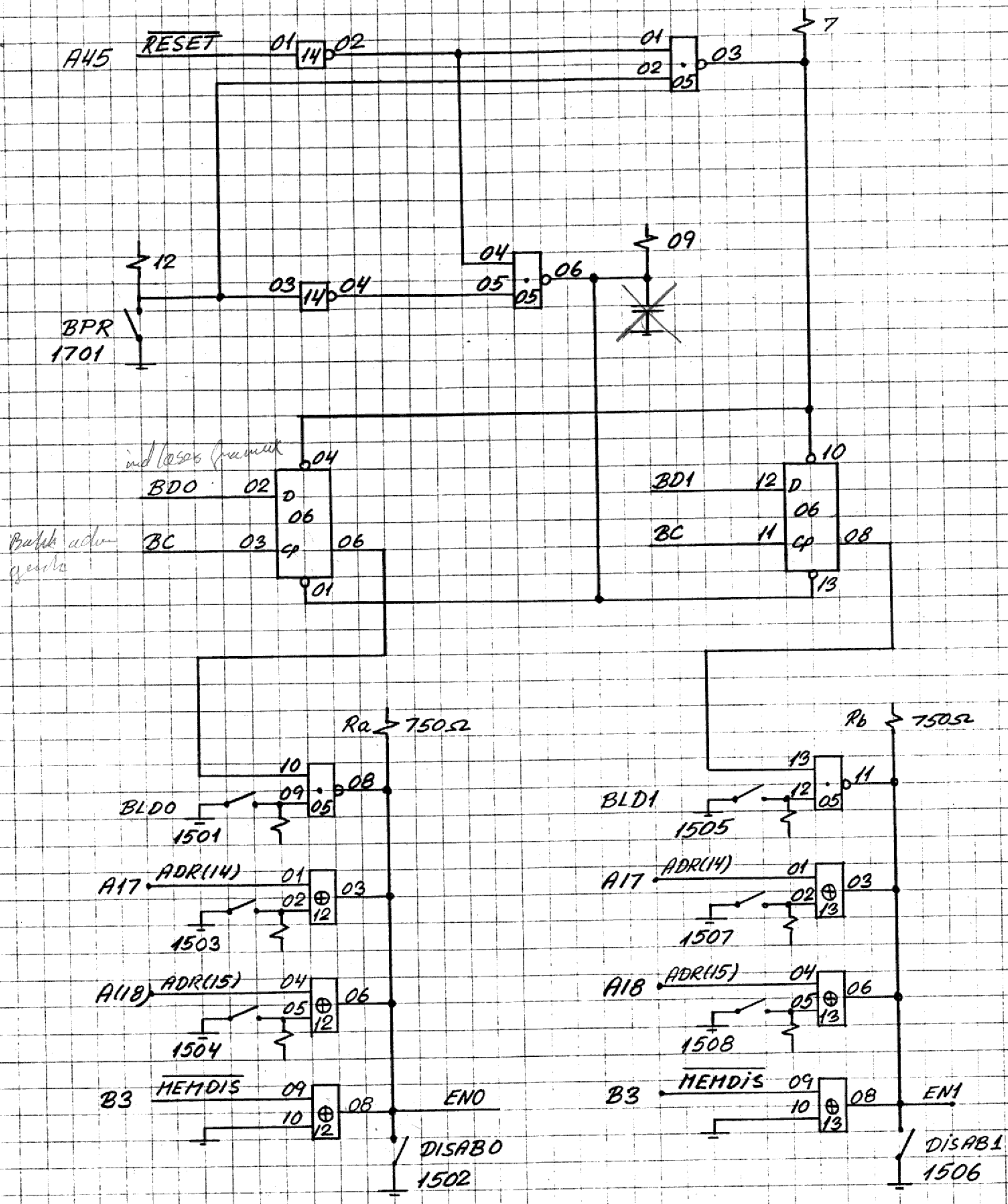
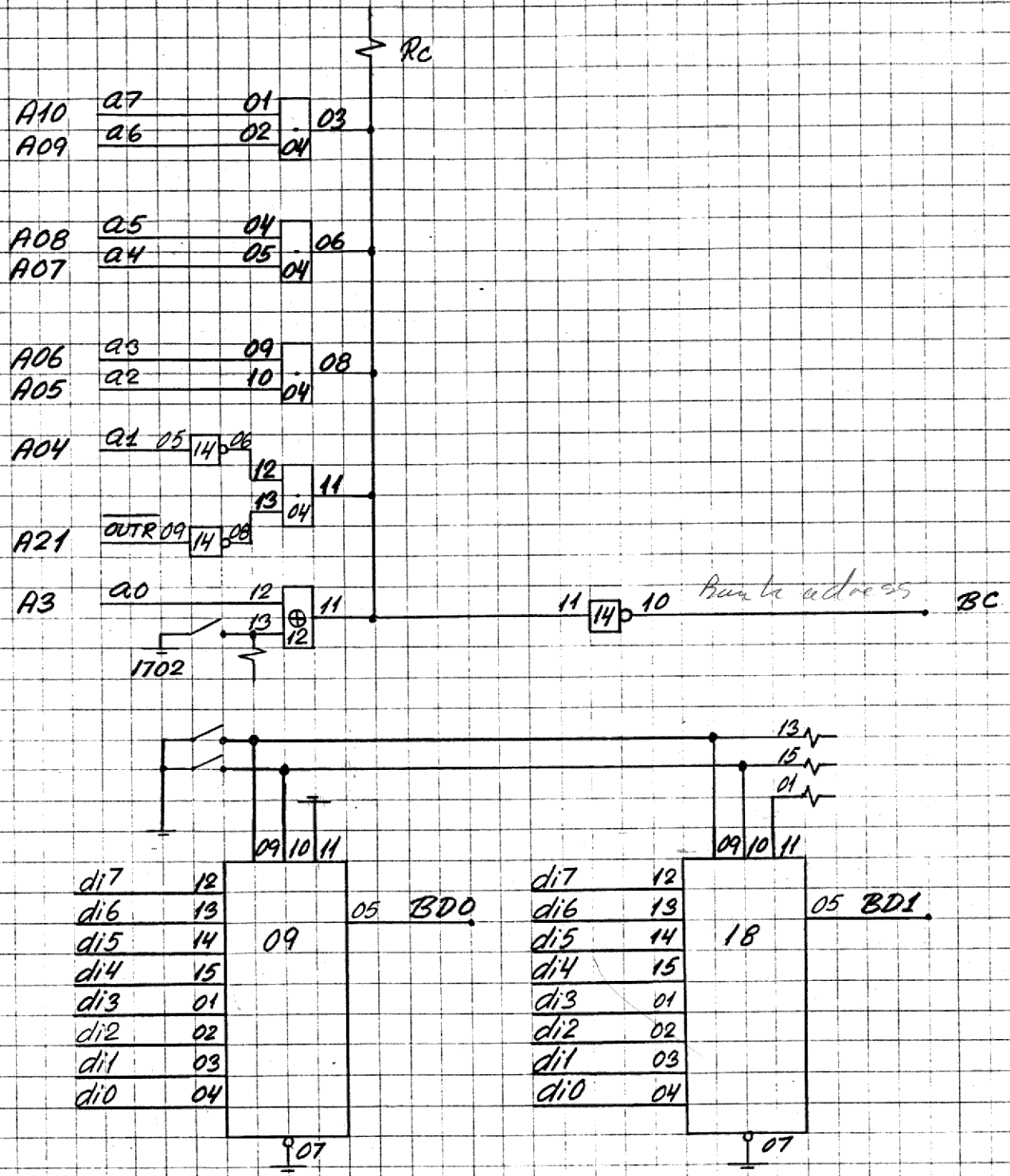
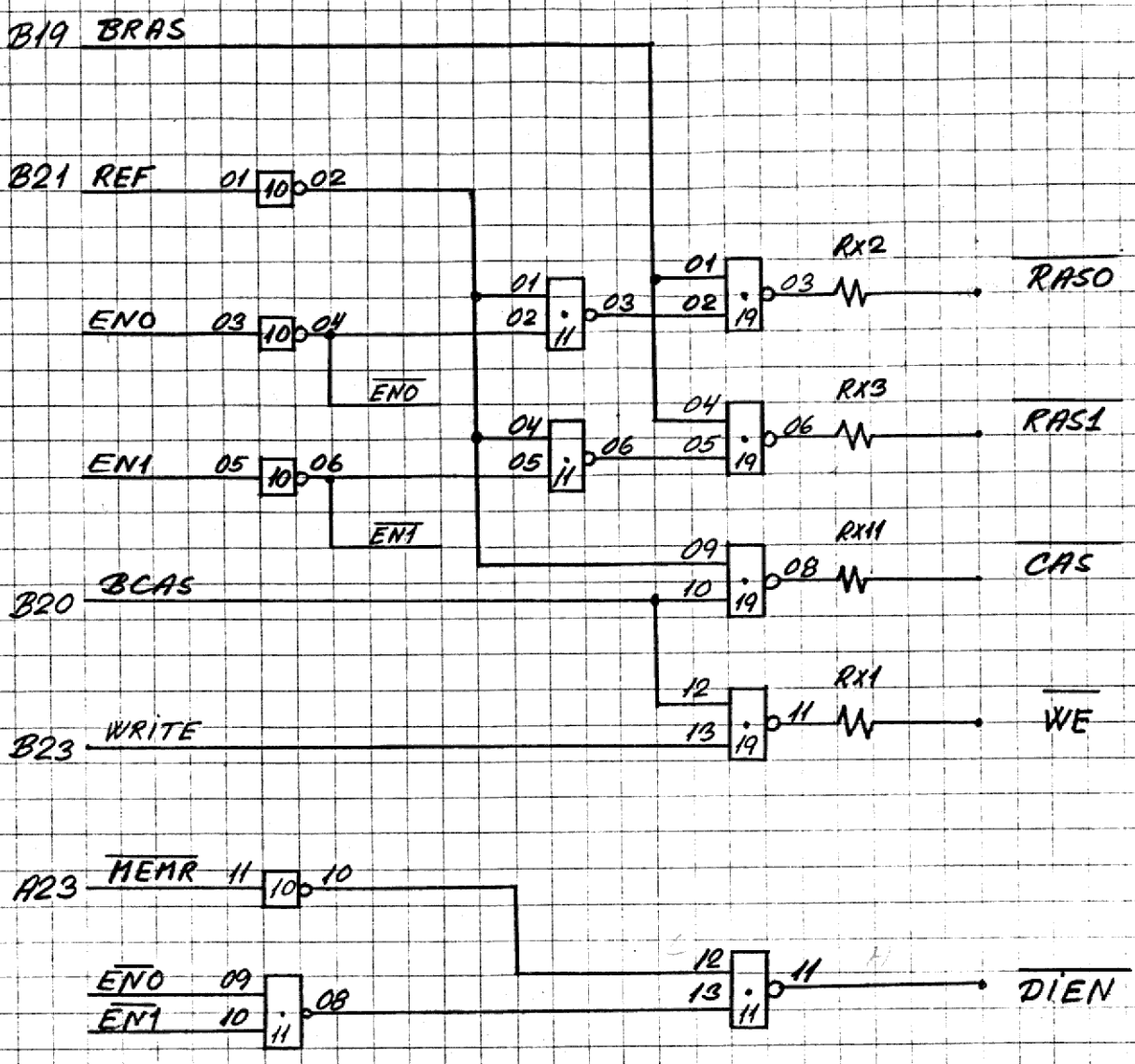
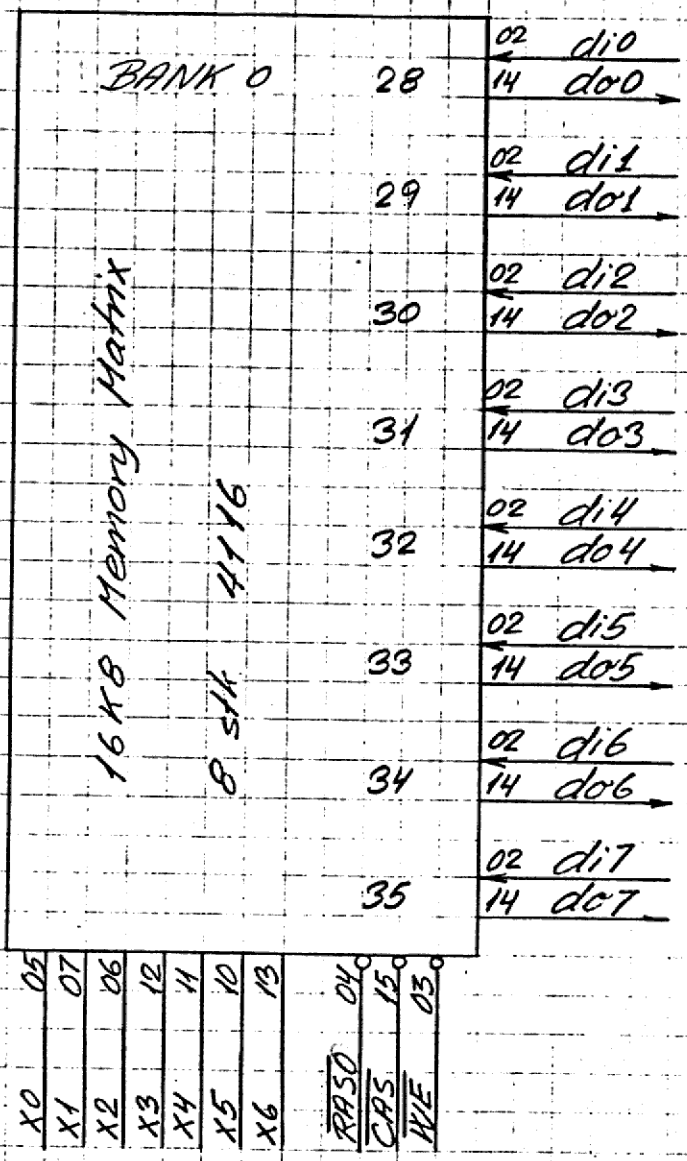


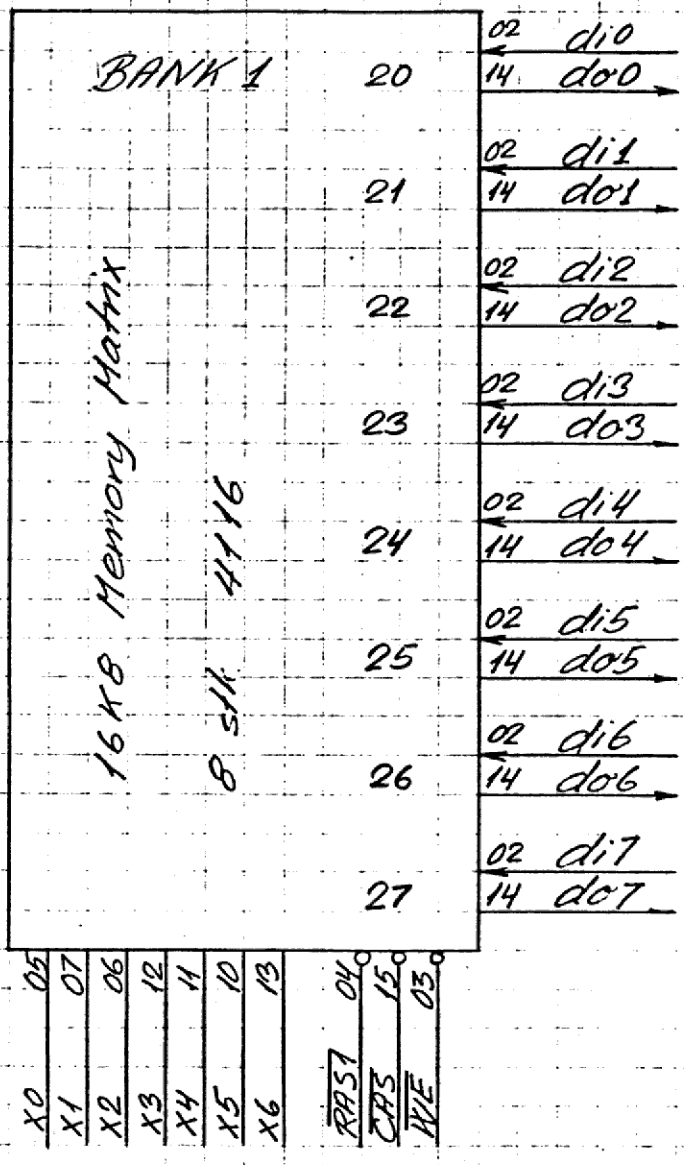
Figure 2

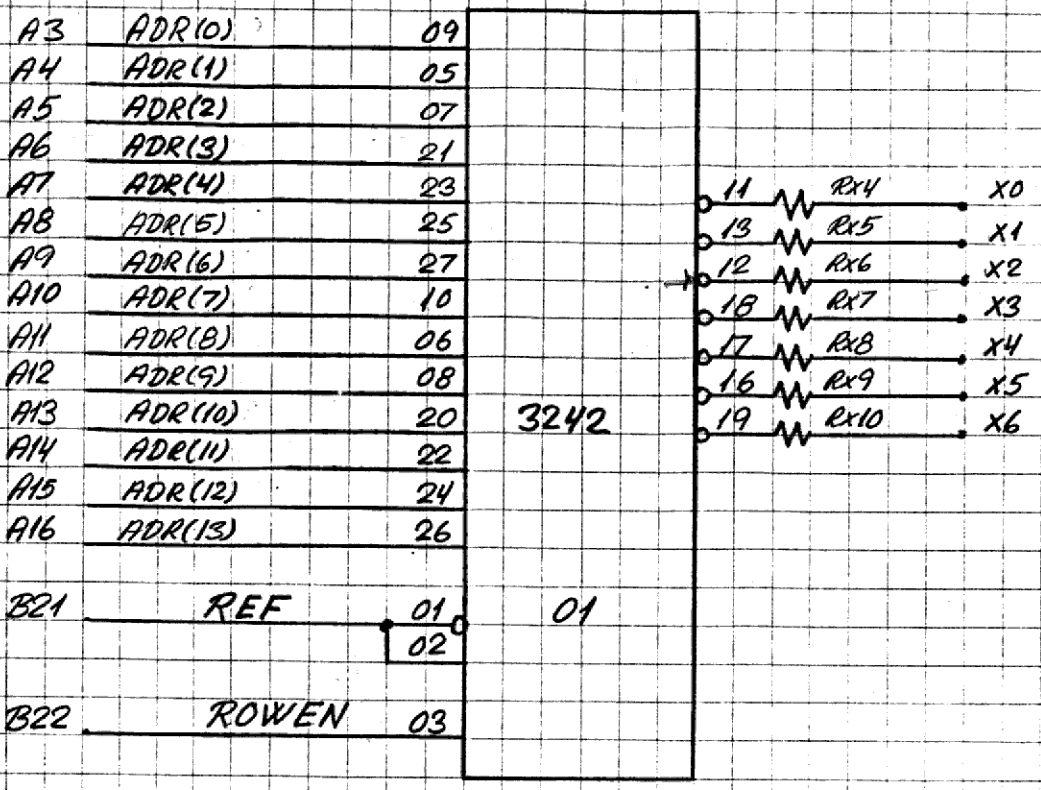

A45
RESET
01
14
02
01
02
05
03
7
12
03
14
04
04
05
05
06
09
BPR
1701
04
BDO
02
D
06
BC
03
cp
06
01
10
BD1
12
D
06
BC
11
cp
08
13
Ra
750Ω
10
09
05
08
BLDO
1501
A17
ADR(14)
01
02
12
03
1503
A(18)
ADR(15)
04
05
12
06
1504
B3
MEMDIS
09
10
12
08
ENO
DISABO
1502
Rb
750Ω
13
12
05
11
BLD1
1505
A17
ADR(14)
01
02
13
03
1507
A18
ADR(15)
04
05
13
06
1508
B3
MEMDIS
09
10
13
08
EN1
DISAB1
1506


Rc
A10
A09
a7
a6
01
02
03
04
A08
A07
a5
a4
04
05
06
04
A06
A05
a3
a2
09
10
08
04
A04
a1
05
14
06
12
13
11
04
A21
OUTR 09
14
08
A3
a0
12
13
11
12
1702
11
14
10
Bus ta address
BC
13
15
01
09
10
11
di7
di6
di5
di4
di3
di2
di1
di0
12
13
14
15
01
02
03
04
09
05
BD0
07
18
05
BD1
07


B19 BRAS
B21 REF
ENO
EN1
B20 BCAS
B23 WRITE
A23 MEMR
ENO
EN1
Rx2
Rx3
Rx11
Rx1
RAS0
RAS1
CAS
WE
DIEN

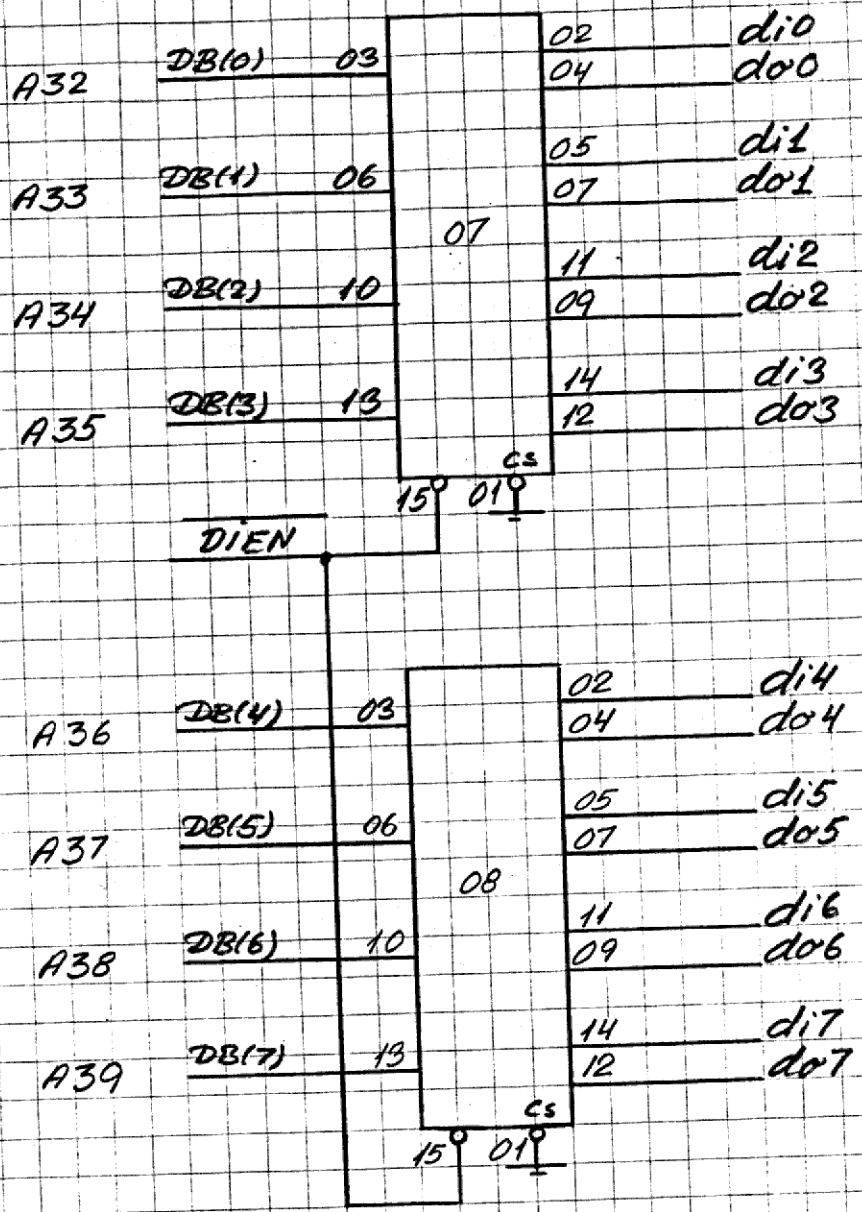

BANK 0
16 K 8 Memory Matrix
8 stk 4116
28
29
30
31
32
33
34
35
02 di0
14 do0
02 di1
14 do1
02 di2
14 do2
02 di3
14 do3
02 di4
14 do4
02 di5
14 do5
02 di6
14 do6
02 di7
14 do7
05 X0
07 X1
06 X2
12 X3
11 X4
10 X5
13 X6
04 RAS0
15 CAS
03 WE


BANK 1
16K8 Memory Matrix
8 stk 4116
20
21
22
23
24
25
26
27
02 di0
14 do0
02 di1
14 do1
02 di2
14 do2
02 di3
14 do3
02 di4
14 do4
02 di5
14 do5
02 di6
14 do6
02 di7
14 do7
05 X0
07 X1
06 X2
12 X3
11 X4
10 X5
13 X6
04 RAS1
15 CAS
03 WE


A3 ADR(0) 09
A4 ADR(1) 05
A5 ADR(2) 07
A6 ADR(3) 21
A7 ADR(4) 23
A8 ADR(5) 25
A9 ADR(6) 27
A10 ADR(7) 10
A11 ADR(8) 06
A12 ADR(9) 08
A13 ADR(10) 20
A14 ADR(11) 22
A15 ADR(12) 24
A16 ADR(13) 26
B21 REF 01
02
B22 ROWEN 03
3242
01
11 RX4 X0
13 RX5 X1
12 RX6 X2
18 RX7 X3
17 RX8 X4
16 RX9 X5
19 RX10 X6

98 → 50 (50-1)*2

0 1


A32
DB(0)
03
A33
DB(1)
06
A34
DB(2)
10
A35
DB(3)
13
07
02
di0
04
do0
05
di1
07
do1
11
di2
09
do2
14
di3
12
do3
Cs
15
01
DIEN
A36
DB(4)
03
A37
DB(5)
06
A38
DB(6)
10
A39
DB(7)
13
08
02
di4
04
do4
05
di5
07
do5
11
di6
09
do6
14
di7
12
do7
Cs
15
01

Protective Circuit

Initialer/dato	Side
KAN 790206	13
Revideret	Projekt 7037