ID-7042

Serial Bus Module

ID-7000 System

Dansk Data Elektronik ApS

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1. General Description:

The ID-7042 Serial Bus Module is used to transmit and receive information from a maximum of 64 slave units (SU's) connected to one 5 wire cable. I/O-signals are CMOS-compatibel (÷5V-+5V).

The principle of operation is as follows:

The module transmit a clock frame of 64 clock cycles on 2 balanced clocklines. The SU's on the cable are programmed to transmit and receive information in one specific clock cycle. Using both clock half-cycles, two bits of information can be tranferred between the ID-7042 module and the SU in one complete clock frame. To synchronize the SU's to the clock frame, a delay of a certain minimum time (depending of the SU-design) should be present between clock frames.

The clock rate of the clock frame can be strapselected to 1KHz, 2KHz, 4KHz and 8KHz.

During the clock frame, data are tranferred between the module and the CPU 16 times for 4 units each. The module contains a buffer register for data in either direction. The data tranfer between module and CPU can be interrupt driven or based on status polling. An overrun/underrun condition during a clock frame is detected and signaled to the CPU via the status word.

A special output signal, AUX, is available for all the SU's connected to the module. Also a $\pm$ 5V powersupply for the SU's is available in the cable connector.

Appendix 1 contains a complete logic schematic of the module.

2. Programming Description.

2.1 Addressing. The module uses four concecutive I/O-addresses. The base address of the module is determined by a 6 bit switch-register on the module.

2.2 Output Functions.

OUT 4n+0: Data is tranferred from the CPU accumulator to the output buffer register of the module.

BU4	BU3	BU2	BU1	AU4	AU3	AU2	AU1
7	6	5	4	3	2	1	0

The data elements AU1, BU1 are transferred to the first SU in a group of four. AU2, BU2 to the next SU etc. The AU data element is transferred in the first clock half-cycle; the BU element in the last clock half-cycle. Execution of an OUT 4n+0 instruction, resets the READY flip-flop of the module.

OUT 4n+1: Execution of this OUT instruction starts a new clock frame. Before this, the data elements to the first 4 SU's should be loaded using the OUT 4n+0 instruction. The content of the accumulator is irrelevant when the OUT 4n+1 instruction is executed.

OUT 4n+2: This instruction loads the interrupt mask flip-flop, MASK, of the module. Furthermore the state of the output line, AUX, is determined:

					MASK		AUX
7	6	5	4	3	2	1	0

bit 0: AUX
- 1: AUX-line is activated (+5V)
- 0: AUX-line is deactivated (÷5V)

bit 1: not used

bit 2: MASK
- 1: SID-interrupt enabled
- 0: SID-interrupt disabled

bit 7:3:not used

OUT 4n+3: Not used, no function.

2.3 Input

IN 4n+0: This instruction transfers 8 data elements from the input buffer register of the module to the accumulator of the CPU.

BI4	BI3	BI2	BI1	AI4	AI3	AI2	AI1

AI1 and BI1 are data elements from the first SU in a group of four. AI2, BI2 from the next etc. AI is transferred in the first clock half-cycle; BI in the last clock half-cycle.

IN 4n+1: This instruction transfers the status register of the module to the accumulator of the CPU

7	6	5	4	3	2	1	0
				DATAI	MASK	OE	READY

bit 0: READY — This status bit is 1 if the output buffer register of the module is ready to receive data and the input buffer register is loaded with data elements from the SU's[++]

bit 1: OE — Overrun Error. This status bit is set when the module is not served correctly by the CPU during a clock frame. The status bit is reset when a new clock frame is started.

bit 2: MASK — This status bit indicates the content of the interrupt mask flip-flop of the module, as determined by the OUT 4n+2 instruction.

[++] The first time the READY-flag is activated after starting the CLOCK-frame (using the OUT 4n+1 instruction) no data are present in the input buffer. At this time the output buffer register can be loaded with data elements for SU no.5,6,7 and 8.

bit 3: DATAI: This status bit directly indicates the state of the data input line of the module:

DATAI=1 Data input line active(-5V)

DATAI=0 Data input line passive(+5V)

bit 7:4: undefined

IN 4n+2: Not used

IN 4n+3: Not used

2.4 Interrupt: The module has two interrupt sources: The READY-interrupt and the SID-interrupt. The READY-interrupt source is equal to the READY-flag of the module. The SID-interrupt is generated if the data input line is active and the MASK flip-flop is set. The state of the data input line is also available in the status word of the module. The interrupt sources of the module can be connected to the different interrupt request lines $\overline{IR(7:0)}$ using a 16 pin component board (fig.1). The interrupt sources are open collector, active low types, and may be "wire-or'ed" to other interrupt sources.

$\overline{READY}$	01	0	$\overline{IR(7)}$
	02	0	$\overline{IR(6)}$
	03	0	$\overline{IR(5)}$
	04	0	$\overline{IR(4)}$
$\overline{SID-MASK}$	05	0	$\overline{IR(3)}$
	06	0	$\overline{IR(2)}$
	07	0	$\overline{IR(1)}$
	08	0	$\overline{IR(0)}$

fig. 1 Interrupt Strapping

3. Electrical Specifications.

3.1 Interface to Slave Units (SU's).

The interface to the slave units is performed via an onboard DE9S connector. The interface contains the following signals:

pin 1: KLOK P pin 2: KLOK N	These lines contains the clock frame from the module. The signal levels are 0V and -2V, 180 degrees out of phase. Output impedance 100Ω.
pin 3: DATAO	This line transfer serial data from the module. The signal levels are -5V (line passive) and +5V (line active). Output impedance 100-300Ω.
pin 4: $\overline{\text{DATAI}}$	This line transfers serial data from the SU's to the ID-7042 module. The signal level should be nominel $\pm$5V, +5V corresponding to passiv line and -5V corresponding to an active line. The input threshold i 0V. The module has a pull-up resistor of 1KΩ to +5V. In this way, the input line could be driven by open collector outputs on the SU's driving the line to a negative potential when active.
pin 5: -V	Negative supply optionally used by the SU's.
pin 6: GND	Ground reference of the interface.
pin 7: +V	Positive supply optionally used by the SU's.
pin 8: not used	

pin 9: AUX — This lines transfers the content of the AUX-flip-flop to the SU's. Signal levels as DATAO-signal.

To protect against shorts, the power supplies of the computer system are connected to the interface via two on-board fuses. The interface power supply may optionally be taken from lines B7 and B8 in the microcomputer bus system.

3.2 Timing.

Fig. 2 shows the timing relationships of the module. In this timing diagram Q_0 to Q_3 refers to an on-board counter. Q_1 is an on-board clock signal with the same clock rate and phase as the clock frame in the SU's.

The AU-information is shifted to the DATAO-line on first $Q_0\uparrow$ and is sampled in the SU on $Q_1\downarrow$. The BU-information is shifted to the DATAO-line on second $Q_0\uparrow$ and sampled in the SU on $Q_1\uparrow$. The AI-information is gated to the $\overline{\text{DATAI}}$-line by the SU in the positive Q_1 clock half-cycle and sampled by the module on first $Q_0\uparrow$. The BI-information is gated to the $\overline{\text{DATAI}}$-line by the SU in the negative Q_1 clock half-cycle and sampled by the module on second $Q_0\uparrow$. Using a strap area on the module, the clock rate of Q_1 (and the SU-clock) can be selected to 1KHz, 2KHz, 4KHz and 8KHz.

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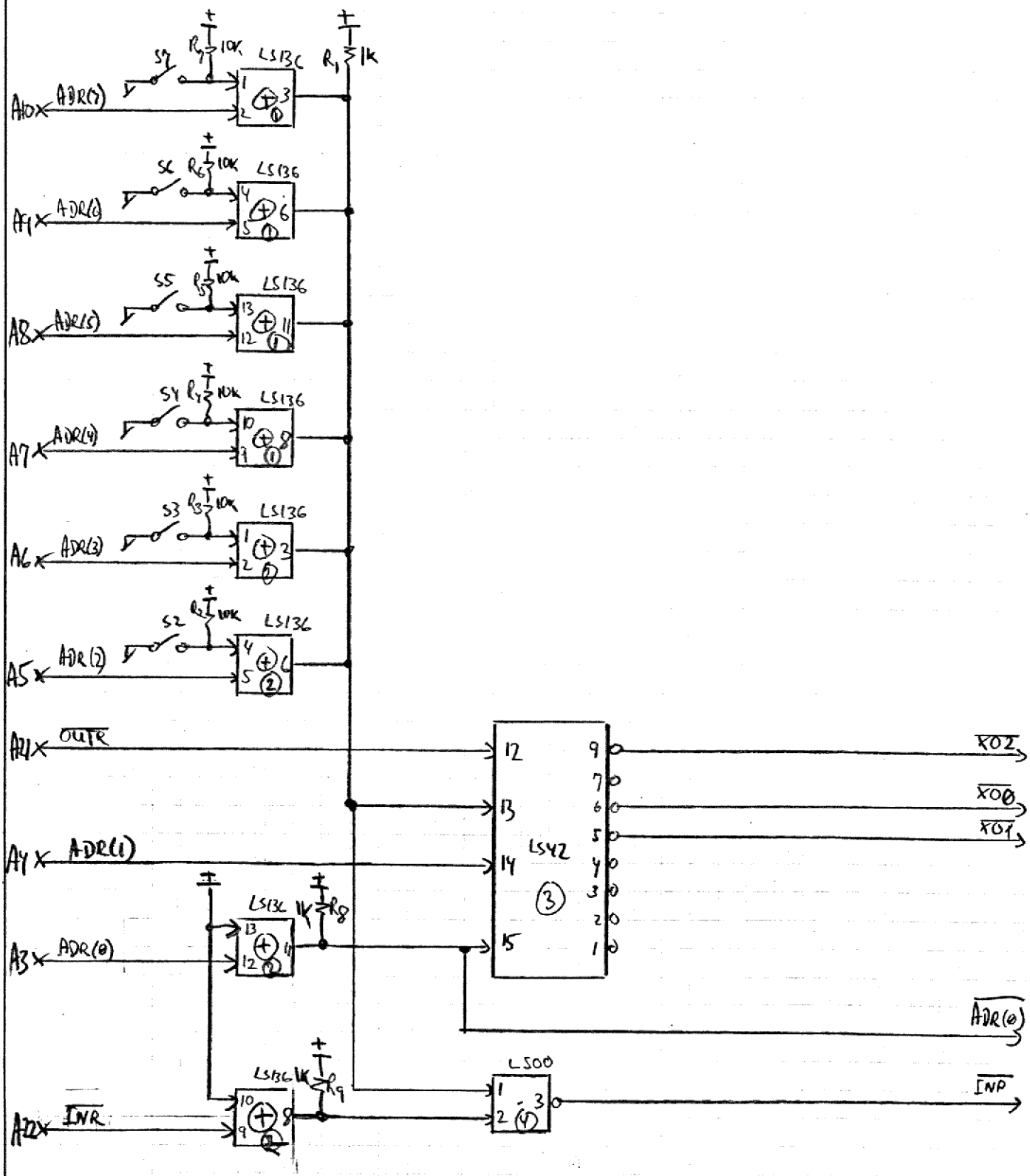
ID-7042 serial bus module

Logic Schematic: Address decode and control

Initialer/dato	Side
OL 4-2-78	1
Revideret	Projekt



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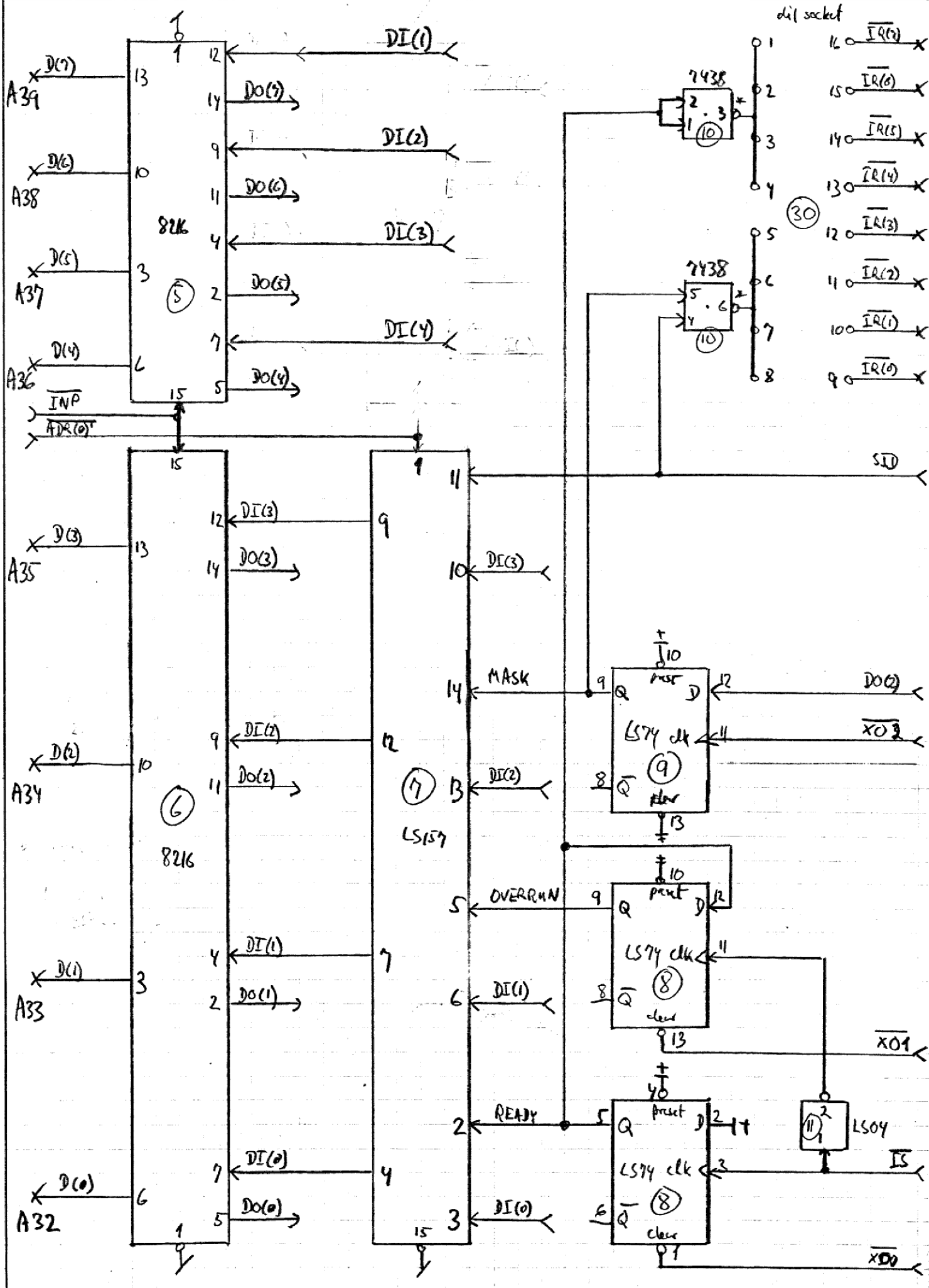
ID-7042 Serial bus module

Logic Schematic: Data bus, Status Reg and Interrupt logic.

Initialer/dato	Side
OL-4-2-78	2
Revideret	Projekt



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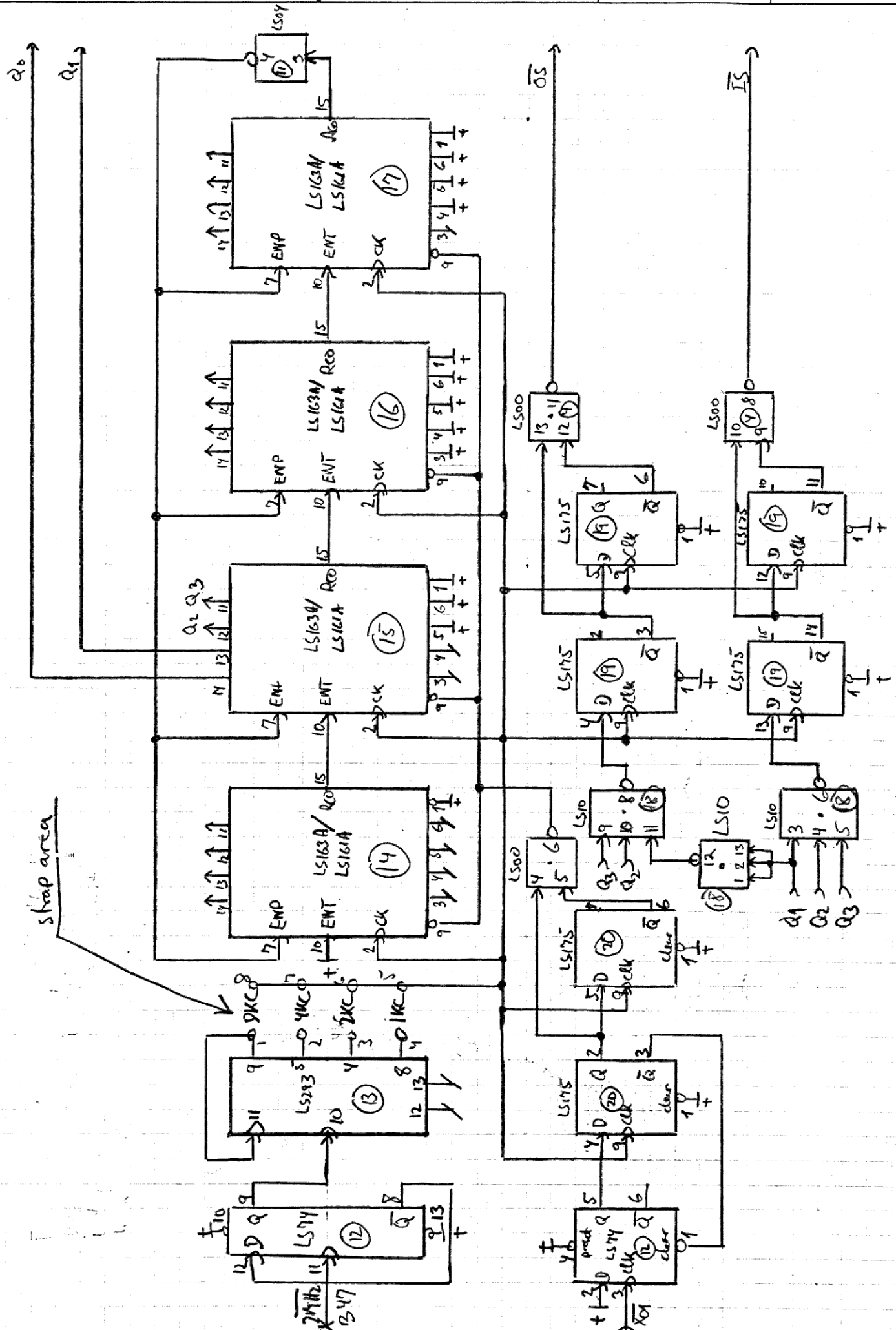
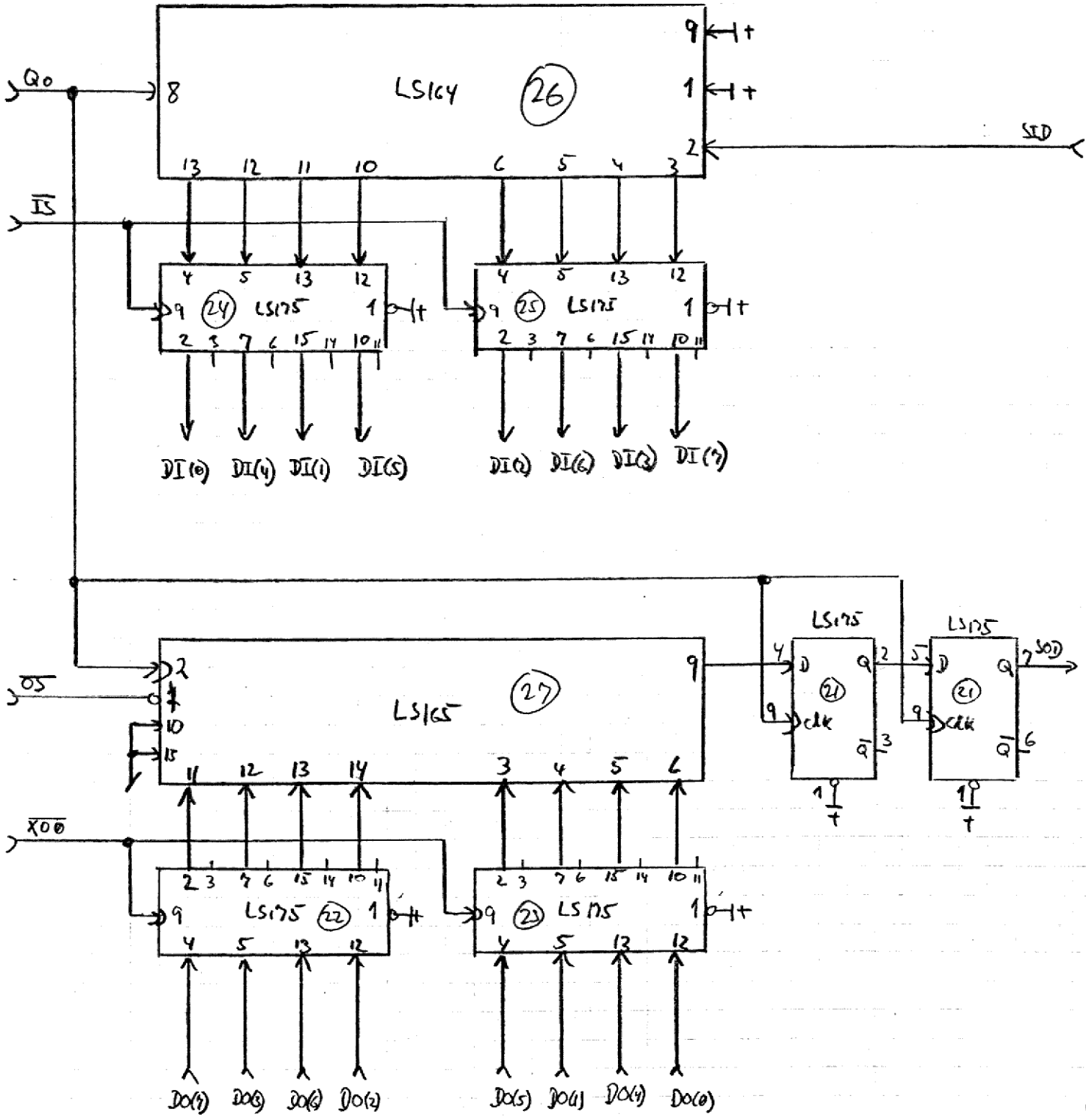
Logic Schematic: Timing generator.

Initialer/dato	Side
OL 4-2-78	3
Revideret	Projekt




Qo
LS164
26
SID
IS
LS175
24
25
DI(0) DI(4) DI(1) DI(5)
DI(3) DI(6) DI(2) DI(7)
OS
LS165
27
LS175
21
SOD
XOO
LS175
22
23
DO(7) DO(3) DO(6) DO(2)
DO(5) DO(1) DO(4) DO(0)

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ID-7042 Serial b/w module

Logic Schematic: Communication Interface

Initialer/dato	Side
OL 4-2-28	5
Revideret	Projekt