DANSK DATA ELEKTRONIK

ID-7045 FLOPPY DISK CONTROLLER

for the

ID-7000 MICROPROCESSOR SYSTEM

November 1979

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1. DESCRIPTION.

THE ID-7045 MODULE comes in two different versions X and Y depending upon the actual components installed on the module.

The X version controls a maximum of three 5" mini floppy disk drives, while the Y version controls a maximum of four 8" normal floppy disk drives. In both cases the drives may be single or dual headed and the recording method may be FM or MFM.

The key component on the ID-7045 module is the FD 1791 Floppy Disk Controller which is described in appendix 1.

2. ADDRESSING.

The ID-7045 module uses eight addresses. When ADR(2)=0 the FD 1791 controller is addressed and ADR(1:0) selects the various registers in the FD 1791 controller as described in appendix 1. When ADR(2)=1 an external control register ECR(7:0) is addressed and ADR(1:0) is not used.

The address of the module is selected by a switch on the module. ADR(7:3) is compared with the switch register and if there is a match a card select signal is generated.

3. EXTERNAL CONTROL REGISTER.

The external control register is named ECR. The bits in ECR have the following meaning:

ECR(1:0)	: Selects the disk drive.
ECR(2)	: Disables the disk drive.
ECR(3)	: Motor ON; see comments below.
ECR(4)	: Not used.
ECR(5)	: Side.
ECR(6)	: Single density.
ECR(7)	: Not used.

Comments: If ECR(1:0)=11 no disk drive is selected in the X version. This is equivalent to ECR(2)=1. If ECR(3)=1 the motor is running in the X version while it is stopped in the Y version.

If a single sided diskette is placed in a dual headed disk drive you must use ECR(5)=0.

NOTICE: Data is complemented before ECR is loaded.

4. PROGRAMMING.

The module allows DMA or non DMA transfers. When non DMA tranfers are used the program must read the status of the controller in order to determine if a new byte is ready to be transferred.

When selecting head stepping rate you must know the clock rate which is 1 MHz for the X version and 2 MHz for the Y version.

5. INTERRUPTS.

The module has two interrupt sources, INTRQ from the FD 1791 floppy disk controller and INTDMA form the DMA channel. INTRQ is described in appendix 1. INTDMA is active when the word-count in the associated DMA channel equals zero. The interrupt INTDMA is cleared when you read the status of the controller or when you send a new command to the controller. By a strap on the module you can connect the interrupt source to the interrupt request lines IR(7:0).

Notice: You cannot use programmed interrupt driven data transfers as DRQ cannot be connected to IR(7:0).

Version X: 5" Mini Floppy Disk Interface.

PIN	SINAL NAME
2	HEAD LOAD
4	.....
6	READY
8	INDEX/SECTOR
10	DRIVE SELECT 0
12	DRIVE SELECT 1
14	DRIVE SELECT 2
16	MOTOR ON
18	DIRECTION IN
20	STEP
22	WRITE DATA
24	WRITE GATE
26	TRACK 00
28	WRITE PROTECT
30	READ DATA
32	SIDE
34	.....

Odd numbered pins: GROUND

Connector: 3M 3431-100 flat cable connector

Version Y: 8" Floppy Disk Interface.

PIN	SIGNAL NAME
02	.....
04	MOTOR OFF
06	.....
08	LOI
10	.....
12	.....
14	SIDE 2
16	.....
18	.....
20	INDEX
22	READY
24	.....
26	SELECT 0
28	SELECT 1
30	SELECT 2
32	SELECT 3
34	STEP IN
36	STEP
38	WRITE DATA
40	WRITE GATE
42	TRACK ZERO
44	WRITE PROTECT
46	READ DATA
48	.....
50	.....

ODD numbered pins: Ground.

Connector: 3M 3433-100 flat cable connector.

WESTERN DIGITAL
CORPORATION

FD1791A/B Floppy Disk Formatter/Controller

FEATURES

- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- READ MODE
  - Single/Multiple Record Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- WRITE MODE
  - Single/Multiple Record Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Selectable Head Settling and Head Engage Times
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers Comprehensive Status Information
- WRITE PRECOMPENSATION (MFM AND FM)
- WINDOW EXTENSION (IN MFM)
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY

APPLICATIONS

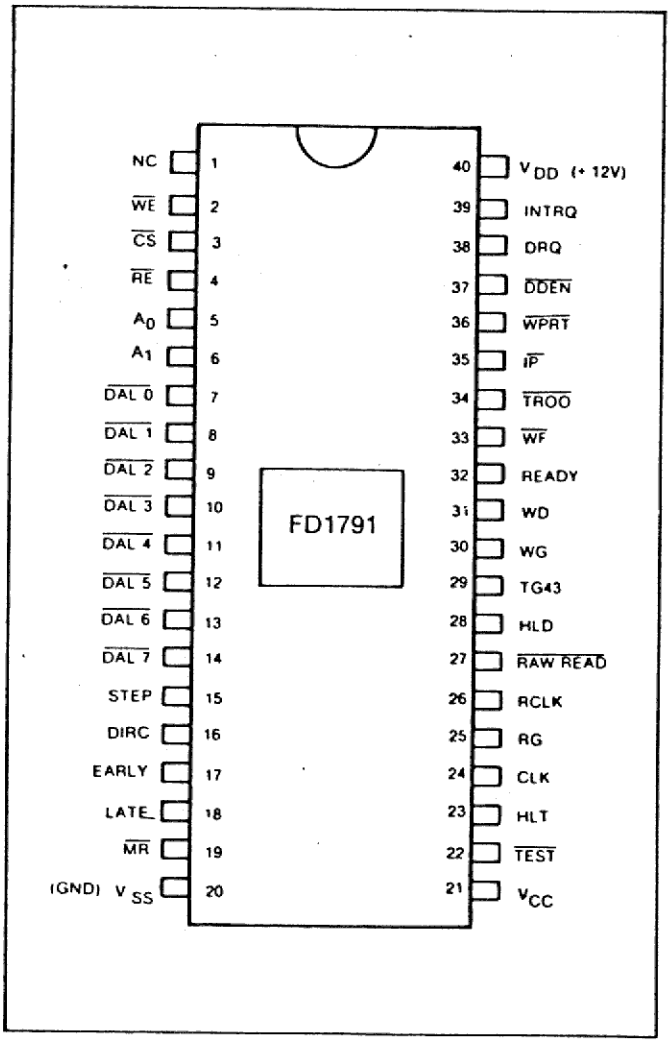
FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
NEW MINI-FLOPPY CONTROLLER

GENERAL DESCRIPTION

The FD1791 is a MOS LSI device which performs the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD1791, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD1791 contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD1791 designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

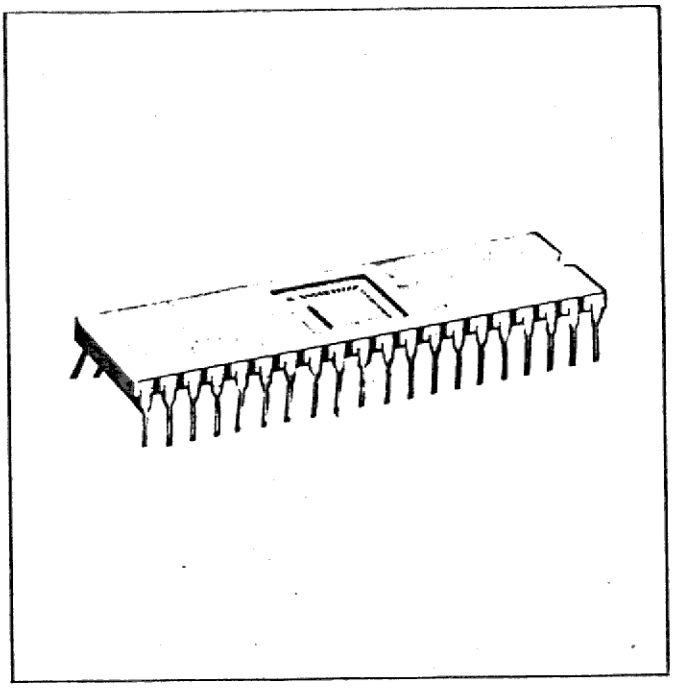
The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD1791 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1791 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs.



PIN CONNECTIONS

Uldvejen 10
DK-2970 Hørsholm
☎ 02-*5708 88



ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 3. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

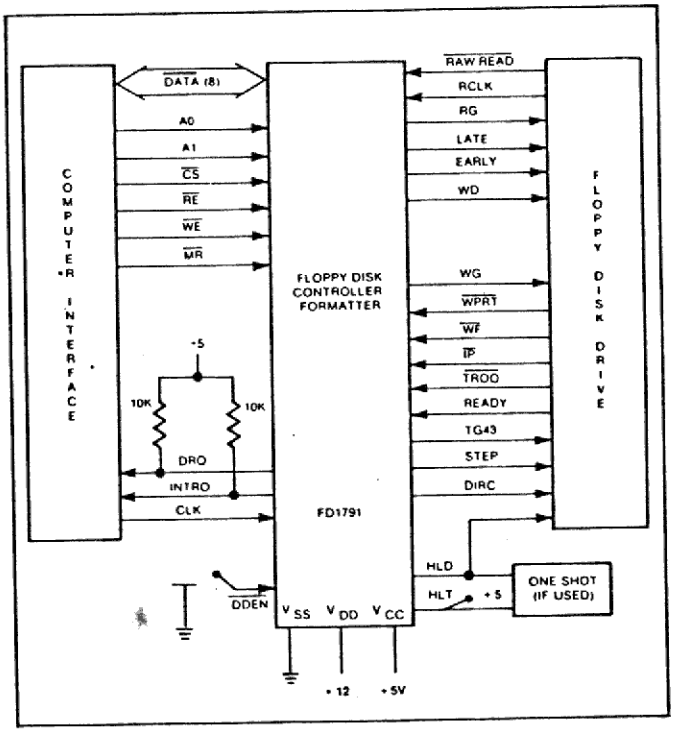
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

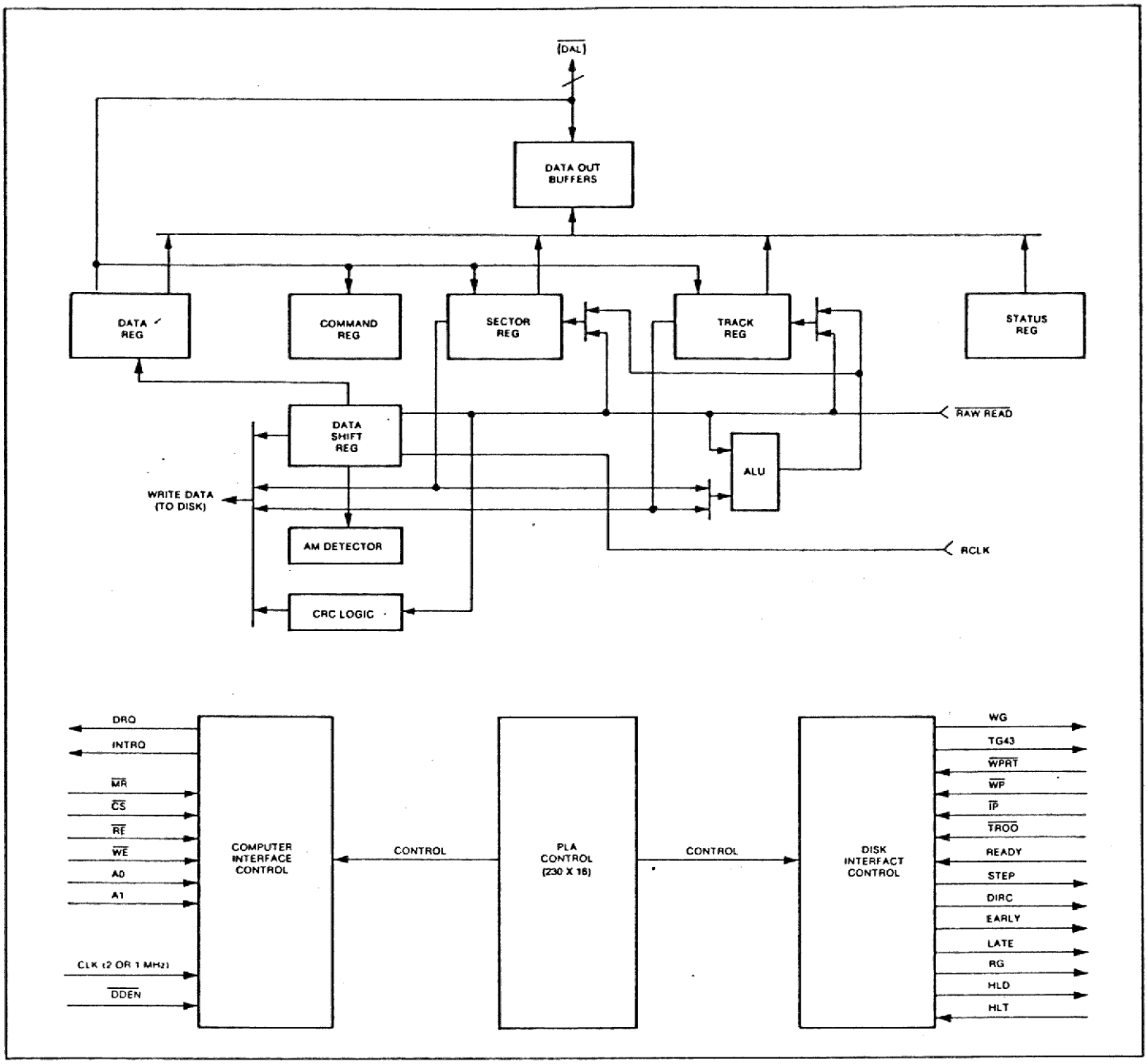
Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.



1791 SYSTEM BLOCK DIAGRAM



FD1791 BLOCK DIAGRAM

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD1791. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The least-significant address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1791 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by

the processor. If the Data Register is read after one or more characters are lost, by having new data transferrd into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 1791 has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type 2 or 3 command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

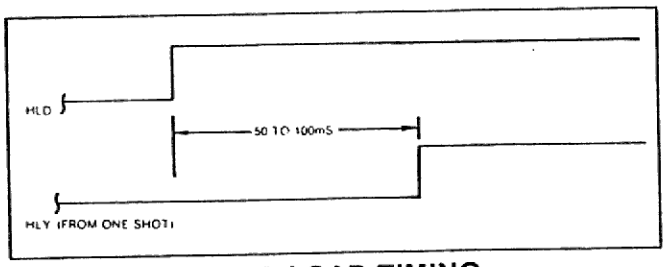
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD1791 must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1		
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3 ms	3 ms	6 ms	6 ms	Approx.	Approx.
0 1	6 ms	6 ms	12 ms	12 ms	200 μs	400 μs
1 0	10 ms	10 ms	20 ms	20 ms		
1 1	15 ms	15 ms	30 ms	30 ms		

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD1791 is in an idle state (non-busy) and 15 index pulses have occurred, it is reset.

Head Load Timing (HLT) is an input to the FD1791 which is used for the head engage time. When HLT = 1, the FD1791 assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD1791.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD1791 will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD1791 waits for HLT to be

true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD1791 then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true, with E flag on HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector Length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD1791 is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD1791 is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

For read operations, the FD1791 requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loop, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which informs some phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD1791 must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD1791 is deriving any useful information from the data stream. Similarly for MFM, RG is made active true when 4 bytes of "00" or "FF" are detected. The FD1791 must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1791 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1791 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the $\overline{\text{Write Gate}}$ output becomes inactive.

For write operation, the FD1791 provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$ = 1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. EARLY is valid for the duration of the pulse. LATE is active true when the WD pulse is to be written late. If both are low when a WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD1791. The write precompensation signals EARLY and LATE are valid in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD1791 samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD1791 will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1.

Table 2. COMMAND SUMMARY

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	X	E	0	0
II	Write Command	1	0	1	m	X	E	X	a_0
II	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	X
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_0

X = Don't care
Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on last track
V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

Table 4. FLAG SUMMARY

TYPE II

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

a_0 = Data Address Mark (Bit 0)

a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay

E = 1, 15 ms delay

E = 0, no 15 ms delay

Table 5. FLAG SUMMARY

TYPE IV

Ii = Interrupt Condition flags (Bits 3-0)

I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to Not-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt

The Type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1791 receives a command that specifically disengages the head. If the FD1791 is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD1791 terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{\text{TROO}}$) input is sampled. If $\overline{\text{TROO}}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{\text{TROO}}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{\text{TROO}}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{\text{TROO}}$ input does not go active low after 255 stepping pulses, the FD1791

terminates operation, interrupts, and sets the Seek error status bit. Note that the Restore command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

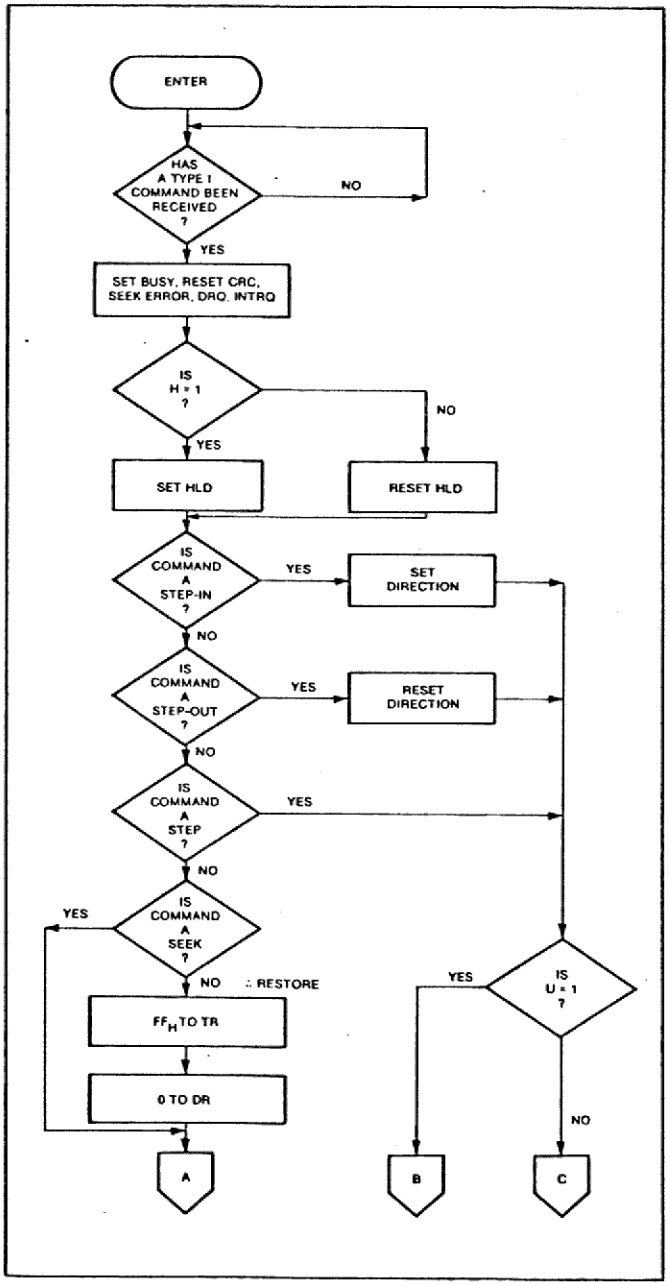
This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1791 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

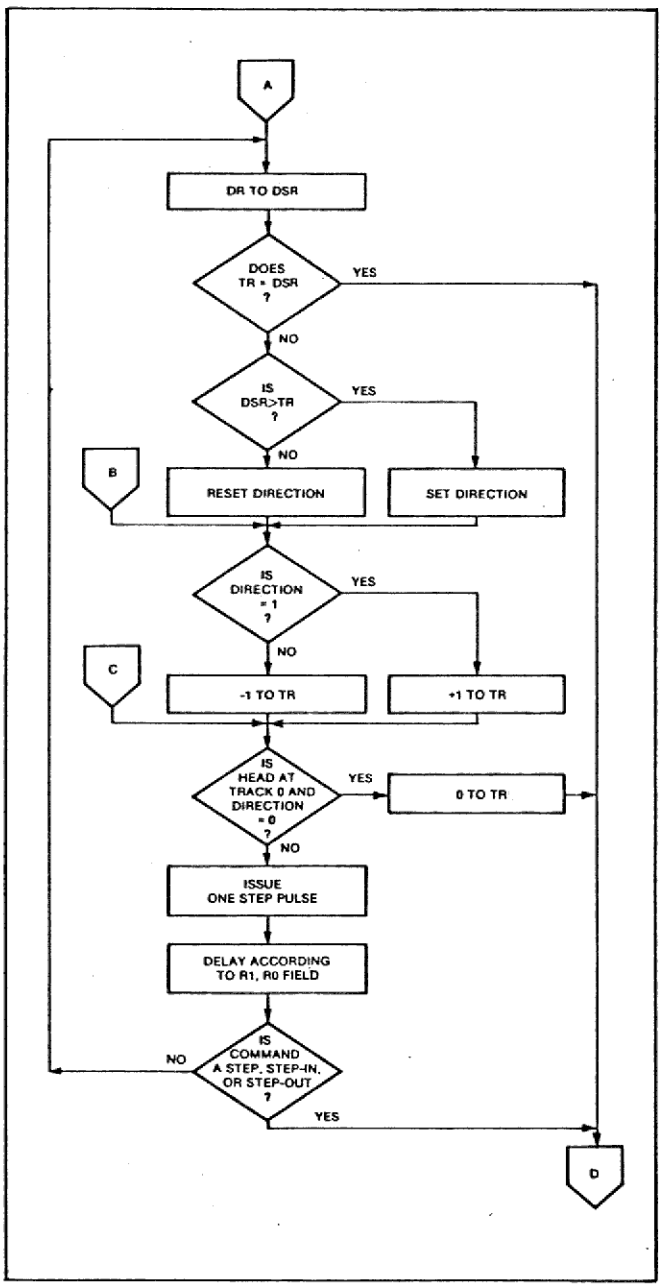
Upon receipt of this command, the FD1791 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD1791 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.



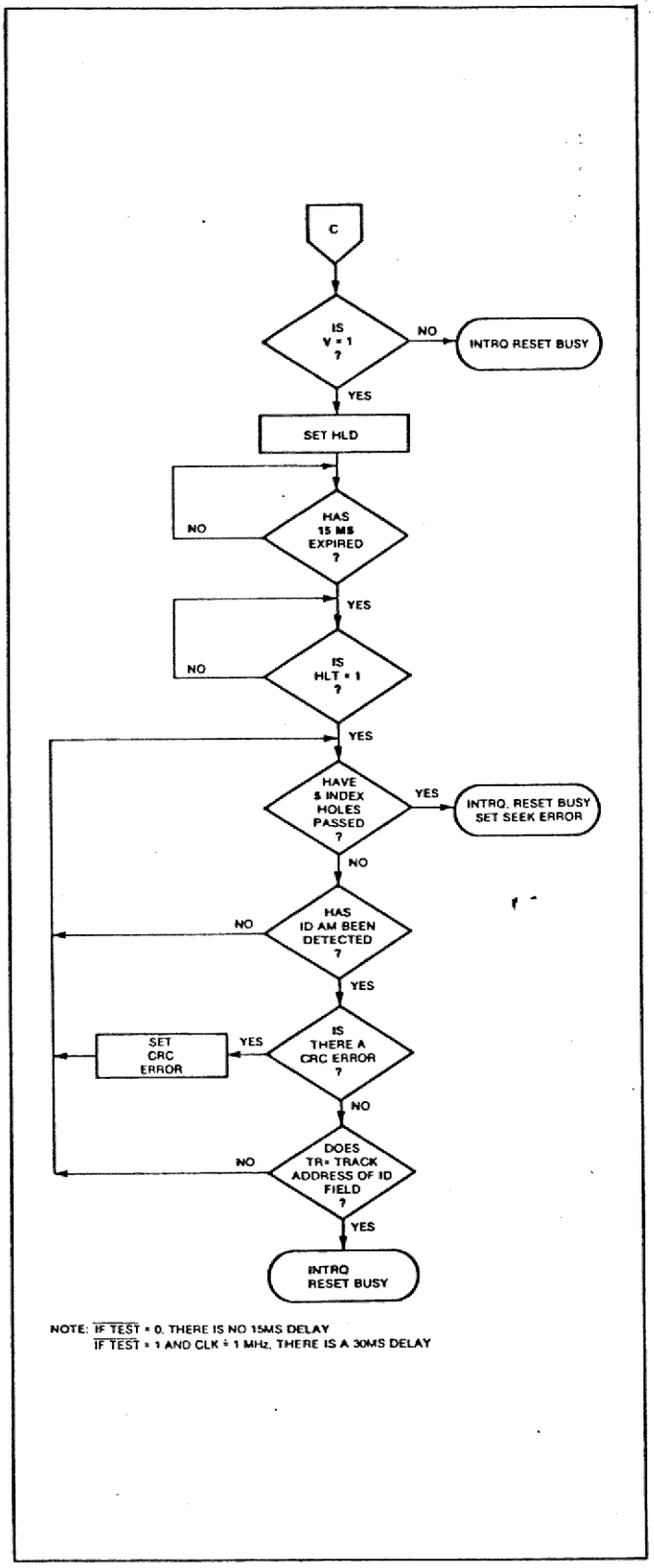
TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

STEP-OUT

Upon receipt of this command, the FD1791 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows thee start of the command. An interrupt is generated at the completion of the command.



NOTE: $\overline{\text{IF TEST}}$ = 0, THERE IS NO 15MS DELAY
$\overline{\text{IF TEST}}$ = 1 AND CLK = 1 MHz, THERE IS A 30MS DELAY

TYPE I COMMAND FLOW

TYPE II COMMANDS

The type II Commands include the Read Sector (s) and Wriie Sector (s) commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown below.

When an ID field is located on the disk, the FD1791 compares the Track number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD1791 must find an ID field with a Track number, Sector number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

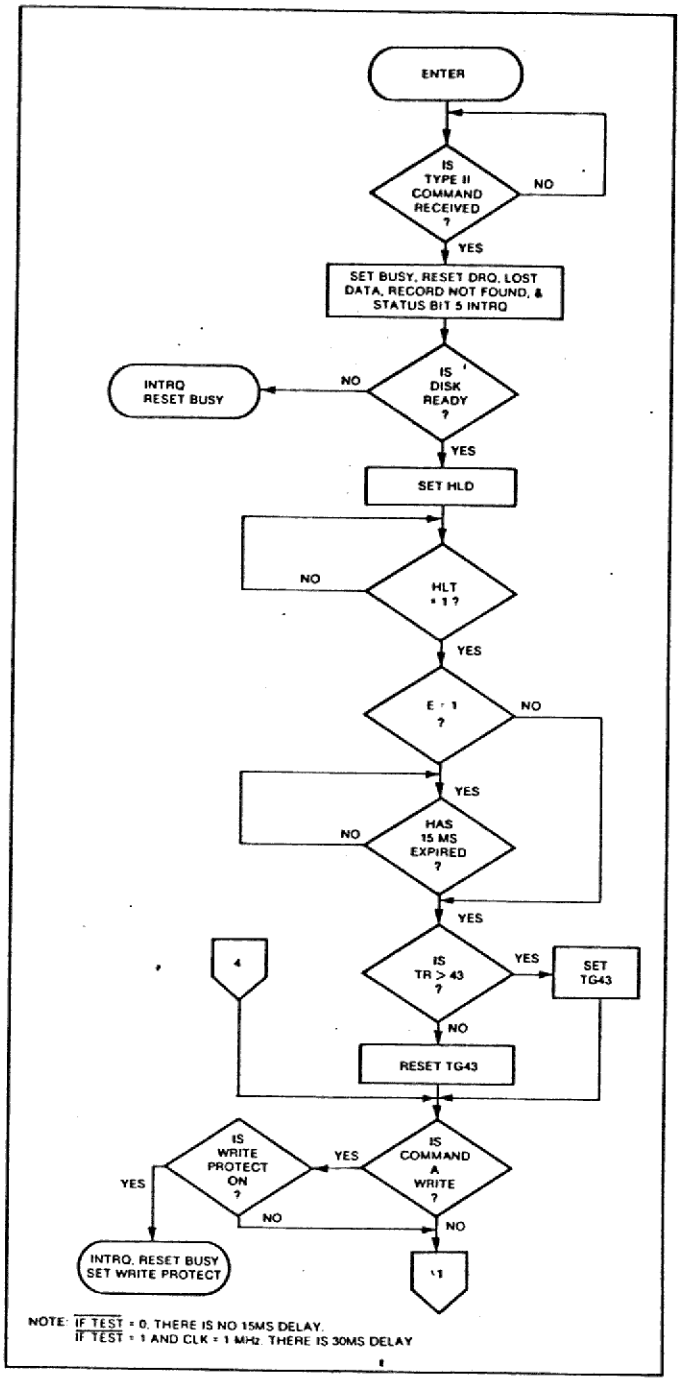
Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1791 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

READ COMMAND

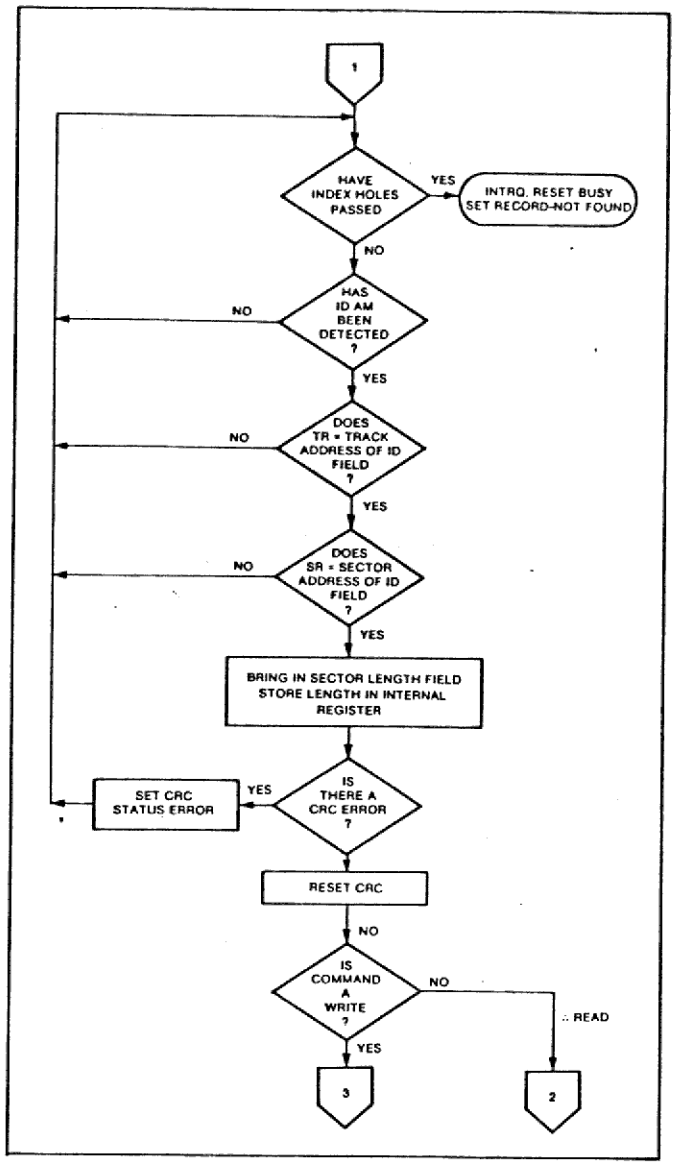
Upon receipt of the Read command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.



TYPE II COMMAND



TYPE II COMMAND

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

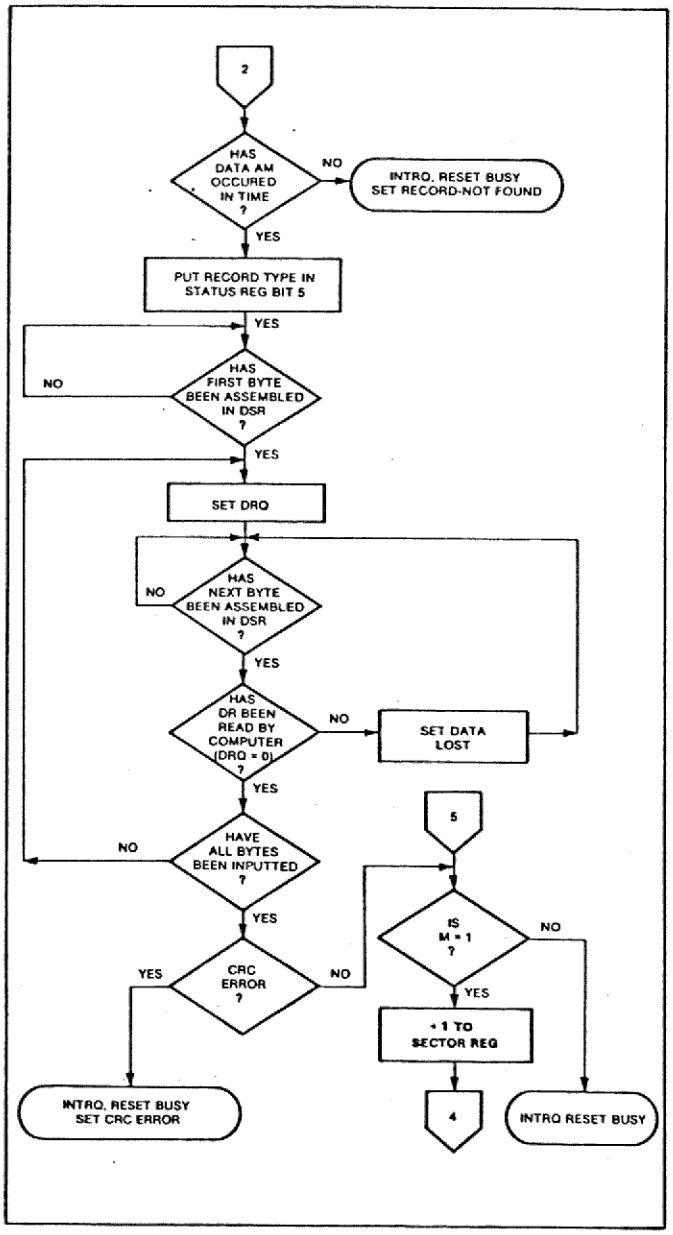
At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE COMMAND

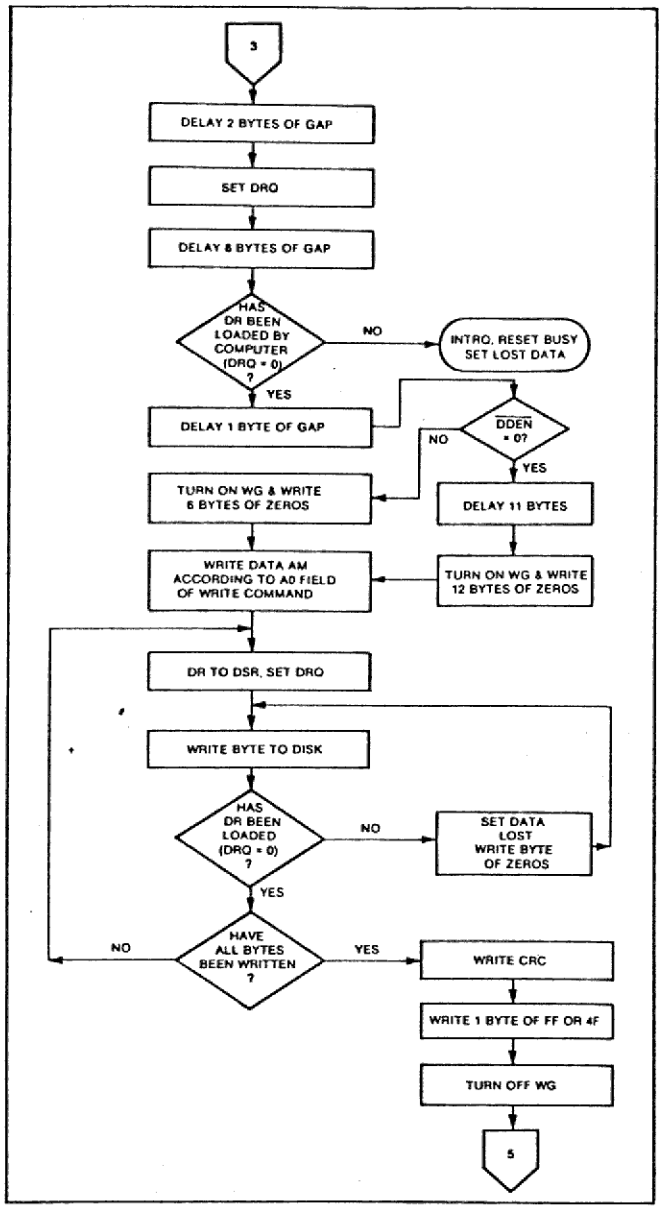
Upon receipt of the Write command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1791 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark



TYPE II COMMAND

The FD1791 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or 4F in MFM. The WG output is then deactivated.



TYPE II COMMAND

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 2	CRC 2
1	2	3	4	5	6

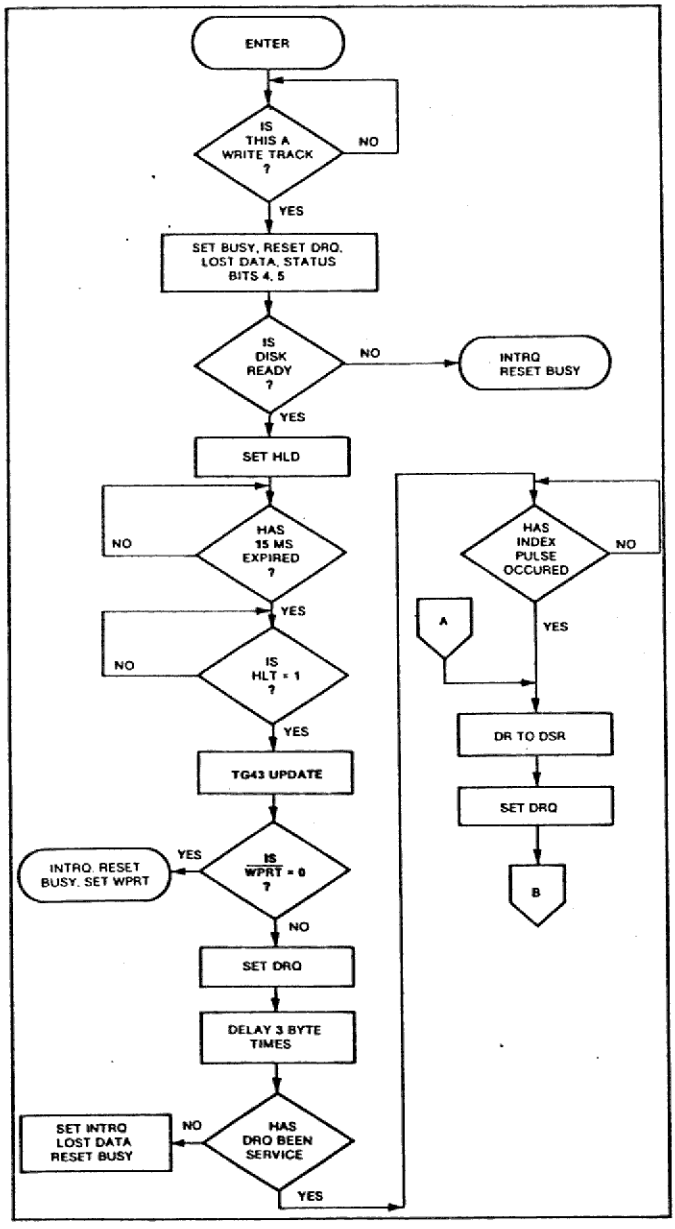
Although the CRC characters are transferred to the computer, the FD1791 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

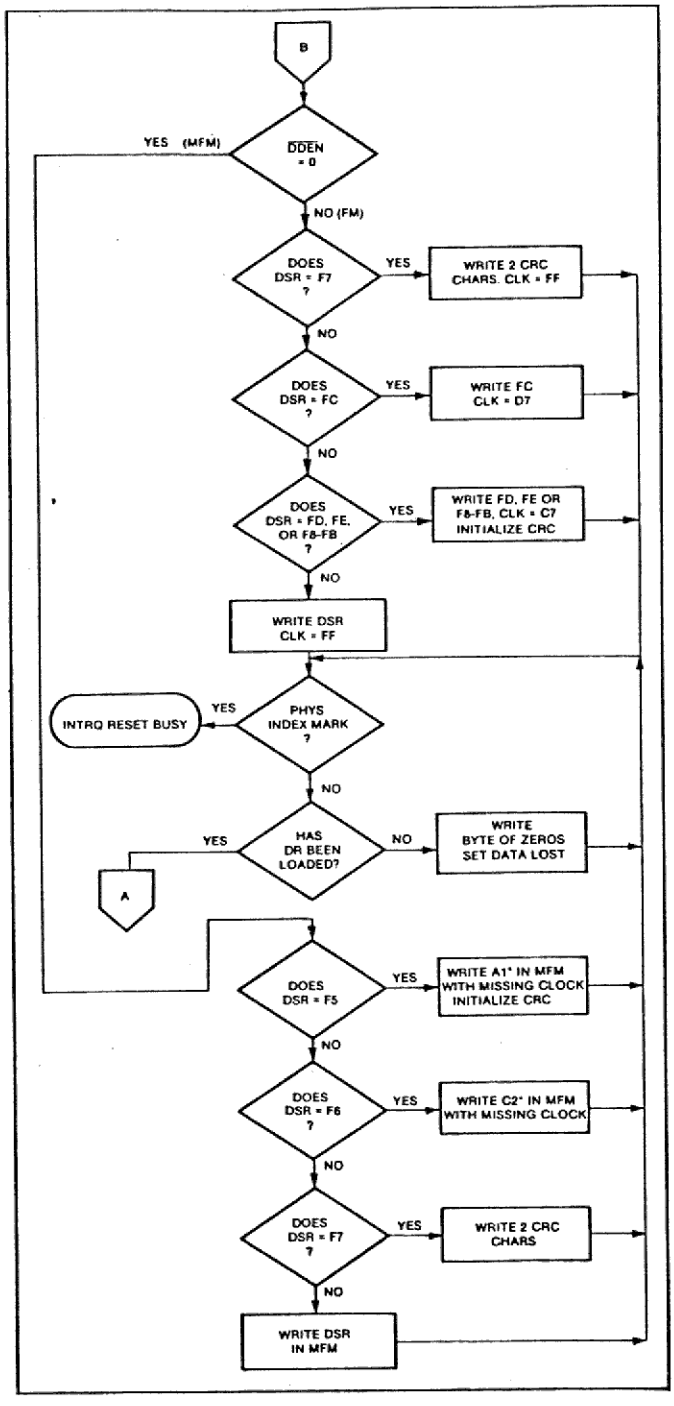
Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD1791 INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with Clk = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5
**Missing clock transition between bits 3 and 4

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0= Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will clear the immediate interrupt.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

Table 6. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD	0	RECORD NOT FOUND	0	WRITE FAULT	WRITE FAULT
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" or HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S2 TRACK 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1791 raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD1791 detects a data pattern on F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, in FM an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 FORMAT—128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	FF
	6	00
	1	FC (Index Mark)
	26	FF
*	6	00
	1	FE (ID Adress Mark)
	1	Track Number
	1	00
	1	Sector Number (1 thru 1A)
	1	00
	1	F7 (2 CRC's written)
	11	FF
	6	00
	1	FB (Data Address Mark)
	128	Data (IBM uses E5)
	1	F7 (2 CRC's written)
	27	FF
	247**	FF

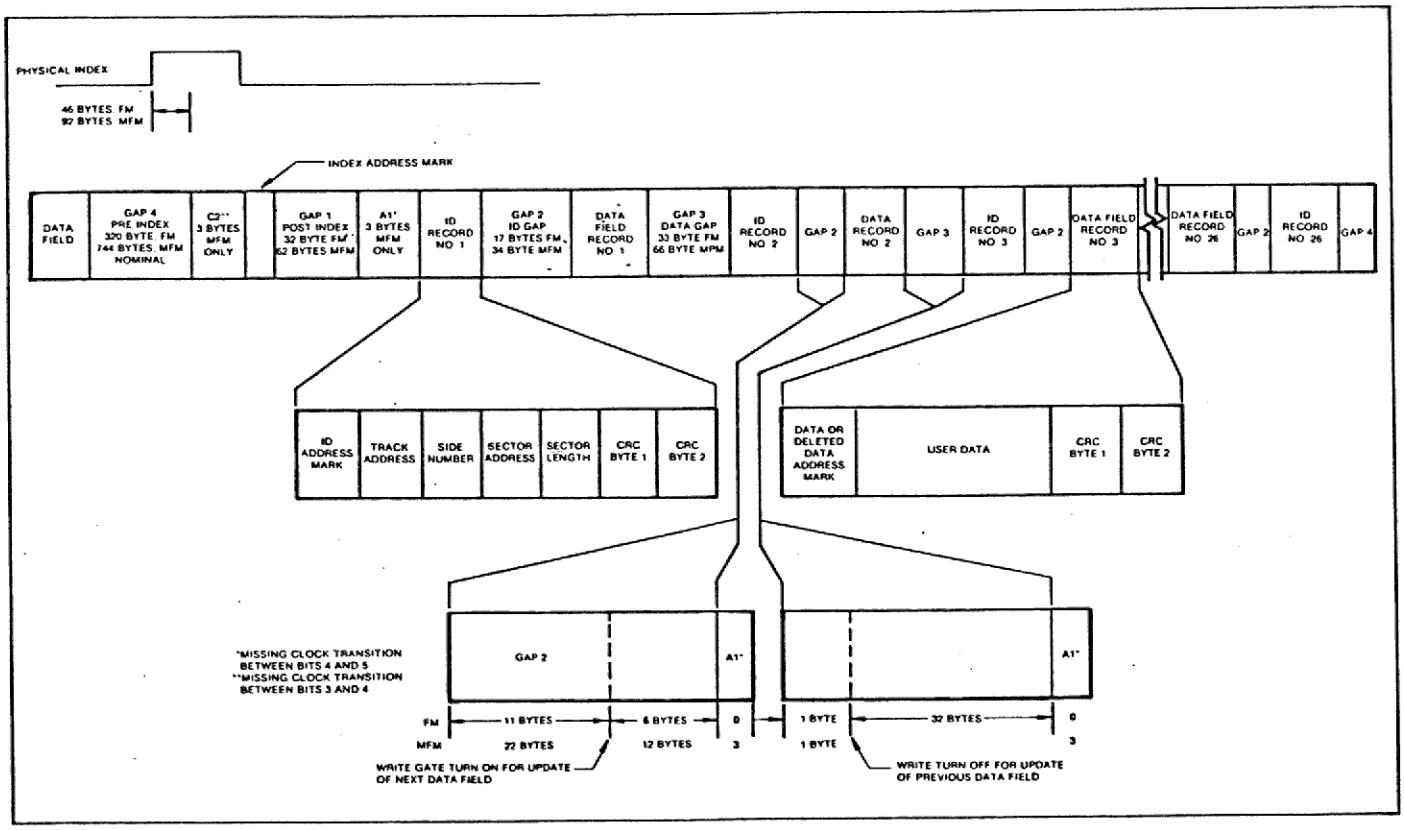
*Write bracketed field 26 times
**Continue writing until FD1791 interrupts out. Approx. 247 bytes.

IBM SYSTEM 34 FORMAT-256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette, the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	80	4E
	12	00
	3	F6
	1	FC
	50	4E
*	12	00
	3	F5
	1	FE
	1	Track Number (0 thru 4C)
	1	Side Number (0 or 1)
	1	Sector Number (0 thru 1A)
	1	01
	1	F7
	22	4E
	12	00
	3	F5
	1	FB
	256	40
	1	F7
	54	4E
	598**	

*Write bracketed field 26 times.
**Continue writing until FD1791 interrupts out. Approx. 598 bytes.



IBM TRACK FORMAT

NON-IBM FORMATS

Variations in the IBM format are possible to a limited extent if the following requirements are met: sector size must be a choice of 128, 256, 512 or 1024 bytes; gap size must be according to the following table. Note that the Index Mark is not required by the FD1791.

	FM	MFM
Gap I	16 bytes FF	16 bytes 4E
Gap II *	11 bytes FF 6 bytes 00	22 bytes 4E 12 bytes 00 3 bytes A1
Gap III **	10 bytes FF 4 bytes 00	16 bytes 4E 8 bytes 00 3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.

**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

REFERENCES:

1. IBM Diskette OEM Information GA21-9190-1
2. SA900 IBM Compatibility Reference Manual—Shugart Associates.
3. IBM Two-Sided Diskette OEM Information GA21-9257-1

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground)	+15 to -0.3V
Max. Voltage to Any Input With Respect to V_{SS}	+15 to -0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = +12.0V ±.6V, V_{SS} = 0V, V_{CC} = +5V ±.25V

V_{DD} = 10 ma Nominal, V_{CC} = 35 ma Nominal

SYMBOL	CHARACTERISTIC	MIN.	TYPE.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (all			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = 100 μA
V_{OL}	Output Low Voltage			0.4	V	I_O = 1.6 mA

NOTE: Pin 1 is normally connected to substrate with internal back bias generator. Be sure not to connect anything to Pin 1.

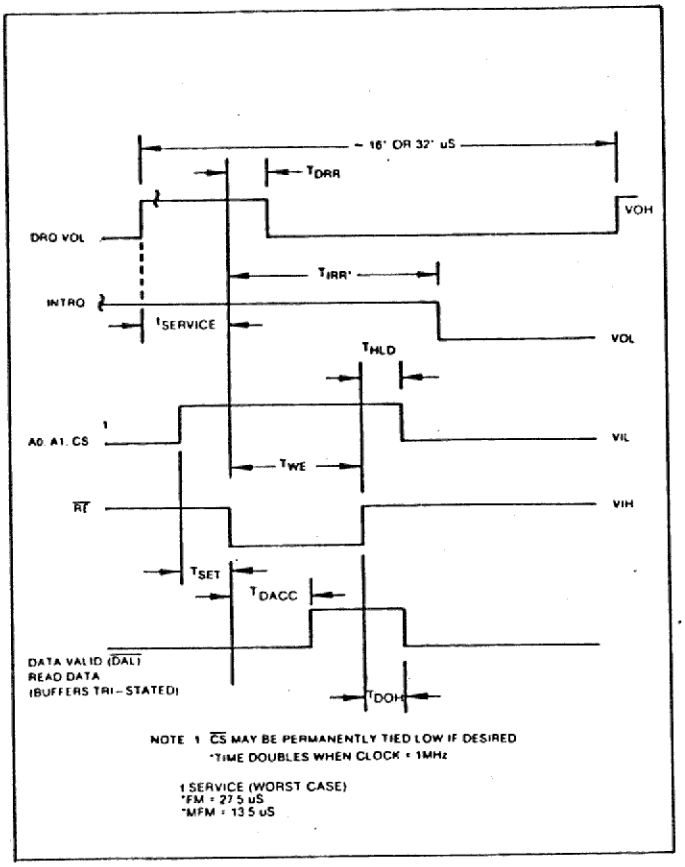
TIMING CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

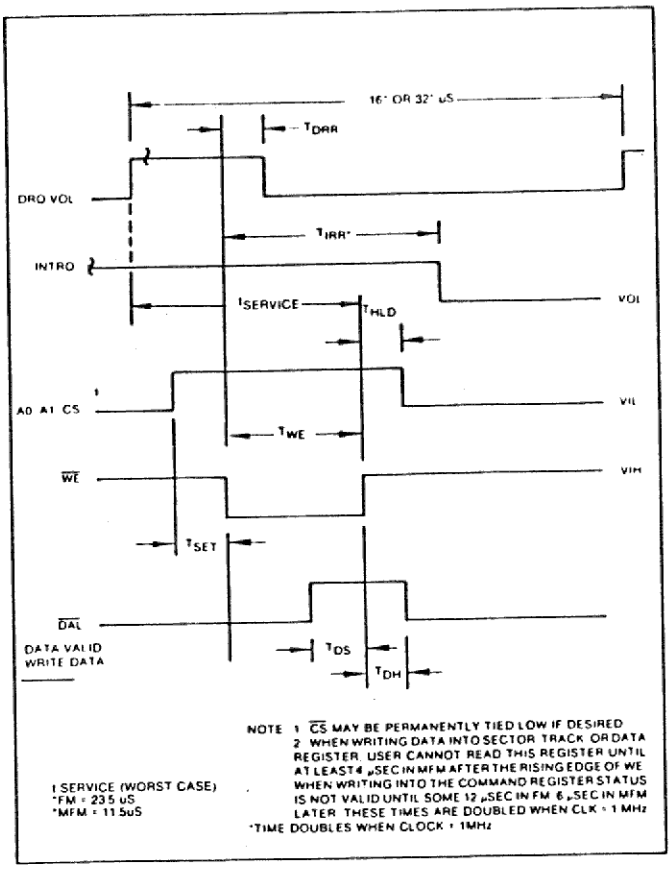
NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz.

READ OPERATIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 25 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 25 pf



READ ENABLE TIMING



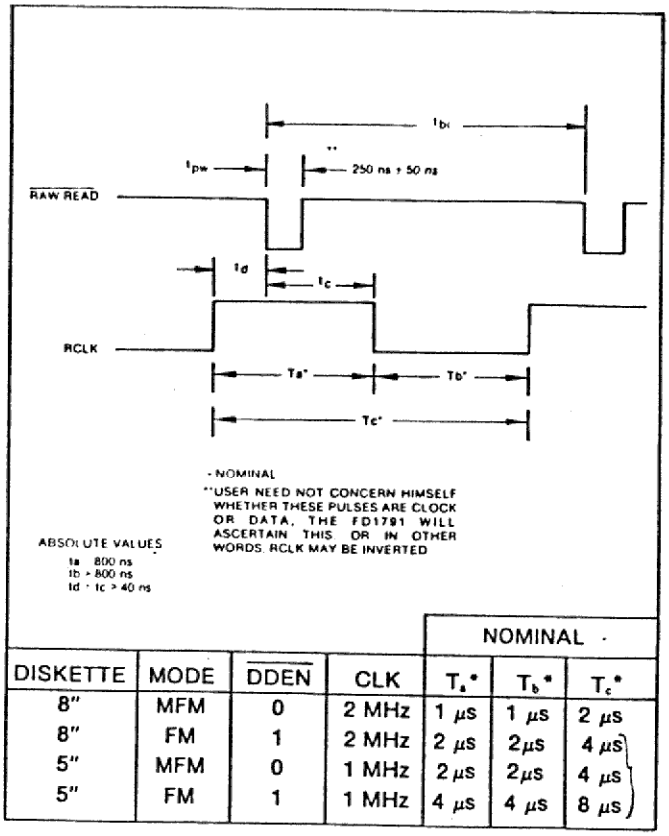
WRITE ENABLE TIMING

WRITE OPERATIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	20			nsec	

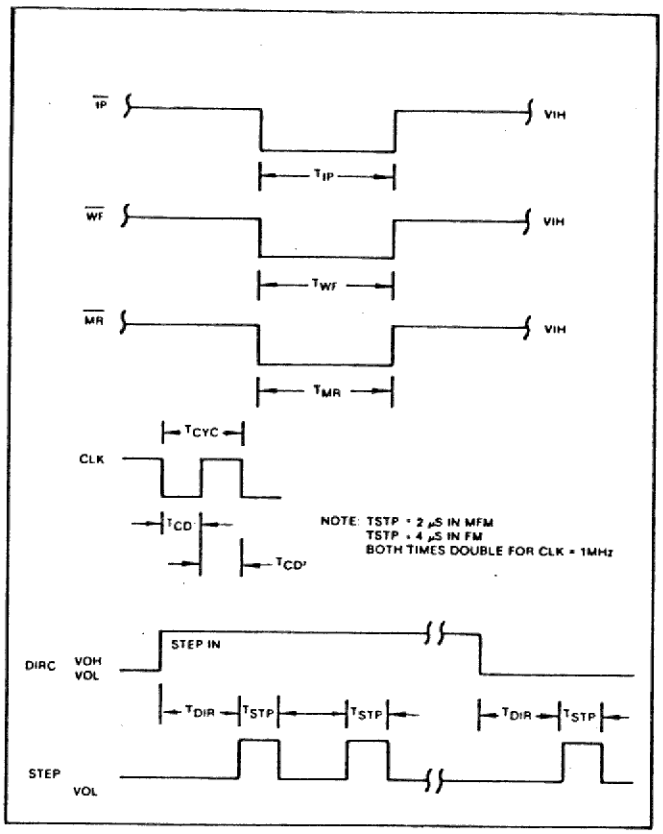
MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230			nsec	
TCD_2	Clock Duty (high)	200			nsec	
TSTP	Step Pulse Output	2 or 4			µsec	
TDIR	Dir Setup to Step	12			µsec	See Note
TMR	Master Reset Pulse Width	50			µsec	
TIP	Index Pulse Width	10			µsec	
TWF	Write Fault Pulse Width	10			µsec	



				NOMINAL		
DISKETTE	MODE	$\overline{\text{DDEN}}$	CLK	T_a*	T_b*	T_c*
8"	MFM	0	2 MHz	1 μs	1 μs	2 μs
8"	FM	1	2 MHz	2 μs	2μs	4 μs
5"	MFM	0	1 MHz	2 μs	2μs	4 μs
5"	FM	1	1 MHz	4 μs	4 μs	8 μs

INPUT DATA TIMING



MISCELLANEOUS TIMING

NOTES:

1. Pulse width on $\overline{\text{RAW READ}}$ (p.27) is normally 250 ± 50 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. When flux reversals are totally nonexistent, the external separator should insure $\overline{\text{RAW READ}}$ = 1. Also, RCLK should be free running at all times.
3. t_{bc} (see input data timing) should be 2, 3, or 4 μs nominal in MFM and 2 or 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. In MFM, the EARLY and LATE signals are valid at least 125 ns from either edge of WD.

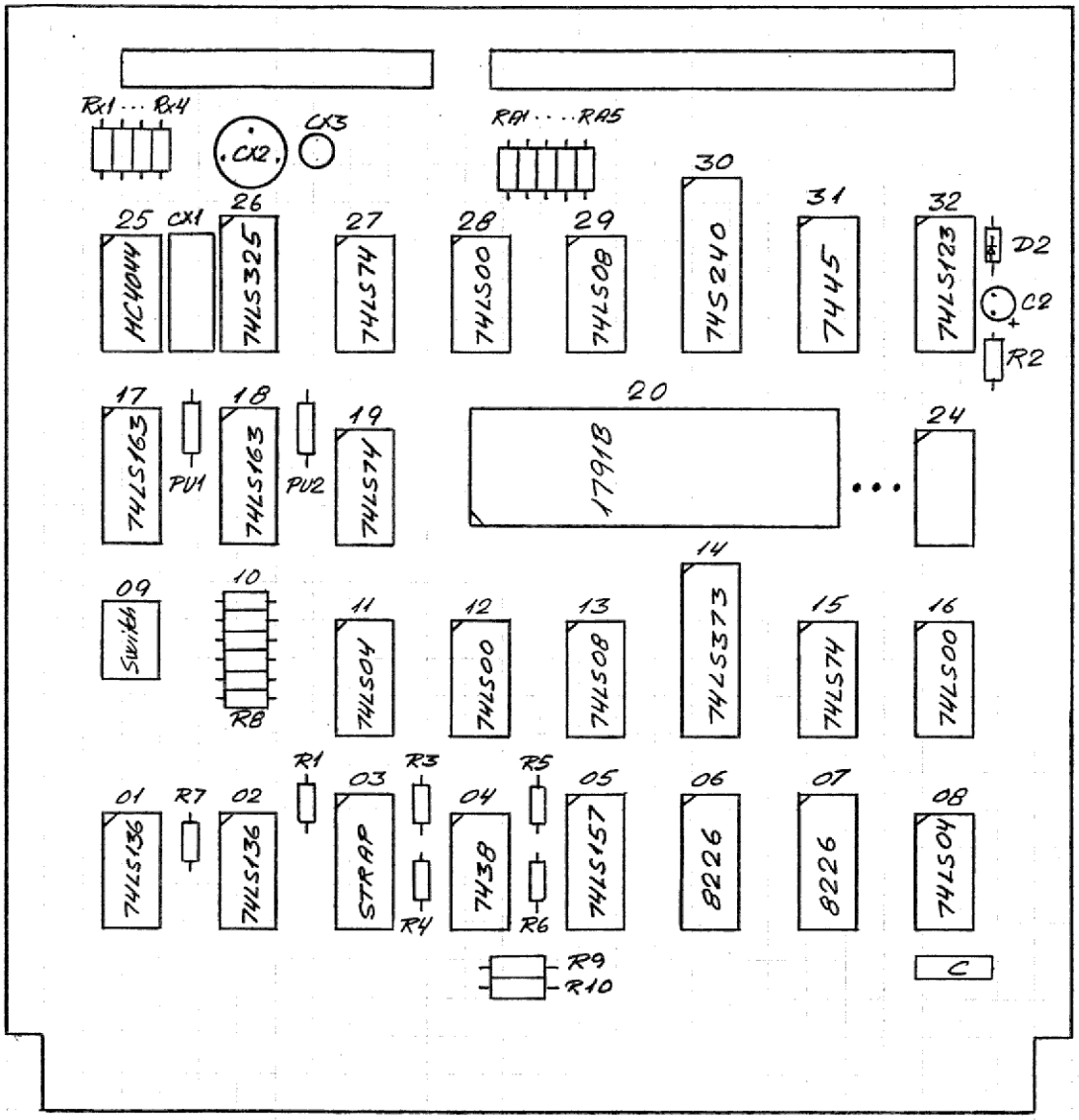
PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
19	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	A logic low on this input resets the device and loads hex 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When MR is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive. Also, hex 01 is loaded into sector register.
COMPUTER INTERFACE:			
7-14	$\overline{\text{DATA ACCESS LINES}}$	$\overline{\text{DAL0}}$-$\overline{\text{DAL7}}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by WE or a transmitter enabled by RE.
3	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	A logic low on this input selects the chip and enables computer communication with the device.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/ transfer data on the DAL lines under RE and WE control: A1 A0 RE WE 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register or the status register is read. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for regular drives, 1 MHz for mini-drives.
FLOPPY DISK INTERFACE:			
25	READ GATE	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flex transition. WD contains the unique Address marks as well as data in both FM and MFM formats.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	RAW READ	$\overline{RAW\ READ}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media. When a logic high is found on the HLT input the head is assumed to be engaged.
23	HEAD LOAD TIMING	HLT	
15	STEP	STEP	Step and direction motor control. The step output contains a pulse for each step and the direction output is active high when stepping in, active low when stepping out.
16	DIRECTION	DIRC	

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
17	EARLY	EARLY	Indicates that the write data pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read-Write head is positioned between the 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid when writing is to be performed on the diskette.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	This input detects writing faults indications from the drive. When WG = 1 and $\overline{\text{WF}}$ goes low the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD1791 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	Input, when low for a minimum of 10 μsec, informs the FD1791 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminated the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice actuated motors.

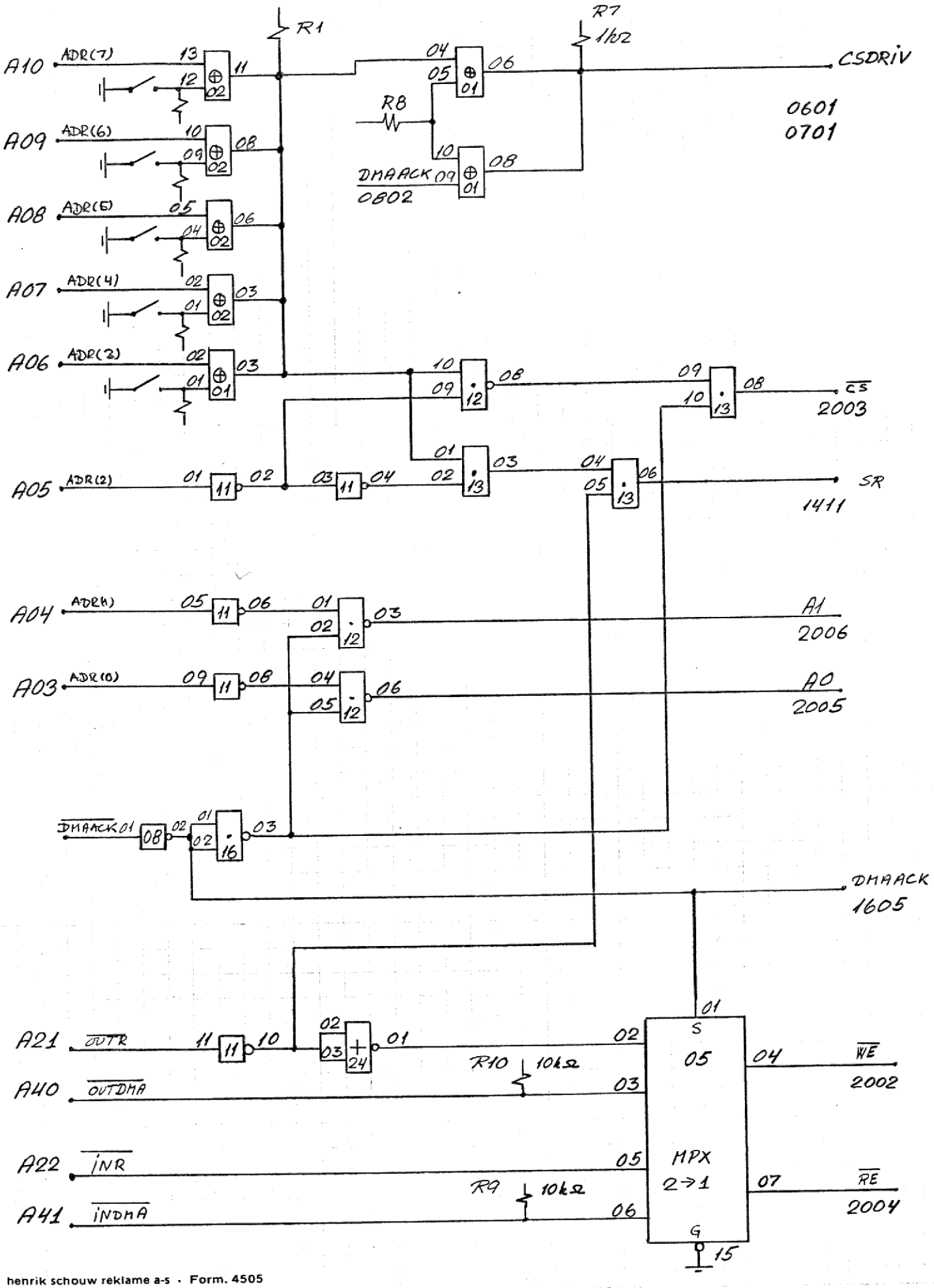
7045 Floppy Disk Controller



dansk data elektronik aps

Floppy Disk Controller

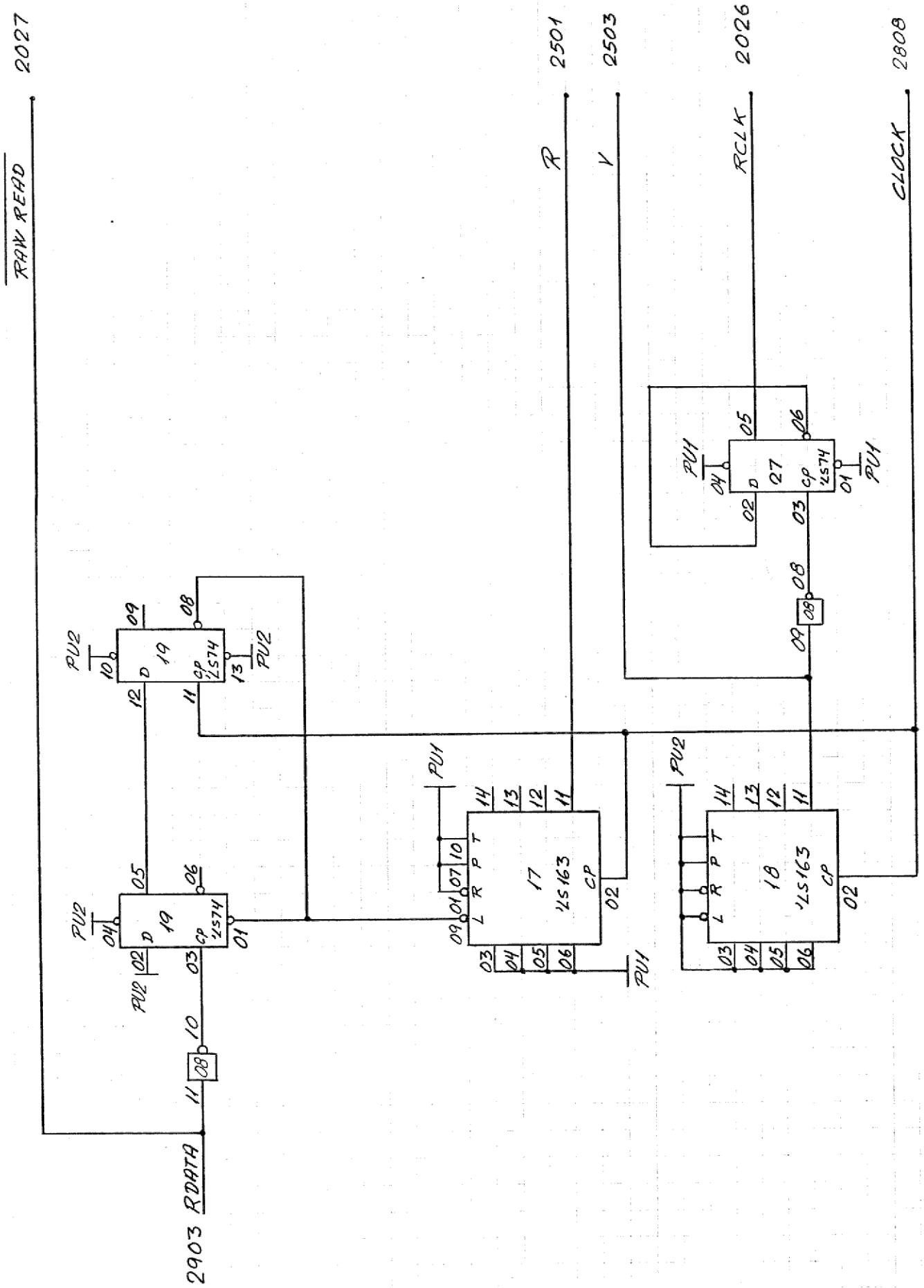
Initialer/dato	Side
KAN 790518	1
Revideret	Projekt 7045

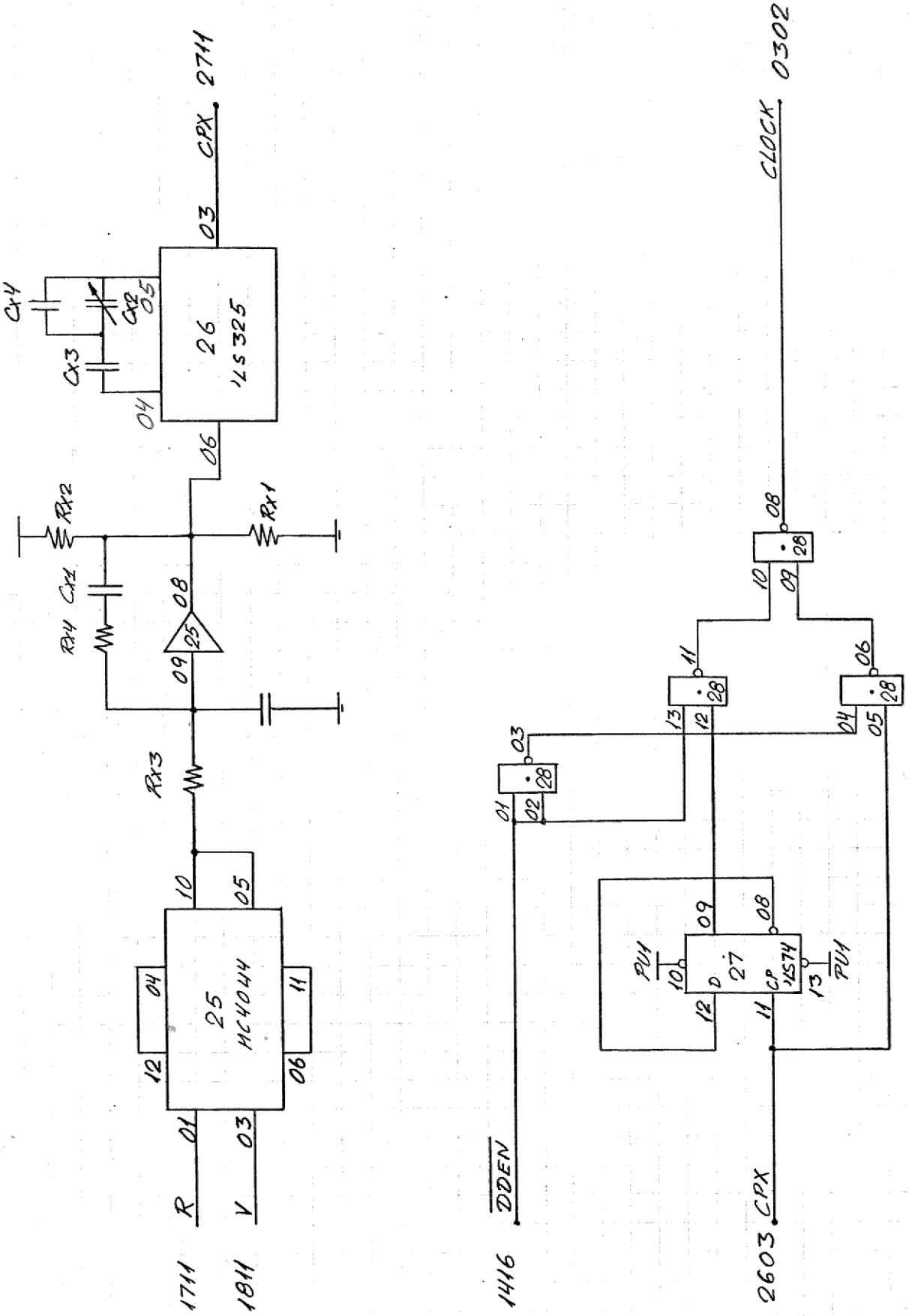


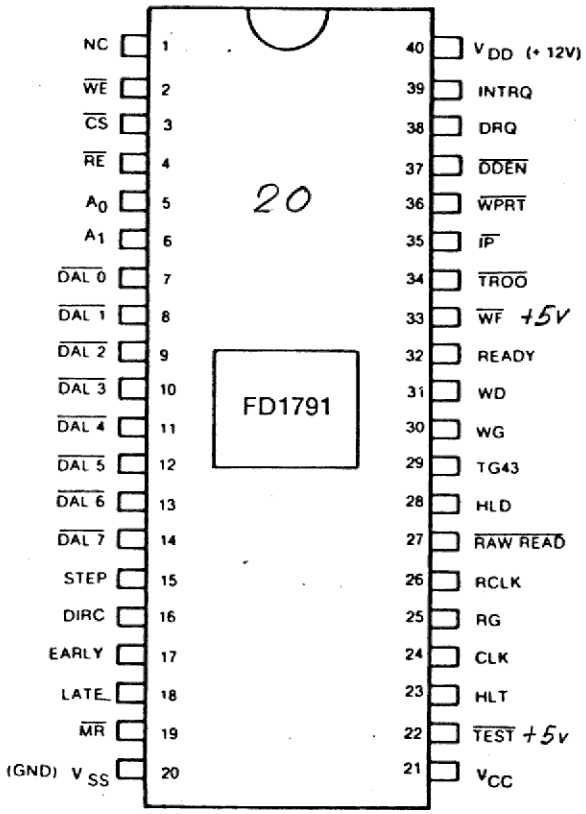
dansk data elektronik aps

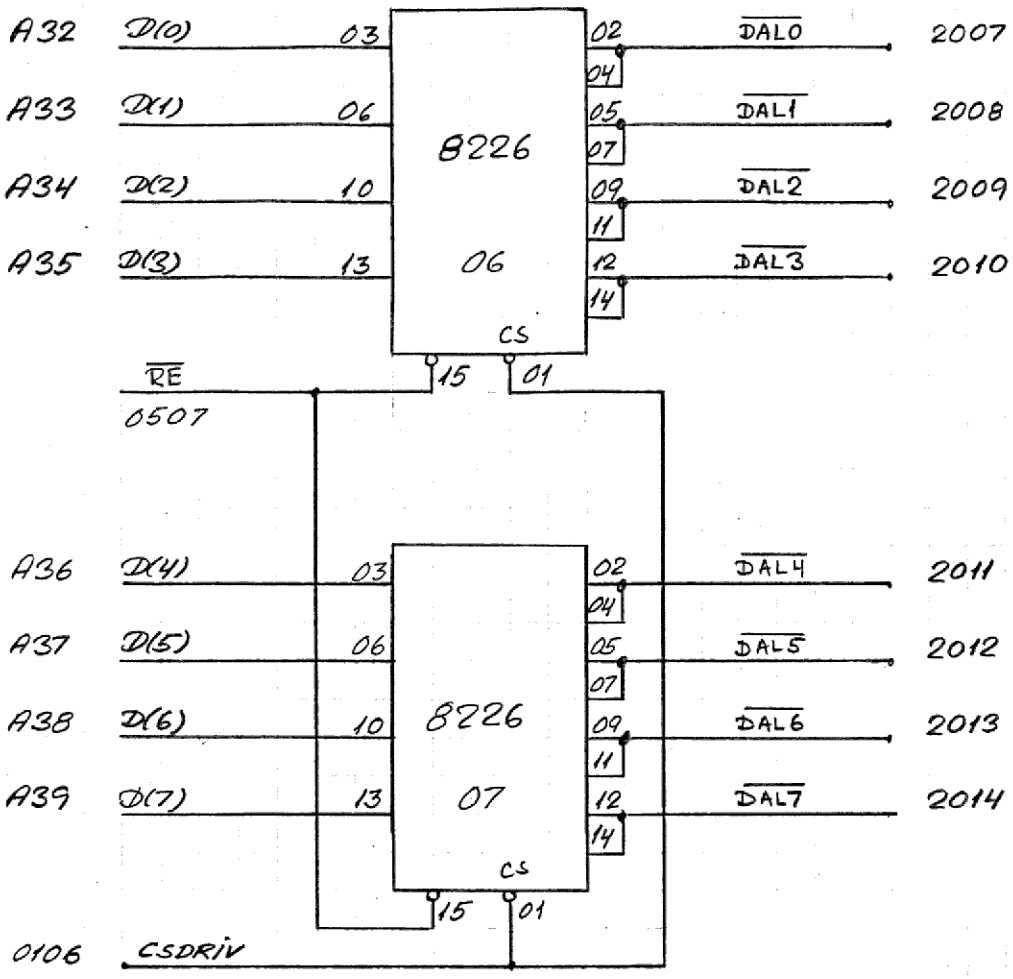
Floppy Disk Controller

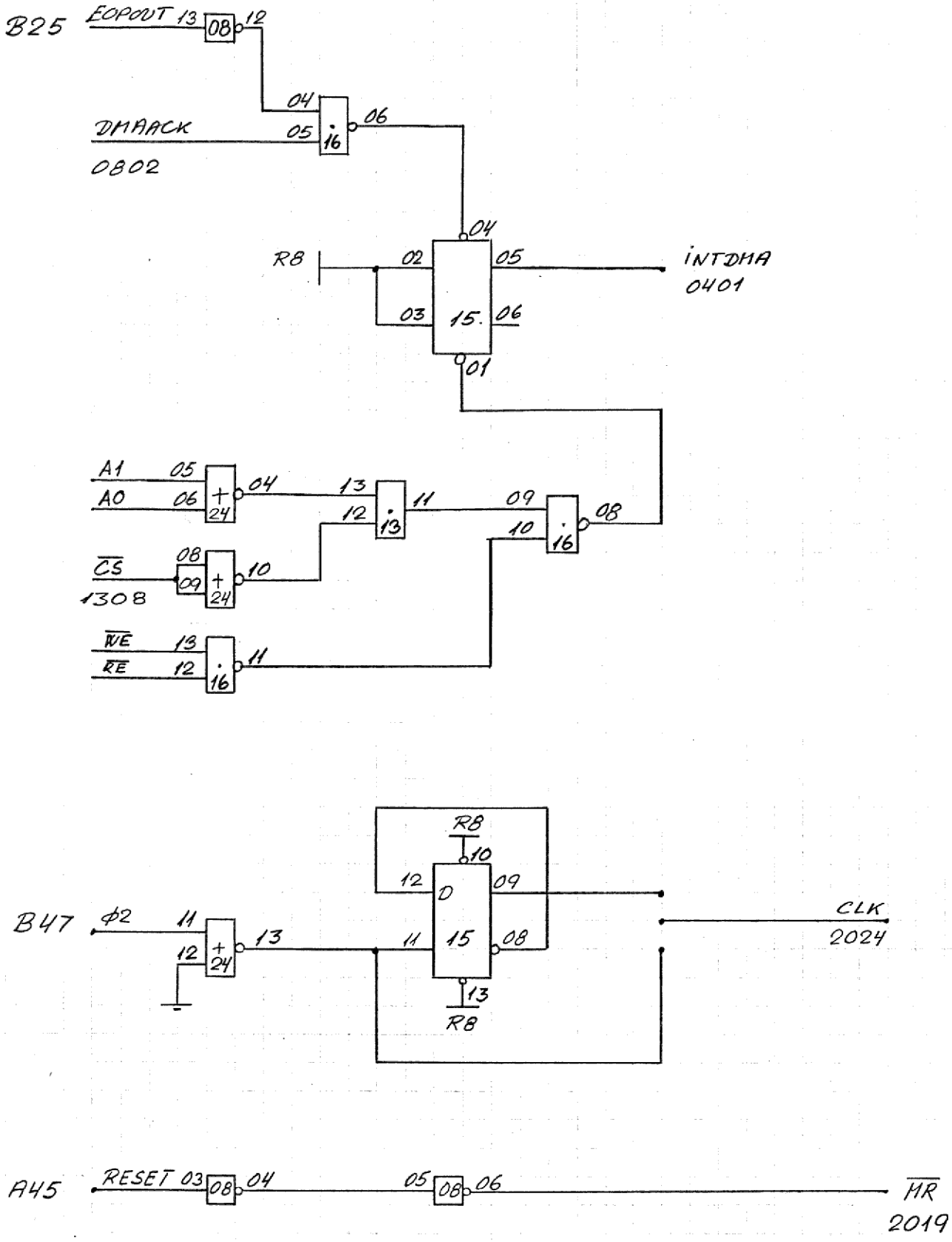
Initialer/dato	Side
KAN 790518	2
Revideret	Projekt 7045

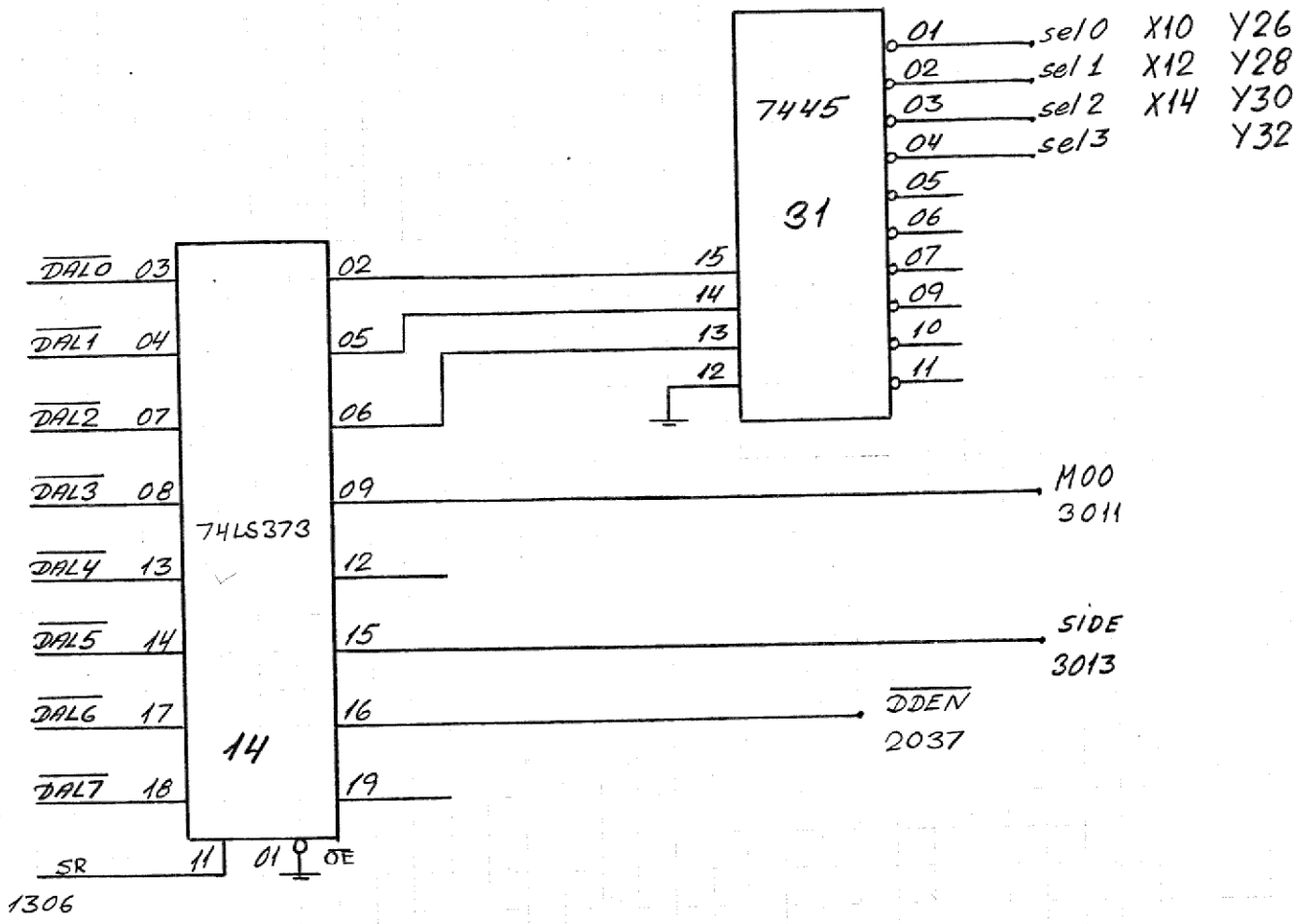


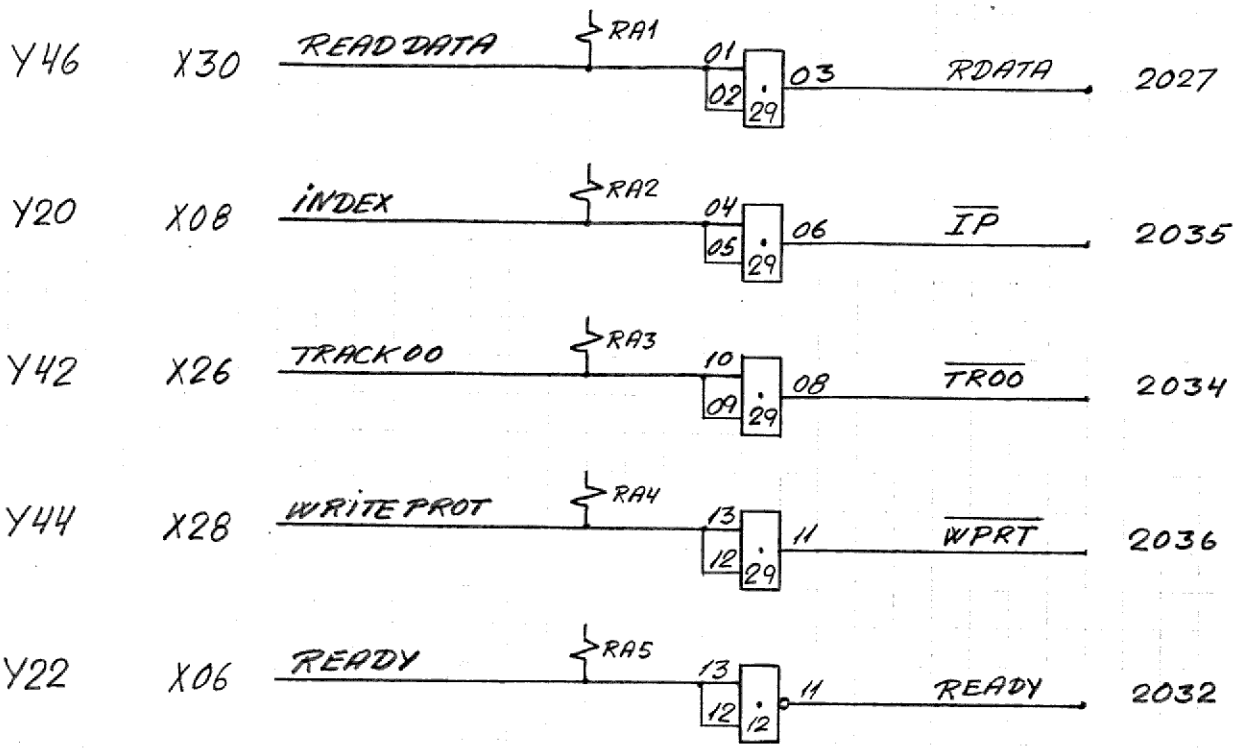

2711
CPX
03
26
LS 325
04
05
06
Cx4
Cx3
Cx8
Rx2
Rx1
Rx4
Cx1
08
25
09
Rx3
10
05
25
MC4044
04
11
12
06
01
03
R
V
1711
1811
0302
CLOCK
08
28
10
09
11
06
13
12
04
05
03
01
02
DDEN
1416
PU1
09
08
10
D
27
CP
LS74
13
12
11
2603
CPX

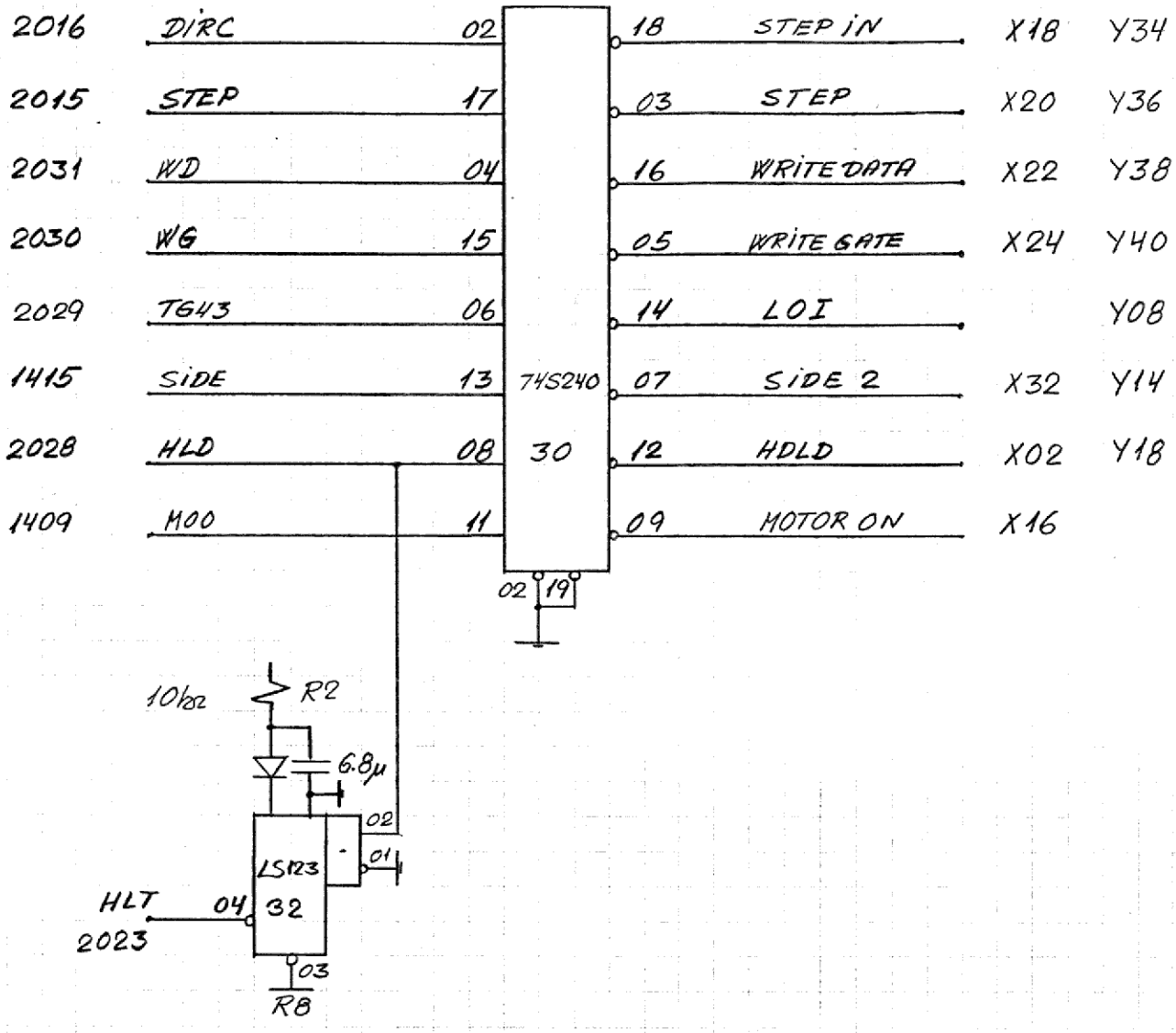

NC 1
WE 2
CS 3
RE 4
A0 5
A1 6
DAL 0 7
DAL 1 8
DAL 2 9
DAL 3 10
DAL 4 11
DAL 5 12
DAL 6 13
DAL 7 14
STEP 15
DIRC 16
EARLY 17
LATE 18
MR 19
(GND) VSS 20
20
FD1791
40 VDD (+ 12V)
39 INTRQ
38 DRQ
37 DDEN
36 WPRT
35 IP
34 TROO
33 WF +5V
32 READY
31 WD
30 WG
29 TG43
28 HLD
27 RAW READ
26 RCLK
25 RG
24 CLK
23 HLT
22 TEST +5v
21 VCC

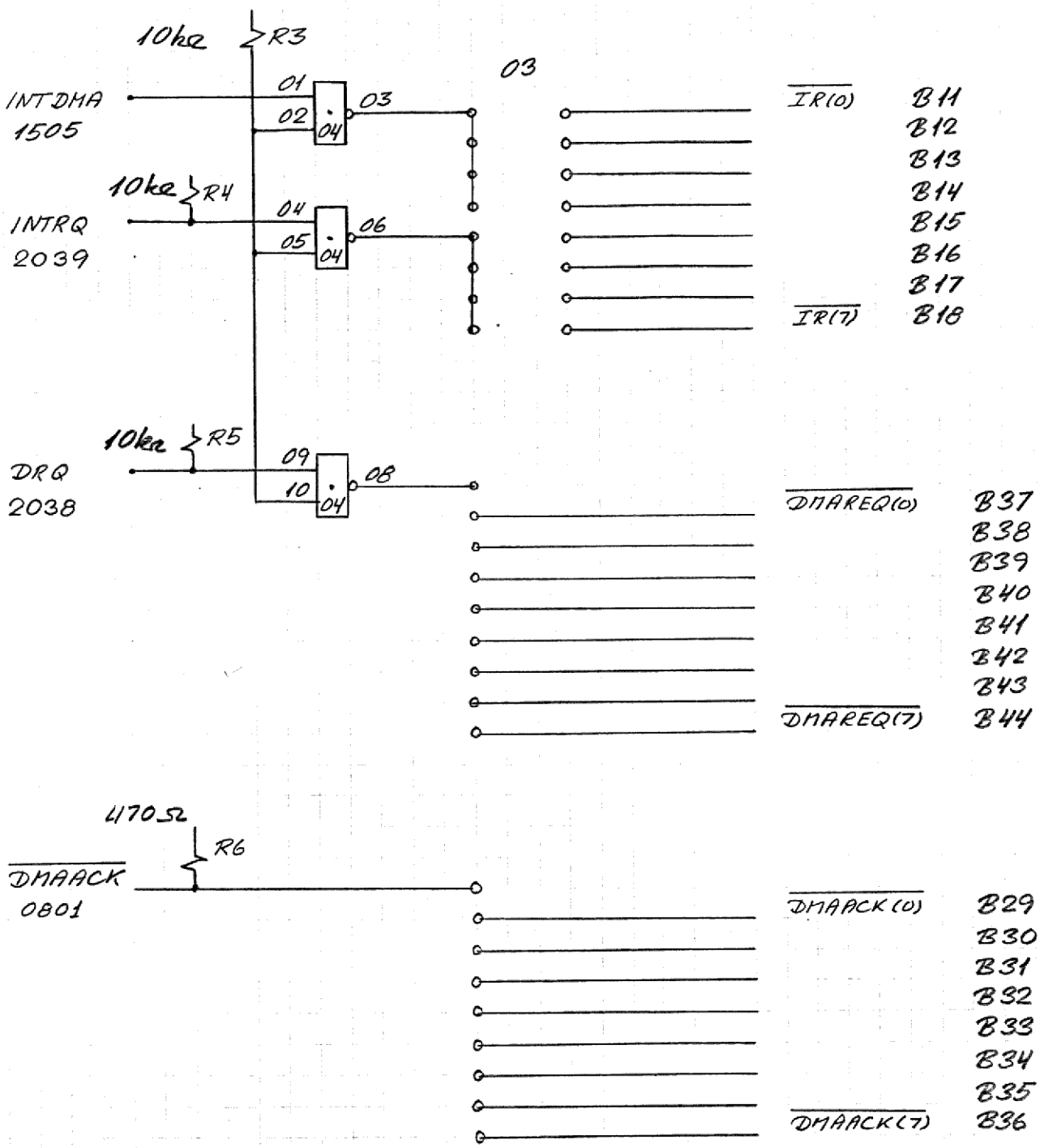

A32
D(0)
03
02
DAL0
2007
04
A33
D(1)
06
8226
05
DAL1
2008
07
A34
D(2)
10
09
DAL2
2009
11
A35
D(3)
13
06
12
DAL3
2010
14
CS
RE
15
01
0507
A36
D(4)
03
02
DAL4
2011
04
A37
D(5)
06
05
DAL5
2012
07
A38
D(6)
10
8226
09
DAL6
2013
11
A39
D(7)
13
07
12
DAL7
2014
14
CS
15
01
0106
CSDRIV


B25
EOPOUT 13
08
12
04
DMAACK
05
16
06
0802
04
R8
02
05
INTDMA
0401
03
15.
06
01
A1
05
A0
06
24
04
13
12
13
11
09
10
16
08
CS
08
09
24
10
1308
WE
13
RE
12
16
11
R8
10
12
D
09
CLK
2024
B47
Φ2
11
12
24
13
11
15
08
13
R8
A45
RESET 03
08
04
05
08
06
MR
2019


7445
31
01 sel0 X10 Y26
02 sel1 X12 Y28
03 sel2 X14 Y30
04 sel3 Y32
05
06
07
09
10
11
15
14
13
12
74LS373
14
DAL0 03
DAL1 04
DAL2 07
DAL3 08
DAL4 13
DAL5 14
DAL6 17
DAL7 18
02
05
06
09
12
15
16
19
M00
3011
SIDE
3013
DDEN
2037
SR
1306
11
01
OE


Y46
X30
READ DATA
RA1
01
02
29
03
RDATA
2027
Y20
X08
INDEX
RA2
04
05
29
06
IP
2035
Y42
X26
TRACK 00
RA3
10
09
29
08
TR00
2034
Y44
X28
WRITE PROT
RA4
13
12
29
11
WPRT
2036
Y22
X06
READY
RA5
13
12
12
11
READY
2032


2016 DIRC 02
2015 STEP 17
2031 WD 04
2030 WG 15
2029 TG43 06
1415 SIDE 13
2028 HLD 08
1409 M00 11
74S240
30
02 19
18 STEP IN X18 Y34
03 STEP X20 Y36
16 WRITE DATA X22 Y38
05 WRITE GATE X24 Y40
14 LOI Y08
07 SIDE 2 X32 Y14
12 HDLD X02 Y18
09 MOTOR ON X16
10/82 R2
6.8µ
LS123
02
01
HLT
2023
04
32
03
R8


10kΩ
R3
INTDMA
1505
01
02
03
04
03
10kΩ
R4
INTRQ
2039
04
05
06
04
10kΩ
R5
DRQ
2038
09
10
08
04
470Ω
R6
DMAACK
0801
IR(0)
IR(7)
B11
B12
B13
B14
B15
B16
B17
B18
DMAREQ(0)
DMAREQ(7)
B37
B38
B39
B40
B41
B42
B43
B44
DMAACK(0)
DMAACK(7)
B29
B30
B31
B32
B33
B34
B35
B36