DANSK DATA ELEKTRONIK

ID-8530 CPU MODULE

and

ID-8538 REFRESH MODULE

for the

SPC-1 MICROCOMPUTER SYSTEM

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1.1 DESCRIPTION OF ID-8530.

The ID-8530 CPU module is the CPU module in the SPC-1 microcomputer. The CPU module drives the address bus and generates all the necessary control signals except control signals for the dynamic RAM memory which are generated by ID-8538. The ID-8530 module works with the other modules in the ID-7000 series. In the SPC-1 it normally works with:

ID-7037:	32 K Dynamic RAM with bank switching.
ID-8538:	Refresh for the ID-7037 dynamic RAM.
ID-7045:	Floppy disk controller.
ID-7009:	DMA controller/Interrupt controller.
ID-7012:	4 port communication module.
ID-7018:	General purpose I/O module.

Appendix 1.1 is a listing of the signals in the SPC-1 bus for communication between modules.

The ID-8530 CPU module contains a 8085A-2 microprocessor and the following peripherial units:

A. BOOT LOADER PROM.
B. TIMER.

The ID-8530 CPU module is available in a 2.5 Mhz and a 5 Mhz version. It should be noted, that the memory timing requirements are different for the two versions.

1.2 THE 8085A-2 MICROPROCESSOR.

The 8085A-2 is the key component on the CPU module. It drives the address bus and generates all the necessary control signals.

The SOD output signal from the 8085A-2 is used in a special way which is described later.

The odd interrupt levels 5.5 and 6.5 are used by the communication ports on the ID-8538 module while level 7.5 is used by the timer on the CPU module. The odd interrupt level TRAP is used as a DEBUG CALL.

Appendix 1.2 is a data sheet including the instruction set for the 8085A-2.

1.3 BOOT LOADER PROM.

The CPU module contains an UV erasable PROM type 2708. The boot loader PROM is enabled when ADR(15:10)=0 and SOD=0. When the boot loader PROM is enabled the external memory modules are disabled.

During power up the reset signal is generated. This signal resets the CPU and all the modules connected to the SPC-1 bus. After power up SOD equals zero, and the CPU starts reading its first instruction in address zero. As SOD equals zero the instruction is read from the boot loader PROM.

The APU on the ID-8538 module is reset by the SOD signal inverted, so the program in the boot loader PROM cannot use the APU.

It is the responsibility of the boot loader program to reset the APU properly as described in the data sheet and to disable the PROM when the boot loader program has finished.

If the ID-8530 CPU MODULE is used in other configurations than the SPC-1, the function of the BOOT LOADER PROM may be disabled by connecting a strap between pin 6 and pin 7 on IC2. In this case the CPU operates on external memory modules independent of the state of the SOD signal.

1.4 TIMER.

The output frquency of the 8085A-2 is 5 Mhz or 2.5 Mhz depending on the version of the module. This signal is divided down by 8 decimal counters. Several outputs from these counters are connected to a socket position 35 on the module. See figure 1.1. The odd interrupt input RST 7.5 and the input SID is connected to the same socket. The time interval between interrupts is set in the following way:

The RST 7.5 input is connected to one of the timer outputs. Pin 16 of the socket is connected to one of the outputs x1, x2, or x5. The time interval between interrupts is the time shown in the figure multiplied by a factor which is 1, 2, or 5, when pin 16 is connected to x1, x2 or x5, respectively.

The SID input can be connected to one of the outputs from the counters. In this way the signal on the SID pin will be a symmetrical square wave with a time period which is equal to the time shown in the figure multiplied by the same factor as used when calculating the time between interrupts. By testing SID which is normally connected to a slow varying counter output it is possible to program a real time clock even if the interrupt system is disabled for a period of time so the program is unable to respond to all timer interrupts.

1.5 DEBUG CALL.

The odd interrupt level TRAP can be connected to a switch through a debouncing flip flop. When the switch is activated a TRAP interrupt is generated. The CPU stacks its instruction counter and fetches its next instruction from location 24 hex. This location should contain a jump instruction to the debug program. Notice that the TRAP interrupt cannot be disabled so the only reason why a debug call cannot be performed is that the jump instruction in location 24 has been destroyed.

2.1 DESCRIPTION OF ID-8538.

ID-8538 is used in the SPC-1 microcomputer together with ID-8530 CPU MODULE. It refreshes ID-7037 dynamic RAM modules and generates all the necessary control signals for memory read and write cycles.

Besides refresh circuitry the module contains the following peripherial units:

Communication Port 0.
Communication Port 1.
Arithmetic Processing Unit.
Baud Rate Generator.

2.2 REFRESH.

The refresh part of the ID-8538 module is invisible to the programmer. This means that the programmer do not have to concern himself about refresh af dynamic memory. Though it should be noted that refresh is performed every 14 microsecond. A refresh cycle takes 450 nanosecond.

2.3 COMMUNICATION INTERFACES.

The refresh module contains two programmable interfaces type 8251A. In the following text these will be referred to as port 0 and port 1.

In the SPC-1 microcomputer port 0 is normally used for the CRT terminal and port 1 is used for the printer.

The interface consist of:

RxD: Receiver data.
TxD: Transmitter data.
CTS: Clear to Send.
GND: Ground.

The baud rate can be strapped individually for port 0 and port 1. The interfaces to port 0 and port 1 are found in two 16 pin DIP sockets at the top of the module; see figure 2.2

Addresses and interrupt levels for port 0 and port 1:

	BASE ADDRESS	INTERRUPT LEVEL
PORT 0	E2	6.5
PORT 1	E4	5.5

The interrupt request is generated if TxRDY or RxRDY is true and the port has CLEAR to SEND.

Appendix 2.1 is a data sheet for the 8251A.

2.4 ARITHMETIC PROCESSING UNIT.

The refresh module contains an Arithmetic Processing Unit, APU The APU is connected to the SPC-1 bus system through transceivers. The CPU module uses the APU in order to facillitate calculations with floating point numbers and to facillitate calculations af mathematical functions.

The base address of the APU is E8. The APU is not connected to the interrupt system.

The reset pin of the APU is not connected to the reset singal in the system bus. Instead it is conneted to SOD inverted. SOD is an output pin from the 8085A-2. The APU is reset when SOD=0. For normal operation SOD should be 1.

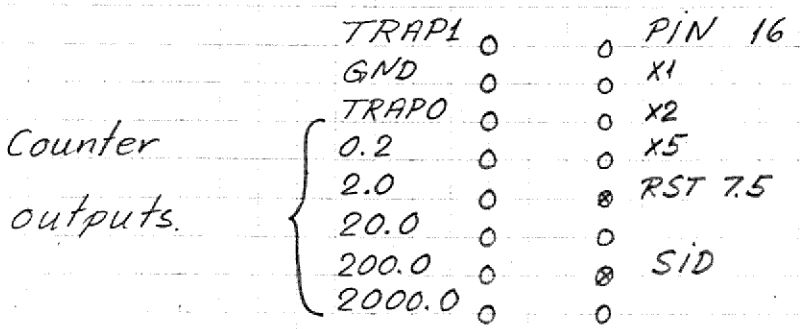
Appendix 2.2 is a data sheet for the AD9511A APU used on the board.

2.5 BAUD RATE GENERATOR.

The refresh module contains a 16 MHz crystal controlled oscillator. The oscillator drives the 16 MHz clock lines in the SPC-1 bus. The signal from the oscillator is divided down to 2 MHz which drives the clock lines in the SPC-1 bus. The signal is divided further down to give the various baud rates for Port 0 and Port 1. The baud rates are selected by means of a strap at the top of the refresh module. The strapping possibilities are shown in figure 2.1. The baud rates are as shown in

the figure when the communication ports are programmed to divide by 16.

Timer Interrupts



Times measured in ms

Figure 1.1

The times shown are for the 5 Mhz version. For the 2.5 MHz version all times are multiplied by two.

Position 39

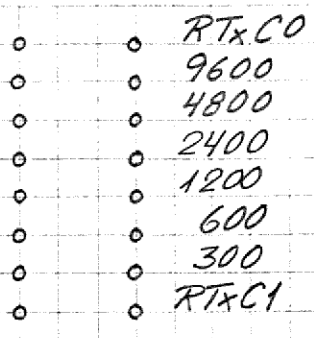


figure 2.1

Communication Port Interface

Port 0 : Position 37; Port 1 : Position 38.

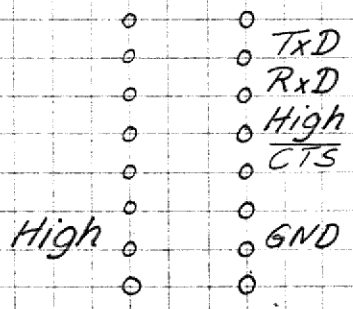


figure 2.2

Appendix 1.1: SPC-1 BUS SYSTEM.

SOLDER SIDE SIDE A	PIN NO.	COMPONENT SIDE SIDE B
+5V	1	GND
-5V	2	GND
ADR(0)	3	*MEMDISABLE*
ADR(1)	4	---
ADR(2)	5	---
ADR(3)	6	---
ADR(4)	7	ANALOG GROUND
ADR(5)	8	+15V ANALOG SUPPLY
ADR(6)	9	-15V ANALOG SUPPLY
ADR(7)	10	-12V
ADR(8)	11	*IR(0)*
ADR(9)	12	*IR(1)*
ADR(10)	13	*IR(2)*
ADR(11)	14	*IR(3)*
ADR(12)	15	*IR(4)*
ADR(13)	16	*IR(5)*
ADR(14)	17	*IR(6)*
ADR(15)	18	*IR(7)*
---	19	BRAS
WR	20	BCAS
OUTR	21	REF
INR	22	ROWEN
RR	23	WRITE
AFBR	24	*EOPIN*
---	25	*EOPOUT*

<SIGNAL NAME> : The signal is active low.

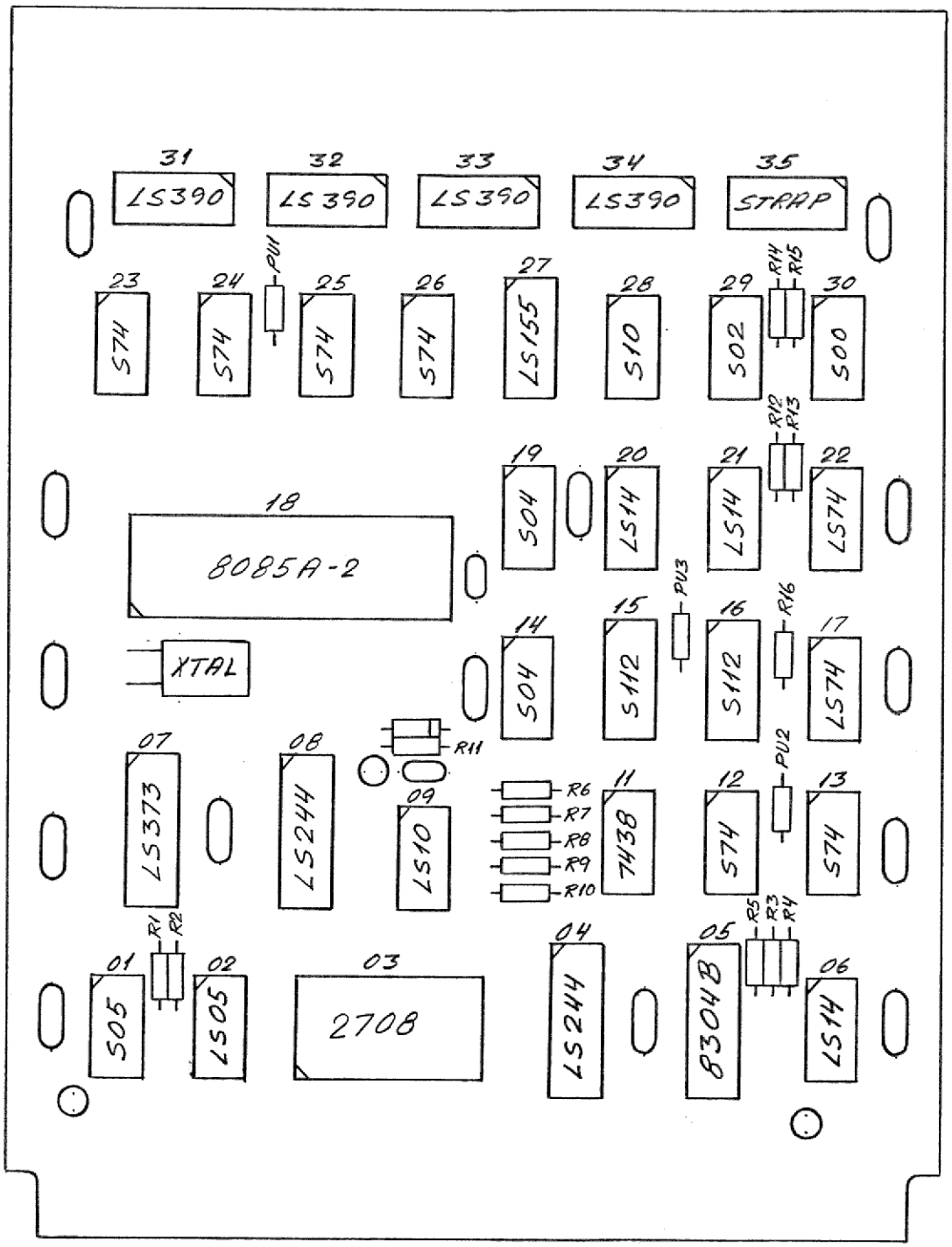
Appendix 1.1: SPC-1 BUS SYSTEM.

SOLDER SIDE SIDE A	PIN NO.	COMPONENT SIDE SIDE B
ABUSDISABLE	26	*DBUSDISABLE*
---	27	*HOLDR*
VENT	28	HOLDA
INT	29	*DMAACK(0)*
---	30	*DMAACK(1)*
---	31	*DMAACK(2)*
D(0)	32	*DMAACK(3)*
D(1)	33	*DMAACK(4)*
D(2)	34	*DMAACK(5)*
D(3)	35	*DMAACK(6)*
D(4)	36	*DMAACK(7)*
D(5)	37	*DMAREQ(0)*
D(6)	38	*DMAREQ(1)*
D(7)	39	*DMAREQ(2)*
OUTDMA	40	*DMAREQ(3)*
INDMA	41	*DMAREQ(4)*
---	42	*DMAREQ(5)*
RST 5.5	43	*DMAREQ(6)*
RST 6.5	44	*DMAREQ(7)*
RESET	45	---
---	46	---
SOD	47	O2
16Mhz	48	16Mhz
GND	49	+12V
GND	50	+5V

<SIGNAL NAME> : The signal is active low.

Appendix 1.3 : Logic schematic

ID-8530



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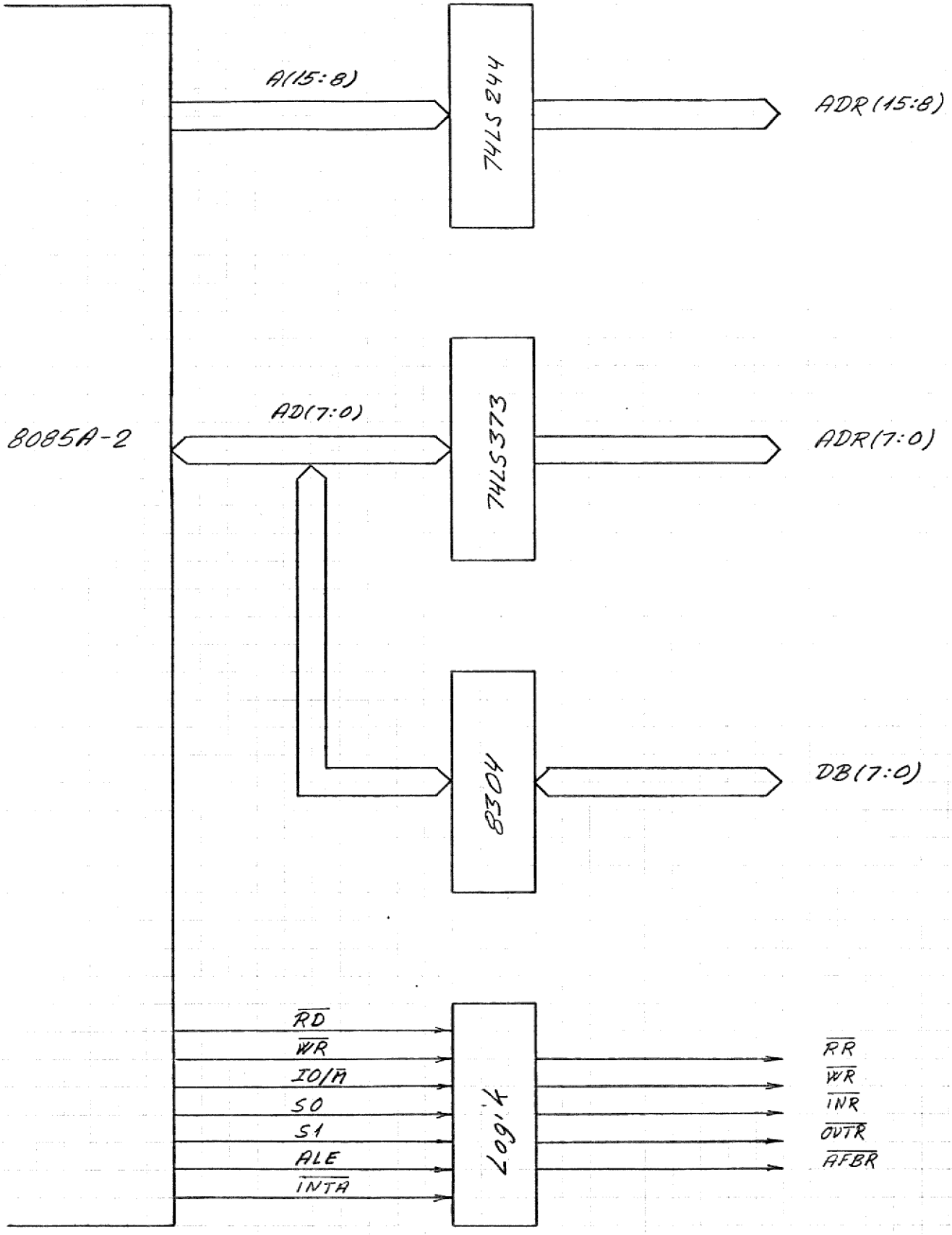
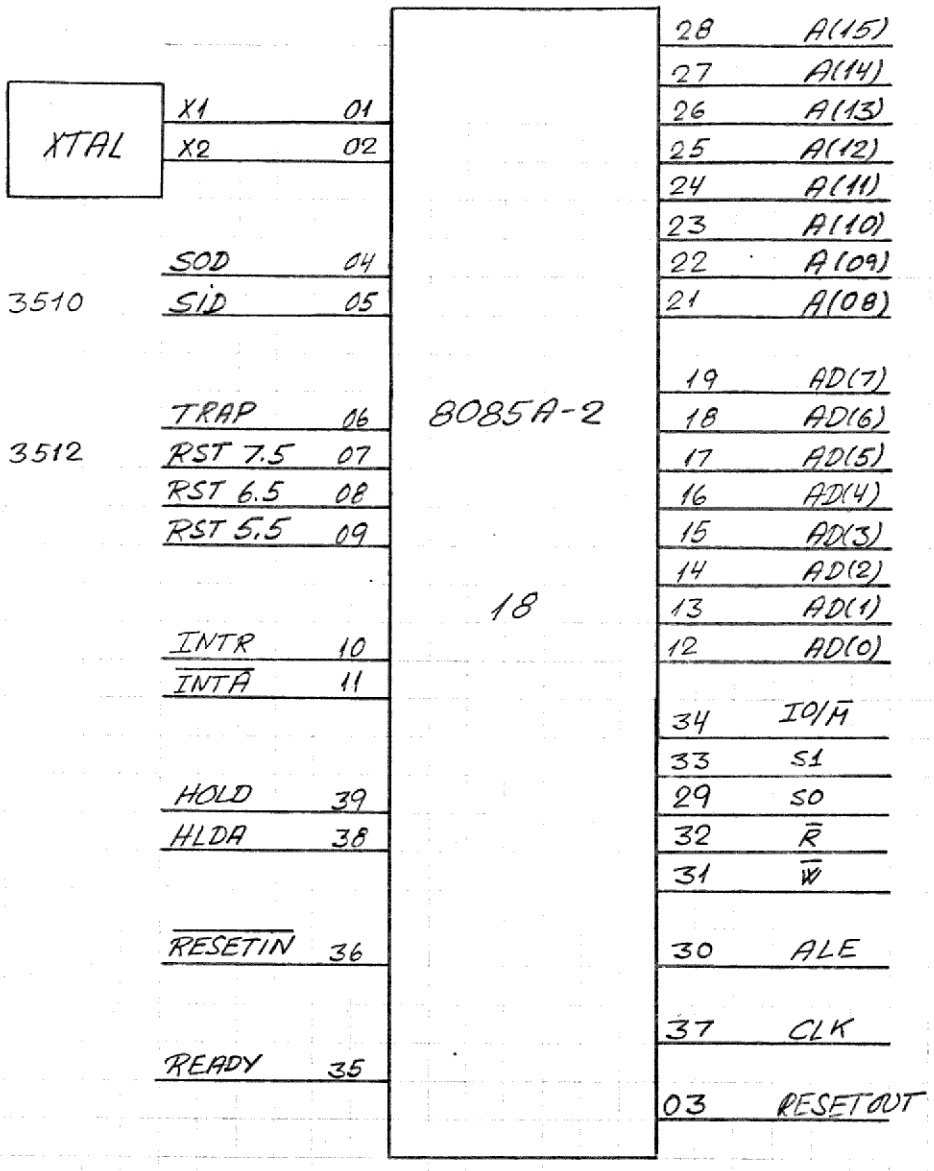
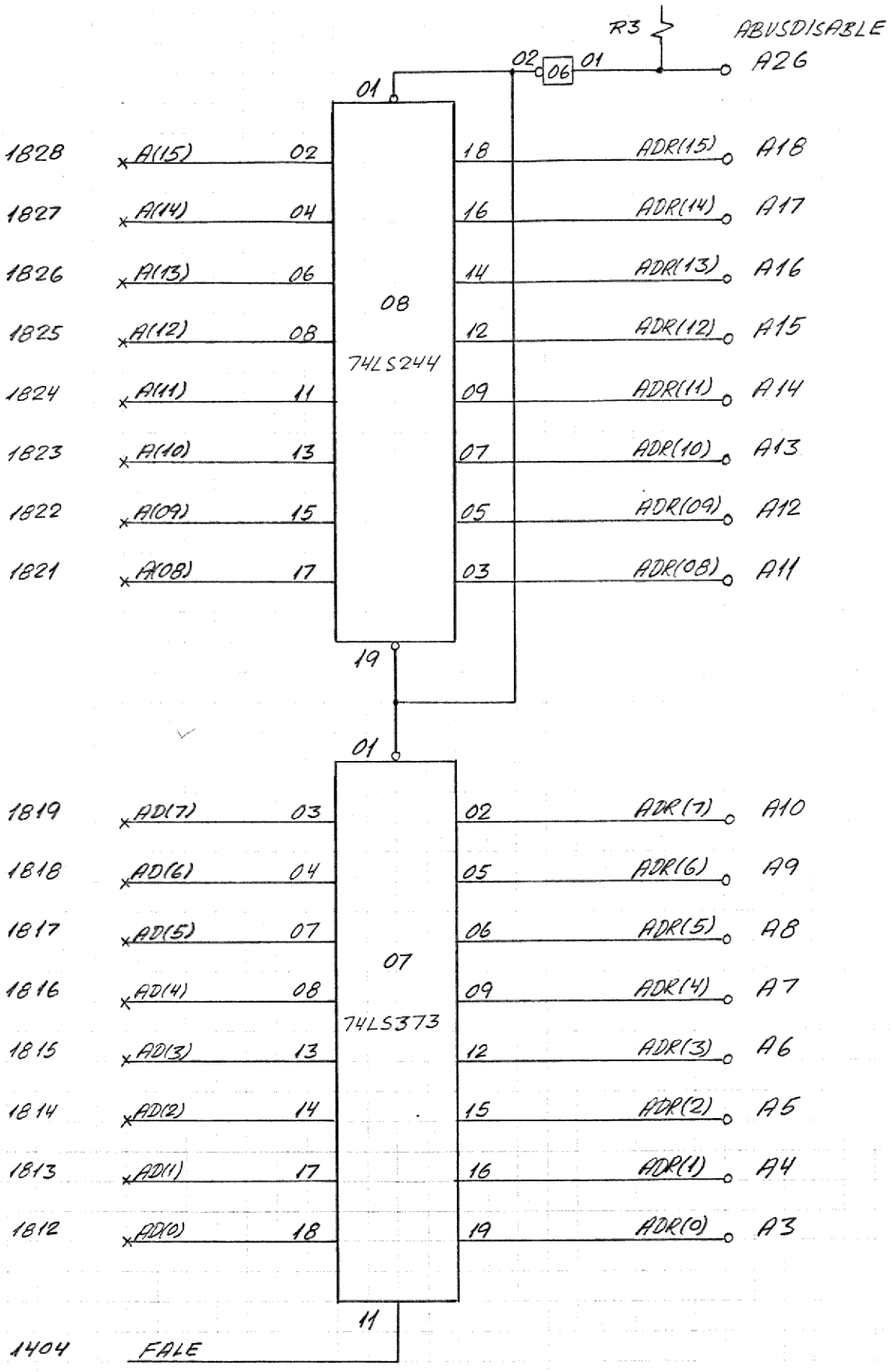
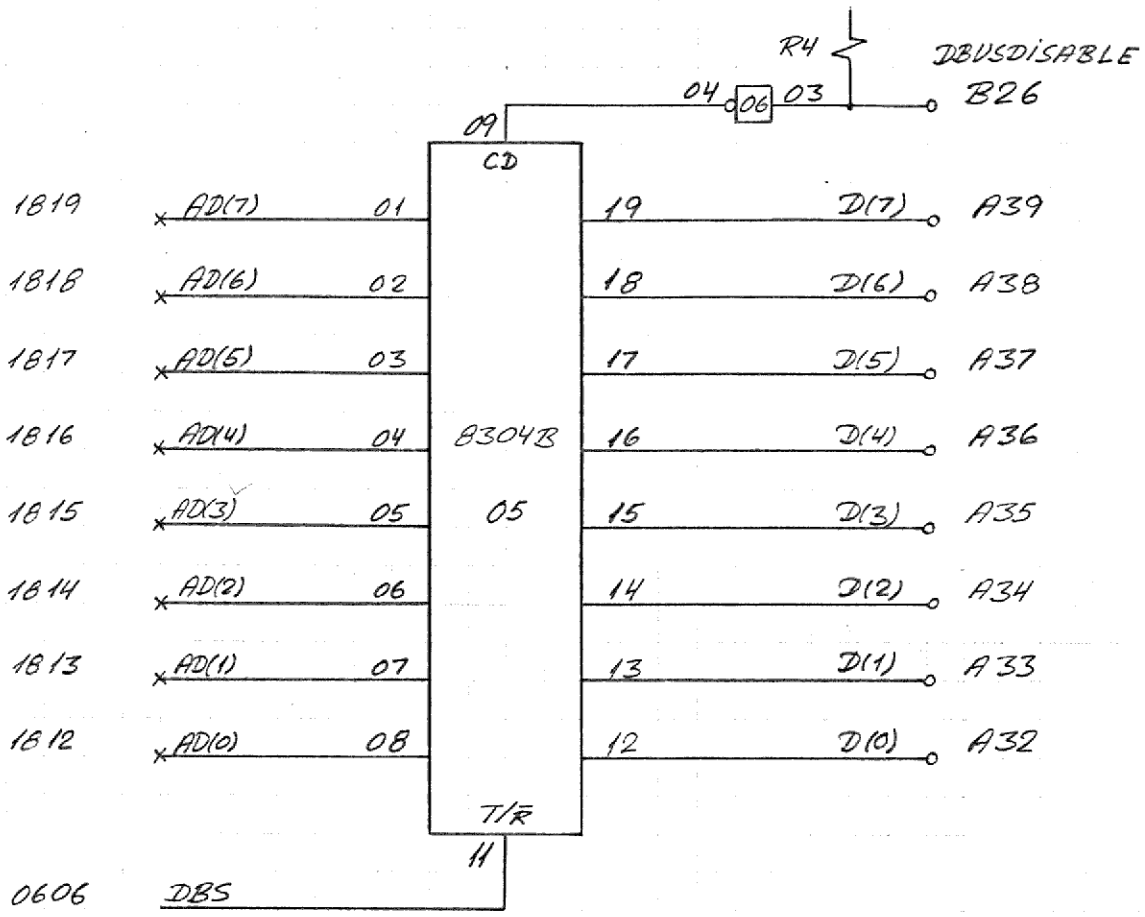
ID-8530 SURVEY

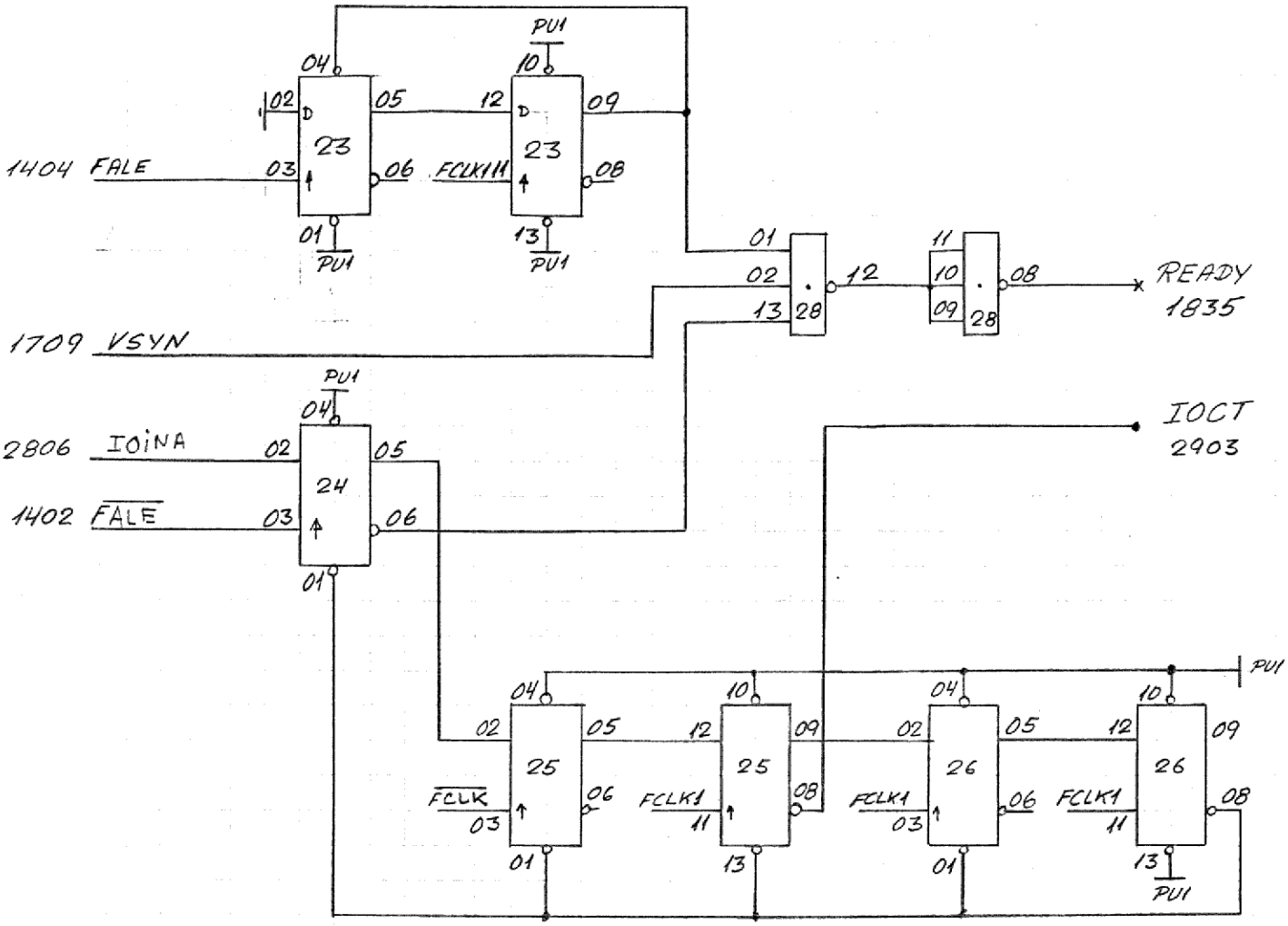
Initialer/dato	Side
KAN 790523	1
Revideret	Projekt 7030-2

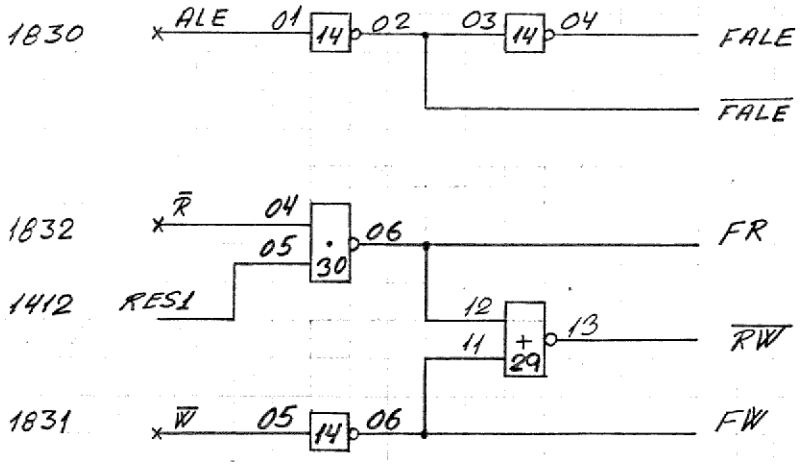



XTAL
X1 01
X2 02
SOD 04
3510 SID 05
TRAP 06
3512 RST 7.5 07
RST 6.5 08
RST 5.5 09
INTR 10
INTA 11
HOLD 39
HLDA 38
RESETIN 36
READY 35
8085A-2
18
28 A(15)
27 A(14)
26 A(13)
25 A(12)
24 A(11)
23 A(10)
22 A(09)
21 A(08)
19 AD(7)
18 AD(6)
17 AD(5)
16 AD(4)
15 AD(3)
14 AD(2)
13 AD(1)
12 AD(0)
34 IO/M
33 S1
29 SO
32 RD
31 WR
30 ALE
37 CLK
03 RESETOUT


R3
ABUSDISABLE
02
06
01
A26
01
08
74LS244
1828
A(15)
02
18
ADR(15)
A18
1827
A(14)
04
16
ADR(14)
A17
1826
A(13)
06
14
ADR(13)
A16
1825
A(12)
08
12
ADR(12)
A15
1824
A(11)
11
09
ADR(11)
A14
1823
A(10)
13
07
ADR(10)
A13
1822
A(09)
15
05
ADR(09)
A12
1821
A(08)
17
03
ADR(08)
A11
19
01
07
74LS373
1819
AD(7)
03
02
ADR(7)
A10
1818
AD(6)
04
05
ADR(6)
A9
1817
AD(5)
07
06
ADR(5)
A8
1816
AD(4)
08
09
ADR(4)
A7
1815
AD(3)
13
12
ADR(3)
A6
1814
AD(2)
14
15
ADR(2)
A5
1813
AD(1)
17
16
ADR(1)
A4
1812
AD(0)
18
19
ADR(0)
A3
11
1404
FALE

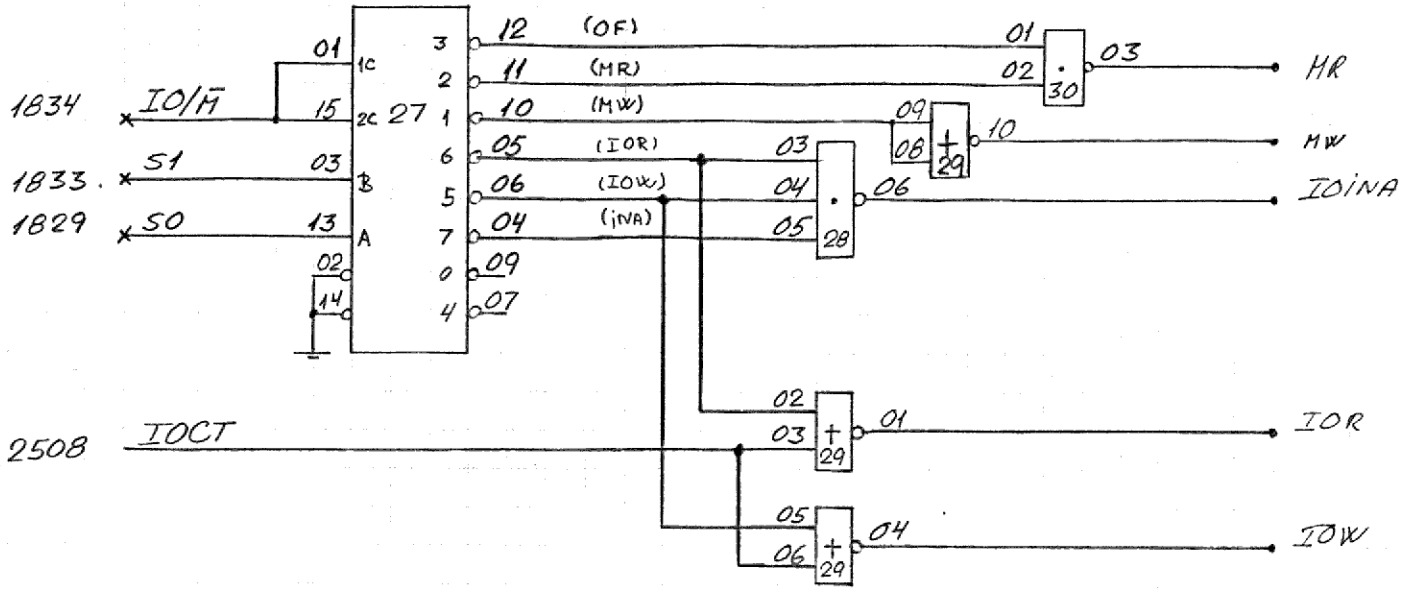

R4
DBUSDISABLE
04
06
03
B26
09
CD
1819
AD(7)
01
19
D(7)
A39
1818
AD(6)
02
18
D(6)
A38
1817
AD(5)
03
17
D(5)
A37
1816
AD(4)
04
8304B
16
D(4)
A36
1815
AD(3)
05
05
15
D(3)
A35
1814
AD(2)
06
14
D(2)
A34
1813
AD(1)
07
13
D(1)
A33
1812
AD(0)
08
12
D(0)
A32
T/R
11
0606
DBS

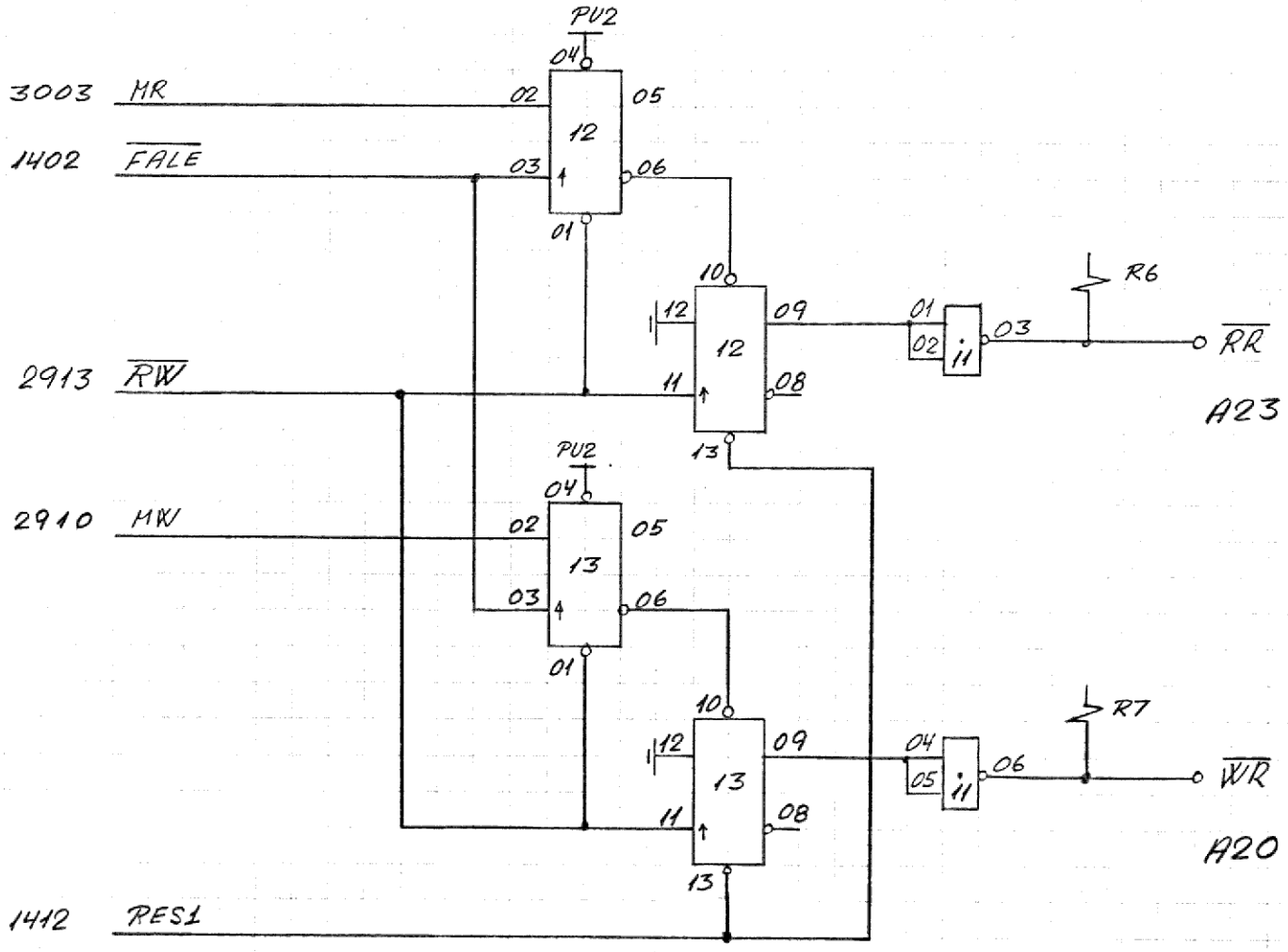

PU1
04
10
02
D
05
12
D
09
23
23
1404 FALE
03
06
FCLK111
08
01
PU1
13
PU1
01
02
13
28
12
11
10
09
28
08
READY
1835
1709 VSYN
PU1
04
IOCT
2903
2806 IOINA
02
05
24
1402 FALE
03
06
01
PU1
04
10
04
10
02
05
12
09
02
05
12
09
25
25
26
26
FCLK
03
06
FCLK1
11
08
FCLK1
03
06
FCLK1
11
08
01
13
01
13
PU1

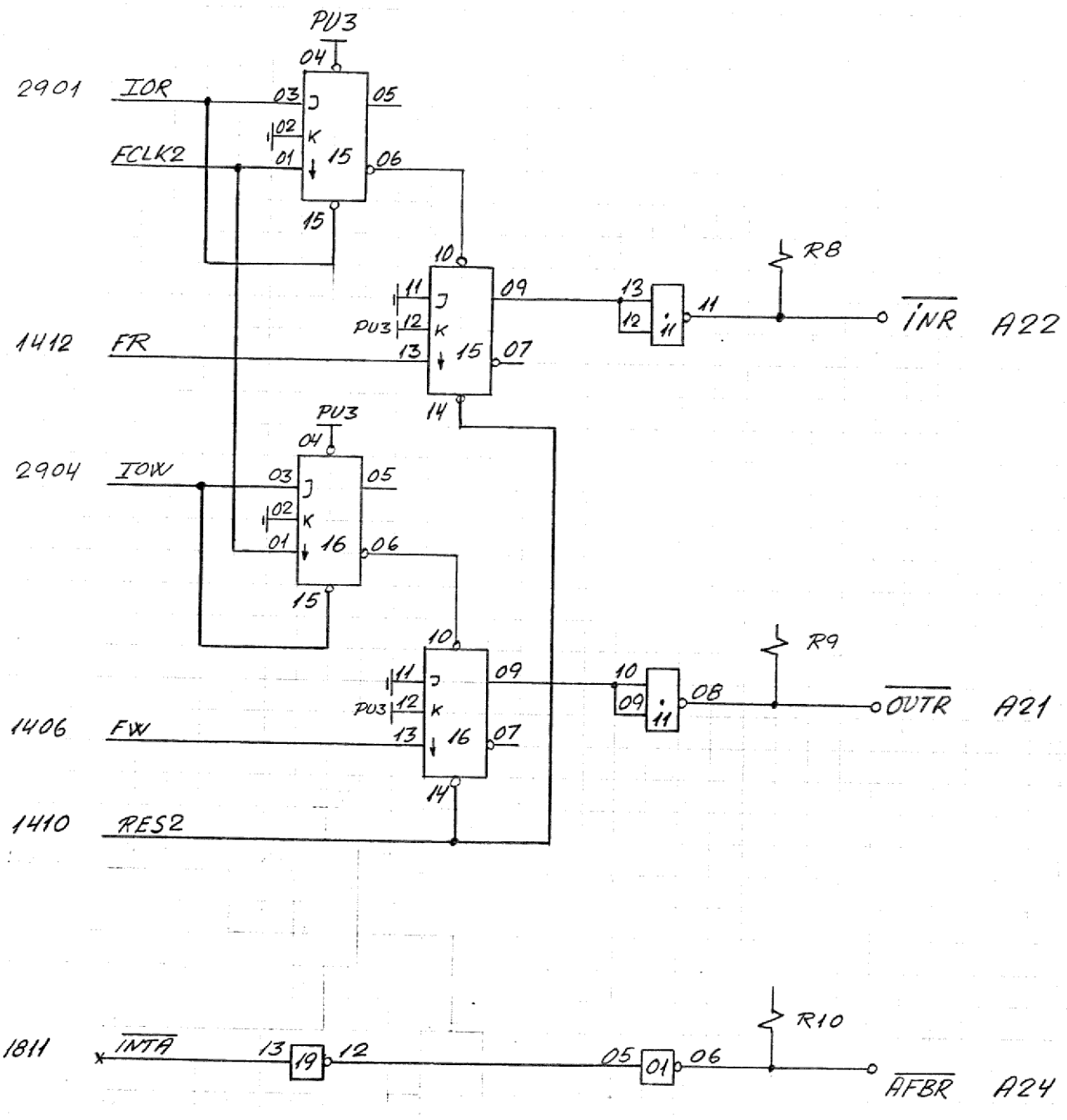

1830
ALE
01
14
02
03
14
04
FALE
FALE
1832
R
04
05
30
06
FR
1412
RES1
12
11
+
29
13
RW
1831
W
05
14
06
FW

Generering af styresignaler

Initialer/dato	Side
KAN 790719	6
Revideret	Projekt



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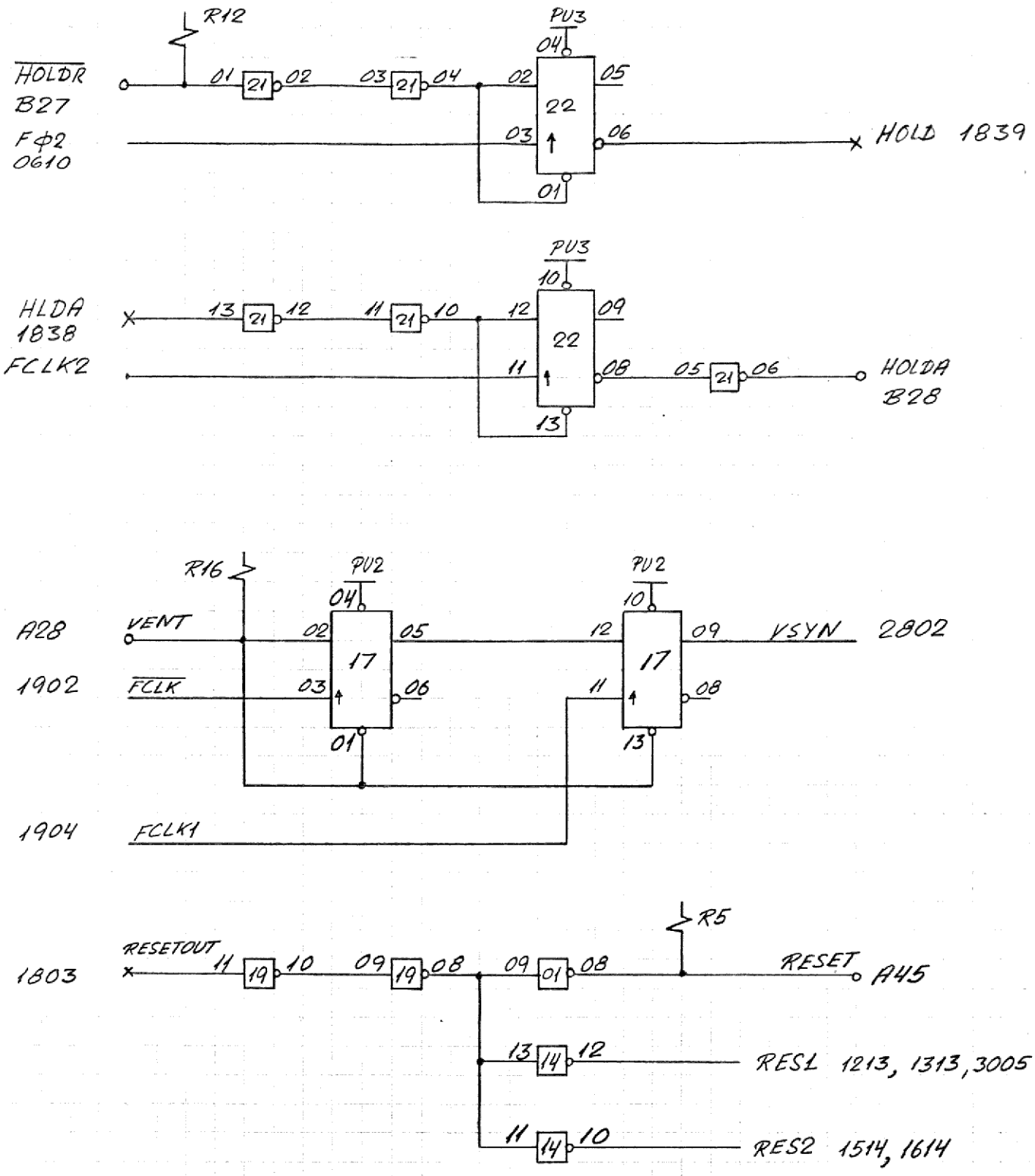
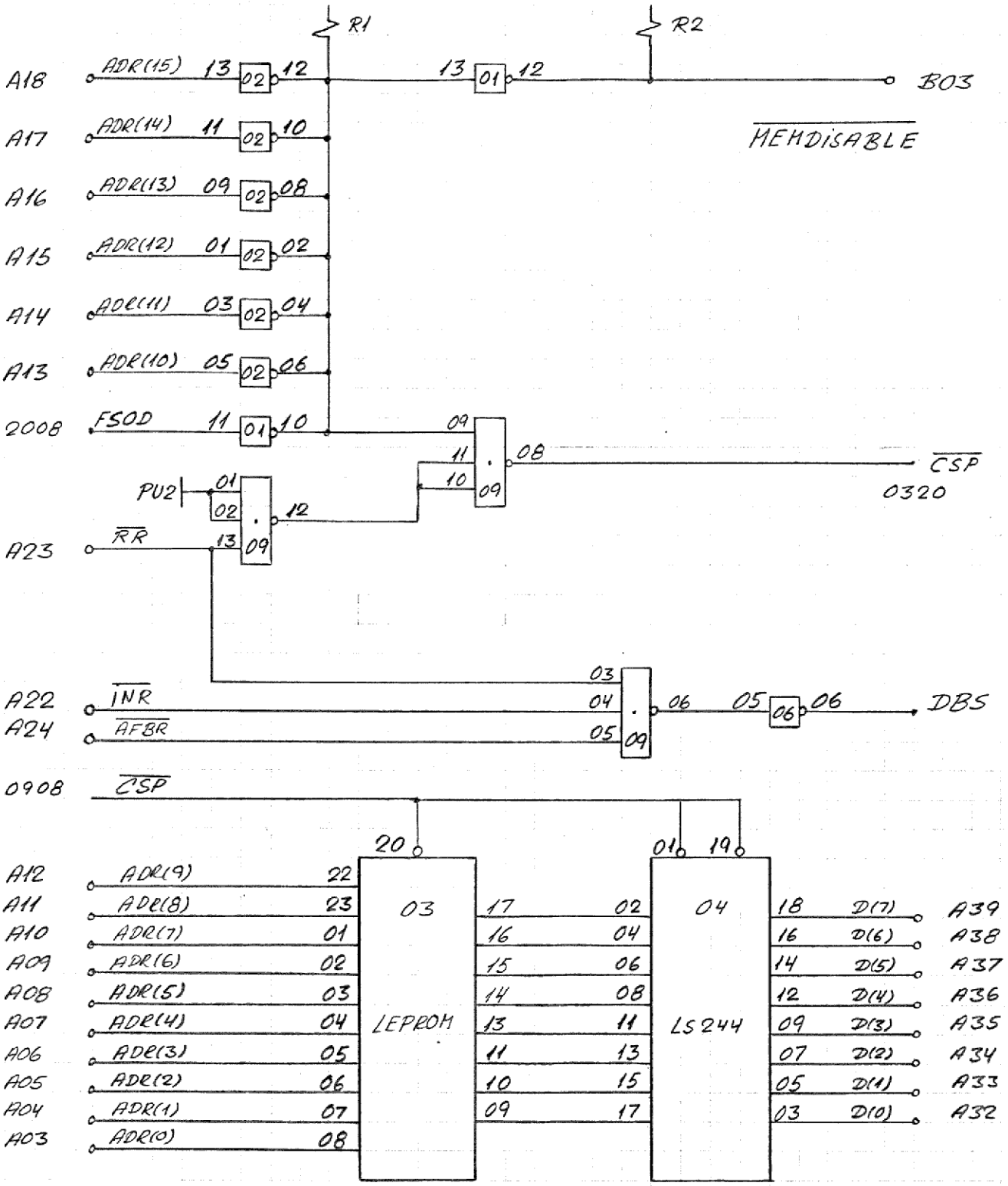
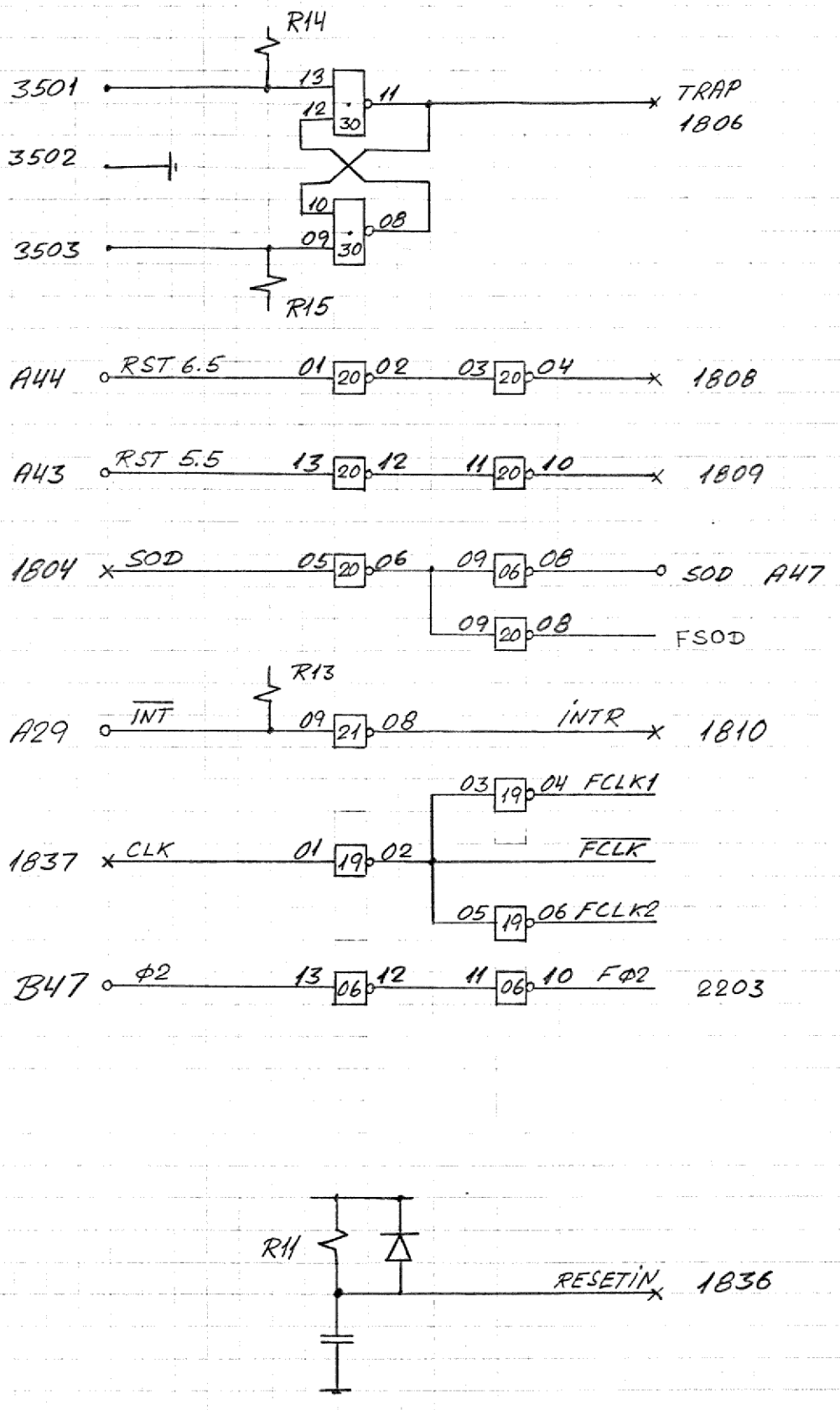
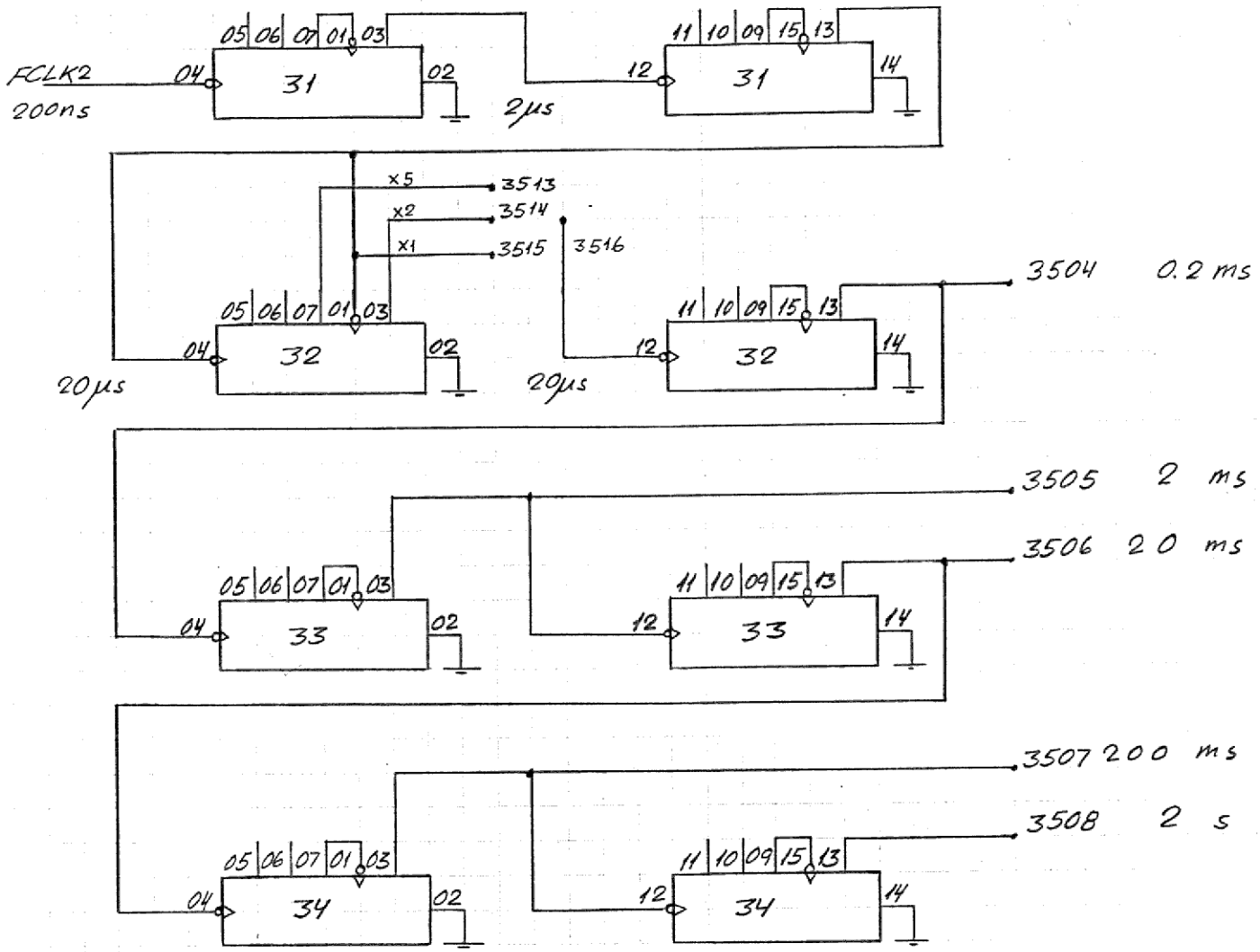
2901
IOR
FCLK2
FR
2904
IOW
FW
1406
1410
RES2
R8
R9
R10
INR
OUTR
AFBR
A22
A21
A24
1811
INTA

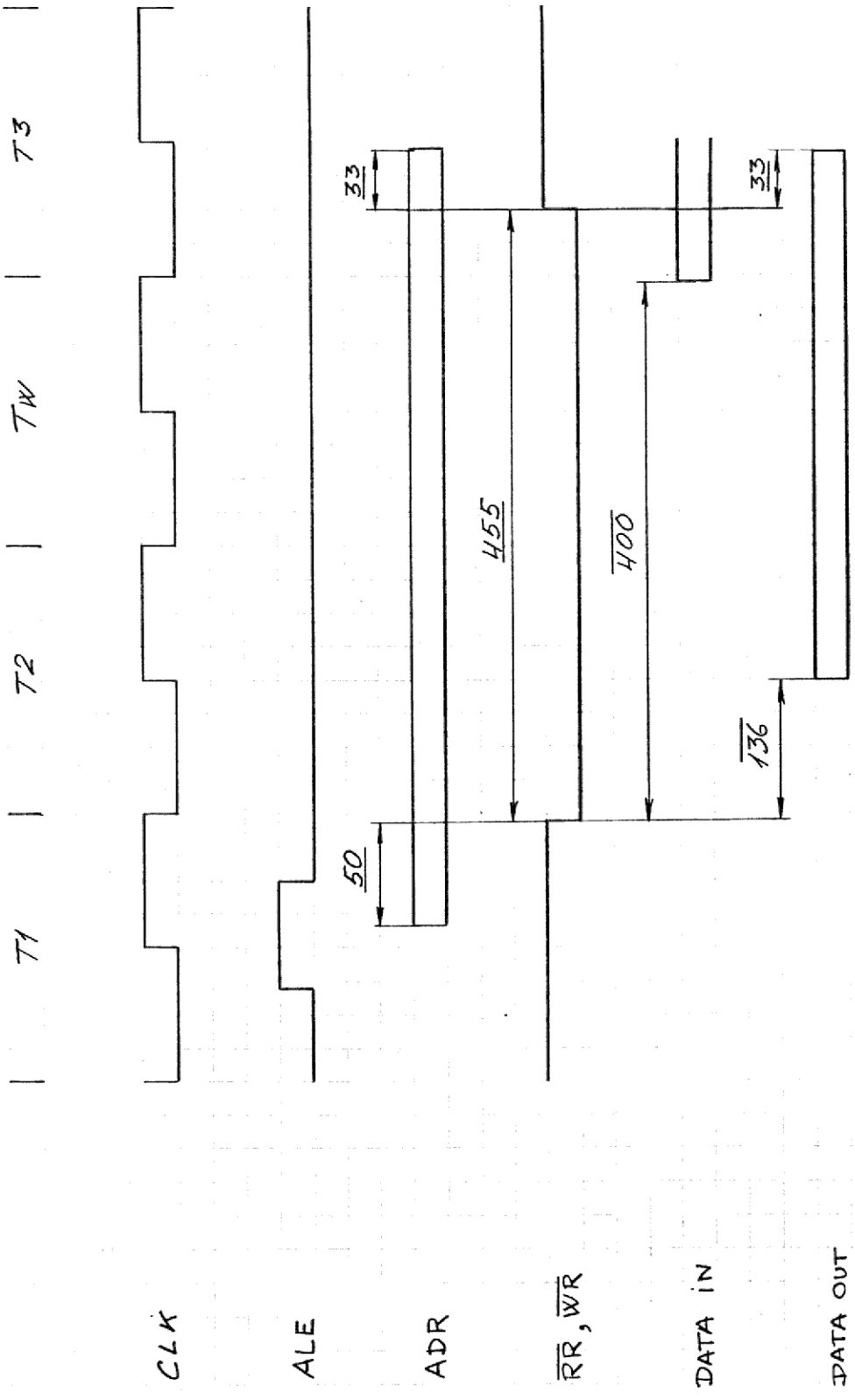

R12
PU3
HOLDR
B27
FΦ2
0610
HOLD 1839
HLDA
1838
FCLK2
HOLDA
B28
R16
PU2
A28
VENT
FCLK
1902
VSYN 2802
1904
FCLK1
1803
RESETOUT
R5
RESET A45
RES1 1213, 1313, 3005
RES2 1514, 1614

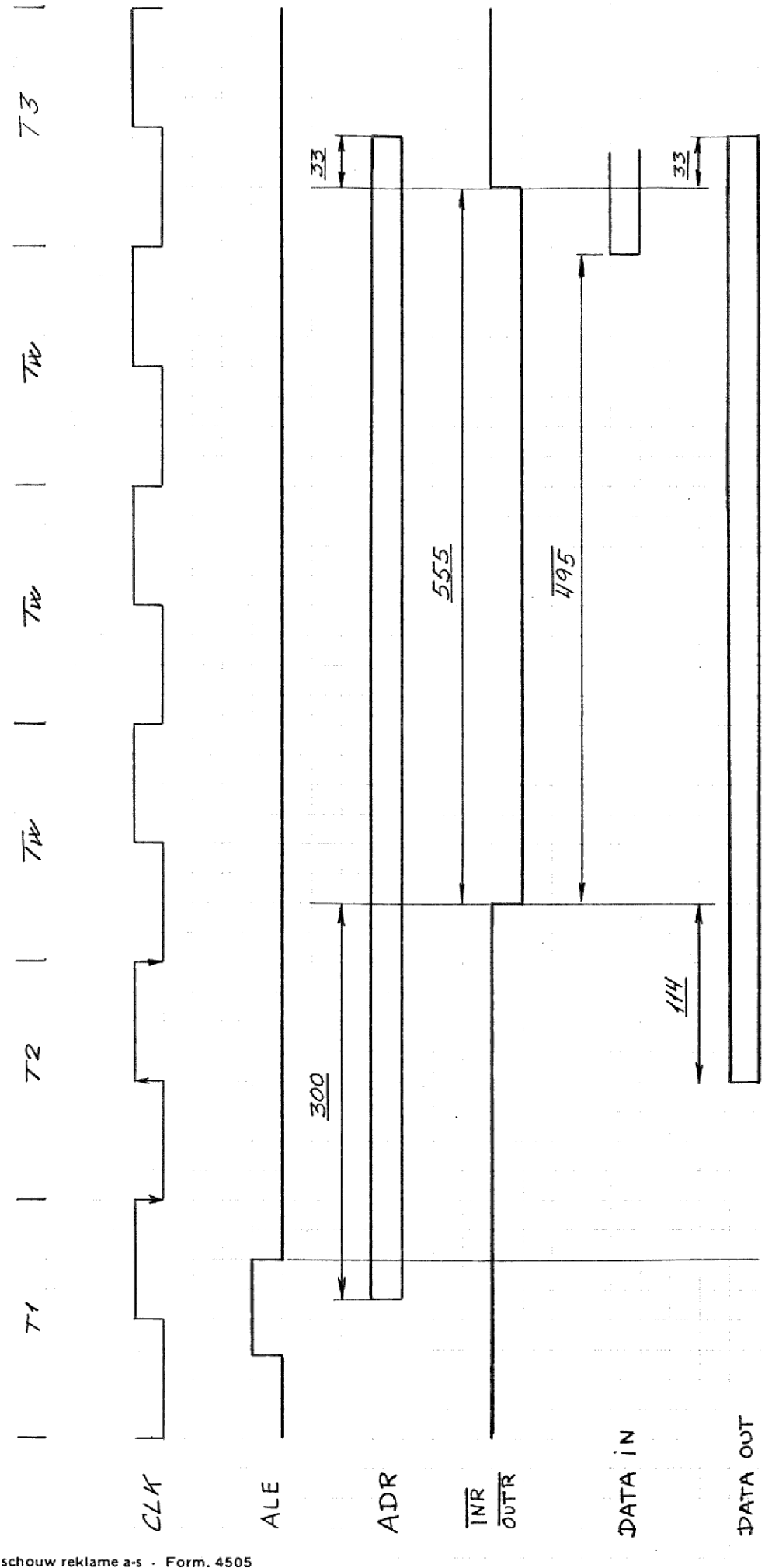

R1
R2
A18
ADR(15)
A17
ADR(14)
A16
ADR(13)
A15
ADR(12)
A14
ADR(11)
A13
ADR(10)
2008
FSOD
PU2
A23
RR
A22
INR
A24
AFBR
0908
CSP
BO3
MEMDISABLE
CSP
0320
DBS
A12
A11
A10
A09
A08
A07
A06
A05
A04
A03
ADR(9)
ADR(8)
ADR(7)
ADR(6)
ADR(5)
ADR(4)
ADR(3)
ADR(2)
ADR(1)
ADR(0)
03
LEPROM
04
LS244
D(7)
D(6)
D(5)
D(4)
D(3)
D(2)
D(1)
D(0)
A39
A38
A37
A36
A35
A34
A33
A32


R14
3501
13
12
30
11
TRAP
1806
3502
10
09
30
08
3503
R15
A44
RST 6.5
01
20
02
03
20
04
1808
A43
RST 5.5
13
20
12
11
20
10
1809
1804
SOD
05
20
06
09
06
08
SOD A47
09
20
08
FSOD
R13
A29
INT
09
21
08
INTR
1810
03
19
04 FCLK1
1837
CLK
01
19
02
FCLK
05
19
06 FCLK2
B47
Φ2
13
06
12
11
06
10 FΦ2
2203
R11
RESETIN
1836

Henning Jensen afd 415 B, K.

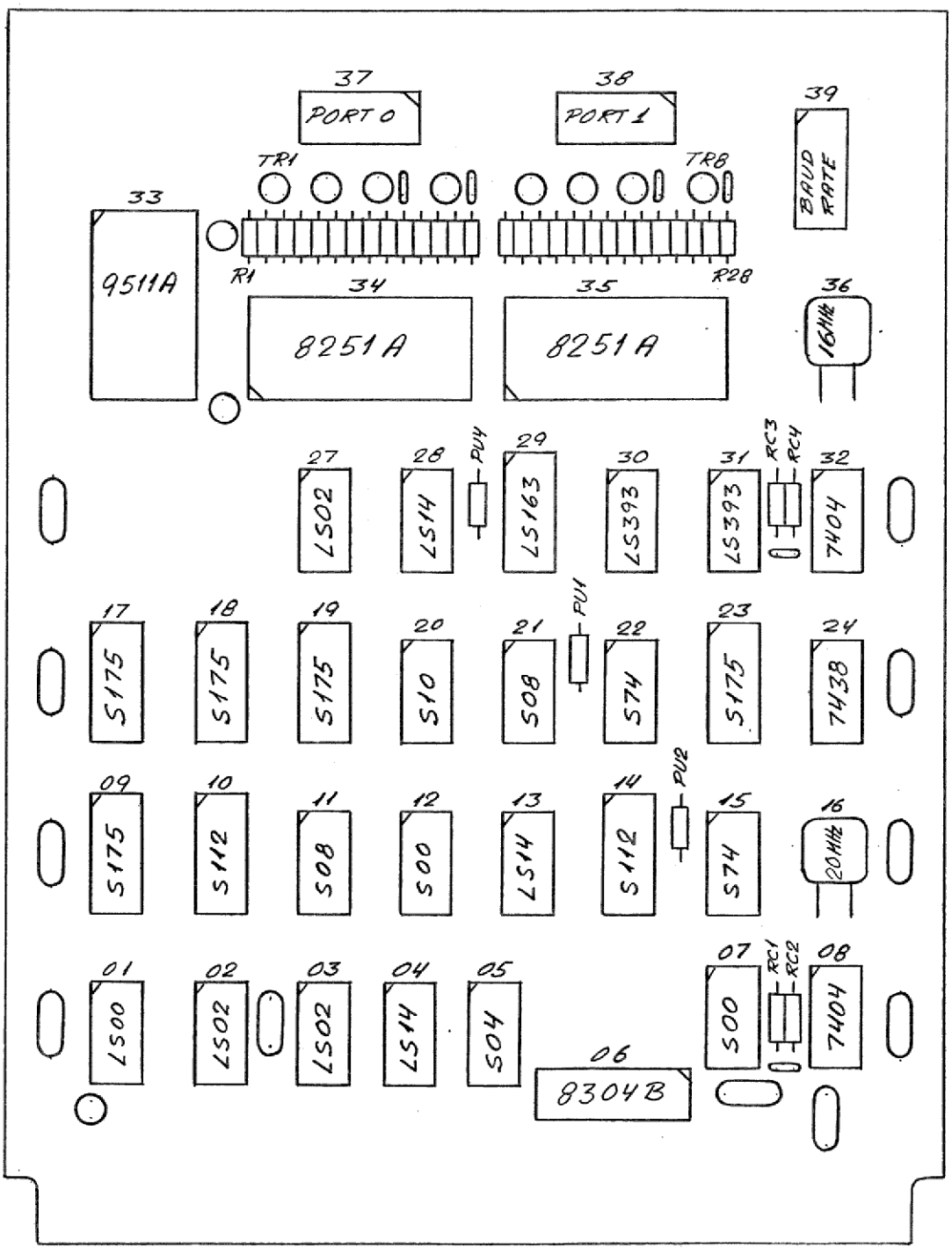


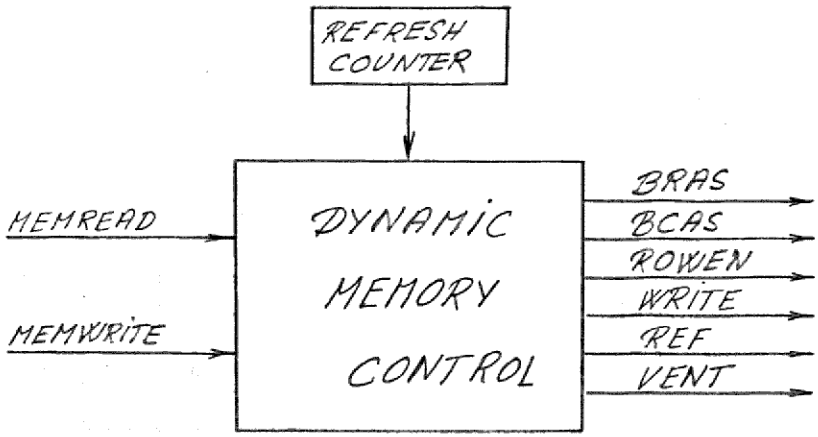

T3
Tw
T2
T1
33
455
400
33
50
136
CLK
ALE
ADR
RD, WR
DATA IN
DATA OUT

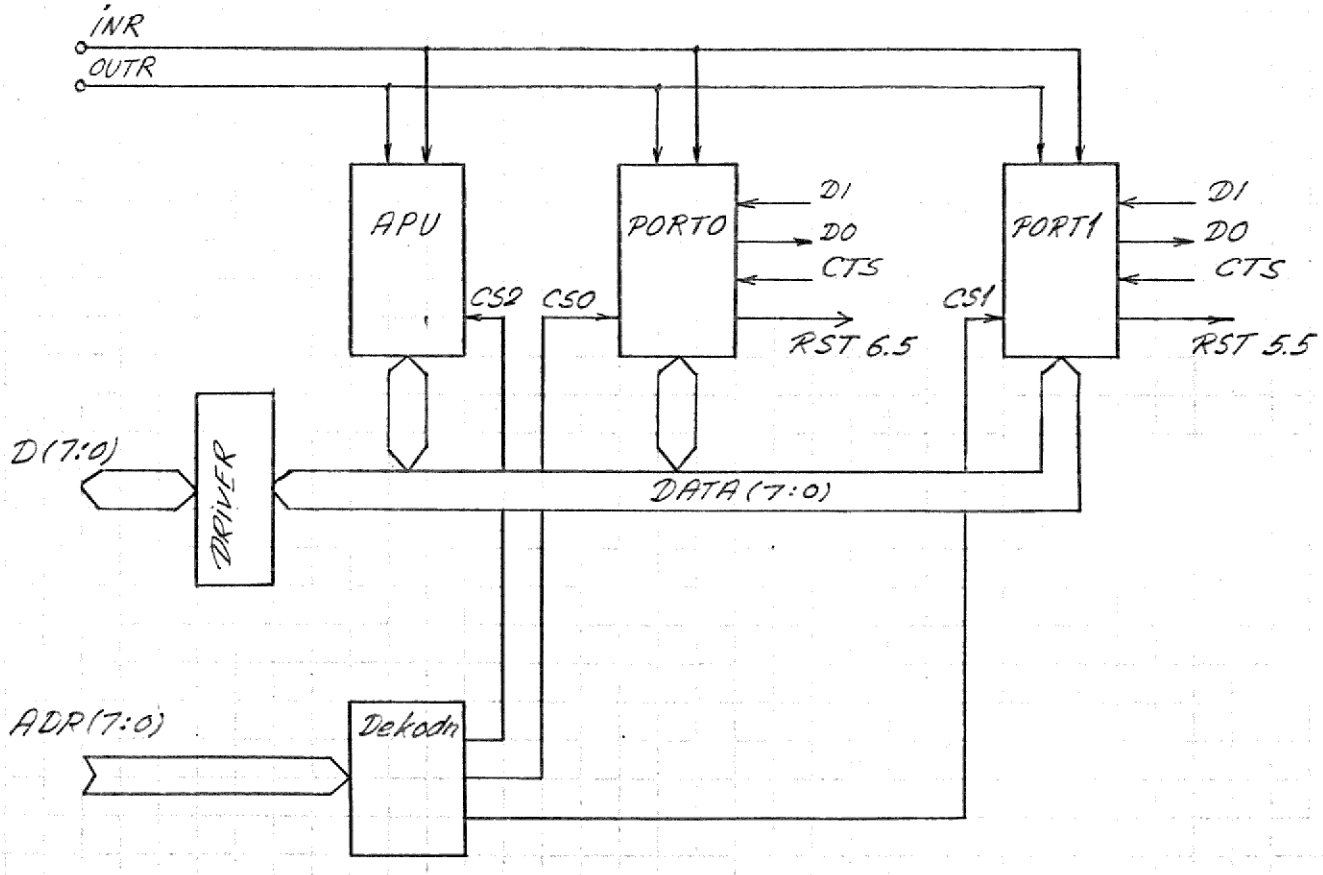

T3
Tw
Tw
Tw
T2
T1
CLK
ALE
ADR
INR
OUTR
DATA IN
DATA OUT
33
33
555
1195
300
114

Appendix 2.3 : Logic schematic

ID-8538

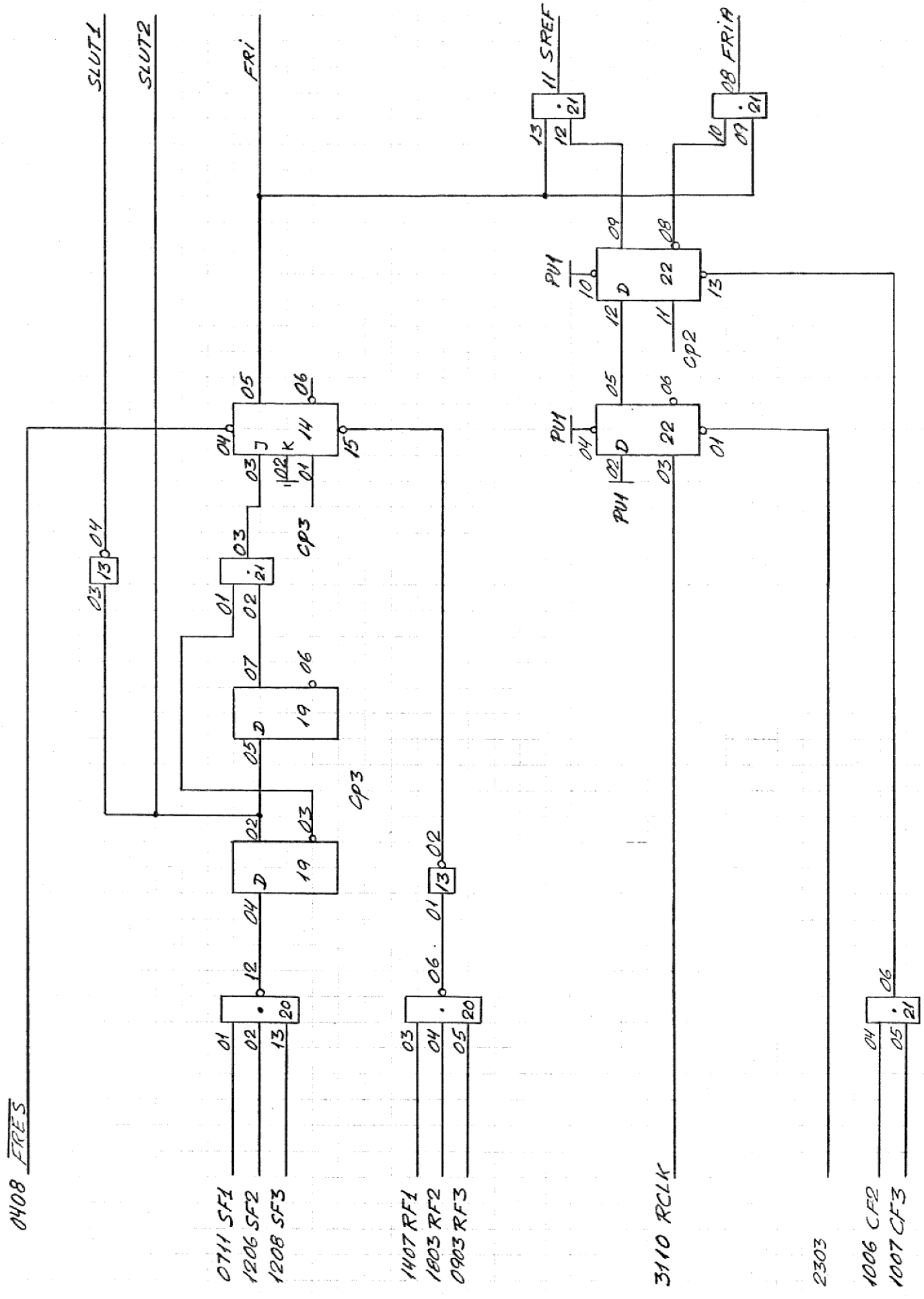


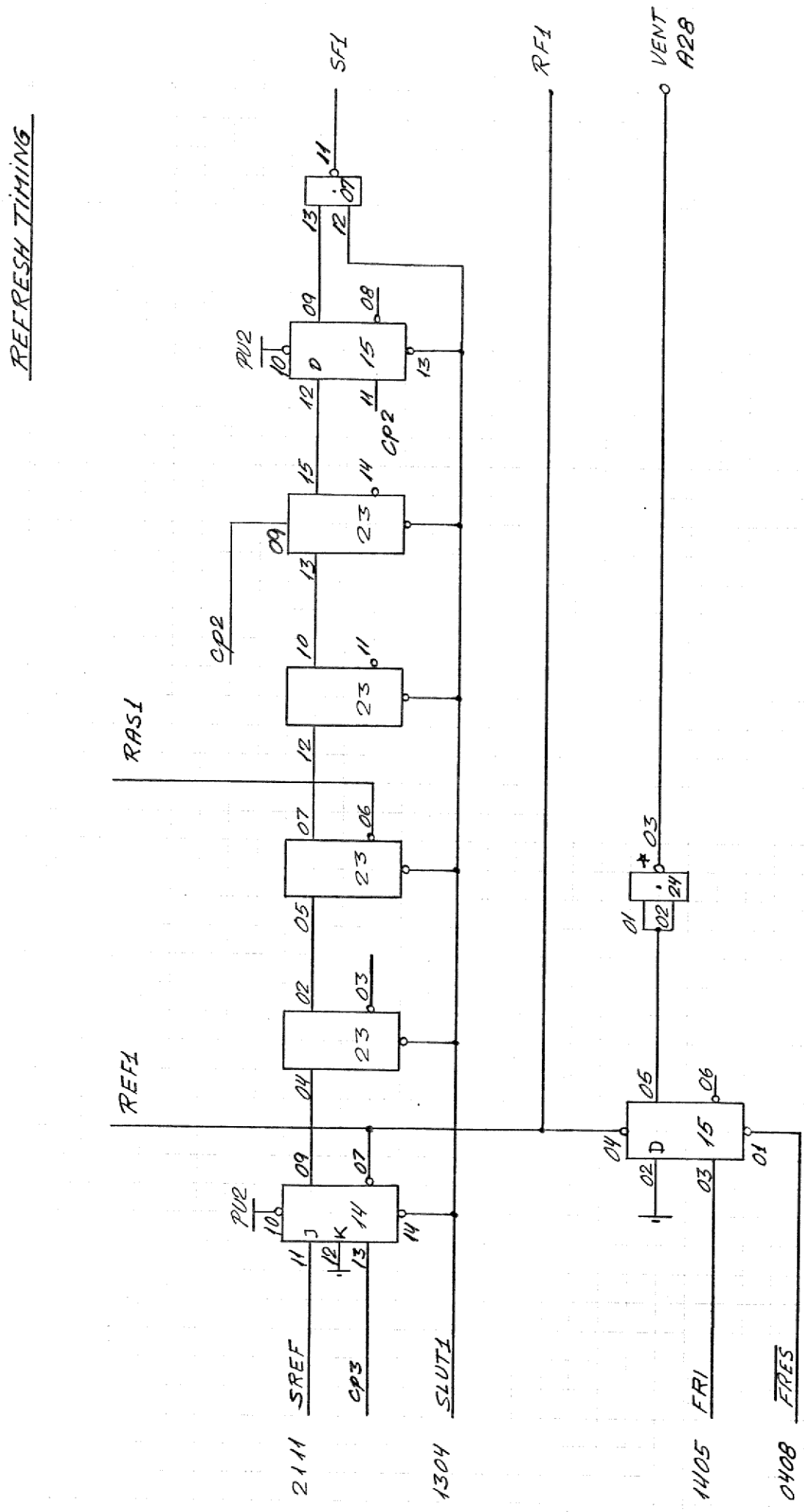

REFRESH COUNTER
MEMREAD
MEMWRITE
DYNAMIC MEMORY CONTROL
BRAS
BCAS
ROWEN
WRITE
REF
VENT


INR
OUTR
APU
PORTO
PORT1
DI
DO
CTS
CS2
CS0
CS1
RST 6.5
RST 5.5
D(7:0)
DRIVER
DATA(7:0)
ADR(7:0)
Dekodn

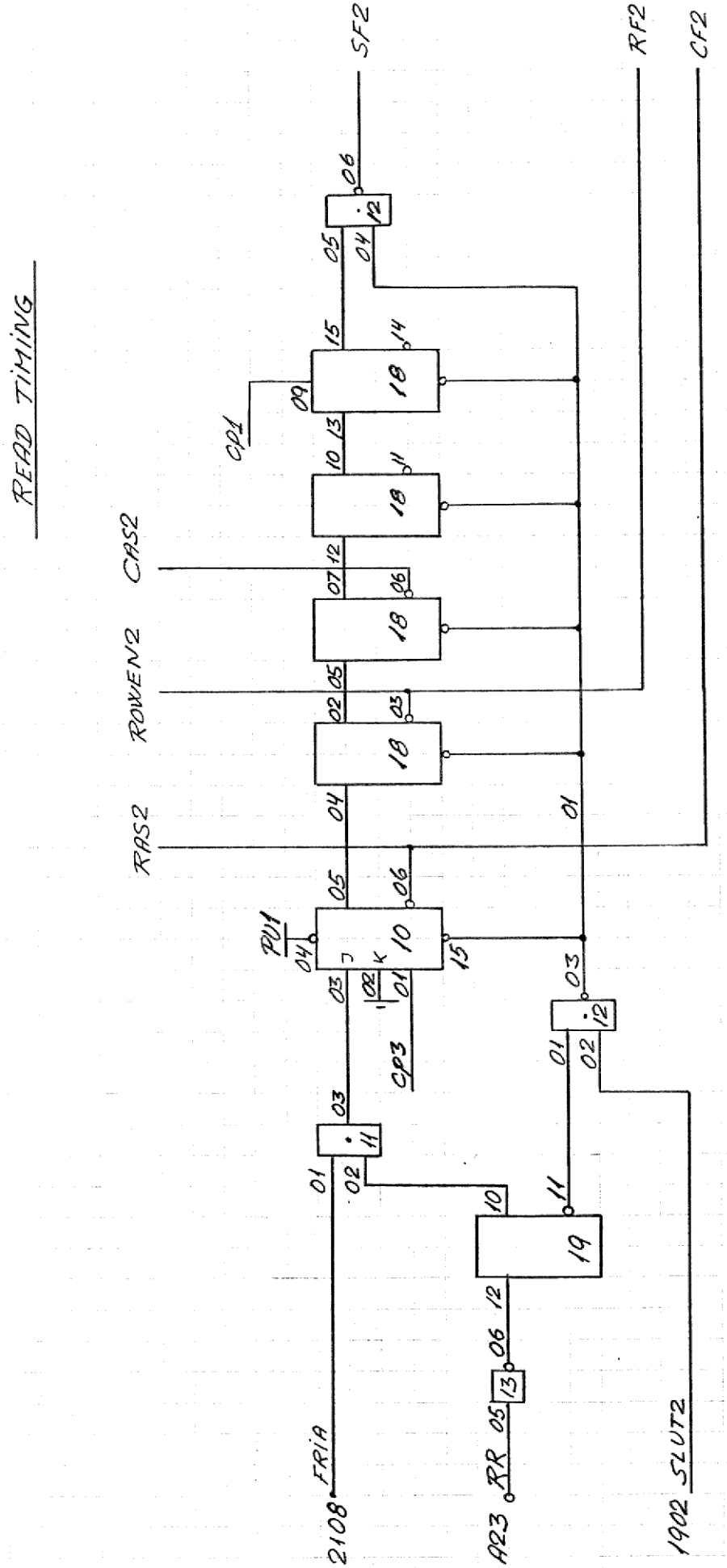
dansk data elektronik aps

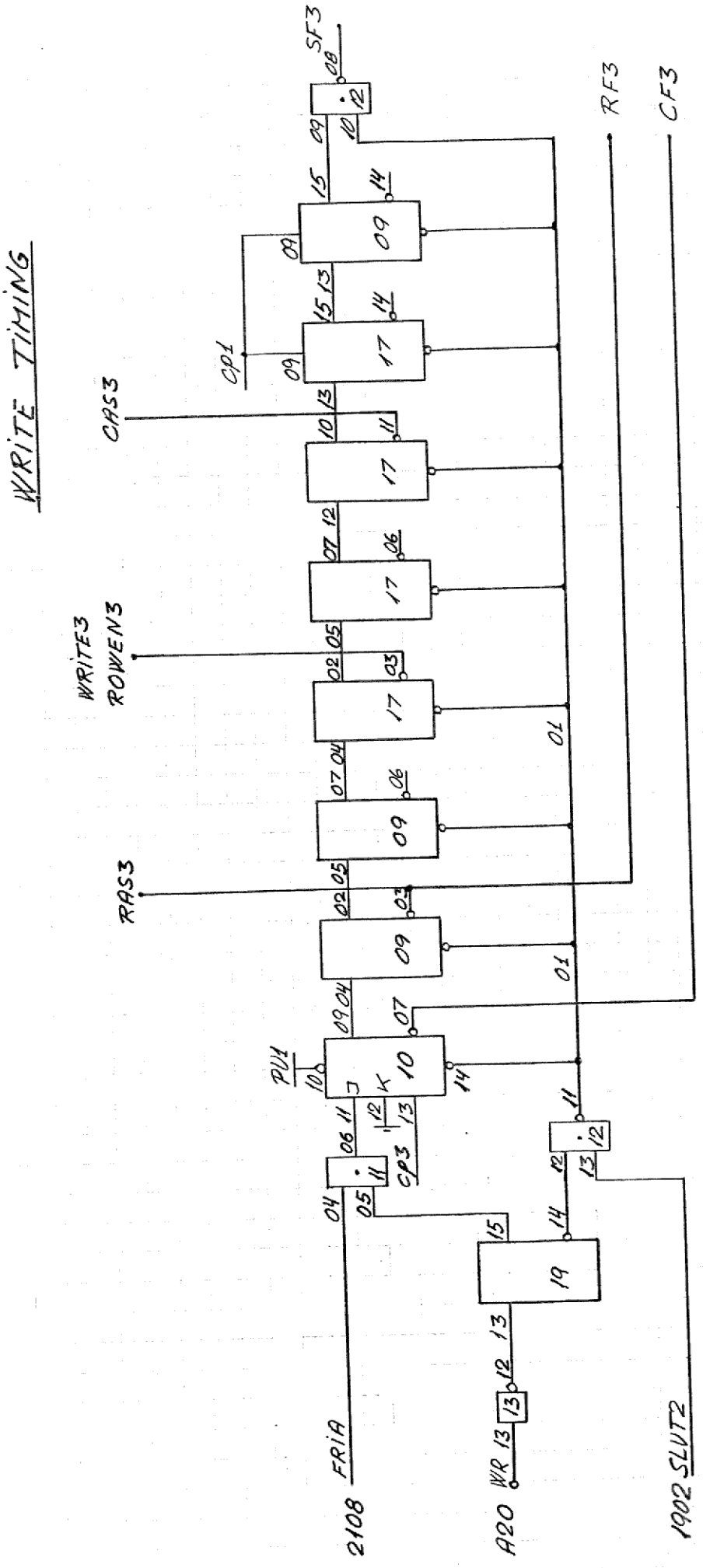
Initialer/dato	Side
KAN 790712	1
Revideret	Projekt

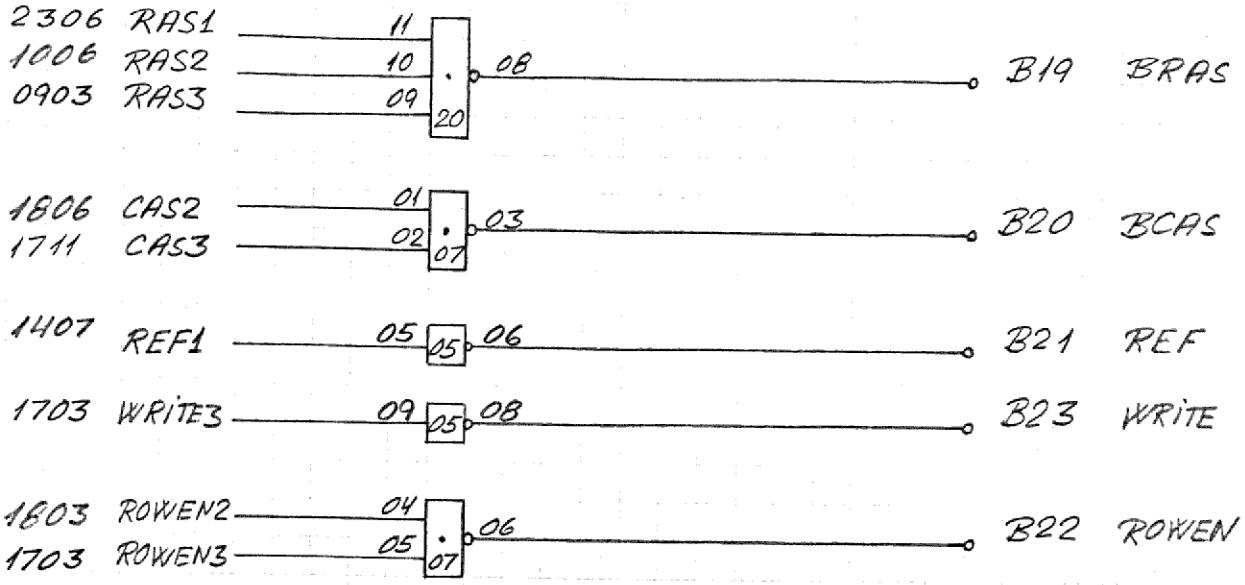


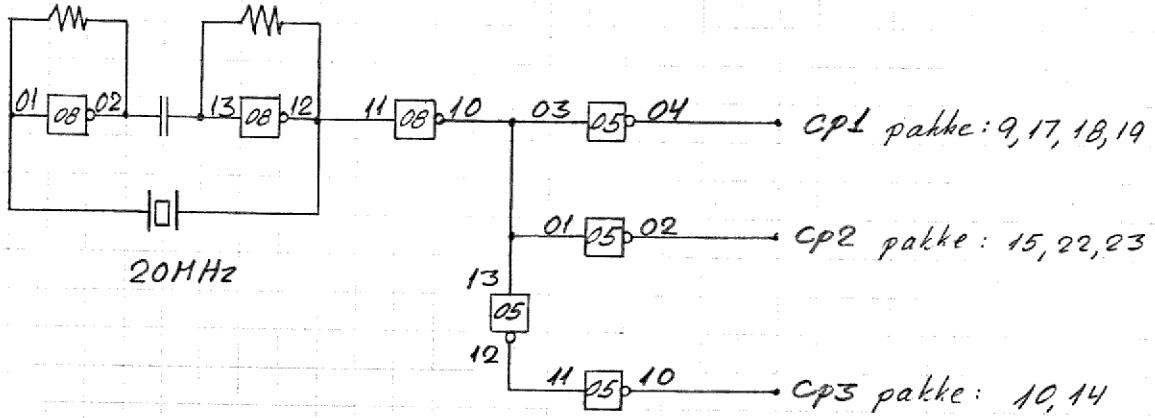

REFRESH TIMING
SFI
RFI
VENT
A28
RAS1
REF1
CP2
PU2
SREF
CP3
SLUT1
FRI
FRES
2111
1304
14405
0408

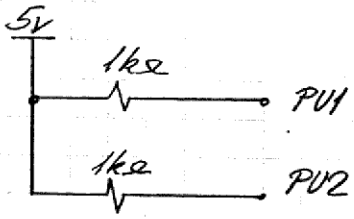
READ TIMING

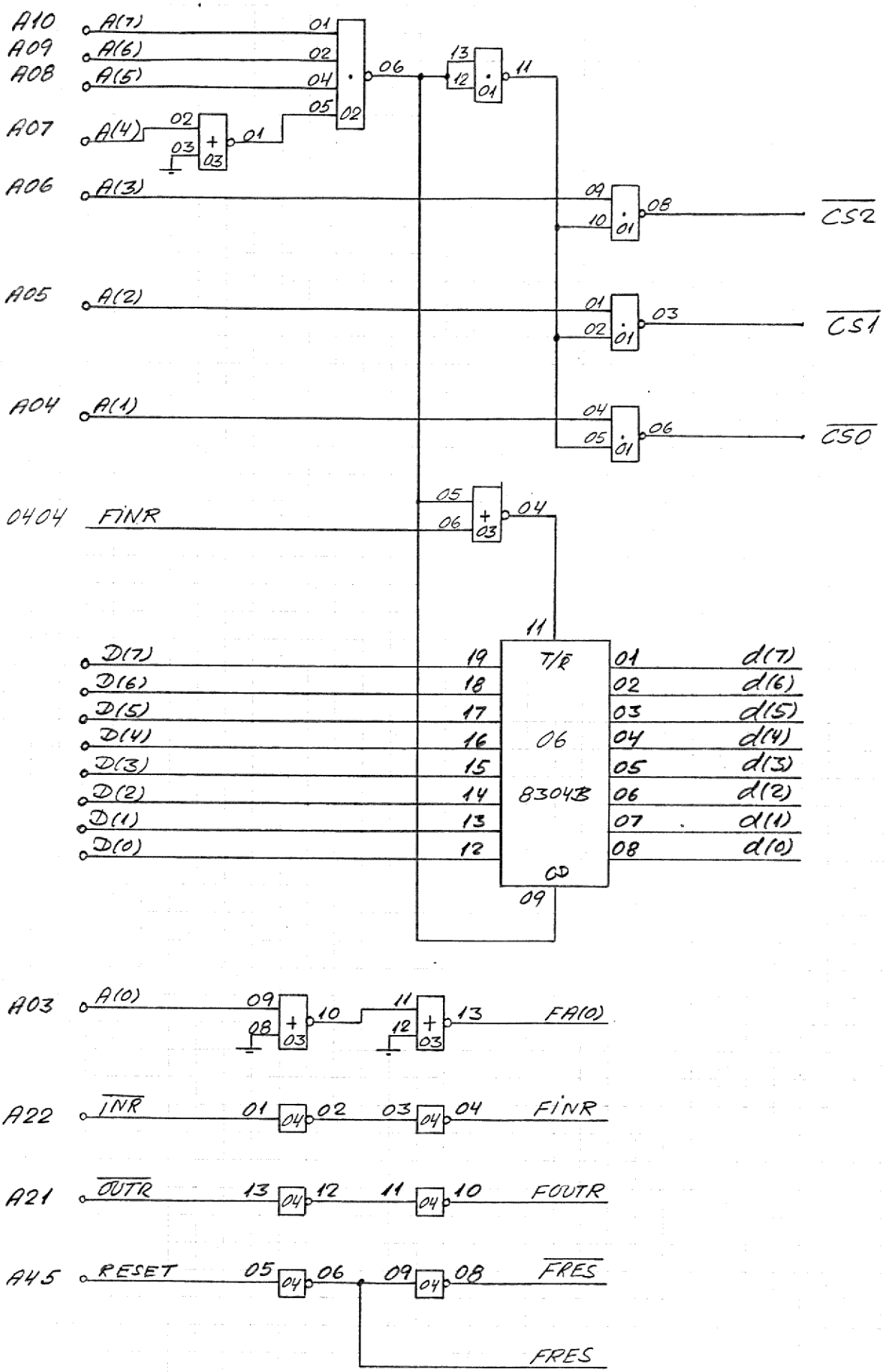

SF2
RF2
CF2
CAS2
ROWEN2
RAS2
OP1
OP3
PU1
FRIA
RR
SLUT2
2108
A23
1902
10
19
11

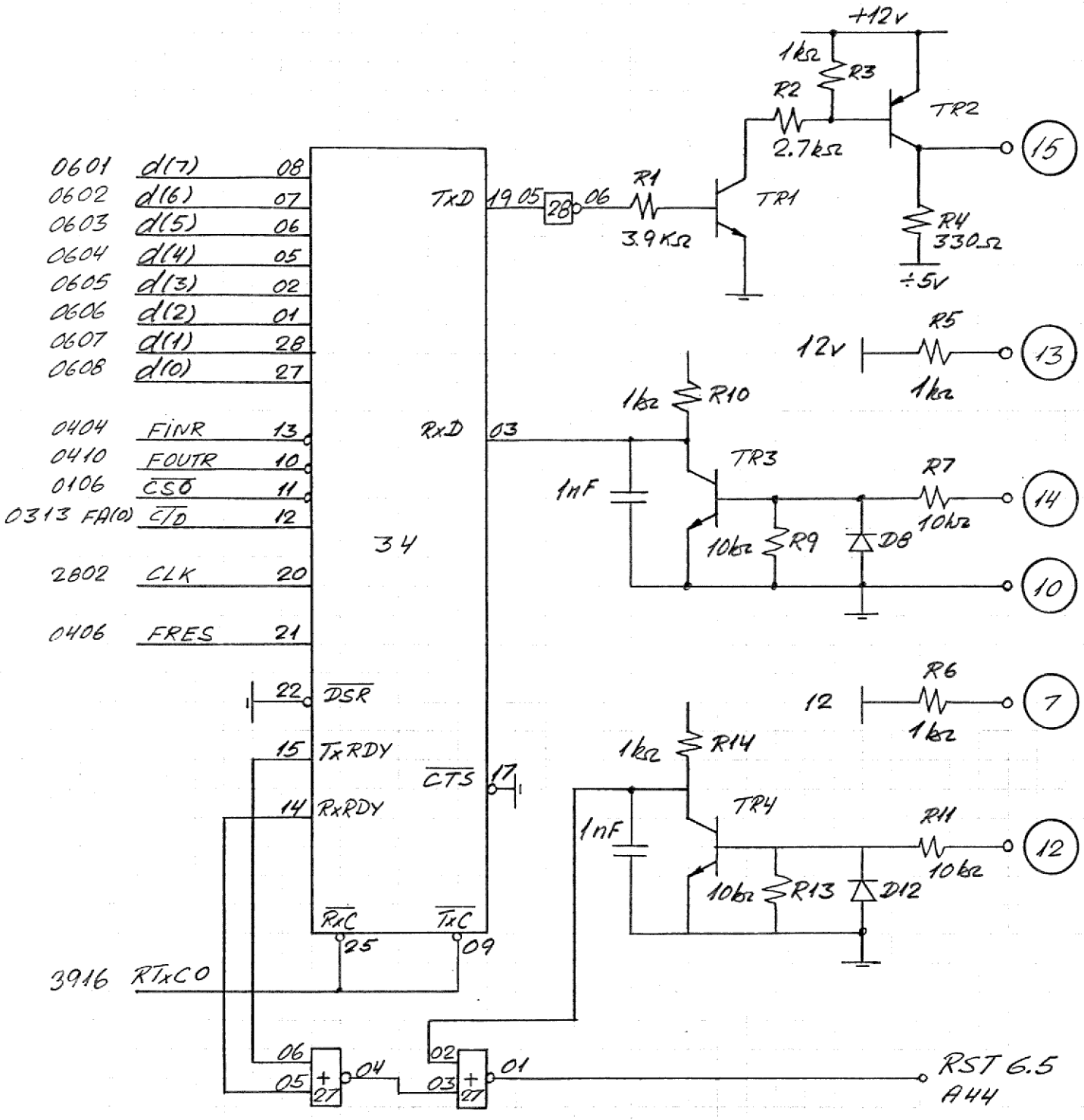

WRITE TIMING
SF3
RF3
CF3
CAS3
WRITE3
ROWEN3
RAS3
OP1
PU4
SP3
FRIA
2108
A20 WR
1902 SLUT2

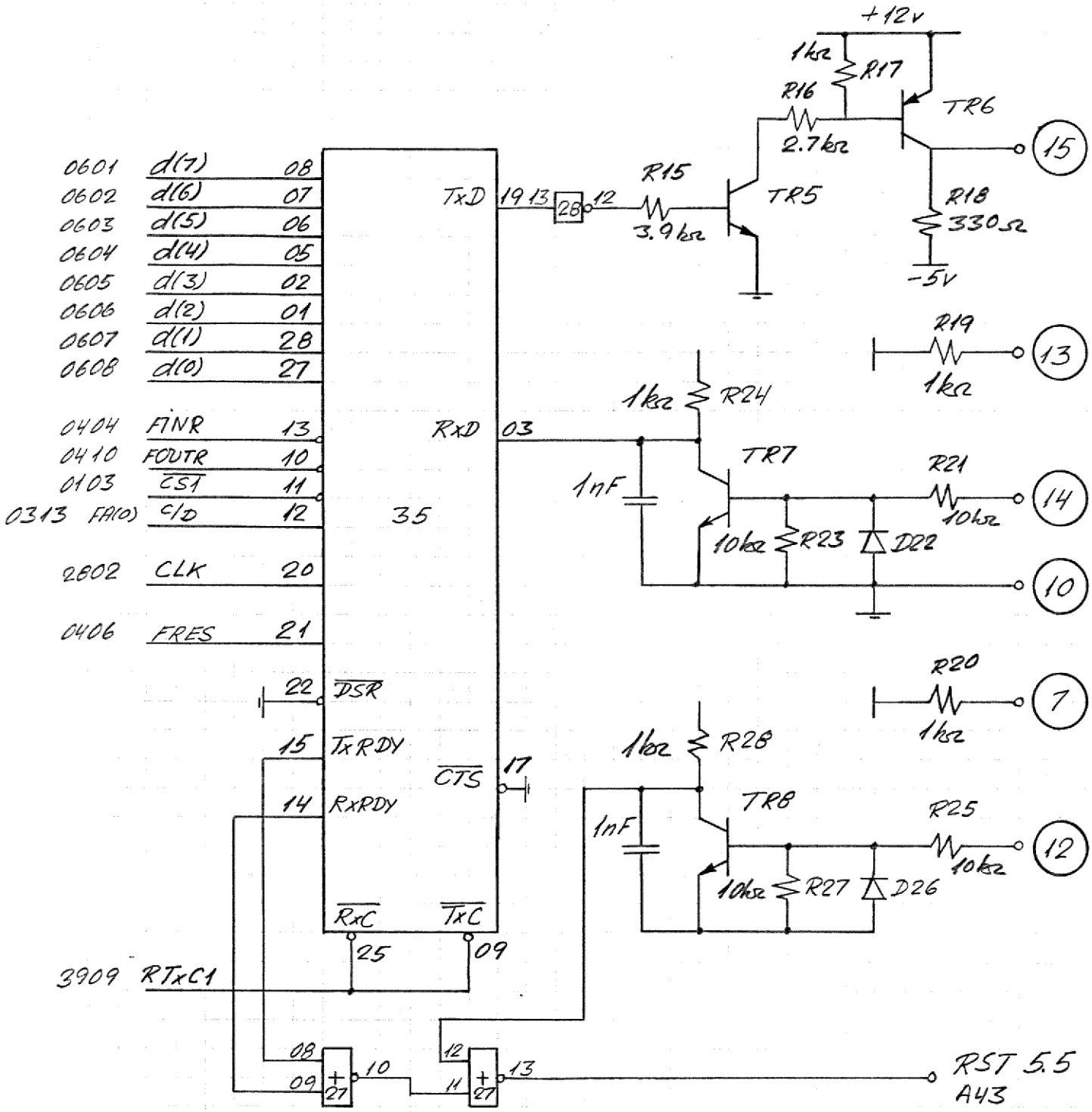

2306 RAS1
1006 RAS2
0903 RAS3
11
10
09
20
08
B19 BRAS
1806 CAS2
1711 CAS3
01
02
07
03
B20 BCAS
1407 REF1
05
06
B21 REF
1703 WRITE3
09
08
B23 WRITE
1603 ROWEN2
1703 ROWEN3
04
05
07
06
B22 ROWEN

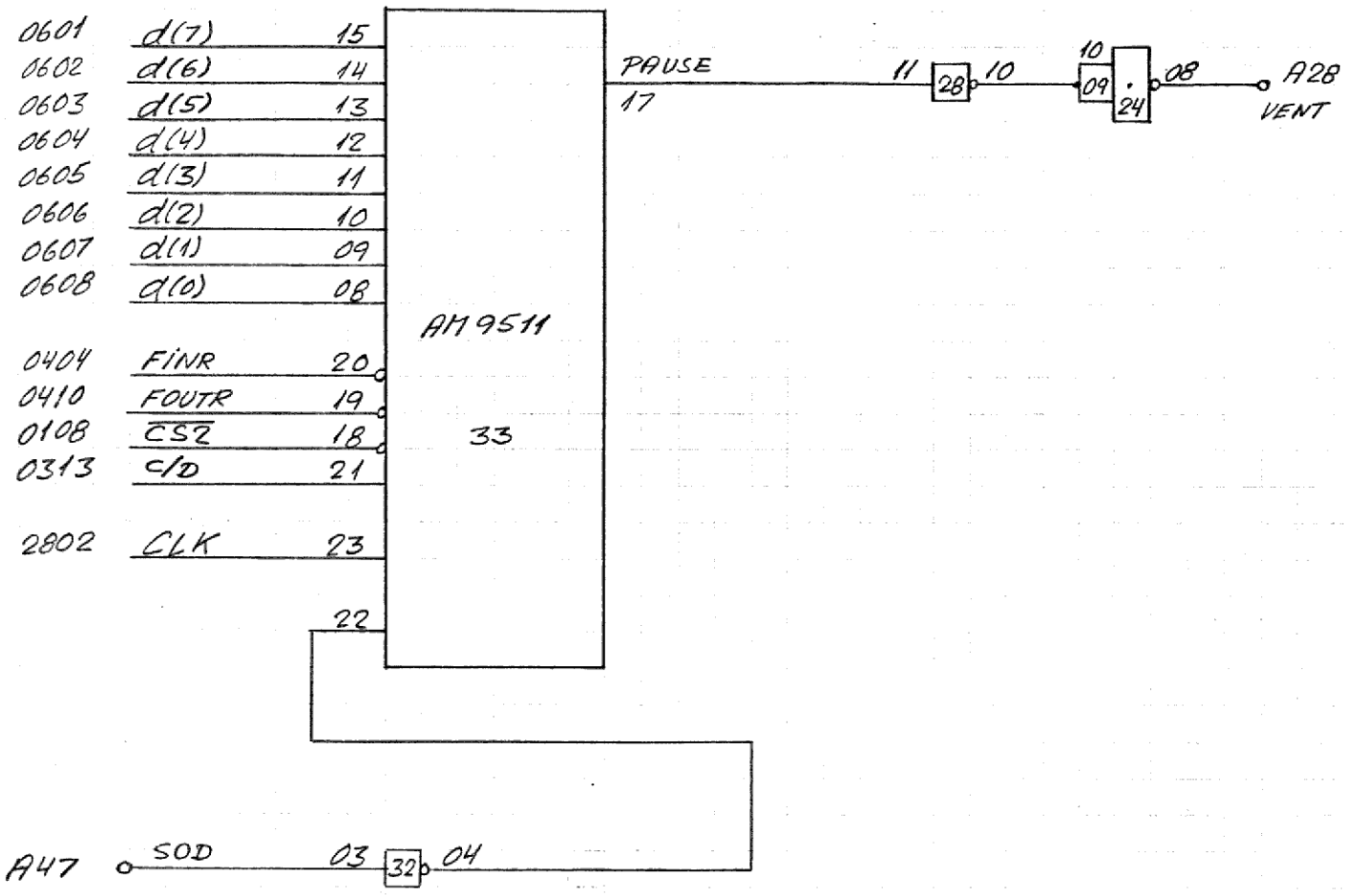

01
02
13
12
11
10
03
04
20MHz
Cp1 pakke: 9, 17, 18, 19
01
02
Cp2 pakke: 15, 22, 23
13
12
11
10
Cp3 pakke: 10, 14

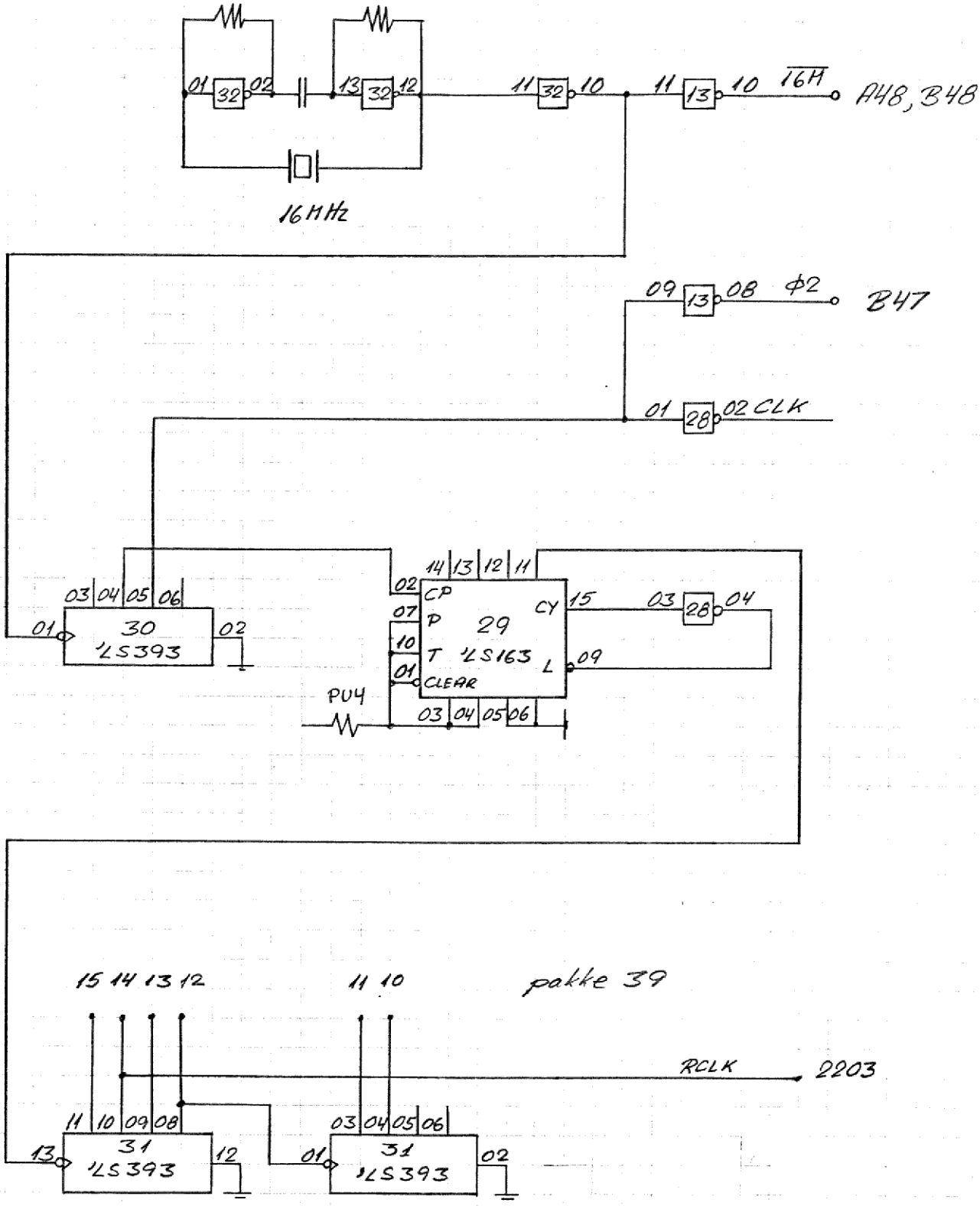

5V
1kΩ
PU1
1kΩ
PU2


A10
A09
A08
A07
A06
A05
A04
0404
A03
A22
A21
A45
A(7)
A(6)
A(5)
A(4)
A(3)
A(2)
A(1)
FINR
A(0)
INR
OUTR
RESET
D(7)
D(6)
D(5)
D(4)
D(3)
D(2)
D(1)
D(0)
T/R
06
8304B
CD
d(7)
d(6)
d(5)
d(4)
d(3)
d(2)
d(1)
d(0)
CS2
CS1
CS0
FA(0)
FINR
FOUTR
FRES
FRES


+12v
1kΩ
R3
R2
2.7kΩ
TR2
15
R1
3.9kΩ
TR1
R4
330Ω
÷5V
TxD
19 05
28
06
0601 d(7) 08
0602 d(6) 07
0603 d(5) 06
0604 d(4) 05
0605 d(3) 02
0606 d(2) 01
0607 d(1) 28
0608 d(0) 27
0404 FINR 13
0410 FOUTR 10
0106 CS0 11
0313 FA(0) C/D 12
2802 CLK 20
0406 FRES 21
34
RxD
03
R5
12v
1kΩ
13
R10
1kΩ
TR3
1nF
R7
10kΩ
14
10kΩ
R9
D8
10
22 DSR
15 TxRDY
14 RxRDY
CTS
17
R6
12
1kΩ
7
R14
1kΩ
TR4
1nF
R11
10kΩ
12
10kΩ
R13
D12
RxC
TxC
25
09
3916 RTxC0
06
05
+
27
04
02
03
+
27
01
RST 6.5
A44


+12v
1kΩ
R17
R16
2.7kΩ
TR6
15
R15
3.9kΩ
TR5
R18
330Ω
-5v
TxD
19 13
28
12
0601 d(7) 08
0602 d(6) 07
0603 d(5) 06
0604 d(4) 05
0605 d(3) 02
0606 d(2) 01
0607 d(1) 28
0608 d(0) 27
0404 FINR 13
0410 FOUTR 10
0103 CS1 11
0313 FA(0) C/D 12
35
2802 CLK 20
0406 FRES 21
RxD 03
R19
1kΩ
13
1kΩ R24
TR7
1nF
R21
10kΩ
14
10kΩ R23
D22
10
22 DSR
15 TxRDY
14 RxRDY
CTS 17
R20
1kΩ
7
1kΩ R28
TR8
1nF
R25
10kΩ
12
10kΩ R27
D26
RxC
TxC
25
09
3909 RTxC1
08
09
÷27
10
12
11
÷27
13
RST 5.5
A43


0601 d(7) 15
0602 d(6) 14
0603 d(5) 13
0604 d(4) 12
0605 d(3) 11
0606 d(2) 10
0607 d(1) 09
0608 d(0) 08
AM 9511
33
0404 FINR 20
0410 FOUTR 19
0108 CS2 18
0313 C/D 21
2802 CLK 23
22
PAUSE
17
11
28
10
10
09
24
08
A28
VENT
A47
SOD
03
32
04


16MHz
A48, B48
B47
02 CLK
30 LS393
29 LS163
CLEAR
PU4
pakke 39
RCLK 2203
31 LS393
31 LS393