DANSK DATA ELEKTRONIK

ID-8530 5 MHZ CPU MODULE

for the

SPC-1 MICROCOMPUTER SYSTEM

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1. DESCRIPTION.

The ID-8530 CPU module is the CPU module in the 5 MHz SPC-1 microcomputer. The CPU module drives the address bus and generates all the necessary control signals. The ID-8530 module works with the other modules in the ID-7000 series. In the SPC-1 it normally works with:

ID-7037:	32 K Dynamic RAM with bank switching.
ID-8538:	5 MHz refresh for the ID-7037 dynamic RAM.
ID-7045:	Floppy disk controller.
ID-7009:	DMA controller.
ID-7003:	Interrupt priority module.
ID-7012:	4 port communication module.
ID-7018:	General purpose I/O module.

The ID-8538 CPU module contains a 8085A-2 microprocessor and the following peripherial units:

A. BOOT LOADER PROM.
B. TIMER.

2. THE 8085A-2 MICROPROCESSOR.

The 8085A-2 is the key component on the CPU module. It drives the address bus and generates all the necessary control signals.

The SOD output signal from the 8085A-2 is used in a special way which is described later.

The odd interrupt levels 5.5 and 6.5 are used by the communication ports on the ID-8538 module while level 7.5 is used by the timer on the CPU module. The odd interrupt level TRAP is used as a DEBUG CALL.

3. BOOT LOADER PROM.

The CPU module contains an UV erasable PROM type 2708. The boot loader PROM is enabled when ADR(15:10)=0 and SOD=0. When the boot loader PROM is enabled the external memory modules are disabled.

During power up the reset signal is generated. This signal resets the CPU and all the modules connected to the SPC-1 bus. After power up SOD equals zero, and the CPU starts reading its first instruction in address zero. As SOD equals zero the instruction is read from the boot loader PROM.

The APU on the ID-8538 module is reset by the SOD signal inverted, so the program in the boot loader PROM cannot use the APU.

It is the responsibility of the boot loader program to reset the APU properly as described in the data sheet and to disable the PROM when the boot loader program has finished.

4. TIMER.

The 8085A-2 is driven by a 10 MHz crystal. The output frequency from 8085A-2 is 5 MHz. This signal is divided down by 8 decimal counters. Several outputs from these counters are connected to a socket position 35 on the module. See figure 1. The odd interrupt input RST 7.5 and the input SID is connected to the same socket. The time interval between interrupts is set in the following way:

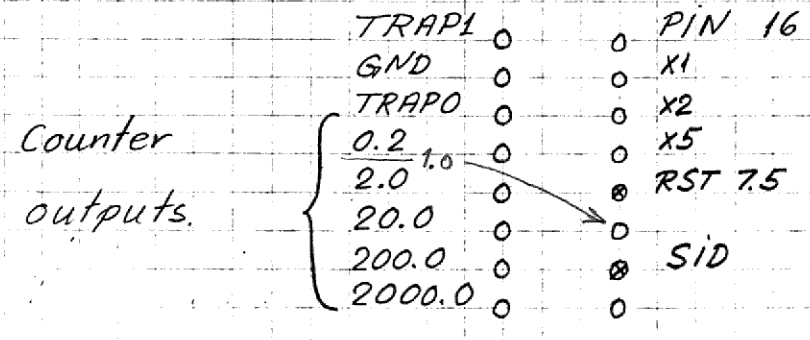
The RST 7.5 input is connected to one of the timer outputs. Pin 16 of the socket is connected to one of the outputs x1, x2, or x5. The time interval between interrupts is the time shown in the figure multiplied by a factor which is 1, 2, or 5, when pin 16 is connected to x1, x2 or x5, respectively.

The SID input can be connected to one of the outputs from the counters. In this way the signal on the SID pin will be a symmetrical square wave with a time period which is equal to the time shown in the figure multiplied by the same factor as used when calculating the time between interrupts. By testing SID which is normally connected to a slow varying counter output it is possible to program a real time clock even if the interrupt system is disabled for a period of time so the program is unable to respond to all timer interrupts.

5. DEBUG CALL.

The odd interrupt level TRAP can be connected to a switch through a debouncing flip flop. When the switch is activated a TRAP interrupt is generated. The CPU stacks its instruction counter and fetches its next instruction from location 24 hex. This location should contain a jump instruction to the debug program. Notice that the TRAP interrupt cannot be disabled so the only reason why a debug call cannot be performed is that the jump instruction in location 24 has been destroyed.

Timer Interrupts

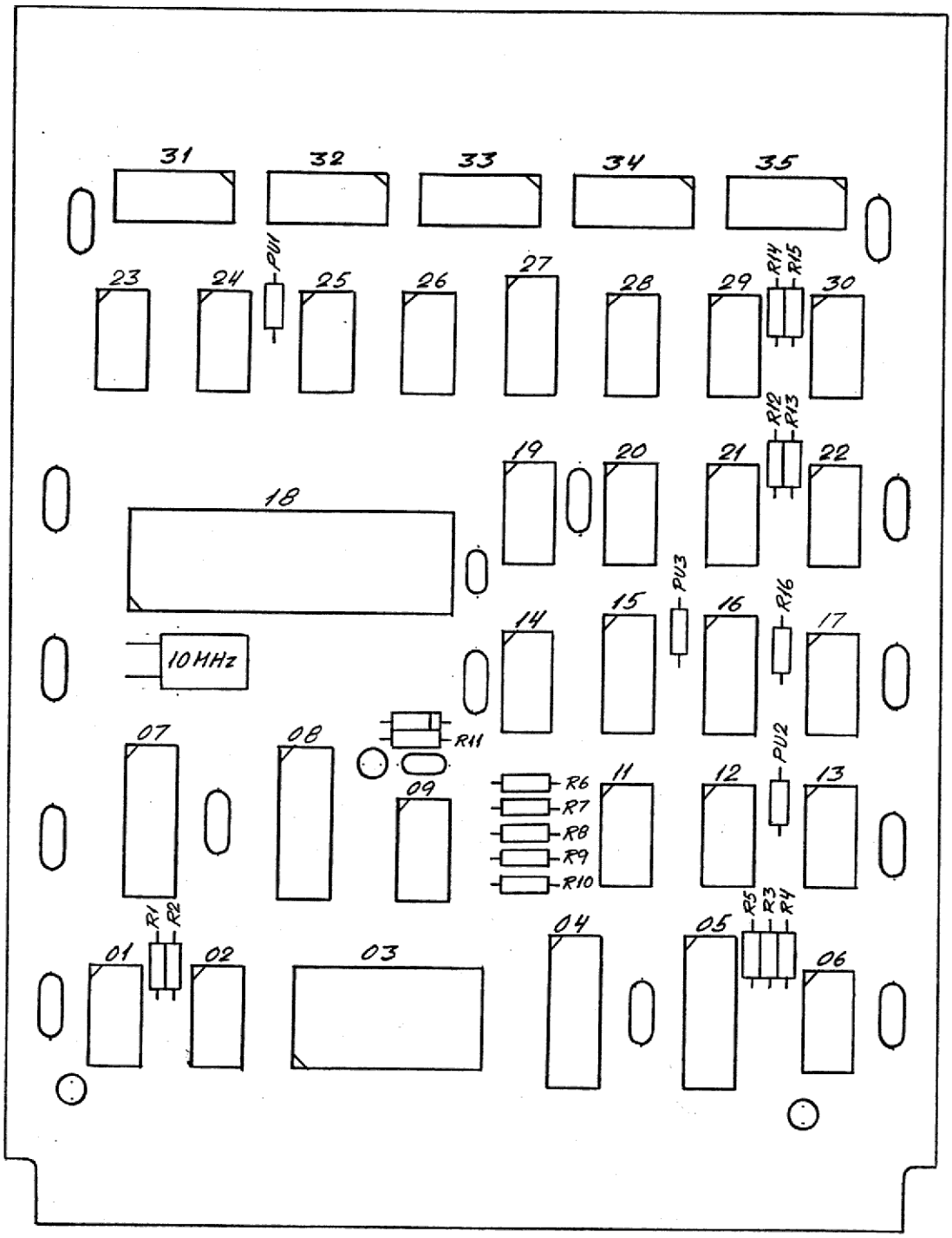


Times measured in ms

* Med 5 MHz krystal skal tiderne ganges med 2.

Figure 1.

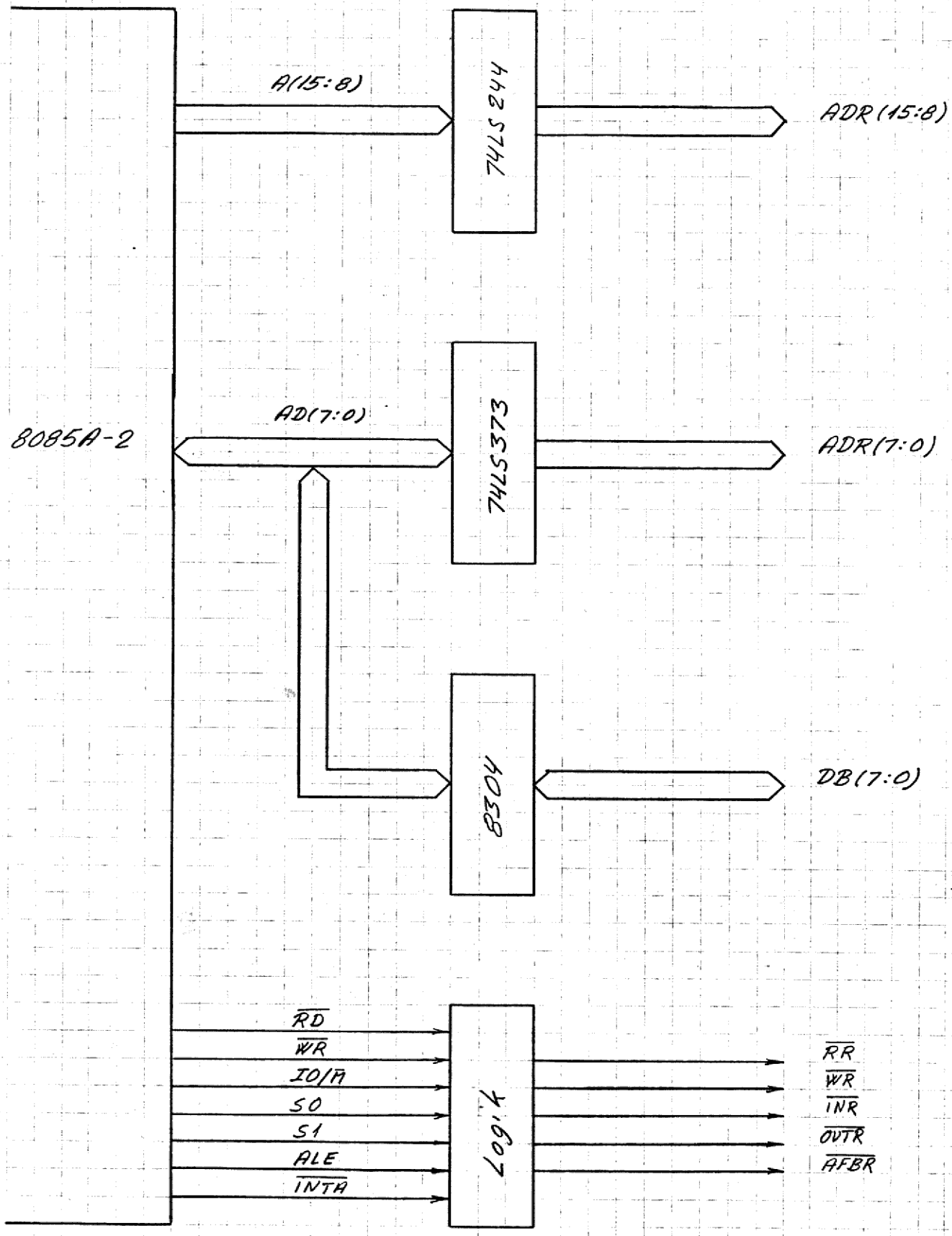
5MHz CPU

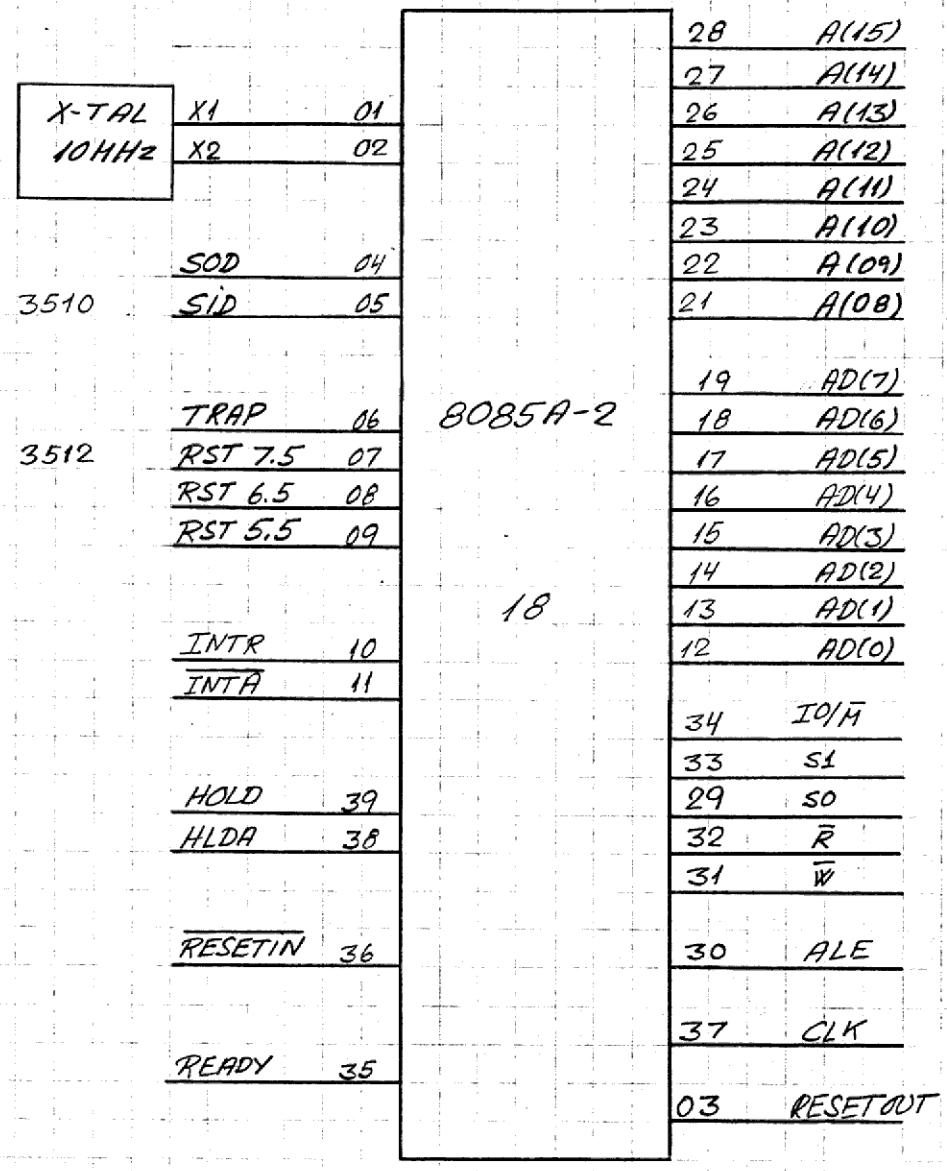

31
32
33
34
35
23
24
PU1
25
26
27
28
29
R14
R15
30
R12
R13
19
20
21
22
18
PU3
15
16
R16
17
14
10MHz
R11
07
08
09
R6
R7
R8
R9
R10
11
12
PU2
13
R1
R2
01
02
03
04
05
R5
R3
R4
06

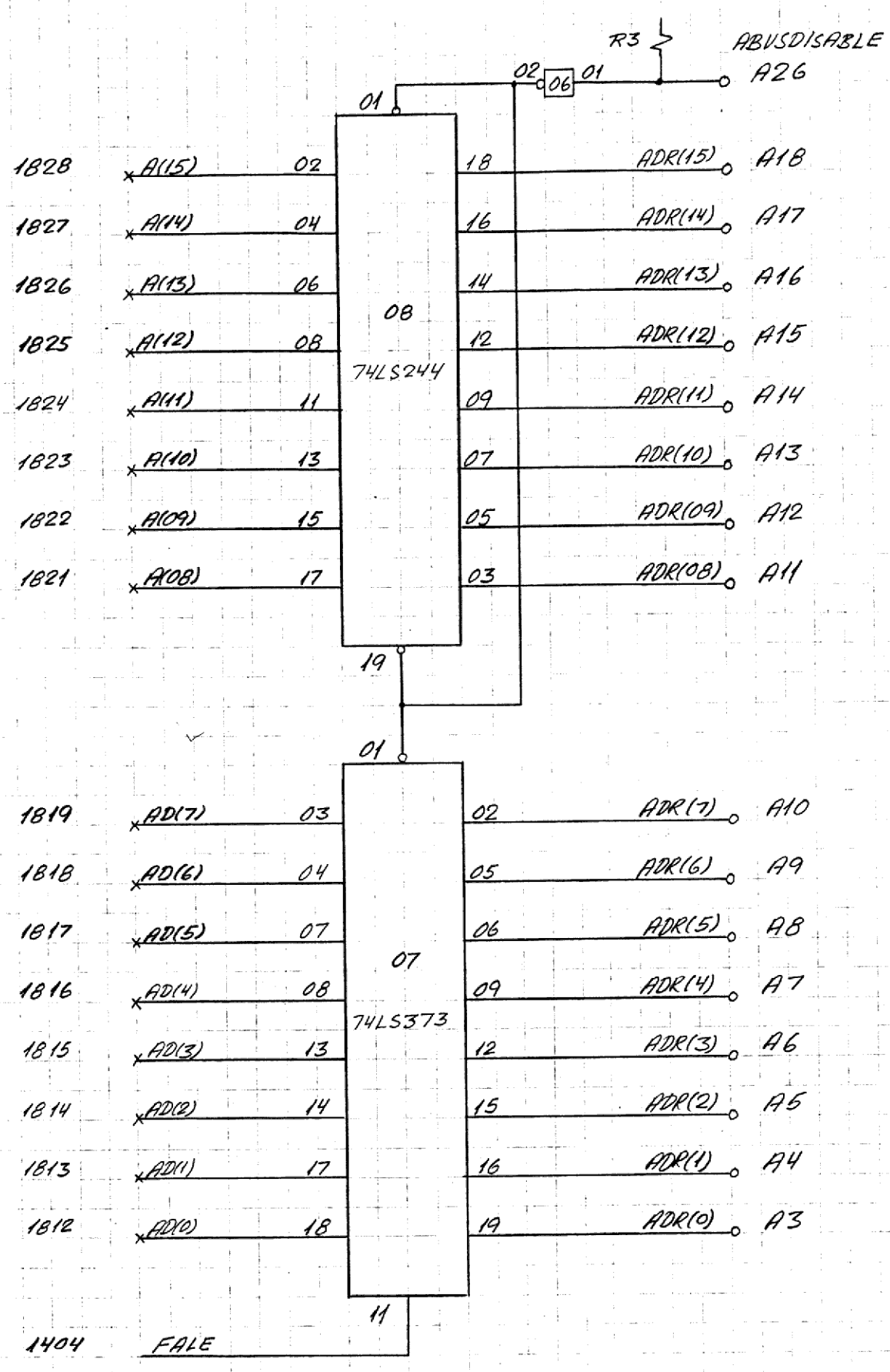
dansk data elektronik aps

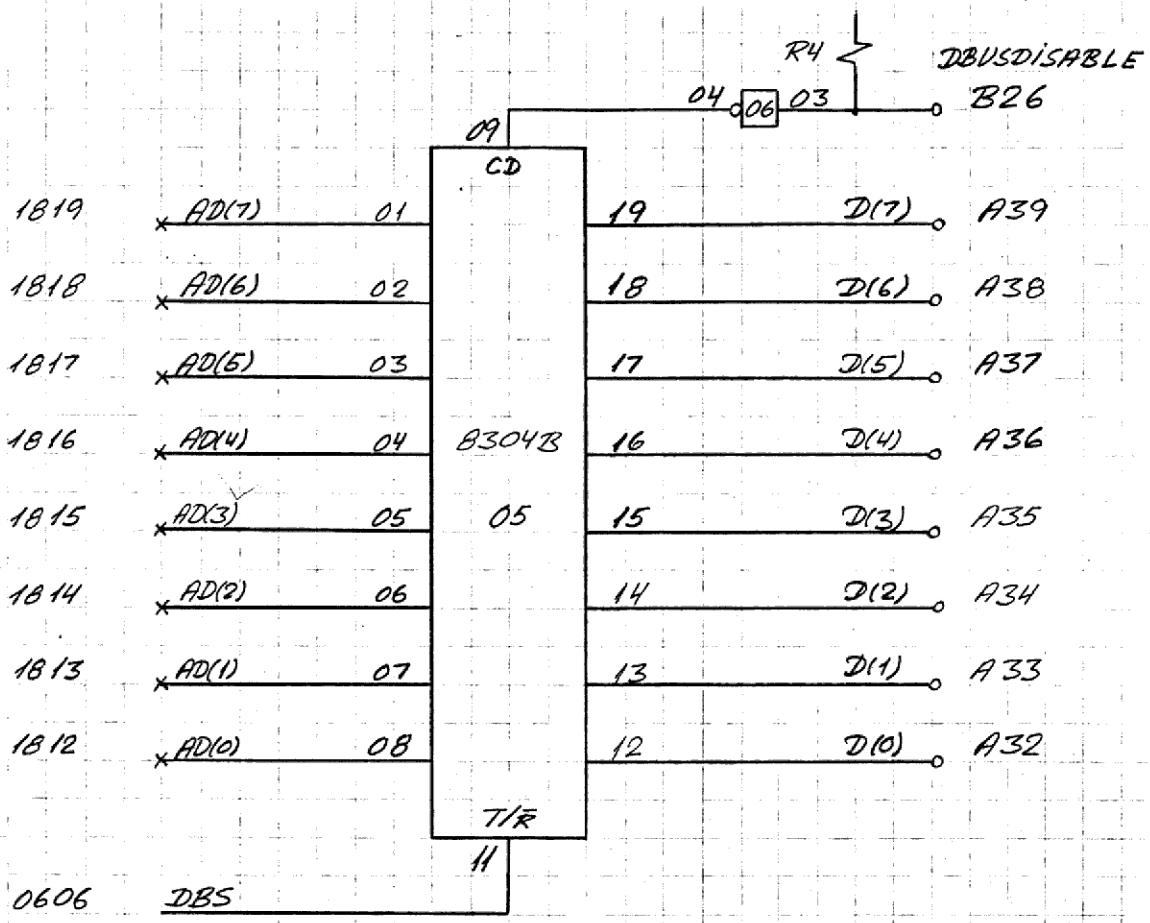
Oversigt

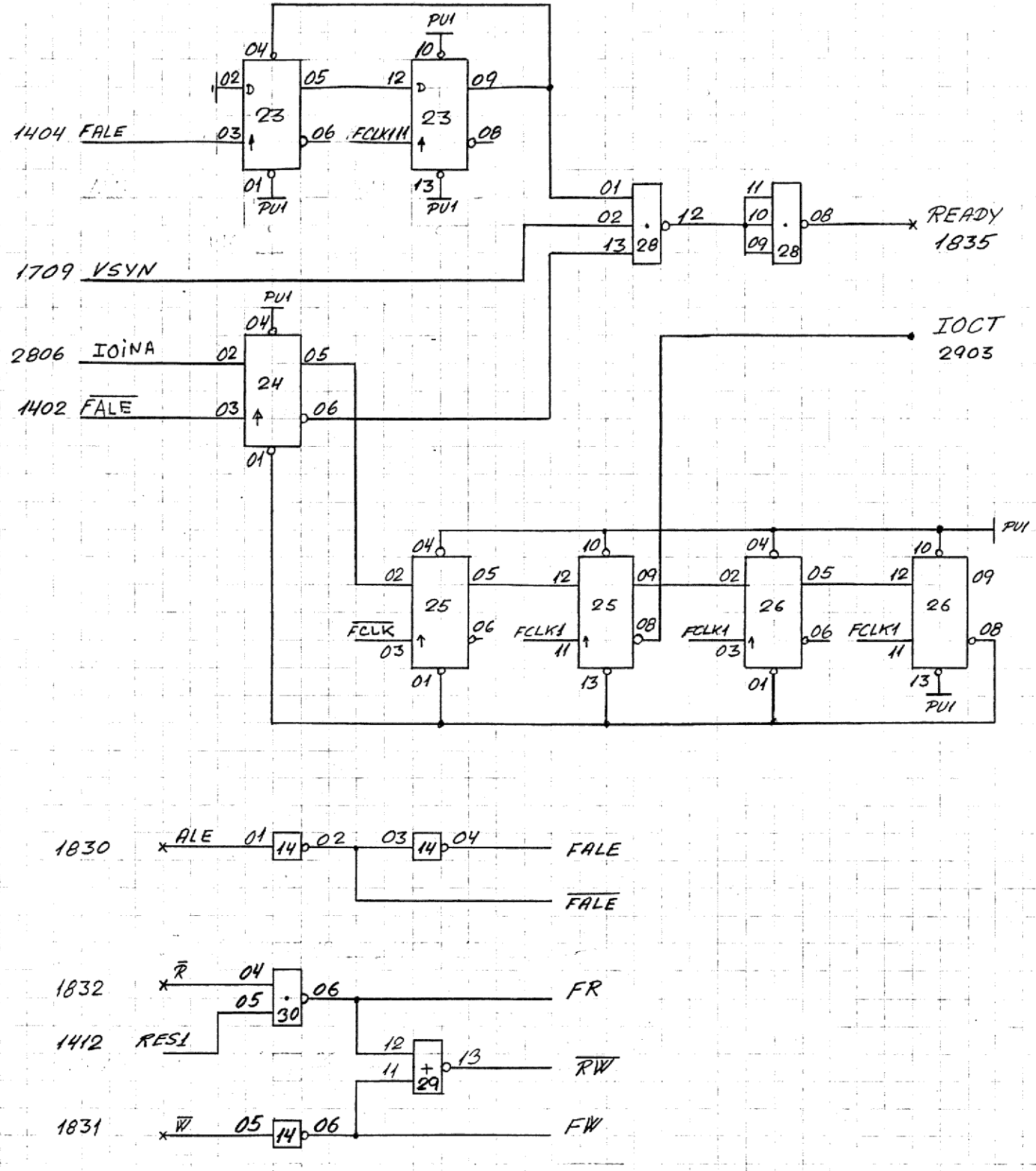
Initialer/dato	Side
KAN 790523	1
Revideret	Projekt 7030-2



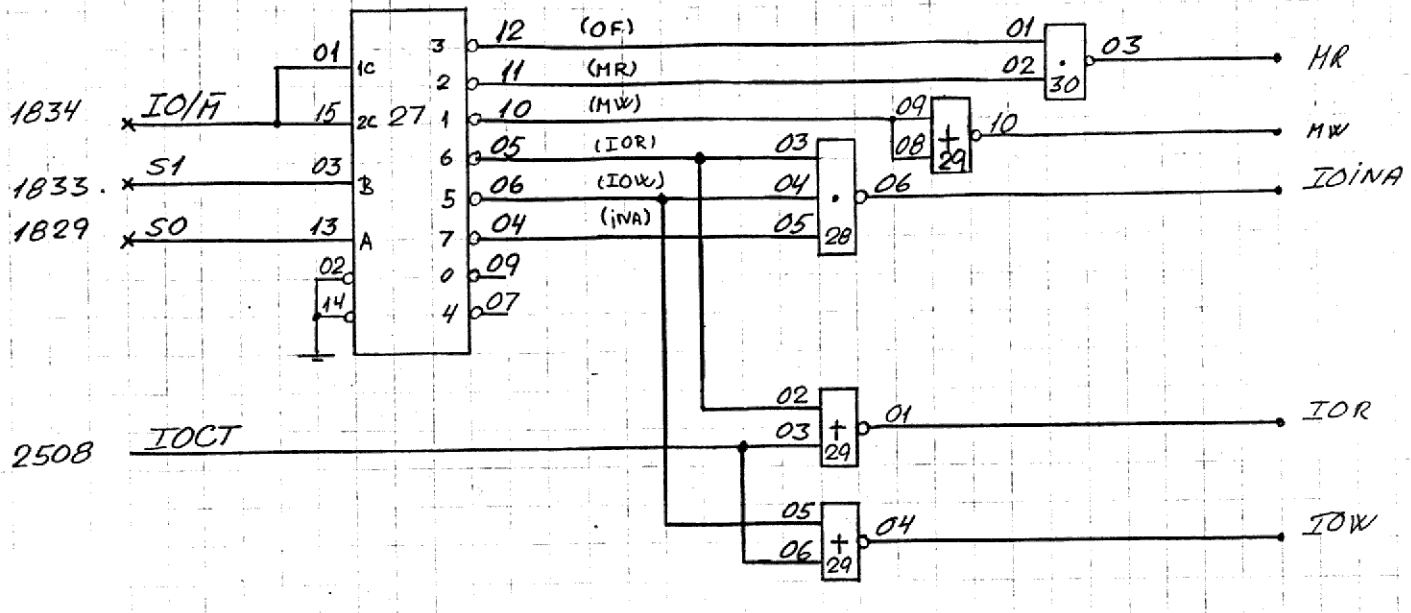

X-TAL
10MHz
X1
X2
01
02
SOD
SID
04
05
3510
TRAP
RST 7.5
RST 6.5
RST 5.5
06
07
08
09
3512
INTR
INTA
10
11
HOLD
HLDA
39
38
RESETIN
36
READY
35
8085A-2
18
28 A(15)
27 A(14)
26 A(13)
25 A(12)
24 A(11)
23 A(10)
22 A(09)
21 A(08)
19 AD(7)
18 AD(6)
17 AD(5)
16 AD(4)
15 AD(3)
14 AD(2)
13 AD(1)
12 AD(0)
34 IO/M
33 S1
29 SO
32 R
31 W
30 ALE
37 CLK
03 RESETOUT

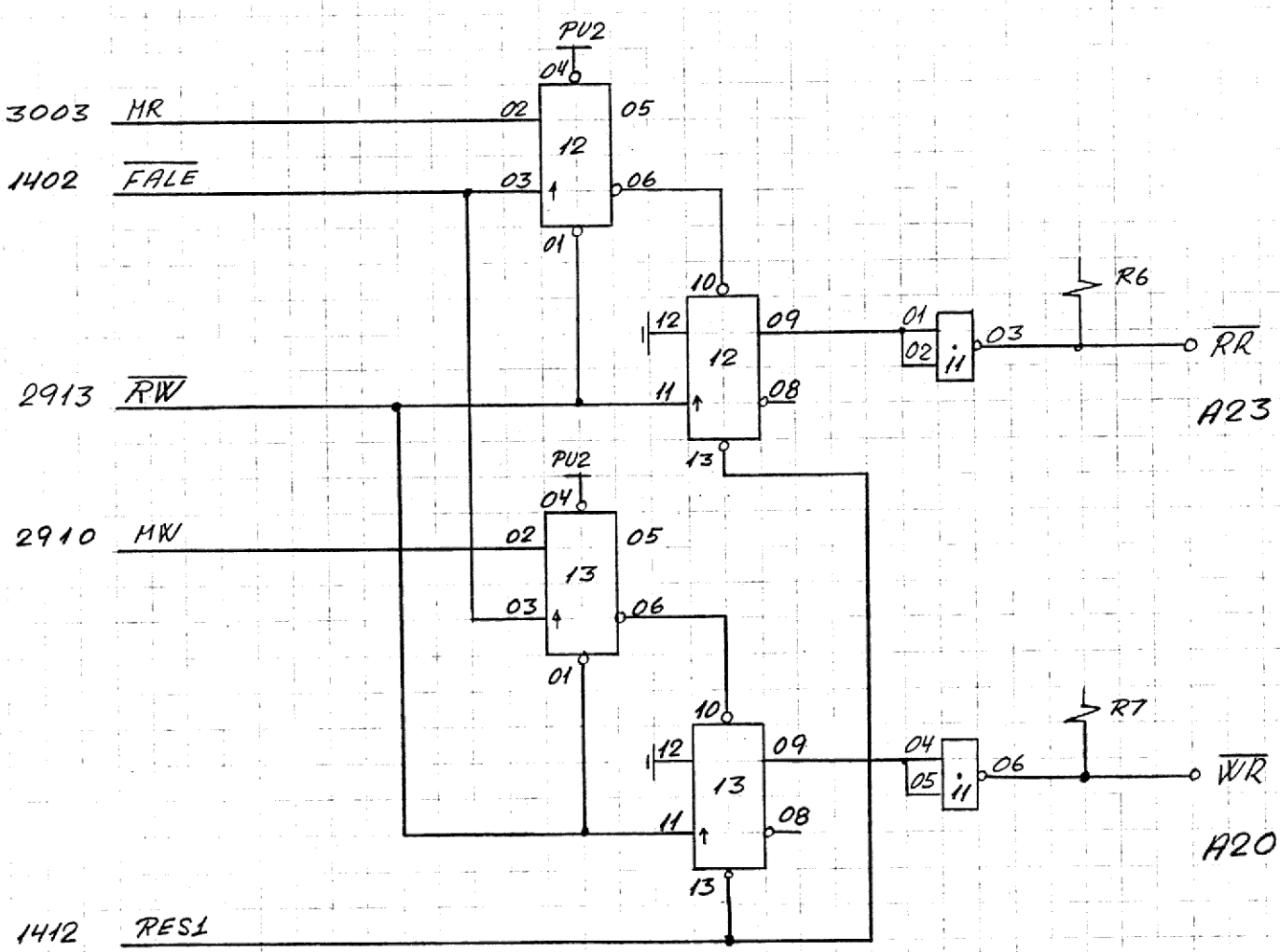

R3
ABUSDISABLE
A26
02
06
01
01
08
74LS244
1828
A(15)
02
18
ADR(15)
A18
1827
A(14)
04
16
ADR(14)
A17
1826
A(13)
06
14
ADR(13)
A16
1825
A(12)
08
12
ADR(12)
A15
1824
A(11)
11
09
ADR(11)
A14
1823
A(10)
13
07
ADR(10)
A13
1822
A(09)
15
05
ADR(09)
A12
1821
A(08)
17
03
ADR(08)
A11
19
01
07
74LS373
1819
AD(7)
03
02
ADR(7)
A10
1818
AD(6)
04
05
ADR(6)
A9
1817
AD(5)
07
06
ADR(5)
A8
1816
AD(4)
08
09
ADR(4)
A7
1815
AD(3)
13
12
ADR(3)
A6
1814
AD(2)
14
15
ADR(2)
A5
1813
AD(1)
17
16
ADR(1)
A4
1812
AD(0)
18
19
ADR(0)
A3
11
1404
FALE

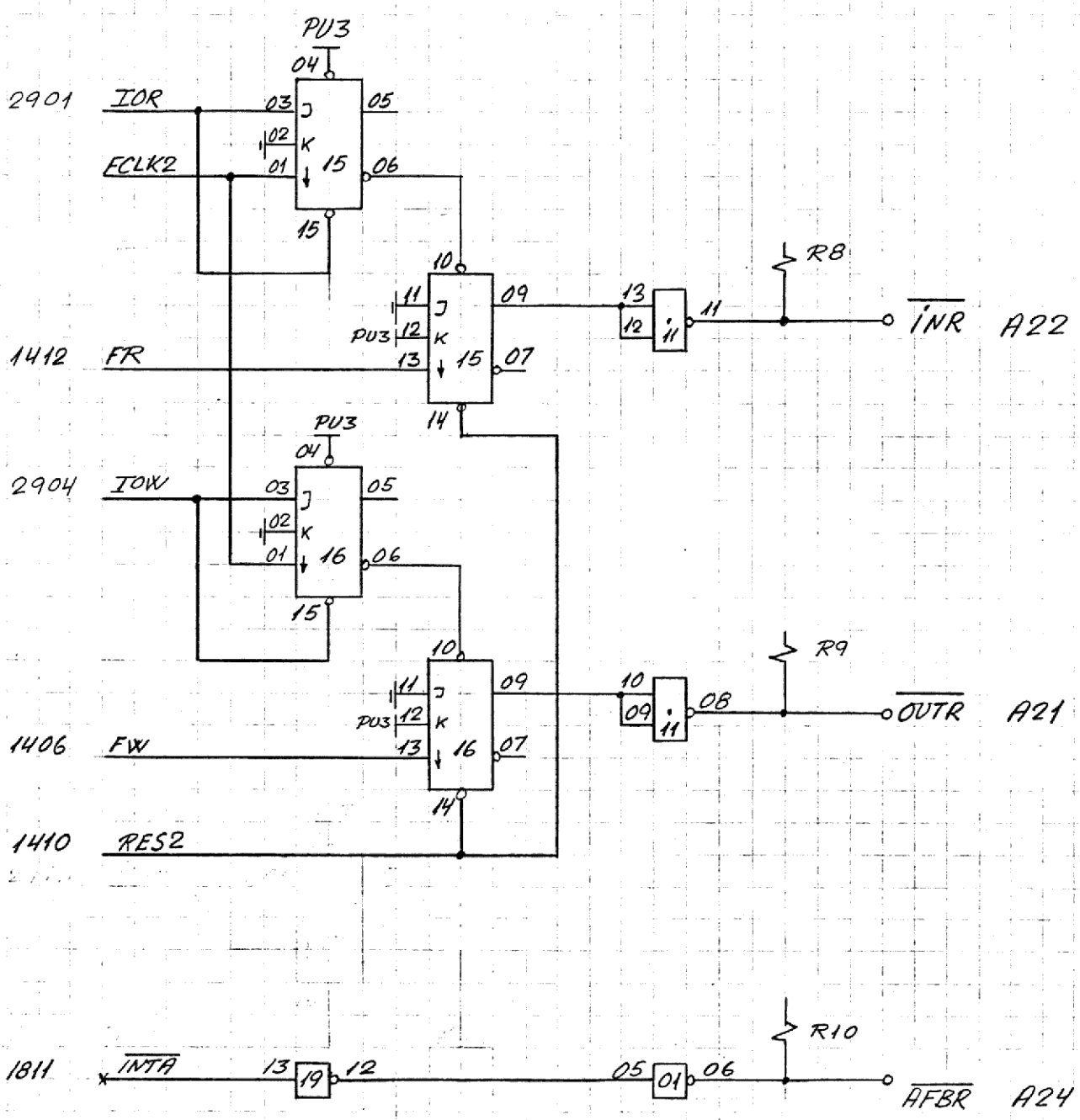

R4
DBUSDISABLE
04
06
03
B26
09
CD
1819
AD(7)
01
19
D(7)
A39
1818
AD(6)
02
18
D(6)
A38
1817
AD(5)
03
17
D(5)
A37
1816
AD(4)
04
8304B
16
D(4)
A36
1815
AD(3)
05
05
15
D(3)
A35
1814
AD(2)
06
14
D(2)
A34
1813
AD(1)
07
13
D(1)
A33
1812
AD(0)
08
12
D(0)
A32
T/R
11
0606
DBS

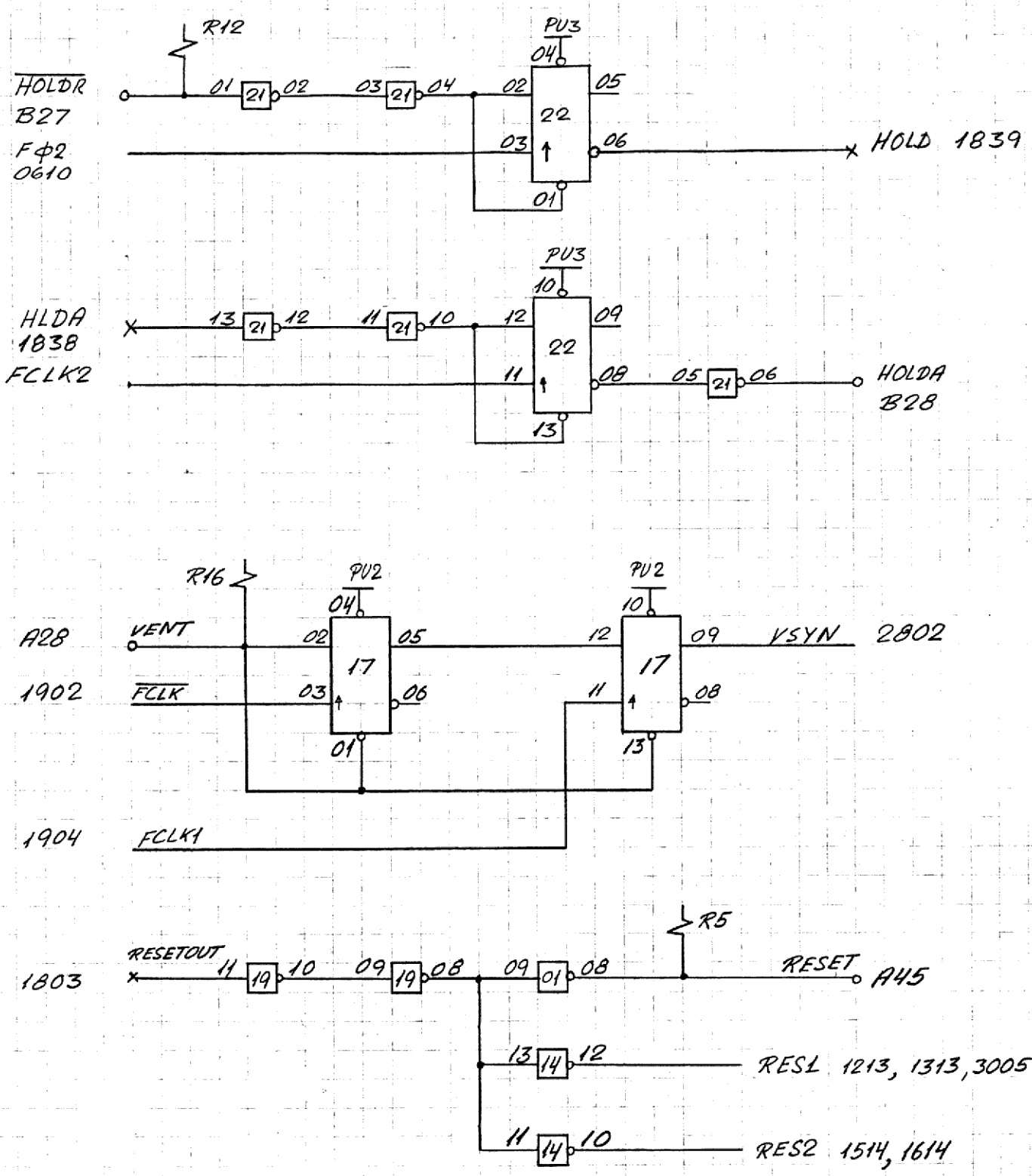

1404 FALE
1709 VSYN
2806 IOINA
1402 FALE
FCLK111
PU1
READY 1835
IOCT 2903
FCLK
FCLK1
23
24
25
26
28
30

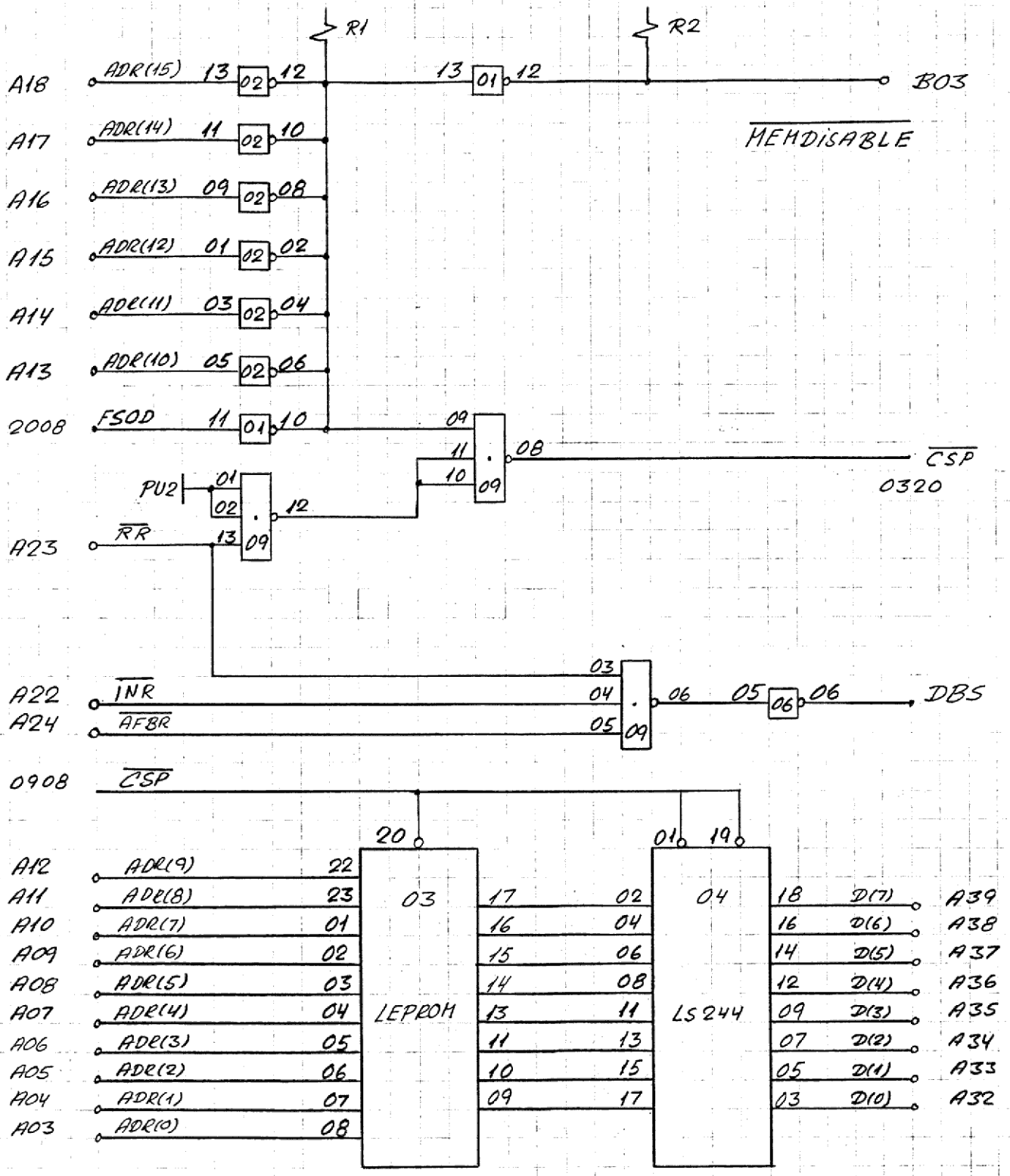
1830
ALE
FALE
FALE
1832
R
FR
1412
RESI
RW
1831
W
FW
14
29
30

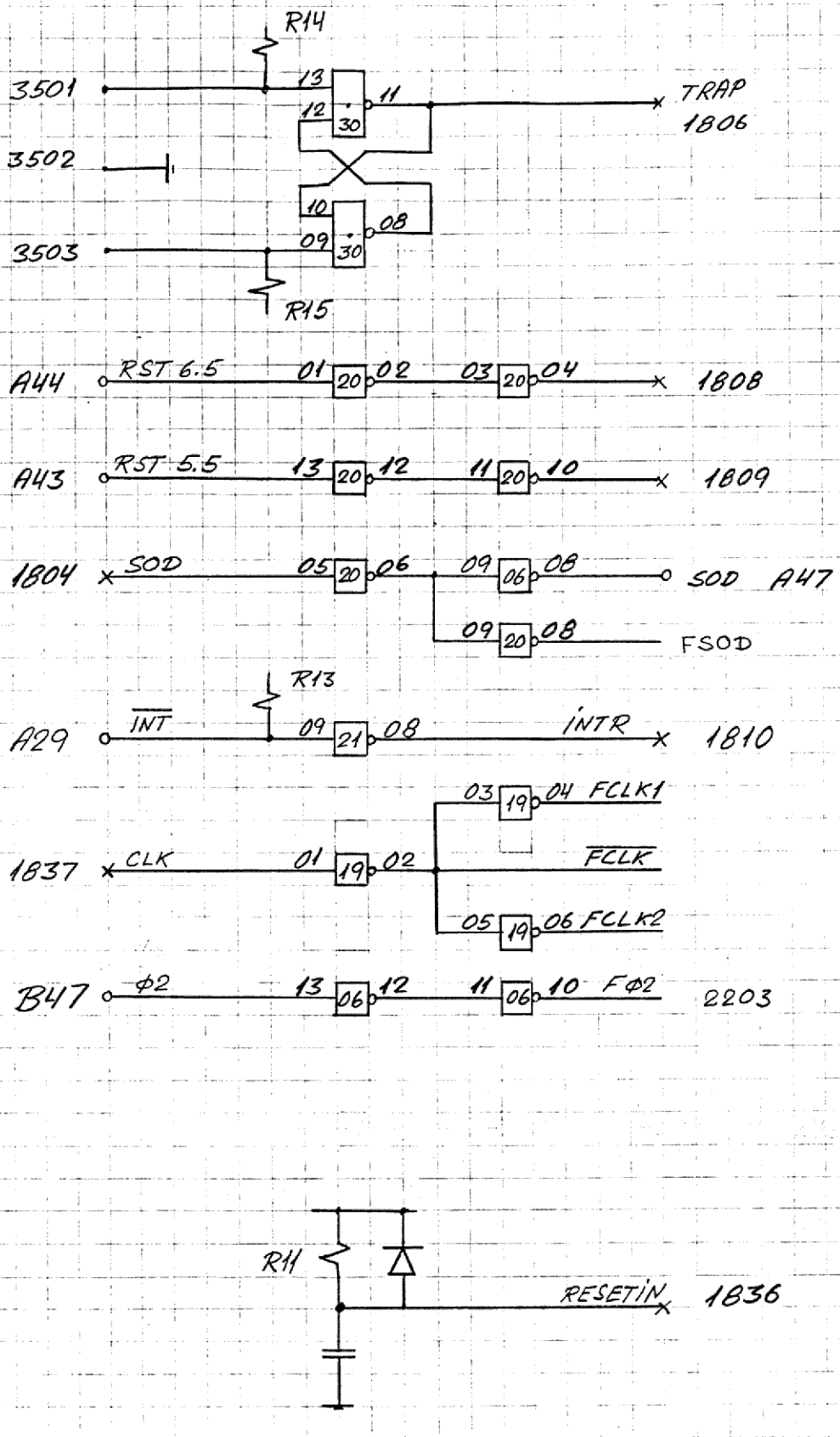

1834 IO/M
1833. S1
1829 S0
2508 IOCT
27
(OF)
(MR)
(MW)
(IOR)
(IOW)
(INA)
28
29
30
MR
MW
IOINA
IOR
IOW

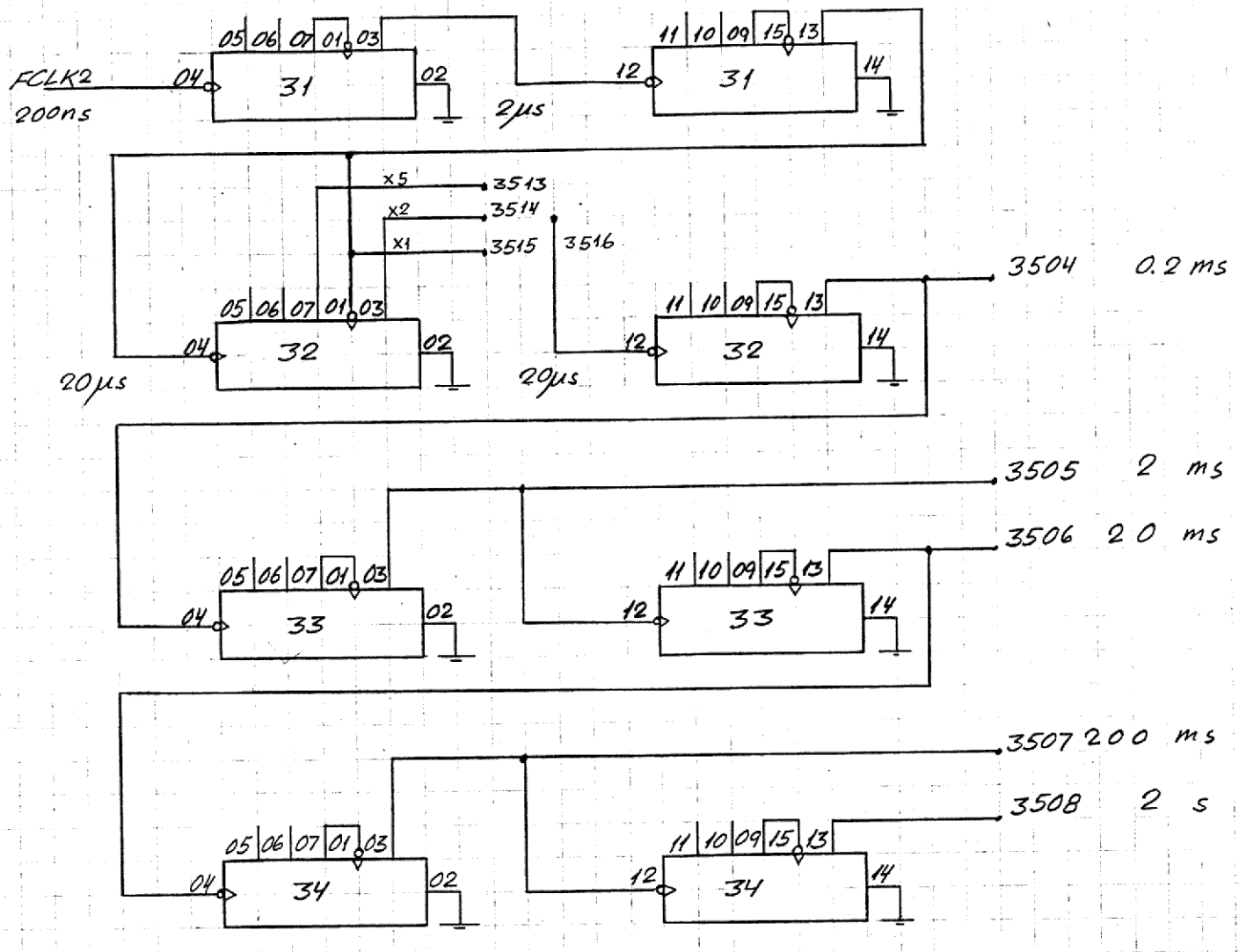

3003 MR
1402 FALE
2913 RW
2910 MW
1412 RES1
PU2
12
13
11
R6
R7
RR
WR
A23
A20

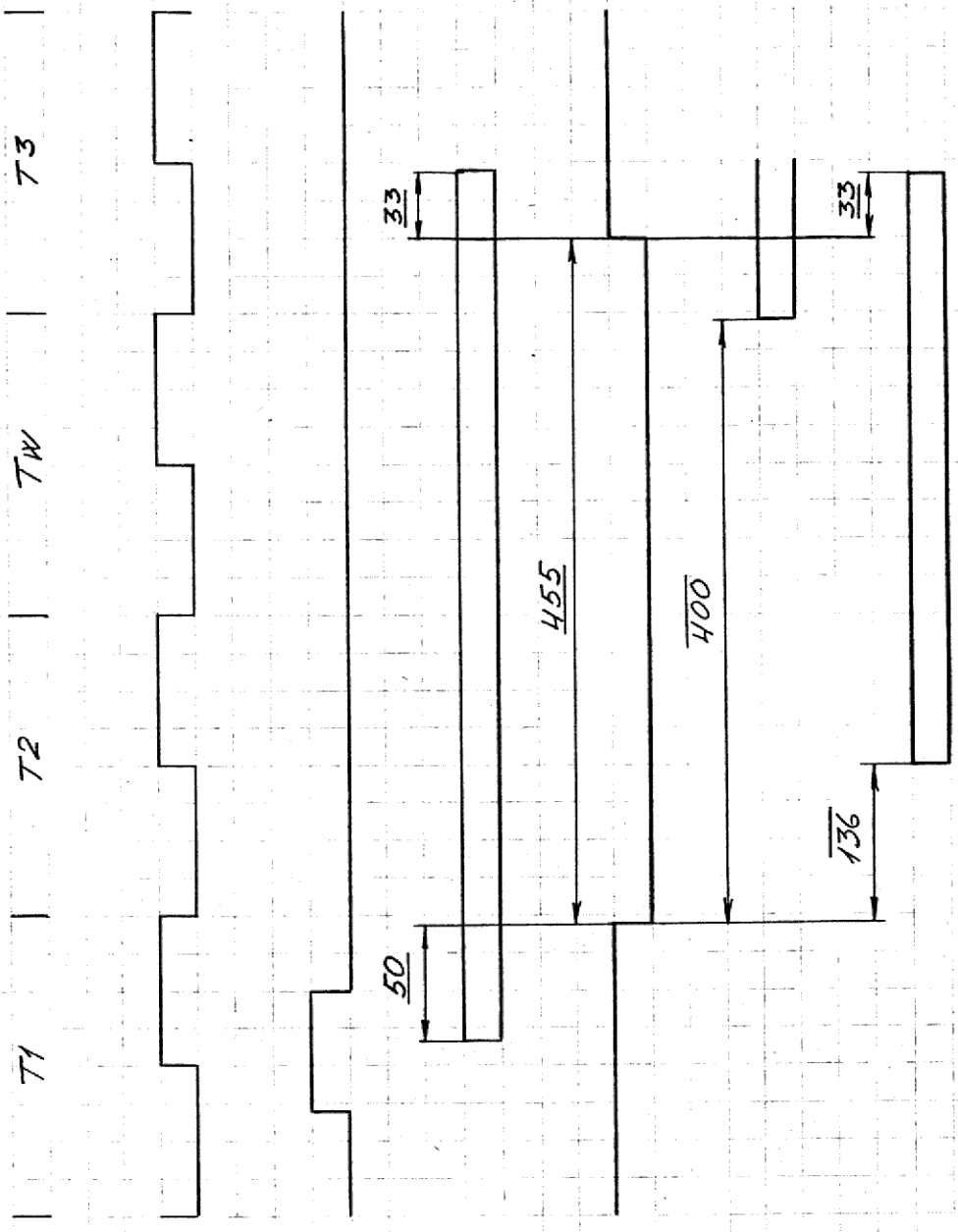

PU3
2901
IOR
FCLK2
03
02
01
05
06
15
J
K
1412
FR
10
11
12
13
09
07
PU3
R8
INR
A22
2904
IOW
16
1406
FW
1410
RES2
R9
OUTR
A21
1811
INTA
19
12
05
01
R10
AFBR
A24

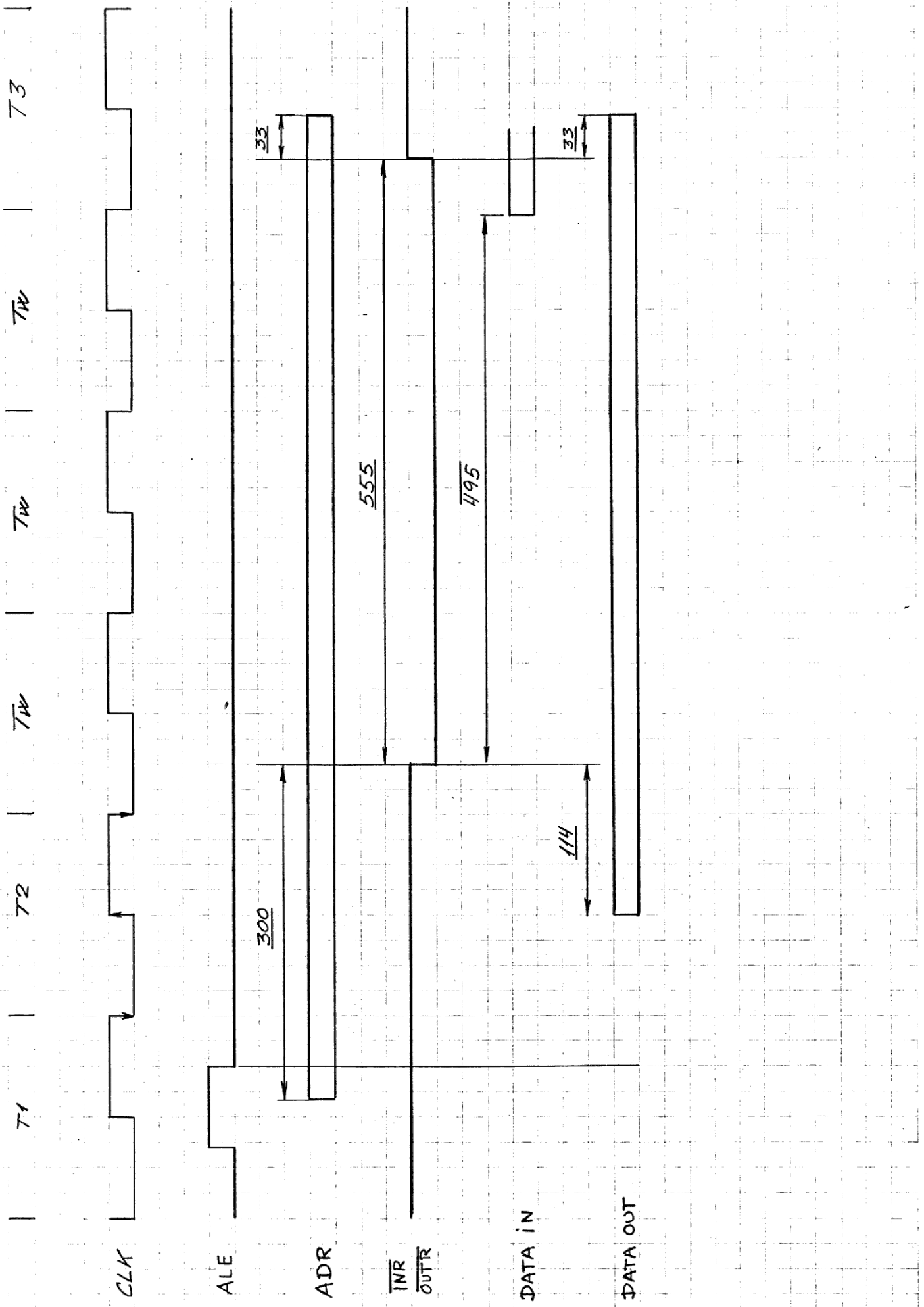

R12
PU3
HOLDR
B27
FΦ2
0610
HOLD 1839
HLDA
1838
FCLK2
HOLDA
B28
R16
PU2
A28
VENT
VSYN
2802
1902
FCLK
1904
FCLK1
R5
1803
RESETOUT
RESET
A45
RES1 1213, 1313, 3005
RES2 1514, 1614


R1
R2
A18
ADR(15)
13
02
12
13
01
12
B03
A17
ADR(14)
11
02
10
MEMDISABLE
A16
ADR(13)
09
02
08
A15
ADR(12)
01
02
02
A14
ADR(11)
03
02
04
A13
ADR(10)
05
02
06
2008
FSOD
11
01
10
09
11
10
08
CSP
0320
PU2
01
02
12
A23
RR
13
09
A22
INR
A24
AFBR
03
04
05
06
05
06
06
DBS
0908
CSP
20
01
19
A12
ADR(9)
22
A11
ADR(8)
23
A10
ADR(7)
01
A09
ADR(6)
02
A08
ADR(5)
03
A07
ADR(4)
04
A06
ADR(3)
05
A05
ADR(2)
06
A04
ADR(1)
07
A03
ADR(0)
08
03
LEPROM
17
16
15
14
13
11
10
09
02
04
06
08
11
13
15
17
04
LS244
18
16
14
12
09
07
05
03
D(7)
D(6)
D(5)
D(4)
D(3)
D(2)
D(1)
D(0)
A39
A38
A37
A36
A35
A34
A33
A32


R14
3501
13
12
30
11
TRAP
1806
3502
10
09
30
08
3503
R15
A44
RST 6.5
01
20
02
03
20
04
1808
A43
RST 5.5
13
20
12
11
20
10
1809
1804
SOD
05
20
06
09
06
08
SOD A47
09
20
08
FSOD
R13
A29
INT
09
21
08
INTR
1810
03
19
04 FCLK1
1837
CLK
01
19
02
FCLK
05
19
06 FCLK2
B47
Φ2
13
06
12
11
06
10 FΦ2
2203
R11
RESETIN
1836


FCLK2
200ns
05 06 07 01 03
04
31
02
2µs
11 10 09 15 13
12
31
14
x5
x2
x1
3513
3514
3515
3516
3504 0.2 ms
20µs
32
20µs
3505 2 ms
3506 20 ms
33
3507 200 ms
3508 2 s
34


T1
T2
TW
T3
CLK
ALE
ADR
RR, WR
DATA IN
DATA OUT
33
33
455
400
136
50


T1
T2
Tw
Tw
Tw
T3
CLK
ALE
ADR
INR
OUTR
DATA IN
DATA OUT
33
33
555
1195
300
114

SPC-1 BUS SYSTEM.

SOLDER SIDE SIDE A	PIN NO.	COMPONENT SIDE SIDE B
+5V	1	GND
-5V	2	GND
ADR(0)	3	MEMDISABLE
ADR(1)	4	---
ADR(2)	5	---
ADR(3)	6	---
ADR(4)	7	ANALOG GROUND
ADR(5)	8	+15V ANALOG SUPPLY
ADR(6)	9	-15V ANALOG SUPPLY
ADR(7)	10	±12V
ADR(8)	11	IR(0)
ADR(9)	12	IR(1)
ADR(10)	13	IR(2)
ADR(11)	14	IR(3)
ADR(12)	15	IR(4)
ADR(13)	16	IR(5)
ADR(14)	17	IR(6)
ADR(15)	18	IR(7)
---	19	BRAS
WR	20	BCAS
OUTR	21	REF
INR	22	ROWEN
RR	23	WRITE
AFBR	24	EOPIN
---	25	EOPOUT

SPC-1 BUS SYSTEM.

SOLDER SIDE SIDE A	PIN NO.	COMPONENT SIDE SIDE B
$\overline{\text{ABUSDISABLE}}$	26	$\overline{\text{DBUSDISABLE}}$
---	27	$\overline{\text{HOLDR}}$
$\overline{\text{VENT}}$	28	HOLDA
$\overline{\text{INT}}$	29	$\overline{\text{DMAACK(0)}}$
---	30	$\overline{\text{DMAACK(1)}}$
---	31	$\overline{\text{DMAACK(2)}}$
D(0)	32	$\overline{\text{DMAACK(3)}}$
D(1)	33	$\overline{\text{DMAACK(4)}}$
D(2)	34	$\overline{\text{DMAACK(5)}}$
D(3)	35	$\overline{\text{DMAACK(6)}}$
D(4)	36	$\overline{\text{DMAACK(7)}}$
D(5)	37	$\overline{\text{DMAREQ(0)}}$
D(6)	38	$\overline{\text{DMAREQ(1)}}$
D(7)	39	$\overline{\text{DMAREQ(2)}}$
$\overline{\text{OUTDMA}}$	40	$\overline{\text{DMAREQ(3)}}$
$\overline{\text{INDMA}}$	41	$\overline{\text{DMAREQ(4)}}$
---	42	$\overline{\text{DMAREQ(5)}}$
RST 5.5	43	$\overline{\text{DMAREQ(6)}}$
RST 6.5	44	$\overline{\text{DMAREQ(7)}}$
$\overline{\text{RESET}}$	45	---
---	46	---
SOD	47	$\emptyset 2$
16M	48	16M
GND	49	+12V
GND	50	+5V