TITLE: MULTI PURPOSE MULTI PROCESSOR BOARD MPMP

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MULTI PURPOSE MULTI PROCESSOR BOARD
MPMP PRODUCT SPECIFICATION

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PAGE RECORD AND ISSUE LOG.

PAGE	ISSUE							
	1	2	3	4	5	6	7	8
01								
02								
03								
04								
05								
06								
07								
08								
09.								
10								
11								
12								
13								
14								
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16								
17								
18								
19								
20								
21								
22								
23								
24								
25								
26								
27								
28								
29								
30								
31								
32								
33								

PAGE	ISSUE							
	1	2	3	4	5	6	7	8
34								
35								
36								
37								
38								
39								
40								
41								
42								
43								
44								
45								
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53								
54								
55								
56								
57								
58								
59								
60								
61								
62								
63								
64								
65								
66								

PAGE	ISSUE							
	1	2	3	4	5	6	7	8
67								
68								
69								
70								
71								
72								
73								
74								
75								
76								
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98								
99								
100								

ISSUE	DATE	PREPARED BY	APPROVED BY	AUTHORIZED BY
1	810130	HSH/TK HSH	TK	TK
2	810501	HSH/TK HSH	TK	TK
3	820219	HSH		

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Table of content

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MULTI PURPOSE MULTI PROCESSOR BOARD MPMP PRODUCT SPECIFICATION	sion/date HSH/820219	page 1
	replace TK/810501	project

Scope

The scope of this document is to specify the interface characteristics of the Multi Purpose Multi Processor Board ($(MP)^2$) which is a general microcomputer board interfacing to MULTIBUS (Intel) and to a wide range of communication and storage systems as TDX-Bus, PAM lines, UPI lines, Floppy Discs, communication I/F etc.

The document specifies only the hardware and that part of the firmware which includes address decoders, state controllers etc., while software is outside the scope of this specification.

Applicable Documents

TBS

0. SYSTEM ADVANTAGES

The Multi Purpose Processor, $(MP)^2$ card, is a standard micro computer module designed and manufactured by CHRISTIAN ROVSING A/S (CRAS).

The module is a highly integrated single card, dual processor micro computer system with a wide range of on-board interfaces and options, which makes it expandable to meet application requirements ranging from very small to very large systems.

- Mechanically and electrically compatible with INTEL's SBC boards, making the single board multiprocessor (MP^2) share a large no. of commercially available packing and power supply options with INTEL's multibus boards (SBC).

- Standard INTEL Multibus Interface (IEEE796) making the single board multiprocessor expandable with standard Multibus boards, (available from INTEL and hundreds of commercial vendors); such as Parallel I/O. Analog interface boards, memory boards, processor boards, hard disc interface, etc.

- (MP^2) highly compatible with CRAS standard communication interfaces (LTU), making communications S/W (Protocols) interchangeable.

- On-board connectors and Multimodule I/F for expansion with up to 3 standard INTEL iSBX Multimodule or CR custom interface modules.

- The $(MP)^2$ may be installed with two processors, one processor (8088 or Z80) or without any processors as a general memory and input/output board.

- The Main Processor (8088) may be extended with on-board mathematic co-processor (8087).

- On-board RAM 128 K byte, divided as 64 K byte local RAM on each of the two processors, and globally the total 128 K RAM is accessible by both processors.

- PROM area (standard 4 or 8 K byte) may be extended with on-board standard INTEL or CR custom PROM extension card to max. 64 K byte.

- On-board Floppy Disc interfaces for up to four floppy disc drives.

- Two on-board serial interfaces, one limited (terminal) and one full modem interface capable of synchroneous/asynchroneous operation with HDLC, SDLC, BSC etc.

- On-board TDX or X-net interface, by CR custom interface module.
- On board UPI or PAM serial process control interface and drivers, by CR Custom interface module each capable of handling 2 UPI or PAM lines, making hybrid systems combining UPI and PAM circuits possible.

1. INTRODUCTION

The Multi Purpose Multi Processor ((MP)^2) specified in this document is a high performance dual microcomputer configured with a Multibus interface by which the module may communicate with slavemodules as well as master modules.

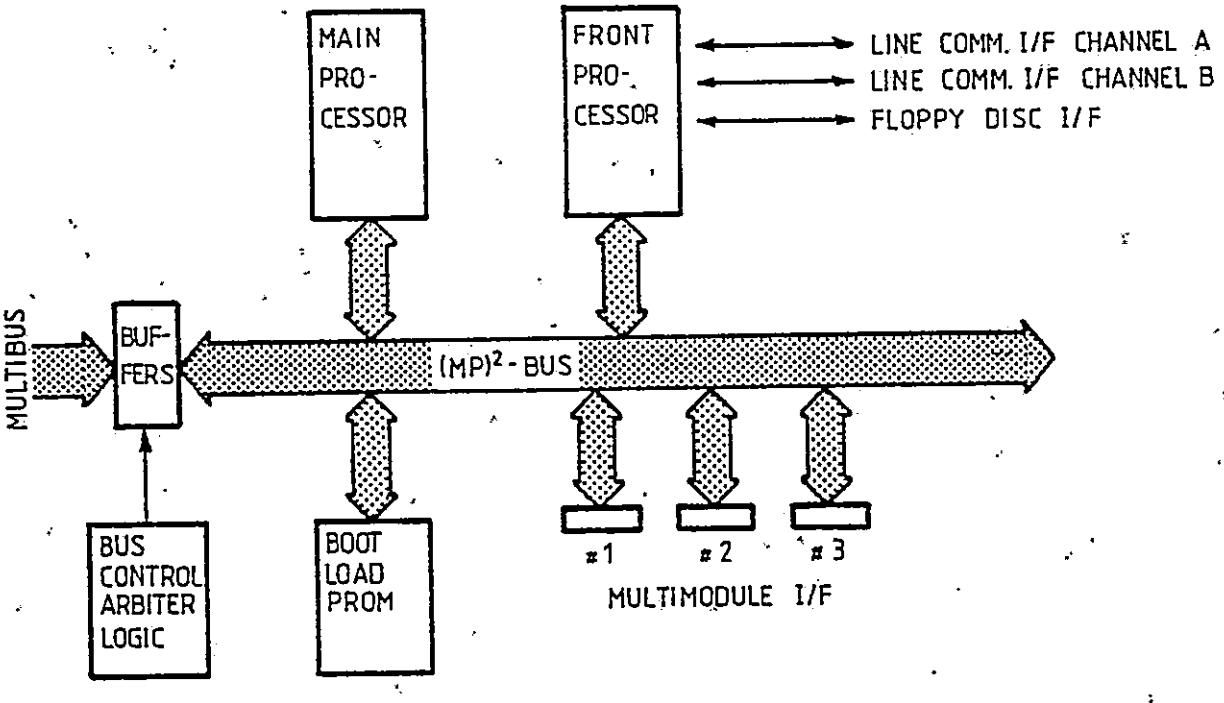
The two microcomputers are configured as general microcomputers with common access to all on board in- output devices, to the Multibus and to all on board memory, except for that part of each processors memory being reserved to contain its program code, which optionally can be protected via the address decoder.

Both computers may be equipped with up to 64 K memory (Dynamic RAM) which all may be battery backed up to ensure no data loss during Power failures.

To obtain the highest degree of expandability the internal bus structure ((MP)^2 Bus) is connected to three 36 pin on board connectors to which Multimodules and CR custom interface modules may be plugged in.

To control the Multibus (MP)^2 Bus and its interfaces a central Bus Control And Arbiter Logic is implemented.

A PROM area is interfaced to the (MP)^2 Bus. This area is normally only accessed during a boot load procedure or after a system-reset when the programs for built-in-test are accessed. This PROM area is 4K Byte bus is extendable to 64K by use of a small on board extension board.


MAIN PRO-CESSOR
FRONT PRO-CESSOR
LINE COMM. I/F CHANNEL A
LINE COMM. I/F CHANNEL B
FLOPPY DISC I/F
MULTIBUS
BUF-FERS
(MP)²-BUS
BUS CONTROL ARBITER LOGIC
BOOT LOAD PROM
#1
#2
#3
MULTIMODULE I/F

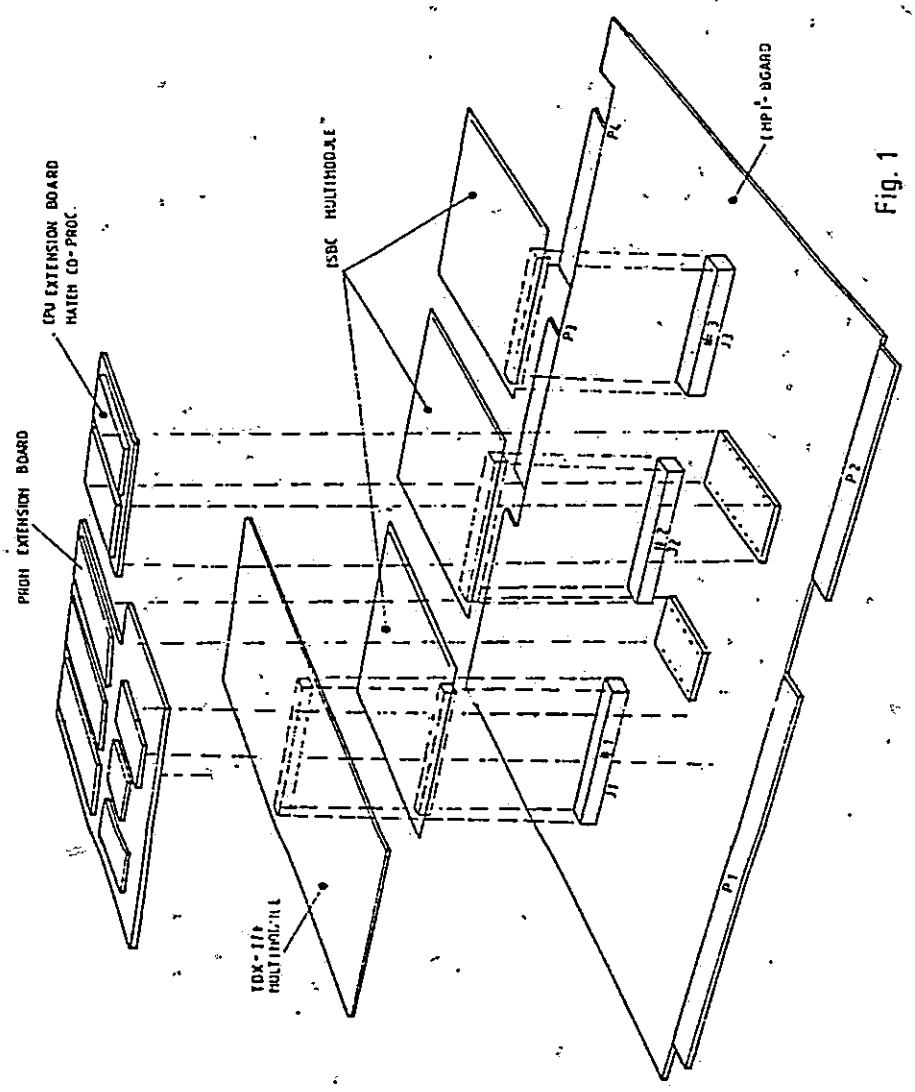


Fig. 1

CHRISTIAN ROVSING A/S

(MP)²

Onboard Extension Overview

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Parts no							
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1.1 Functional Summary

This brief functional description is based on the block diagram on fig. 2. The description handles only special interfaces and conditions as the (MP)[1] is designed ot be a simple general microcomputer with bidirectional access to a common bus system. All referred circuits are implied to be wellknown by the reader and only the HW interfaces and the addresses are included in this document.

The real performance of this module will not be obtained without an operating system controlling the interface between the two systems and the use of all common addressable devices as the DMA, the MAP register etc. by f.x. semaphore protection technics.

1.2 Block Diagram

Fig. 2 shows the (MP)[2] Block Diagram containing common internal busstructure called (MP)[2] - Bus interfacing to following logic functions:

- Main Processor
- Front Processor
- Multibus Interface
- Multimodule Interface
- Bus Arbiter & Control Logic
- Boot Load Prom

The following sections describe briefly the functions and control of these logic blocks.

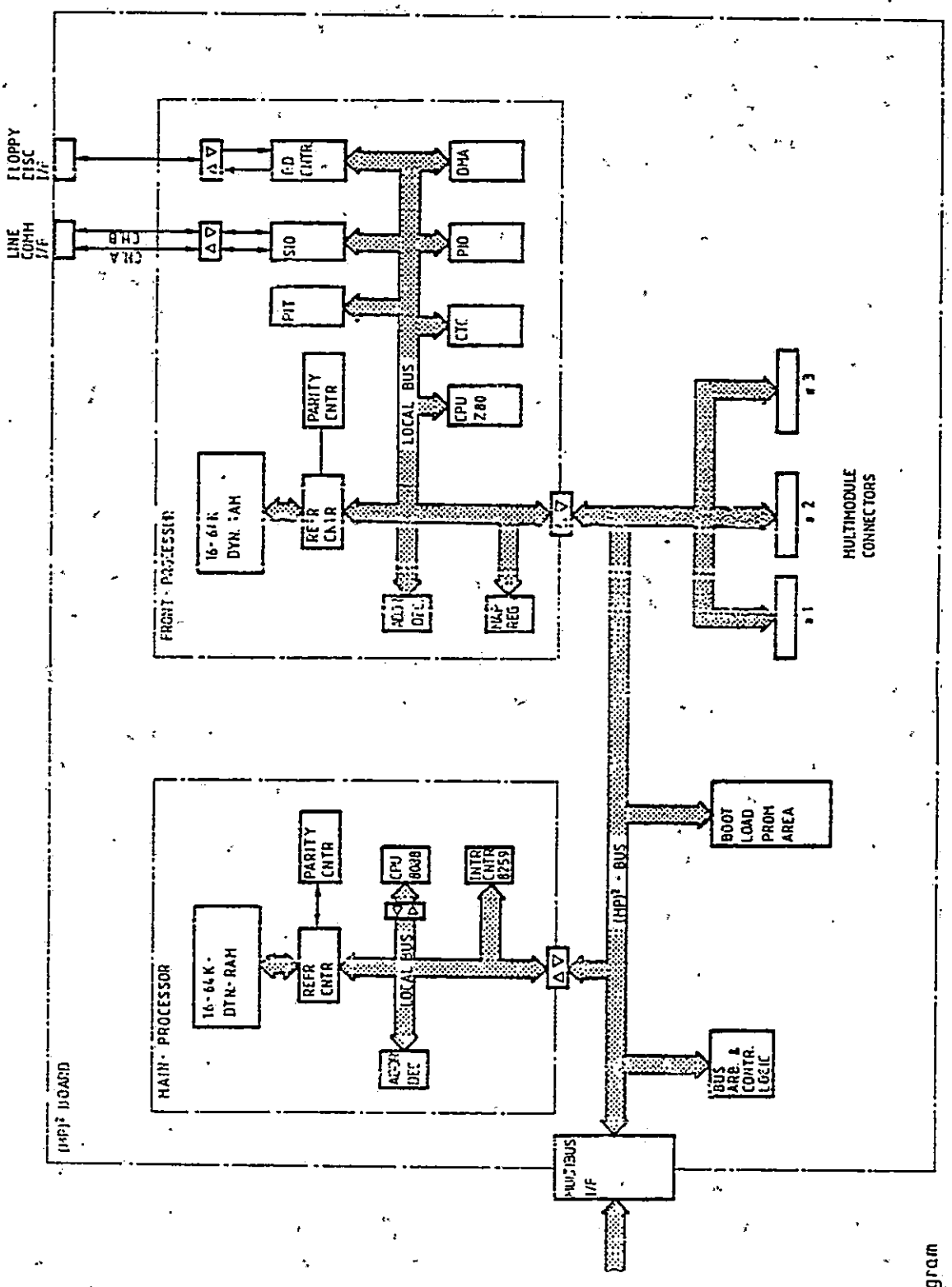


Fig 2
(MP)²
Block Diagram

1.2.1 Main Processor

The Main Processor is a microcomputer with its own local bus, 8 bit data bus and 20 bit address bus allowing control of 1 MByte memory.

The Main Processor consists of a CPU (i8088), an interruptcontroller (i8259), a 16/64K Ram-memory with parity control and a $(MP)^2$-bus interface. Refresh and control of the memory is automatic generated by the Ram interface circuit.

1.2.1.1 CPU

The CPU is configured in "Maximum Mode" for a well defined multiprocessor control via a handshake sequence. Following pin configurations of the CPU must be observed :

Reset is activated by the Power Control Logic when the power supplies are below the defined levels and kept active about 40 msec after the levels have been re-established.
Reset may be supplied to,or activated from the multibus. See sect. 2.1.

NMI is activated by a parity error, by time out during $(MP)^2$-bus access, by a watchdog alarm, or by Power Fail interrupt. $\overline{NMI}$ is ored together with $\overline{NMI}$ on Front Processor.

1.2.1.2 Interrupt Controller

The Interrupt Controller (i8259A) is controlling following interrupts, all supplied from the Front Processor.

IR0 : INT MBT Interrupt from Multibus Interface
IR1 : Floppy Disc Controller

IR2	:	CHANNEL 0 from PIT (8253)	
IR3	:	INTMP	INTERRUPT FROM FRONT PROCESSOR
IR4	:	N.C.	
IR5	:	MINTR0	MULTIMODULE I/F - 0
IR6	:	MINTR1	MULTIMODULE I/F - 1
IR7	:	MINTR2	MULTIMODULE I/F - 2

1.2.2 Front Processor

The Front Processor is a microcomputer with its own local bus, 8 bit databus and 16 bit address bus extended during global access with a 4 bit MAP-register.

The Front Processor consists of a CPU, a 16/64K RAM-memory with parity control, a $(MP)^2$-Bus interface, a timer, a DMA and some in- output circuits.

1.2.2.1 CPU

The CPU is a Z80A on which following pin connections must be observed:

Reset is activated by the Power Control Logic when power supplies are below the defined levels and kept active about 40 msec after the levels have been re-established.
Reset may be supplied to, or activated from the Multibus.

NMI is activated by a parity error, by timeout during $(MP)^2$-bus access, by watchdog alarm or by Power Fail interrupt. $\overline{NMI}$ to FP and MP are ored together.

1.2.2.2 CTC

The Timer-circuit (Z80-CTC) is configured as timer and interrupt controller as follows :

CH0 : Interrupt from DMA (EOP)
CH1 : Floppy Disc-interrupt
CH2 : Software Timer.
CH3 : Interrupt from Mainprocessor Multimodules
-Jumper Possibility for connecting a Interrupt from Multibus Interface instead of the interrupt from the Mainprocessor.

1.2.2.3 DMA

The DMA controller Am9517A is configured as follows:

CH0 : Floppy Disc controller.

CH1 :

CH2 : Z80-SIO channel A.

CH3 : Z80-SIO channel B.

CH0 and CH1 are also used during memory to memory transferes.

The DMA programming:
1. Normal timing
2. Late write
3. DREQ active high
4. DACK active low

1.2.2.4 SIO

The line communication interface (Z80-SIO) is a dualized serial interface with V24/V28 drivers/re-

ceivers.

Further specification of the interface is found in section 2.4.

Channel A : Extended Line Communication Interface.

Channel B : Limited Line Communication Interface.

The Z80-SIO may be serviced by one DMA channel per serial interface, receive or transmit direction selected by software, or it could be serviced in an interrupt or polling scheme.

1.2.2.5 PIT 8253

Channel 0: Interrupt to Main Processor / Bus Time For (8259A interrupt line 2) / MP^2 bus.

Channel 1: Baudrate generator to Channel A.

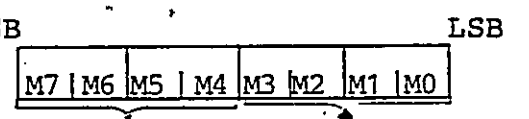
Channel 2: Baudrate generator to Channel B.

Input frequency to the PIT is 1,25 MHz.

1.2.2.6 PIO

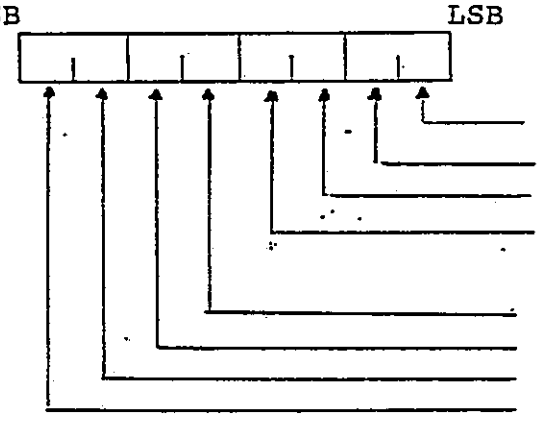
To extend the lay out of control lines for the SIO, a PIO (i8255) and an output register has been implemented. The parallel in-outputs of the PIO are assigned as follows:

PORT A
(output)
(add 08 H)

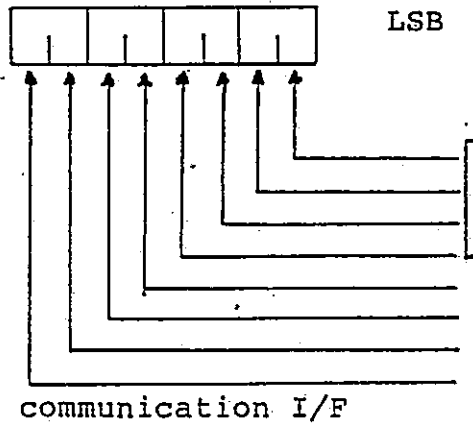


Map Register 1
Map Register 2
(See table 1)

PORT B
(Input)
(add 09 H)



PORT C
(bit 0-7:output)
(add 0A H)



* To extended line communication I/F

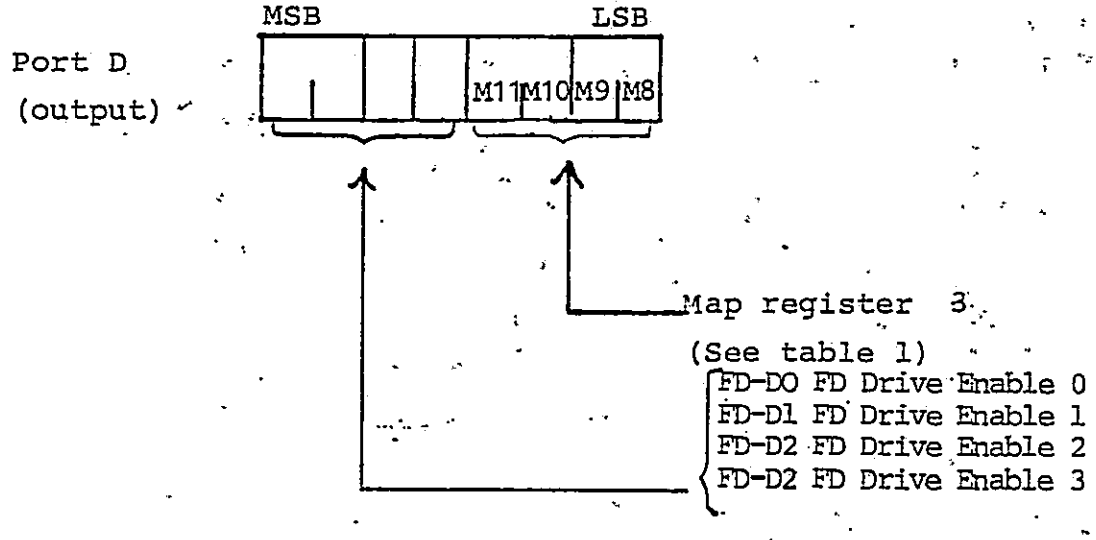
** The bus time out signal BKS (active high) indicate a bus time out and $\overline{NMI}$. The BKS and $\overline{NMI}$ signals are reset and disabled by pulling $\overline{BTR}$ low and enabled when $\overline{BTR}$ are set high again.

*** These bits are used to invert address line 15 when the Pront Processor access the (MP^2) bus.

"0" invert AF15
"1" non invert AF15

PORT D

The register is assigned as follows:



To extend the area addressed directly by Front Processor and DMA, a tripple MAP register is implemented. The control of these registers is rather complicated and must be executed under semaphore protection by a general operating system. (See sect. 3.1).

1.2.2.7 Floppy Disc. Controller

A general floppy disc. controller (WD 1797 or 1793) has been implemented for accessing one to four single or double density, single or double sided, 8" or 51/4" floppy disc. drives.

The controller is connected to a DMA channel and to an interrupt-input of the Front Processor which means that data transfers are normally controlled by this processor.

1.2.2.8 Interrupt Priority

The Z80-CTC and Z80-SIO is connected in a daisy chain interrupt structure where the Z80-CTC has highest priority.

1.2.3 Multibus Interface

The structure of the Multibus is built upon the master-slave concept where the master device in the system takes control of the Multibus interface and the slave device upon decoding its address, acts upon the command provided by the master. Multimasters are allowed to interface the Multibus, controlled by a simple arbitor/grant technic.

The $(MP)^2$ Multibus interface is provided to act as master or as an intelligent slave on the Multibus addressing 1M byte on an 8-bit databus structure. The interface is buffered and controlled according to the multibus specifications. (sect. 2.1.)

1.2.4. Multimodule Interface

On the $(MP)^2$ board three connectors are placed for interfacing standard iSBX modules or special purpose/function modules.

Each of the three connectors are addressed in a separate I/O area of 16 consecutive addresses.

Interrupt request lines are connected to main processor but DMA-request lines have no connection on the $(MP)^2$-board.

1.2.5. Bus Arbiter & Control Logic

The $(MP)^2$-bus includes an 8-bit databus, 20-bit address bus and a control bus.

The interfaces to the bus are seperated in the slave interfaces (multimodule I/F) and the master/slave interfaces (Multibus I/F, Main Proc., Front Proc.)

Seen from the Bus-Arbiter and Control Logic there is no difference between the three interfaces and the complete function is issued by a state controller performing a rotating access-priority scheme and a very fast arbitration mechanism operating with the functions request/grant/release.

Overleaf is shown timing diagram for a $(MP)^2$ bus access.

(MP^2) BUS ACCESS TIMING

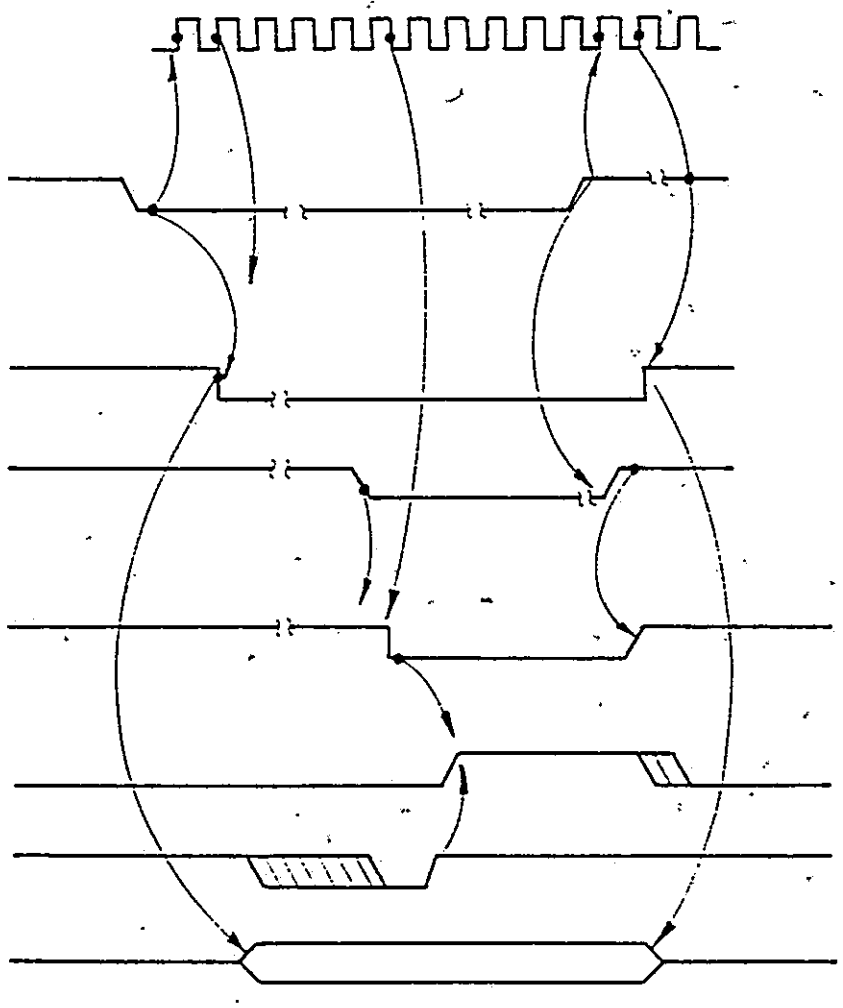


Fig. 3

1.3. Mechanical Layout

Fig. 4 shows the outline of the $(MP)^2$ board.

Connector Assignment

P3: Floppy Disc Interface.

P4: Pin 0-25 Extended Line Communication Interface.

Pin 26-50 Limited Line Communication Interface.

J1: Multimodule Interface # 1.

J2: Multimodule Interface # 2.

J3: Multimodule Interface # 3.

P1: Multibus Interface

P2: Optional Bus (Part of Multibus spec.)

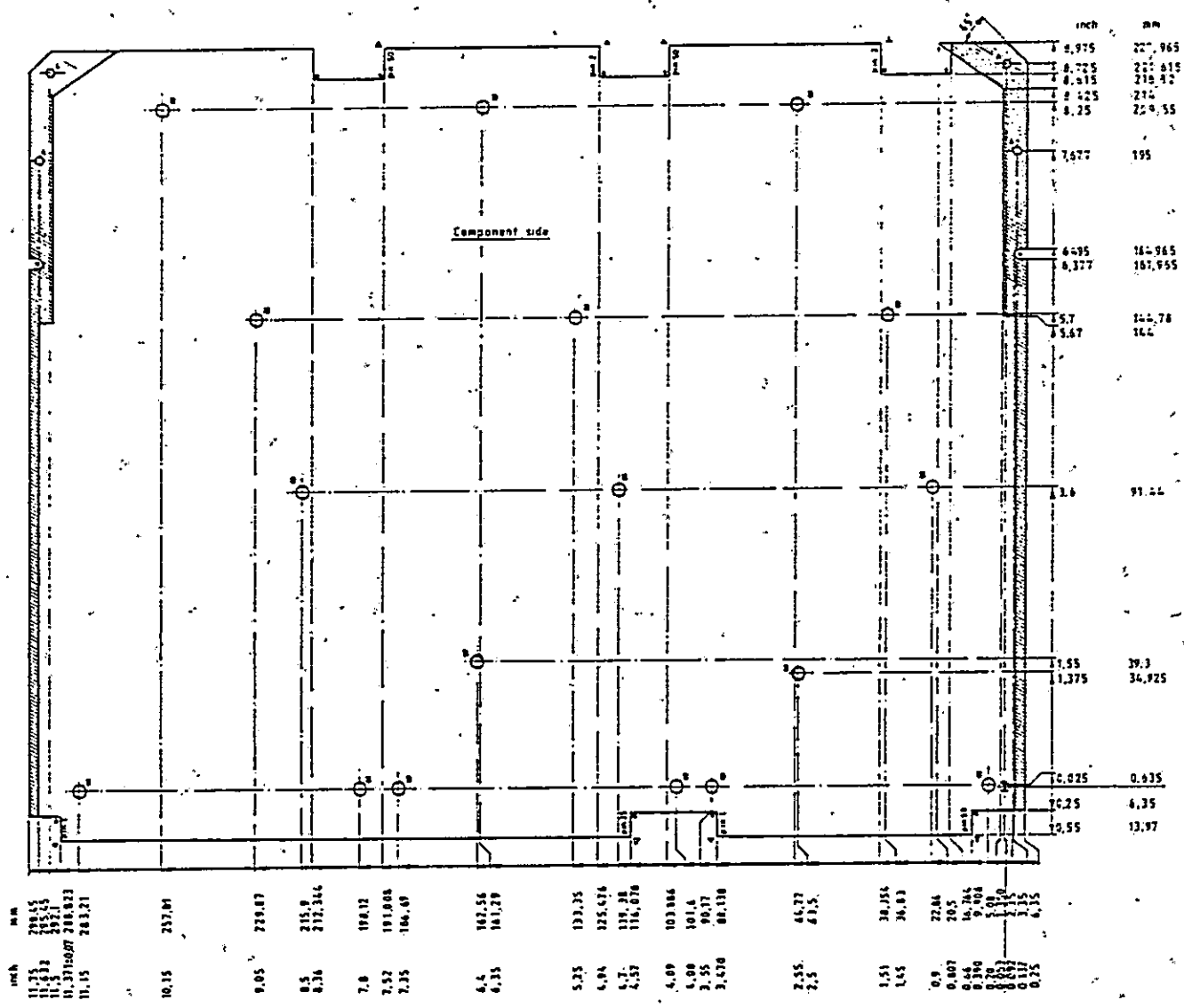


Fig. 4
$(MP)^2$ - PCB Outline.

2. INTERFACE SPECIFICATIONS

The $(MP)^2$ interfaces to external devices via the edge connectors P1, P2, P3, P4 and the on board connectors J1, J2, J3 and optionally for special purposes via the CPU socket and the Boot-load Prom-socket.

In the following section all these interfaces will be specified in the matter of signals, mechanical as well as electrical sizes and values.

2.1. Multibus Interface

The MULTIBUS interface is the flexible bus structure used to interface the family of SBC boards which include 8- and 16-bit single board computer, memory expansion boards, digital and analog I/O boards and peripheral controllers. It supports direct addressability up to one megabyte through 20-bit addresses and 8- and 16-bit data transfers.

The bus structure is built upon the master-slave concept where the master device in the system takes control of the MULTIBUS interface and the slave device, upon decoding its address, acts upon the command provided by the master. This handshake between master and slave devices allows modules of different speeds to use the MULTIBUS interface and allows data rates up to five million byte transfers per second.

Another important MULTIBUS feature is the ability to connect multiple master modules for multiprocessing configurations. The MULTIBUS interface provides control signals for connecting multiple masters either in a daisy-chain priority fashion or in parallel. With this latter arrangement, up to sixteen masters may share MULTIBUS resources.

The MULTIBUS Interface of the $(MP)^2$ is a limited MULTIBUS Interface as defined in the following sections.

It may be configured as master module or as intelligent slave module.

2.1.2. Signal Specifications

Table 2 and 3 contain definitions of the signals which appear on the limited multibus connector P1 and P2.

Timing specifications are according to those recommended for Multibus interfaces.

TABLE 2.

MULTIBUS Connector (P1) Signal Definitions

SIGNAL	FUNCTIONAL DESCRIPTION
ADR0/ ADRF/ ADR10/ -ADR13/	Address. These 20 lines transmit the address of the memory location or I/O port to be accessed. For memory access, ADR0/ (when active) enables the even byte bank (DAT0/-DAT7/) on the Multibus; i.e., ADR0/ is active for all even addresses. ADR13/ is the most significant address bit.
BCLK/	Bus Clock. Used to synchronize the bus contention logic on all bus masters.
BPRN/	Bus Priority In. When low indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN/ is synchronized with BCLK/.

TABLE 2 (CONTINUED)

BPRO/	Bus Priority Out. In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	Bus Request. In parallel priority resolution schemes BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	Bus Busy. Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	Common Bus Request. Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller raises the CBRQ/ signal.
CCLK/	Constant Clock. Provides a clock signal of constant frequency for use by other system modules.
DAT0/ DAT7/	Data. These 8 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DAT7/ is the most significant bit.
INIT/	Initialize. Reset the entire system to a known internal state.

TABLE 2 (CONTINUED)

INTO/- ILT7/	INTERRUPT REQUEST. Non Bus victored interrupt inputs, high to low edge triggered. Only one of the Interrupt Request lines is serviced by the $(MP)^2$. The input is selected by strap but INT0/ is standardwise connected to the interrupt controller of the Main Processor.
IORC/	I/O Read Command. Indicates that the address of an I/O port is on the Multibus address lines and that the output of that port is to be read (placed) onto the Multibus data lines.
IOWC/	I/O Write Command. Indicates that the address of an I/O port is on the Multibus address lines and that the contents on the Multibus data lines are to be accepted by the addressed port.
MRDC/	Memory Read Command. Indicates that the address of a memory location is on the Multibus address lines and that the contents of that location are to be read (placed) on the Multibus data lines.
MWTC/	Memory Write Command. Indicates that the address of a memory location is on the Multibus address lines and that the contents on the Multibus data lines are to be written into that location.
XACK/	Transfer Acknowledge. Indicates that the address memory location has completed the specified read or write operation. That is, data has been placed onto or accepted from the Multibus data lines.

Table 3

Auxiliary Connector (P2) Signal Definitions

SIGNAL	FUNCTIONAL DESCRIPTION
RESET/	Reset. This externally generated signal initiates a power-up sequence.
PFIN/	Power Failure Interrupt. This signal from the power supply interrupts both processor by NMI when a power failure occurs.

Tables 4 and 5 contain connector pin assignments for P1 and P2.

Table 4

Pin Assignment of Bus Signals on Multibus Board Connector (P1)

	PIN	(COMPONENT SIDE) MNEMONIC	DESCRIPTION	PIN	(CIRCUIT SIDE) MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Sig GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9			10		
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock. 10MHZ	14	INIT/	Initialize
	15	BPRN/	Bus Pri.In	16	BPRO/	Bus Pri.Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24		
BUS CONTROLS AND ADDRESS	25			26		
	27			28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk.	32	AD12/	Bus
	33		10MHZ ($\overline{\text{BCLK}}$/)	34	AD13/	
INTERRUPTS	35	INT6/		36	INT7/	
	37	INT4/	PARALLEL	38	INT5/	PARALLEL
	39	ILT2/	INTERRUPT	40	INT3/	INTERRUPT
	41	INT/0	REQUESTS	42	INT1/	REQUESTS
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0		58	ADR1/	
DATA	59			60		
	61			62		
	63			64		
	65			66		
	67	DAT6/	Data	68	DAT7/	Data
	69	DAT4/	Bus	70	DAT5/	Bus
	71	DAT2/		72	DAT3/	
	73	DAT0		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77			78		
	79	-12V	-12Vdc	80	-12V	-12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

Table 5

P2 Connector PIN Assignment of Optional Bus Signals

PIN	(COMPONENT SIDE) MNEMONIC	DESCRIPTION	PIN	(CIRCUIT SIDE) MNEMONIC	DESCRIPTION
1	GND	Signal GND	2	GND	Signal GND
3	5VB	+5V Battery	4	5VB	+5V Battery
5			6		
7			8		
9			10		
11			12		
13			14		
15			16		
17	PFIN/	POWER FAILURE Interrupt	18		
19			20		
21	GND	Signal GND	22	GND	Signal GND
23			24		
25			26		
27			28		
29			30		
31			32		
33			34		
35			36		
37			38	AUX RESET/	Reset switch
39			40		
41			42		
43			44		
45			46		
47			48		
49			50		
51			52		
53			54		
55			56		
57			58		
59			60	AUX PWR	AUX. POWER

2.1.2 Electrical Specifications

This section provides electrical specifications that are unique to each signal or groups of signals.

Table 6 lists all the specifications.

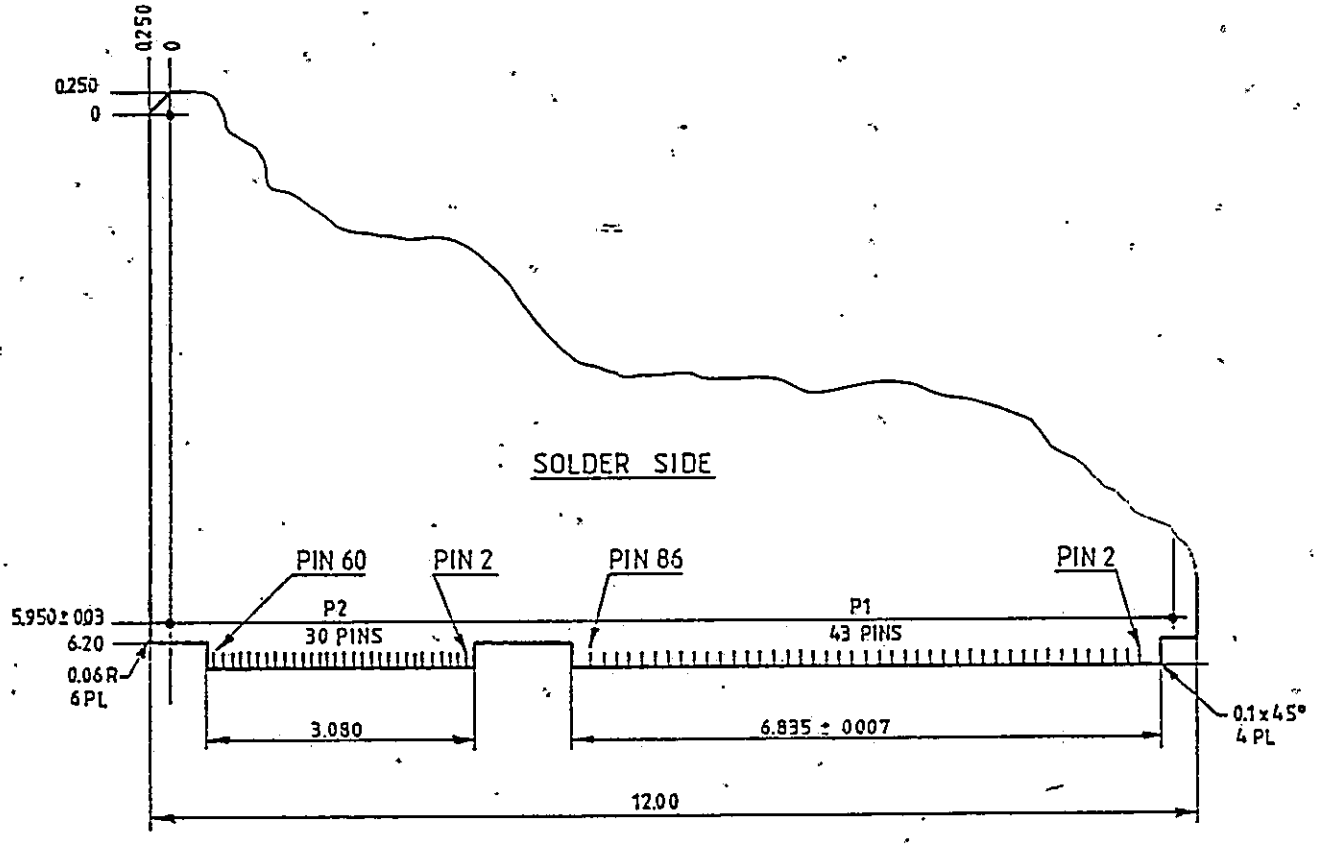
Table 6

Electrical Specifications of Bus Drivers, Receivers,

Bus Signals	Driver 1,3					Receiver 2,3				Termination			
	Location	Type	I_{OL} Min ma	I_{OH} Min µa	C_O Min pf	Location	I_{IL} Max ma	I_{IH} Max µa	C_I Max pf	Location	Type	R	Units
DAT0'DATF/ (16 lines)	Masters and Slaves	TRI	16	-2000	300	Masters and Slaves	-0.8	125	18				
ADR0/-ADRB/ (20 lines)	Masters	TRI	16	-2000	300	Slaves	-0.8	125	18				
MRDC/.MWTC/	Masters	TRI	32	-2000	300	Slaves (Memory; memory-mapped I/O)	-2	125	18	(MP)[2]	Pullup	1	KΩ
IORC/.IOWC/	Masters	TRI	32	-2000	300	Slaves (I/O)	-2	125	18	(MP)[2]	Pullup	1	KΩ
XACK/	Slaves	TRI	32	-2000	300	Masters	-2	125	18	(MP)[2]	Pullup	510	Ω
BCLK/	1 Place	TTL	48	-1000	300	Master	-2	125	18	Mother-board			
BREQ/	Each Master	TTL	5	-400	60	Central Priority Module	-2	50	18	Central Priority Module			
BPRO/	Each Master	TTL	5	-400	60	Next Master in Serial Priority Chain at Its PRN/	-1.6	50	18				
BPRN/	Parallel: Central Priority Module Serial: Masters BPRO/	TTL	5	-400	60	Master	-2	50					
BUSY/.CBRQ	All Masters	O.C.	32	-	300	All Masters	-2	50	18	(MP)[2]	Pullup	1	KΩ
INIT/	Master	O.C.	32	-	300	All	-2	50	18	(MP)[2]	Pullup	2.2	KΩ
CCLK/	1 place	TTL	48	-3000	300	Any	-2	125	18	Mother-board			

2.1.3 Mechanical Specification

This section specifies the mechanical lay out of P1 and P2 connector.



2.2 Multimodule Interface

The Multimodule I/F is a unique interface facilitating onboard expansion with Multimodule boards. The Multimodule bus is derived directly from the $(MP)^2$ bus and as such, a Multimodule board plugged into the $(MP)^2$ bus becomes an integral element of the $(MP)^2$. The physical interface between the $(MP)^2$ and the Multimodule board is a unique connector designed specifically for this interface. The Multimodule bus is brought out to a female connector on the $(MP)^2$ and mates with its male equivalent resident on the Multimodule board.

The $(MP)^2$ contains three Multimodule interfaces which are limited Multimodule Interfaces numbered # 1, # 2 and # 3.

2.2.1 Signal Specifications

Tables 7 and 8 contain definitions of the signals which appears on the limited Multimodule interface connectors J1, J2 and J3.

Timing specifications are according to those recommended for Multimodules.

Table 7

Multimodule Connector Signal Definitions

Signal	Functional Description
MD0-MD7.	Data These active high bidirectional data lines transmit data between the Multimodule and $(MP)^2$.
IORD/ IOWRT/	I/O Read I/O Write The command lines are active low signals which provide the communication link between the $(MP)^2$ board and the Multimodule board. An active command line, conditioned by chip select, indicates to the Multimodule board that the address lines are valid and the Multimodule board should perform the specified operation.
MA0-MA2	Address These positive true input lines to the Multimodule boards are generally the least three significant bits of the I/O address. In conjunction with the command and chip select lines, they establish the I/O port address being accessed.
MCS0/- MCS1/	Chip Select Lines These input lines to the Multimodule board are the result of the base board I/O decode logic. MCS/ is an active low signal and thus enables communication with the Multimodule boards.
RESET	Reset This input line to the Multimodule board is generated by the base board to put the Multimodule board into a known internal state. Aktiv High

TABLE 7

CONTINUED

MWAIT/- MPST/	WAIT Multimodule Present. These output signals form the Multimodule board control the state of the system. Active MWAIT/(Active Low) will put the CPU on the board into a wait state providing additional time for the Multimodule board to perform the requested operation. MWAIT/ must be generated from address (address plus chip select) information only. If MWAIT/ is driven active due to a glitch on the CS line during address transitions, MWAIT/ must be driven inactive in less than 75 ns. The Multimodule board present (MPST/) is an active low signal (tied to signal ground) that informs the base board I/O decode logic that an Multimodule board has been installed.
MINTRØ-1	INTERRUPT LINES These active high output lines from the Multimodule board are used to make interrupt requests to the base board. Only one is connected to interrupt controller of Main Processor. Selectable by straps. The three selected interrupts from the multimodules are gated together and connected to CTC channel 3.

TABLE 7
CONTINUED

MCLK	CLOCK LINES This 10MHz input to the Multimodule board is a timing signal.
AUX-PWR	AUX. POWER This is a power input for special purposes

TABLE 8

Pin assigment of Bus Signals on Multimodule connector J1, J2, J3.

Pin	Mnemonic	Description	Pin	Mnemonic	Description
35	GND	Signal Ground	36	+5V	+5 volt
33	MD0	MDATA Bit 0	34		
31	MD1	MDATA Bit 1	32		
29	MD2	MDATA Bit 2	30		
27	MD3	MDATA Bit 3	28		
25	MD4	MDATA Bit 4	26		
23	MD5	MDATA Bit 5	24		
21	MD6	MDATA Bit 6	22	MCS0/	M Chip Select 0
19	MD7	MDATA Bit 7	20	MCS1/	M Chip Select 1
17	GND	Signal Gnd	18	+5V	+5 Volts
15	IORD/	I/O Read Cmd	16	MWAIT/	M Wait
13	IOWRT/	I/O Write Cmd	14	MINTR0	M Interrupt 0
11	MA0	M Address 0	12	MINTR1	M Interrupt 1
9	MA1	M Address 1	10	AUX.PWR	AUX. POWER
7	MA2	M Address 2	8	MPST/	iSBX Multimodule Board Present
5	RESET	Reset	6	MCLK	M Clock
3	GND	Signal Gnd	4	+5V	+5 Volts
1	+12V	+12 Volts	2	−12V	−12 Volts

2.2.2 Electrical Specifications

This section provides the electrical specifications that are unique to each signal of the Multimodule interface.

Table 10 lists all the specifictions.

TABLE 10

Multimodules interfacing to $(MP)^2$ shall fulfill following electrical specifications.

Output[1]

Bus Signal Name	Type[2] Drive	I_{OL} Max −Min (mA)	@ Volts (V_{OL} Max)	I_{OH} Max −Min (μA)	@ Volts (V_{OH} Min)	Co (Min) (pf)
MD0-MD7	TRI	1.6	0.5	−200	2.4	130
MINTR0-1	TTL	2.0	0.5	−100	2.4	40
MDRQT	TTL	1.6	0.5	− 50	2.4	40
MWAIT/	TTL	1.6	0.5	− 50	2.4	40
OPT1-2	TTL	1.6	0.5	− 50	2.4	40
MPST/	TTL	Note 3				

Input[1]

Bus Signal Name	Type[2] Receiver	I_{IL} Max (mA)	@ V_{IN} Max (volts)	I_{IH} Max (μA)	@ V_{IN} Max (volts)	Ci Max (pf)
MD0-MD7	TRI	−0.5	0.8	70	2.0	40
MA0-MA2	TTL	−0.5	0.8	70	2.0	40
MCS0/-MCS1/	TTL	−4.0	0.8	100	2.0	40
MRESET	TTL	−2.1	0.8	100	2.0	40
MDACK/	TTL	−1.0	0.8	100	2.0	40
IORD/ IOWRT/	TTL	−1.0	0.8	100	2.0	40
MCLK	TTL	−2.4	0.8	100	2.0	40
OPT1-OPT2	TTL	−2.0	0.8	100	2.0	40

NOTES:
1. Per iSBX Multimodule I/O board.
2. TTL = standard totem pole output. TRI = Three-state.
3. iSBX Multimodule board must connect this signal to ground.

2.2.3 Mechanical Specifications

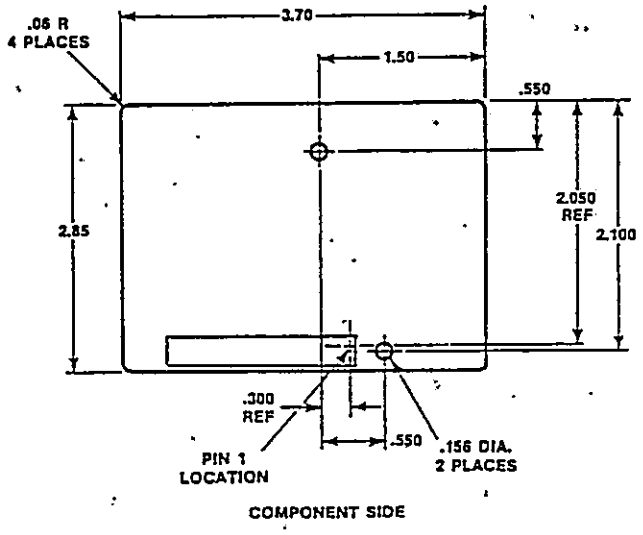
This section specifies the mechanical Lay out for different Multimodules.

Fig. 5 contains three standard lay outs, and fig. 6 shows a special extended Multimodule, the TDX-Interface-module (See sect. 4.1.1).

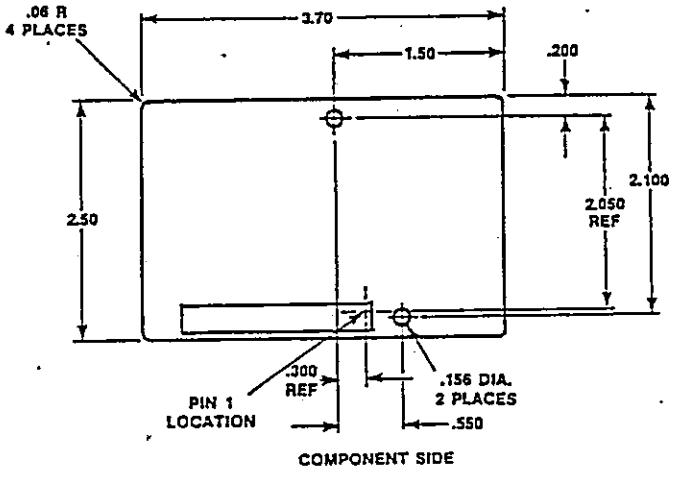
Mechanical Lay Out for Standard Multimodules

The outlined connectors are placed on the solder side of the PCB.

A.



B.



C.

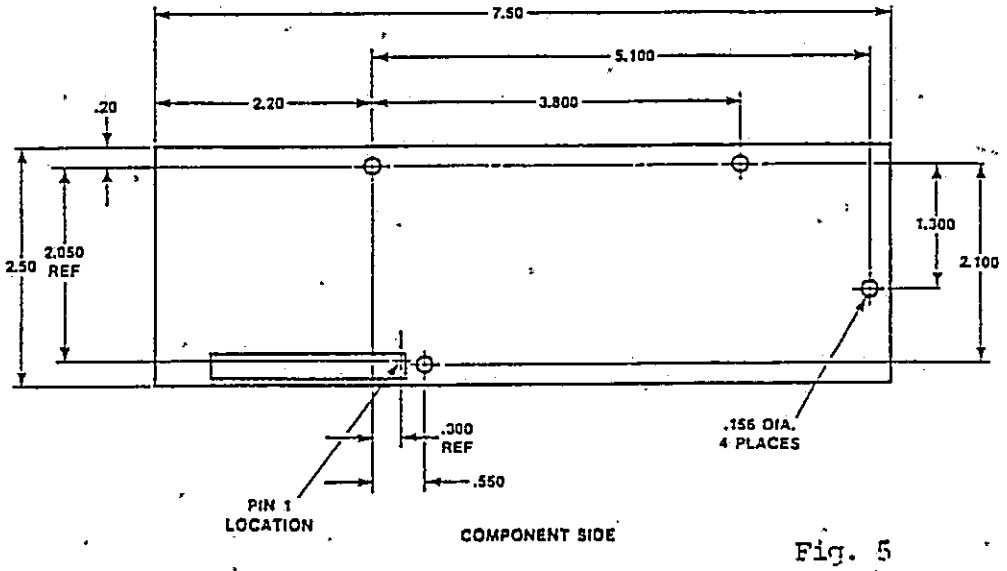


Fig. 5

Mechanical Lay-Out for TDX-Multimodule

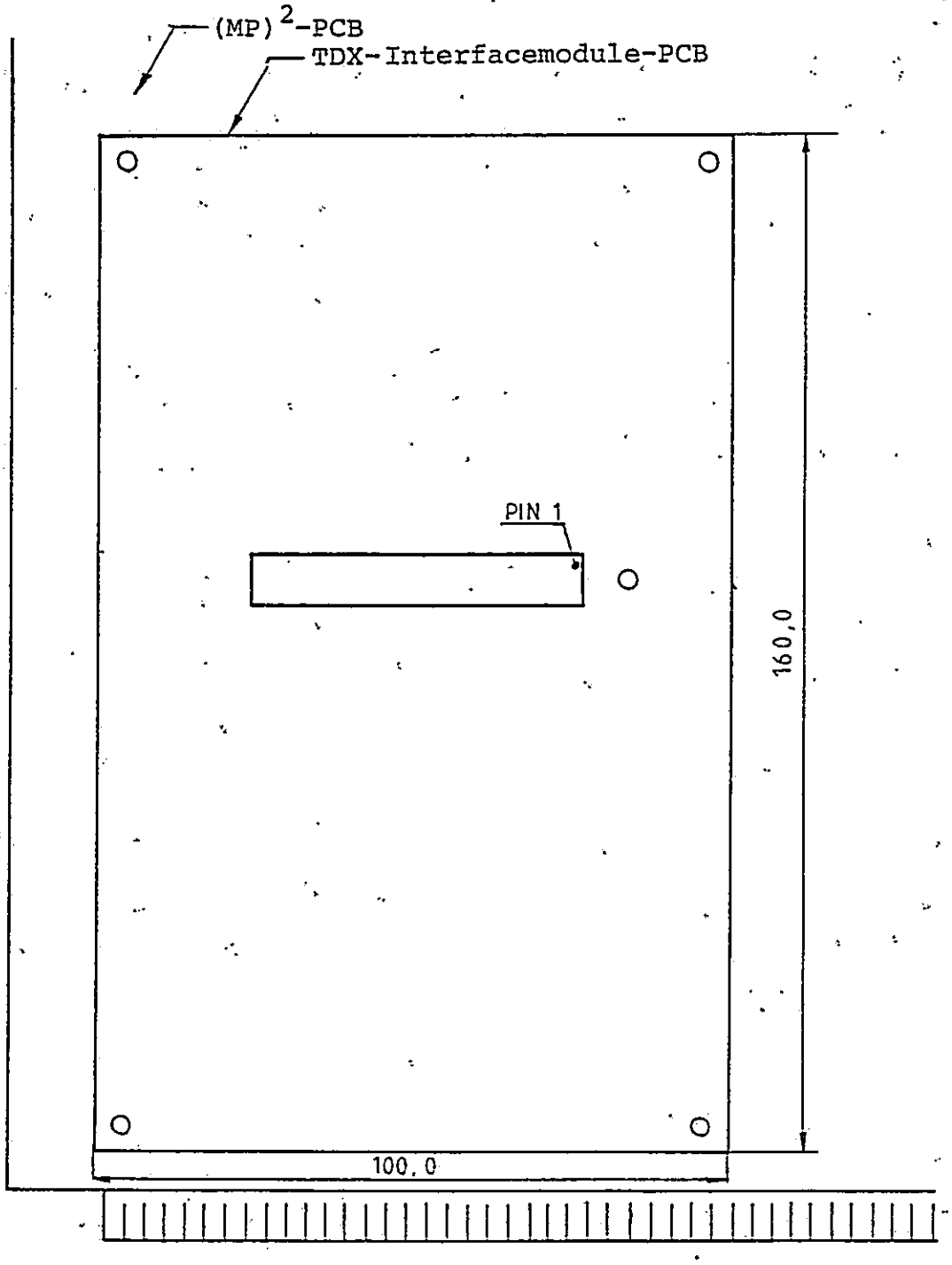


Fig 6

The outlined connector is placed on the solder side of the TDX-Interfacemodule PCB.

2.3 Floppy Disc Interface

This interface is mechanical placed on a 50 pin edgeconnector (J1) to which a standard flat cable connector may be connected upto four floppy disc on a daisy chained bus.

Double Density $5^1/_4$"	upto 3 Floppy Disc Drive. *
Single Density $5^1/_4$"	upto 3 Floppy Disc Drive. *
Double Density 8"	upto 4 Floppy Disc Drive.
Single Density 8"	upto 4 Floppy Disc Drive.

* One select output is used as Motor Drive on.

Iff Double side Disc Drive is used either Floppy Disk Contr. 1797 can be used, (1797 have a output for Head-select) or 1793 and one select output to Head-select.

2.3.1 Signal Specifications

Table 11 contains definitions of the signals which appear on the Floppy Disc Interface connector J1, and table 12 defines the pin assignment of this connector.

TABLE 11

Floppy Disc Interface Signal Spec.

Signal	Functional Description
READY	Ready. This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed.
$\overline{TR0}$	TRACK ZERO. This input informs that the Read-Write Head is positioned over Track 00 when a logic low.
$\overline{INDEX}$	INDEX HOLE Input, when low for a minimum of 10 µsec. informs the controller when an index mark is encountered on the diskette.

Table 11
Continued

Signal	Functional Description
$\overline{\text{WPRT}}$	Write Protected. This interface signal is provided by the drive to give the system an indication when a Write Protected Diskette is installed.
$\overline{\text{READ DATA}}$	READ DATA The data input signal directly from the drive. This input shall be a pulse for each recorded flux transition.
$\overline{\text{WRITE DATA}}$	WRITE DATA This interface line provides the data to be written on the diskette.
$\overline{\text{DIR}}$	DIRECTION This interface line is a control signal which defines direction of motion the R/W head will take when the step line is pulsed.

TABLE 11
Continued

Signal	Functional Description
$\overline{HLD}$	HEAD LOAD The HLD output controls the loading of the Read-Write head against the media.
$\overline{WG}$	Write gate This output is made valid when writing is to be performed on the diskette.
$\overline{STEP}$	Step The step output contains a pulse for each step. The R/W head has to move with the direction of motion as defined by the Direction Select line (DIR).
$\overline{DR0}$-$\overline{DR3}$	Drive Select Lines Activates, when active, one of four Floppy Disc Drives.
HEAD SELECT	Side select when using double sided Floppy Disk. If using 1793 chip, DR2 can be strapped to Head Select by jumper. 1797 have a output pin for Head Select.

TABLE 12

Pin Assignment of signals on Floppy Disc Interface

PIN	Description	Pin	Description
		11	GND
22	READY/DR3.	15	GND
42	TR0	17	GND
20	INDEX	19	GND
44	WPRT	21	GND
46	READ DATA	23	GND
38	WRITE DATA	25	GND
18	HLD	27	GND
40	WG	29	GND
34	DIR	31	GND
36	STEP	33	GND
26	$\overline{DR0}$	35	GND
28	$\overline{DR1}$	37	GND
3o	$\overline{DR2}$	39	GND
32	$\overline{DR3}$	41	GND
24	INDEX	43	GND
		45	GND
48	Head Select/$\overline{DR2}$	47	GND
14		49	GND

2.3.2 Electrical Specification

This section provides the electrical specifications that are unique to each groups of signals.

Table 13

Electrical Specifications of
Floppy Disc. Interface

Inputs:	Signal Name	Receivers	Pullup rest	Iil (max)	Vil (max.
	SEPC READY TRQ INDEX WRPT READ DATA	TTL (7414)	150Ω	-1.2mA	0,6V
Outputs:	Signal name	Drivers		Iol (max)	Vol(max)
	WRITE DATA DIR HLD WG STEP DR0 - DR3	TTL (OC) (7438)		48mA	0,4V

2.3.3 Mechanical Specification

Mechanical lay out and dimension are shown on Fig. 1.

2.4 Line Communication Interfaces

These two interfaces are connected to the edge connector J2 in a matter that when a 50 wire flatcable and connector is fitted to P4, and when the cable is splitted between the wires 25 and 26, it may be mounted with two 25 pin Cannon connectors. The connectors will then be configured in accordance with CCITT V24 recommendation for DTE devices.

2.4.1 Signal Specifications

The signals and their timing specifications are according to the CCITT V24 recommendations.

Table 14 and 15 contains the signal definition of the channel A and B interfaces (Extended Line Communication Interface/Limited Line Communication Interface).

Table 16 lines out the pin assignment of the interface, and the pin connection of the common connectors mounted on the splitted flatcable.

Table 14

Line Communication Signal Definition
Channel A (Extended Line Communication Interface)

CIRCUIT NO.	DRIVER/ RECEIVER	CONNECTION TO/FROM	DESCRIPTION
103	DRIVER	SIO	TRANSMITTED DATA
104	RECEIVER	SIO	RECEIVED DATA
105	DRIVER	SIO	REQUEST TO SEND
106	RECEIVER	SIO	CLEAR TO SEND
107	RECEIVER	PIO	DATA SET READY
108	DRIVER	SIO	DATA TERMINAL READY
109	RECEIVER	SIO	DATA CARRIER DETECT
111	DRIVER	PIO	DATA SIGNALLING RATE SELECT
113	DRIVER	TIMER	TRANSMITTER CLOCK
114	RECEIVER	SIO	TRANSMITTER CLOCK
115	RECEIVER	SIO	RECEIVER CLOCK
116	DRIVER	PIO	SELECT STANDBY
117	RECEIVER	PIO	STANDBY INDICATOR
125	RECEIVER	PIO	CALL INDICATOR

Table 15

Line Communication Signal Definition Channel B

CIRCUIT NO.	DRIVER/ RECEIVER	CONNECTION TO/FROM	
103	DRIVER	SIO	TRANSMITTED DATA
104	RECEIVER	SIO	RECEIVED DATA
105	DRIVER	SIO	REQUEST TO SEND
106	RECEIVER	SIO	CLEAR TO SEND
108	DRIVER	SIO	DATA TERMINAL READY
109	RECEIVER	SIO	DATA CARRIER DETECT
C113	DRIVER	TIMER	TRANSMITTER CLOCK
C115	RECEIVER	SIO	RECEIVER CLOCK

Table 16

Pin assignment of Line Communication Interface:

Signal	Cannon Connector	P4 Connector		Cannon Connector	Signal	
	1	1	2	14		
C-103	2	3	4	15	C-114	
C-104	3	5	6	16		
C-105	4	7	8	17	C-115	
C-106	5	9	10	18		
C-107	6	11	12	10		
C-102	7	13	14	20	C-108	
C-109	8	15	16	21		
	9	17	18	22	C-125	Channel A
	10	19	20	23		
C-111	11	21	22	24	C-116	
	12	23	24	25	C-117	
	13	25				
			26	1		
	14	27	28	2	C-103	
C113	15	29	30	3	C-104	
	16	31	32	4	C-105	
C115	17	33	34	5	C-106	
	18	35	36	6		
	19	37	38	7	C-102	
C-108	20	39	40	8	C-109	Channel B
	21	41	42	9		
	22	43	44	10		
	23	45	46	11		
	24	47	48	12		
	25	49	50	13		

Channel A (Pin 1-25) is called the "Extended Line Communication Interface".

Channel B (Pin 26-50) is called "Limited Line Communication Interface"

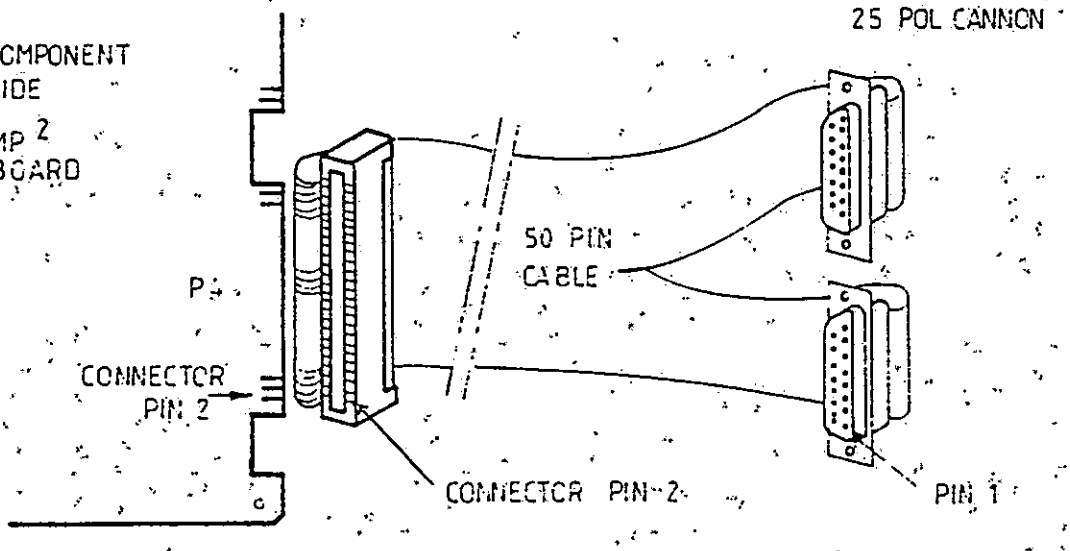
2.4.2 Electrical Specifications

The electrical specifications are according to CCITT-V28 recommendation.

2.4.3 Mechanical Specification

The mechanical layout of the edge connector is shown on Fig. 4. If a flat cable connector is connected to the edge connector and the cable is splitted between wire 25 and 26, then the two 25 pin Cannon connectors of female type shall be mounted on these flat cables as follows:

Cannon Connector	Cable wire	P4-pin
A, pin 1	1	1
B, pin 1	26	26



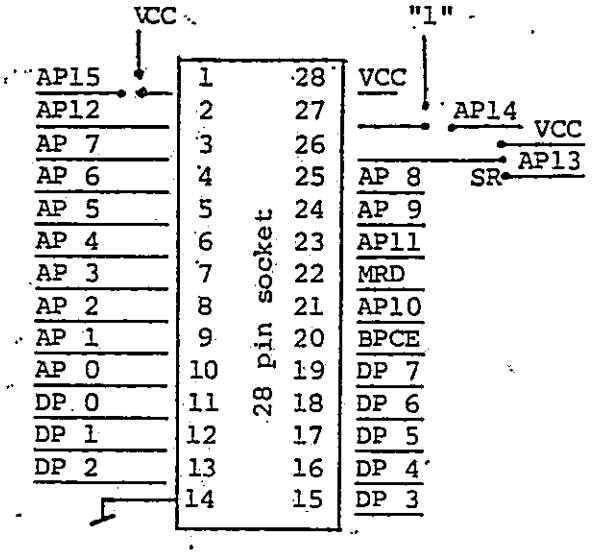
2.5 Boot Load PROM

The PROM-area of the $(MP)^2$ may be extended by replacing the PROM with a small PROM-board with a socket fitting directly into the PROM socket.

All needed functions as decoding buffering etc. are placed on this extension board.

In this way the Boot Load PROM-area may be extended upto (64 K-bytes)..

2.5.1 Signal specification



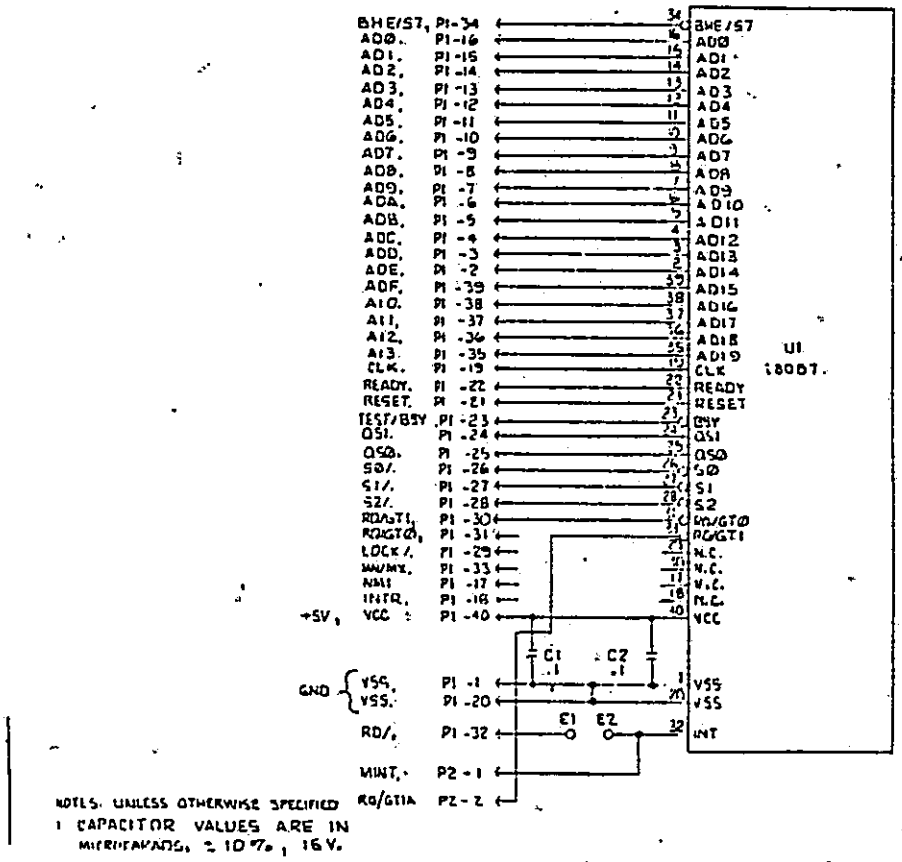
2.6 Mathematic Co-Processor

By replacing the Main processor-CPU with a small PCB containing a CPU and a mathematic co-processor a very high performance is obtained in number-crunching applications.

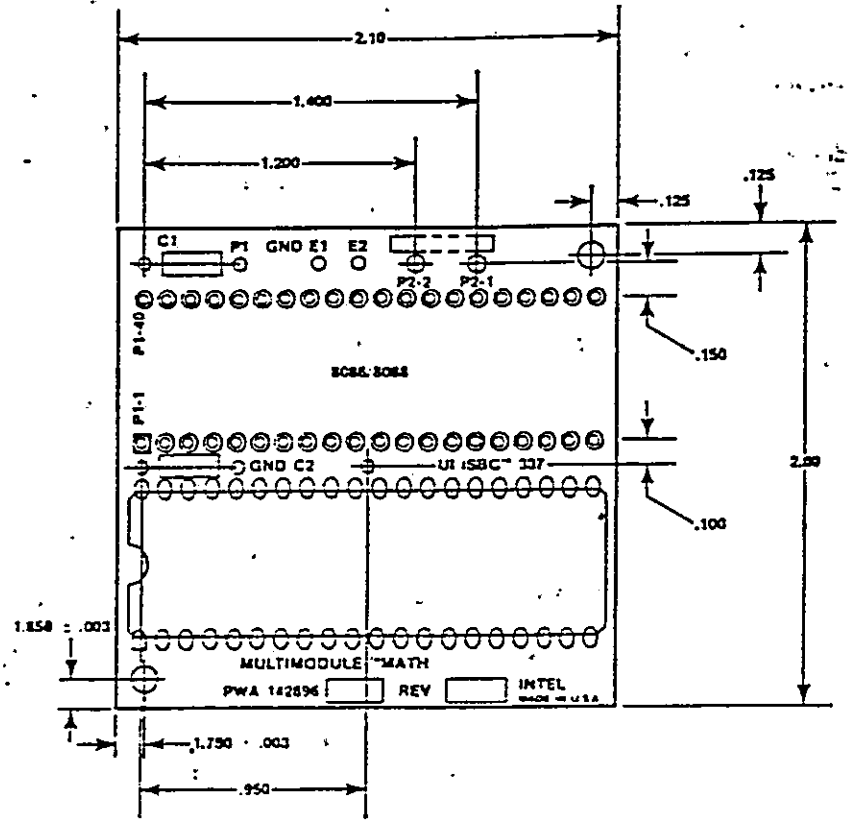
All needed circuits for this extension are prepared on the $(MP)^2$ or are situated on the PCB which fits directly into the CPU socket.

Intel offers a standard Co-processor Multimodule, iSBC 337 containing a 8088 CPU and a 8087 Numberic Data Processor.
Interrupt from ISBC 337 is not connected to the $(MP)^2$ board

2.6.1 Signal Specifications



2.6.3 Mechanical Specifications



3. OPERATIONS

Hardware wise, there is nearly no operational restrictions, but software wise, a well designed grant technic must be observed for access to all I/O-devices especially the DMA and the MAP Registers.

To obtain a safe HW system the $(MP)^2$-Bus interfaces are equipped with a time out function which means that no $(MP)^2$-Bus access must take more than 50 µSec., and to recognize that both processors are well working a watch Dog function is implemented. This means that the line called Watch Dog Pulse, on Port C of the PIO (see sect. 1.2.2.6) has to be pulsed continously, i.e. set by Front Processor and reset by the Main Processor about once per 250 m Sec.

The Bustime out function come in force in two situations. The first is if one of the two onboard processors have addressed a restricted area or a non existing module. The second is when a bus lock situation occur.

Bus lock situation can happen if the Front Processor on two MP^2 boards addresses each other at the same time, none of them can answer on a Bus request.

It will also happen if the FP on a MP^2 board and a processor on another processor board addresses each other at the same time.

If a MP and a FP addresses each other the conflict will be solved. The FP get a special acces to the MP's bus first. The bus-controller on the MP^2 bus detect the conflict and the drivers/latches nearest the 8088 CPU are disabled the 8088 stay in wait, and the FP get acces to the MP RAM area.

The Bus time out logic will give a $\overline{NMI}$ to both processors and disable the wait states.

Processors can now read a status bit BKS on the PIO port B bit 7 (msb), when "high" it is a Bus Time out. The status bit and $\overline{NMI}$ are reset again when bit 4 on port C $\overline{BTR}$ is pulled low and high.

If $\overline{BTR}$ (Bus Time Reset) stay "low" the Bus time out function is disabled.

When a time-out situation has been placed the Main Processor has to read the status bit and if necessary reset the function with $\overline{BTR}$ in less than one CLK INT period from the NMI.

CLK INT is an output from the PIT (8253) channel 0. It is used as timer interrupt to Main Processor too. The period for CLK INT has to be a compromise between these two functions. Recommended Bus Time Out period is about 50 µSec.

3.1 Address MAP

This section describes the local and global address MAP for each of the processors of the $(MP)^2$ and globally seen from the Multibus. In section 3.2 is found a description of the Map function performed by the Front Processor. Boot Load PROM contains Boot Load programs and builtin-test programs for both processors and is normally only accessable after a reset or when "Clear Boot Mode" output from PIO is activated.

A proper switch technic for the Boot Load PROM must be observed to avoid MAP collisions.

3.1.1 Global Address Map.

	I/O	Memory
Boot Load Prom		*00000-0FFFF
Multimodule I/F #1	*50-5F	(40000-4FFFF)
Multimodule I/F #2	*60-6F	(80000-8FFFF)
Multimodule I/F #3	*70-7F	(C0000-CFFFF)
Main Processor		*10000-1FFFF (50000-5FFFF)
Memory		(90000-9FFFF)
Interruptcontroller Interrupt to Front Processor		(D0000-DFFFF)
Front Processor		
Memory		*20000-2FFFF
CTC		(60000-6FFFF)
PIO	*08-0F	(A0000-AFFFF)
SIO	*10-1F	(E0000-EFFFF)
Map-reg.	*20-2F	
DMA	*30-3F	
Floppy Disc. Contr.	*40-4F	
8253 PIT	*D0-DF	
Maynot be used	Rest of I/O add. in 0-400H	*30000-3FFFF

Boot Load Prom is globally accessable without any influence from the state of the "Clear Boot Mode" lines. (see sect. 1.2.2.5).

* There is possibility for changing the base address for the $(MP)^2$ Module seen from the Multi bus interface.

K

Global Add. Continued

The $(MP)^2$ board occupy 4 pages of Memory (1 page = 64 K) seen from the Multibus Interface. The I/O area is 400 Hex wide.

The base address for the $(MP)^2$ board is selectable by two jumpers SR18 and SR19.

	SR19	SR18	I/O	MEMORY
No. 0.	A("0")	A("0")	0000-0400	00000-3FFFF
No. 1.	A("0")	B("0")	4000-4400	40000-7FFFF
No. 2.	B("1")	A("0")	5000-5400	80000-BFFFF
No. 3.	B("1")	B("1")	6000-6400	C0000-FFFFF

In No. 0 the memory area 30000-3FFFF can not be used, as well as all I/O add. 0-400 H not specified in the address map may not be used.

In No. 1 has Boot Load prom the area 40000-4FFFF H, MP - 50000-5FFFF H, and FP - 60000-6FFFF H. 70000-7FFFF may not be used.

The I/O add. is 4000-4400. The I/O addresses not specified in the area 4000-4400 may not be used.

In No. 2 may memory add. B0000-BFFFF not be used and the I/O add. not specified in the area 5000-5400 may not be used.

In no. 3 may memory add. F0000-FFFFF not be used, and I/O addresses not specified in the area 6000-6400 may neither be used.

Main Processor Address Map

	I/O	MEMORY
Boot Load Prom		F0000-FFFF (can be addressed on page 1 too, 10000-1FFFF).
Multimodule I/F # 1 $\overline{MCS0}$	50-57	
Multimodule I/F # 1 $\overline{MCS1}$	58-5F	
Multimodule I/F # 2 $\overline{MCS2}$	60-67	
Multimodule I/F # 2 $\overline{MCS3}$	68-6F	
Multimodule I/F # 3 $\overline{MCS4}$	70-77	
Multimodule I/F # 3 $\overline{MCS5}$	78-7F	
Main Processor		
Memory		00000-0FFFF
Interrupt Contr. 8259A	C0-CF	
Interrupt to Front Processor	80-8F	
Front Processor		
Memory		28000-2FFFF (20000-27FFF are protected. Can be used on boards where only Front Processor RAM is mounted).
PIO	08-0F	
SIO	10-1F	
Map REG 3/Floppy Drive select.	20-2F	
DMA	30-3F	
8253 PIT	D0-DF	
Floppy Disk Contr.	40-4F	
Multi Bus Interface		
Memory	90-CF E0-FF	40000-EFFFF
I/O	4000-FFFF	
May not be used	Rest of I/O Addresses	30000-3FFFF.

The 8088 CPU start after power up or reset at address FFFF0. It will always be in the top of the Boot Load prom. If only a 4K Prom 2732A is used, address FFFFOH from 8088 will be address FFOH in the Prom.

If it is a 8K Prom 2764A the address will be 1FFOH, and if it is a 64K Prom board the address will be FFFO.

Front Processor Address Map

	I/O	MEMORY
Boot Load Prom		30000-3FFFF
Multiboard I/F # 1 $\overline{\text{MCS0}}$	50-57	
Multiboard I/F # 1 $\overline{\text{MCS1}}$	58-5F	
Multiboard I/F # 2 $\overline{\text{MCS2}}$	60-67	
Multiboard I/F # 2 $\overline{\text{MCS3}}$	68-6F	
Multiboard I/F # 3 $\overline{\text{MCS4}}$	70-77	
Multiboard I/F # 3 $\overline{\text{MCS5}}$	78-7F	
Main Processor		
Memory		18000-1FFFF **
Front Processor		
Memory		00000-0FFFF
CTC	00-07	
PIO	08-0F	
SIO	10-1F	
Map Reg 3/Floppy Drive Select	20-2F	
DMA	30-3F	
8253 PIT	DO-DF	
Floppy Disc Controller	40-4F	
Multi Bus Interface		
Memory		40000-FFFFF
I/O *	0080-00CF	
	00E0-00FF	
May not be used		20000-2FFFF

After reset or power up will memory address 0-7FFF be mapped out to the Boot Load Prom area.

Address 8000-FFFF will still be in the FP RAM, (if Map reg. 3="0").

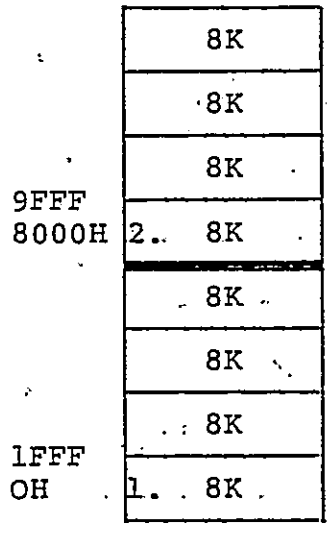
The boot mode is disabled by resetting Boot F signal, output from PIO.

* When addressing I/O interface out on the Multibus, be aware of the 8 msb address lines, 16 addresses lines are used.

I/O devise on the MP^2 board seen from the Front Processor use only the 8 lsb add. lines, the rest is not used.

** Memory area 10000-17FFF H are protected by local decoders on the full implemented boards where the Main Processor RAM is mounted and not the rest of the Main Processor.

If the RAM area is only 16K the first 8K are placed from 0-1FFFH and the last 8K from 8000-9FFF.



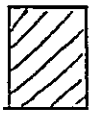
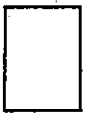
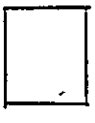
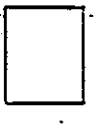
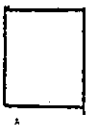
The first 8K will be reflected 3 times up to add. 8000H.

The last 8K will be reflected 3 times up to add. FFFFH.

3.2 MAP FUNCTION

To extend the memory space addressable to the Front Processor CPU three Map registers have been implemeted The dedecated use of these registers is shown in table 18 while the address map procedure has been illustrated in table 17.

Table 17.

	INTERNAL memory		EXTERNAL memory		
PAGE	0	1	2	...	15
ADDR. 0000 7FFF					
8000 FFFF					
MAP REG.	0000	0001	0010	...	1111
Port C Bit 3	1	0 1	0 1		0 1

Address area 0-7FFF in page 0 may be proceted against access from the $(MP)^2$-Bus.

When Bit 3 port C is "0" address line AF15 will be inverted when the Front Processor acces the MP^2 bus.
If not in Boot Mode the area 0-7FFFH will always be F.P. own Ram. The area 8000-FFFFH depend on the current Map register. If the FP have to acces a area 0-7FFF on page 1-15, it have to address the area 8000-FFFF and provide that AF15 will be inverted.

TABLE 17

Controlling Device	Type of data-transfer	Memory Map Register 1	2	3
Front-Proc.	Between CPU and external memory (64K - 1 M			X
Front-Proc. or Main Proc.	Memory to memory DMA transfers	Data read	Data write	
Front-proc. or Main Proc.	DMA Transfers. Z80-SIO to memory (or opposite).	X		
Front-Proc. or Main Proc.	DMA transfers. Floppy Disc Controller to Memory (or opposite).		X	

By external memory means external to the Front Processor

4. Options

The $(MP)^2$ module concept offers a design where a wide range of Multiboards and Multimodules may be combined to fulfil the application requirements.

In this section some special Multimodules are briefly described.

4.1 Multimodules

Standard Multimodules (iSBX) are offered on the market fulfilling the signal, electrical and mechanical requirements of the $(MP)^2$.

The following section contains a briefly description of some special Multimodules offered by CRAS.

4.1.1 TDX-Interface

See Documentation for

$Xnet\ (MP)^2$ Adapter
CR2525--/001--/00

K

4.1.2 PAM-Interface

TBS

4.1.3 UPI Interface

TBS

4.1.4 Line Communication Interface

TBS

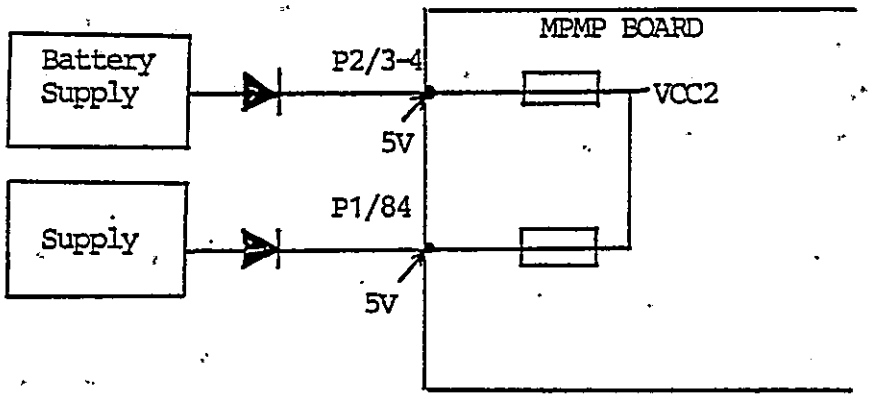
4.2 Battery Back-Up

To protect against data loss during power failures or simple power-off, a battery back-up option has been implemented.

The circuits which may be supplied from the Multibus connection called "5V Battery", are the dynamic Ram memories of the Main Processor and the Front processor.

When the main power supply (5V) level is below 5V ÷ 5% the Ram chips and the refresh and control circuits are supplied from this optional connection and external access to the memories during this state is not possible.

VCC2 supply to RAM chips and refresh control



In case of using Battery back up there have to be connected a extern supply and a diode.

The voltage on the connector have to be 5V ± 5%.

The voltage from supply and the battery need to be more the 5 Volt.

5. Power Specifications

VCC+VCC2	5V ~ 5,0A ± 0.5A	
	12V ~ 0,1A *	
	-12V ~ 0,1A *	

*V24 Channel is not connected

VCC2	5V ~ 0,50A	Activ RAM operation
	~ 0,35A	stand by