SUPERMAX HARDWARE

Programmers Manual
for the
SIOC MODULE 300
October 1983

This document describes the Serial I/O Controller module in the SUPERMAX computer system, as seen by the programmer. The document contains information about how to configure and install SIOC modules in the SUPERMAX computer.

TABLE OF CONTENTS.

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1. INTRODUCTION.

The SUPERMAX computer concept and basic functions are described in the manual: "SUPERMAX hardware characteristics". Some general information is repeated here.

The SUPERMAX computer system is a modular, multi-CPU computer system. The main processing elements are the CPU modules. A SUPERMAX Computer system consists of a number of CPU modules, each with its own main memory, and a number of intelligent I/O controllers, IOCs.

The IOCs performs all input/output between the CPU modules and peripherals. An IOC is able to transfer data directly to and from user memories without any CPU intervention. CPU modules and IOCs are connected to a common I/O bus.

The I/O bus is basically a memory bus, because all units connected to the bus are accessed as memory from the I/O bus. A bus transfer involves two units: one, the active, takes the initiative to the bus cycle, and addresses the other unit, the passive, and performs a read or write cycle in its memory. CPU modules and IOCs can participate in bus transfers both as active and passive units. When a module is the passive unit in a bus transfer, it is just a port to its own main memory. When a module is the active part in a bus transfer, it is able to access an address space of 16 Mb, in up to 15 units connected to the I/O bus. 16 units can be connected to the I/O bus. A module is able to address only 15 units because it is not able to address itself via the I/O bus.

Units connected to the common bus are able to interrupt each other. A unit sends an interrupt to another unit by writing in a certain part of its memory. Each unit connected to the I/O bus has a part of its memory reserved for this purpose. Interrupts generated in this manner are called external interrupts. Normally a unit has a number of interrupt sources on the unit itself, for examble, timer interrupt and various error interrupts. These interrupts are called internal interrupts.

2. BASIC HARDWARE ELEMENTS.

The SIOC is a single printed circuit board with standard SUPERMAX dimensions. The SIOC performs all input output between terminals, printers, modems or other peripherals with RS-232-C/RS-422 interface.

The PCB contains the following basic hardware elements:

* CPU.
* Memory.
* Service port.
* Interrupt unit.
* Memory mapping unit.
* I/O bus interface.
* Serial communication interface.
* Baud rate generators.
* Parallel printer interface.
* Error detecting and handling circuit.

3. CPU.

The CPU used in the intelligent Serial I/O Controller is an INTEL 8085-A2, running with an effective speed of 5 MHz. The 8085 is a 8 bit general purpose microprocessor. The processor is capable of accessing 64 kbyte of memory. All peripherals are serviced by I/O mapped I/O, not memory mapped I/O.

4. MEMORY LAYOUT.

The on-board memory consists of 64 kbyte parity-checked dynamic RAM and 8 kbyte EPROM. The EPROM is divided into two parts. One half is placed in the address space from address 0x0000 to 0x1000. The other half is placed from address 0xE000 to 0xFFFF. The lower part of the EPROM is selected by the 8085 signal SOD. Upon power up reset the signal is active, and the lower part of the EPROM is selected. The RAM in the same address area is, of cource, deselected. The lower part of the EPROM is deselected by deactivating SOD.

The address area 0x1000 to 0xbfff is always RAM. The decoding of the addresses from 0xc000 to 0xffff depends on the content of the address mapping register.

AMR(7:0), Address Mapping Register.
Access mode: I/O write.
I/O address : 0xBB
Upon power up reset: AMR(7:0) = 0

AMR(0) : /EDEB, Enable DEBugger.

AMR(0) = 0 : The EPROM is enabled in address area 0xe000 to 0xffff.
AMR(0) = 1 : The RAM is enabled in address area 0xe000 to 0xffff.

AMR(1) : ENBO, Enable Bus Out.

AMR(1) = 0 : The RAM is enabled from adr. 0xc000 to 0xe000 or 0xffff depending on AMR(0).
AMR(1) = 1 : Any memory access in area 0xc000 to 0xe000 or 0xffff will be performed as an I/O bus transfer.

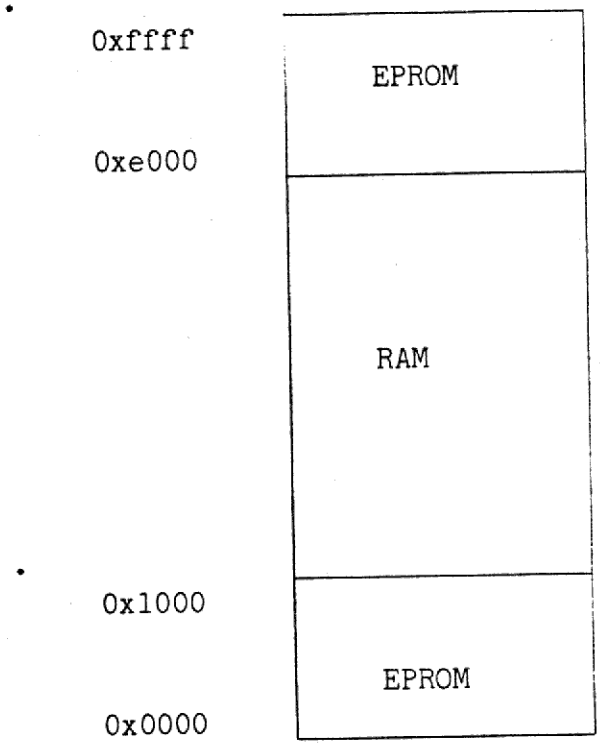
AMR(2) : ENBI, Enable Bus In.

AMR(2) = 0 : An access to the SIOC module from the I/O bus is not answered.
AMR(2) = 1 : All locations in the 64 kbyte RAM memory are available from the I/O bus.

AMR(7:3) are not used.

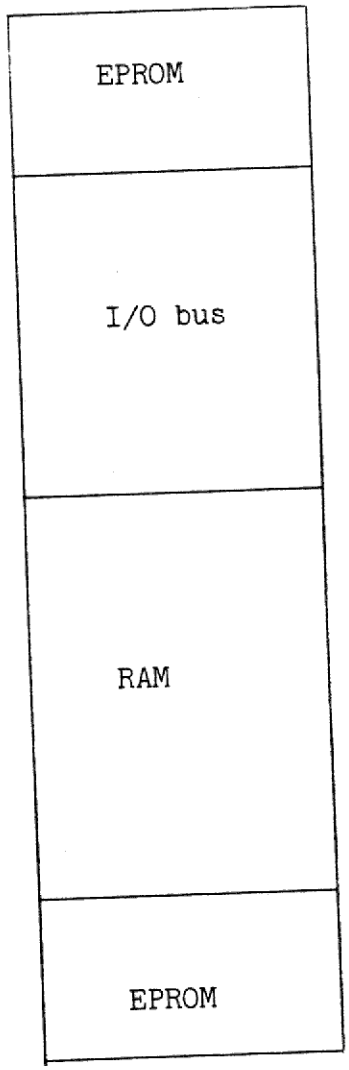
Memory layout after reset:

AMR(2:0) = 000



Memory layout for program development.

AMR(2:0) = 110

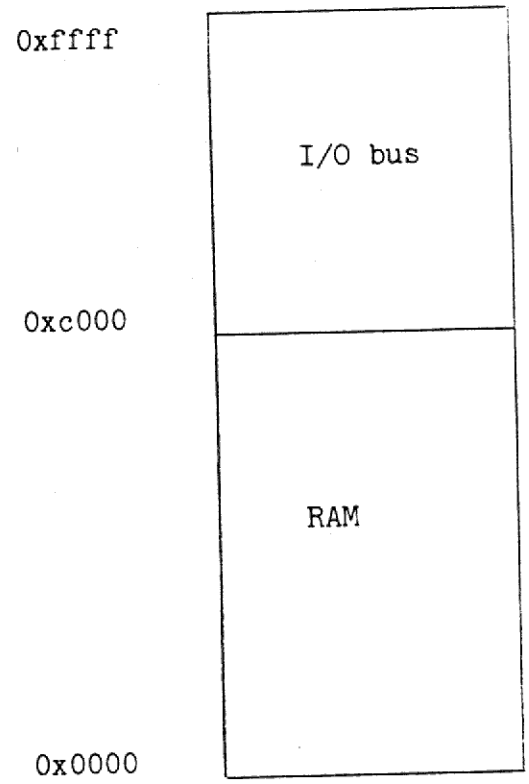


Debug/monitor program.

Bootloader program.

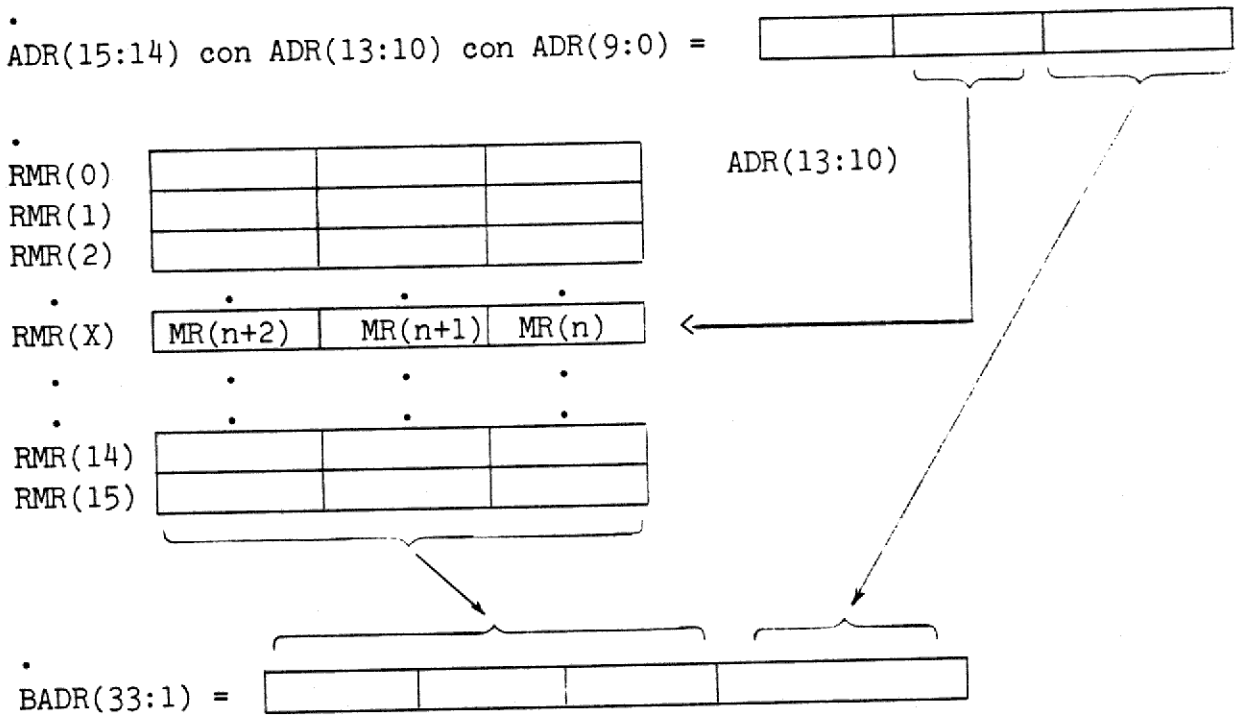
Memory layout for normal use.

AMR(2:0) = 111



5. MEMORY MAPPING UNIT.

When the SIOC is the active part in a I/O bus transfer, the 16 bit 8085 address is expanded through a memory mapping unit. This enables the SIOC to transfer data directly to and from all memory locations connected to the I/O bus. The 8085 address is called ADR(15:0). When ADR(15:14) = 11 and the 8085 performs a memory cycle, the cycle will be a cycle to the I/O bus. (depends on contents of AMR)
ADR(13:10) is used to select one of 16 entries to the memory mapper. Each entry is called a Resulting memory Map Register, RMR. Each RMR consist of three Map Registers, MR. Each map register is 8 bit wide.



The resulting address is the I/O bus address: BADR(33:1)

BADR(33:0) = RMR(X) con ADR(9:0)
BADR(33:0) = MR(n+2)(7:0) con MR(n+1)(7:0) con MR(n)(7:0) con ADR(9:0)

MR(47:0)(7:0), Map Register. 48 map registers, each 8 bits wide.
Access mode: I/O write and I/O read.
Upon power up reset: Contents undefined.

I/O addresses:

	MR(n+2)	MR(n+1)	MR(n)
RMR(0)	0xC2	0xC1	0xC0
RMR(1)	0xC6	0xC5	0xC4
RMR(2)	0xCA	0xC9	0xC8
RMR(3)	0xCE	0xCD	0xCC
RMR(4)	0xD2	0xD1	0xD0
RMR(5)	0xD6	0xD5	0xD4
RMR(6)	0xDA	0xD9	0xD8
RMR(7)	0xDE	0xDD	0xDC
RMR(8)	0xE2	0xE1	0xE0
RMR(9)	0xE6	0xE5	0xE4
RMR(10)	0xEA	0xE9	0xE8
RMR(11)	0xEE	0xEd	0xEC
RMR(12)	0xF2	0xF1	0xF0
RMR(13)	0xF6	0xF5	0xF4
RMR(14)	0xFA	0xF9	0xF8
RMR(15)	0xFE	0xFD	0xFC

An example:

```
        MVI  A,30
        OUT  0C2        ;SETUP MR(2)
        MVI  A,89
        OUT  0C1        ;SETUP MR(1)
        MVI  A,23
        OUT  0C0        ;SETUP MR(0)
        LDA  C056       ;READ A BYTE FROM A UNIT ON THE I/O BUS.
```

The I/O bus address is:

```
00  1100 0010  0010 0100  1000 1100  0101 0110 = 0x0c2248c56
uu  uuaa aaaa  ssss
```

Unit number: 0x3
Address space number: 0x2
segment number: 0x2
address: 0x48c56

6. I/O BUS INTERFACE.

The SIOC contains a full I/O bus interface. When the SIOC acts as the active part in a bus transfer, the 16 bit 8085 address is expanded through the memory mapping unit. This means that the SIOC has full I/O bus addressing capability. Before an active I/O bus cycle, the SIOC has to set up the desired addresses in the memory mapping unit and enable the access to the I/O bus. (Address Mapping Register)
A memory access in address area 0xc000 to 0xffff will be decoded as a I/O bus access. The decoding circuit sends a request to the I/O bus arbitration circuit. After the arbitration, the SIOC drives the address and control lines in the I/O bus. The address specifies another unit connected to the I/O bus, called the passive unit. The SIOC gets access to the memory of the passive unit and performs a read or write cycle in the specified memory location. When the address mapping register bit AMR(2), ENBI, is set, the SIOC is able to act in a bus transfer as a passive unit.

The following cycles are implemented:

Active cycles: Byte read and write.

Passive cycles: Byte read and write.
Word read and write.
Read modify write.

The available memory seen from the I/O bus is the 64 kbyte RAM.

Note: It is not possible to run programs in the EPROM simultaneously with passive memory cycles in the RAM.

7. SERVICE PORT.

The service port is a asynchronous RS-232-C line. The port consists of an INTEL 8251A USART and RS-232-C receivers/transmitters. The service port is normally used by diagnostics programs. The port is also useful for program development and debuging. The USART signal Rxrdy is connected to the hardware interrupt RST 5.5. The Rxclk and Txclk are wired together and have one of the following values:

9600 x 16 baud
4800 x 16 baud
2400 x 16 baud
1200 x 16 baud

The effective baud rate is programmable. The available speeds are: 9600, 4800, 2400, 1200, 600 and 300 baud. The RS-232-C signals are connected to a 20 pin header. The signals are:

pin	name	
03	Txd	; Transmitter data.
05	Rxd	; Receiver data.
07	RTS	; Modem signals.
09	CTS	
11	DSR	
14	DTR	

The connector is located in position: C 4,3

Access mode: I/O read and write.
I/O address : 0x60, data.
0x61, control.

8. SERIAL COMMUNICATION INTERFACE.

The serial communication interface contain eight channels. The first six channels support the asyncronous RS-232-C interface standard. The last two channels support the asyncronous/syncronous RS-232-C or the RS-422 interface standard.

All eight channels are built around the USART; INTEL 8251. For further information about this LSI device, see the data sheet.
Interrupt handling is described in section 11. INTERRUPT.

Channel(0):

USART(0), INTEL 8251.
Access mode: I/O read and write.
I/O address: 0x50, data.
0x51, control.
Transmitter and receiver clocks are supplied by counter(0,0).

Channel(1):

USART(1), INTEL 8251.
Access mode: I/O read and write.
I/O address: 0x52, data.
0x53, control.
Transmitter and receiver clocks are supplied by counter(0,1).

Channel(2):

USART(2), INTEL 8251.
Access mode: I/O read and write.
I/O address: 0x54, data.
0x55, control.
Transmitter and receiver clocks are supplied by counter(0,2).

Channel(3):

USART(3), INTEL 8251.
Access mode: I/O read and write.

I/O address: 0x56, data.
0x57, control.
Transmitter and receiver clocks are supplied by counter(1,0).

Channel(4):

USART(4), INTEL 8251.
Access mode: I/O read and write.
I/O address: 0x58, data.
0x59, control.
Transmitter and receiver clocks are supplied by counter(1,1).

Channel(5):

USART(5), INTEL 8251.
Access mode: I/O read and write.
I/O address: 0x5A, data.
0x5B, control.
Transmitter and receiver clocks are supplied by counter(1,2).

Channel(6):

USART(6), INTEL 8251.
Access mode: I/O read and write.
I/O address: 0x5C, data.
0x5D, control.
Transmitter and receiver clocks are supplied by counter(2,0). It is possible to supply the clocks from the connected peripheral.
See section 14. STRAPS.
Choice of RS-232-C or RS-422 interface.

Channel(7):

USART(7), INTEL 8251.
Access mode: I/O read and write.
I/O address: 0x5E, data.
0x5F, control.
Transmitter and receiver clocks are supplied by counter(2,1). It is possible to supply the clocks from the connected peripheral.

See section 14. STRAPS.
Choice of RS-232-C or RS-422 interface.

The INTEL 8251 USARTs are supplied with a clock for internal device timing. The clock speed is 2.5 MHz.

Choice of interface standard.

Channel(6) and channel(7) supports either the RS-232-C or the RS-422 interface standard. The selection of interface standard is programmable, but selection of transmitter/receiver clock source is strapable. The transmitter/receiver clocks can be supplied from a peripheral or from an internal baud rate generator. See section 14. STRAPS. Channel(6) and channel(7) are quite independent.

The selection of interface standard is made with the Communication Mode Register, CMR.

CMR(7:0), Communication Mode Register.
Access mode: I/O write.
I/O address : 0xBE
Upon power up reset: Contents undefined.

CMR(0) : RS-422/RS-232-C.

CMR(0) = 0 : Input to USART(7) from RS-232-C interface.
CMR(0) = 1 : Input to USART(7) from RS-422 interface.

CMR(1) : CTS.

CMR(1) = 0 : If CMR(0) = 1, then the USART(7) input CTS is low.
CMR(1) = 1 : If CMR(0) = 1, then the USART(7) input CTS is connected to the RS-422 signal: Indicator.

CMR(2) : IINTE4, Indicator INTerrupt Enable 4.

CMR(2) = 0 : IINT4 interrupt line is inactive.
CMR(2) = 1 : IINT4 interrupt line is enabled.

CMR(3) : IINTE3, Indicator INTerrupt Enable 3.

CMR(3) = 0 : IINT3 interrupt line is inactive.
CMR(3) = 1 : IINT3 interrupt line is enabled.

CMR(4) : RS-422/RS-232-C.

CMR(4) = 0 : Input to USART(6) from RS-232-C interface.
CMR(4) = 1 : Input to USART(6) from RS-422 interface.

CMR(5) : CTS.

CMR(5) = 0 : If CMR(0) = 1, then the USART(6) input CTS is low.
CMR(5) = 1 : If CMR(0) = 1, then the USART(6) input CTS is connected to the RS-422 signal: Indicator.

CMR(6) : IINTE2, Indicator INTerrupt Enable 2.

CMR(6) = 0 : IINT2 interrupt line is inactive.
CMR(6) = 1 : IINT2 interrupt line is enabled.

CMR(7) : IINTE1, Indicator INTerrupt Enable 1.

CMR(7) = 0 : IINT1 interrupt line is inactive.
CMR(7) = 1 : IINT1 interrupt line is enabled.

Interface signals.

All interface signals are connected to the SIOC back plane. The SIOC back plane is mounted on the rear of the SUPERMAX card cabinet.

The available signals are:

RS-232-C interface.

Channel(0) to Channel (5): Txd, Transmitter data.
Rxd, Receiver data.
RTS, Request to send.
CTS, Clear to send.
DSR, Data set ready.
DTR, Data terminal ready.

Channel(6) and Channel(7): Txd, Transmitter data.
Rxd, Receiver data.
RTS, Request to send.
CTS, Clear to send.
DSR, Data set ready.
DTR, Data terminal ready.
TxC, Transmitter clock.
RxC, Receiver clock.

RS-422 standard.

Channel(6) and Channel(7): T(A), Transmitter data.
T(B), Transmitter data.
R(A), Receiver data.
R(B), Receiver data.
C(A), Control.
C(B), Control.
I(A), Indicator.
I(B), Indicator.
S(A), Signal element timing.
S(B), Signal element timing.

For further information see the manual: "SUPERMAX hardware characteristics".

RS-422 receiver section:

Logical 1 on data circuits: V(A) - V(B) < -0.3 VOLT.

Logical 0 on data circuits: V(A) - V(B) > +0.3 VOLT.

RS-422 transmitter section:

Logical 1 on data circuits: V(A) - V(B) < -2.0 VOLT.

Logical 0 on data circuits: V(A) - V(B) > +2.0 VOLT.

The RS-422 signals is implemented as follows:

T signal is connected to USART output Txd.
R signal is connected to USART input Rxd.
S signal is connected to USART input Txclk and Rxclk.
C signal is connected to USART output DTR.
I signal is connected to USART input DSR and CTS. The CTS signal can be activated in RS-422 mode with the communication mode register.

Four special interrupt lines are implemented. An interrupt can be generated when the indicator signal shifts from low to high or from high to low. See section 11. INTERRUPT.

9. BAUD RATE GENERATORS.

Three INTEL 8253 LSI counters are used to generate clock to the transmitter and receiver clock inputs on USARTS. Each LSI device has one input clock and three output clocks. One counter output is used as real time clock.
All counters are supplied with a basic clock. The speed is 1.25 MHz.
The counters must be programmed to "mode 3" for correct baud rate generation. For further information, see the data sheet.

Counter(0)
Access mode: I/O read and write.
I/O address: 0x80 to 0x83

Counter(1)
Access mode: I/O read and write.
I/O address: 0x84 to 0x87

Counter(2)
Access mode: I/O read and write.
I/O address: 0x88 to 0x8b

Counter outputs:

Each counter has three outputs. Counter(0) channel 0 is called Counter(0,0) etc.

Counter(0,0) is connected to USART(0), Txclk and Rxclk.
Counter(0,1) is connected to USART(1), Txclk and Rxclk.
Counter(0,2) is connected to USART(2), Txclk and Rxclk.

Counter(1,0) is connected to USART(3), Txclk and Rxclk.
Counter(1,1) is connected to USART(4), Txclk and Rxclk.
Counter(1,2) is connected to USART(5), Txclk and Rxclk.

Counter(2,0) is connected to a RS-232-C and a RS-422 driver. The drivers supply the two interfaces with clock signals; Txclk, Rxclk and Signal element timing. The USART(6) is supplied with this internal generated clock or with a clock from a connected peripheral. See section 14. STRAPS.

Counter(2,1) is connected to a RS-232-C and a RS-422 driver. The drivers supply the two interfaces with clock signals; Txclk, Rxclk and Signal element timing. The USART(7) is supplied with this internal generated clock or with a clock from a connected peripheral. See section 14. STRAPS.

Counter(2,2) is connected to the INTEL 8085 hardware interrupt RST7.5.

10. PARALLEL PRINTER PORT.

The parallel printer port is a simple "CENTRONICS" compatible interface. The interface uses the following signals:

DBC(7:0),	8 bit parallel data.	Output from the SIOC.
DS	, Data strobe.	Output from the SIOC.
ACK	, Acknowledge.	Input to the SIOC.
BUSY	, Busy.	Input to the SIOC.

The interface consist of a data register and some control logic.

CDR(7:0), Centronics Data Register.
Access mode: I/O write.
I/O address : 0xBD

CDR(0) : DATA(0).

CDR(0) = 0 : Centronics bus signal DBC(0) is low.
CDR(0) = 1 : Centronics bus signal DBC(0) is high.

CDR(1) : DATA(1).

CDR(1) = 0 : Centronics bus signal DBC(1) is low.
CDR(1) = 1 : Centronics bus signal DBC(1) is high.

CDR(2) : DATA(2).

CDR(2) = 0 : Centronics bus signal DBC(2) is low.
CDR(2) = 1 : Centronics bus signal DBC(2) is high.

CDR(3) : DATA(3).

CDR(3) = 0 : Centronics bus signal DBC(3) is low.
CDR(3) = 1 : Centronics bus signal DBC(3) is high.

CDR(4) : DATA(4).

CDR(4) = 0 : Centronics bus signal DBC(4) is low.
CDR(4) = 1 : Centronics bus signal DBC(4) is high.

CDR(5) : DATA(5).

CDR(5) = 0 : Centronics bus signal DBC(5) is low.
CDR(5) = 1 : Centronics bus signal DBC(5) is high.

CDR(6) : DATA(6).

CDR(6) = 0 : Centronics bus signal DBC(6) is low.
CDR(6) = 1 : Centronics bus signal DBC(6) is high.

CDR(7) : DATA(7).

CDR(7) = 0 : Centronics bus signal DBC(7) is low.
CDR(7) = 1 : Centronics bus signal DBC(7) is high.

The control logic activates the data strobe signal each time data is written into the CDR. The data strobe signal is a pulse. The printer answers each data transfer with the ACK signal and perhaps with the BUSY signal. The control logic decodes these two status lines to one printer busy line. (The ACK signal is a puls) The busy line is called PBUSY. The status of PBUSY can be read in the ESR register. See section 12. The status of the PBUSY line is undefined upon power up reset. The polarity of the three status lines is strapable. See section 14. STRAPS.

The time from data valid to data strobe activ is minimum 0,9 micro sec.

The data strobe width is minimum 1,4 micro sec.

It is posible to change the timing with two resistors/capacitors.

11. INTERRUPT.

The five hardware interrupt inputs provided in the 8085 are used. The general purpose INTR line causes the CPU to fetch an externally placed instruction on the data bus. The instruction is placed by an interrupt and priority unit. The instructions are RST7, RST6....RST0. RST0 has first priority.

External interrupts.

An external interrupt is generated when a unit on the I/O bus performs an active write cycle in the local memory. A specific memory area is used for this purpose. The area is 0x0080 to 0x00FF. The area consists of 8 blocks, each 16 bytes. Total 128 bytes. An active write cycle in block zero, 0x0080 to 0x008F, will activate the INTR line and a RST0 instruction is executed. The interrupt program has to clear this interrupt before enabling new interrupts. The RST0 interrupt is cleared by execution of the instruction OUT 00. A RST1 interrupt is cleared with an OUT 01 instruction etc. The active write cycles that

cause an interrupt are: Byte write, word write or a read modify write cycle.

The interrupt unit includes a mask register. With the mask register it is possible to mask out one or several of the eight interrupt levels.

IMR(7:0), Interrupt Mask Register.

Access mode: I/O write.
I/O address : 0xB8
Upon power up reset: Contents undefined.

IMR(0) = 1 : Interrupt level 7 enabled.
IMR(0) = 0 : Interrupt level 7 disabled.

IMR(1) = 1 : Interrupt level 6 enabled.
IMR(1) = 0 : Interrupt level 6 disabled.

IMR(2) = 1 : Interrupt level 5 enabled.
IMR(2) = 0 : Interrupt level 5 disabled.

IMR(3) = 1 : Interrupt level 4 enabled.
IMR(3) = 0 : Interrupt level 4 disabled.

IMR(4) = 1 : Interrupt level 3 enabled.
IMR(4) = 0 : Interrupt level 3 disabled.

IMR(5) = 1 : Interrupt level 2 enabled.
IMR(5) = 0 : Interrupt level 2 disabled.

IMR(6) = 1 : Interrupt level 1 enabled.
IMR(6) = 0 : Interrupt level 1 disabled.

IMR(7) = 1 : Interrupt level 0 enabled.
IMR(7) = 0 : Interrupt level 0 disabled.

Internal interrupts.

The internal interrupts use three hardware interrupt lines provided on the 8085 and the general purpose interrupt unit, RST0 to RST7. The interrupt lines are: TRAP, RST7.5, RST6.5 and INTR.

Timer interrupt.

The timer interrupt uses the RST7.5 hardware interrupt. The timer frequency is programmable. See section 9. BAUD RATE GENERATORS.

Service port interrupt.

The service port uses the RST6.5 hardware interrupt. The USART generate interrupts with the Rxrdy signal. The Txrdy signal is not used.

USART interrupt.

Interrupts from the eight USARTs use the general purpose interrupt unit. The USARTs are able to activate the INTR line with the USART signals: Transmitter ready and Receiver ready. (Txrdy and Rxrdy). The eight Rxrdy signals are connected to a receiver mask unit and the eight Txrdy signals are connected to a transmitter mask unit. The masked receiver/transmitter ready signals are connected to two strap sockets. It is possible to connect one or more of the interrupt lines together to one or more interrupt levels. (RST0 to RST7) See section 14. STRAPS.

RMR(7:0), Receiver Mask Register.

Access mode: I/O write.
I/O address : 0xB9
Upon power up reset: Contents undefined.

RMR(0) = 1 : Rxrdy from USART(0) is connected to strap socket 1.
RMR(0) = 0 : Rxrdy from USART(0) is masked out.

RMR(1) = 1 : Rxrdy from USART(1) is connected to strap socket 1.
RMR(1) = 0 : Rxrdy from USART(1) is masked out.

RMR(2) = 1 : Rxrdy from USART(2) is connected to strap socket 1.
RMR(2) = 0 : Rxrdy from USART(2) is masked out.

RMR(3) = 1 : Rxrdy from USART(3) is connected to strap socket 1.
RMR(3) = 0 : Rxrdy from USART(3) is masked out.

RMR(4) = 1 : Rxrdy from USART(4) is connected to strap socket 1.
RMR(4) = 0 : Rxrdy from USART(4) is masked out.

RMR(5) = 1 : Rxrdy from USART(5) is connected to strap socket 1.
RMR(5) = 0 : Rxrdy from USART(5) is masked out.

RMR(6) = 1 : Rxrdy from USART(6) is connected to strap socket 1.
RMR(6) = 0 : Rxrdy from USART(6) is masked out.

RMR(7) = 1 : Rxrdy from USART(7) is connected to strap socket 1.
RMR(7) = 0 : Rxrdy from USART(7) is masked out.

TMR(7:0), Transmitter mask Register.

Access mode: I/O write.
I/O address : 0xBA
Upon power up reset: Contents undefined.

TMR(0) = 1 : Txrdy from USART(0) is connected to strap socket 2.
TMR(0) = 0 : Txrdy from USART(0) is masked out.

TMR(1) = 1 : Txrdy from USART(1) is connected to strap socket 2.
TMR(1) = 0 : Txrdy from USART(1) is masked out.

TMR(2) = 1 : Txrdy from USART(2) is connected to strap socket 2.
TMR(2) = 0 : Txrdy from USART(2) is masked out.

TMR(3) = 1 : Txrdy from USART(3) is connected to strap socket 2.
TMR(3) = 0 : Txrdy from USART(3) is masked out.

TMR(4) = 1 : Txrdy from USART(4) is connected to strap socket 2.
TMR(4) = 0 : Txrdy from USART(4) is masked out.

TMR(5) = 1 : Txrdy from USART(5) is connected to strap socket 2.
TMR(5) = 0 : Txrdy from USART(5) is masked out.

TMR(6) = 1 : Txrdy from USART(6) is connected to strap socket 2.
TMR(6) = 0 : Txrdy from USART(6) is masked out.

TMR(7) = 1 : Txrdy from USART(7) is connected to strap socket 2.
TMR(7) = 0 : Txrdy from USART(7) is masked out.

RS-422 indicator interrupt.

It is possible to generate an interrupt when the indicator signal is switched from one level to another. The four indicator interrupts use the general purpose interrupt unit. (RST0 to RST7)

Channel(6) indicator signal:

IINT1 : Active when a transition from logical 1 to 0 is detected.
IINT2 : Active when a transition from logical 0 to 1 is detected.

Channel(7) indicator signal:

IINT3 : Active when a transition from logical 1 to 0 is detected.
IINT4 : Active when a transition from logical 0 to 1 is detected.

The four interrupt lines are connected to a strap socket. It is possible to connect one or more of the interrupt lines together to one or more interrupt levels. (RST0 to RST7) See section 14. STRAPS.

Interrupts are enabled and disabled with the communication mode register.

CMR(7:0), Communication Mode Register.
Access mode: I/O write.
I/O address : 0xBE
Upon power up reset: Contents undefined.

CMR(0) : RS-422/RS-232-C.

CMR(0) = 0 : Input to USART(7) from RS-232-C interface.
CMR(0) = 1 : Input to USART(7) from RS-422 interface.

CMR(1) : CTS.

CMR(1) = 0 : If CMR(0) = 1, then the USART(7) input CTS is low.
CMR(1) = 1 : If CMR(0) = 1, then the USART(7) input CTS is connected to the RS-422 signal: Indicator.

CMR(2) : IINTE4, Indicator INTerrupt Enable 4.

CMR(2) = 0 : IINT4 interrupt line is inactive.
CMR(2) = 1 : IINT4 interrupt line is enabled.

CMR(3) : IINTE3, Indicator INTerrupt Enable 3.

CMR(3) = 0 : IINT3 interrupt line is inactive.
CMR(3) = 1 : IINT3 interrupt line is enabled.

CMR(4) : RS-422/RS-232-C.

CMR(4) = 0 : Input to USART(6) from RS-232-C interface.
CMR(4) = 1 : Input to USART(6) from RS-422 interface.

CMR(5) : CTS.

CMR(5) = 0 : If CMR(4) = 1, then the USART(6) input CTS is low.
CMR(5) = 1 : If CMR(4) = 1, then the USART(6) input CTS is connected to the RS-422 signal: Indicator.

CMR(6) : IINTE2, Indicator INTerrupt Enable 2.

CMR(6) = 0 : IINT2 interrupt line is inactive.
CMR(6) = 1 : IINT2 interrupt line is enabled.

CMR(7) : IINTE1, Indicator INTerrupt Enable 1.

CMR(7) = 0 : IINT1 interrupt line is inactive.
CMR(7) = 1 : IINT1 interrupt line is enabled.

RS-422 receiver section:

Logical 1 on data circuits: V(A) - V(B) < -0.3 VOLT.

Logical 0 on data circuits: V(A) - V(B) > +0.3 VOLT.

Error detection interrupt.

The error detection hardware uses the non-maskable interrupt line, TRAP. There are eight different interrupt sources. The sources are described later in this manual. The status from the eight sources can be read in the error status register, ESR.

ESR(7:0), Error Status Register.
Access mode: I/O read.
I/O address : 0x70.

ESR(0) : TOUT, Time OUT.

ESR(0) = 1 : Time-out.
ESR(0) = 0 : No time-out.

ESR(1) : BEO, BusError Out.

ESR(1) = 1 : Bus error out.
ESR(1) = 0 : No bus error out.

ESR(2) : BEI, Bus error In.

ESR(2) = 1 : Bus error in.
ESR(2) = 0 : No bus error in.

ESR(3) : PER, Parity ERror.

ESR(3) = 1 : Parity error.
ESR(3) = 0 : No parity error.

ESR(4) : ERROR, ERROR signal in I/O bus.

ESR(4) = 1 : Error signal in bus active.
ESR(4) = 0 : Error signal in bus inactive.

ESR(5) : IERROR, Internal ERROR signal.

ESR(5) = 1 : The SIOC has activated the ERROR signal.
ESR(5) = 0 : No error.

ESR(7) : PBUSY, BUSY signal from parallel printer interface.

ESR(7) = 1 : Printer is busy.
ESR(7) = 0 : Printer is ready.

ESR(6) is not used.

Notice that it is possible to force a non-maskable TRAP interrupt with a switch connected to strap socket 1.

12. ERROR DETECTING AND HANDLING CIRCUIT.

General description.

Time-out.

Local CPU cycles and active bus cycles are monitored by a time-out circuit. A time-out occurs if the CPU executes a HLT instruction, or if the CPU performs an active bus cycle with an illegal destination address. An illegal address is perhaps an address to an unit which is not present.

Parity error.

A parity bit is generated when a write cycle is made in the local RAM. The parity is checked during all memory read cycles. The parity is generated/checked independent of the type of memory cycle.
(CPU and I/O bus cycles.)

Bus error.

A passive part in a I/O bus cycle is able to answer the active part with one of two signals. If the performed memory cycle is without any errors the answer is DTACK, Data Transfer ACKnowledge. If an error occurs, the passive unit answers with the Bus error signal. The SIOC is able to generate, and to act upon the bus error signal.

Error.

The I/O bus signal ERROR indicates that a unit has detected an internal failure. Upon power up reset the SIOC activates the ERROR signal in the I/O bus. The ERROR signal can be activated or deactivated by the program.

Two registers are used for control and diagnosis of errors.

ECR(7:0), Error Command Register.
Access mode: I/O write.
I/O address : 0xBC.
Upon power up reset ECR(7:0) = 0.

ECR(0) : ETOUT, Enable Time OUT.

ECR(0) = 1 : Enable the time-out circuit.
ECR(0) = 0 : No time-out.

ECR(1) : EBO, Enable Bus error Out.

ECR(1) = 1 : Enable bus error out circuit.
ECR(1) = 0 : No bus error out.

ECR(2) : EBI, Enable Bus error In.

ECR(2) = 1 : Enable bus error in circuit.
ECR(2) = 0 : No reaction on a bus error in.

ECR(3) : EPE, Enable Parity Error.

ECR(3) = 1 : Enable parity checking circuit.
ECR(3) = 0 : No parity check.

ECR(4) : SER, Set ERror.

ECR(4) = X : The transition from 0 to 1 sets the error line with the value specifed in ECR(6).

ECR(6) : ERV, ERror Value.

ECR(6) = 1 : Error signal active.
ECR(6) = 0 : No error.

ECR(5) and ECR(7) are not used.

ESR(7:0), Error Status Register.
Access mode: I/O read.
I/O address : 0x70.

ESR(0) : TOUT, Time OUT.

ESR(0) = 1 : Time-out.
ESR(0) = 0 : No time-out.

ESR(1) : BEO, BusError Out.

ESR(1) = 1 : Bus error out.
ESR(1) = 0 : No bus error out.

ESR(2) : BEI, Bus error In.

ESR(2) = 1 : Bus error in.
ESR(2) = 0 : No bus error in.

ESR(3) : PER, Parity ERror.

ESR(3) = 1 : Parity error.
ESR(3) = 0 : No parity error.

ESR(4) : ERROR, ERROR signal in I/O bus.

ESR(4) = 1 : Error signal in bus active.
ESR(4) = 0 : Error signal in bus inactive.

ESR(5) : IERROR, Inetrnal ERROR signal.

ESR(5) = 1 : The SIOC has activated the ERROR signal.
ESR(5) = 0 : No error.

ESR(7) : PBUSY, BUSY signal from parallel printer interface.

ESR(7) = 1 : Printer is busy.
ESR(7) = 0 : Printer is ready.

ESR(6) is not used.

Time out:

Detection: 1. ECR(0) = 1.
2. Active I/O bus cycle is too long.
3. Internal memory cycle is too long.
4. Passive I/O bus cycle in the local memory is too long.

Reaction: 1. Error status register bit ESR(0) = 1.
2. A non-maskable interrupt, TRAP, is generated.
3. Indicator led2 is switched on.

Reset: ECR(0) = 0 deactivates the interrupt line, switches the indictor led2 off and sets ESR(0) = 0.

Bus error out:

Detection: 1. ECR(1) = 1.
2. A parity error occurs during a passive bus cycle.

Reaction: 1. Error status register bit ESR(1) = 1.

2. A non-maskable interrupt, TRAP, is generated.
3. Indicator led5 is switched on.

Reset: ECR(1) = 0 deactivates the interrupt line, switches the indicator led5 off, and sets ESR(1) = 0.

Note: Independent of ECR(1), a unit is answered with a bus error if a parity error is detected.

Bus error in:

Detection: 1. ECR(2) = 1.
2. The SIOC receives a bus error during a active bus cycle.

Reaction: 1. Error status register bit ESR(2) = 1.
2. A non-maskable interrupt, TRAP, is generated.
3. Indicator led3 is switched on.

Reset: ECR(0) = 0 deactivates the interrupt line, switches the indicator led3 off and sets ESR(2) = 0.

Note: If ECR(2) = 0 and the SIOC receives a bus error, the SIOC accepts the data without any warning.

Parity error:

Detection: 1. ECR(3) = 1.
2. Parity error during a memory cycle.
3. The ERROR signal is deactivated by the SIOC.

Reaction: 1. Error status register bit ESR(3) = 1.
2. An internal reset signal is generated. This means that the boot prom is enabled, and access to and from the I/O bus is disabled.
3. A non-maskable interrupt, TRAP, is generated during the first executed instruction in the boot prom.
4. Indicator led4 is switched on.
5. The ERROR signal is activated.

Reset: The ERROR signal and ECR(5) are deactivated by ECR(4) and ECR(6).

Note: The programmer has to deactivate the ERROR signal before enable of the parity error checking circuit. If a main CPU activates the ERROR RESET signal, the ERROR signal is deactivated.

13. INDICATOR LEDS.

Five red light emitting diodes are used to indicate errors and special status.

LED1.

On: The boot prom is enabled.
Off: The boot prom is disabled.
Upon power up: The LED1 is on.

LED2.

On: A time out is pending.
Off: No time out.
Upon power up: The LED2 is off.

LED3.

On: A bus error is received.
Off: No bus error.
Upon power up: The LED3 is off.

LED4.

On: The ERROR line is active. The error line is set by the program or becaurse of parity error.
Off: No error.
Upon power up: The LED4 is on.

LED5.

On: The SIOC has answered with a bus error.
Off: No error.
Upon power up: The LED5 is off.

14. STRAPS.

Strap socket 1.

Function: USART interrupt, Rxrdy.

Position: A 2,10
Name : A6

	1.		
Rxrdy(0)	*	*	RST0
Rxrdy(1)	*	*	RST1
Rxrdy(2)	*	*	RST2
Rxrdy(3)	*	*	RST3
Rxrdy(4)	*	*	RST4
Rxrdy(5)	*	*	RST5
Rxrdy(6)	*	*	RST6
Rxrdy(7)	*	*	RST7

Strap socket 2.

Function: USART interrupt, Txrdy.

Position: A 1,10
Name : A7

	1.		
Txrdy(0)	*	*	RST0
Txrdy(1)	*	*	RST1
Txrdy(2)	*	*	RST2
Txrdy(3)	*	*	RST3
Txrdy(4)	*	*	RST4
Txrdy(5)	*	*	RST5
Txrdy(6)	*	*	RST6
Txrdy(7)	*	*	RST7

Strap socket 3.

Function: RS-422 Indicator interrupt.

Position: A 1,9
Name : A8

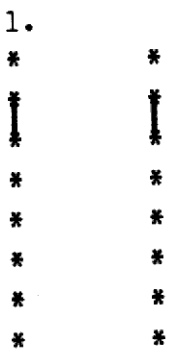
```
          1.
IINT1     *       *  RST7
IINT1     *       *  RST6
IINT2     *       *  RST5
IINT2     *       *  RST4
IINT3     *       *  RST3
IINT3     *       *  RST2
IINT4     *       *  RST1
IINT4     *       *  RST0
```

Strap socket 4.

Function: Possible to connect two switches: One is able to generate an internal reset pulse and the other is able to generate a hardware interrupt. (TRAP)

Position: C 4,1

Under normal circumstances the strap socket is mounted as follows:



Pin 4 to 13 are not used.

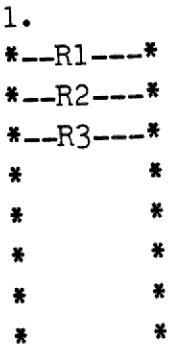
An internal reset pulse is generated if the connection between pin 2 and 3 is removed, and pins 1 and 2 are connected together.

A non-maskable interrupt TRAP is generated if the connection between pin 14 and 15 is removed, and pins 15 and 16 are connected together.

Strap socket 5.

Function: RS-232-C interface for service port.

Position: C 3,3
Name : J4



More service ports may be connected in parallel to a peripheral. Three pull-down resistors must be mounted for correct transmission if only the SIOC is connected to a peripheral.

Strap 1.

Function: Baud rate to service port. Connected to both Txclk and Rxclk.

Position: B 7,1

Jumper	Clock
1	9600 x 16 baud.
2	4800 x 16 baud.
3	2400 x 16 baud.
4	1200 x 16 baud.

Strap 2.

Function: Special option for hardware service.

Position: B 8,3

Under normal circumstances, the jumper must be in position two.

Strap 3.

Function: Polarity of the parallel printer port signal "DATA STROBE".
The data strobe signal is an output signal.
Position: C 3,4
Name : SP2

Jumper	Function
1	Active high data strobe.
2	Active low data strobe.

Strap 4.

Function: Polarity of the parallel printer port signal "BUSY".
The BUSY signal is an input.
Position: C 2,4
Name : SP3

Jumper	Function
1	Active high BUSY signal.
2	Active low BUSY signal.

Strap 5.

Function: Polarity of the parallel printer port signal "ACKNOWLEDGE".
The ACK signal is an input.
Position: C 2,4
Name : SP1

Jumper	Function

1	Active low ACK signal.
2	Active high ACK signal.

Strap 6.

Function: Transmitter clock to USART(6). RS-232-C interface.

Position: B 6,10
Name : SS1

1	The SIOC drives the RS-232-C interface signal Txclk with baud rate counter(2,0). The clock is an input to USART(6).
2	The RS-232-C interface signal Txclk is an input to USART(6).

Strap 7.

Function: Receiver clock to USART(6). RS-232-C interface.

Position: B 6,10
Name : SS2

Jumper	Function
1	The SIOC drives the RS-232-C interface signal Rxclk with baud rate counter(2,0). The clock is an input to USART(6).
2	The RS-232-C interface signal Rxclk is an input to USART(6).

Strap 8 and 9.

Function: Receiver/transmitter clock to USART(6). RS-422 interface.

Position: B 6,7
Name : SS3 and SS4.

Jumper	Function
1	The SIOC drives the RS-422 interface signal Signal element timing with baud rate counter(2,0). The clock is an input to USART(6).
2	The RS-422 interface signal Signal element timing is an input to USART(6). (Rxclk and Txclk)

Note that SS3 and SS4 jumpers must be in the same position.

Strap 10.

Function: Transmitter clock to USART(7). RS-232-C interface.

Position: B 9,6
Name : ST1

Jumper	Function
1	The SIOC drives the RS-232-C interface signal Txclk with baud rate counter(2,1). The clock is an input to USART(7).
2	The RS-232-C interface signal Txclk is an input to USART(7).

Strap 11.

Function: Receiver clock to USART(7). RS-232-C interface.

Position: B 9,6
Name : ST2

Jumper	Function
1	The SIOC drives the RS-232-C interface signal Rxclk with baud rate counter(2,1). The clock is an input to USART(7).
2	The RS-232-C interface signal Rxclk is an input to USART(7).

Strap 12 and 13.

Function: Receiver/transmitter clock to USART(7). RS-422 interface.

Position: B 6,6
Name : ST3 and ST4.

Jumper	Function
1	The SIOC drives the RS-422 interface signal Signal element timing with baud rate counter(2,1). The clock is an input to USART(7).
2	The RS-422 interface signal Signal element timing is an input to USART(7). (Rxclk and Txclk)

Note that ST3 and ST4 jumpers must be in the same position.

15. INSTALLATION.

All modules in a SUPERMAX computer system differ in some details.

Unit number.

Each intelligent module connected to the common, I/O bus has an unique address. The address is called the unit number. The unit number is coded in a programable device, called a PAL. The PAL is marked with the text SUXX. XX is the decimal unit number. The unit number PAL is located in position A 4,5.

Priority.

The arbitration scheme used in the common, I/O bus is based on fixed priorities. The priority is coded in a PAL. Two units connected to the I/O bus cannot use the same priority. The priority PAL is marked DPXX, where XX is the priority. The SIOC module uses one priority. The PAL is located in position A 1,6.

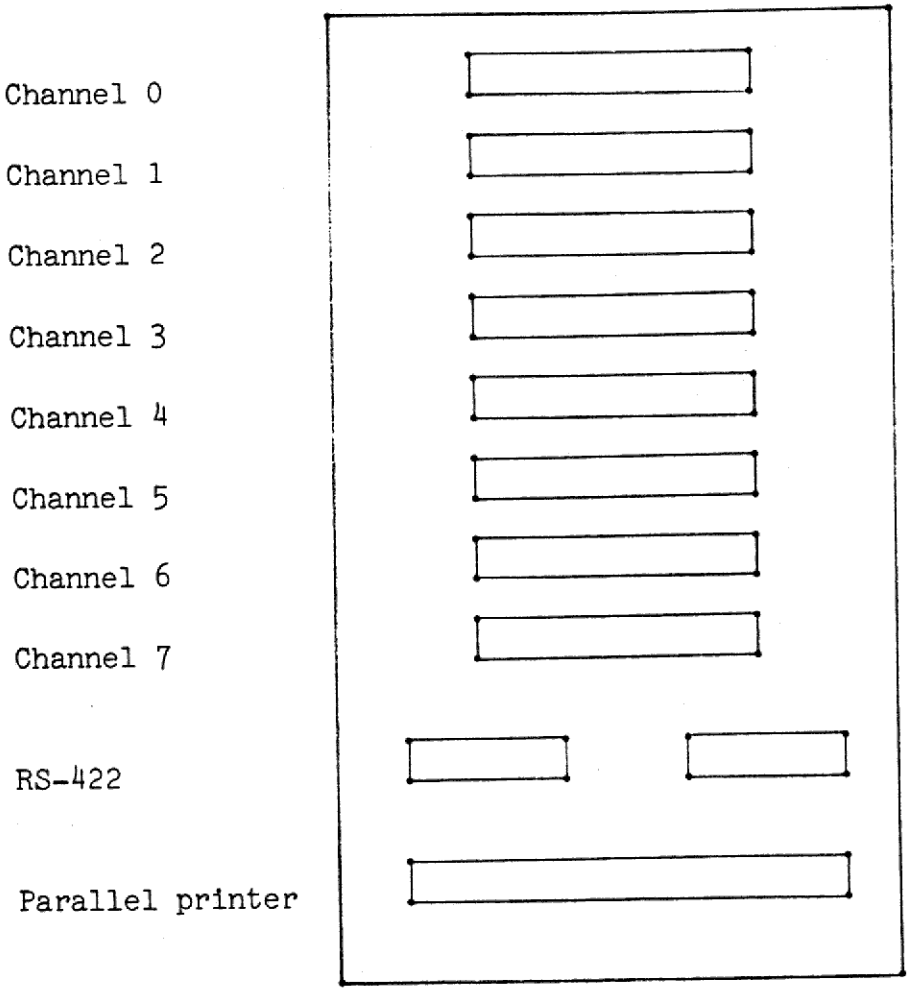
16. CABLES.

The connection between the SIOC module and the SIOC back panel is made with two flat cable connectors. The headers mounted on the PCB are positioned as follows:

RS-232-C signals: C 4,8

RS-422 signals and parallel printer signals: C 2,8

The SIOC back panel is mounted on the rear of the SUPERMAX card cabinet.



SIOC back panel seen from the rear

The connection to the service port is placed in position C 4,3.

17. BOARD SURVEY.