SUPERMAX SYSTEM COURSE.

SUPERMAX OVERVIEW.

I/O BUS SYSTEM.

CPU

SIOC

DIOC

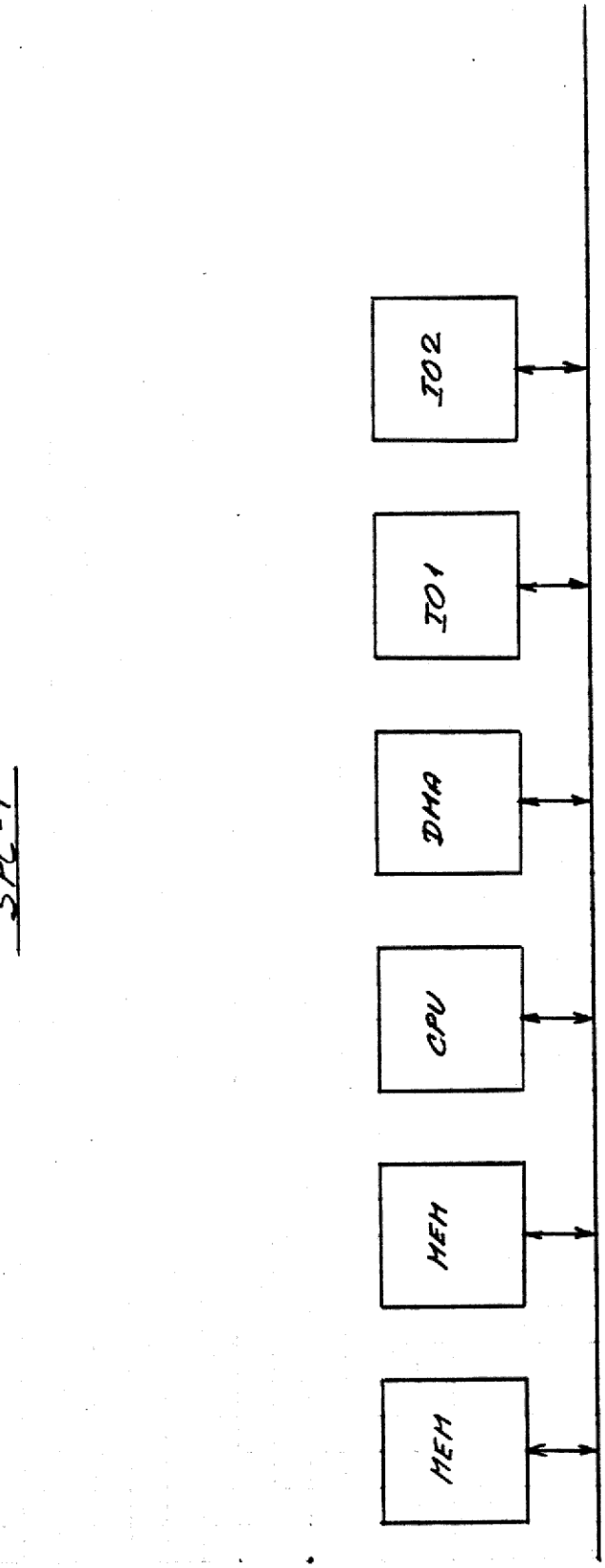
FUTURE IOCS

SERVICE PORT

BOOT PROCEDURE

HOW TO CONFIGURE A SUPERMAX SYSTEM. HANDS ON

SPC-1



SUPERMAX COMPARED TO SPC/1

SIMILARITIES:

1. Modular computer system
2. Expandable computer system

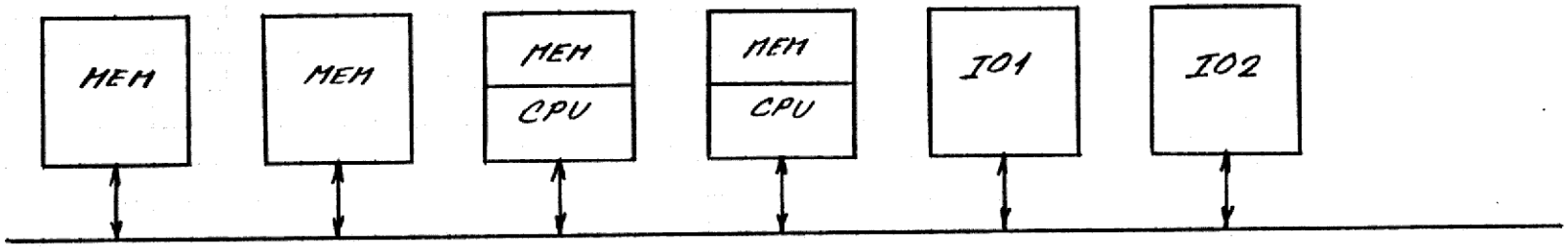
DIFFERENCIES:

1. Multi processor system
2. Intelligent IO controllers, IOCs
3. Organization of main memory
4. Protection features
5. Error correction on main memories
6. Parity check on all IOCs.

TECHNOLOGY:

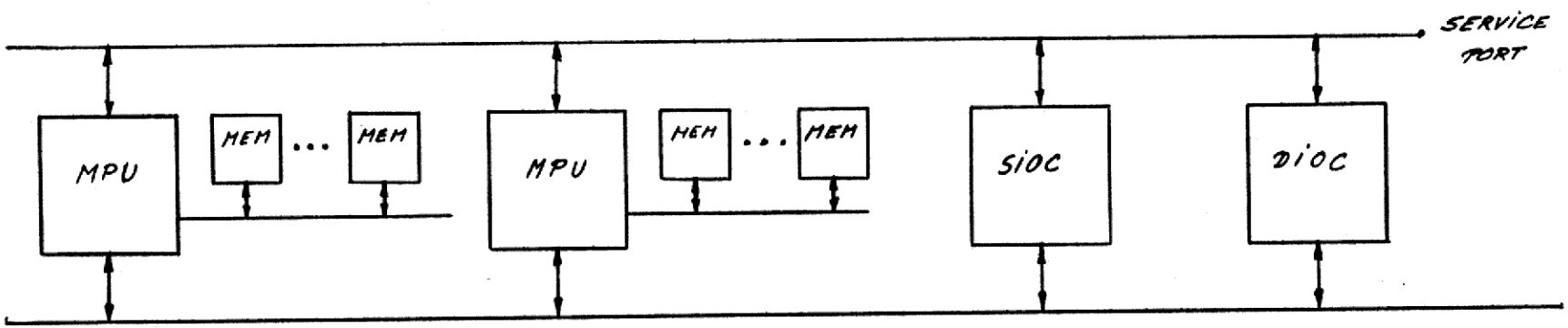
1. Use of PALs
2. Multi layer printed circuit boards.
3. Logic family: 74ALS

Multi master bussystem : Multibus, VME



Problem : Bus overload caused by limited amount of local memory

Supermax



Expandable local memory
I/O Bus used for I/O only

DISK I/O COMMAND.

Ex. program-load from a winchester disk.

The principle is that the CPU intervention in an I/O access is as small as possible.

1. User program (vox, shell etc.) makes an operating system call.

2. The OS builds a disk-command in main memory.

   Command: Read/write
   Disk address
   Destination/source address

3. The DIOC contains a number channels. ("car")
   One or more for each logical disk.

4. The OS makes a reservation of a car area.

5. The OS writes the disk-command address in the car area.

6. The OS writes a byte in the interrupt area.

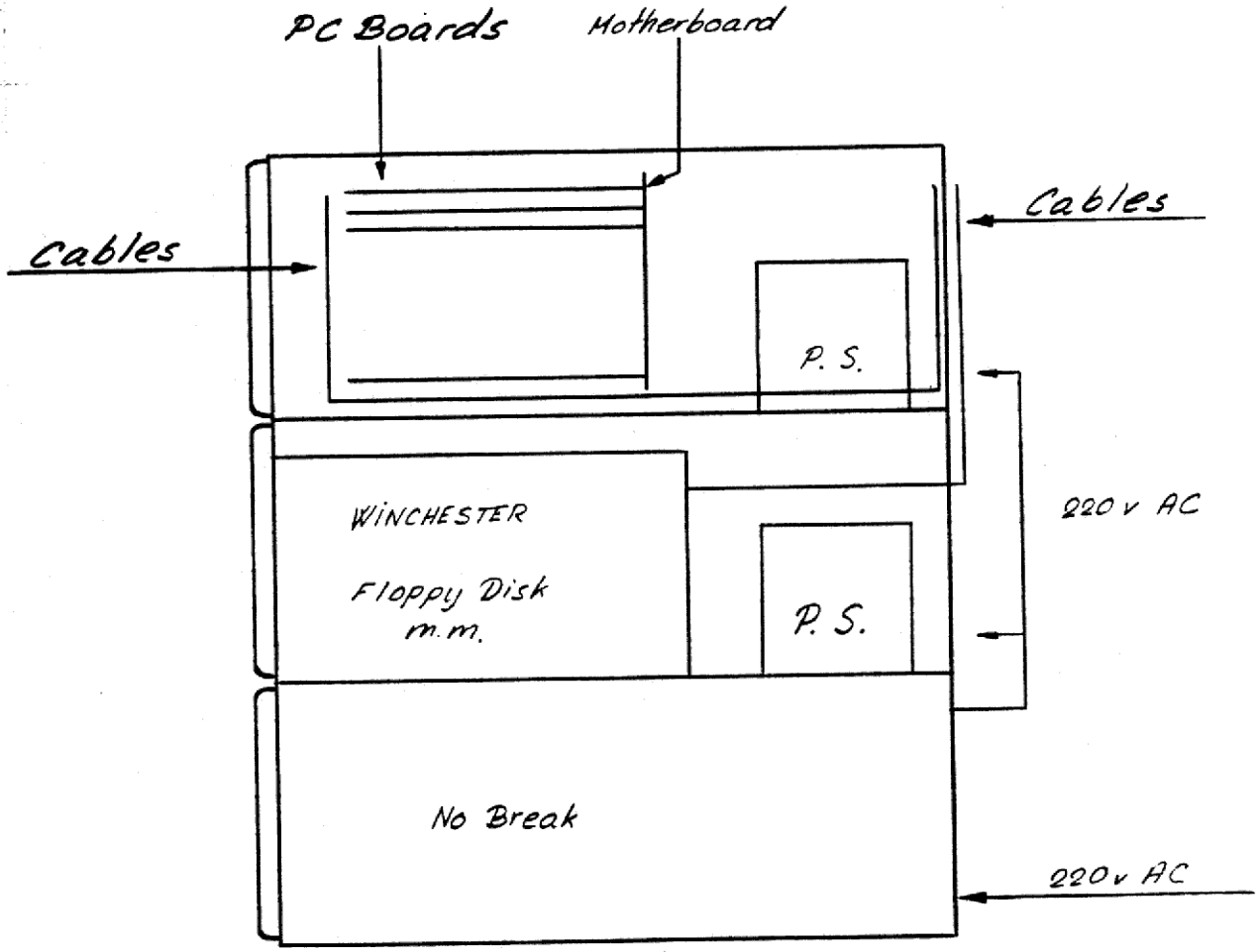
7. Now the DIOC is able to perform the disk transport without any CPU intervention.

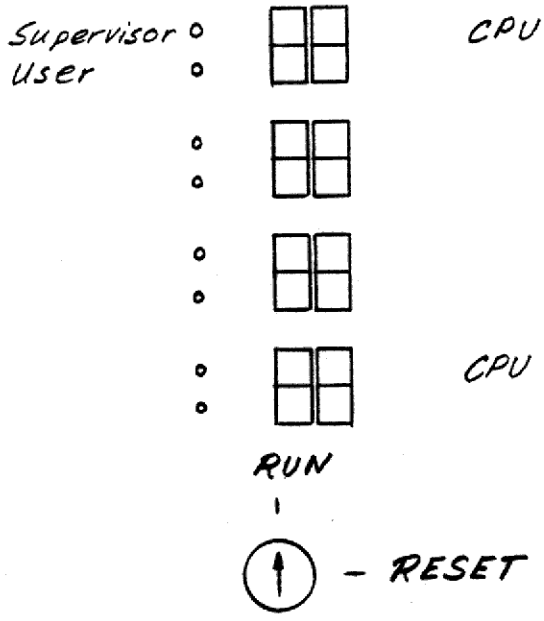
8. After the data transport into the main memory the DIOC completes the command writing three bytes into the main memory.
   1. an I/O result.
   2. a completion signal.
   3. an interrupt byte.

9. The OS checks the load module structure.

10. The program execution can start.

SUPERMAX

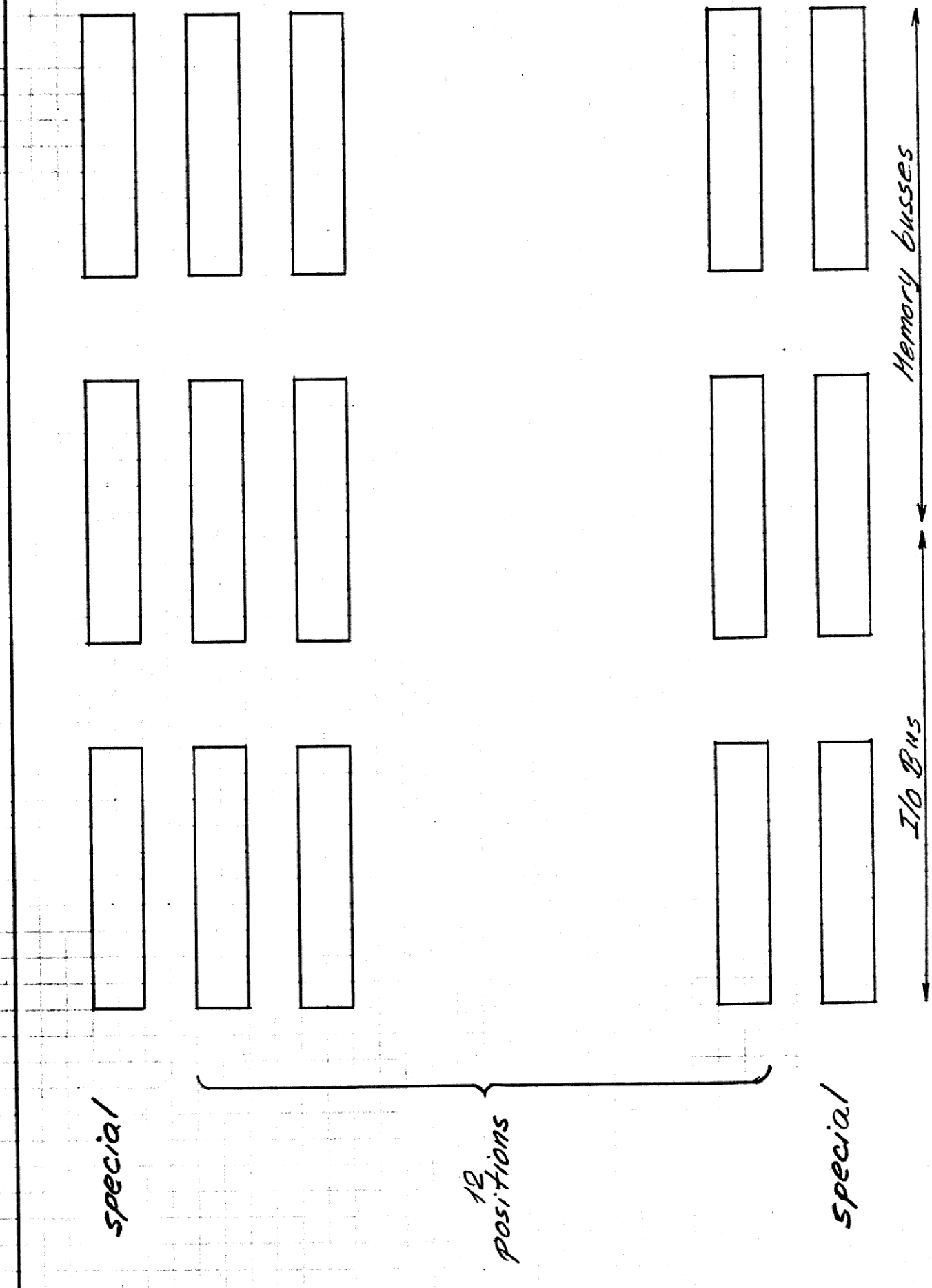

PC Boards
Motherboard
Cables
Cables
P. S.
WINCHESTER
Floppy Disk
m.m.
P. S.
220 v AC
No Break
220v AC

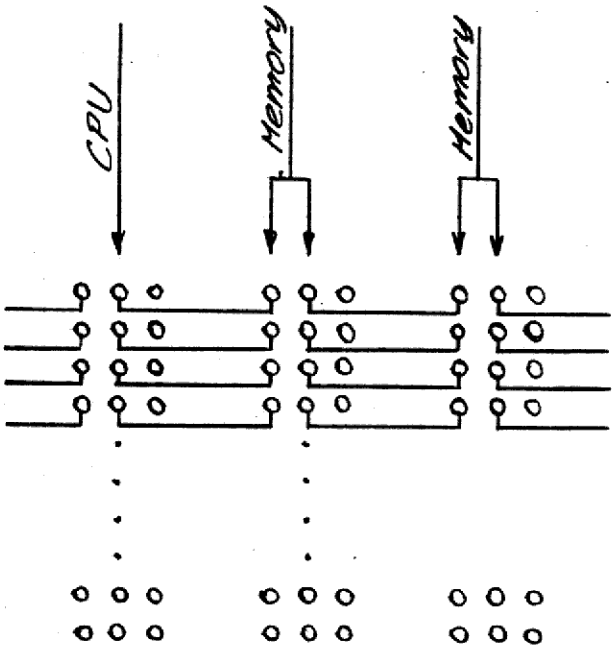

Supervisor
User
CPU 0
CPU 3
RUN
RESET

dansk data elektronik aps

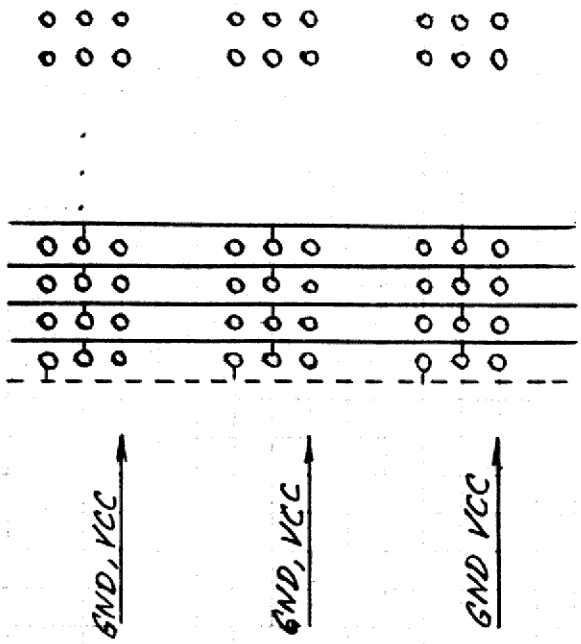
Motherboard

Initialer/dato	Side
KAN 830520	
Revideret	Projekt





Memory Busses



I/O bus

MEMORY BUS

Multiplexed address/data, MB(43:0)

MB(43:0):	DATA(43:0)
MB(23:0):	ADDR(23:1) CON DW

CONTROL SIGNALS:

NM	NO MEMORY
ERD	ENABLE READ DATA
EWD	ENABLE WRITE DATA
RAS	ROW ADDRESS STROBE
ROWEN	ROW ADDRESS ENABLE
CAS	COLUMN ADDRESS STROBE
WP	WRITE PULSE
REF	REFRESH

IO BUS

ADDRESS:

UNIT(3:0)	UNIT NUMBER OF PASSIVE UNIT
ASN(5:0)	ADDRESS SPACE NUMBER
ADDR(23:1)	BYTE ADDRESS

DATA:

DATA(31:0)

CONTROL SIGNALS:

RW	READ/WRITE
AS	ADDRESS STROBE
UDS	UPPER DATA STROBE
LDS	LOWER DATA STROBE
DWS	DOUBLE WORD DATA STROBE
DTACK	DATA TRANSFER ACKNOWLEDGE
BERR	BUS ERROR

ARBITRATION:

BR	BUS REQUEST
SR(4:0)	PRIORITY LINES
BCLOCK	10 MHz BUS CLOCK

SPECIAL:

RESET	RESET SIGNAL
ERROR	
ERROR RESET	
DIAGNOSE	
KEY	
POWER FAIL	POWER FAILURE INTERRUPT
XINT0	INTERRUPT LINE
XINT1	INTERRUPT LINE

SPECIAL SIGNALS IN THE IO BUS.

KEY	Connected to a reset key.
RESET	Generated by CPUs during and after KEY active System reset to all units.
ERROR	Generated by CPUs and IOCs after a fatal hardware or software error. Interrupt input to all CPUs.
ERROR RESET	Generated by CPUs. Reset signal to all units which have activated ERROR.
DIAGNOSE	Generated by CPUs. A CPU which has activated ERROR, is opened for testing by another CPU.

IO BUS CYCLES.

Two units participate in an IO bus cycle:

1. The ACTIVE unit takes the initiative to the IO bus cycle and addresses the other unit, the PASSIVE unit.

2. The PASSIVE unit is accessed from the IO bus. Seen from the IO bus the PASSIVE unit is just a block of memory.

As two or more units may try to access the IO bus simultaneously, an arbitration scheme is used.

An IO bus cycle is divided into two parts:

1. An arbitration cycle.

2. A data transfer cycle.

ARBITRATION BETWEEN FIVE UNITS. (SIMPLIFIED)

Five priority lines, SR(4:0), are used.

SR(4) has the highest priority.

SR(0) has the lowest pririty.

All priority lines are inputs to all five units.

A priority line is driven by one an only one unit.

When a unit wants an access to the IO bus, it activates its priority line.

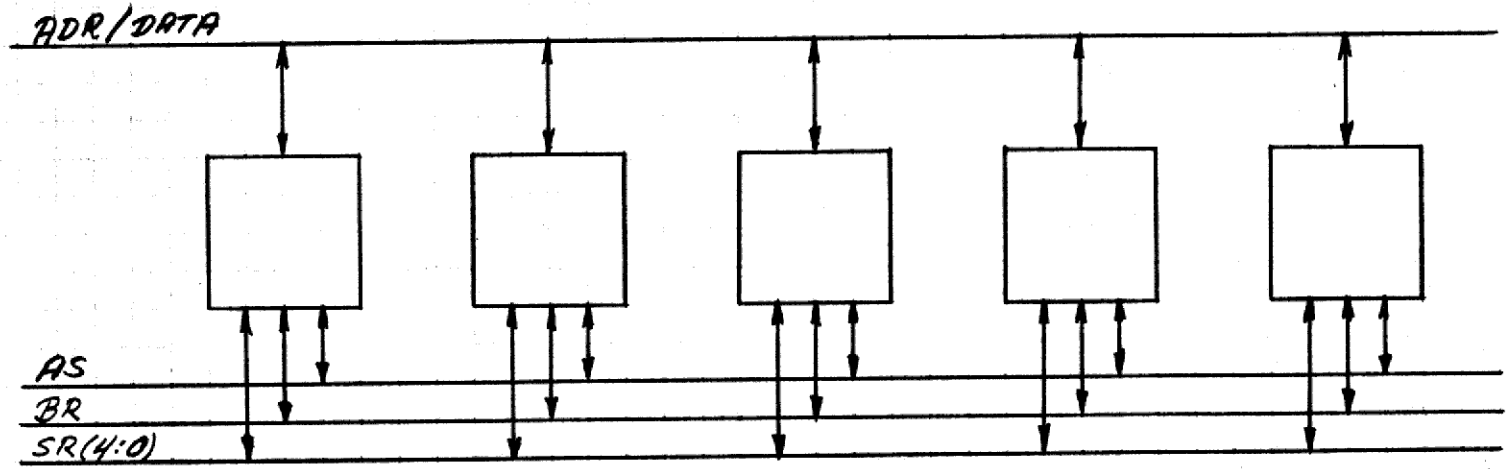
The unit that drives the line with the highest priority takes the IO bus.

EXPANSION TO FIVE TIMES FIVE UNITS.

The arbitration is done in two clock cycles.

A unit has two priorities, one for each clock cycle.

Units that have the highest priority in the first clock cycle participate in the second clock cycle.



A unit has a column priority : 0, 1, 2, 3 or 4
and a row - priority : 0, 1, 2, 3 or 4
} max. 25 priorities

IO BUS ARBITRATION

10 MHZ synchronous arbitration.
Arbitration in two clock cycles.
Arbitration runs in parallel with the data transfer cycle.
Each unit has its own fixed priority.
All units have equal access to the IO bus.
Each unit has its own arbitration logic.

SIGNALS:

AS	IO BUS occupied by data transfer cycle.
BR	Arbitration in progress or finished.
SR(4:0)	Priority lines.

RULES:

1. A unit is allowed to start an arbitration cycle, when BR is inactive.

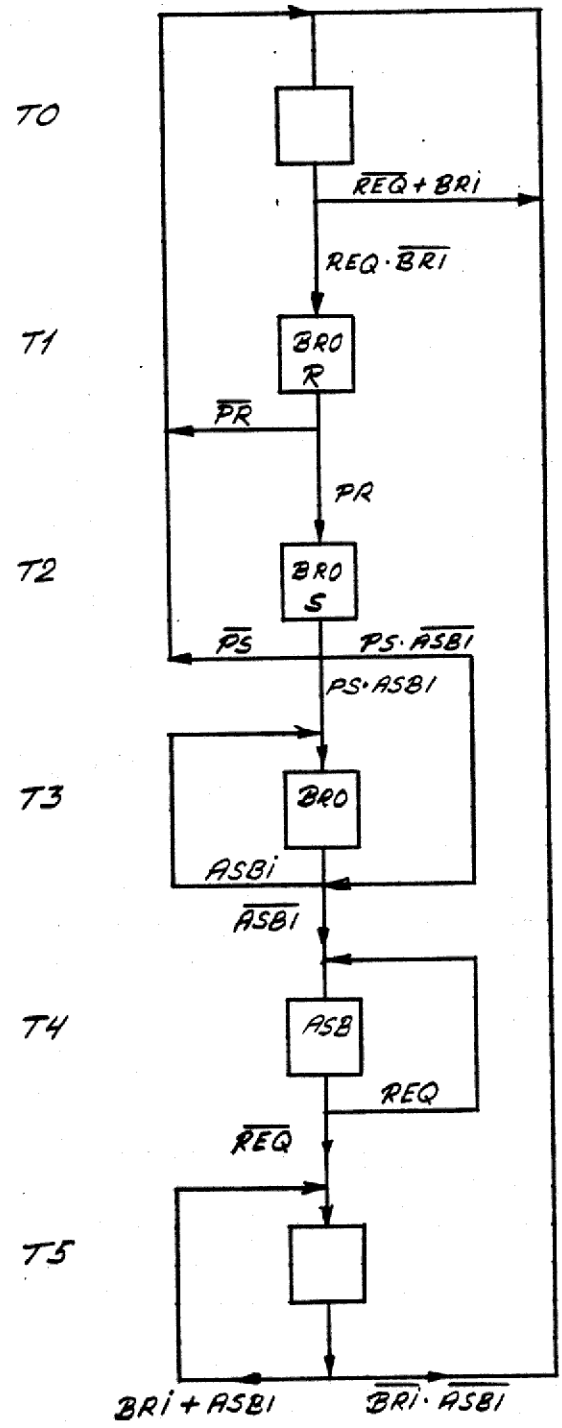
2. The unit that won the arbitration cycle keeps BR active, until it starts its data transfer cycle.

3. The unit that won the arbitration cycle starts its data transfer cycle, when AS is inactive.

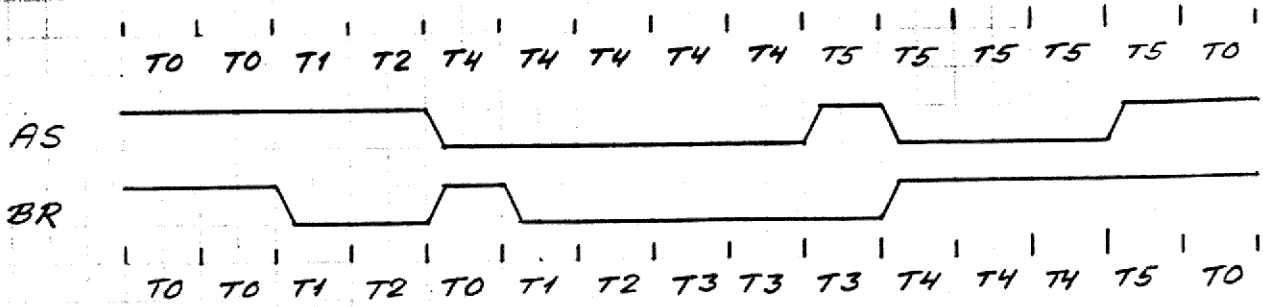
4. A unit that starts its data transfer cycle, activates AS and deactivates BR.

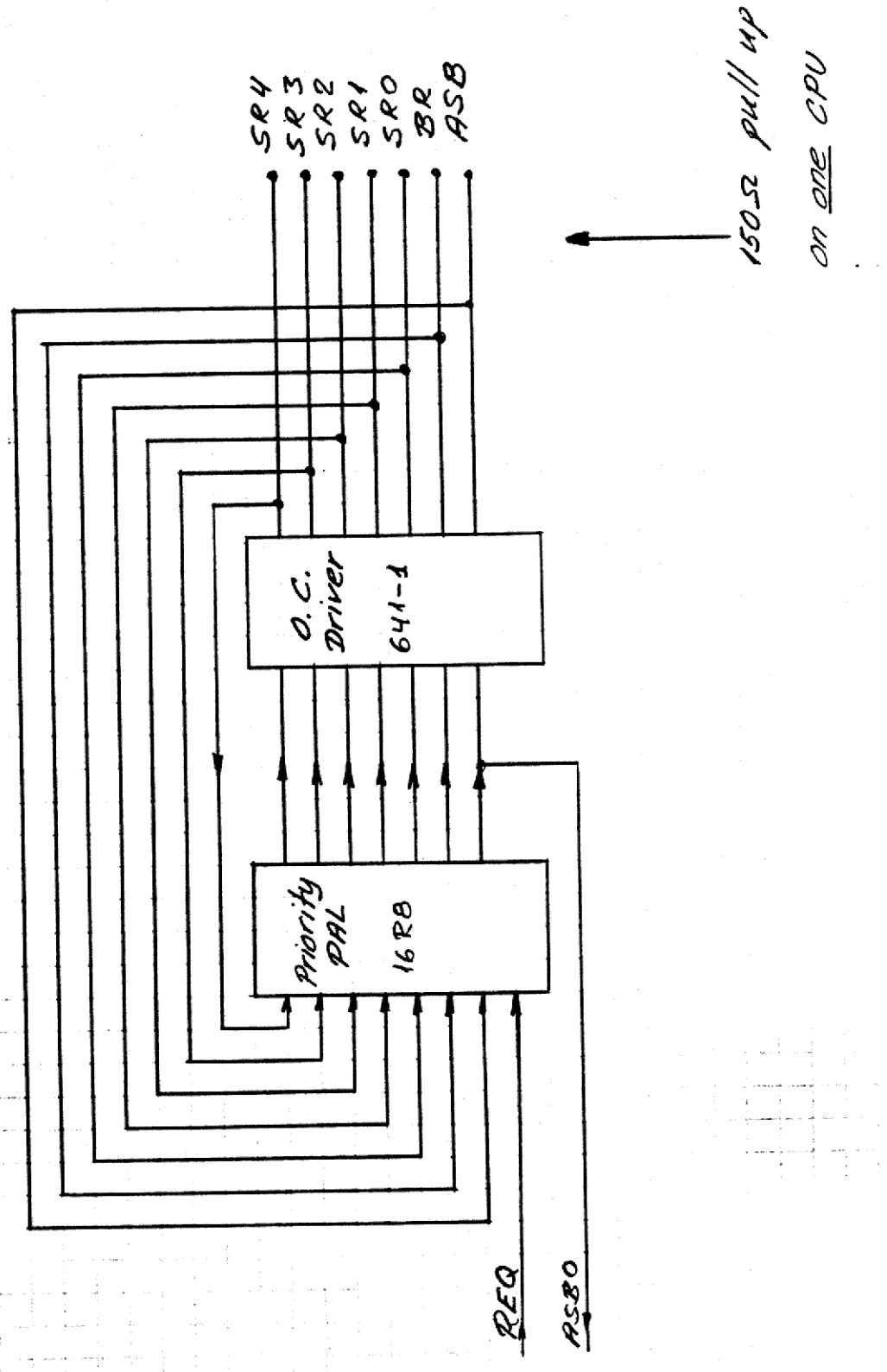
5. A unit terminates its data transfer cycle by deactivating AS.

6. A unit that has executed an IO bus cycle, will only participate in a new arbitration cycle when it sees that the IO bus is completely free, that is when both BR and AS are inactive.



	ASBO	BRO	N	SR4	SR3	SR2	SR1	SR0
T0	0	0	0	0	0	0	0	0
T1	0	1	0	R				
T2	0	1	1	S				
T3	0	1	0	0	0	0	0	0
T4	1	0	0	0	0	0	0	0
T5	0	0	1	0	0	0	0	0




SR4
SR3
SR2
SR1
SR0
BR
ASB
150Ω pull up
on one CPU
O.C. Driver
641-1
Priority PAL
16R8
REQ
ASBO

IO BUS DATA TRANSFER CYCLE.

THE ACTIVE UNIT DRIVES:

UNIT(3:0)
ASN(5:0)
ADDR(23:1)

AS
DWS, UDS, LDS
RW

DATA(31:0) if the cycle is a write cycle.

THE PASSIVE UNIT DRIVES:

DTACK or BERR

DATA(15:0) if the cycle is a read cycle.

If the active unit does not receive DTACK or BERR within 100 us, it terminates the bus cycle by deactivating AS.

IO BUS INTERRUPT.

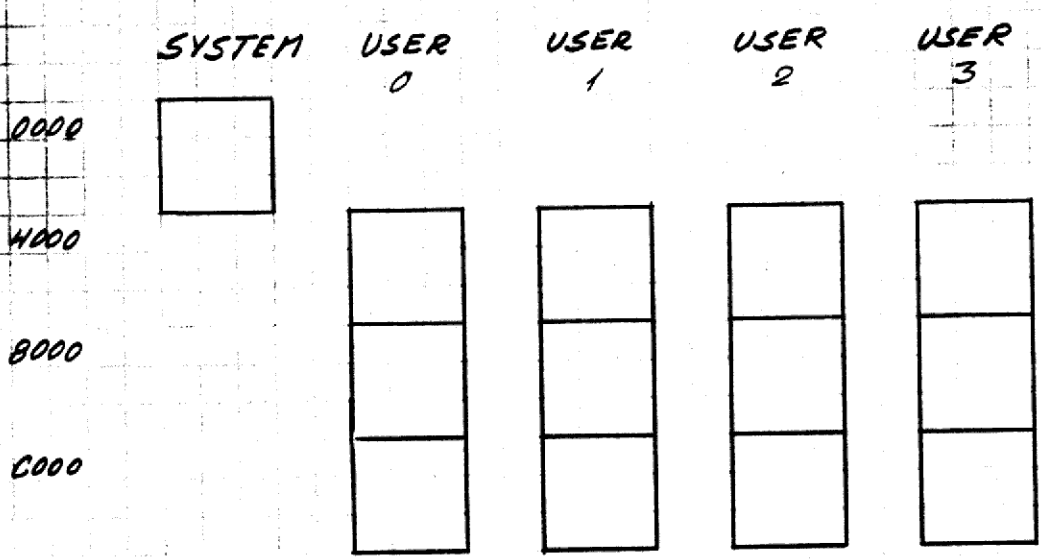
No dedicated wires for interrupt between units.

Interrupt is generated by usual IO bus cycles.

The active unit interrupts the passive unit by writing in a certain part of its main memory.

Hardware in the passive unit decodes the write address and generates the interrupt.

SPC/1 Memory Picture



Bank switching

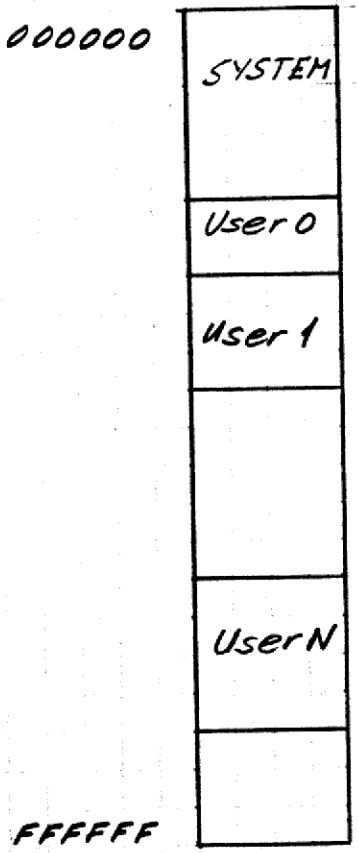
Purpose: Multi user system in 64kb.

Advantage: User programs allways start in 4000.

Disadvantage: Max. 48 kb user programs.
Max 64 kb total.

No memory protection

Linear Memory 0-16 Mb

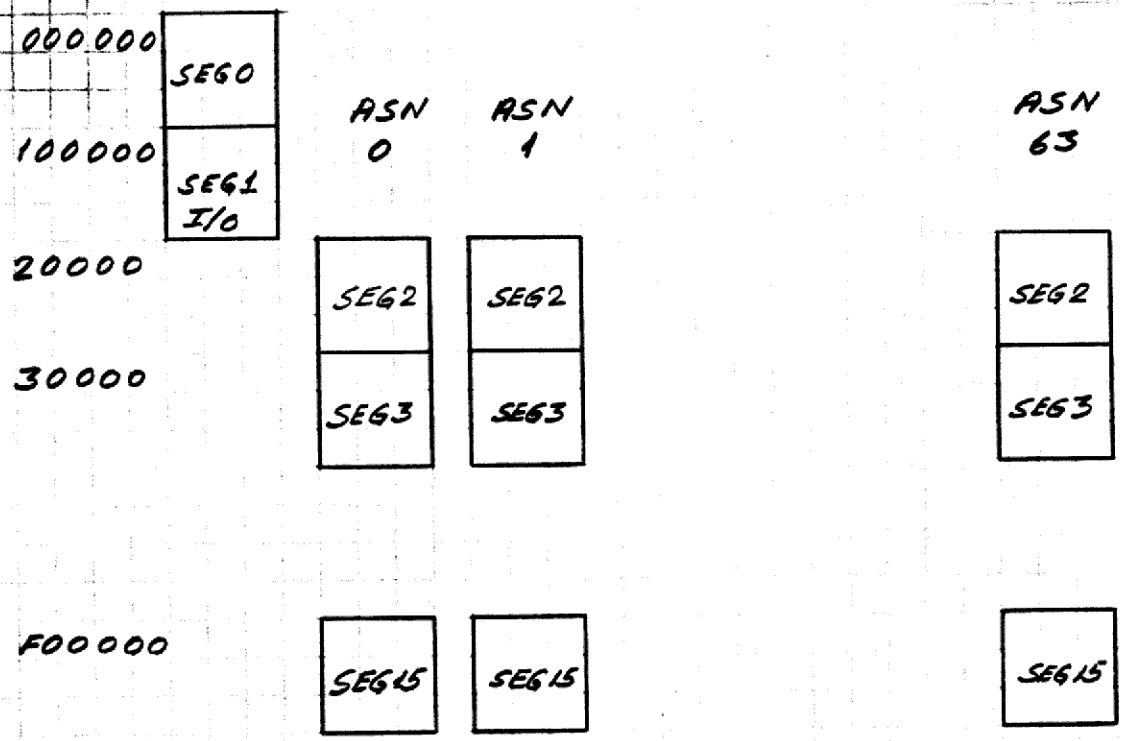


Advantage: Variable user areas

Disadvantage: User programs use different starting addresses.

No obvious scheme for memory protection.

Logical memory in SUPERMAX



64 Address Space Numbers ASN
14 logical segments pr. ASN
Variable physical segment size : 256b - 1Mb

User programs may use the same logical starting address.
Different logical segments can be mapped to the same physical addresses.

Memory Management Unit MMU
Translates logical to physical addresses
Protects the main memory.

Logical address
0
07
19
20
23
0
SEG
ASN
5
Compare
Physical address
Offset
Length
ACC
Segment descriptor
MMU memory

ACCESS CODE ACC(3:0)

ACC(0): IO	Access from IO bus allowed
ACC(1): U	User mode allowed
ACC(2): W	Write allowed
ACC(3): X	Segment descriptor is a part of the logical address used to access the IO bus

Violation of memory protection causes a bus error.

Parity check

P	D2	D1	D0

$P = D2 \oplus D1 \oplus D0$

P1	P0	D2	D1	D0

$P0 = D1 \oplus D0$

$P1 = D2 \oplus D1$

	D2	D1	D0
P0		×	×
P1	×	×	

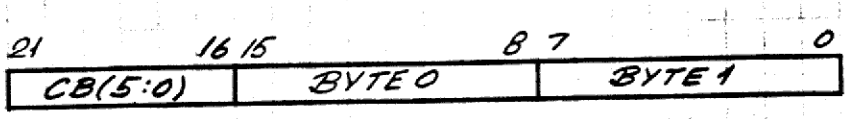
The bit in error is inverted.

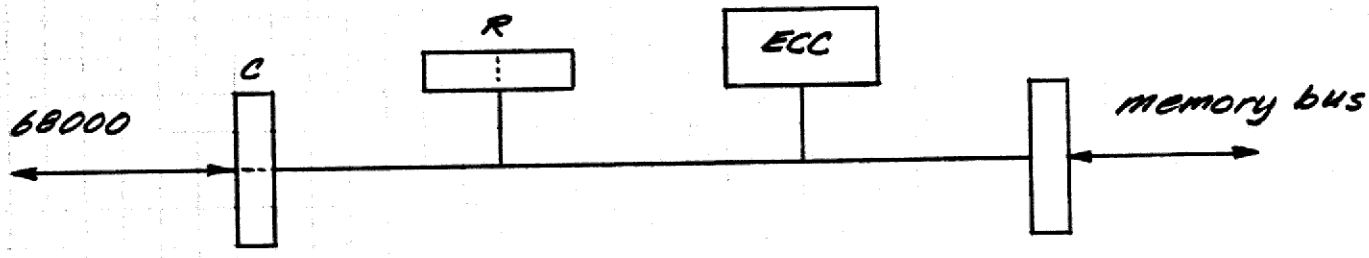
16 bit data word and 6 ECC bits:

All single bit errors are corrected

Double bit errors are detected.

ECC and byte write





Byte write

1. Latch new byte in C.
2. Read word from memory
3. Latch word in ECC and R.

   If error

   Correct data

   Latch corrected data in R.
4. Output new byte from C
5. Output old byte from R
6. Generate check bit
7. Write word in memory.

IO UNITS ON THE CPU MODULE.

ADDRESS		
100XXX:	MMU	16 RW
101000:	Command Register	16 W
101002:	Status Register	16 R
101005:	Error Address	8 R
101006:	Syndrome Bits	16 R
101008:	Interrupt Mask	16 RW
10100A:	Interrupt Pending	16 R
10100D:	Ext. Interrupt Set/Reset.	8 W
101011:	USART Data Register	8 RW
101013:	USART Status/Command	8 RW
101014:	Display Register	16 W
101017:	Address Space Register	8 RW
10102X:	Unit Number	8 bytes read Odd addresses only

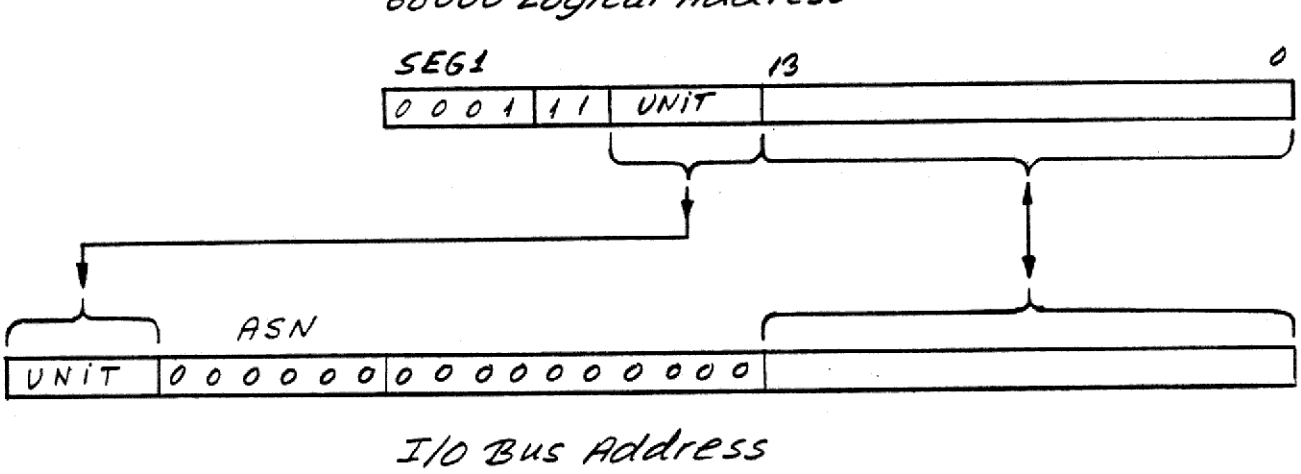
COMMAND REGISTER.

BIT	
15:	Not used
14:	Not used
13:	Not used
12:	Not used
11:	Not used
10:	Error Reset Out. (OC signal in IO bus)
9:	Diagnose out. (OC signal in IO bus)
8:	No Error in Unit.(OC signal in IO bus)
7:	Enable Access to Registers from IO Bus
6:	Disable Boot Loader PROM
5:	Enable Protection against User in SEG 0 and SEG 1.
4:	Enable Error Detection.
3:	Enable Access Code Test
2:	Enable Address Mapping.
1:	Enable Access from IO Bus
0:	Enable Access to IO Bus

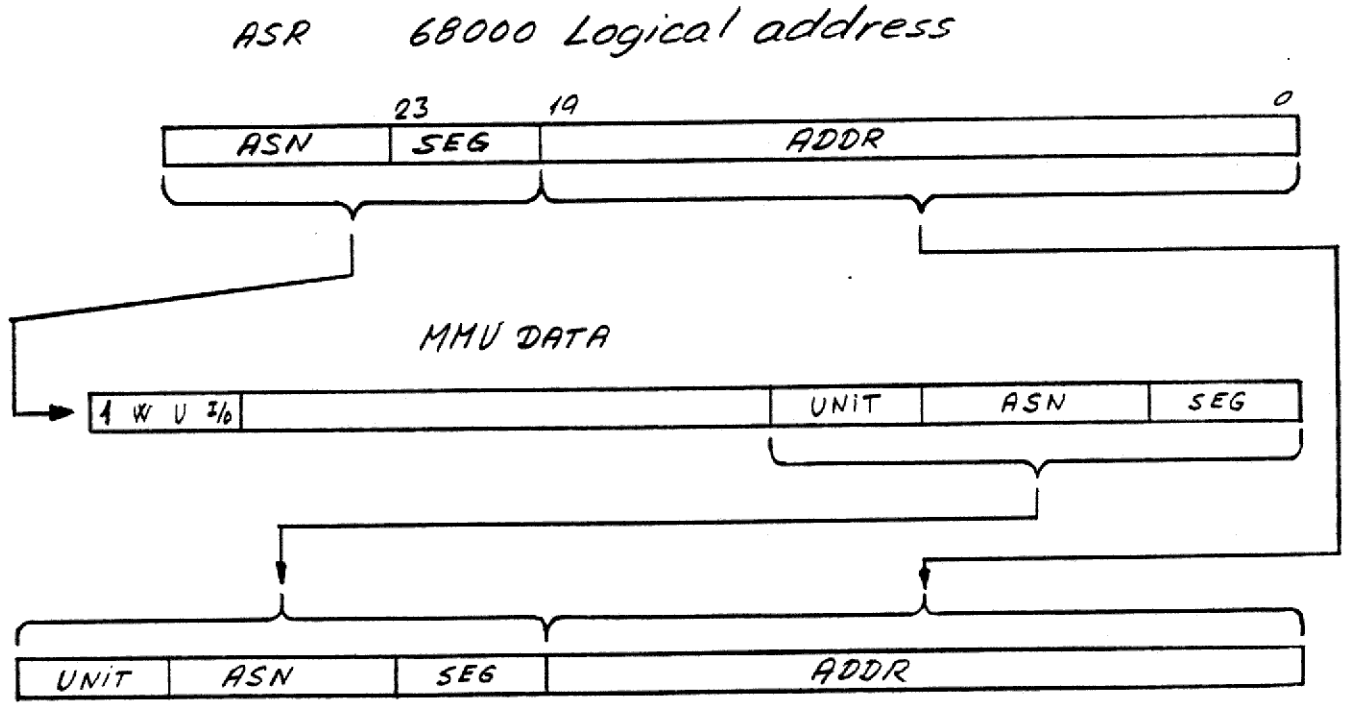
STATUS REGISTER.

BIT	
15:	Not used
14:	Not used
13:	TxRDY Service USART
12:	RxRDY Service USART
11:	Power Loss
10:	Error in Unit
9:	Timer Interrupt
8:	Single Fault in Memory
7:	Double Fault in Memory
6:	Bus Error from IO Bus
5:	No Memory
4:	Time out
3:	Segment too Long
2:	Illegal Write
1:	Illegal Bus
0:	Illegal User

Short access to I/O bus:



Long access to I/O bus:



CPU MODULE INTERRUPT STRAP.

POSITION: Z5

PIN 1: POWER FAILURE	PIN 16: Not used
PIN 2: ERROR IN UNIT	PIN 15: Interrupt level 6
PIN 3: MEMORY VIOLATION	PIN 14: Interrupt level 5
PIN 4: FAULT IN MEMORY	PIN 13: Interrupt level 4
PIN 5: TIMER INTERRUPT	PIN 12: Interrupt level 3
PIN 6: SERVICE PORT	PIN 11: Interrupt level 2
PIN 7: Not used	PIN 10: Interrupt level 1
PIN 8: Not used	PIN 9 : Not used.

CPU MODULE CLOCK STRAP.

POSITION: Z6

PIN 1:	6 Mhz output	PIN 16:	CPU clock input
PIN 2:	8 Mhz output	PIN 15:	CPU clock input
PIN 3:	10 Mhz output	PIN 14:	CPU clock input
PIN 4:	10 Mhz output	PIN 13:	BUS clock input
PIN 5:	12 Mhz output	PIN 12:	BUS clock input
PIN 6:	16 Mhz output	PIN 11:	BUS clock input
PIN 7:	16 Mhz output	PIN 10:	INTERNAL clock input
PIN 8:	20 Mhz output	PIN 9 :	INTERNAL clock input

CPU MODULE TIMER STRAP.

POSITION: Z4

PIN 1: BAUD rate input	PIN 16: 5 ms output
PIN 2: 9600 baud rate output	PIN 15: Interrupt input
PIN 3: 4800 baud rate output	PIN 14: 10 ms output
PIN 4: 2400 baud rate output	PIN 13: 20 ms output
PIN 5: 1200 baud rate output	PIN 12: Interrupt input
PIN 6: 600 baud rate output	PIN 11: 40 ms output
PIN 7: 300 baud rate output	PIN 10: 80 ms output
PIN 8: Not used	PIN 9 : Interrupt input

CPU MODULE INDICATORS.

Front pannel display:

RED diode: Supervisor mode

GREEN diode: User mode

The diodes are set and cleared in each CPU cycle.

Programmable seven segment display. Two digits.

LED on the CPU module:

ON if the CPU module drives the ERROR IN UNIT line, that is:

1. ON after RESET.

2. ON if the CPU enters the HALT state.

The LED is switched off by the program.

CPU MODULE INSTALLATION.

The FIRST CPU module (Unit number 3):

This module drives the BUS CLOCK.

This module contains pull up resistors for various bus signals.

Check CPU TIMER strap position Z4:

PIN 1 and PIN 2 connected: Service USART 9600 baud.
PIN 11 and PIN 12 connected: Timer interrupt 40 ms.

Check CPU INTERRUPT strap position Z5:

PIN 5 and PIN 15 connected: Timer interrupt level 6.

Check CPU CLOCK strap position Z6:

PIN 3 and PIN 14 connceted: CPU clock 10 Mhz.
PIN 2 and PIN 13 connected: BUS clock 8 Mhz.
PIN 7 and PIN 10 connected: INTERNAL clock 16 Mhz.

Check SIL resistors:

Position SI25: 150 ohm
Position SI26: 150 ohm
Position SI27: 1.0 Kohm

Check unit and priority PAL:

Unit PAL position B8: C173
Priority PAL position B9: C163

CPU MODULE INSTALLATION.

NOT THE FIRST CPU MODULE.

Check CPU TIMER strap position Z4:

PIN 1 and PIN 2 connected: Service USART 9600 baud.
PIN 11 and PIN 12 connected: Timer interrupt 40 ms.

Check CPU INTERRUPT strap position Z5:

PIN 5 and PIN 15 connected: Timer interrupt level 6.

Check CPU CLOCK strap position Z6:

PIN 3 and PIN 14 connceted: CPU clock 10 Mhz.
PIN 7 and PIN 10 connected: INTERNAL clock 16 Mhz.

Check SIL resistors:

Position SI25: Not installed.
Position SI26: Not installed.
Position SI27: Not installed.

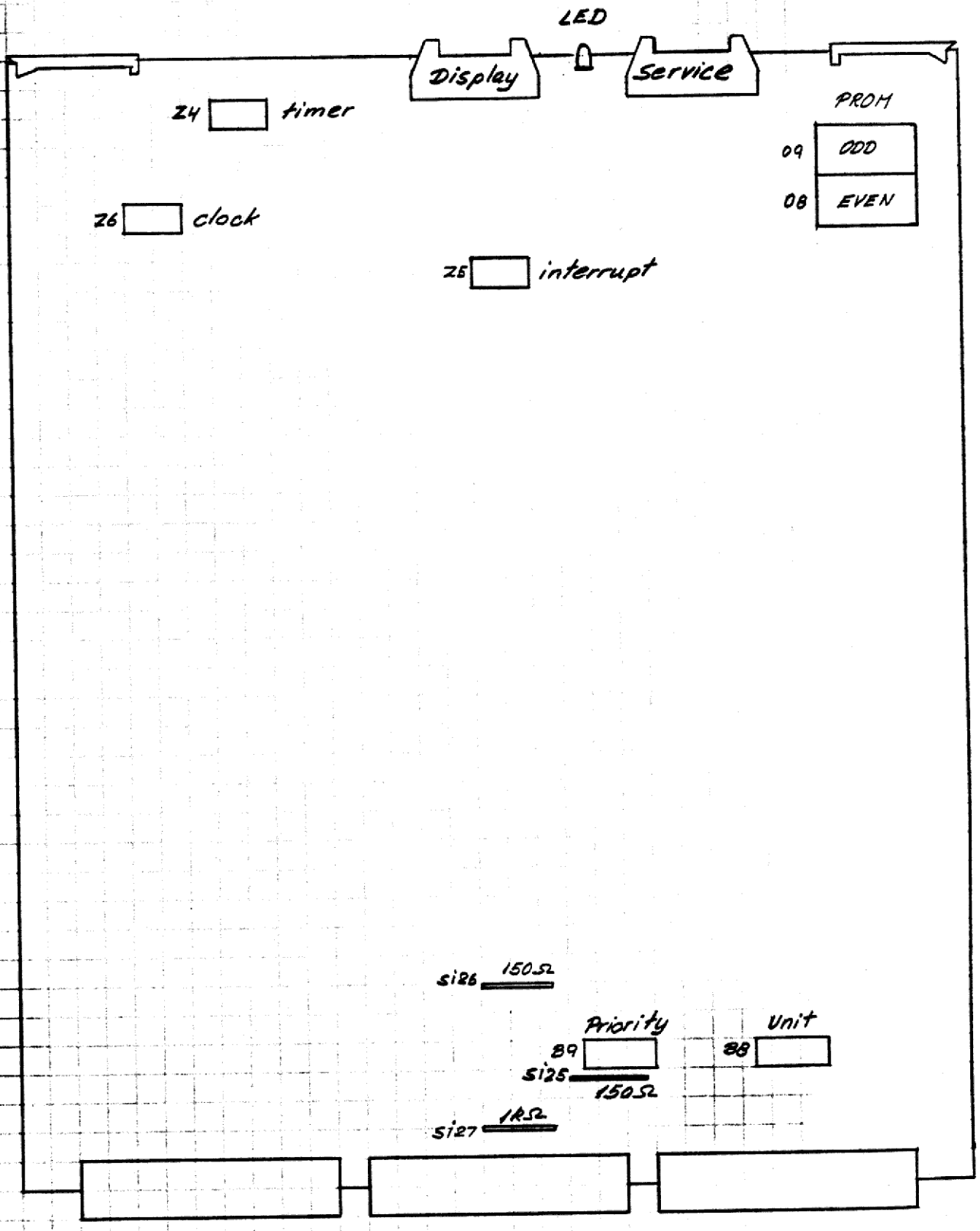
Check unit and priority PAL:

Unit PAL position B8: C170 to C175. See list.
Priority PAL position B9: C160 to C165. See list.

dansk data elektronik a/s

CPU Module

Initialer/dato	Side
KAN 840120	
Revideret	Projekt



MEMORY MODULE INSTALLATION.

Memory modules are placed in adjacent slots beneath their corresponding CPU module.

Check the address PAL:

Memory starting address	PAL Label
0	C180
1 Mb	C181
2 Mb	C183
3 Mb	C184
4 Mb	C185
.	.
.	.
9 Mb	C189
10 Mb	C18A
.	.
.	.
15 Mb	C18F

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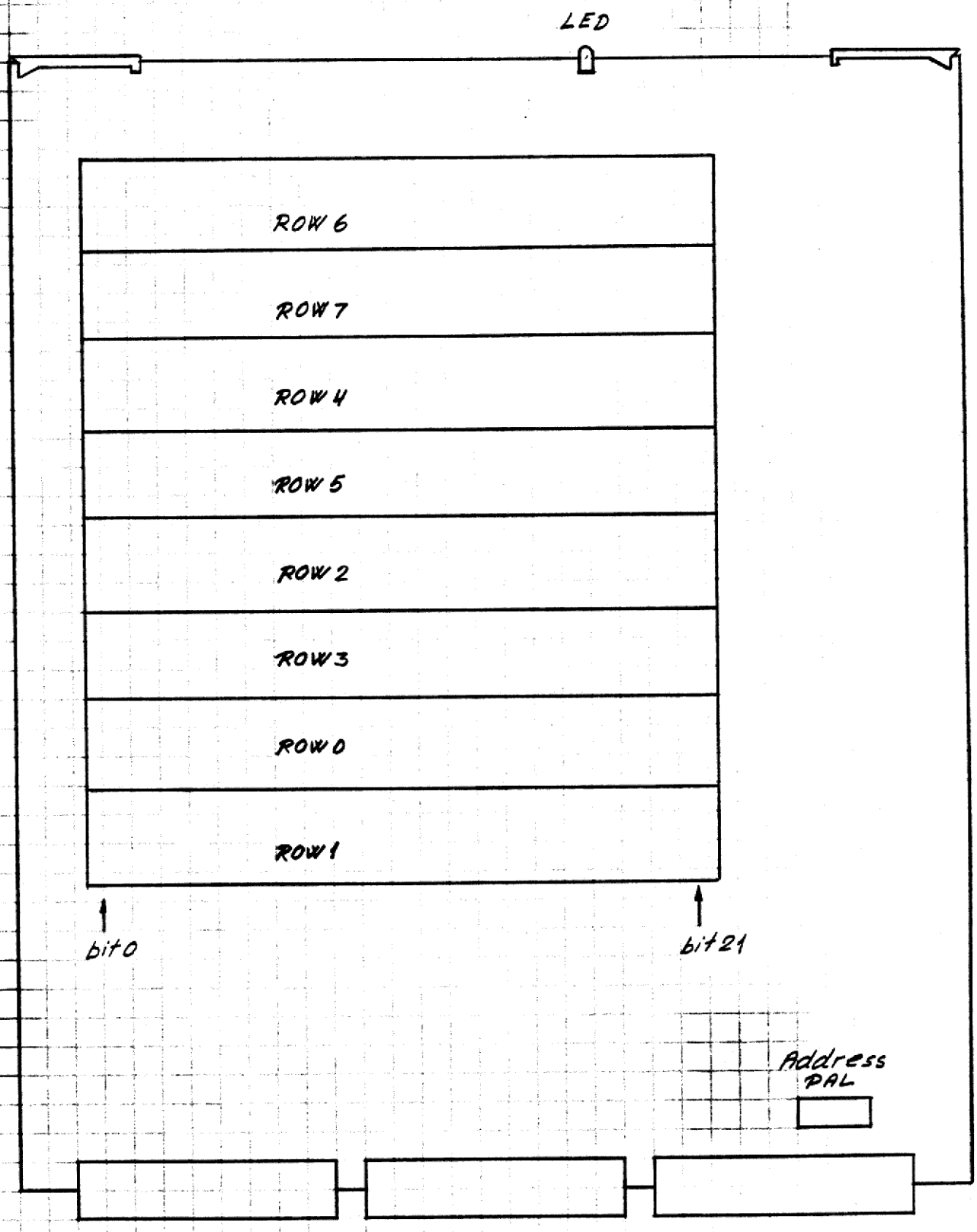
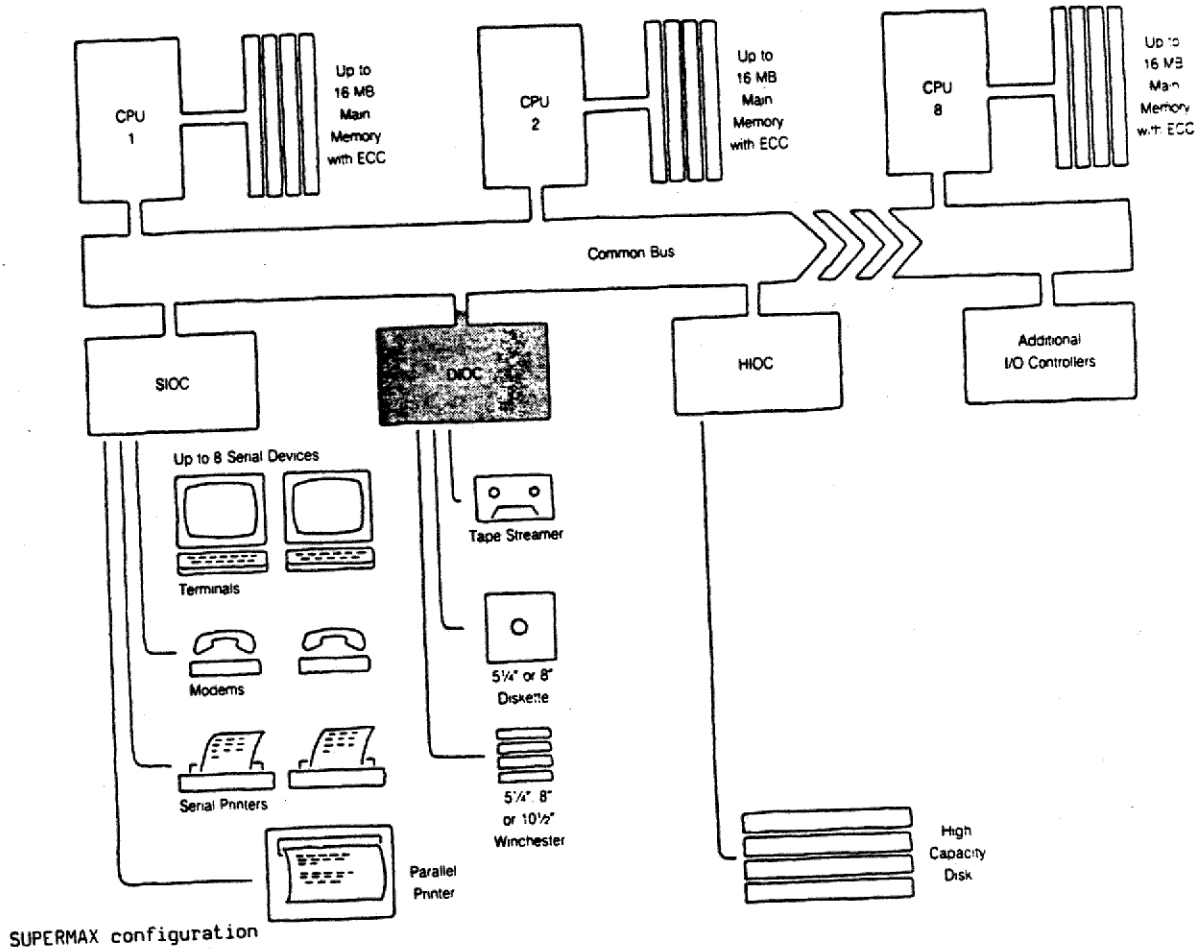
RAM Module

Initialer/dato	Side
KAN 840120	
Revideret	Projekt



DISK I/O CONTROLLER



SUPERMAX configuration

* DIOC, Disk I/O Controller.
* Intelligent Supermax module.
* Interface between disks and the I/O bus.

BASIC ELEMENTS.

* 8 bit microprocessor with RAM and PROM.
* Direct memory access, four channels.
  For internal use only.
* Full interface to I/O bus.
* Block transport unit, BTU, for
  high speed data transfers.
* Interrupt unit.
* Service port, RS-232-C, open collector.
* On board floppy disk interface.
* On board streaming tape interface.
* On board winchester disk interface.

FLOPPY DISK INTERFACE.

* Full onboard floppy disk controller.

* Board mounted for interface to 8 inch drives or 5.25 inch drives.

8 inch floppy interface:

* One to four 8 inch floppy drives.

* Double sided, double density encoding or single sided, single density IBM 3740 compatible format.

5.25 inch floppy interface:

* One to three 5.25 inch floppy drives.

* Double sided, double density encoding.

Disk drive capacity, formatted:

* 8 inch drive: 1025024 bytes.

* 5.25 inch drive: 573440 bytes.

STREAMING TAPE INTERFACE.

* Full on board streaming tape interface.

* Quater-inch Interchange Committee interface standard. QIC II interface.

* Cartridge streaming drive:

  - 20 Mbytes formatted capacity.
  - 30 kb/sec. transfer rate.

WINCHESTER DISK INTERFACE.

* Full onboard winchester disk interface.

* Host interface level:
  Shugarts Associated Standard Interface bus.
  SASI provides a fast and flexible interface
  between the DIOC and a disk controller.

* One to eight disk controllers connected
  to the SASI bus.

* Device level interface:

  Examples:
  - ST 506
  - SMD
  - etc.

* One or two disk drives connected to each
  disk controller. Depends on the contoller
  type.

BASIC HARDWARE ELEMENTS.

* 8 bit microprocessor with DRAM + PROM.

* Direct memory access, four channels.
  For internal use only.

* Full interface to I/O bus.

* Block transport unit, BTU, for
  high speed data transfers.

* Interrupt unit.

* Service port, RS-232-C, open collector.

MICROPROCESSOR.

* 8 bit microprocessor.
  8085-2 with 10 Mhz clock input.

* 64 kbytes dynamic RAM. 8 bit + parity.

* 8 kb PROM for bootstrap program
  and resident test programs.

* Direct Memory Access. DMA.
  AMD 9517, 4 Mhz.

* Parity-check during all read cycles.

* Time-out on all memory cycles.

INTERRUPT.

* All interrupt inputs provided in the 8085 microprocessor are all used.

Internal interrupts:

* RST 5.5, Service port.

* RST 6.5, Disk interface interrupt. Status register.

* RST 7.5, Real time clock.

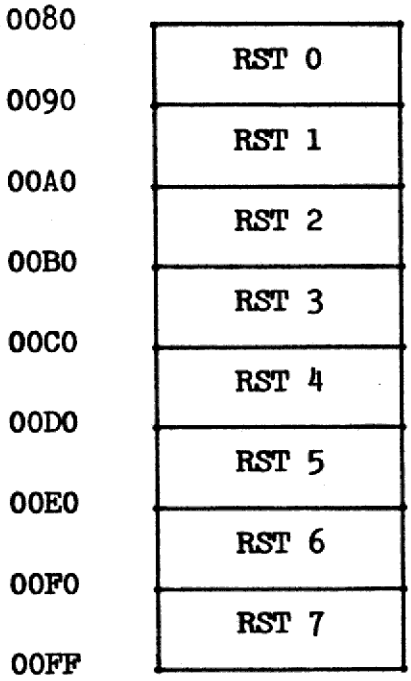
* TRAP, Error detection.

External interrupts:

* RST 7 to RST 0 are used. Memory write cycles from the I/O bus. 8 blocks each 16 bytes.

EXTERNAL INTERRUPT.

128 bytes of the 64 kb DRAM area.



Bus cycles: Word write.
Byte write.
Read modify write.

BLOCK TRANSPORT UNIT. BTU.

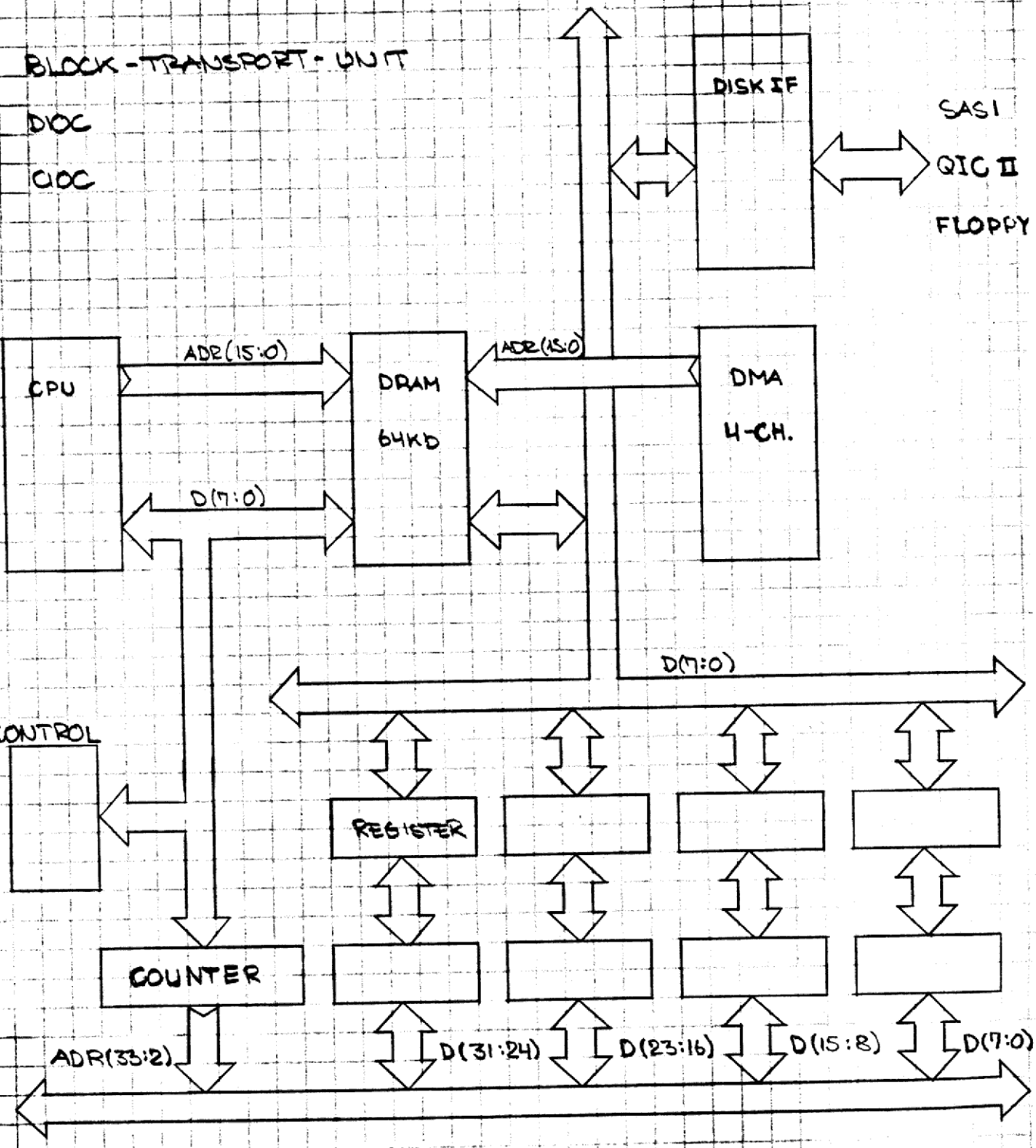
* Built for high speed data transfers between DIOC and the memories of CPU modules connected to the I/O bus.

* Uses 32 bit wide data transfers on the I/O bus. Because of the double word transfers, the load on the I/O bus is minimum.

dansk data elektronik a/s

Initialer/dato	Side
840122 BS	
Revideret	Projekt

SUPERMAX BTU



DW
DTACK
ASB
BUSERROR

TIME-OUT

I/O BUS INTERFACE.

* 8085 address expanded through a memory mapping unit. This means that the DIOC has full I/O bus addressing capability.

* The DIOC is able to act in I/O bus cycles as a passive or an active unit.

* Access to memory is shared evenly between DMA, CPU and I/O bus cycles.

* Following cycles are implemented:

  Active cycles : Byte read and write.

  Passive cycles: Byte read and write.
  Word read and write.
  Read modify write.

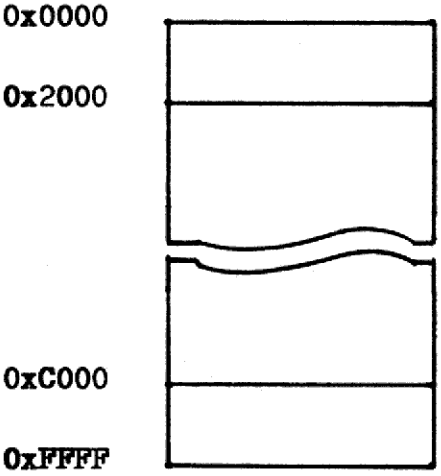
* The DIOC is able to act on the error signals implemented in the I/O bus.

* Time out function on all memory cycles.
  BTU I/O bus cycles.
  8085 memory cycles.
  8085 active bus cycles.

MEMORY MAPPING UNIT.

* Translatation from 8085 16 bits address to the 34 bits I/O bus address.

Memory layout:



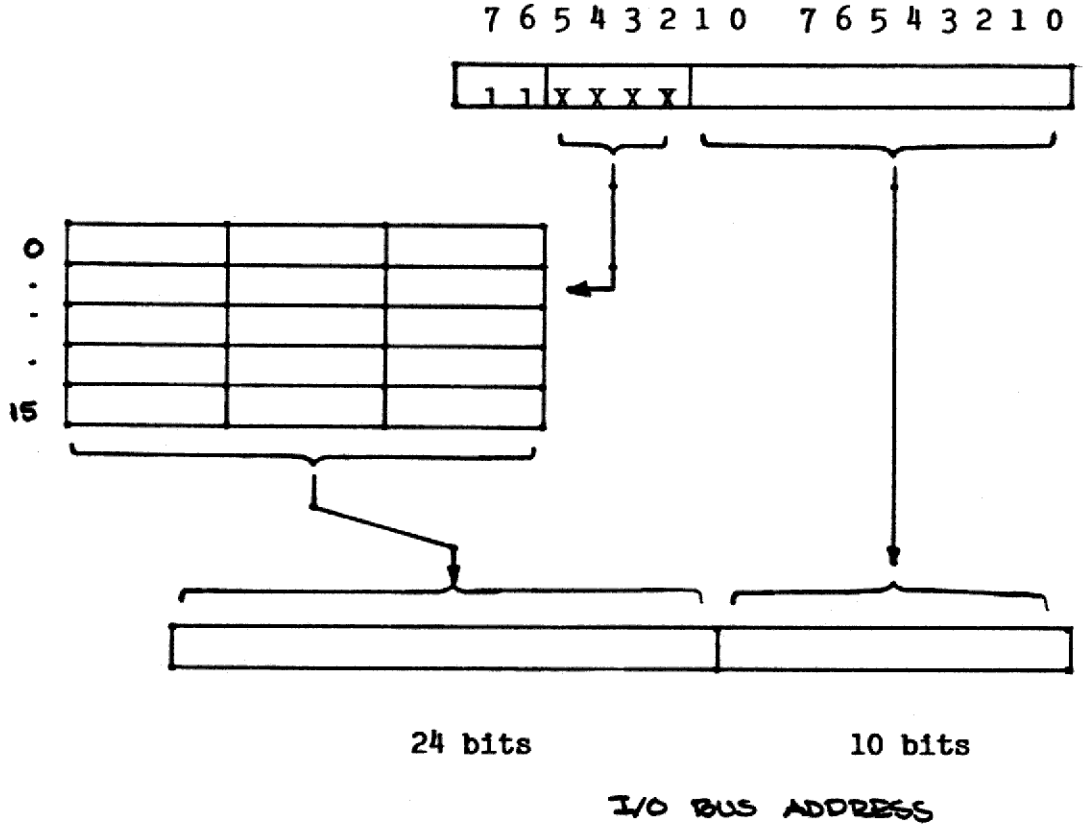
Boot loader PROM or RAM.

Access to I/O bus or internal RAM.

* Possible to bankswitch the most significant 16 k bytes of RAM.

MEMORY MAPPING UNIT.

* 24 bits wide. 16 entries.



INDICATOR LEDS.

Five red light emitting diodes are used to indicate errors and special status.

LED1.

On: The boot prom is enabled.
Off: The boot prom is switched out.
Upon power up: The LED1 is on.

LED2.

On: A time out is pending.
Off: No time out.
Upon power up: The LED2 is off.

LED3.

On: A bus error is received.
Off: No bus error.
Upon power up: The LED3 is off.

LED4.

On: The ERROR line is active. The error line is set by the program or becaurse of parity error.
Off: No error.
Upon power up: The LED4 is on.

LED5.

On: The DIOC has answered with a bus error.
Off: No error.
Upon power up: The LED5 is off.

STRAPS.

Strap 1.

Function: Real time clock.

Position: C 3,2

Jumper	Clock
1	0.8 milliseconds
2	3.9 milliseconds
3	7.8 milliseconds
4	39.0 milliseconds
5	78.0 milliseconds

Strap 2.

Function: Baud rate to service port. Connected to both Txclk and Rxclk.

Position: B 7,3

Jumper	Clock
1	9600 x 16 baud.
2	4800 x 16 baud.
3	2400 x 16 baud.
4	1200 x 16 baud.

Strap 3.

Function: Special option for hardware service.

Position: B 4,3

Under normal circumstances, the jumper must be in position two.

Strap socket 1.

Function: Possible to connect two switches: One is able to generate an internal reset pulse and the other is able to generate a hardware interrupt. (TRAP)

Position: C 4,1

Under normal circumstances the strap socket is mounted as follows:

```
    * *=* * * * * *
1.  * *=* * * * * *
```

An internal reset pulse is generated if the connection between pin 2 and 3 is removed, and pins 1 and 2 are connected together.

A non-maskable interrupt TRAP is generated if the connection between pin 14 and 15 is removed, and pins 15 and 16 are connected together.

INSTALLATION.

All modules in a SUPERMAX computer system differ in some details.

Unit number.

Each intelligent module connected to the common, I/O bus has an unique address. The address is called the unit number. The unit number is coded in a programable device, called a PAL. The PAL is marked with the text DUXX. XX is the decimal unit number. The unit number PAL is located in position A 4,6.

Priority.

The arbitration scheme used in the commen, I/O bus is based on fixed priorities. The priority is coded in a PAL. Two units connected to the I/O bus cannot use the same priority. The priority PAL is marked DPXX, where XX is the priority. The DIOC module uses two priorities. The PALs are located in position A 1,9 and A 1,10.

18. CABLES.

The connection between the DIOC module and the disks is made with three flat cable connectors.

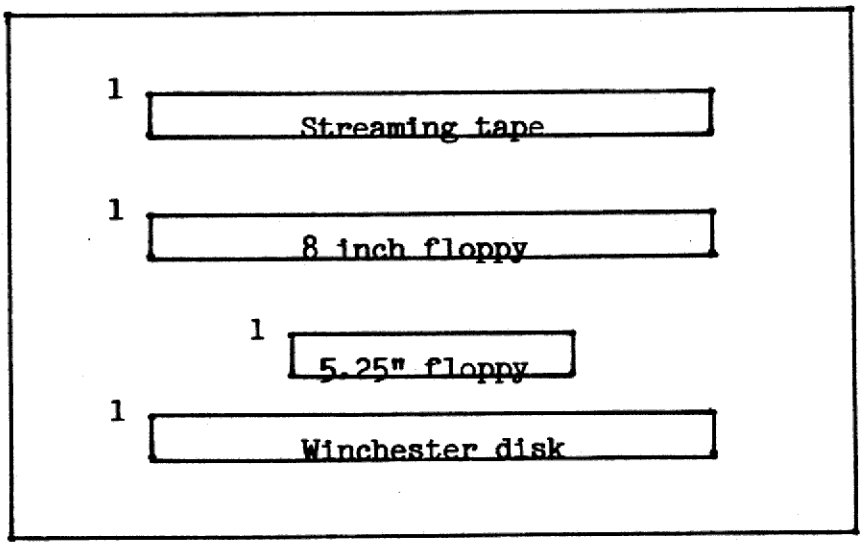
The headers mounted on the PCB are positioned as follows:

Winchester disk: C 1,8.

Floppy disk: C 3,8.

Streaming tape: C 5,8.

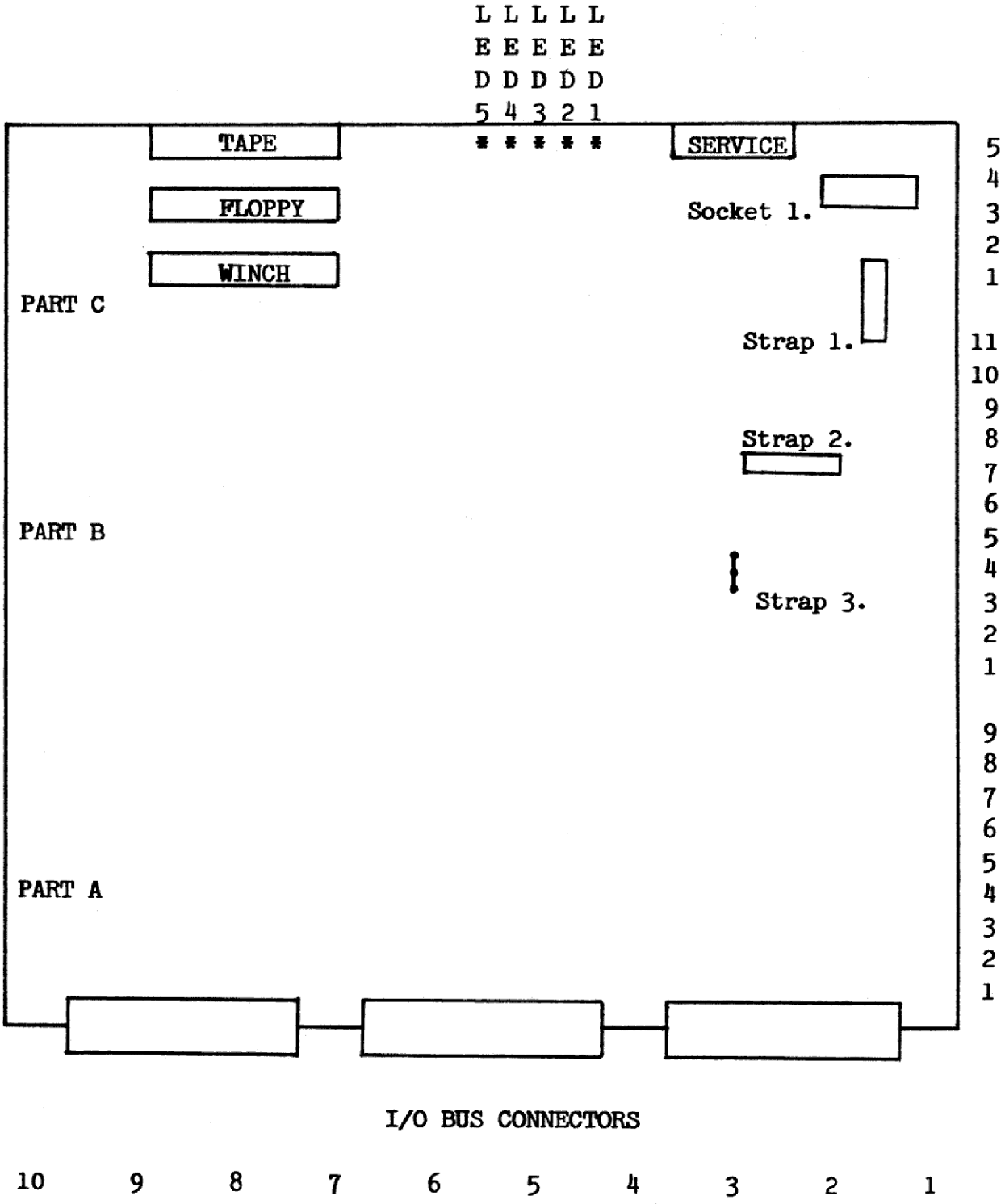
The three flat cables are connected to the DIOC back panel The DIOC back panel is mounted on the rear of the SUPERMAX card cabinet.



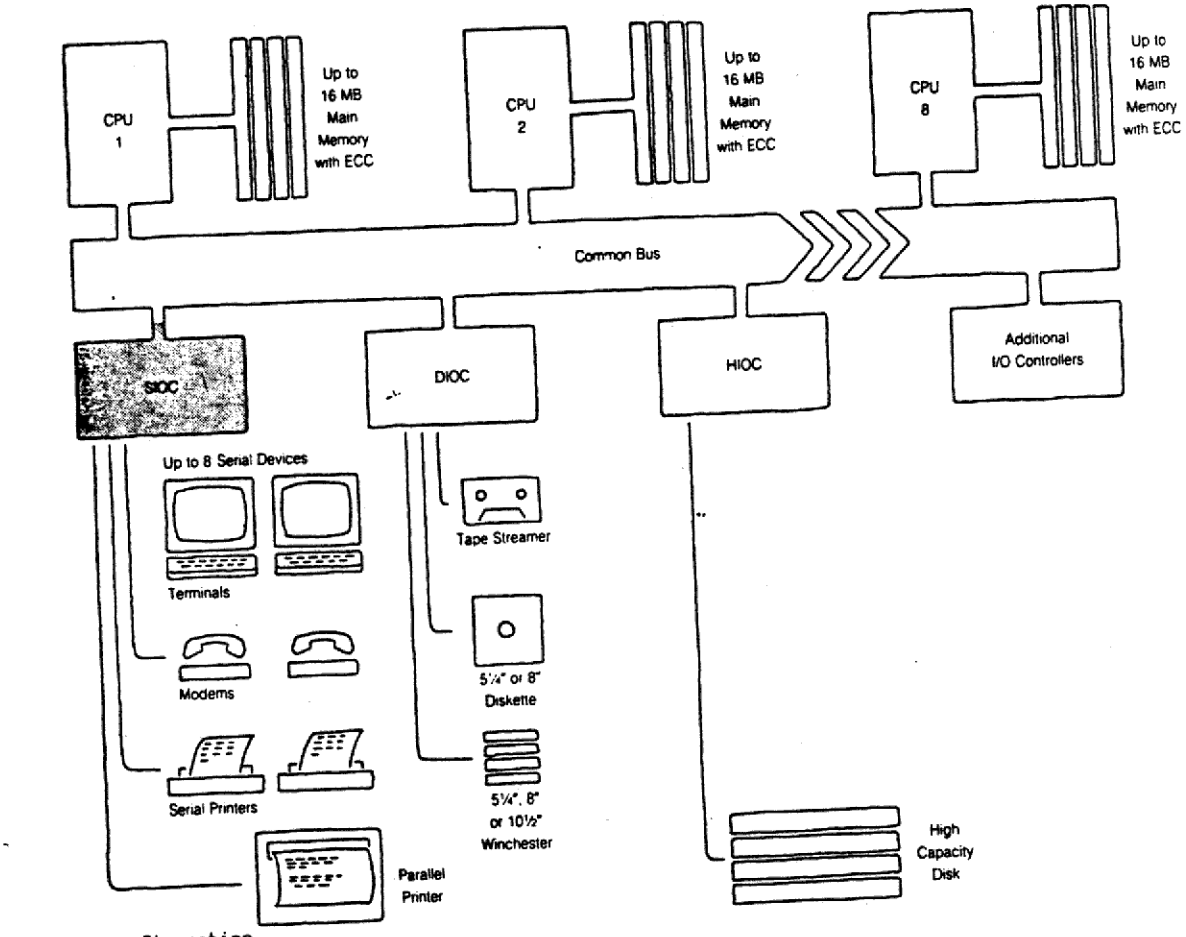
Card cabinet disk interface panel
Seen from the rear.

The connection to the service port is located in position C 5,3.

BOARD SURVEY.



SERIEL I/O CONTROLLER



SUPERMAX configuration

* SIOC, Seriel I/O Controller.
* Intelligent Supermax module.
* Interface between RS-232-C or RS-422 devices and the I/O bus.

BASIC ELEMENTS:

* 8 bit microprocessor with RAM and PROM.
* Full interface to I/O bus.
* Interrupt unit.
* Service port, RS-232-C, open collector.
* Eight seriel channels.
* One parallel printer port.

SERIAL INTERFACE.

* 6 asyncronous channels.
  RS-232-C interface.

* 2 syncronous or asyncrounous channels.
  RS-232-C or RS-422 interface.

* Choice of interface standard is under program control.

* Baud rates from 50 to 19.200 baud.
  Programmable.

* Character length from 5 to 8 bits.

* Odd, even or no parity.

* 1, 1.5 or 2 stop bits.

Parallel printer port.

* Simple parallel printer port.

* Centronics compatible.

BASIC HARDWARE ELEMENTS:

* 8 bit microprocessor with DRAM + PROM.
* Full interface to I/O bus.
* Interrupt unit.
* Service port, RS-232-C, open collector.

MICROPROCESSOR.

* 8 bit microprocessor.
  8085-2 with 10 Mhz clock input.

* 64 kbytes dynamic RAM. 8 bit + parity.

* 8 kb PROM for bootstrap program
  and resident test programs.

* Parity-check during all read cycles.

* Time-out on all memory cycles.

INTERRUPT.

* All interrupt inputs provided in the 8085 microprocessor are all used.

Internal interrupts:

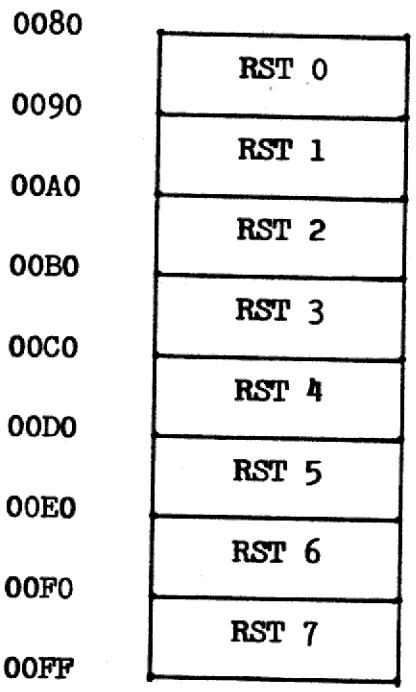
* RST 5.5, Service port.
* RST 6.5, Not used.
* RST 7.5, Real time clock.
* TRAP, Error detection.
* RST 0 to RST 7, USARTs.
  Straps.

External interrupts:

* RST 0 to RST 7 are used.
  Memory write cycles from the I/O bus.
  8 blocks each 16 bytes.

EXTERNAL INTERRUPT:

128 bytes of the 64 kb DRAM area.



16 bytes

Bus cycles: Word write.
Byte write.
Read modify write.

I/O BUS INTERFACE.

* 8085 address expanded through a memory mapping unit. This means that the SIOC has full I/O bus addressing capability.

* The SIOC is able to act in I/O bus cycles as a passive or an active unit.

* Access to memory is shared evenly between CPU and I/O bus cycles.

* Following cycles are implemented:

  Active cycles : Byte read and write.

  Passive cycles: Byte read and write.
  Word read and write.
  Read modify write.

* The SIOC is able to act on the error signals implemented in the I/O bus.

* Time out function on all memory cycles.
  8085 memory cycles.
  8085 active bus cycles.

INDICATOR LEDS.

Five red light emitting diodes are used to indicate errors and special status.

LED1.

On: The boot prom is enabled.
Off: The boot prom is disabled.
Upon power up: The LED1 is on.

LED2.

On: A time out is pending.
Off: No time out.
Upon power up: The LED2 is off.

LED3.

On: A bus error is received.
Off: No bus error.
Upon power up: The LED3 is off.

LED4.

On: The ERROR line is active. The error line is set by the program or becaurse of parity error.
Off: No error.
Upon power up: The LED4 is on.

LED5.

On: The SIOC has answered with a bus error.
Off: No error.
Upon power up: The LED5 is off.

STRAPS.

Strap socket 1.

Function: USART interrupt, Rxrdy.

Position: A 2,10
Name : A6

	1.		
Rxrdy(0)	*	*	RST0
Rxrdy(1)	*	*	RST1
Rxrdy(2)	*	*	RST2
Rxrdy(3)	*	*	RST3
Rxrdy(4)	*	*	RST4
Rxrdy(5)	*	*	RST5
Rxrdy(6)	*	*	RST6
Rxrdy(7)	*	*	RST7

Strap socket 2.

Function: USART interrupt, Txrdy.

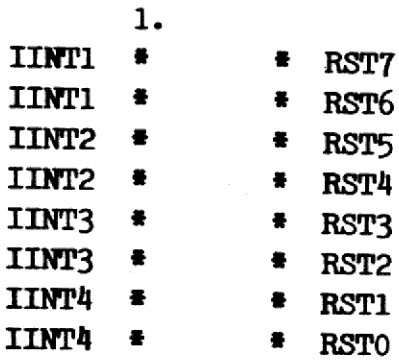
Position: A 1,10
Name : A7

	1.		
Txrdy(0)	*	*	RST0
Txrdy(1)	*	*	RST1
Txrdy(2)	*	*	RST2
Txrdy(3)	*	*	RST3
Txrdy(4)	*	*	RST4
Txrdy(5)	*	*	RST5
Txrdy(6)	*	*	RST6
Txrdy(7)	*	*	RST7

Strap socket 3.

Function: RS-422 Indicator interrupt.

Position: A 1,9
Name : A8

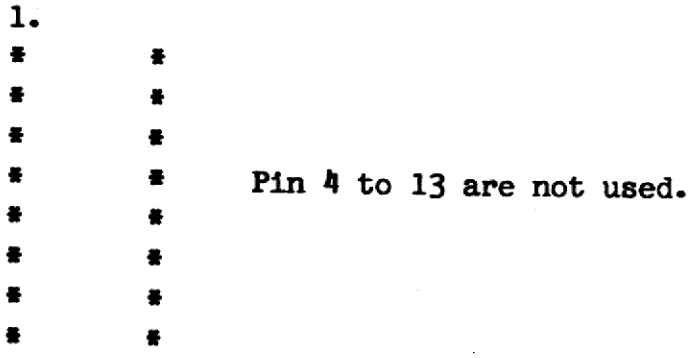


Strap socket 4.

Function: Possible to connect two switches: One is able to generate an internal reset pulse and the other is able to generate a hardware interrupt. (TRAP)

Position: C 4,1

Under normal circumstances the strap socket is mounted as follows:



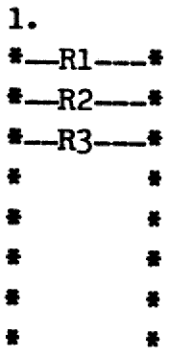
An internal reset pulse is generated if the connection between pin 2 and 3 is removed, and pins 1 and 2 are connected together.

A non-maskable interrupt TRAP is generated if the connection between pin 14 and 15 is removed, and pins 15 and 16 are connected together.

Strap socket 5.

Function: RS-232-C interface for service port.

Position: C 3,3
Name : J4



More service ports may be connected in parallel to a peripheral. Three pull-down resistors must be mounted for correct transmission if only the SIOC is connected to a peripheral.

Strap 1.

Function: Baud rate to service port. Connected to both Txclk and Rxclk.

Position: B 7,1

Jumper	Clock
1	9600 x 16 baud.
2	4800 x 16 baud.
3	2400 x 16 baud.
4	1200 x 16 baud.

Strap 2.

Function: Special option for hardware service.

Position: B 8,3

Under normal circumstances, the jumper must be in position one.

Strap 3.

Function: Polarity of the parallel printer port signal "DATA STROBE".
The data strobe signal is an output signal.
Position: C 3,4
Name : SP2

Jumper	Function
1	Active high data strobe.
2	Active low data strobe.

Strap 4.

Function: Polarity of the parallel printer port signal "BUSY".
The BUSY signal is an input.
Position: C 2,4
Name : SP3

Jumper	Function
1	Active high BUSY signal.
2	Active low BUSY signal.

Strap 5.

Function: Polarity of the parallel printer port signal "ACKNOWLEDGE".
The ACK signal is an input.
Position: C 2,4
Name : SP1

Jumper	Function

1	Active low ACK signal.
2	Active high ACK signal.

Strap 6.

Function: Transmitter clock to USART(6). RS-232-C interface.

Position: B 6,10
Name : SS1

1	The SIOC drives the RS-232-C interface signal Txclk with baud rate counter(2,0). The clock is an input to USART(6).
2	The RS-232-C interface signal Txclk is an input to USART(6).

Strap 7.

Function: Receiver clock to USART(6). RS-232-C interface.

Position: B 6,10
Name : SS2

Jumper	Function
1	The SIOC drives the RS-232-C interface signal Rxclk with baud rate counter(2,0). The clock is an input to USART(6).
2	The RS-232-C interface signal Rxclk is an input to USART(6).

Strap 8 and 9.

Function: Receiver/transmitter clock to USART(6). RS-422 interface.

Position: B 6,7
Name : SS3 and SS4.

Jumper	Function
1	The SIOC drives the RS-422 interface signal Signal element timing with baud rate counter(2,0). The clock is an input to USART(6).
2	The RS-422 interface signal Signal element timing is an input to USART(6). (Rxclk and Txclk)

Note that SS3 and SS4 jumpers must be in the same position.

Strap 10.

Function: Transmitter clock to USART(7). RS-232-C interface.

Position: B 9,6
Name : ST1

Jumper	Function
1	The SIOC drives the RS-232-C interface signal Txclk with baud rate counter(2,1). The clock is an input to USART(7).
2	The RS-232-C interface signal Txclk is an input to USART(7).

Strap 11.

Function: Receiver clock to USART(7). RS-232-C interface.

Position: B 9,6
Name : ST2

Jumper	Function
1	The SIOC drives the RS-232-C interface signal Rxclk with baud rate counter(2,1). The clock is an input to USART(7).
2	The RS-232-C interface signal Rxclk is an input to USART(7).

Strap 12 and 13.

Function: Receiver/transmitter clock to USART(7). RS-422 interface.

Position: B 6,6
Name : ST3 and ST4.

Jumper	Function
1	The SIOC drives the RS-422 interface signal Signal element timing with baud rate counter(2,1). The clock is an input to USART(7).
2	The RS-422 interface signal Signal element timing is an input to USART(7). (Rxclk and Txclk)

Note that ST3 and ST4 jumpers must be in the same position.

INSTALLATION.

All modules in a SUPERMAX computer system differ in some details.

Unit number.

Each intelligent module connected to the common, I/O bus has an unique address. The address is called the unit number. The unit number is coded in a programable device, called a PAL. The PAL is marked with the text SUXX. XX is the decimal unit number. The unit number PAL is located in position A 4,5.

Priority.

The arbitration scheme used in the common, I/O bus is based on fixed priorities. The priority is coded in a PAL. Two units connected to the I/O bus cannot use the same priority. The priority PAL is marked DPXX, where XX is the priority. The SIOC module uses one priority. The PAL is located in position A 1,6.

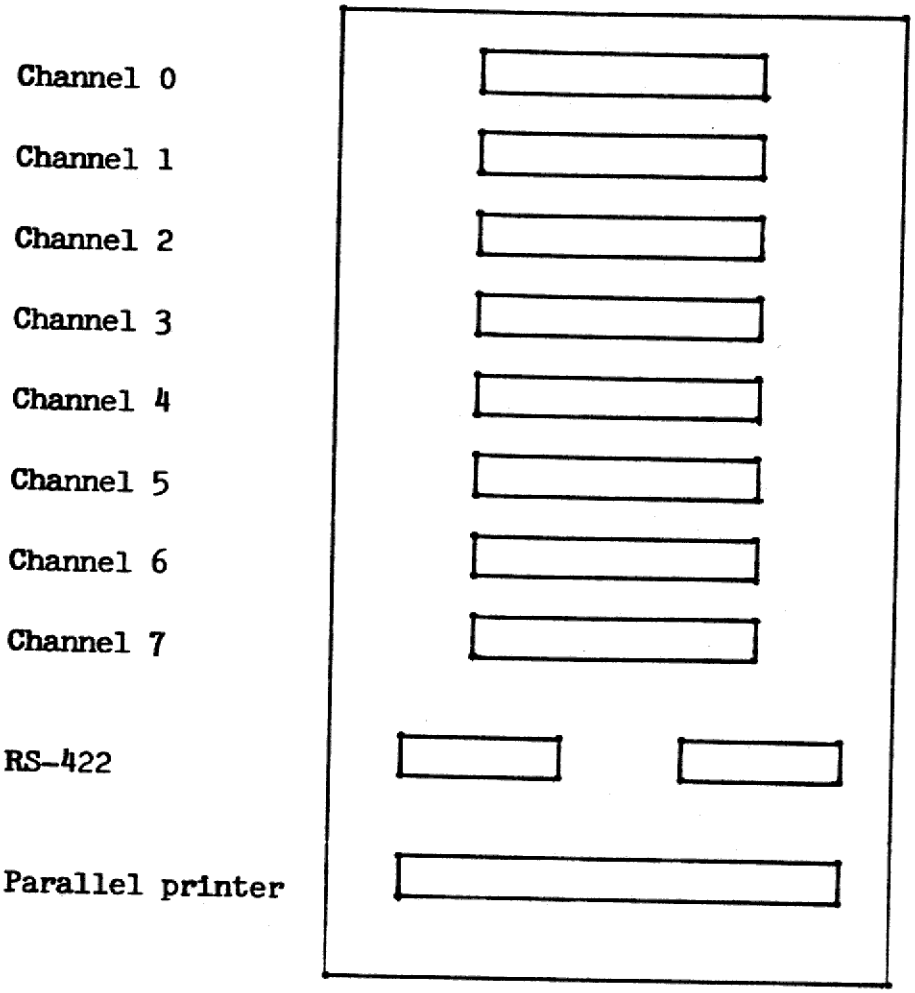
CABLES.

The connection between the SIOC module and the SIOC back panel is made with two flat cable connectors. The headers mounted on the PCB are positioned as follows:

RS-232-C signals: C 4,8

RS-422 signals and parallel printer signals: C 2,8

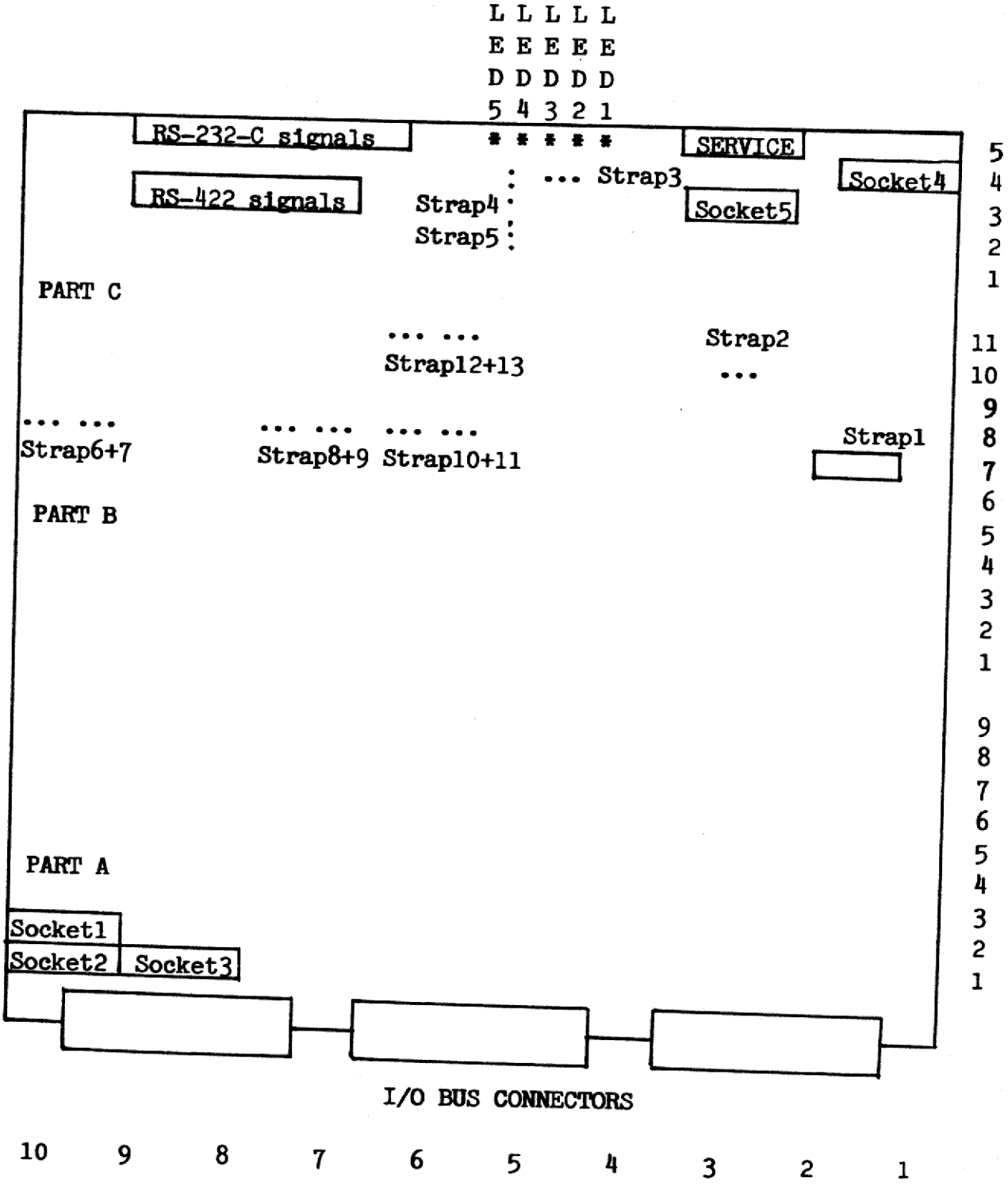
The SIOC back panel is mounted on the rear of the SUPERMAX card cabinet.



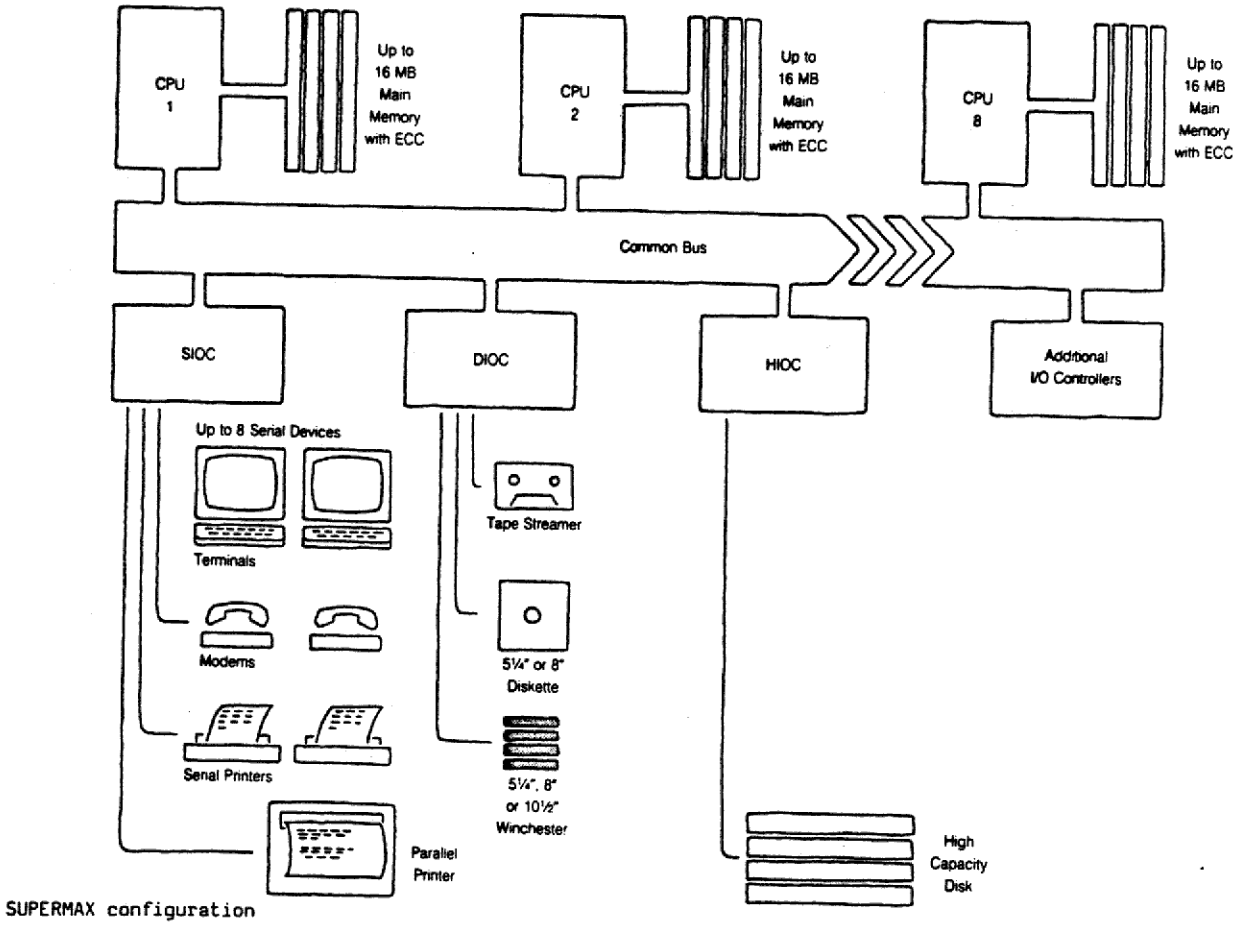
SIOC back panel seen from the rear

The connection to the service port is placed in position C 4,3.

BOARD SURVEY.



COMMUNICATION I/O CONTROLLER



SUPERMAX configuration

* CIOC, Communication I/O Controller.
* Intelligent Supermax module.
* Interface between advanced data communication ports and the I/O bus.

BASIC ELEMENTS:

* 8 bit microprocessor with RAM and PROM.

* Direct memory access, eigtht channels.
  For internal use only.

* Full interface to I/O bus.

* Block transport unit, BTU, for
  high speed data transfers.

* Interrupt unit.

* Service port, RS-232-C, open collector.

* Two advanced data communication ports.

DATA COMMUNICATION PORTS.

* Each port consist of
  - one HDLC/SDLC Controller.
  - two USARTs.
  - two DMA channels.

  Selection between the LSI devices and the interface is under program control.

* Syncronous or asyncronous transmission.
  Programmable baud rate. 50 to 64 kbit/s.

* RS-232-C or RS-422 interface.
  Programmable.

BASIC HARDWARE ELEMENTS:

* 8 bit microprocessor with DRAM + PROM.

* Direct memory access, eight channels.
  For internal use only.

* Full interface to I/O bus.

* Block transport unit, BTU, for
  high speed data transfers.

* Interrupt unit.

* Service port, RS-232-C, open collector.

MICROPROCESSOR.

* 8 bit microprocessor.
  8085-2 with 10 Mhz clock input.

* 64 kbytes dynamic RAM. 8 bit + parity.

* 8 kb PROM for bootstrap program
  and resident test programs.

* Direct Memory Access. DMA.
  AMD 9517, 4 Mhz.

* Parity-check during all read cycles.

* Time-out on all memory cycles.

INTERRUPT.

* All interrupt inputs provided in the 8085 microprocessor are all used.

Internal interrupts:

* RST 5.5, Service port.

* RST 6.5, Direct memory access interrupt.
  Status register.
  Mask register.

* RST 7.5, Real time clock.

* TRAP, Error detection.

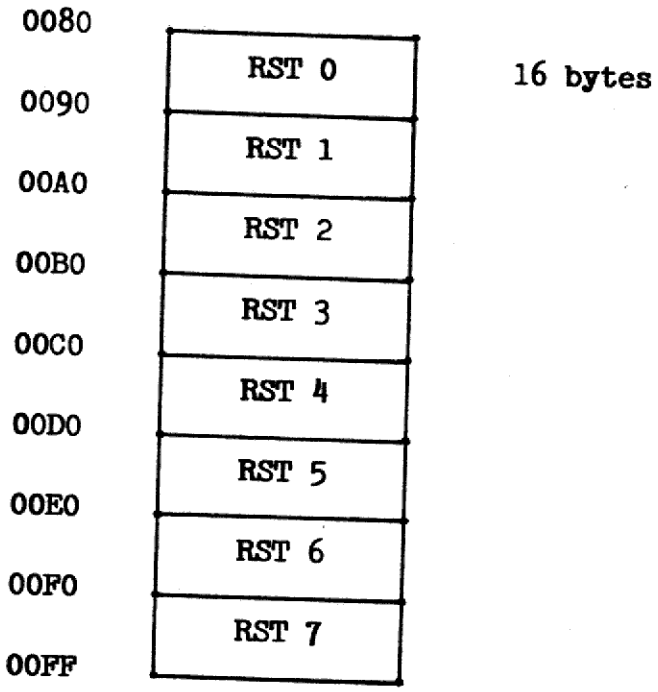
* RST 0 to RST 7, Communication ports.
  Strap. Mask register.

External interrupts:

* RST 7 to RST 0 are used.
  Memory write cycles from the I/O bus.
  8 blocks each 16 bytes.

EXTERNAL INTERRUPT:

128 bytes of the 64 kb DRAM area.



Bus cycles: Word write.
Byte write.
Read modify write.

BLOCK TRANSPORT UNIT. BTU.

* Built for high speed data transfers between CIOC and the memories of CPU modules connected to the I/O bus.

* Uses 32 bit wide data transfers on the I/O bus. Because of the double word transfers, the load on the I/O bus is minimum.

I/O BUS INTERFACE.

* 8085 address expanded through a memory mapping unit. This means that the CIOC has full I/O bus addressing capability.

* The CIOC is able to act in I/O bus cycles as a passive or an active unit.

* Access to memory is shared evenly between DMA, CPU and I/O bus cycles.

* Following cycles are implemented:

  Active cycles : Byte read and write.

  Passive cycles: Byte read and write.
  Word read and write.
  Read modify write.

* The CIOC is able to act on the error signals implemented in the I/O bus.

* Time out function on all memory cycles.
  BTU I/O bus cycles.
  8085 memory cycles.
  8085 active bus cycles.

BOOT PROCEDURE (PRELIMINARY).

One unit, the master DIOC, is responsible for booting all other units in a SUPERMAX SYSTEM.

After POWER UP or RESET all units start executing programs placed in the boot loader PROMs.

All units initialize their memory and wait.

The master DIOC waits until the floppy disk drive becomes ready.

The master DIOC reads its own program from the floppy disk starting in a certain track and sector.

The master DIOC starts extcuting the loaded program.

The master DIOC addresses all possible units in a system to see which units are present.

The unit with the highest unit number is booted first.

When booting of a unit is finished, the master DIOC signals the unit that it has been booted and the unit starts executing the program.

The master DIOC goes on to boot the next unit, until all units have been booted.

The information loaded into a unit only depends upon the unit number:

UNIT NUMBER	UNIT TYPE	FILE LOADED	BOOT PROM
0 - 5	CPU	MCUB-6	CBOOT
6 - 10	SIOC	SCMIKM-0	SBOOT
11- 13	DIOC	DCMIKM-0	DCDRONE
14	MASTER DIOC	DCMIKM-0	DBOOT
15	DIOC	DCMIKM-0	DCDRONE

UNIT NUMBERS AND PRIORITIES.

The following is a list of unit numbers and priorities currently used in the SUPERMAX computer.

A new list will be introduced with the implementation of a new boot-procedure.

Unit type	Unit number	Priority	Unit PAL	Priority PAL
1. CPU	03	03	C173	C163
2. CPU	00	00	C170	C160
3. CPU	01	01	C171	C161
4. CPU	02	02	C172	C162
5. CPU	04	04	C174	C164
6. CPU	05	05	C175	C165
1. SIOC	08	13	SU08	SP13
2. SIOC	09	14	SU09	SP14
3. SIOC	10	20	SU10	SP20
4. SIOC	06	11	SU06	SP11
5. SIOC	07	12	SU07	SP12
1. DIOC	14	41, 42	DU14	DP41, DP42
2. DIOC	13	34, 40	DU13	DP34, DP40
3. DIOC	12	32, 33	DU12	DP32, DP33
4. DIOC	11	30, 31	DU11	DP30, DP31
5. DIOC	15	43, 44	DU15	DP43, DP44

Memory board.

Type	PAL
1. Memory board	C180
2. Memory board	C181
3. Memory board	C182
4. Memory board	C183
5. Memory board	C184

SERVICE PORT.

All units in a SUPERMAX system have a service port.

A service port is an "open collector RS 232" connection.

Service ports are wired together in a SUPERMAX system and connected to a terminal or modem.

USE OF SERVICE PORTS.

1. Testing and servicing of stand alone units.

   Boot loader PROMs are replaced by PROMs containing test programs.

2. System test.

   All service ports are connected in parallel to a service terminal or modem.

SYSTEM TEST.

A select sequence is used to connect the service terminal to a selected unit.

The select sequence is a string of characters typed on the terminal by the operator.

After select a menu is displayed on the terminal:

1. CONTINUE.

2. START TEST.

If CONTINUE is selected, the running program will continue but output to the terminal is now allowed. The running program can be:

A. Boot Loader Program.

B. System Program (operating system).

C. Test Program.

If START TEST is selected, a test program is started.

A unit is selected, connected to the terminal, until another unit is selected.