RCSL No: 44-RT2039,

Edition: November 1982

Author: Steen Nørgaard

Title:

RC700 Testsystem
User's Guide

RCSL 42-[illegible]

A/S REGNECENTRALEN
af 1979

Keywords:

RC700, Test Programs.

Abstract:

This manual describes the test system and the test programs for the RC700 Piccolo. The test programs described in this manual are: the memory test, the memory refresh test, the DMA test, the CTC test, the FDC test, the FDD test and the WDC test.

(30 printed pages)

Copyright © 1982, A/S Regnecentralen af 1979
RC Computer A/S

Printed by A/S Regnecentralen af 1979, Copenhagen

Users of this manual are cautioned that the specifications contained herein are subject to change by RC at any time without prior notice. RC is not responsible for typographical or arithmetic errors which may appear in this manual and shall not be responsible for any damages caused by reliance on any of the materials presented.

RCSL: 11905

TABLE OF CONTENTS PAGE

1. INTRODUCTION

This manual describes the diagnostic test programs for the RC700 microcomputer.

The test programs are testing the basic functions of the different parts of the hardware in the computer.

The sequence of the different test programs in the test system is organized with rising complexity. As far as possible, no part of the hardware is used before it is tested.

1.1 Load and Start

The test system is delivered on two flexible disks, a minidiskette and a maxidiskette, and in two PROM versions, a 4K PROM and as 2 x 2K PROM's.

Starting the test system from flexible disk:

- insert the diskette in the drive, push reset button and the tests start automatically.

Starting the test system situated in PROM's:

PROM system 1 (2 x 2K PROM)

These two PROM's are to be used with MIC702 and MIC703.

Turn off the power, remove the hood, install PROM (ROB361) in PROGRAMABLE ROM 0 socket and PROM (ROB362) in PROGRAMABLE ROM 1 socket. Turn on the power again. RESET will start the tests automatically.

PROM system 2 (4K PROM)

This PROM is to be used with MIC703, if print modif is made, and MIC704.

Turn off the power, remove the hood, install PROM (ROB363) in PROGRAMABLE ROM 0 socket. Turn on the power again. RESET will start the tests automatically.

Due to the limited storage capacity in the PROM's, only some of the tests are available. It is the tests which have connection to the flexible disk drives. The tests are: RAM test, DMA test, CTC test and FDD test.

THE TESTS

The testsystem described in this manual consists of 7 tests. The tests are ran under control of a testrouter, which has the purpose of administering the mode in which a particular list is ran. The seven tests are:

Memory test
Memory refresh test
DMA test
CTC test
FDC test
FDD test
WDC test

3. THE TESTROUTER

The testrouter is a central program which main purpose is to compute the address of the next test in the sequence. The address of the next test is derived from a variable holding the present testnumber and normally incremented by one. Every time a test has finished and is not in looping mode, the testrouter is entered.

3.1 Switch Parameters

The variable holding the test number also contains four switch bits, by which the testrouter decides how to administer the tests.

7	6	5	4	3	2	1	0
				test No			

h	l	k	s
a	o	e	u
l	o	y	p
t	p	b	r
		.	.
		o	p
		n	r
			i
			n
			t

halt: 0: halt on error
1: proceed though error

loop: 0: sequential, big loop of all tests
1: looping in the present test

keyb on: 0: the system has not been informed about an installed keyboard
1: a key on the keyboard has been struck at least once

supr print: 0: messages are printed on the display
1: no messages are printed (usable for fast looping)

Initial values of the switch parameters are all zeroes.

3.2 Keyboard Management 3.2

To enter the keyboard management is only possible when a strucked key has informed the system that a keyboard is connected. When this has happened, the testrouter answers with the valid capital letters and digits.

Valid keys are as follows:

H: set halt bit to 0
R: set halt bit to 1
L: set loop bit to 1
G: set loop bit to 0
S: set suppress print bit to 1
P: set suppress print bit to 0
(Please note that capital letters are used)

<esc>: will stop execution.

This is also the fact for any other key. Striking the <return> key will have the test system reentering the looping or running state.

When the testsystem is ran from the PROM version, it is only possible to enter the keyboardmanagement when the first output is seen on the screen after a RESET.

Numbers between 0-F will insert a new test number into the variable.

All other keys will give no response.

If one for example wants to loop in test 6 and not go into a HALT state if error, then strike the keys R, L, G (not necessarily this sequence). Furthermore if one wants to test fast for measuring purpose, one can suppress print by typing S. Suppress print means that nothing from now on will be written into the screenbuffer.

Relationship between the test numbers and actual tests is as follows in the diskette versions:

Test No	Test name
0	RAM checksum and RAM test *)
1	Memory refresh test
2	DMA test
3	CTC test
4	FDC test
5	FDD test
6	WDC test
7	WDC test **)
8	not used yet
9	not used yet
A	not used yet
B	not used yet
C	not used yet
D	not used yet
E	not used yet
F	not used yet

*) The RAM checksum is performed on the first 6 K bytes where the loaded image is.

**) Press the key "7" will force the testsystem to perform the WDC test, see chapter 10.

Relationship between the test numbers and actual tests is as follows in PROM versions:

Test No	Test name
0	PROM checksum and RAM test
1	DMA test
2	CTC test
3	FDD test
4	not used
5	not used
6	not used
7	not used
8	not used
9	not used
A	not used
B	not used
C	not used
D	not used
E	not used
F	not used

The test numbers not used yet will force the test system to return to test number 0.

3.3 Output

The testrouter will respond with some output. This is a version data and a test number. It also responds with the state of the test. This could be either running, stopped, looping or halted.

3.4 Specialities

The testrouter has a waiting point of 3 seconds when entered from the test number 0 to give the user time to key in some input to change parameters.

4. THE MEMORY TEST

The memory test consists of two tests. A PROM checksum test and a RAM test.

4.1 PROM Checksum Test

A check on the contents of the PROM (containing tests) is performed by adding the contents of all locations in the PROM and checking that the result is FF (Hex).

If a difference from FF (Hex) is found, an attempt is made to write an error message on the first line of the display.

The error message has the following layout:

<RC700 TESTSYSTEM chksum err>

Note that when loaded from flexible discs, the checksum is checked on the loaded image.

4.2 RAM Test

The memory test thereafter performs a test of the dynamic RAM memory. Of course, all memory cells are tested by the memory test (all variables are kept in CPU registers).

First the upper part (addresses higher than the last PROM address) of the memory is tested. If this was found OK, the test is moved to this memory area and the memory space shaded by PROM is tested.

The test pattern for the dynamic RAM memory consisting of chips of 1 bit x 16 k is three times 00 followed by three times FF (Hex). When all memory cells have been tested, they are again tested with the inversed pattern. This means that all bits are tested for "zero" and "one" insertion. It is the most convenient

pattern for discovering addressing errors because this modulus 3 pattern will not be repeated equivalent in a higher modulus address.

If an error occurs, a message will be written on the first line of the display. The layout is the following:

<RC700 TESTSYSTEM mem err ha la ex re>

where "ha" is high address, "la" is low address, "ex" is expected value and "re" is received value. All numbers are in hexadecimal notation. (To find any defective chip, consult fig. 1).

When both the PROM checksum test and the RAM memory test are terminated, an attempt is made to write on the display (whether there has been an error or not). This is done as simple as possible without any standard program (without interrupt service). On the first 17 positions of the first line, the identification of the system type will be written followed by a possible error message.

The total turn around time for the selftest is 7.5 seconds.

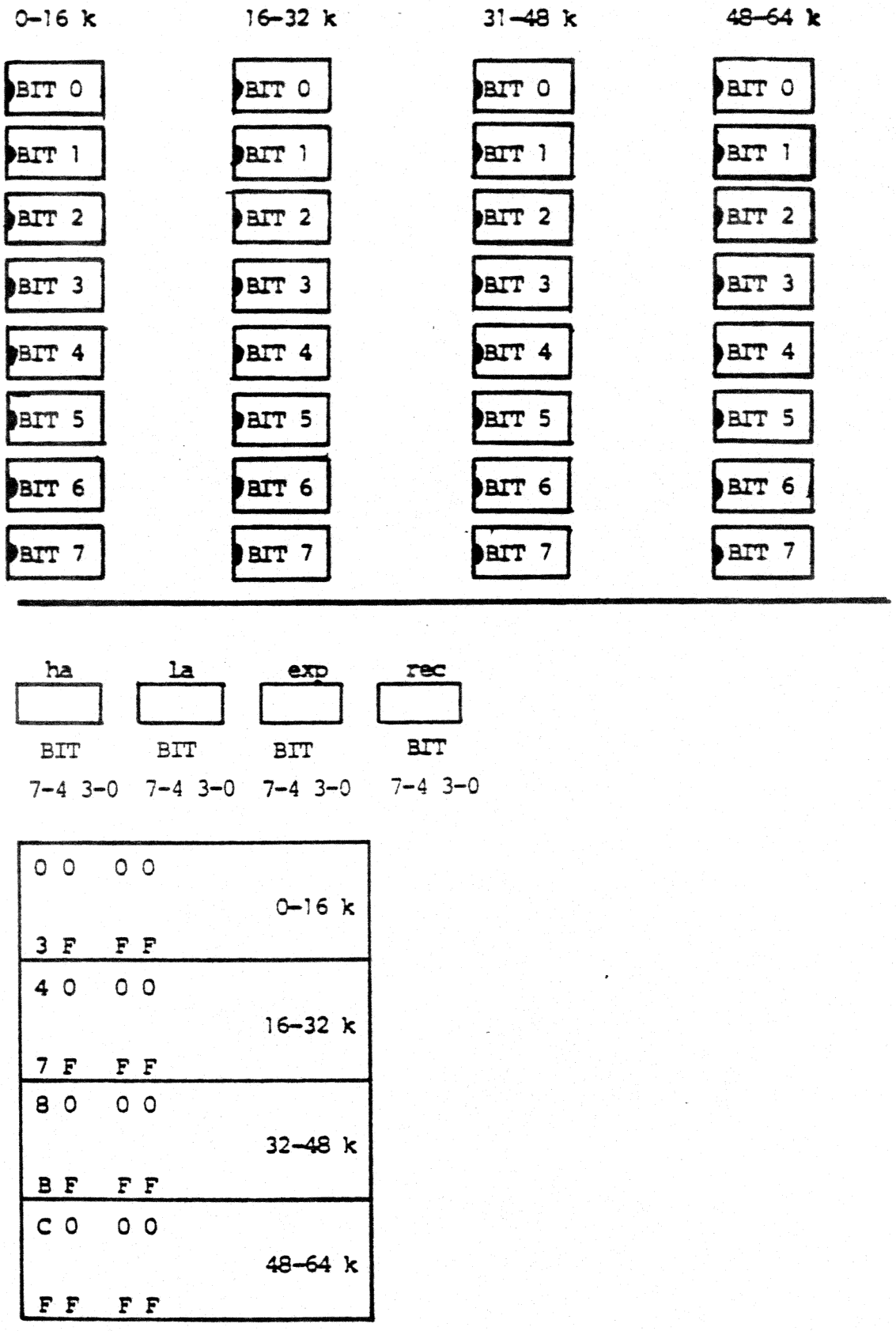

Figure 1: Layout of 64K RAM memory.

5. MEMORY REFRESH TEST 5.

The dynamic memory refresh test is a test which verifies the function of the memory controller chip.

It writes a pattern in memory consisting of an XOR of high and low address part. The pattern is written from the memory address 8000H until the hexadecimal address: F000H (where the display image starts).

When the pattern has been written, the test waits for 5 seconds in a waiting loop before it performs a check of data.

The main purpose of this test is to discover modification of data happened in the delay time, due to malfunction of the refresh counting in the memory controller.

Possible error message is:

<data modified in byte xx xx exp: xx rec: xx>

Output is placed on the fourth line of the display.

6. DMA TEST

6.

The DMA test loop is testing DMA transfers between channel 0 and channel 1. This is done as a memory to memory transport. Channel 1 is receiving and channel 0 is transmitting.

When the transport is finished, the receiving buffer is checked against the transmitted buffer byte by byte.

The DMA test will write its messages on the fifth line of the display.

Apart from the identification of the test, the possible messages from the DMA test are:

<OK>
<TC timeout 200 ms>
<data error, byte no: xx xx exp: xx rec: xx>

All numbers are in hexadecimal notation. "TC timeout ms" shows that the terminal count bit for channel 1 in the DMA status register has not been set within 200 ms. and that the transport is therefore not successful.

The transmitted pattern is a buffer of 1 k containing a counting pattern. The pattern is as follows: 00 FF FE FD etc. repeated 4 times.

7. CTC TEST

7.

This program is testing the counter timer circuit which is used for baud rate generator and as interrupt circuit for the CRT and the FDC controller.

It is tested that the circuit will generate interrupt and that the vector (interrupt address) is correct.

The four channels 0, 1, 2 and 3 are tested. Channels 0 and 1 are tested in counter mode, counting on the fixed input clock giving interrupt after approx. 423 µs. Channels 2 and 3 are tested in timer mode. The timer is for channel 2 started by the interrupt signal from the CRT controller. For channel 3 the timing is started automatically.

The test is based on a timeout loop, so it is checked if the interrupt was received within a specified time (300 ms.). It is also checked that only the specified channel interrupts.

The test can end up with 2 different error messages:

<illegal interrupt, port: xx>
meaning that another channel than the specified has interrupted.

<no interrupt, ch:>
meaning that the test has timed out before interrupt was received.

Texts will be written on the sixth line of the display.

8. FDC TEST 8.

The FDC test is a small test loop included in the big sequential loop of tests.

When the test is entered, it is checked that the main status register of the FDC has bit 7 set to indicate that the controller is ready.

After that, an invalid command is sent to the controller to see if it responds correctly.

The following three error messages could appear:

<not ready receive-transmit>:
bit 7 of the main status register was not set when entering the test.

<wrong data-direction>:
bit 6 of the main status register has wrong polarity.

<fault stat. reg.>:
status register 0 should indicate an invalid command (bit 7 = 1, bit 6 = 0).

Texts will be written on the seventh line of the display.

9. FDD TEST 9.

This test is testing the flexible disk controller and up to four connected drives, either 8" or 5 1/4". It is not a complete test of the flexible disk, but rather a fast verification of the basic functions of the controller and the drives connected to it.

If the system has not been informed that a keyboard is connected, this test is a part of the big sequential loop. If the system has been informed that a keyboard is connected, this test has to be selected by its number (number 5); that is, the big sequential loop does not involve this test.

Please note that before the FDD test is entered, a writeable diskette should be placed in the drive. For diskette stations connected to an RC700 Piccolo, it is recommendable only to use properly formatted diskettes of the type dual head, double side, soft sector, double density with the format 15 sectors/512 bytes on 8" diskettes and 9 sectors/512 bytes on 5 1/4" diskettes.

The test will initialize the controller to a step rate time of maximum 20 ms., a head unload time of maximum 160 ms. and a head load time of maximum 40 ms.

When the testing is initiated, the units which are ready, will be recalibrated. If no units are ready, the text <* all drives: not ready> will be written, and the test enters an idle state. Whenever a unit changes its state from not ready to ready, the testing will start on this unit.

If minidrives are used, the test will use some seconds to find out the drives which are ready.

Because of the READY signal when the drives are 5 1/4" diskette drives, they are only asked one time, if they are ready or not. This is done by trying a recalibration of the drives. Once a drive has been known ready or not, the testprogram expects it to be in this state throughout the test, also in looping. Every drive connected to the system is tested.

The testing sequence for a unit is first a recalibration and then the cyclic sequence, seek, write, read. Not the complete diskette is tested, but only the following 16 tracks are used for data recovery checkout:

For 8" units: 1, 66, 2, 65, 3, 64, 8, 40, 63, 9, 62, 36, 61, 37, 38, 39.

For 5 1/4" units: 1, 35, 2, 34, 3, 32, 8, 15, 31, 9, 30, 16, 29, 17, 25, 24.

The sector number varies from 1 throughout 9. On the first track the data checkout will be performed on sector 1, on the second track on sector 2 and so on.

The test pattern written on the diskette is a counting pattern of 512 bytes, which is transferred via the DMA controller channel 1. When the data is read from the diskette, it is placed in a buffer in the memory, and the write- and read-buffers are compared.

When the test is in loop mode, each byte of the test buffer is incremented by one for each pass.

If an error is detected one of the following errortexts till be written.

9.1 FDD Test Error Messages 9.1

<*fault in main status reg>

Indicates an error in the controller main status register bit 7 or 6.

<not ready>

Indicates that the ready state for a specified drive has been set to not ready (bit 3 of status register 0).

<write protected>

Indicates that the write protect bit has been set (bit 1 of status register 1).

<timeout>

The specified drive has not responded to an operation with an interrupt within approx. 2 s.

<*fault in fdc xx>

Indicates that the status bits of status register 0 are in an invalid state. xx is a hexadecimal number showing the contents of this register.

<seek error>

The drive could not find the specified track of the command issued (bit 5 of status register 0).

<command abort>

The command issued was invalid. The command was never started. It will appear if an earlier command was not terminated correctly (bit 7 = 1 and bit 6 = 0 of status register 0).

<door open>

The drive door has been opened during execution.

<recalibrate error>

The seek end bit did not occur after a recalibrate command (bit 5 of status register 0).

<track 0 signal not found>

The track 0 signal fails to occur after 77 step pulses (bit 4 of status register 0).

<missing address mark in datafield>

No address mark in the datafield (bit 0 of status register 2).

<missing address mark in id-field>

No address mark is detected in the id field (bit 0 of status register 1).

<bad cylinder>

The contents of the cylinder number on the medium are different from the internal register and cylinder number appears to be FF Hex (bit 1 of status register 2).

<wrong cylinder>

The contents of the cylinder number on the medium are different from the internal register (bit 4 of status register 2).

<cannot find sector>

The controller cannot find the sector specified in the internal register (bit 2 of status register 1).

<crc fault in id-field>

The CRC check discovered an error in the id field (bit 5 of status register 1, when bit 5 of status register 2 is zero).

<crc fault in data field>

The CRC check discovered an error in the data field (bit 5 of both status register 1 and 2).

<overrun>

If the controller is not services by the DMA controller within a certain time interval, the error occurs (bit 4 of status register 1).

<access beyond last sector>

The controller has tried to access a sector beyond the final sector of a cylinder (bit 7 of status register 1).

When one of the mentioned error messages, which has relation to a specific drive occurs, a heading is written before the message identifying the drive. The drives are numbered 0 through 3.

Texts will be written on the eighth line of the display.

10. WDC TEST 10.

This test is testing the WDC controller and up to two connected Winchester drives. It is not a complete test of the drives but rather a fast verification of the basic functions of the controller and the drives connected to it.

The test is only run if a controller is installed. This is signalled to the program by setting the switch S6 on the MIC board.

If the system has not been informed that a keyboard is installed, this test will be a part of the big sequential loop if the switch S6 is set.

If the system has been informed that a keyboard is connected, this test has to be selected by its number (number 6). Again, the test is only ran if switch S6 is set.

The system can be forced to perform the winchester test by pressing number 7, no matter what the switch is.

If switch 5 is set, the system is told that a winchester disk with 4 heads is used. With switch 5 reset, it means that a winchester disk with 6 heads is used.

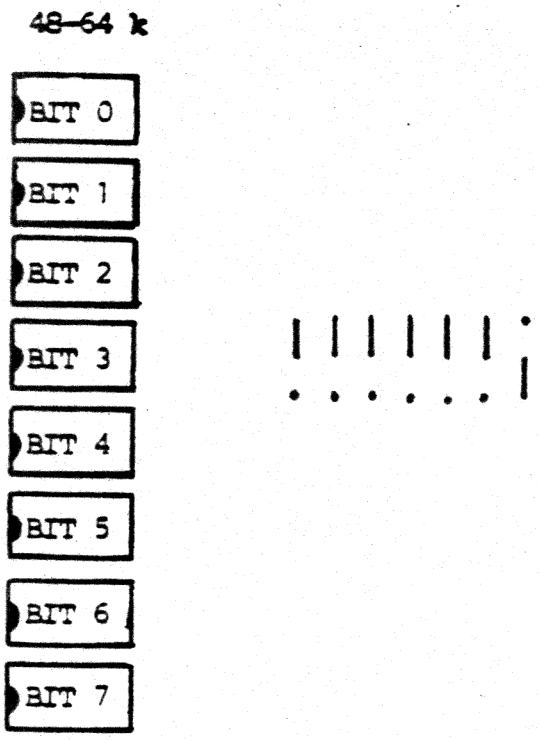

Figure 2: The switches 0-6 (here switch 6 is set).

The test will start with drive 0 and after finishing all the operation the program will check if there is a drive 1 connected, and in that case repeat the operation on drive 1.

When the testing is initiated, the unit will be restored. If there is no unit connected to the controller the texts "drive 0 timeout" or "no winchester drive on" will be written. No drives connected will be treated as an error.

The testing sequence for a unit is first a restore and then the cyclic sequence, format, seek, write, read. The whole Winchester disk is not tested but only cylinder 0 and 1. The system tests the winchester from head number 2 until head number 4 or 6 depending on switch number 5. This will avoid destruction of the configurationsector. A track contains 17 sectors and a sector contains 512 bytes. It is formatted with an interleave rate at 4:1 and no bad sectors.

The testpattern written is first a counting pattern from 0 to FF twice after the pattern is checked the same pattern but inverted is written and checked.

The CRC circuit is checked on the first cylinder.

The data are transferred via the DMA controller channel 0. In testing the CRC circuit the data read from the disk are placed in a buffer in the memory (E200-E3FF) and is compared with the writebuffer (E000-E1FF). If the CRC is found OK, the data on the rest of the cylinders are checked for CRC error.

10.1 WDC Test Error Messages

10.1

<no winchester drive on>

Indicates that no READY signal for drive 0 is recognized.

<cannot restore>

Indicates that the error bit in the status register is set.

<format error>

The error bit is set in the status register after a format operation.

<write error>

The error bit is set in the status register after a write operation.

<fault in crc-circuit>

Means that the CRC is wrong.

<data address mark not found>

Will be written after a READ SECTOR command if, after successfully identifying the ID field, the DATA ADDRESS MARK was not detected within 16 bytes of the ID field.

<aborted command>

Indicates that a valid command has been received that cannot be executed based on status information from the drive.

<id not found>

Indicates the ID field was not found.

<crc fault in id-field>

<crc fault in data field>

11. ERROR CODES 11.

The testrouter outputs an error code, which is specific for the type of error discovered on port 50 Hex. This enables the use to run the testsystem on a MIC board alone without display. The error information may then be detected if a device which can decode the numbers is installed on the system bus.

The error codes are as follow:

0: OK, no error
1: PROM checksum error
2: RAM error
3: data error in DMA test
4: DMA channel 1 has not set the terminal count bit within 200 ms. in DMA test
5: not used
6: not used
7: not used
8: not used
9: not wanted interrupt in CTC test
A: not used
B: CTC test has timed out without interrupt
C: not used
D: not used
E: not used
F: not used
10: not used
11: not used
12: not used
13: not used
14: not used
15: not used
16: not used
17: data error in main memory refresh test
18: FDC not ready to receive or transmit
19: the wrong data direction in FDC
20: FDC fault in status register
31: fault in FDC (in FDD test)

32: seek error
33: FDC command abort
34: open door
35: recalibration error
36: track 0 signal not found
37: missing address mark in data field
38: bad cylinder
39: wrong cylinder
3A: missing address mark in ID field
3B: cannot find sector
3C: CRC fault in ID field
3D: CRC fault in data field
3E: drive not ready
3F: overrun in FDC
40: trying to access beyond last cylinder
41: drive is write protected
42: flexible disk drive timeout
43: flexible disk data error
50: restore error in WDC test
51: timeout in WDC test
52: format error
53: seek error
54: write error
55: fault in CRC circuit
56: CRC fault in data field
57: data address mark not found
58: aborted command
59: ID not found
5A: CRC fault in ID field
5B: bad block detect error
5C: status/errorregister fault
5D: no drives on