SYSTEM CONTROL CONNECTIONS

SYSTEM CONTROL CONNECTIONS

Control of the entire CR80 system is carried out of the MBC or SCM module.
The distribution of the signals can be done either by diskret wiring, flat cable, printed circuit boards or a combination of these. The signals are used for different purposes, so as controlling the address sourcing modules access to the Main Bus, transmission of interrupt priority for the I/O interrupt received by the MBC/SCM and controlling of the CPU and overall system clear. The signals are connected with the 48 pin connector located at the MBC, SCH, above the standard Main Bus connector. The connector pin assignment is specified overleaf.

CHRISTIAN ROVSING A/S

TABLE 1

PIN ASSIGNMENT FOR SYSTEM CONTROL CONNECTION.

sign/date	page
repl	project

Pin no.	Signal Description	Pin no.	Signal Description	Pin no.	Signal Description
1a	GND	1b	BRQ 3	1c	
2a	GND	2b	BRQ 4	2c	
3a	GND	3b		3c	
4a	GND	4b	BRQ 0	4c	
5a	GND	5b	BRQ 1	5c	
6a	GND	6b	BRQ 2	6c	
7a	GND	7b	BG 3	7c	
8a	GND	8b	BG 4	8c	
9a	GND	9b		9c	
10a	GND	10b	BG 0	10c	
11a	GND	11b	BG 1	11c	
12a	GND	12b	BG 2	12c	PFL (L)
13a	INT (L)	13b	OACL (L)	13c	CC (H)
14a	GND	14b	LBG (L)	14c	P0
15a	GND	15b	TI (L)	15c	P1
16a	VCC	16b		16c	CPI (L)

SYSTEM CONTROL CONNECTIONS ELECTRICAL INTERFACE SPECIFICATION

The levels for all the System Control Connections are normal TTL logic levels i.e.

High level: $2.0V < V_H < 5.0V$
Low level: $0\ V < V_L < 0.8V$

The specifications below are for the numerical current values for one module connected with the signals.

Main Bus Authority Control Signals

BRQ (L), BG (L)

Driver: $I_{OL} \geq 48mA$

Receiver: $I_{IH} \leq 100uA$
$I_{IL} \leq 2mA$

LBG (L)
Open collector signal:

Driver: $I_{OL} \geq 48mA$
$I_{OH} \leq 100uA$

Reciever: $I_{IH} \leq 100uA$
$I_{IL} \leq 2mA$

Overall Clear

OACL (L)

Driver:	$I_{OL} \geq$ 48mA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 4mA

Power Failure Look Ahead

PFL (L)
Open collector signal:

Driver:	$I_{OL} \geq$ 48mA
	$I_{OH} \leq$ 100uA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 2mA

CPU Clear

CC (H)
Open collector signal:

Driver:	$I_{OL} \geq$ 60mA
	$I_{OH} \leq$ 100uA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 2mA

I/O Interrupt Signals & Timer Interrupt

INT (L), P0, P1, TI (L)

Driver:	$I_{OL} \geq$ 60mA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 2mA

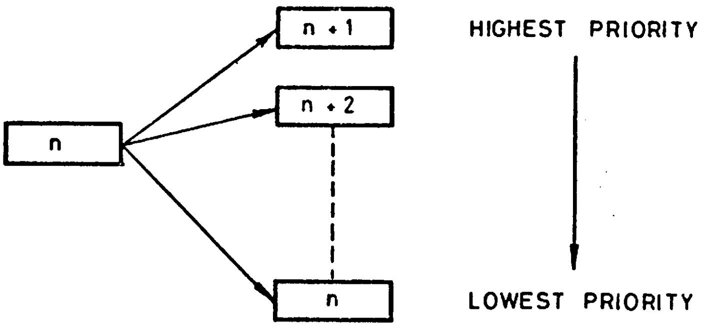
CPU Interrupt

CPI (L)

Open collector signal:

Driver:	$I_{OL} \geq$ 60mA
	$I_{OH} \leq$ 100uA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 2mA

Fig. 1



When module n (BRQn (L)) has the Main Bus authority module n + 1 will get the authority after n if it is requested, else the authority will go to the requesting module with the highest priority.

SYSTEM CONTROL CONNECTIONS FUNCTIONAL DESCRIPTION

The function and the timing specification for the different signals are described in the following section.

MAIN BUS AUTHORITY CONTROL

These signals BRQ, BG & LBG are used for controlling the address sourcing modules access to the Main Bus. There is one BRQ and one BG to each of the modules from the MBC, SCM and one common signal LBG (L) for all the modules which means that more Main Bus transfers can be executed uninterruptable (semaphore protection).

5 stk
ADDR sourcing
modules

When a module will access the Main Bus it issues its BRQ (L) to the system control module. The system control module has a priority scheme for the different BRQ so that all the received BRQ will be served without overhead time and so that the bus can be shared equal between the different address sourcing modules

When a module has issued BRQ and it is allowed to access the bus it will receive a BG (L) from the system control module which means that it has to start the transfer by enabling the Main Bus address line and issue a TRQ (L). The TRQ (L) has to be received in the system control module within 250 ns, else the bus authority will be distributed to another address sourching module. When the address sourcing module recognize the BG (L) it can disable BRQ (L) or if more accesses is wanted it can hold BRQ active.

The diagram on the next page fig. 1 specify the priority scheme and fig. 2 describe the timing specification and the handshaking procedure used for the authority control.

FIG. 2

MAIN BUS AUTHORITY CONTROL HANDSHAKING PROCEDURE

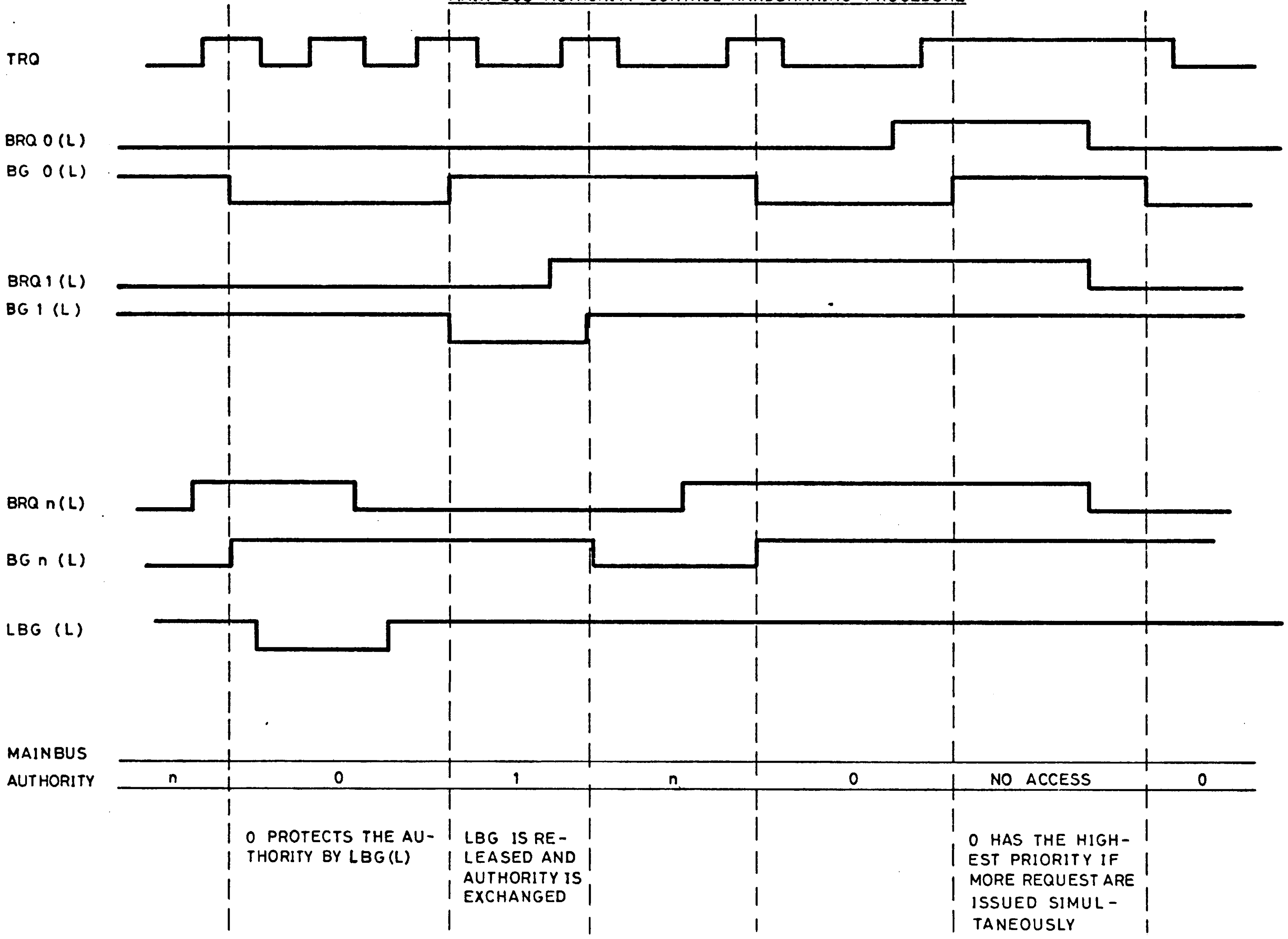
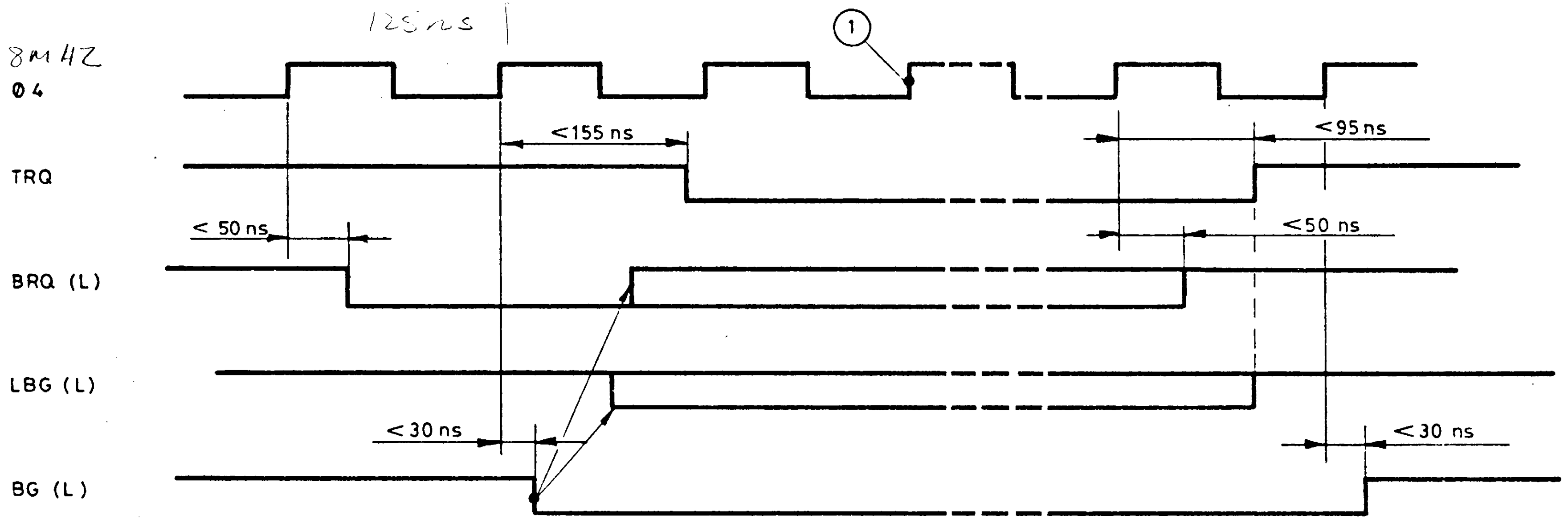

TRQ
BRQ 0 (L)
BG 0 (L)
BRQ 1 (L)
BG 1 (L)
BRQ n (L)
BG n (L)
LBG (L)
MAINBUS AUTHORITY
n
0
1
n
0
NO ACCESS
0
0 PROTECTS THE AUTHORITY BY LBG(L)
LBG IS RELEASED AND AUTHORITY IS EXCHANGED
0 HAS THE HIGHEST PRIORITY IF MORE REQUEST ARE ISSUED SIMULTANEOUSLY

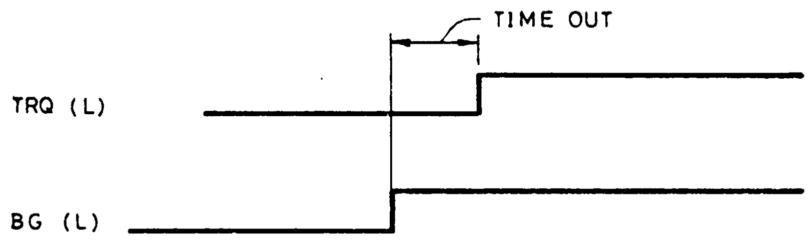
FIG. 3

MAIN BUS AUTHORITY CONTROL TIMING SPECIFICATION



Note 1: The first edge where authority may be changed if a module is accessing the Main Bus, if not the authority can be changed on all the rising edges of Ø4

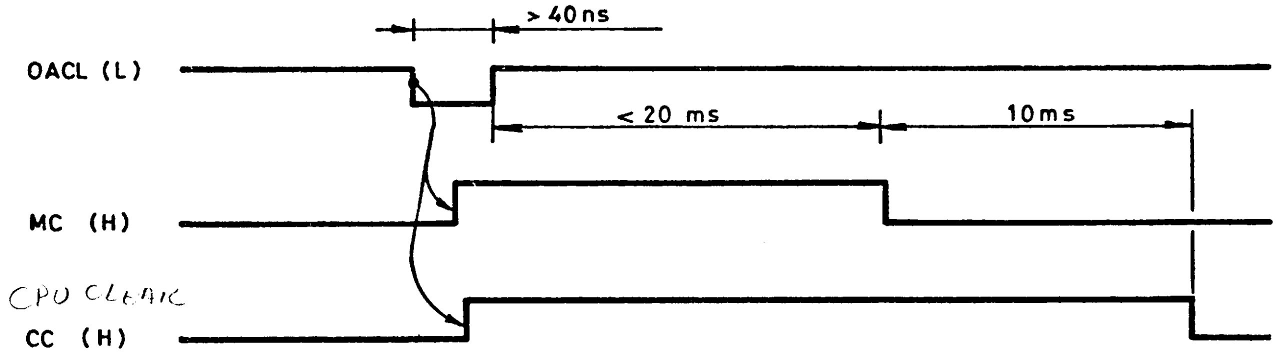
If the width of TRQ exceed 4 us (Time Out) BG (L) shall be disabled ref. timing diagram below.



OVERALL CLEAR

The Overall Clear signal OACL (L) is input to the system control module and is used for clearing of the entire CR80 system. The signal will immediately force CPU Clear CC (H) and Master Clear MC (H) high and thereby clear all the modules in the system. The signal OACL (L) and the response on it is specified in timing diagram below fig. 4.

Fig. 4

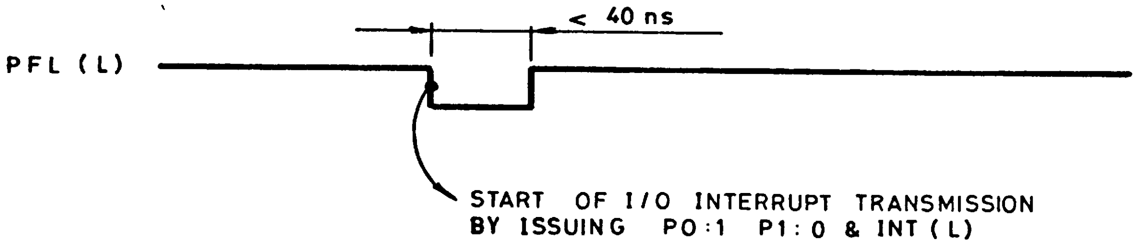


POWER FAILURE LOOK AHEAD

The signal is input to the system control module and is included in the system so that it is possible to get an advantaged power failure detection.

When the module recognize a low on PFL (L) it will issue an I/O interrupt with the highest priority level "3". When the CPU fetch the interrupt from the system control module, this interrupt will be transmitted before the other stored in the module.
The interrupt code for power failure is:
Priority 1 & Address 0.
Timing diagram fig. 5 specify PFL (L).

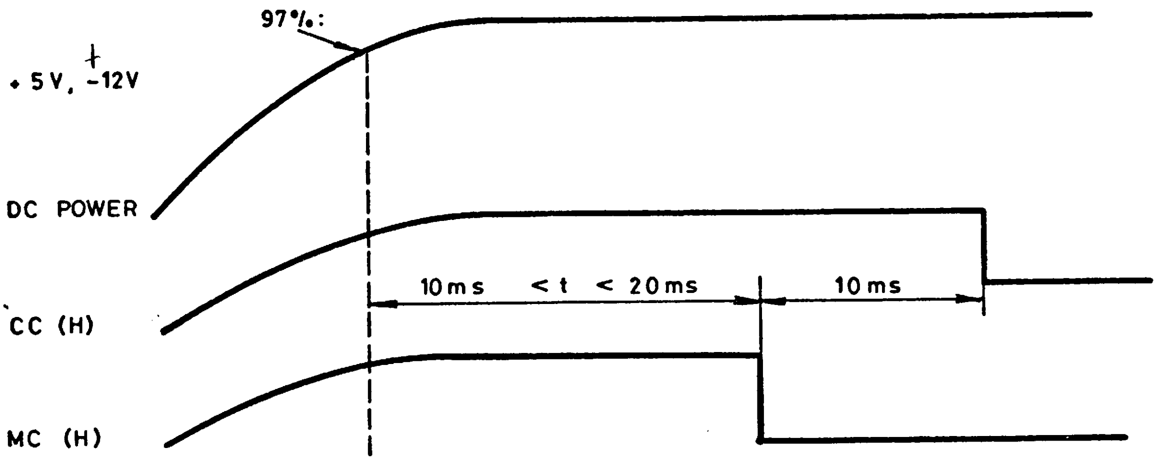
Fig. 5


< 40 ns
PFL (L)
START OF I/O INTERRUPT TRANSMISSION
BY ISSUING PO:1 P1:0 & INT (L)

CPU CLEAR

This signal CC (H) is generated by the system control module when power is switched on the system or when an OACL (L) is received (ref. fig.. 4). The signal is specified in fig. 6 below as a function of the standard DC Power's +5V, ±12V and the master clear signal.

Fig. 6



I/O INTERRUPT SIGNALS

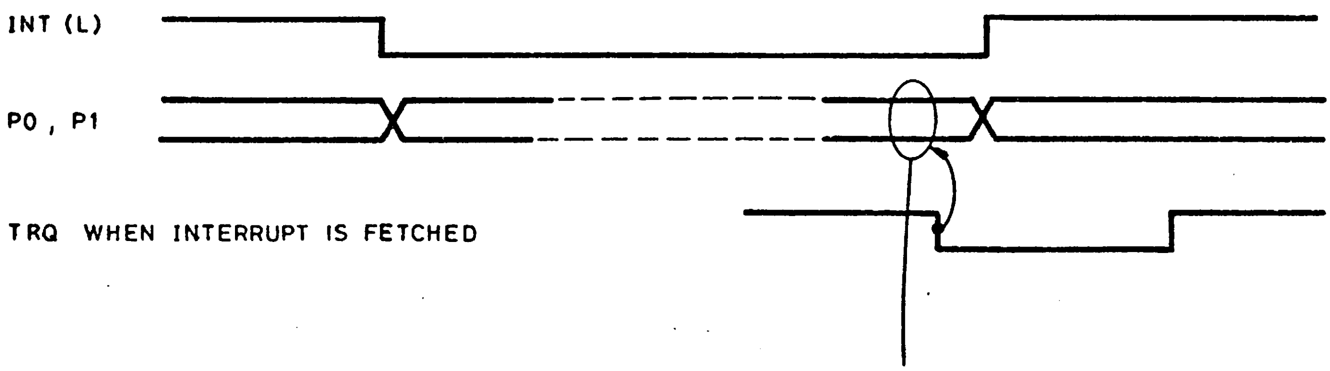
The three I/O Interrupt signals P0, P1 & INT (L) is issued from the system control module to all the CPU's in the CR80 system. The signals contain information about the current state of the interrupt queue located in the module. The contents of the lines is specified in table 2 below.

TABLE 2

INT (L)	P1	PO	STATE OF INTERRUPT QUEUE
1	Ø	Ø	QUEUE EMTY
0	0	0	PRIORITY 0 HIGHEST LEVEL
0	0	1	—"— 1 —"— —"—
0	1	0	—"— 2 —"— —"—
0	1	1	—"— 3 —"— —"—

The change of the signals is synchronized to TRQ (L), when an interrupt is fetched from the CPU, so that the CPU can use its internal generated TRQ for detecting whether it is a valid interrupt there is fetched during an interrupt fetch cycle, the timing diagram fig. 7 below specify the signals.

Fig.7

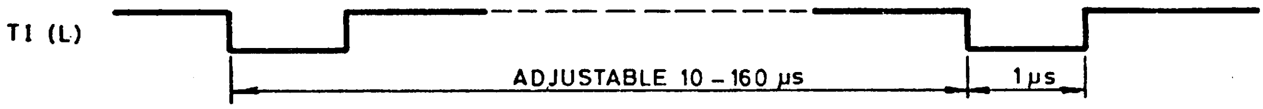


THE CONTENTS OF PO & P1
ON THE FALLING EDGE OF TRQ
IS THE INTERRUPT PRIORITY
FOR THE FETCHED INTERRUPT

TIMER INTERRUPT

The Timer Interrupt signal TI (L) is generated by the system control module and distributed to the CPU's in the system. TI (L) is strap selectable in the module and can be adjusted in steps of 10 us in the interval 10 - 160us.
Timing diagram fig. 8 specify the signal.

Fig. 8



CPU INTERRUPT

This line CPI is used by the CPU's in the system for transferring and receiving the special interrupt. The signal is located on the system control module, connector and the signal is terminated in that module but it could as well be terminated elsewhere in the system if it is a better solution seen from a system point of view.
The pulse transferred to the line has a nominal width of 125 ns and is active low.

CR80 MAIN BUS

CR80 MAIN BUS

There exist two different Main Bus types in the CR80 system, the Master Main Bus and the Slave Main Bus's. The difference between the Slave and the Master is that the Main Bus controlling modules are located in the Master.
The specifications for the signals are the same for Master and the Slave, and therefore no distinction is made in the following description.

The Main Bus consists of one or more printed circuit boards, Mother Boards connected together by active or passive Bus Extension so that the Mother Boards constitute a parallel transmission path terminated in each end by Bus Termination Boards.
The modules is connected to the Main bus by a 86 poled edge connector, containing the signals specified overleave:

● MAIN BUS CONNECTOR - PIN LAYOUT

2 x 43 pin edge connector rear view

	A		B	
	gnd	1	gnd	
	0	2	1	
	2	3	3	
	4	4	5	
DATA (DA)	6	5	7	DATA (DA)
	8	6	9	
	10	7	11	
	12	8	13	
	14	9	15	
	gnd	10	gnd	
	Auxiliary power	11	auxiliary power (same as All)	
	-12V	12	-12V	
	gnd	13	gnd	
	+12V	14	+12V	
	gnd	15	gnd	
	0	16	1	
	2	17	3	
	4	18	5	
	6	19	7	
	gnd	20	gnd	
ASSRESS (AD)	8	21	9	ADDRESS (AD)
	10	22	11	
	12	23	13	
	14	24	15	
	16	25	17	
	18	26	19	
	gnd	27	gnd	
UP	16	28	17	LP
	AUX	29	MC(H)	
	RS(L)	30	gnd	
	TRQ(L)	31	gnd	
	INA(H)	32	gnd	
	INR(L)	33	gnd	
	R/W(L/H)	34	gnd	
	Ø 1	35	gnd	
	Ø 2	36	gnd	
	Ø 3	37	gnd	
	Ø 4	38	gnd	
	gnd	39	gnd	
	+5V	40	+5V	
	+5V	41	+5V	
	gnd	42	gnd	
	gnd	43	gnd	

MAIN BUS ELECTRICAL INTERFACE SPECIFICATION POWER LINES

Aux. power	pin A11, B11
$-12V\ {}^{+\ 0.2V}_{-\quad 0V}$	pin A12, B12
Gnd	pin A13, B13
$+12V\ {}^{+\ 0.2V}_{-\quad 0V}$	pin A14, B14
$+5V\ {}^{+\ 0.2V}_{-\quad 0V}$	pin A40, A41, B40, B41
Gnd	pin A42, A43, B42, B43

The power lines are not feed through the Main Bus Extension and therefore different power supplies are used for the different Mother Boards.

The max. currents supplied through one connector are as specified below:

+12V, -12V,	I max:	2 A
+ 5V ,	I max:	12 A

SIGNAL LINES

The levels for all the Main Bus signals are normal TTL logic levels. i.e.:

High level: $2.0V \leq V_H \leq 5.0V$

Low level : $0V \leq V_L \leq 0.8V$

The load on the different signal lines for one module are as specified on the next page, (all currents are numerical values).

DATA LINES & ADDRESS LINES

DA0 - DA15, UP & LP, AD0 - AD19 & R/W (L/H).

3 - state signals with the followings requirements:

Drivers:		$I_{0H} \geq 5.2$ mA
		$I_{0L} \geq 16.0$ mA
		$I_{0\ off} \leq 100$ uA
Receivers:		$I_{IH} \leq 100$ uA
		$I_{IL} \leq 0.5$ mA
	(1)	$I_{IL} \leq 2$ mA

Note 1: This low level input current is only allowed when the module is addressed.

MASTER CLEAR

MC(H):
Open collector with the following requirements.

Driver:		$I_{0L} \geq 60$ mA
		$I_{0H} \leq 250$ uA
Receiver Schmitt Trigger:		$I_{IH} \leq 100$ uA
		$I_{IL} \leq 0.5$ mA
	(1)	$I_{IL} \leq 2$ mA

Note 1: I_{IL} 2 mA is only allowed for the Main Bus Controller & Main Bus Termination

TRANSFER REQUEST

TRQ (L):

Open collector or 3 - state signal with the following

requirements:

Driver:		I_{OL}	$\geq$ 80	mA
		I_{OH}	$\leq$ 250	uA
Receiver Schmitt Trigger:		I_{IH}	$\leq$ 100	uA
		I_{IL}	$\leq$ 0.5	mA
	(1)	I_{IL}	$\leq$ 2	mA

Note 1: I_{IL} 2 mA is only allowed for the Main Bus Controller & RAM modules with a memory area of 8K word or more.

CLOCK SIGNALS

Ø4 - Ø1:

Driver:	I_{OL}	$\geq$ 120	mA
	I_{OH}	$\geq$ 80	mA
Receiver Schmitt Trigger:	I_{IL}	$\leq$ 2	mA
	I_{IH}	$\leq$ 100	uA

MAIN BUS FUNCTIONAL INTERFACE SPECIFICATION CLOCK SIGNALS

Four clock signals Ø1 - Ø4 are generated from the MBC module or from an Active Bus Extension and transmitted to the bus.
The signals are used for synchronization of the I/O interrupt transmittion and for timing internal in the modules connected to the Main Bus.
The frequencies of the signals are:

Ø1	:	1MHZ	Pin	A35
Ø2	:	2MHZ	Pin	A36
Ø3	:	4MHZ	Pin	A37
Ø4	:	8MHZ	Pin	A38

The timing diagram overleaf specifies the clock signals.

I/O INTERRUPT SIGNALS

The CR80 I/O interrupt system is based upon a serial transmission, of the interrupt code, from the interrupting I/O module.

The serial code will be converted to parallel form by the Main Bus controller and transferred to the CPU's upon request.

Two of the Main Bus lines are used for I/O interrupt transmission:
INR Interrupt Request & INA Acknowledge.

The interrupt code consisting of 8 bit is transmitted to the INR line synchronous with the 1 MHZ signal Ø1.

INR is an open collector line so that all the I/O modules can transmit on the same line, which means that if a module is transmitting a "0" and an other a "1", the line will contain the "0".

INA is an open collector line too, because it is driven from the Main Bus termination boards, one in each end of the Bus. The contents of INA is INR inverted. The interrupting I/O module compare for each of the eight bits the contents of INA with the bits they are transmitting to INR. If the compare does not match which means that a module with a higher interrupt code is transmitting at the same time, the module disable the transferring of its code to INR until the next 1 MHZ periode.

On that way the contents of INR will be unique and correspond to the highest interrupt transmitted during that period. The module which detects this situation will stop the interrupt sending.

The diagram below illustrate the function and the connection of the I/O interrupt circuit:

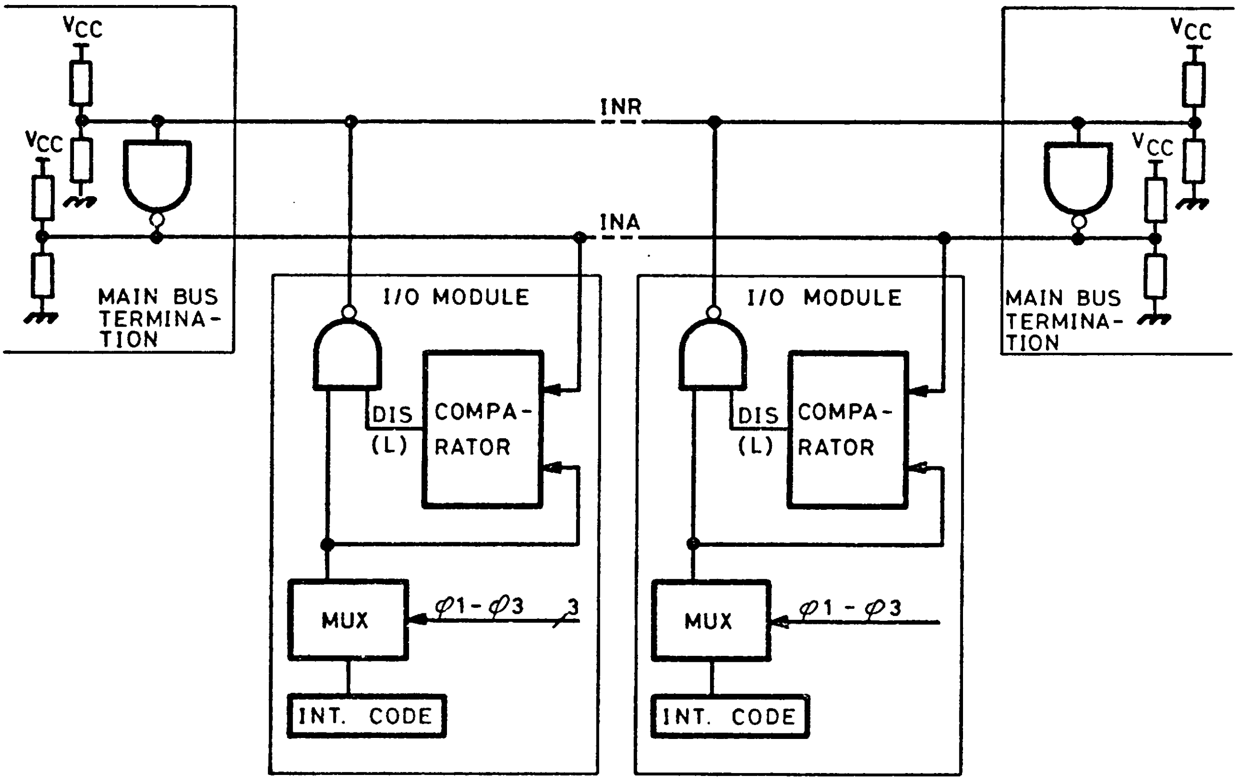


Fig. 2

The 8 bits interrupt code consist of two parts; a 2 bits priority corresponding to four levels and a 6 bits module address corresponding to 64 modules which can operate with I/O interrupt. Two of the 64 module addresses are restricted: The address 00 will not be recognized because it correspond to no module is sending interrupt and the address 63 which is used by the MBC when its internal interrupt queue is full and it therefore has to queue the interrupts directly on the Main Bus.

When an I/O module will transmit an interrupt it start with priority bits and continue with the address bits ref. timing diagram fig. 3.

MASTER CLEAR

The Master Clear signal MC(H) is generated by the Main Bus Controller when power is switched on or when commanded by the CPU. The signal is active high and have a width of min. 10 ms ref. fig 4.

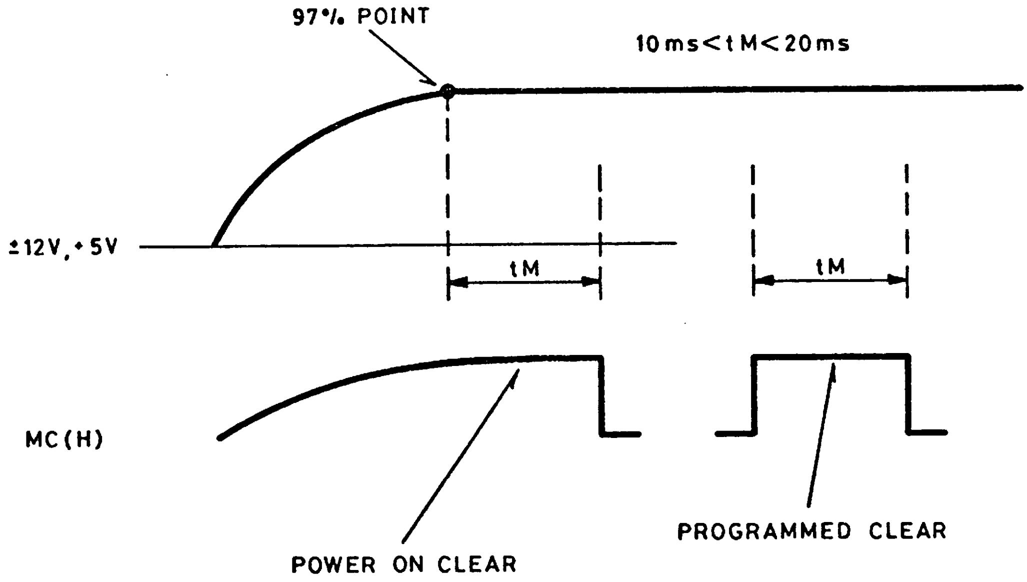


Fig. 4

When the I/O modules recognize a Master Clear they have to reset all there internal functions to the start up condition.

The memory modules may not use the Master Clear signal, but only the power up sequence for resetting.

DATA LINES

The data communicated on the CR80 Main Bus are 16 bits + 2 parity bits. The data lines are bidirectional controlled by the R/W (L/H) line. When R/W (L/H) is logic "0" during a datatransfer the addressed module have to control the contents of the data lines. If the addressed module is a memory module the contents of the parity lines correspond to odd parity for both Up and Lp. Lp referring to data bits 0-7; DA0 Lsb and Up referring to 8-15; DA8 Lsb.
During byte transfer on the Main Bus both Up and Lp have to be correct without regard to the addressed byte.

If the addressed module is an I/O module the contents of the parity lines are ignored which means that the I/O modules do not operate with parity.

For the timing specification on the Main Bus data lines ref. Main Bus Communication, fig. 6 and fig. 7.

Address Lines

21 lines AD0 - AD19 and R/W (L/H) are used to specify the address and the function of the data transfer. The address source is the CPU - or DMA modules.
Read/write R/W (L/H) specify the data source/destination if low the source is the addressed module if high the addressed module is the data destination. AD19 & AD18 specify whether the module is an I/O or a Memory module ref. table on the next page.

AD19	AD18	Data Source / Destination	
0	0	I/O module	
0	1	lower byte DA0 - DA7	Memory module
1	0	upper byte DA8 - DA15	
1	1	Word DA0 - DA15	

During memory transfer AD0 - AD17 is the word pointer (AD0; LSB), corresponding to 256K word. During I/O transfer AD17 is used for separation of Sense I/O (SIO), Control I/O (CIO) and Read I/O (RIO), Write I/O (WIO), the table below specify the bit pattern and the corresponding function during I/O. AD16 is undefined when an I/O transfer take place.

R/W (L/H)	AD17	Function
0	0	SIO
0	1	RIO
1	0	CIO
1	1	WIO

The remaining part of the address field AD15 - AD0 is used for addressing of a specific module, Submodule or/and instruction for the addressed module. The address bits AD0 - AD5 is used as module address and correspond to the six LSB in the I/O interrupt code while the remaining address bits AD6 - AD15 can be used as subaddress or instruction. This I/O addressing scheme means that there can be 1K I/O modules within one module address if the modules do not operate with interrupt.

The table below specify the address field and the functions.

R/W (I/H)	19	18	17	16	15 AD 6	5 0	FUNCTION	MODULE
0	0	0	0	0	SUB ADDRESS OR INSTRUCTION	MODULE ADDRESS	SIO	I/O
0	0	0	1	0			RIO	
1	0	0	0	0			CIO	
1	0	0	1	0			WIO	
0	0	1	WORD ADDRESS, ADD0 : LSB				READ LOWER BYTE	MEMORY
1	0	1					WRITE LOWER BYTE	
0	1	0					READ UPPER BYTE	
1	1	0					WRITE UPPER BYTE	
0	1	1					READ WORD	
1	1	1					WRITE WORD	

TRANSFER CONTOL SIGNALS

Two signals are used for controlling the transfer on the Main Bus; Transfer Request TRQ(L) and Respons RS(L). TRQ(L) is issued from the address sourcing module (CPU/DMA) and RS(L) is issued from the addressed module I/O/Memory).

The handshaking procedure for the signals is specified in fig. 5 below, for the timing requirements ref. Main Bus Communication, fig. 6 and fig. 7.

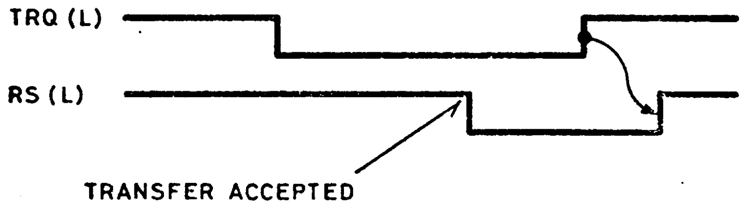


Fig. 5

MAIN BUS COMMUNICATION

This part describe the timing specification for the two different module types connected to the CR80 Main Bus, the address sourcing modules (CPU/DMA) and the address destination modules (I/O / Memory).

Address Sourcing Modules:

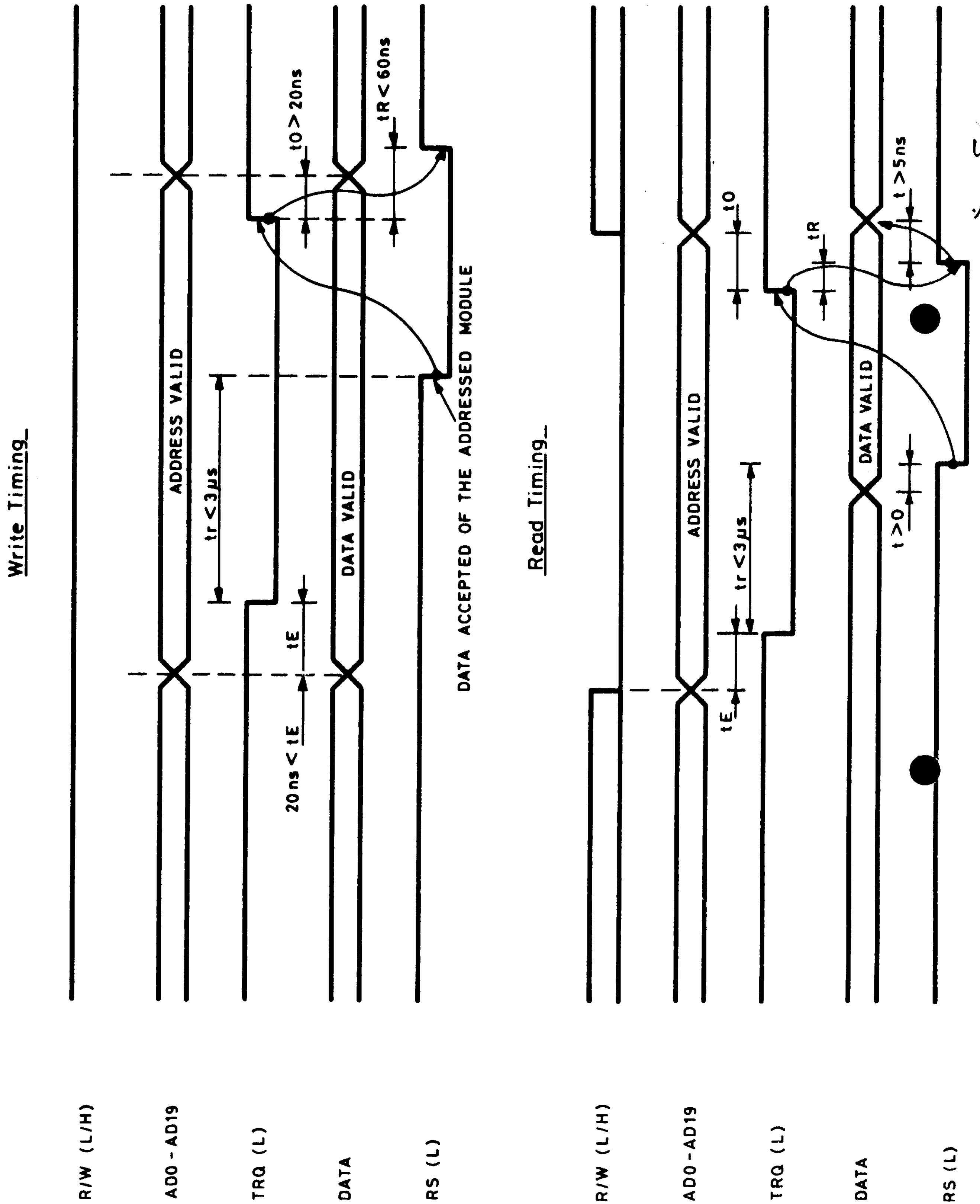
The CPU's and DMA modules gets control of the Main Bus by requesting the MBC. The signals used for the control of the Main Bus access are Bus Request (BRQ(L)) Bus Grand (BG(L)) and Lock Bus Grand (LBG(L)). When a module wishes the authority over the Main Bus it issue an BRQ(L). When the module receives an BG(L) the Main Bus is free and the module can execute its transfer on the Bus. If the module operates with semaphore the signal LBG(L) can be issued and on that way lock the Main Bus authority to the module so that more than one Main Bus transfer can be executed uninterruptable. The signal used for the Main Bus Authority Control is not located on the Main Bus but are seperate wires from the Main Bus Controller to the address sourcing modules.
The timing diagram fig. 6 specify the relationships between the different signals involved during a Main Bus transfer. If TRQ(L) is active more than 4 us the MBC will disable BG(L) and thereby terminate the transfer. This shall be detected in the module as a time out. If a module recognize a BG(L) without requesting the Bus BRQ(L) it may not start a transfer, that means the modules shall disable the effect of BG(L) until requesting for the Bus.

The modules which sense on the Main Bus address lines are seperated in two different types, the I/O modules and the memory modules with regards to the Main Bus timing there is no different in the two types.
The timing diagram fig.7 specify the relationship

between the different signals involved in the Main Bus transfer.

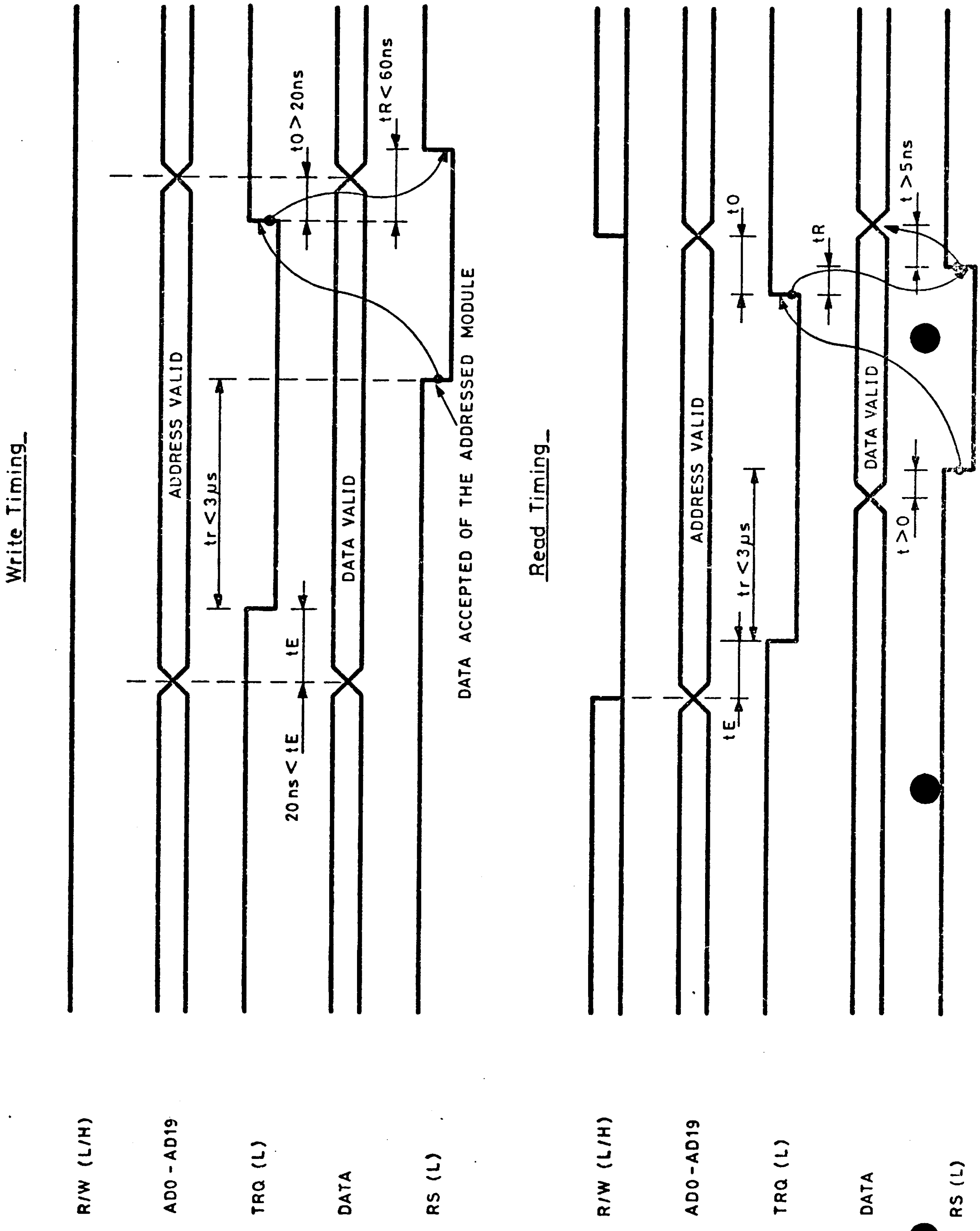
Timing Specifications for Address Destination Modules.

Fig.7



Timing Specifications for Address Destination Modules.

Fig.7



CR80 SUB BUS

CR80 SUB BUS

The CR80 Sub Bus is a local bus which is not distributed throughout the system, but used for interconnection of a limited number of modules. There is no specific limit on the number of Sub Buses in a CR80 system. The Sub Bus is a semi synchronous bus where the address and the data are multiplexed on the same lines. The following different modules can be connected to the Sub Bus, memory modules, Func modules, DMA & CPU modules.

There can in the standard configuration be connected two address sourcing modules i.e. CPU & DMA, two CPU's or two DMA channels to one bus. The number of address destination modules i.e. memory, func modules are limited by the physical dimension of the Sub Bus print board. The maximum length of the bus is 172mm corresponding to ten connector positions.

The Sub Bus consist of a printer circuit board equipped with 48 poled print connector for interconnection of the modules, the pin configuration of the connector is specified in table 1.

The Sub Bus carries, beside the signals relevant for data transfer (SB0 - SB23, ATR(L), DTR(L), FEN(L), MRS(L) & FRS(L)), some signals used for system control:

The system control connections are described in the section System Control Connections.

TABLE 1

sign/date	page
repl	project

CR80 SUB BUS

48 Pin Connector Pin Assignment

Pin no.	Signal Description	Pin no.	Signal Description	Pin no.	Signal Description
1a	~~BG (L)~~	1b	GND	1c	~~BRQ(L)~~
2a	SB2	2b	SB1	2c	SB0
3a	SB5	3b	SB4	3c	SB3
4a	SB8	4b	SB7	4c	SB6
5a	SB11	5b	SB10	5c	SB9
6a	SB14	6b	SB13	6c	SB12
7a	SB17	7b	SB16	7c	SB15
8a	SB20	8b	SB19	8c	SB18
9a	SB23	9b	SB22	9c	SB21
10a	GND	10b	GND	10c	~~CC(H)~~
11a	~~LBG(L)~~	11b	~~PO~~	11c	~~INT(L)~~
12a	~~CPI(L)~~	12b	~~TI(L)~~	12c	~~P1~~
13a	SRQ2	13b	FRS(L)	13c	MRS(L)
14a	DTR(L)	14b	FEN(L)	14c	SRQ1
15a	ATR(L)	15b	GND	15c	GND
16a	AUX1	16b	AUX2	16c	AUX3

SUB BUS ELECTRICAL INTERFACE SPECIFICATIONS

The levels for all the Sub Bus signals are normal TTL logic levels i.e. :

High level:	$2.0V < V_H < 5.0V$
Low level:	$0 \ V < V_L < 0.8V$

The specifications below are for the numerical current values allowed for one module connected to the Sub Bus:

ADDRESS & DATA LINES

SB0 - SB23

3 - state signals with the following requirements:

Drivers:	$I_{0H} \geq 5.2mA$
	$I_{0L} \geq 16.0mA$
	$I_{0\ off} \leq 100\ uA$
Receivers:	$I_{IH} \leq 100\ uA$
	$I_{IL} \leq 0.5mA$
	(1)$I_{IL} \leq 2.0mA$

Note: This low level input current is only allowed when the module is addressed or if it is an address sourcing module i.e. CPU or DMA.

TRANSFER CONTROL SIGNALS

ATR(L), DTR(L), MRS(L), FEN(L), FRS(L).

Open collector or 3 - state enabled when active signals with the following requirements:

Drivers:	$I_{0L} \geq 40\ mA$
	$I_{0H} \leq 100\ uA$

Receivers:

Schmitt Trigger:	I_{IH}	$\leq$	100 uA
	I_{IL}	$\leq$	2.0mA

SUB BUS AUTHORITY SIGNALS

SRQ 1(L) & SRQ 2(L)

Open collector - or 3 - state enabled when active, signals with the following requirements:

Drivers:	I_{0L}	$\geq$	40 mA
	I_{0H}	$\leq$	100 uA

Receivers:

Schmitt Trigger:	I_{IH}	$\leq$	100 uA
	I_{IL}	$\leq$	4.0mA

AUXILIARY SIGNALS

The three auxiliary signals Aux 1 - Aux 3 is available for special use in the system and therefore not specified in this document.

SUB BUS INTERFACE FUNCTIONAL DISCRIPTION

The following paragraphs describes the interface from a functional point of view. Furthermore the timing specification for the signals are included in the timing diagrams.

The communication on the Sub Bus is devided in two phases; the address - and the data phase. When data is communicated between a memory module and a DMA/CPU the address is transferred to the memory in the address phase and the data to/from the memory in the data phase. If the communication is between a func module and a CPU module only the data phase is used.
Control of the Sub Bus lines SB0 - SB23 is carried out by the signals ATR(L) (address phase) and DTR(L) or FEN(L) (data phase). The specification for the different

Sub Bus lines is as described in the table 2 overleaf.

The func module communication can be carried out in more different ways. During the data phase the CPU can transfer/receive data from the func modules controlled by SB18 - SB23. If the data communication is between the func and the memory this two module types can be linked together so that data to/from the two modules can be carried out in one bus cycle.

TABLE 2

		FUNCTION		
PIN NO.	SIGNAL NAME	ADDRESS PHASE	DATA PHASE	
c2	SB 0	Add. 0 (LSB)	DAT 0	(LSB)
b2	SB 1	Add. 1	DAT 1	
a2	SB 2	Add. 2	DAT 2	
c3	SB 4	Add. 3	DAT 3	LB
b3	SB 4	Add. 4	DAT 4	
a3	SB 5	Add. 5	DAT 5	
c4	SB 6	Add. 6	DAT 6	
b4	SB 7	Add. 7	DAT 7	
a4	SB 8	Add. 8	DAT 8	
c5	SB 9	Add. 9	DAT 9	
b5	SB 10	Add. 10	DAT 10	
a5	SB 11	Add. 11	DAT 11	UP
c6	SB 12	NV	DAT 12	
b6	SB 13	NV	DAT 13	
a6	SB 14	NV	DAT 14	
c7	SB 15	Add. 18	DAT 15	
b7	SB 16	Add. 19	LP	
a7	SB 17	R/W (L/H)	UP	
c8	SB 18	Add. 12	FAdd. 0	
b8	SB 19	Add. 13	FAdd. 1	
a8	SB 20	Add. 14	FAdd. 2	
c9	SB 21	Add. 15	FCont. 0	
b9	SB 22	Add. 16	FCont. 1	
a9	SB23	Add. 17	FCont. 2	

SUB BUS ADDRESS SOURCING MODULE TIMING

The address sourcing modules connected to the CR80 Sub Bus i.e. CPU/DMA modules shall observe the specification description under memory and func modules as well as the specification for Sub Bus authority control ref. fig. 1.

ADDRESS PHASE

In the address phase the Sub Bus lines is used for memory addressing, table 3 below specify the function, and the timing specification is described in the section Sub Bus Communication.

TABLE 3

R/W	ADDRESS BITS			FUNCTION
(L/H)	19	18	17 0	
Ø	0	0		NOT ALLOWED
0	0	1	MEMORY WORD ADDRESS ADD 0: LSB	READ LOWER BYTE
0	1	0		READ UPPER BYTE
0	1	1		READ WORD
1	0	1		WRITE LOWER BYTE
1	1	0		WRITE UPPER BYTE
1	1	1		WRITE WORD

The contents of the signals SB12 - SB14 during the address phase is undefined.

Timing Diagram for Sub Bus Authority Control

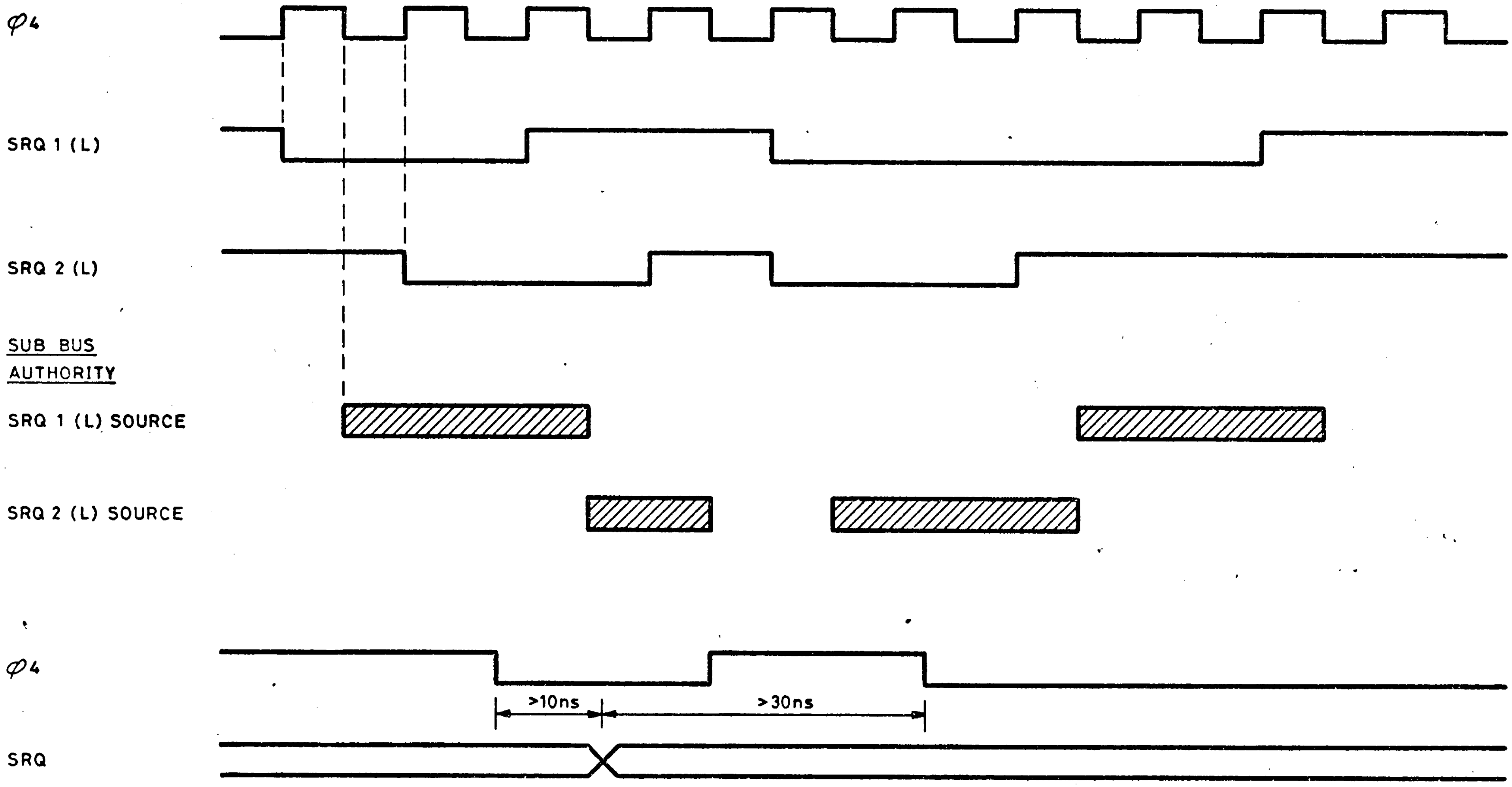


Fig. 1

DATA PHASE

In the data phase the Sub Bus signals are used for transferring the data between the different modules, and at the same time the signals SB18 - SB23 are used for addressing and control of the func modules connected to the bus (F Add 0 - 3) & (F Cont. 0 - 3). This func addressing scheme means that up to eight func modules each with eight control function can be connected to one Sub Bus.
The data word consist of 16 bits + 2 parity bits, one for lower byte L P and one for upper byte U P. The parity used is odd and both parity lines have to be valid during all Sub Bus transfers, byte as well as func transfer.

SUB BUS COMMUNICATION

This part specify the timing relationship and the handshaking procedure for the Sub Bus signals.

When a address sourcing module will start a transfer on the bus it must first get the control of the bus by use of the two signals Sub Bus Request 1 & 2 (SRQ 1(L), SRQ 2(L)). The two DMA/CPU modules which can be connected to the bus can each driver one of the lines and use the other, to detect whether the other module is transferring on the bus or not The DMA/CPU modules connected to the Sub Bus shall have a switch so that it can be selected which of the two SRQ signals it can control.
The module which control SRQ 2(L) has the highest priority, meaning that if SRQ 1(L) and SRQ 2(L) is issued simultaneously from the two modules, it is the module driving SRQ 2(L) there will get the authority over the bus. Timing diagram fig. 1 defines the handshaking procedure and the timing specification for the SRQ signals. The modules have to make the decision whether to access the bus or not on the falling edge of Ø4.

When a module has got the Sub Bus authority it shall start the transfer as soon as possible. The preferred transfer start is at the falling edge of Ø4 when it recognize it has the authority over the bus. The bus authority shall if possible be released by disabling SRQ as soon as the module recognize the respons signal from the addressed module so that no overhead time exist on the Sub Bus.

When a DMA/CPU will access a memory module it starts the sequence by issuing its SRQ and when it gets the Sub Bus authority it transfer the memory address and R/W signals to the bus and for the phase definition the address transfer signal ATR(L). When the addressed modules detect this condition it at once, respons with the memory respons signal MRS(L). The memory modules has to respons very quickly because the CPU's if it do not detect a MRS(L) in the address phase, has to start up a transfer on the Main Bus.

When the address sourcing module has detected MRS(L) it start the data phase by issuing DTR(L) and dependent of the state of SB17 R/W (L/H) in the previously address phase the memory module or the CPU/DMA module transfer the data information to the bus lines SB0 - SB17.

When the memory module has accepted the data transfer it again respons by the signal MRS(L) and the address sourcing module terminates the data phase by releasing DTR(L and if no further transfer is wanted SRQ. If the memory do not respons DTR(L) with MRS(L) within 4us the module shall terminate the transfer and recognize it as a Time Out.

Timing diagram fig. 2 specify the handshaking procedure for this transfer mode (CPU↔Mem.)

A CPU to/from func module transfer is started by SRQ but there is no address phase as during memory transfer. When the CPU get the authority over the Sub Bus it transmit a Func Enable FEN(L) and the six bit SB18 - SB23, specifying the func module and the function, to the Sub Bus and dependent of the function the remaining part of the signals SB0 - SB17 will be driven from the CPU or the func module.

If the addressed module has not responded within 4us it will be interpreted as a time out condition. Timing diagram fig. 3 specify the handshaking procedure for the Sub Bus transfer mode CPU↔Func.

The last possible transfer types on the Sub Bus is the transfer of data between memory and func modules. This transfer start with an address phase where the actual memory module is set up, and dependent of the transfer direction the signal DTR(L) or FEN(L) is issued and when the CPU detects the corresponding respons it transfer the opposite signals to the bus and terminates the transfer when the last issued signal is responded. The time out is detected when one of the signals DTR(L) and FEN(L) has been active more than 4us.
Timing diagram fig. 4 & 5 specify the handshaking procedure for the Sub Bus transfer mode Func↔Mem.

Sub Bus Transfer CPU/DMA → Memory

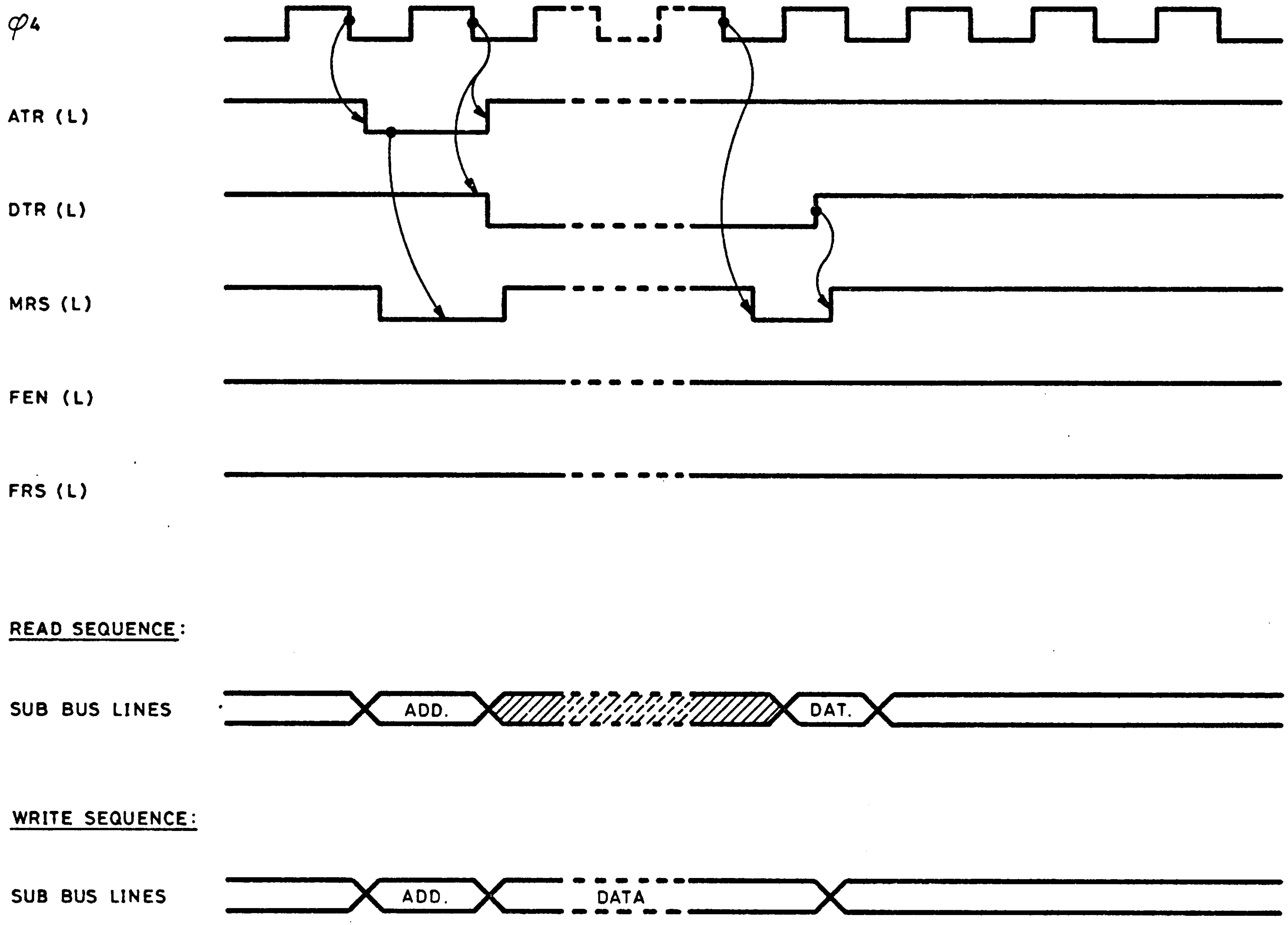


Fig.2

Sub Bus Transfer CPU → FUNC

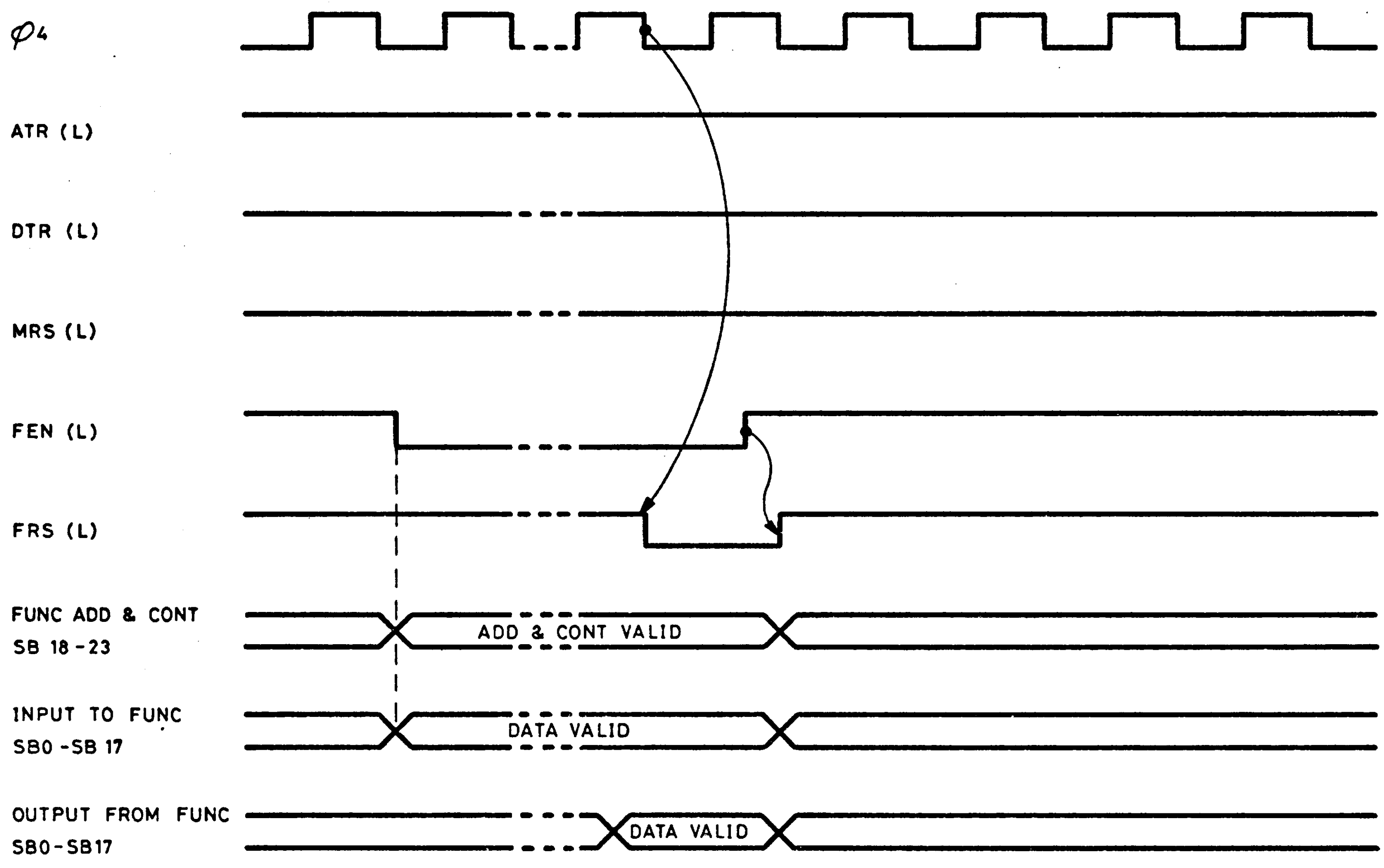


Fig. 3

Sub Bus Transfer FUNC → Memory

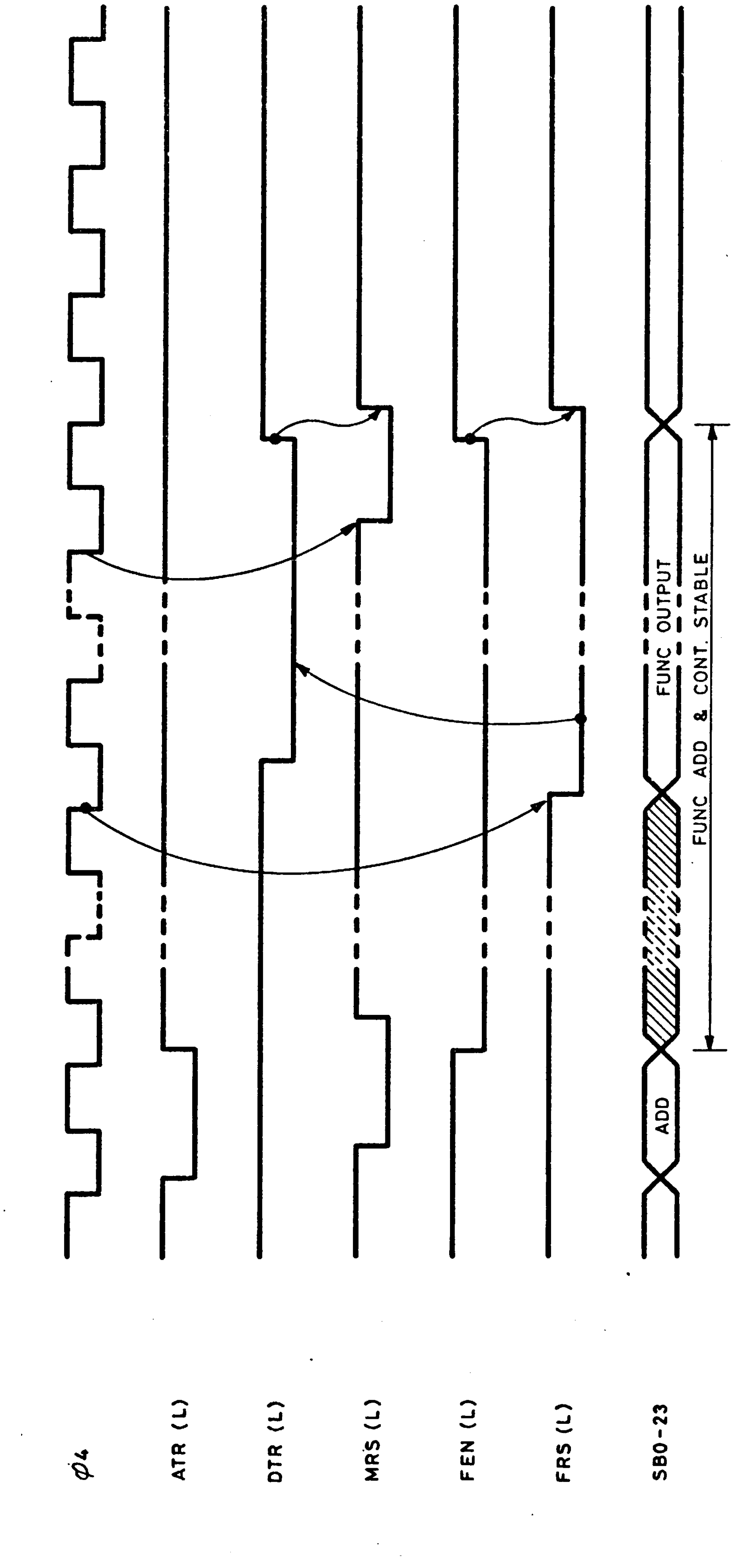


Fig. 4

Sub Bus Transfer Memory→FUNC

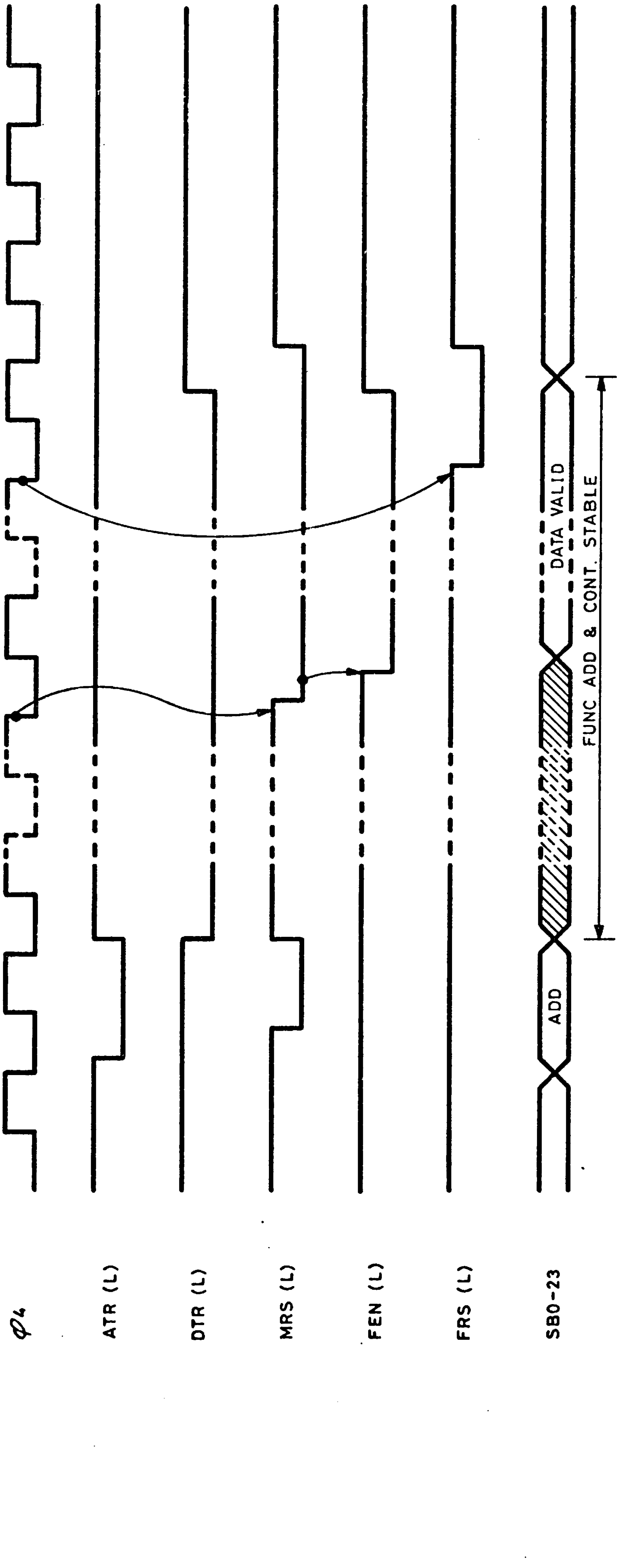
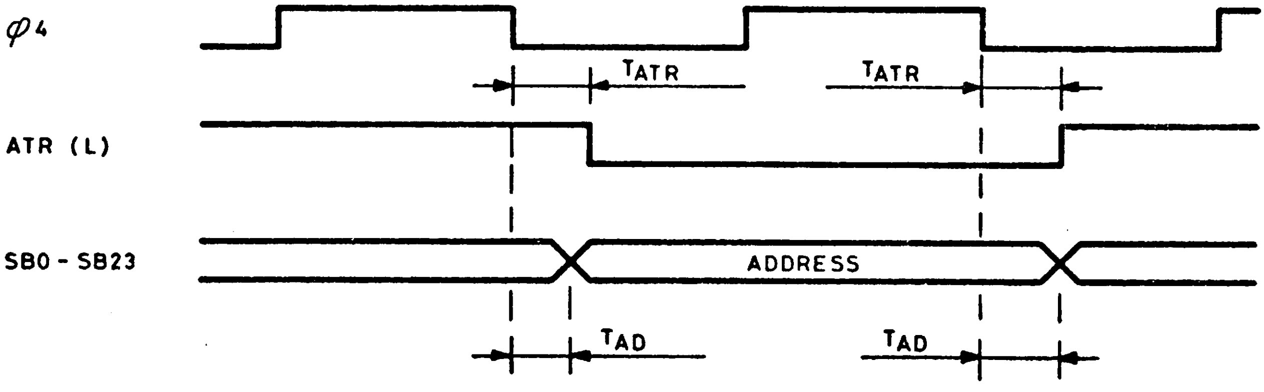


Fig. 5

SUB BUS MEMORY TIMING

This section describes the timing specification for memory modules connected to the CR80 Sub Bus. The communication on the Sub Bus is semisynchronous, meaning that the address transfer from the address sourcing modules and the respons from the memory have to be issued on the edge of the master timing frequence Ø4, the remaining specification is asynchronous. The memory address and the address transfer signal ATR(L) issued from a CPU/DMA will be within the timing limits specified in fig. 6 below.



$0 < T_{ATR} < 25ns$

$0 < T_{AD} < 35ns$

Fig. 6

When a memory recognize its address and ATR(L) it has to respons immediately with MRS(L) and store the address so that it can be used during the data phase. The timing specification for the memory respons on an ATR(L) is specified in fig. 7 below.

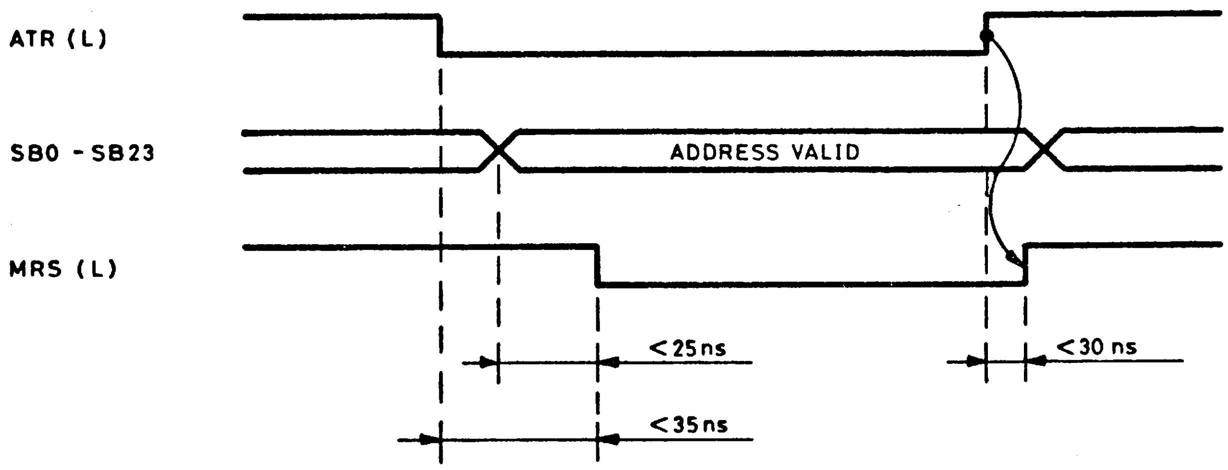


Fig. 7

The data phase can be started immediately after the address phase or it can be delayed, if it is a func→memory transfer, until the func module has responded and the data from the func is transferred to the Sub Bus, therefore the data phase is asynchronous and not locked to the signal Ø4 seen from the memory. The specification for the data phase is shown in fig. 8 for memory read and in fig. 9 for memory write.

Memory Read

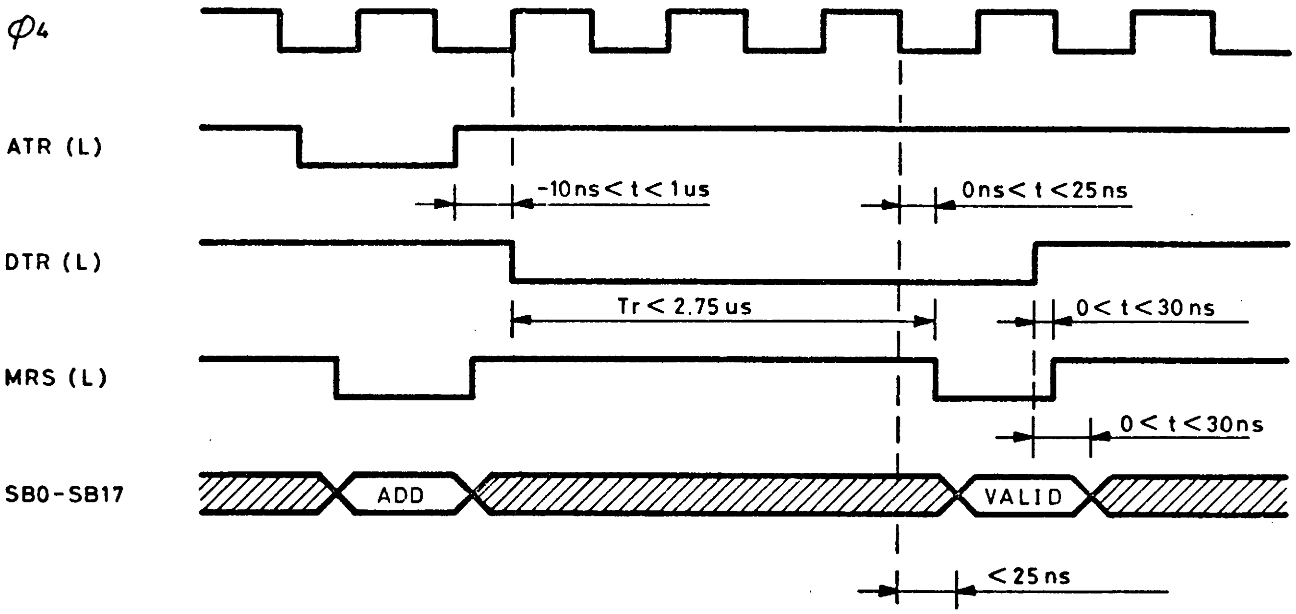


Fig. 8

Memory Write

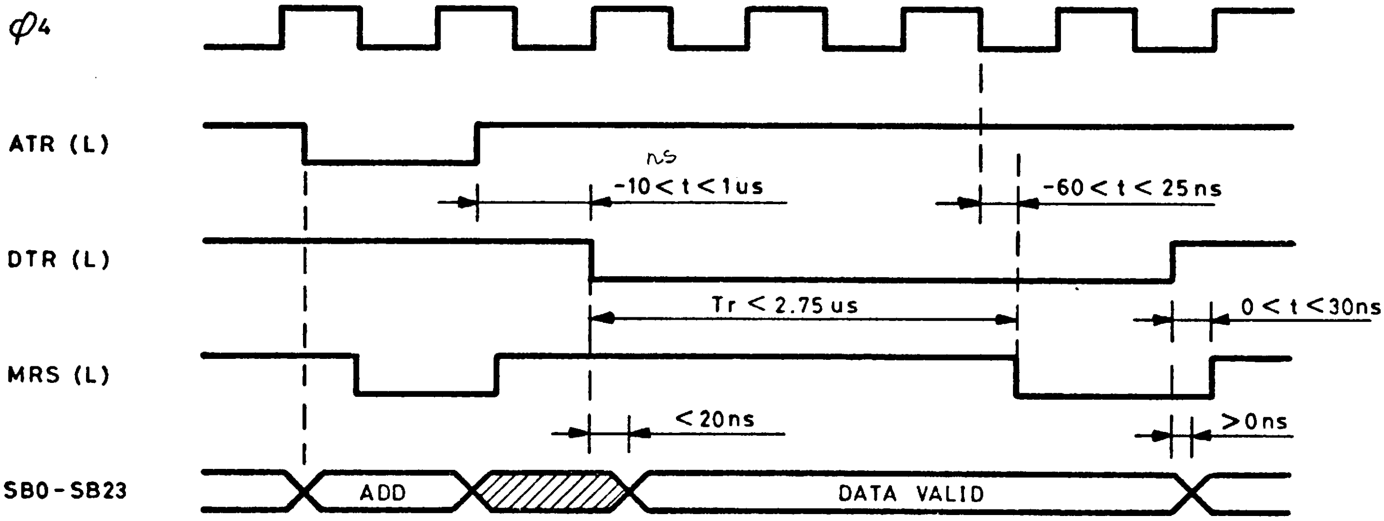


Fig. 9

FUNC TIMING

The Func modules do only use the data phase on the Sub Bus because of the lines SB18 - SB23 are restricted for func addressing and control during this phase. For the handshaking two separate signals are used so that the func module and a memory can be linked together in the data phase. The timing diagrams fig. 10 specify the func out timing and fig. 11 specify the func in timing.

Func. Output Timing

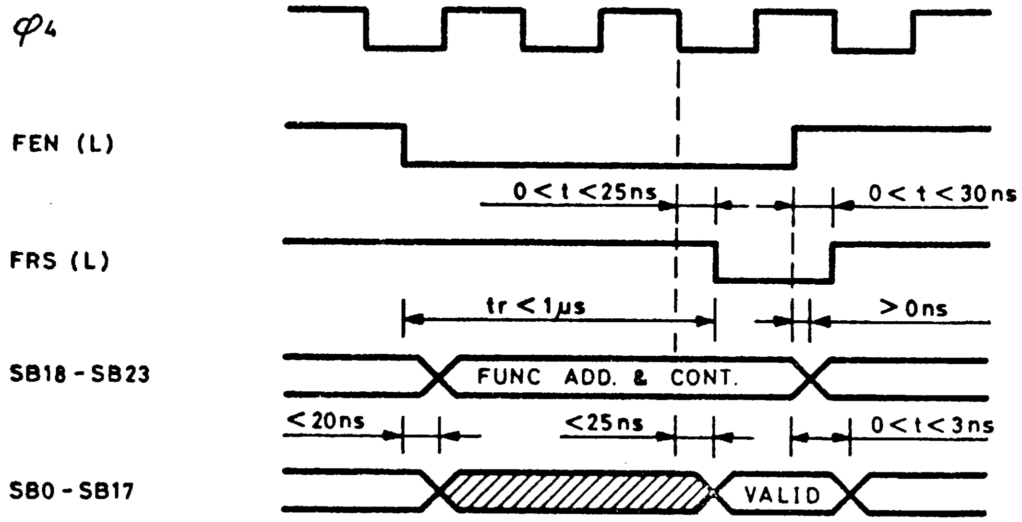


Fig. 10

Func. Input Timing

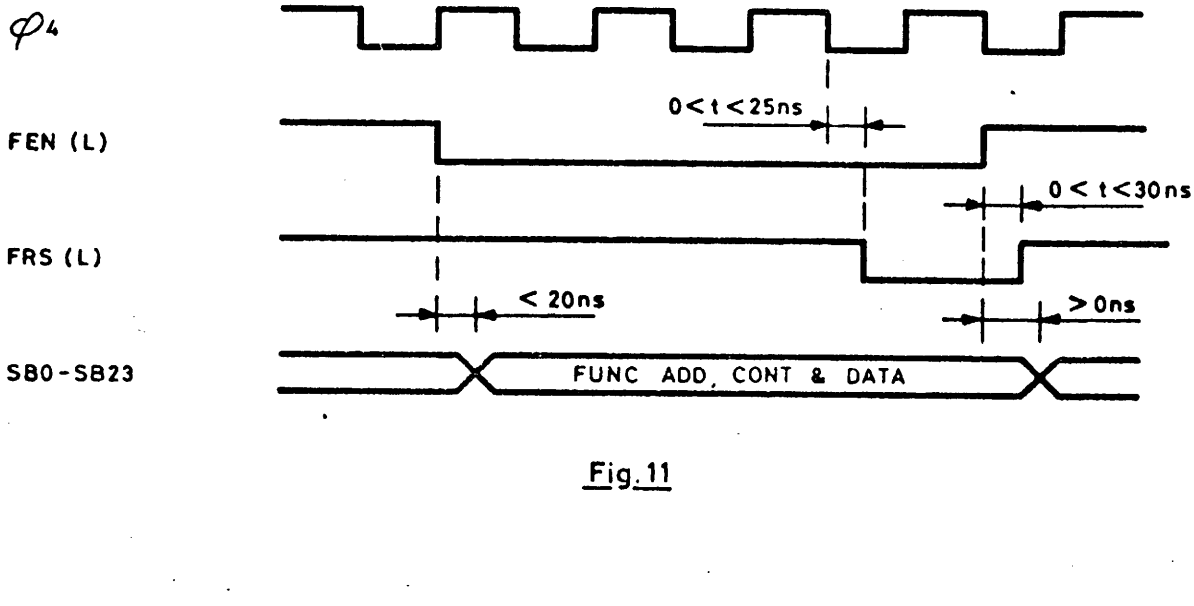
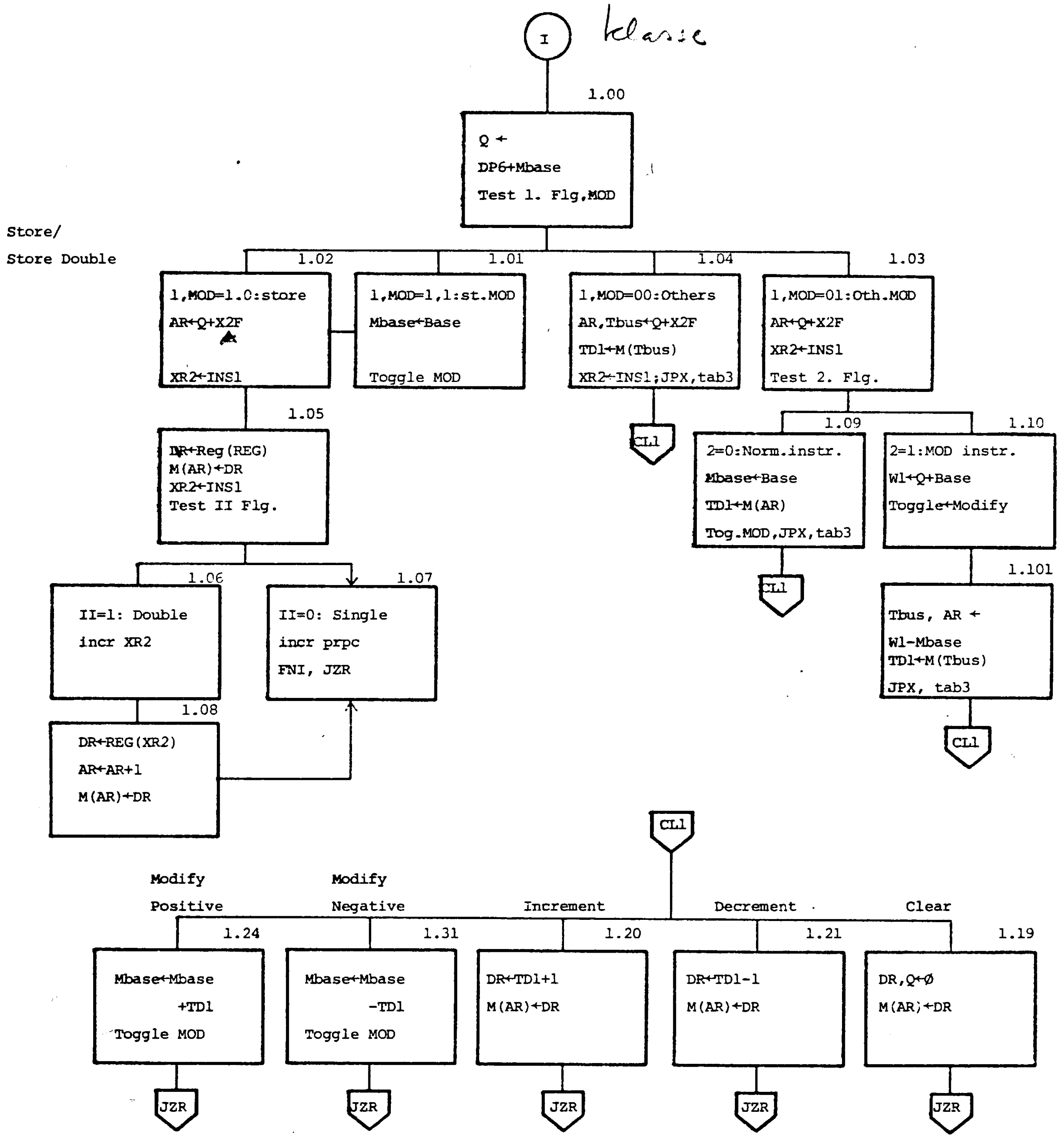


Fig. 11



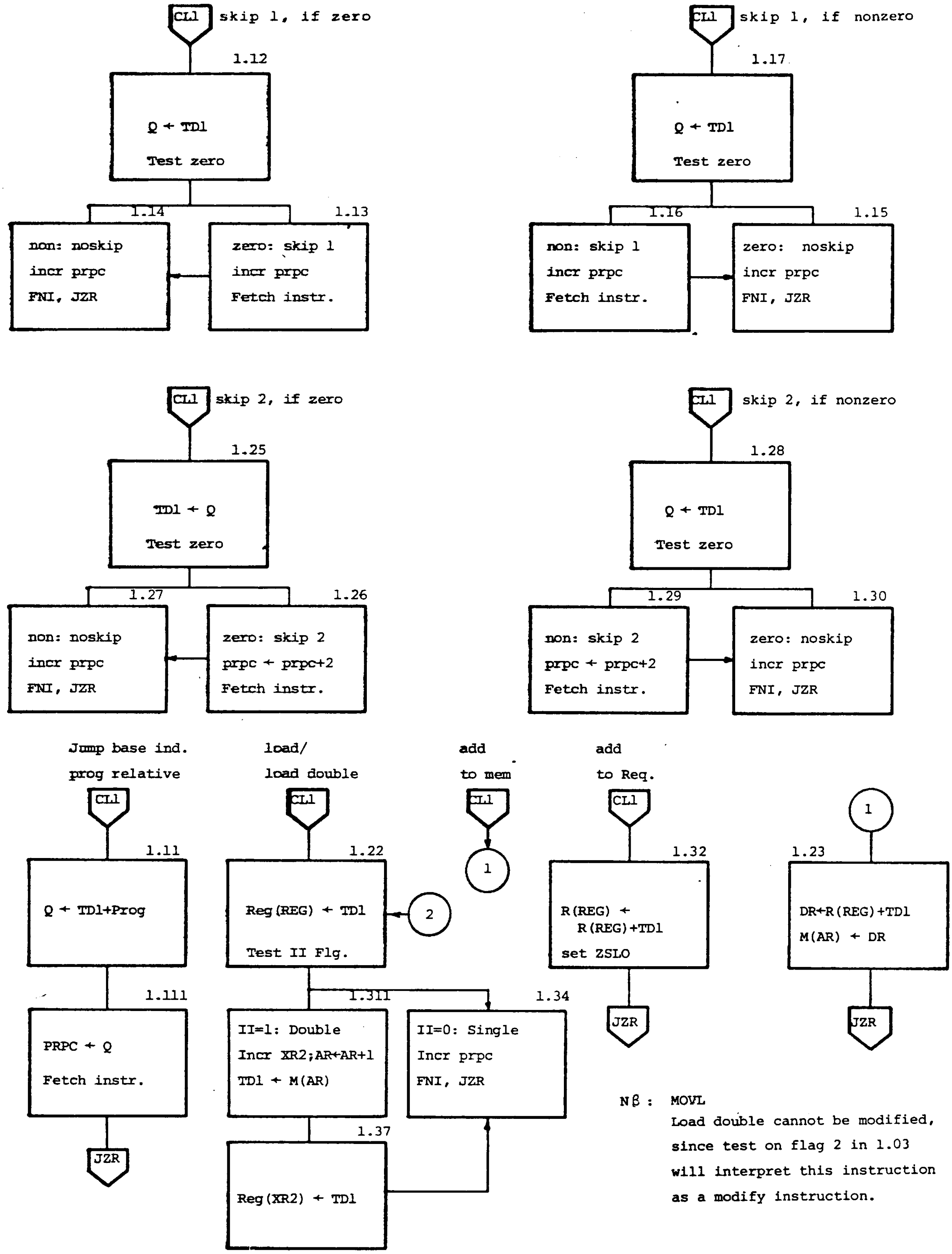
CHRISTIAN ROVSING A/S

CR8001 Instructions
X2F, DP6 Instruction;
Modify, increment; decrement;

751017		2	V6
HØH		751224	770419

3-1677

1 36

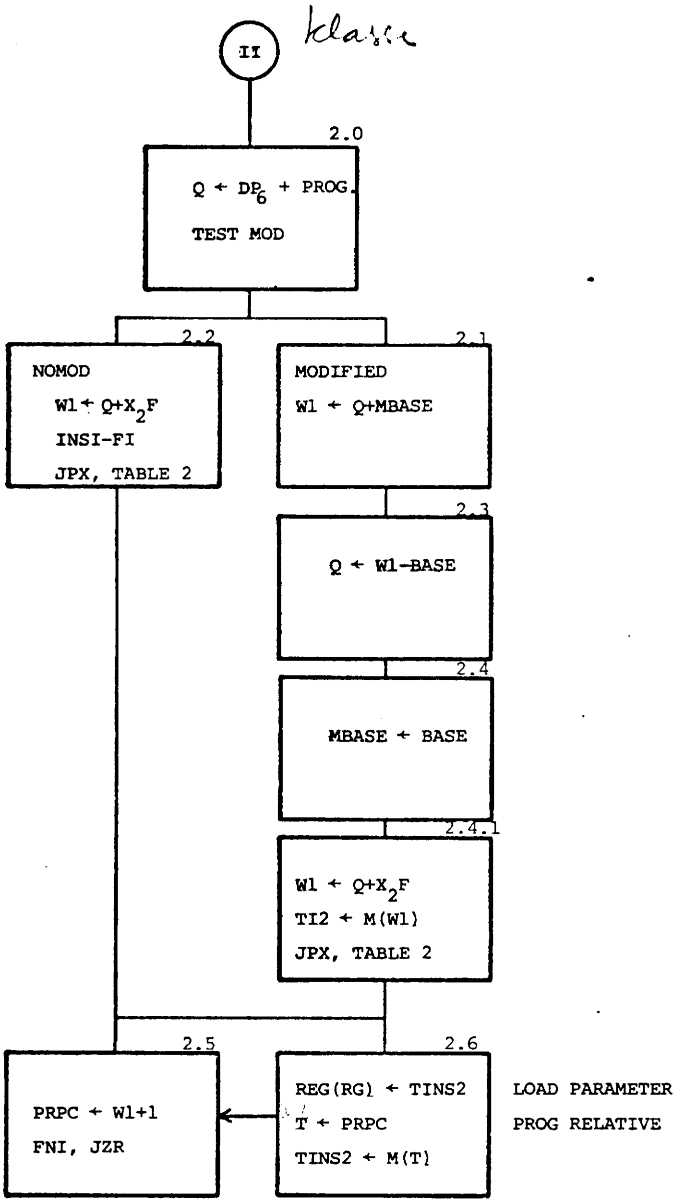


NB : MOVL
Load double cannot be modified,
since test on flag 2 in 1.03
will interpret this instruction
as a modify instruction.

CHRISTIAN ROVSING A/S

CR8001 Instructions
skip, jump base ind. prog rel,
load, load double, add

Date	751017		Issue	V6	V9
Drawn	HØH		Date	770429	770622
Parts no		3-1677	Approved	JHØ	JHØ
		Sheet 2 of 36 sheets			



CHRISTIAN ROVSING A/S

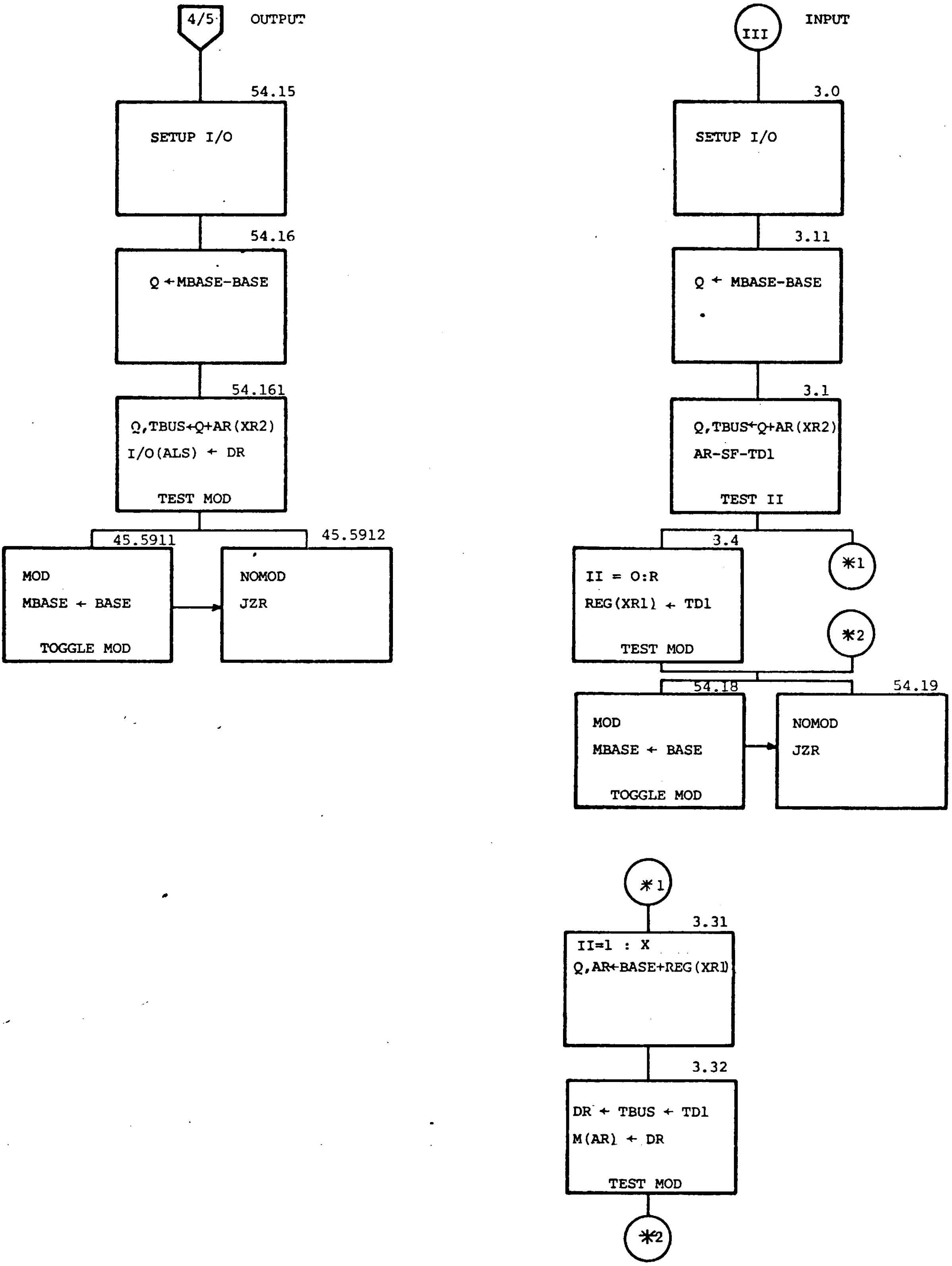
CR8001 INSTRUCTIONS
LOAD PARM., JUMP PROG RELATIVE

Scale	
Date	24.nov.'75
Drawn	HØH
Parts no	
Print no	

3-1677

Sheet 3 of 36 sheets

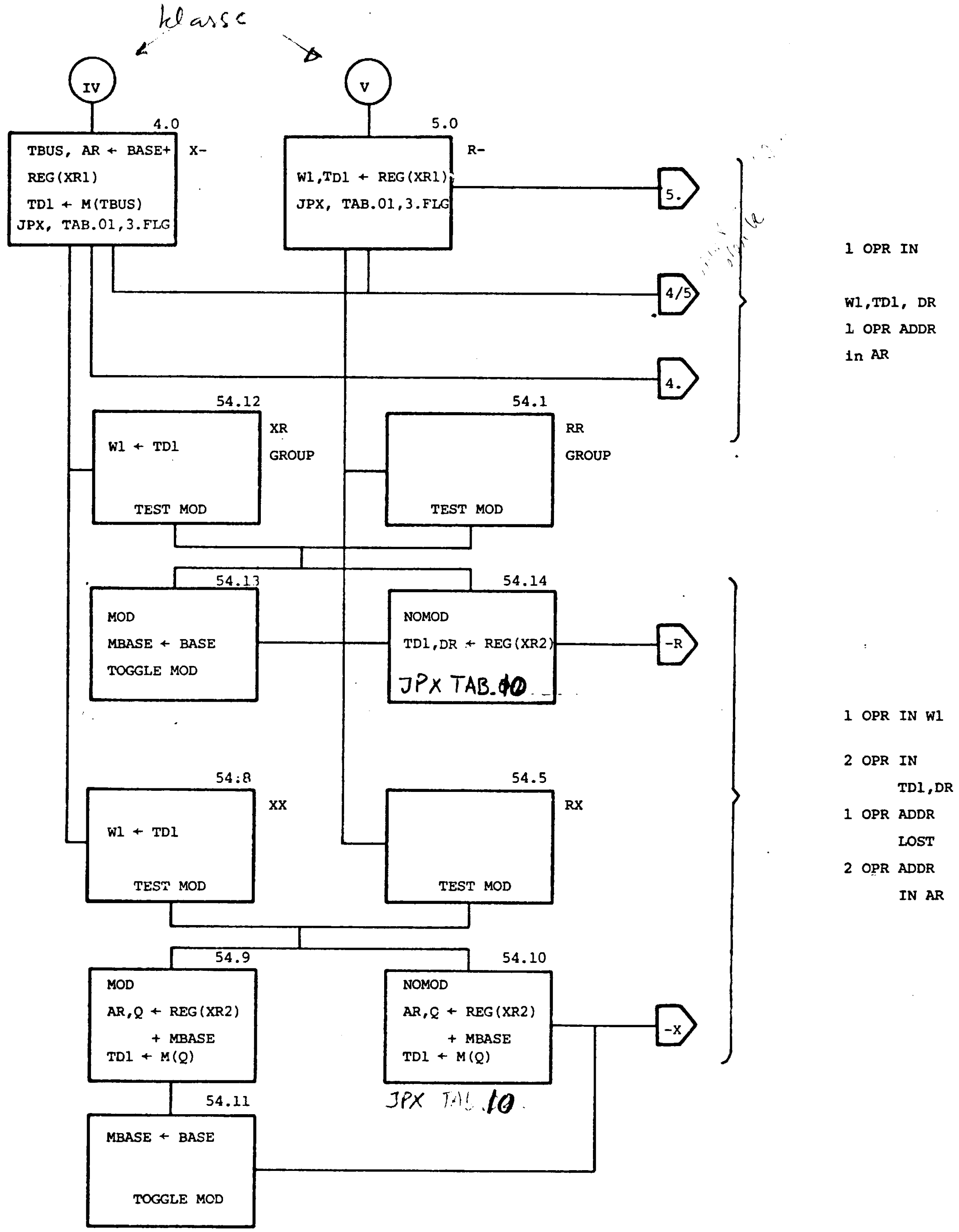
Klasse



CHRISTIAN ROVSING A/S

CR8001 INSTRUCTIONS
I/O : INPUT / OUTPUT

Date	16.oct '75	Approved	Issue
Drawn	HØH		Date
Parts no		3-1677	Approved
		Sheet 4 of 36 sheets	



CHRISTIAN ROVSING A/S

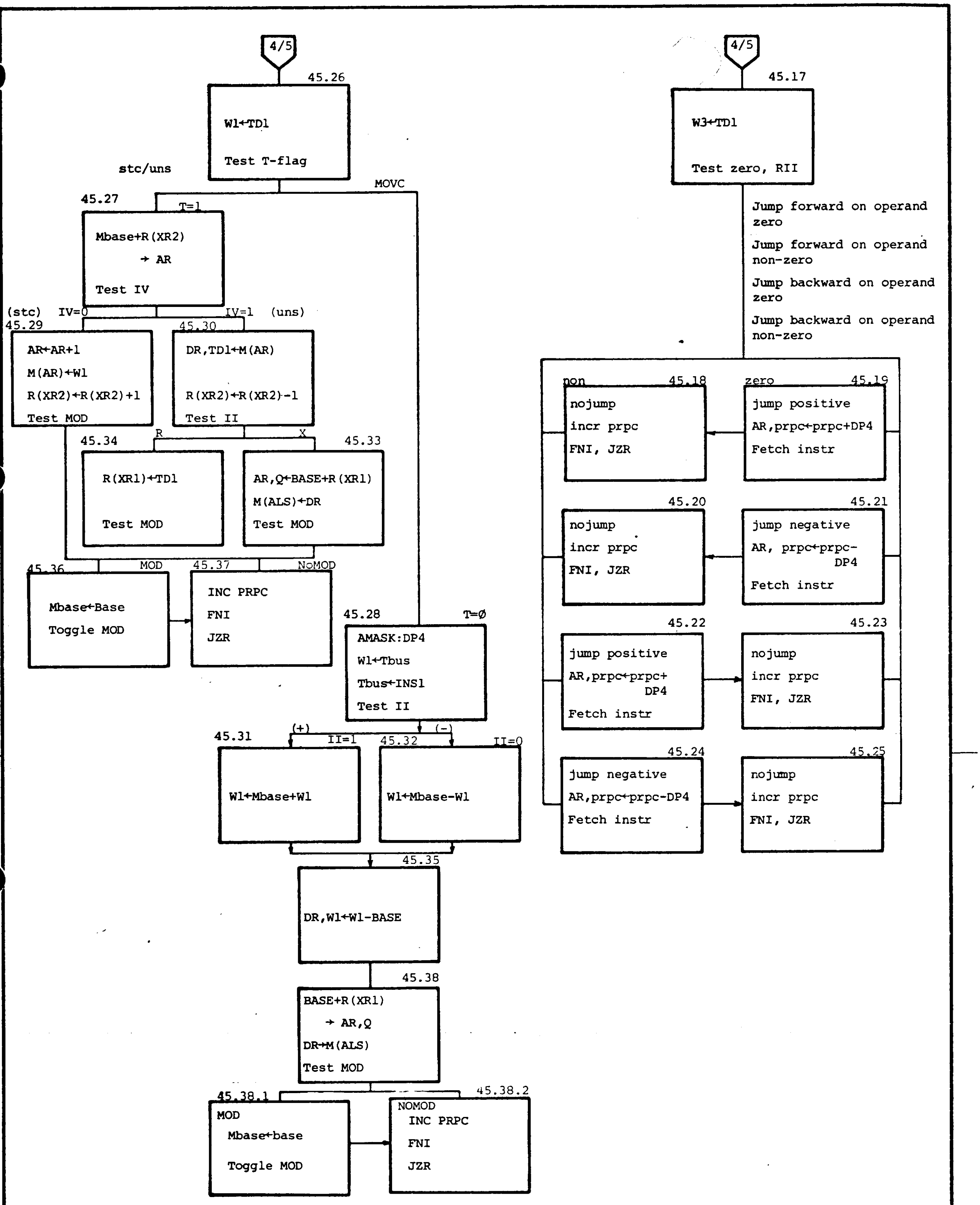
CR8001 INSTRUCTIONS

X, R, XX, XR, RX, RR INTRODUCTIONS

Date	16.oct '75
	HØH

3-1677

5 36

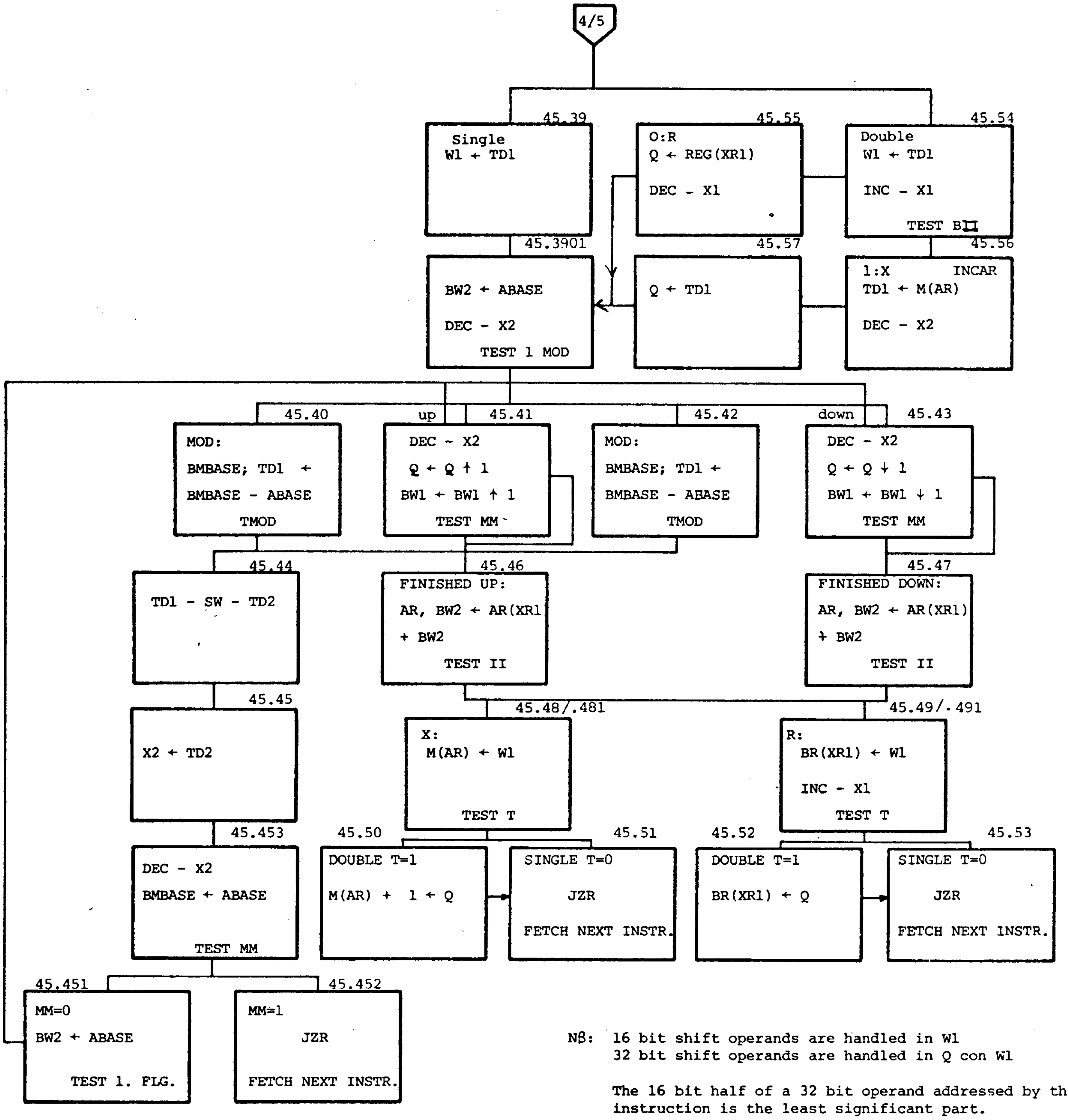


CHRISTIAN ROVSING A/S

CR8001 Instructions

Stack; Unstack; Move Const; Jump on Operand.

Date	751016	Issue	2	V6	
Drawn	HØH	Date	751124	770429	
Parts no		Approved			
Print no		3-1677			
		Sheet 6 of 36 sheets			



NB: 16 bit shift operands are handled in W1
32 bit shift operands are handled in Q con W1

The 16 bit half of a 32 bit operand addressed by the instruction is the least significant part.
The most significant half is fetched from the higher neighbor address to the least sign. part.

CHRISTIAN ROVSING A/S

CR8001

INSTRUCTIONS : SHIFT SINGLE/DOUBLE

Scale

Date

Drawn

Parts no

Approved

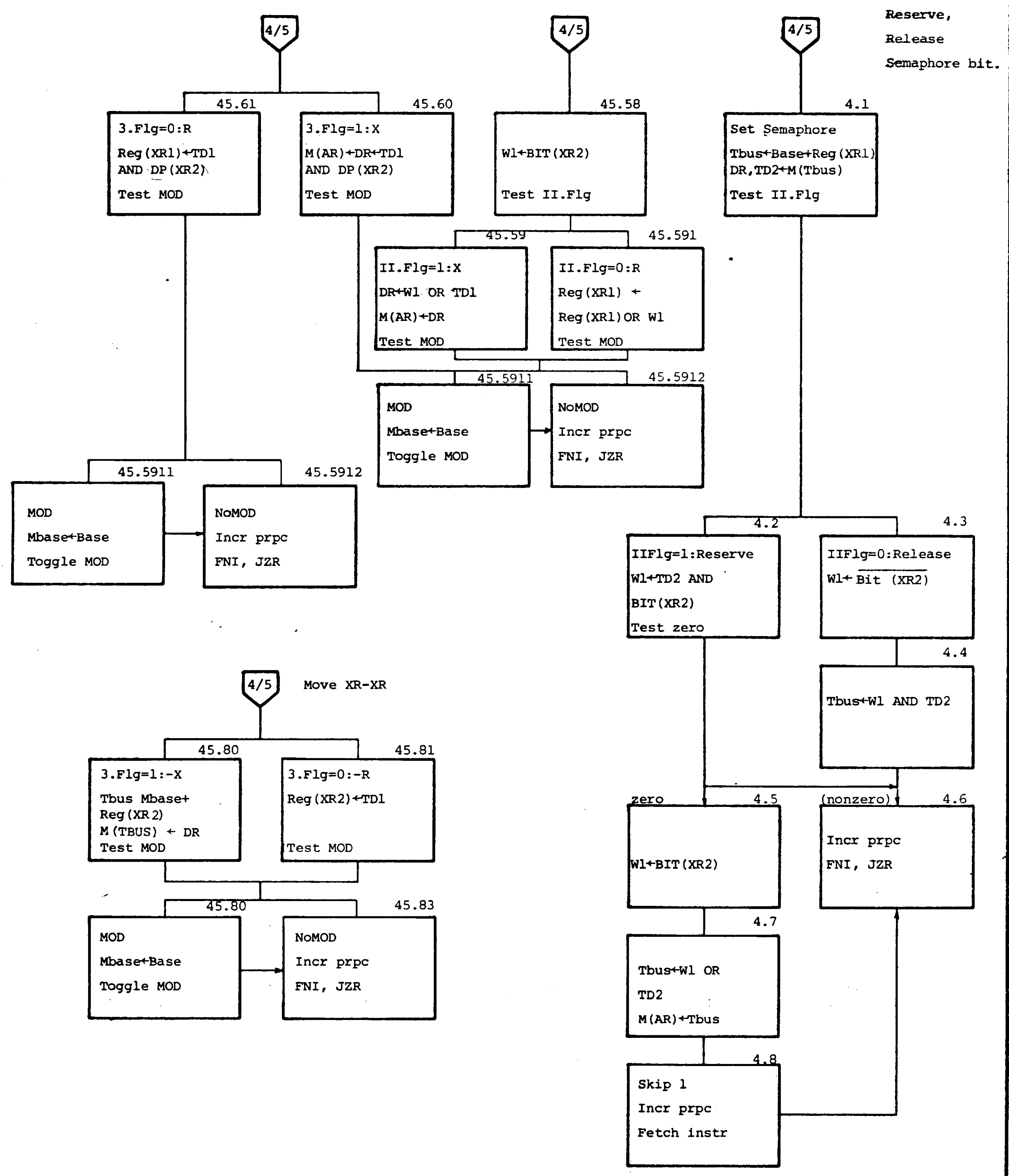
Issue

Date

Approved

3-1677

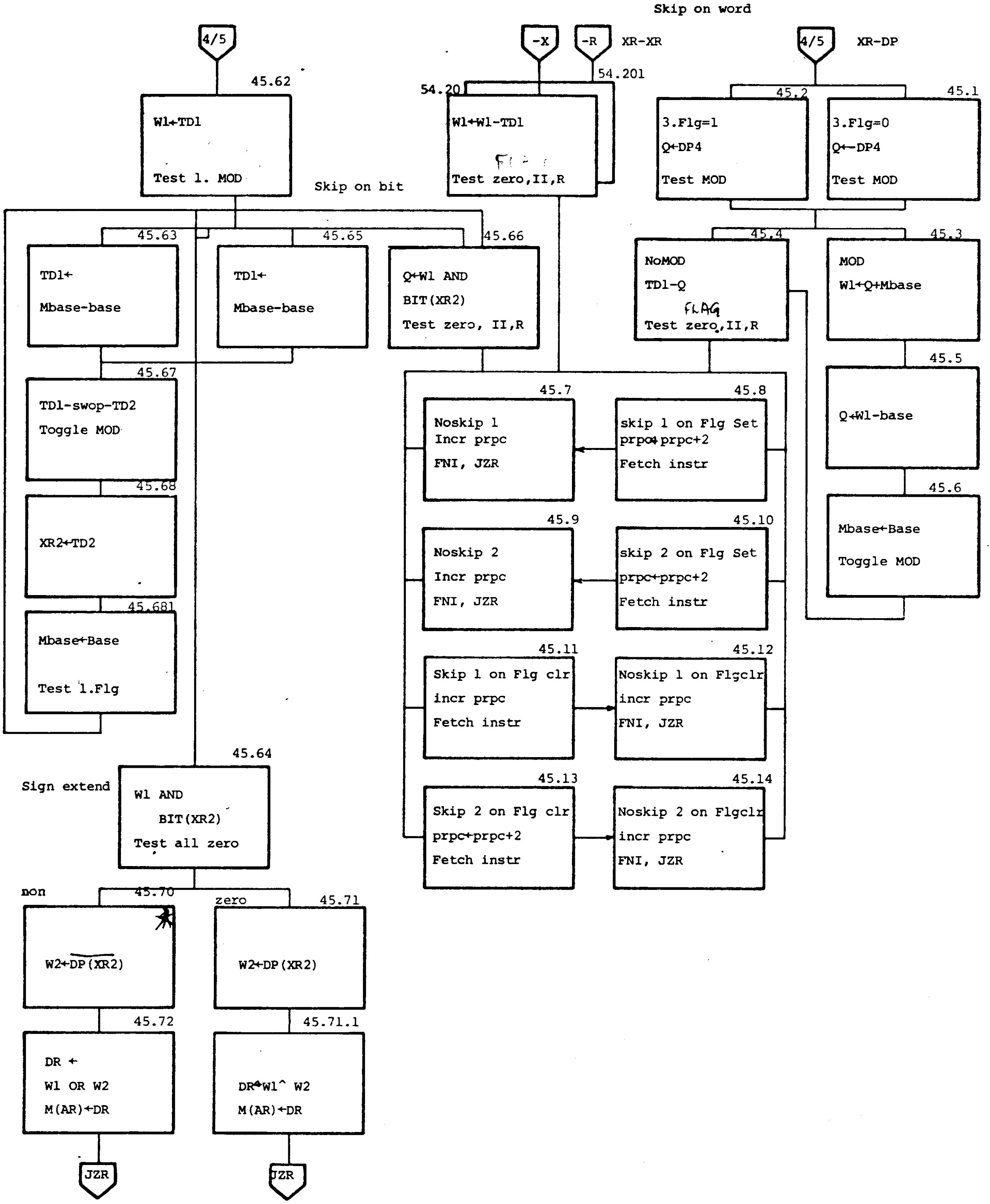
Sheet 7 of 36 sheets



CHRISTIAN ROVSING A/S

CR8001 Instructions
Extract, Setbit, Reserve-Release Sem.
Move XR-XR

Stamp		Approved		Stage	
Date	751016			Date	
Drawn	HØH			Approved	
Parts no		3-1677			
Print no		Sheet 8 of 36 sheets			

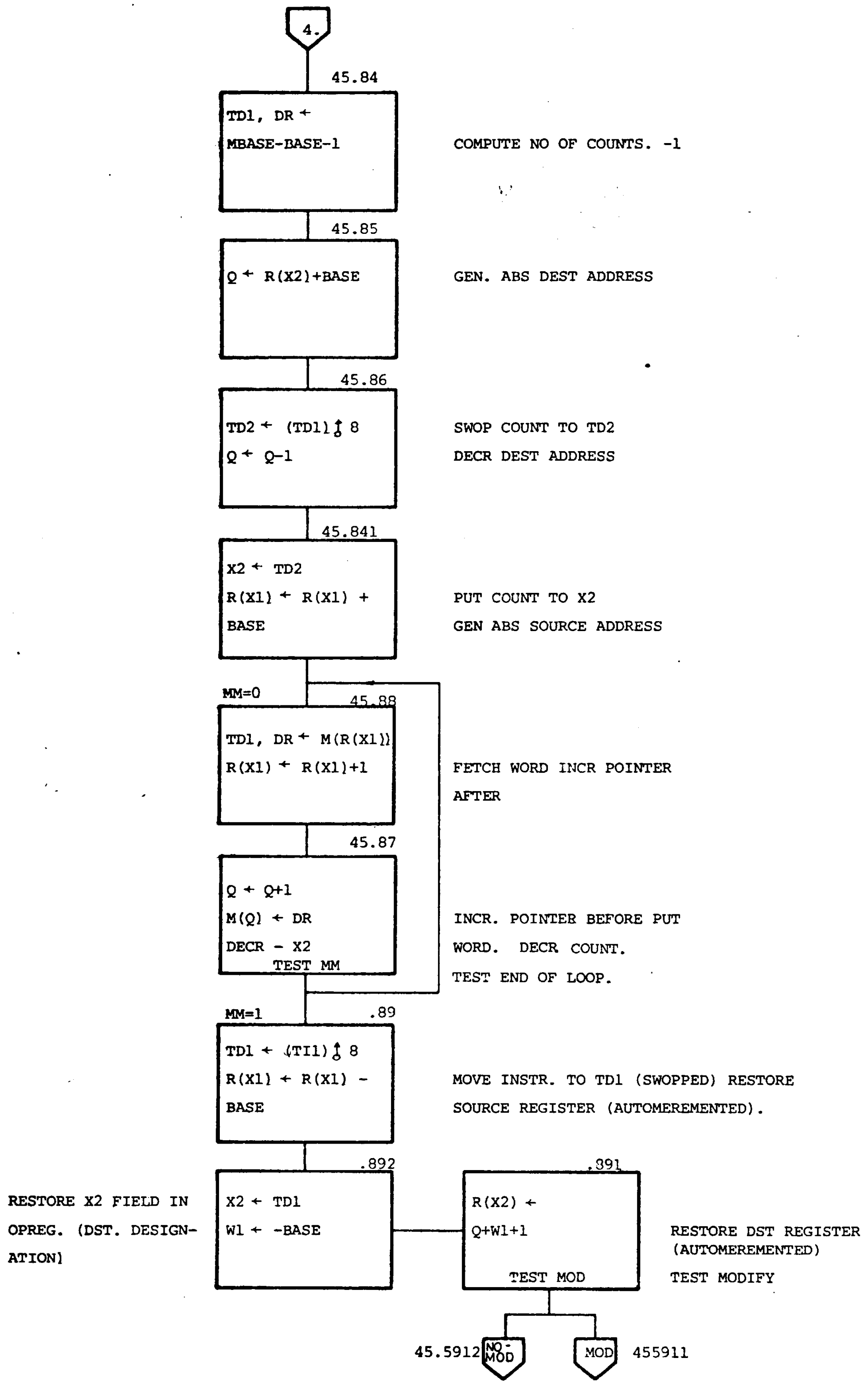


CHRISTIAN ROVSING A/S

CR8001 Instructions

Skip on bit & word; sign extend

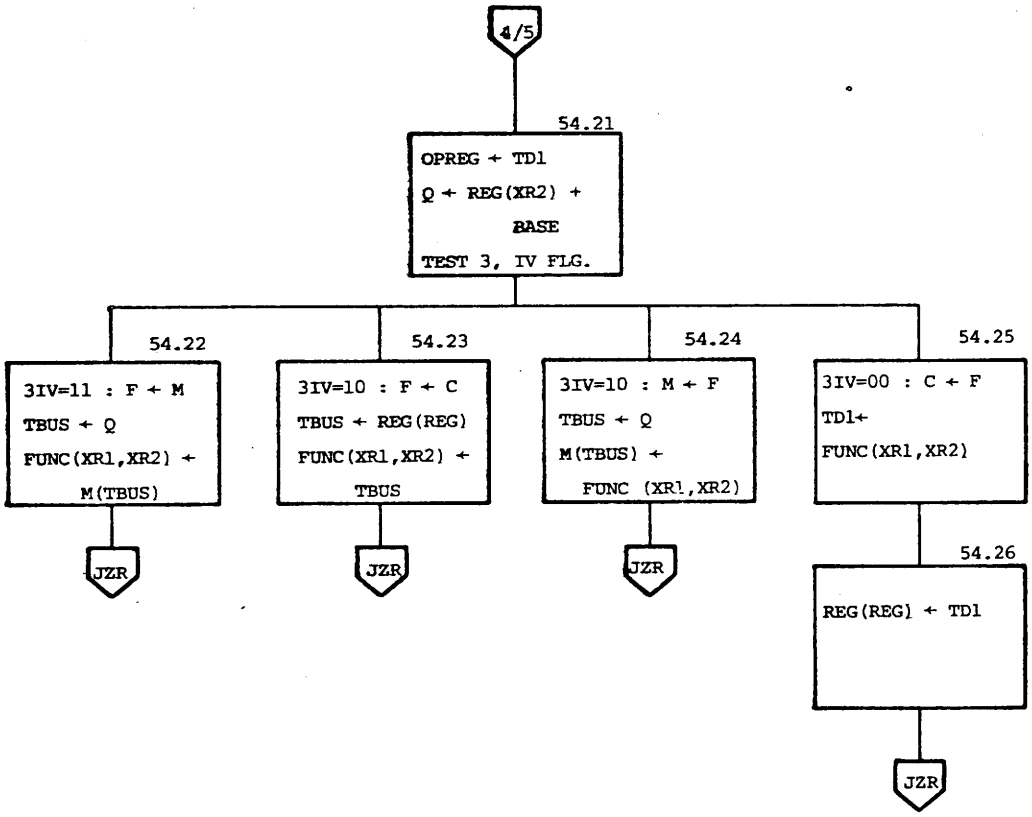
Date	751016			Date	770429
Drawn	HØH			Approved	JHØ
Parts no		3-1677			V6
		Sheet 9 of 36 sheets			



CHRISTIAN ROVSING A/S

CR8001 INSTRUCTIONS
MOVE MULTIPLE WITH AUTOINCR.

Scale		Approved	Issue
Date	2.dec '75		Date
Drawn	HØH		Approved
Parts no		3-1677	
Print no		Sheet 10 of 36 sheets	

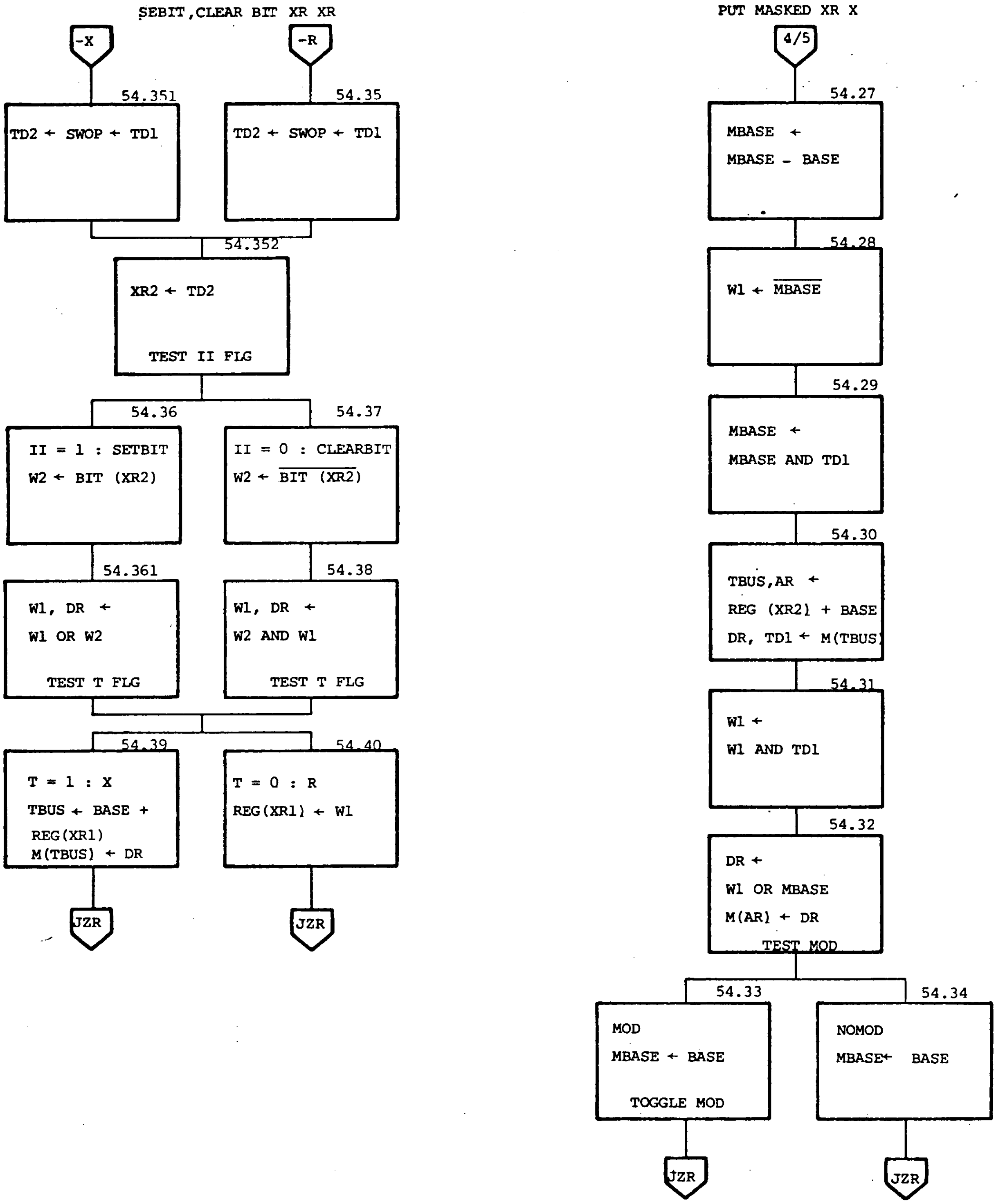


CHRISTIAN ROVSING A/S

CR8001 INSTRUCTIONS
FUNCTION MODULE INSTR.

Scale		Approved	
Date	17 oct '75		
Drawn	HØH		
Parts no		3-1677	
Print no		Sheet 11 of 36 sheets	

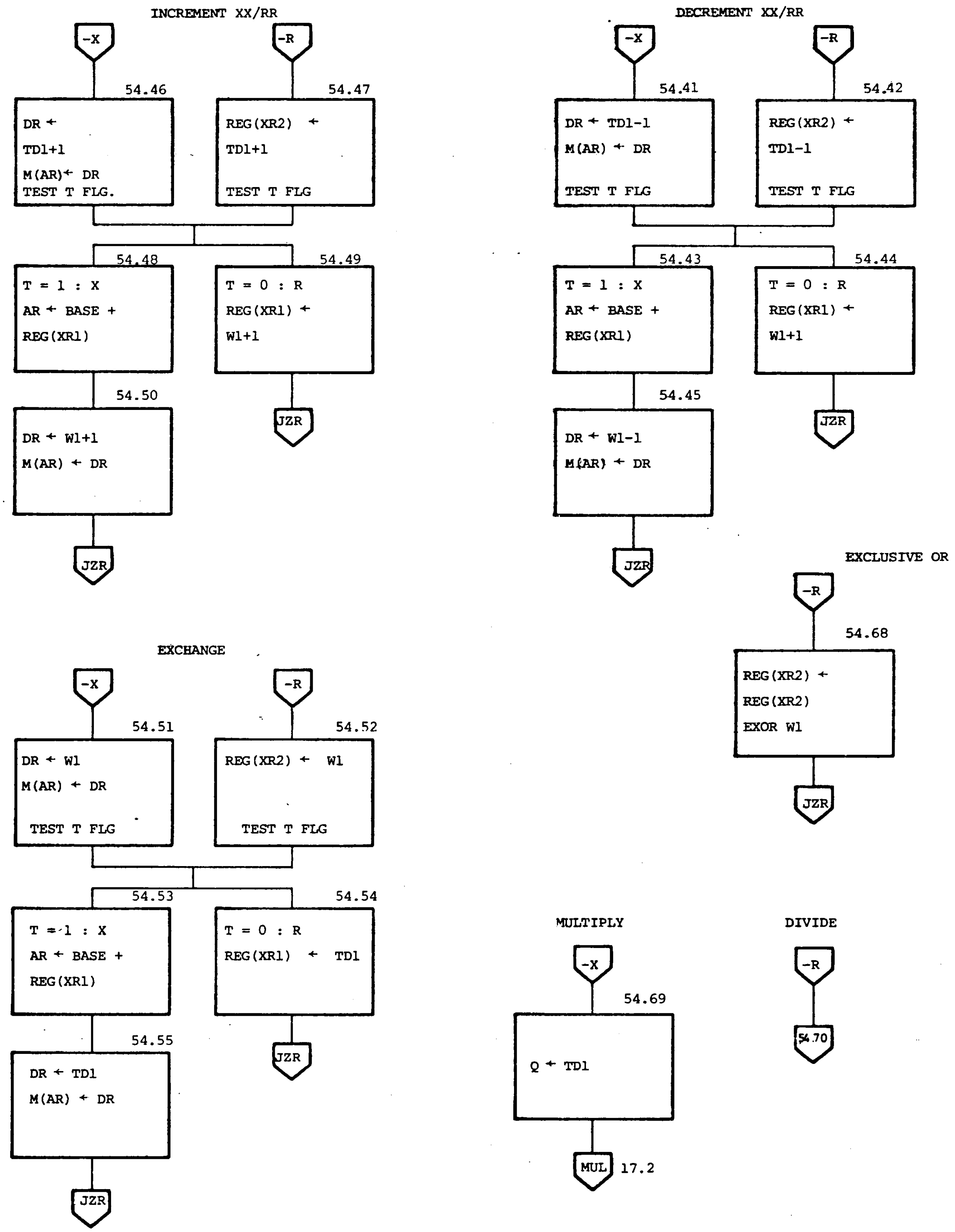
Issue
Date
Approved



CHRISTIAN ROVSING A/S

CR8001 INSTRUCTIONS
SETBIT, CLEARBIT XRXR
PUT MASKED XR X.

Scale		Approved	Issue
Date	17.oct '75		Date
Drawn	HØH		Approved
Parts no		3-1677	
Print no		Sheet 12 of 36 sheets	



CHRISTIAN ROVSING A/S

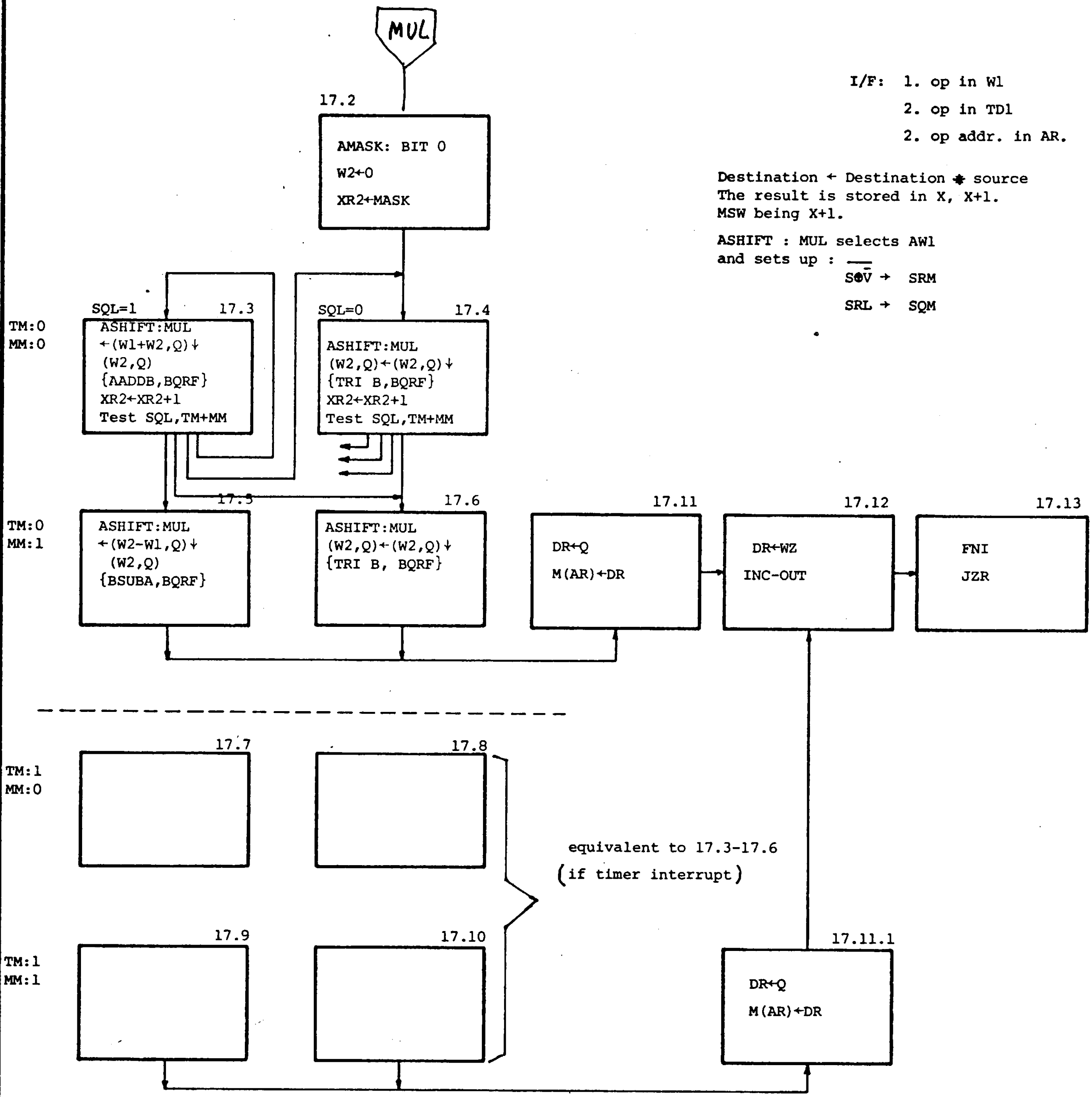
CR8001 INSTRUCTIONS

1 NCR. 2 OPR. DECR. 2 OPR., EXCH. 2 OPR

EXOR; MULTIPLY; DIVIDE.

Scale		Approved	Issue	V6
Date	17.oct '75		Date	770429
Drawn	HØH		Approved	JHØ
Parts no		3-1677		
Print no		Sheet 13 of 36 sheets		

MUL XR, X



I/F: 1. op in W1
2. op in TD1
2. op addr. in AR.

Destination ← Destination ✱ source
The result is stored in X, X+1.
MSW being X+1.

ASHIFT : MUL selects AW1
and sets up : $S \oplus \overline{V}$ → SRM
SRL → SQM

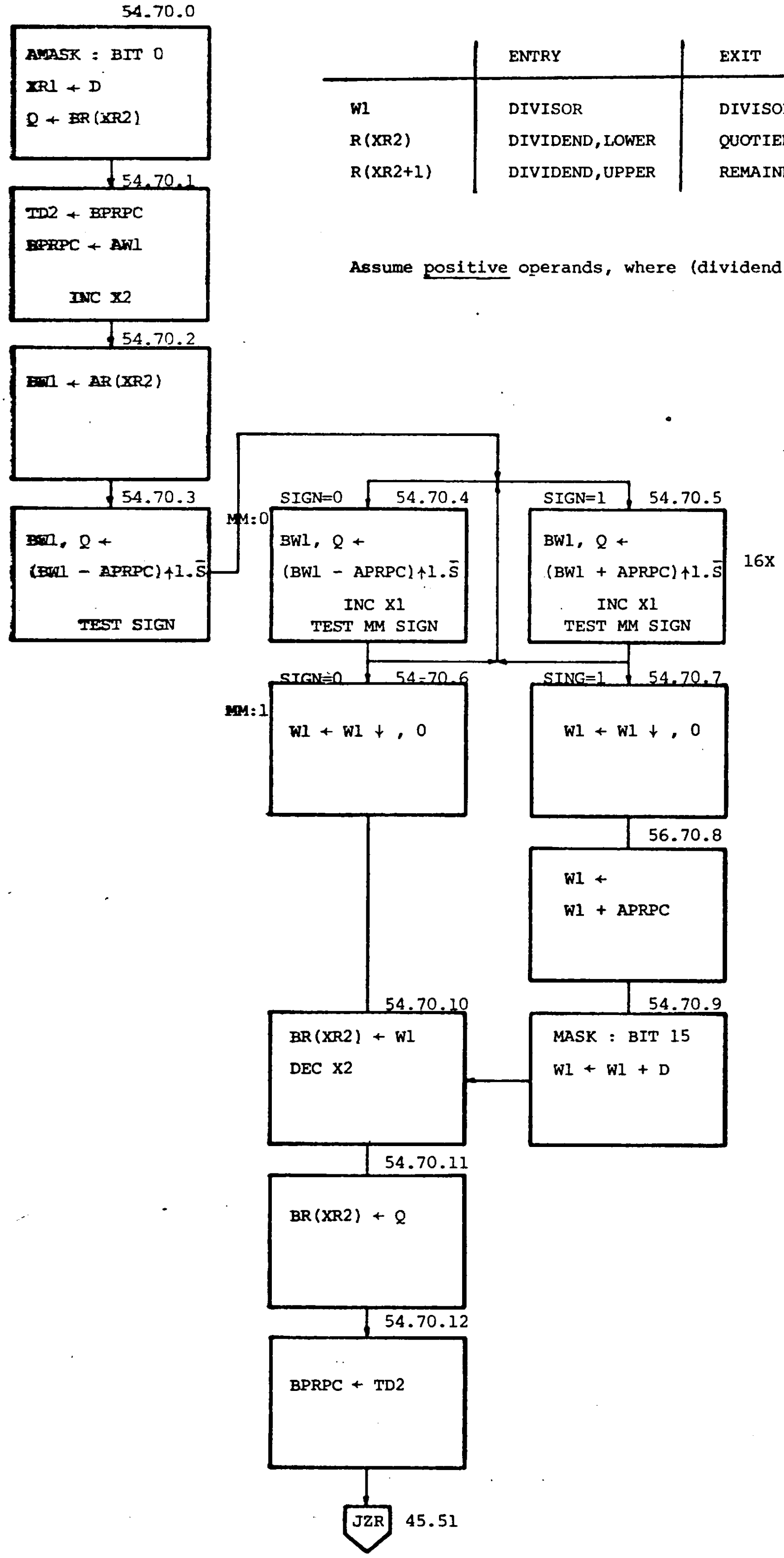
CHRISTIAN ROVSING A/S

CR8001 MP
MULTIPLY

Scale		Approved	Issue
Date	750819		Date
Drawn	JHØ		Approved
Parts no		3-1677	
Print no		Sheet 14 of 26 sheets	

	ENTRY	EXIT
W1	DIVISOR	DIVISOR
R(XR2)	DIVIDEND,LOWER	QUOTIENT
R(XR2+1)	DIVIDEND,UPPER	REMAINDER

Assume positive operands, where (dividend, upper) < divisor $+2^{16}$

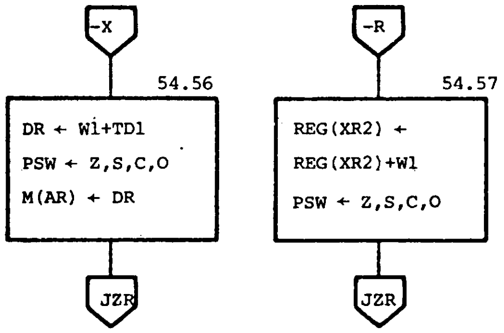


CHRISTIAN ROVSING A/S

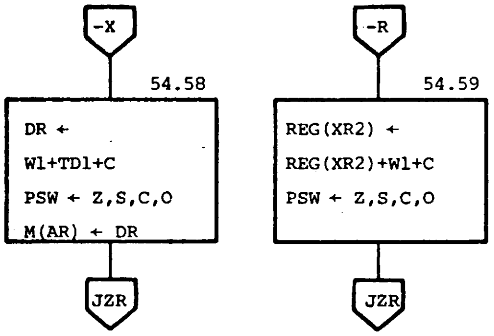
CR8001
DIVIDE

Scale		Issue	V6
Date	Approved	Date	770429
Drawn		Approved	JHØ
Parts no	3-1677		
Print no	Sheet 15 of 36 sheets		

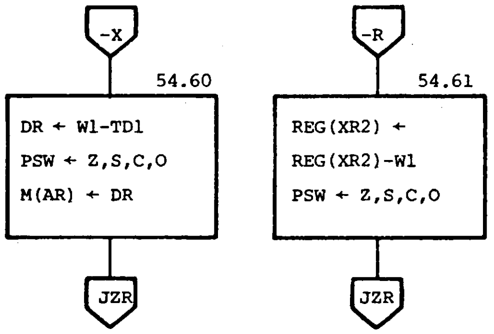
ADD XR XR



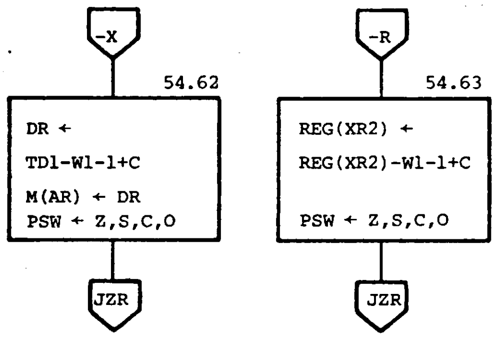
ADD WITH CARRY XR XR



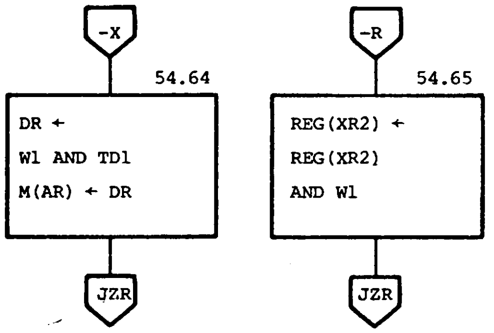
SUB XR XR



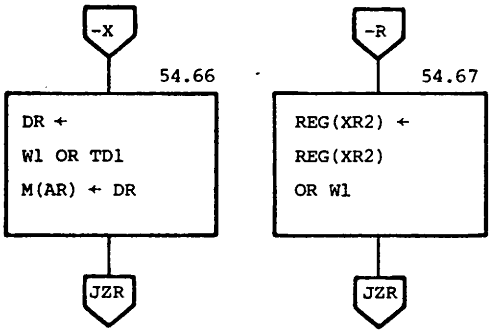
SUB WITH BORROW XR XR



AND XR XR



OR XR XR



CHRISTIAN ROVSING A/S

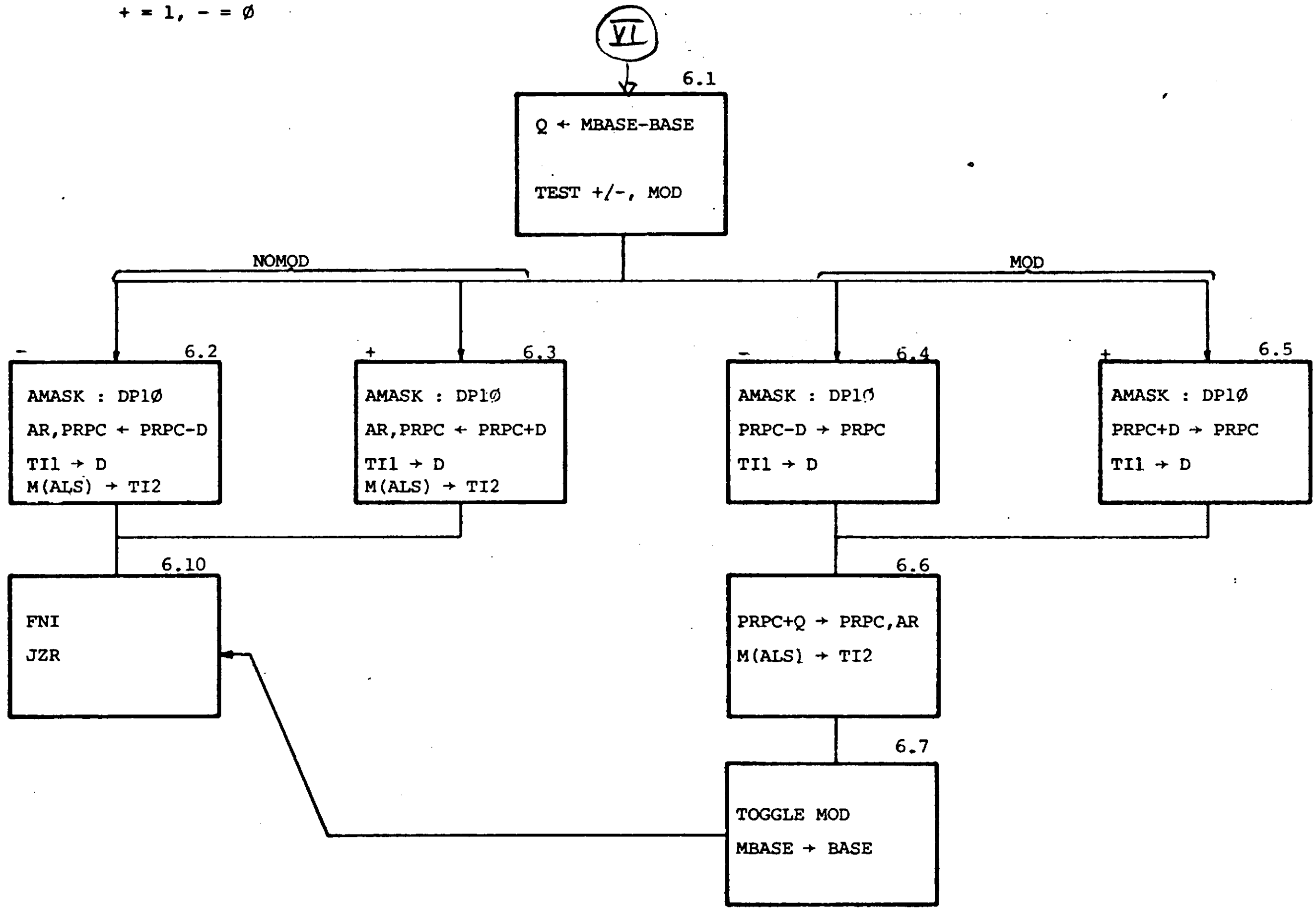
CR8001 INSTRUCTIONS
ADD, ADD WITH CARRY, SUB, SUB WITH
BORROW, AND, OR.

Scale		Approved	Issue
Date	17.oct '75		Date
Drawn	HØH		Approved
Parts no		3-1677	
		Sheet 16 of 36 sheets	

±	1	Ø	1	1	Ø	DP 1Ø

JMP M ± L1Ø

+ = 1, − = Ø



CHRISTIAN ROVSING A/S

CR8001, MP
CLASS VI

Scale		Approved		Issue	1
Date	770620			Date	770620
Drawn	JHØ			Approved	JHØ
Parts no		3-1677			
Printed		Sheet 17 of 36 sheets			

$^1/a$ +/-

$^1/a$ 1 0 0 1	R	DP8
$^1/a$ 0 1 0 1	R	DP8

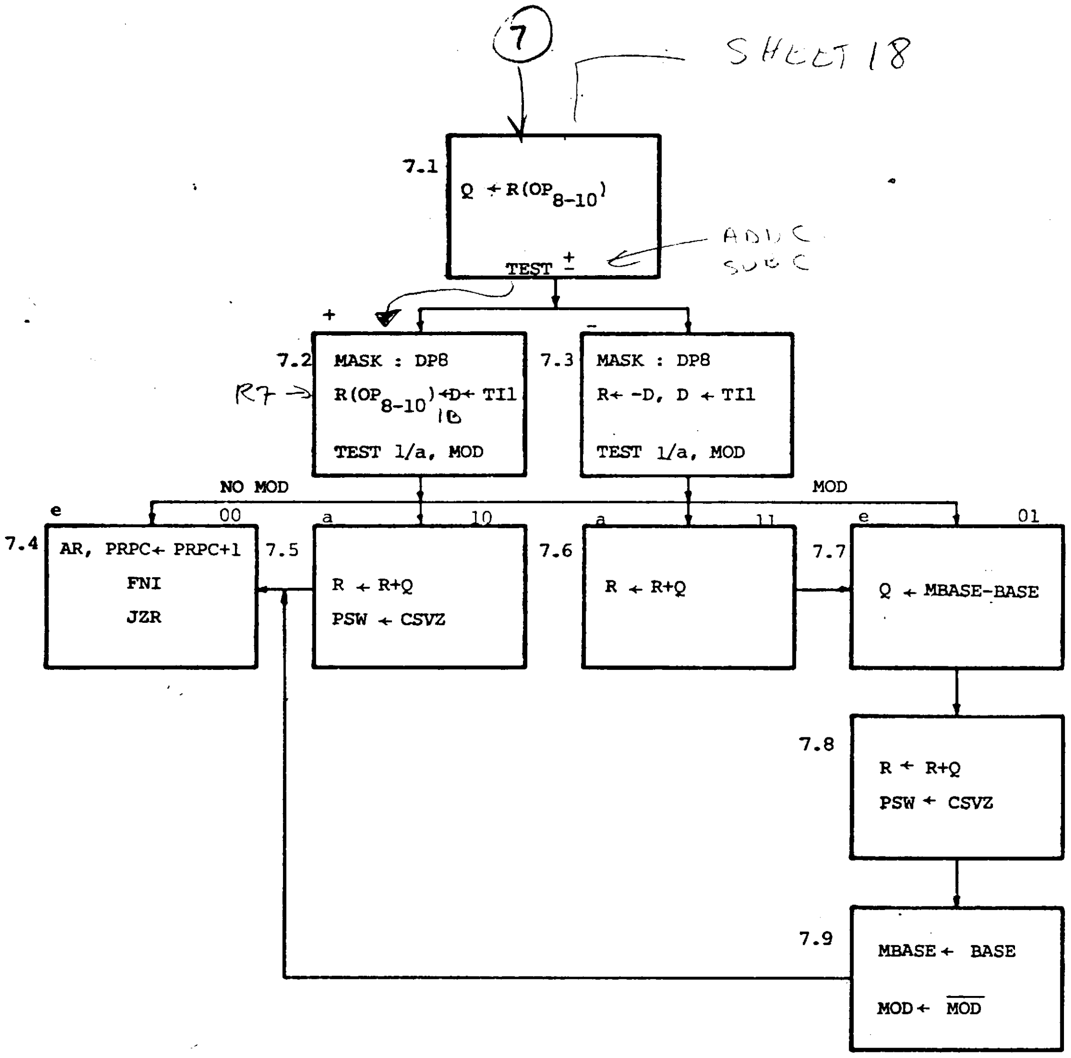
1 : 0, a : 1, + : 1, − : 0.

LOAD/ADD IMMEDIATE

1: $R_{0-7} \leftarrow$ DP8 + MODIFY

a: $R_{0-7} \leftarrow R_{0-7} \pm$ DP8 + MODIFY

klasse



CHRISTIAN ROVSING A/S

CR8001 MP
CLASS VII

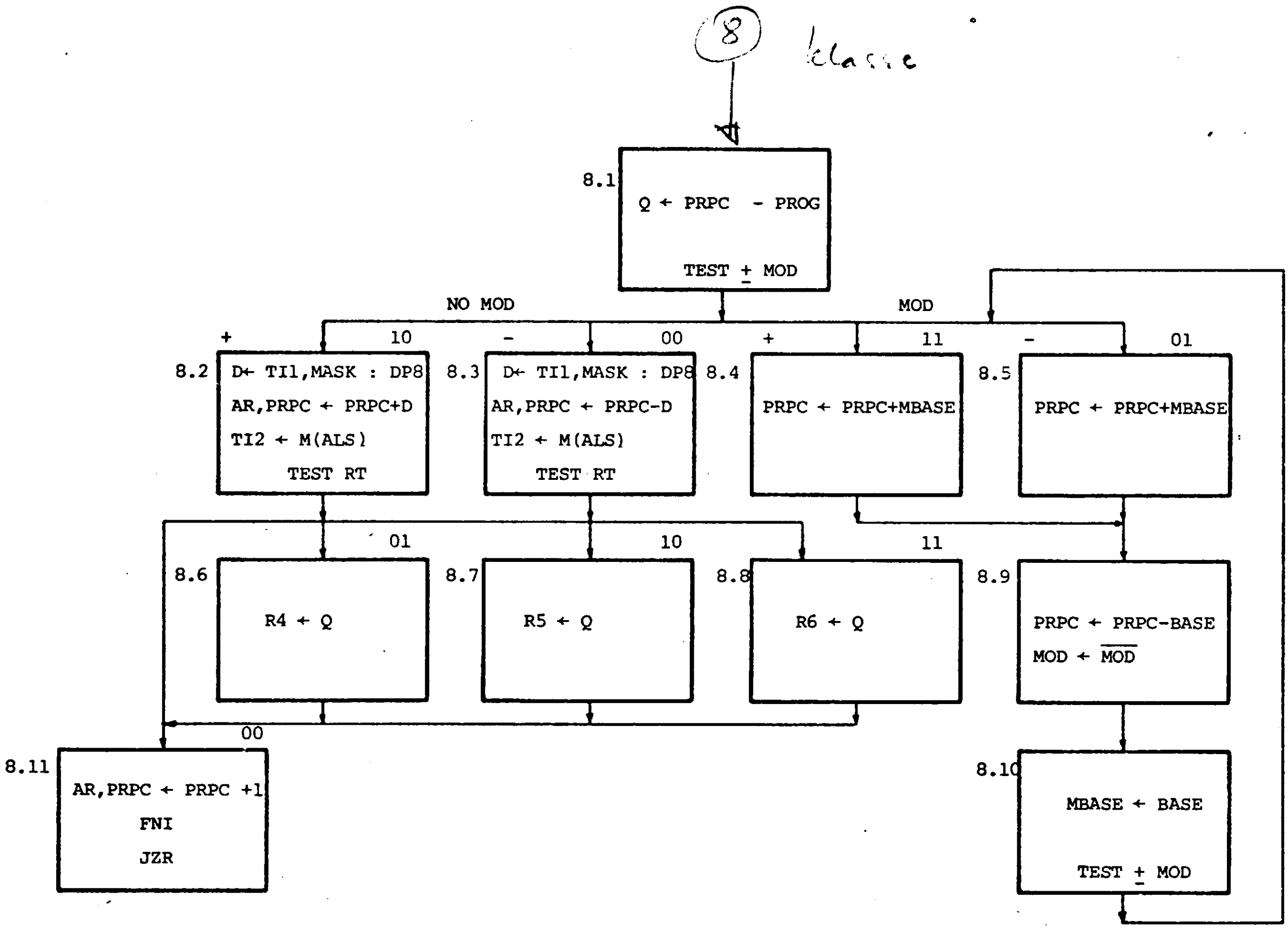
Scale		Approved	Issue
Date	750820		Date
Drawn	JHØ		Approved
Parts no		3-1677	
Print no		Sheet 18 of 36 sheets	

± 1 0 1 1 1	RT	DP8

JUMP RELATIVE

RT_{4-6} ← LOC+1-PROG; RT = 00: NO RETURN REG.

LOC ← LOC+1 ± DP8 + MODIFY



CHRISTIAN ROVSING A/S

CR8001 MP
CLASS VIII

Scale		Approved	Issue
Date	750820		Date
Drawn	JHØ		Approved
Parts no		3-1677	
Print no		Sheet 19 of 36 sheets	

1/j

1 1 1 1 1 1	RT	DP8

JUMP INDIRECT

RT_{4-6} ← LOC+1-PROG ; RT = 00: NO RETURN REGISTER

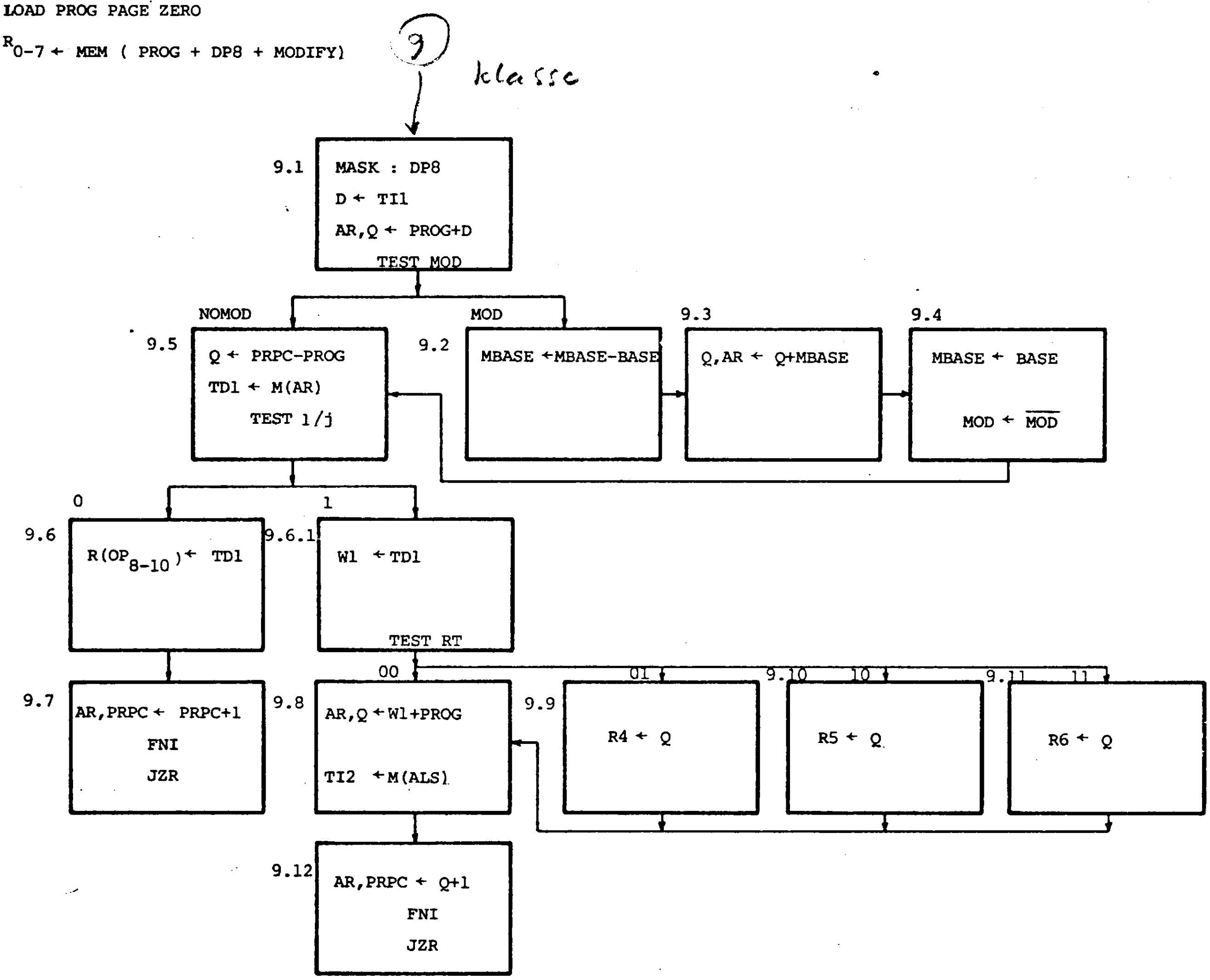
LOC ← PROG+MEM (PROG + DP8 + MODIFY)

1/j

1 0 0 1 1	R	DP8

LOAD PROG PAGE ZERO

R_{0-7} ← MEM (PROG + DP8 + MODIFY)



CHRISTIAN ROVSING A/S

CR8001 MP
CLASS IX

Scale		Approved	Issue
Date	750820		Date
Drawn	JHØ		Approved
Parts no		3-1677	
Print no		Sheet 20 of 36 sheets	

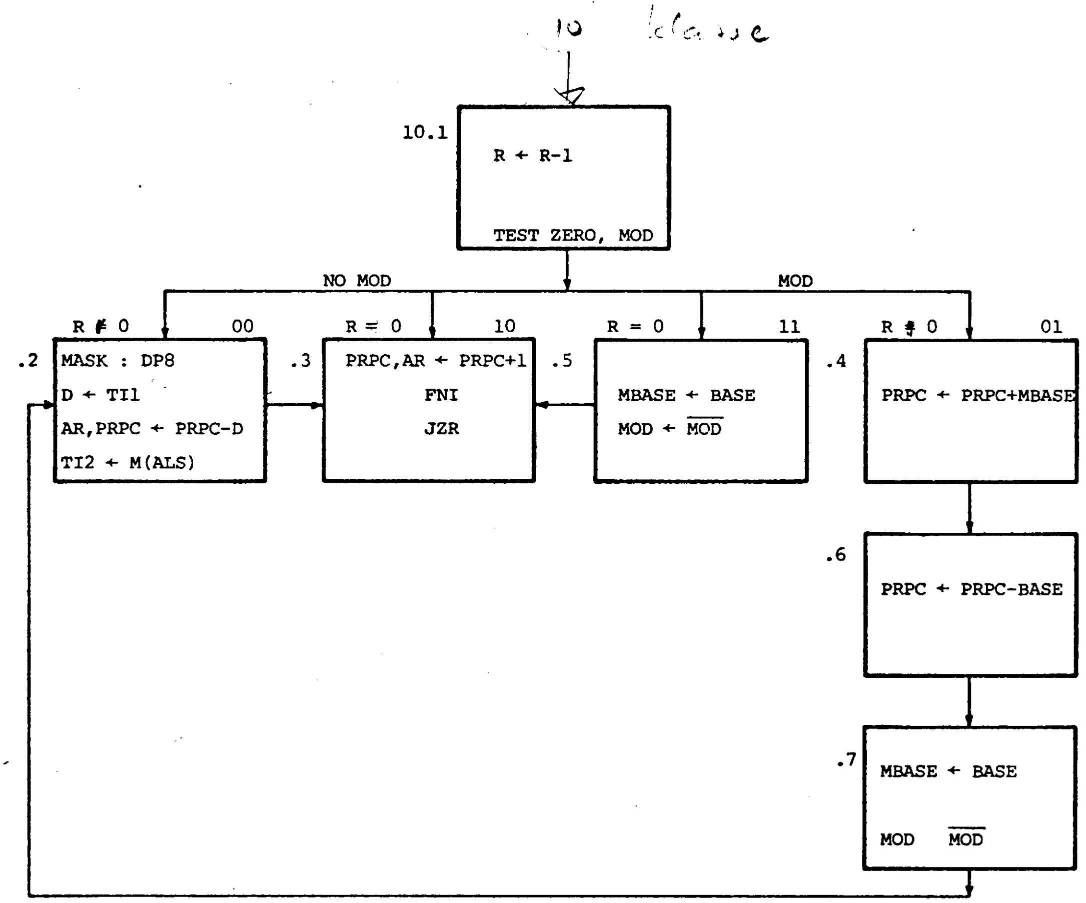
1 1000	R	DP8

SUBTRACT ONE AND BRANCH ON NON ZERO

$R_{0-7} \leftarrow R_{0-7} - 1$

IF $R_{0-7} = 0$ THEN LOC ← LOC+1

ELSE LOC ← LOC+1 - DP8+MODIFY



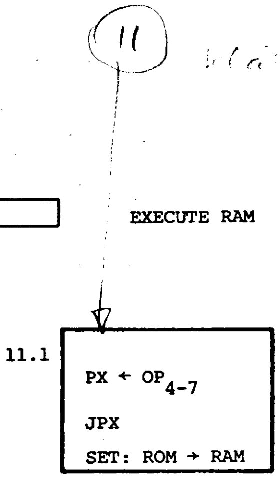
CHRISTIAN ROVSING A/S

CR8001 MP
CLASS X

Scale
Date 750820
Drawn JHØ
Parts no
Print no
Approved
3-1677
Sheet 21 of 36 sheets
Issue
Date
Approved

1110	0110	RAM	

EXECUTE RAM



```
PX ← OP4-7
JPX
SET: ROM → RAM
```

EXECUTE RAM INCLUDES JUMP TO u-LOCATION :

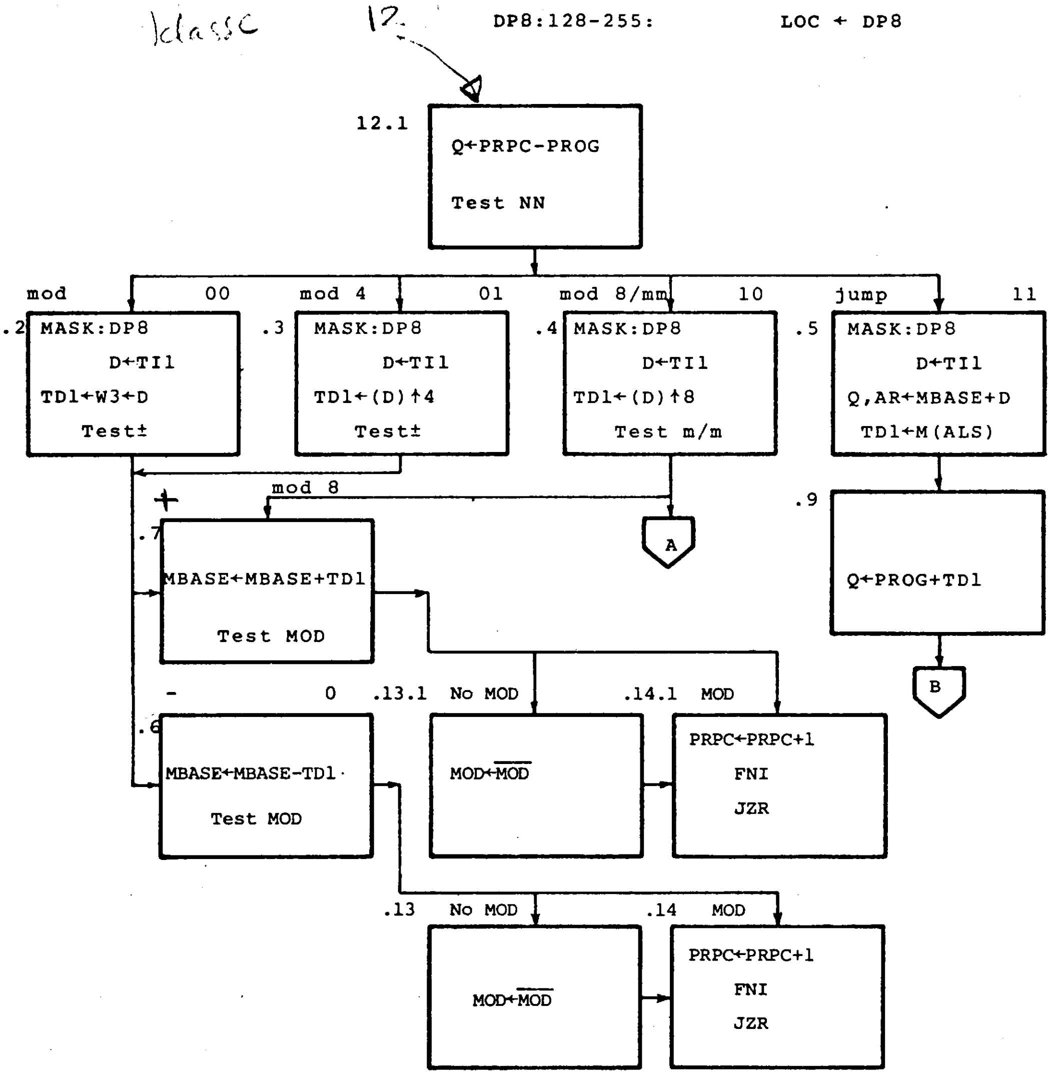
1 1	$\overline{\text{RAM}}$

Nβ: The Microram destination address is determined as the column designed by the inverted 4 bit RAM field in the EXECUTE RAM instruction; and the row always being # 3.

MODC

	NN			
1 ∓ 1 0 0 1	00	DP8	Modify:	MODIFY ← MODIFY ±DP8
1 ± 1 0 0 1	01	DP8	Modify shifted 4:	MODIFY ← MODIFY ±(DP8) ↑4
m/m				
0 1 0 1 0 1	10	DP8	Modify shifted 8:	MODIFY ← MODIFY +(DP8) ↑8
1 1 1 0 0 0	11	DP8	Jump Base Indirect:	LOC← PROG+MEM(BASE+MODIFY+DP8)
m/m				
1 0 1 0 0 1	10	DP8	Monitor Call:	R7← LOC+1-PROG
			DP8:0-63:	LOC ← 63
			DP8:64-127:	LOC ← MEM(DP8)
			DP8:128-255:	LOC ← DP8

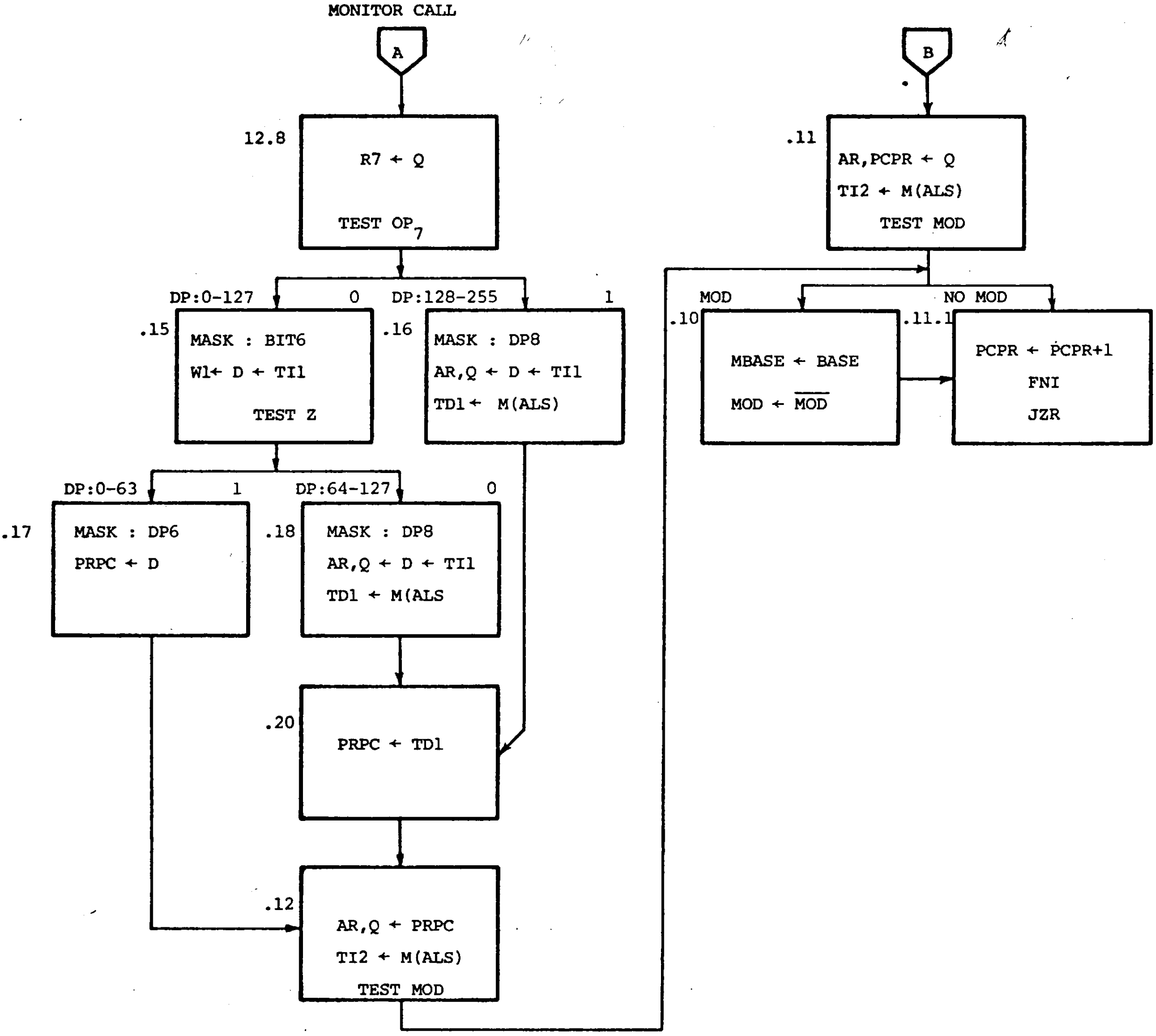
klassC



CHRISTIAN ROVSING A/S

CR8001 MP
CLASS XII

Scale		Approved		Issue	
Date	750820			Date	
Drawn	JHØ			Approved	
Parts no					
Print no		Sheet 23 of 36 sheets			



CHRISTIAN ROVSING A/S

CR8001 MP
CLASS XII

Scale	
Date	750820
Drawn	JHØ
Parts no	
Print no	

Approved

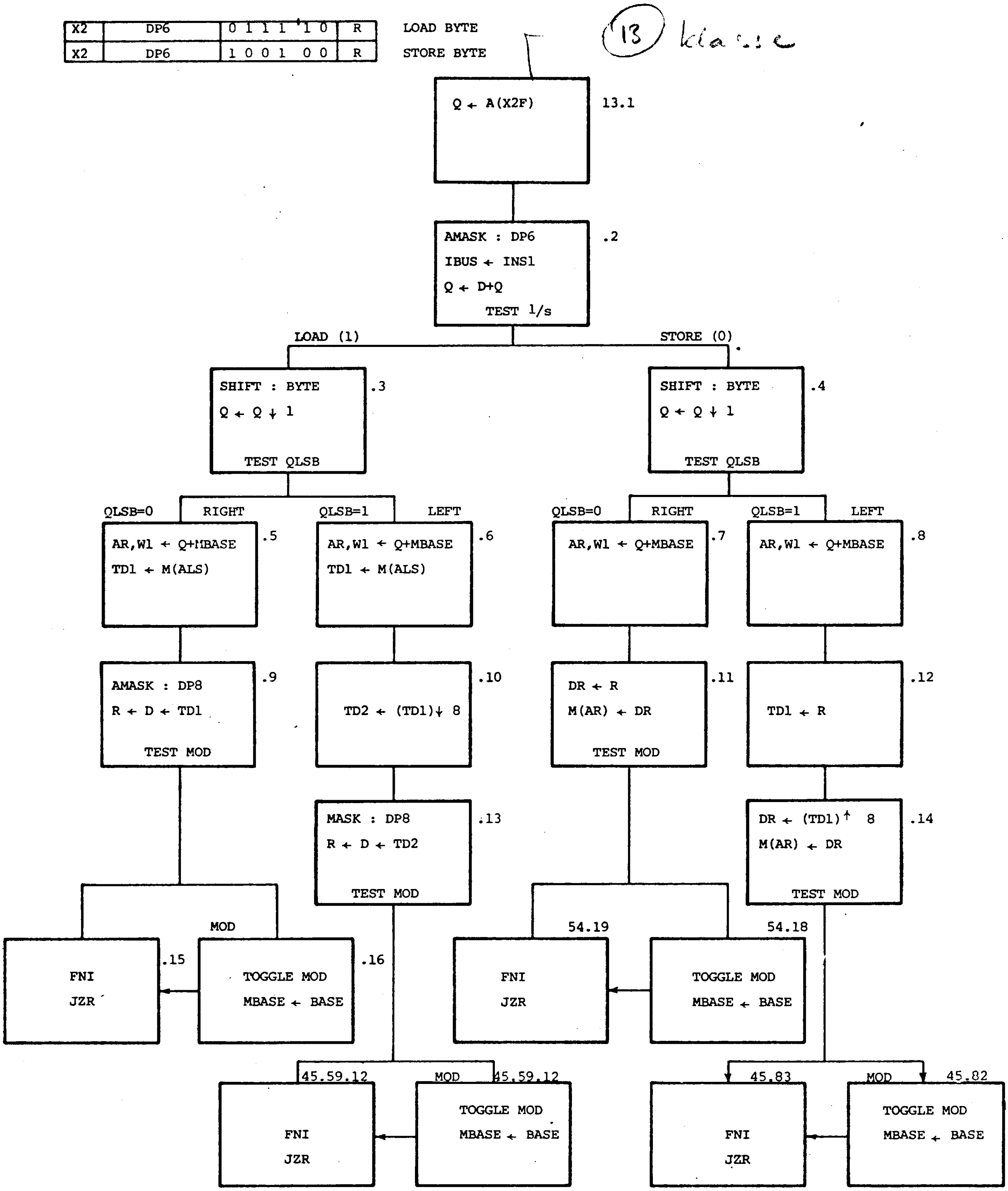
3-1677

Sheet 21 of 26 sheets

Issue	V6	V9
Date	770429	770621
Approved	JHØ	JHØ

X2	DP6	0 1 1 1 1 0	R	LOAD BYTE
X2	DP6	1 0 0 1 0 0	R	STORE BYTE

13 klasse



CHRISTIAN ROVSING A/S

CR8001
MOVE BYTE

Scale		Approved		Issue	2
Date	770601			Date	770601
Drawn	JHØ			Approved	JHØ
Parts no		3-1677			
Print no		Sheet 25 of 36 sheets			

LOAD:

0 1 1 0 1	R	DP8

STORE:

0 1 1 1 0	R	DP8

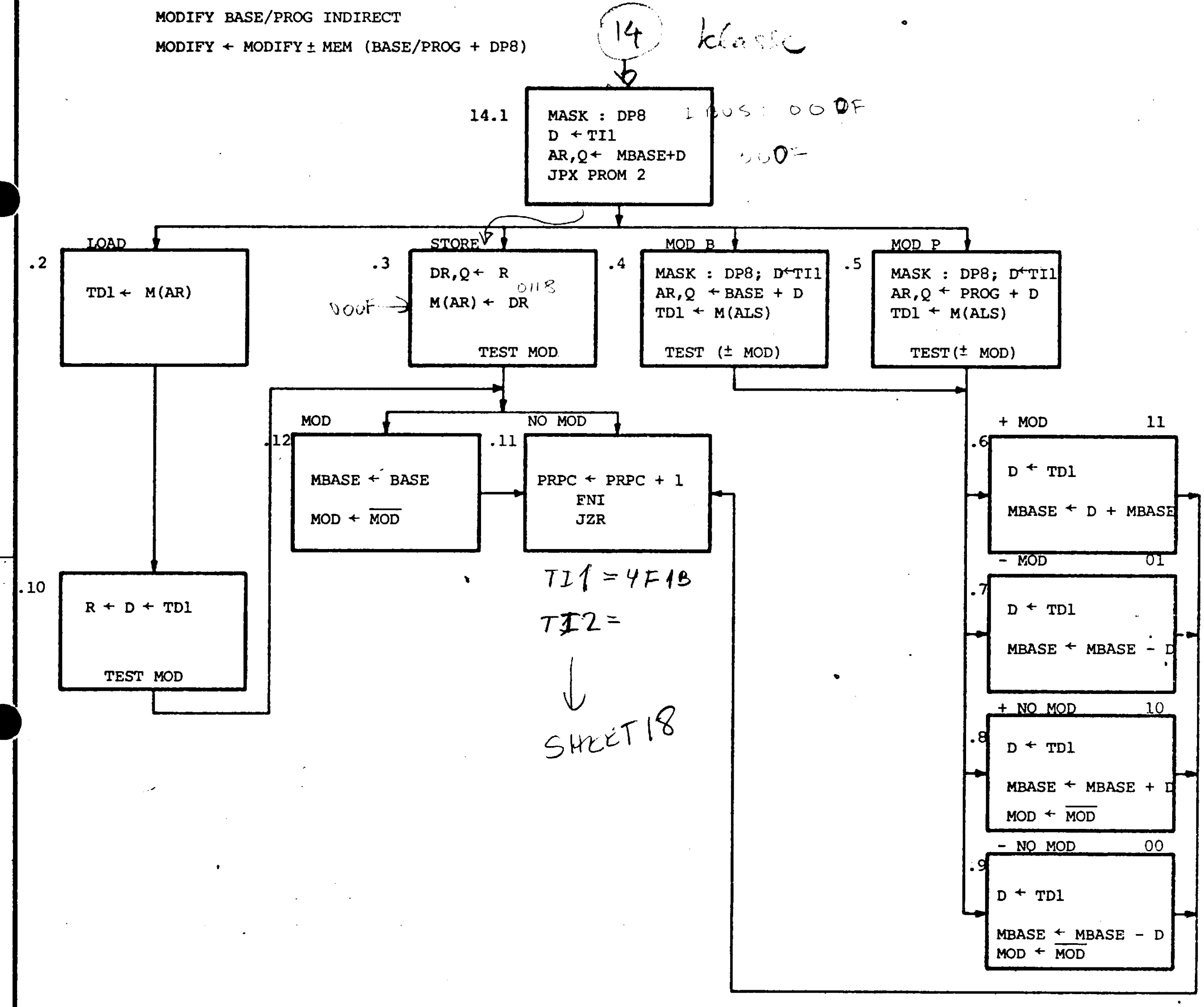
LOAD/STORE BASE RELATIVE

$R_{0-7} \rightleftarrows$ MEM (BASE + MODIFY + DP8)

0 0 1 0 1 0 0	DP8	BASE INDIRECT
0 0 1 0 1 0 1	DP8	PROG INDIRECT

MODIFY BASE/PROG INDIRECT

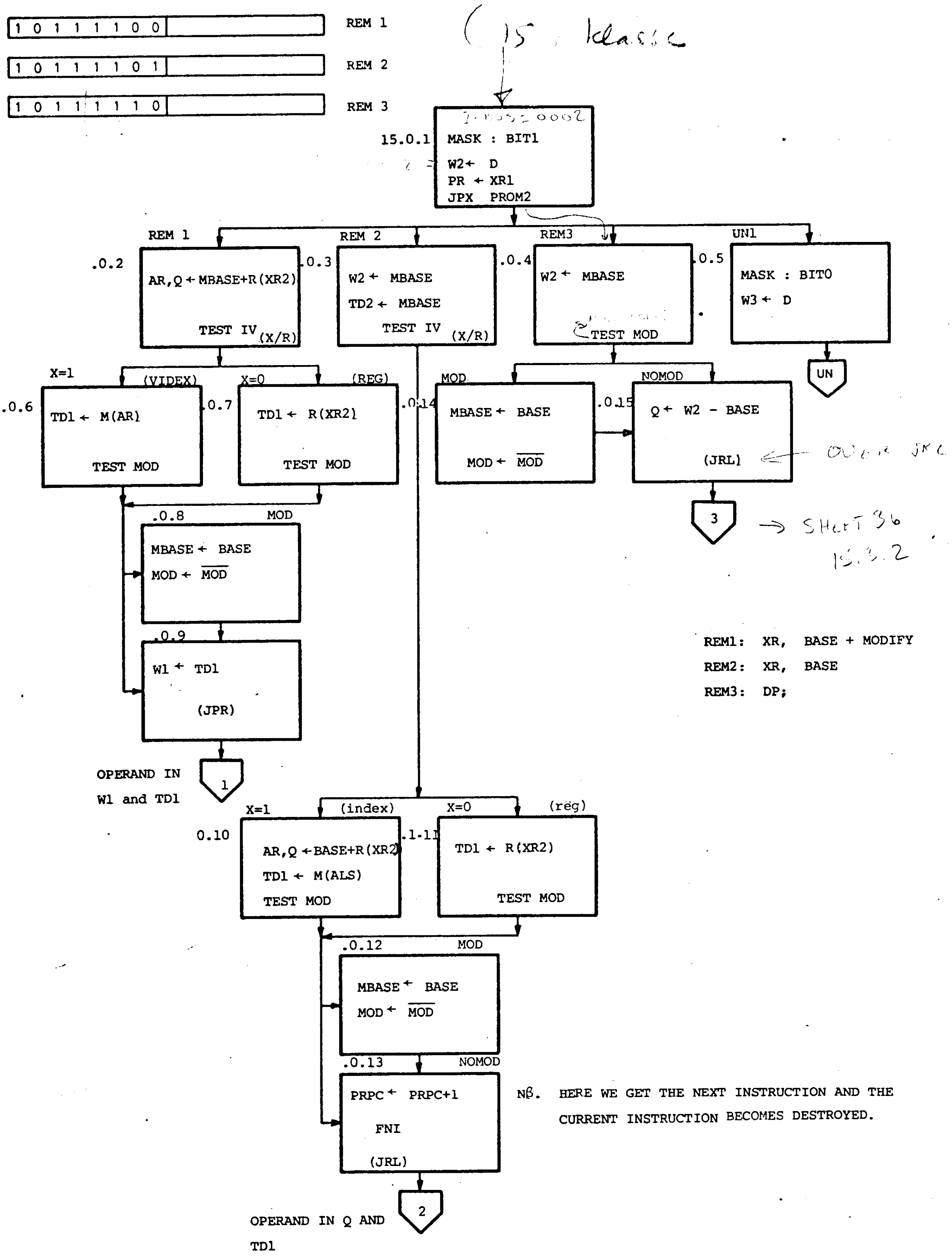
MODIFY ← MODIFY ± MEM (BASE/PROG + DP8)



CHRISTIAN ROVSING A/S

CR8001 MP
CLASS XIV

Scale		Approved		Issue	V6
Date	750821			Date	770429
Drawn	JHØ			Approved	JHØ
Parts no		3-1677			
Print no		Sheet 26 of 36 sheets			



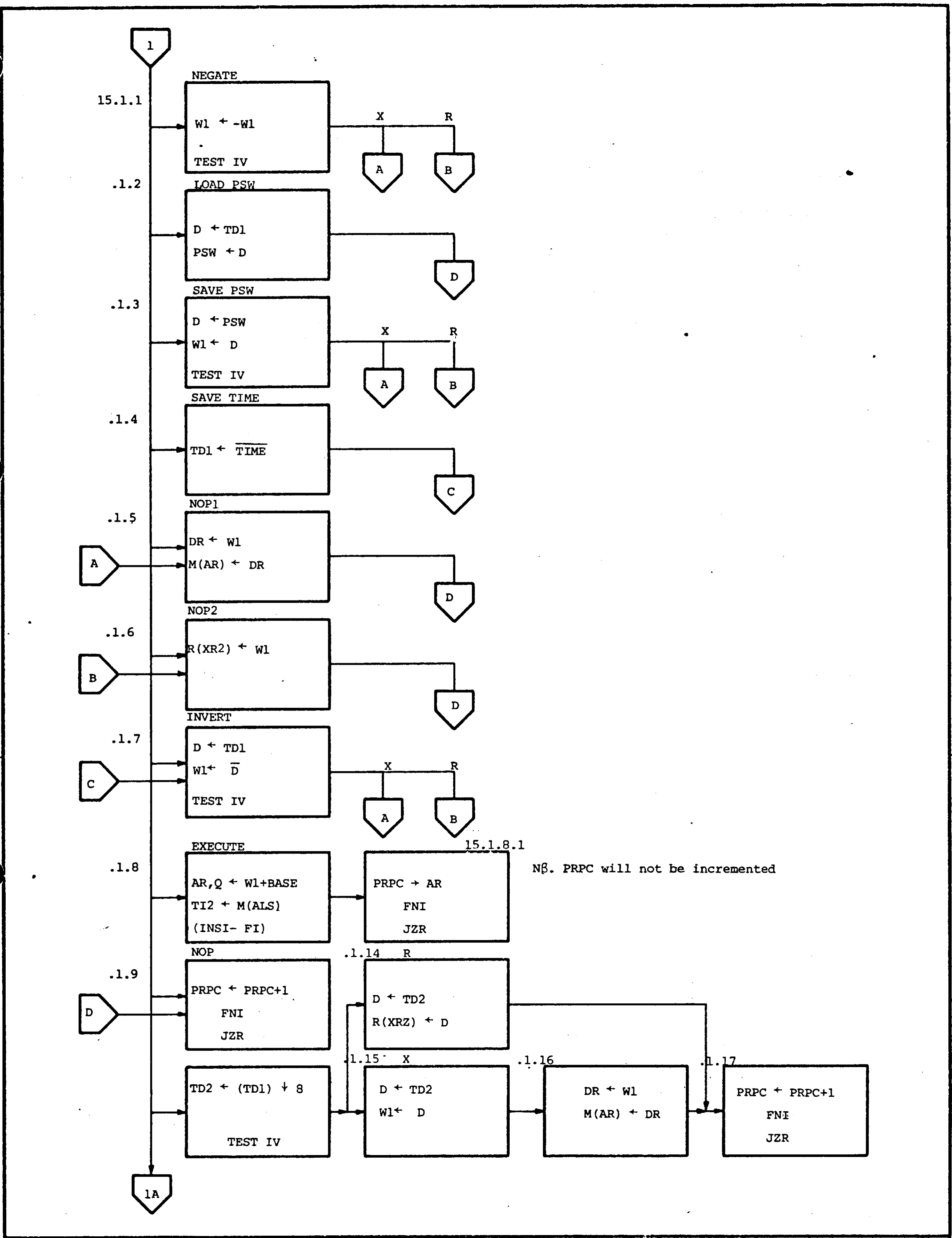
REM1: XR, BASE + MODIFY
REM2: XR, BASE
REM3: DP;

NB. HERE WE GET THE NEXT INSTRUCTION AND THE CURRENT INSTRUCTION BECOMES DESTROYED.

CHRISTIAN ROVSING A/S

CR80C1 MP
CLASS XV

Date	78 - 05 - 18	E	Issue	1
Drawn	JHØ/LJA		Date	78-05-18
Parts no		3-1677		
		Sheet 27 of 36 sheets		

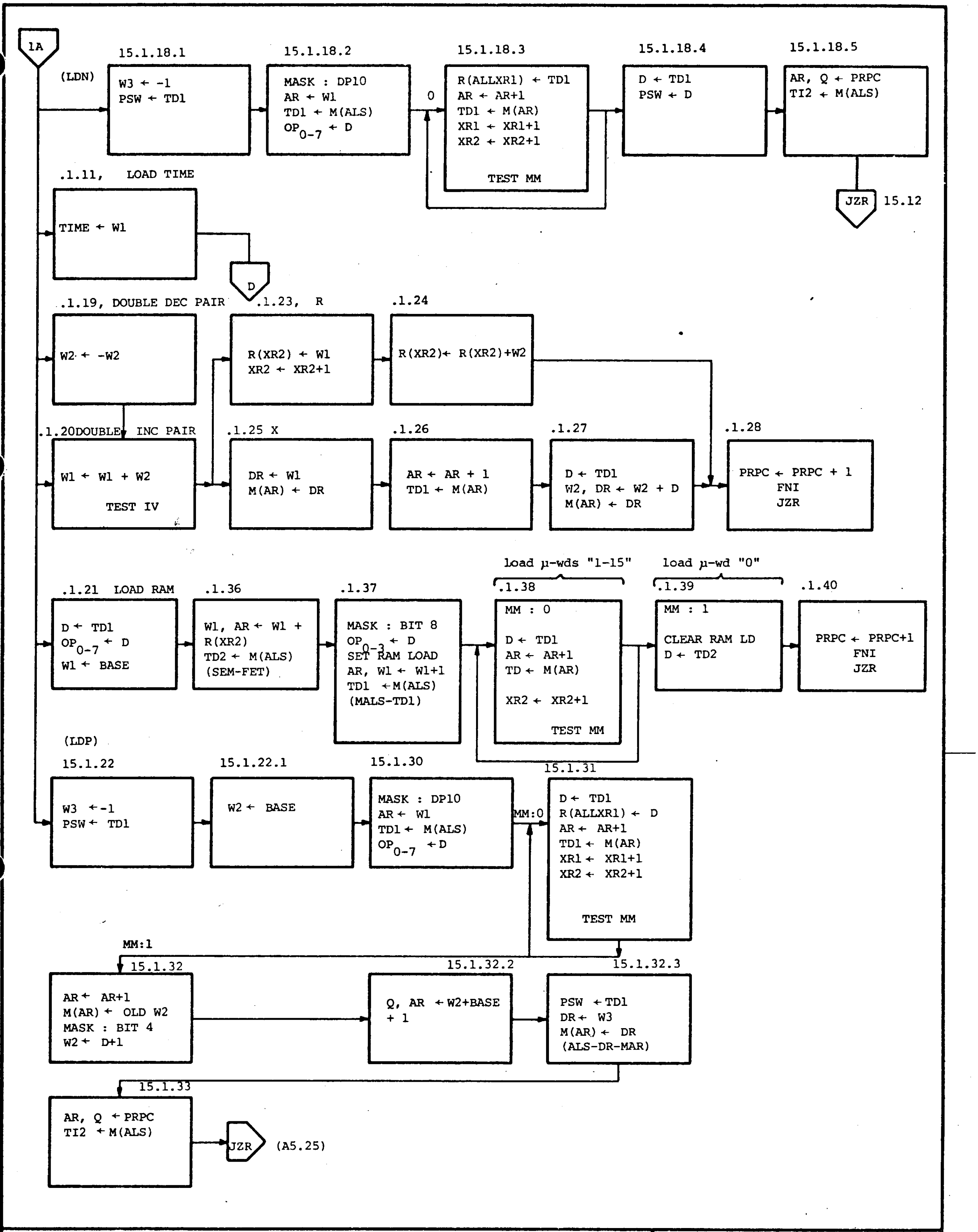


Nβ. PRPC will not be incremented

CHRISTIAN ROVSING A/S

CR8001 MP
CLASS XV

Scale		Approved		Issue	1
Date	78 - 05 - 18	E		Date	78-05-18
Drawn	JHØ/LJA			Approved	
Parts no		3-1677			
Print no		Sheet 25 of 36 sheets			

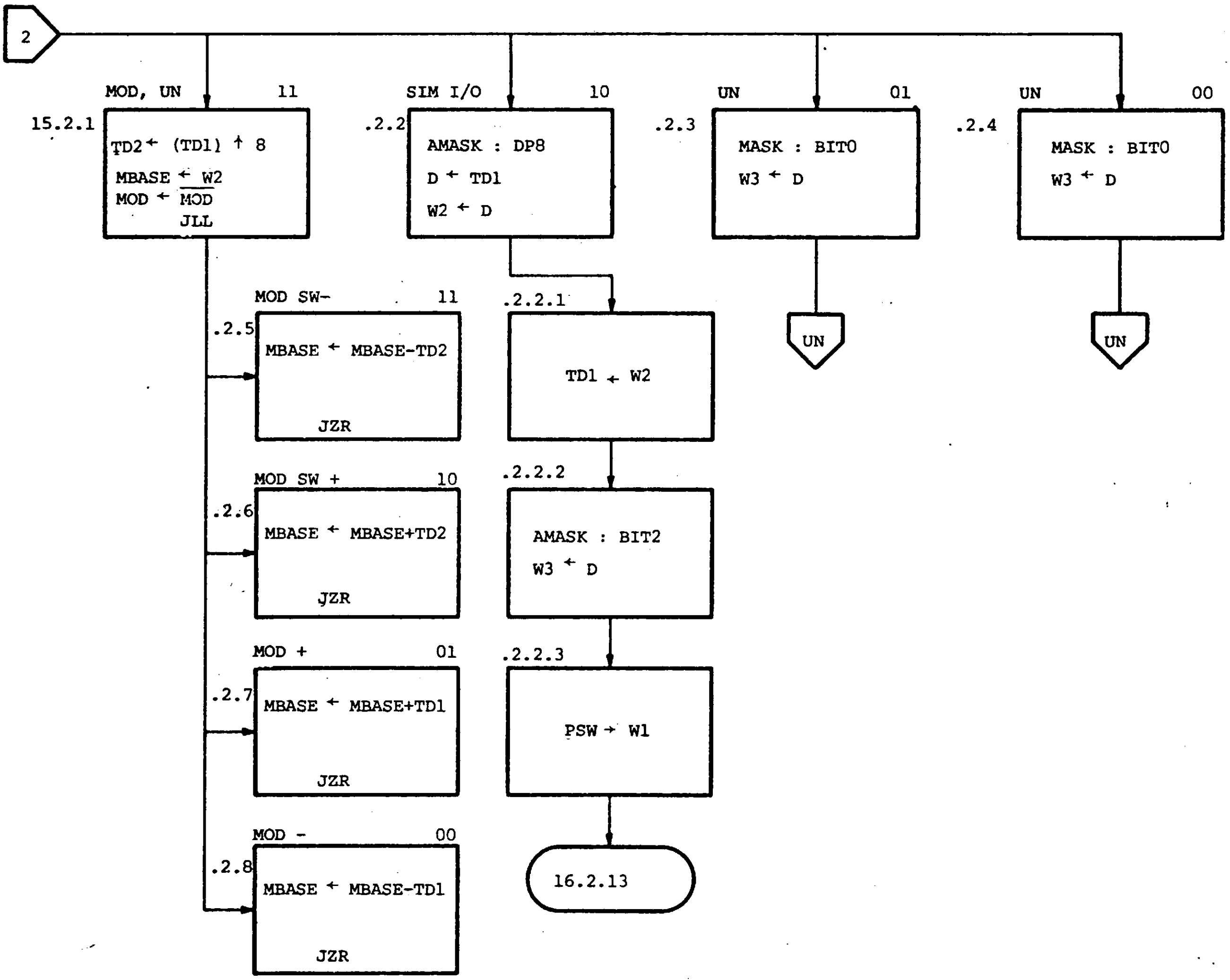


CHRISTIAN ROVSING A/S

CR8001 MP

CLASS XV

Scale		Approved		Issue	1
Date	78 - 05 - 18	E		Date	78-05-18
Drawn	JHØ / LJA			Approved	
Part no		3-1677			
Drawing no		Sheet 29 of 34 sheets			

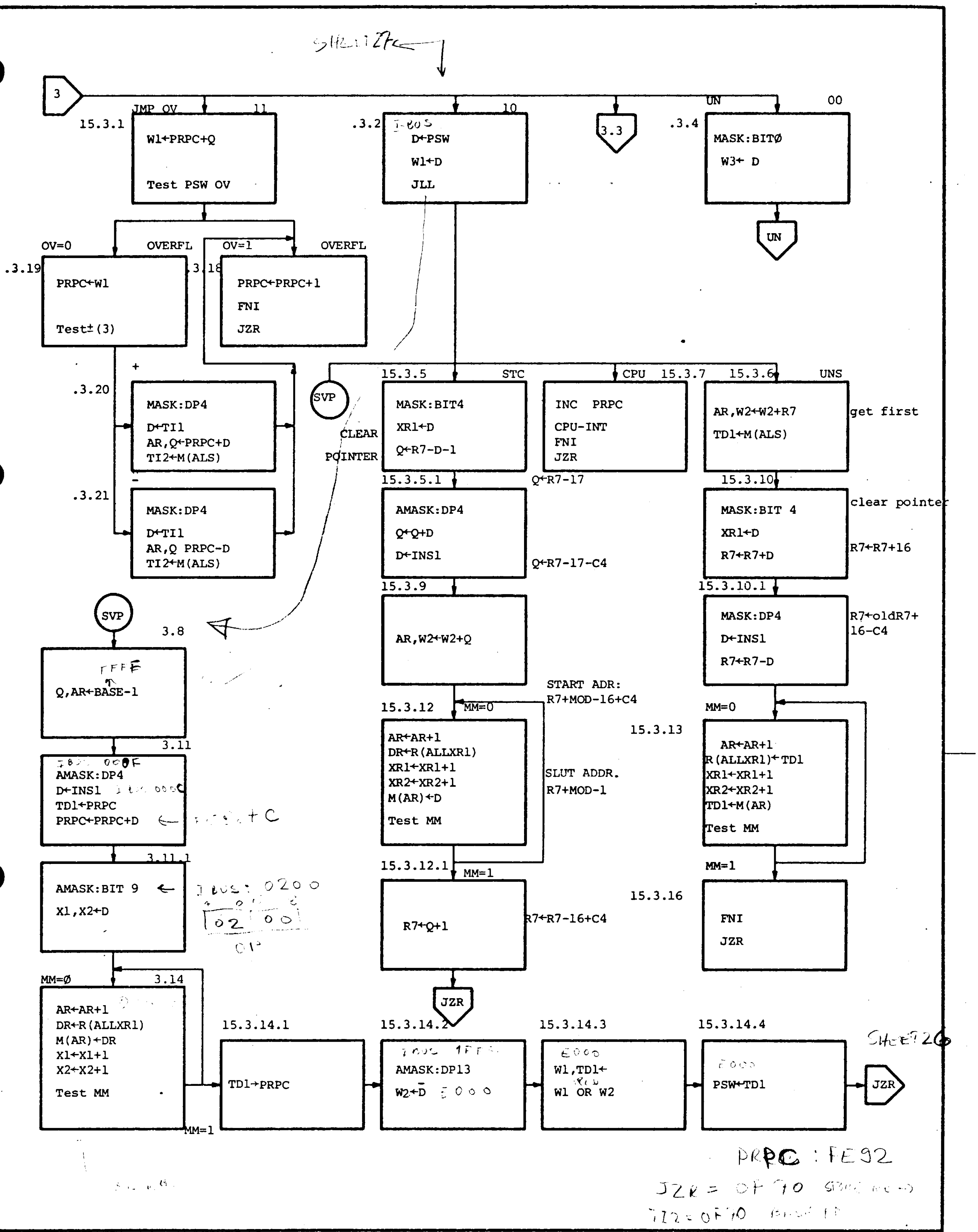


CHRISTIAN ROVSING A/S

CR8001 MP
CLASS XV

Scale		Approved	
Date	78 - 05 - 18	E	
Drawn	JHO / LJA		
Parts no		3-1677	
Print no		Sheet 20 of 36 sheets	

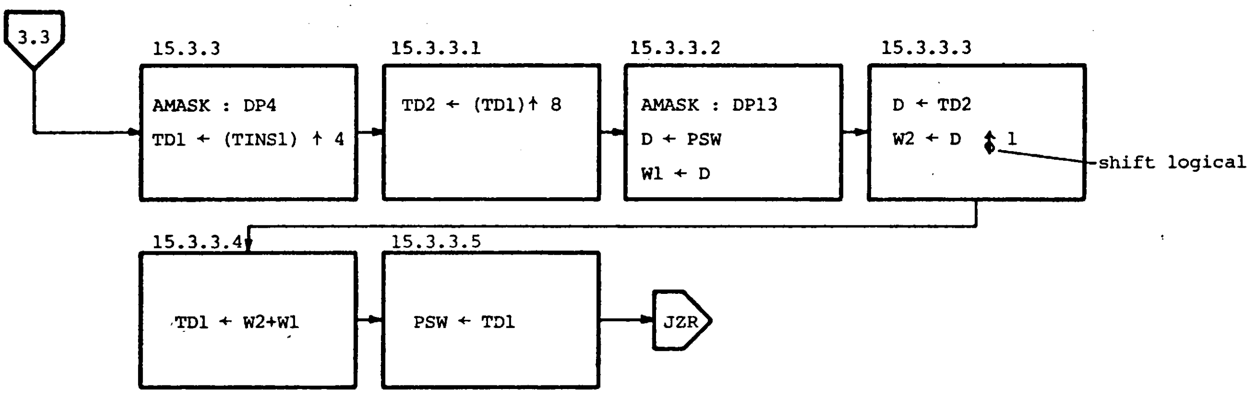
Issue	1
Date	78-05-18
Approved	



CHRISTIAN ROVSING A/S

CR8001 MP
CLASS XV

Scale		Approved		Issue	4	V6
Date	750821			Date	751031	770429
Drawn	JHØ			Approved	JHØ	JHØ
Parts no		3-1677				
Print nr		Sheet 31 of 36 sheets				

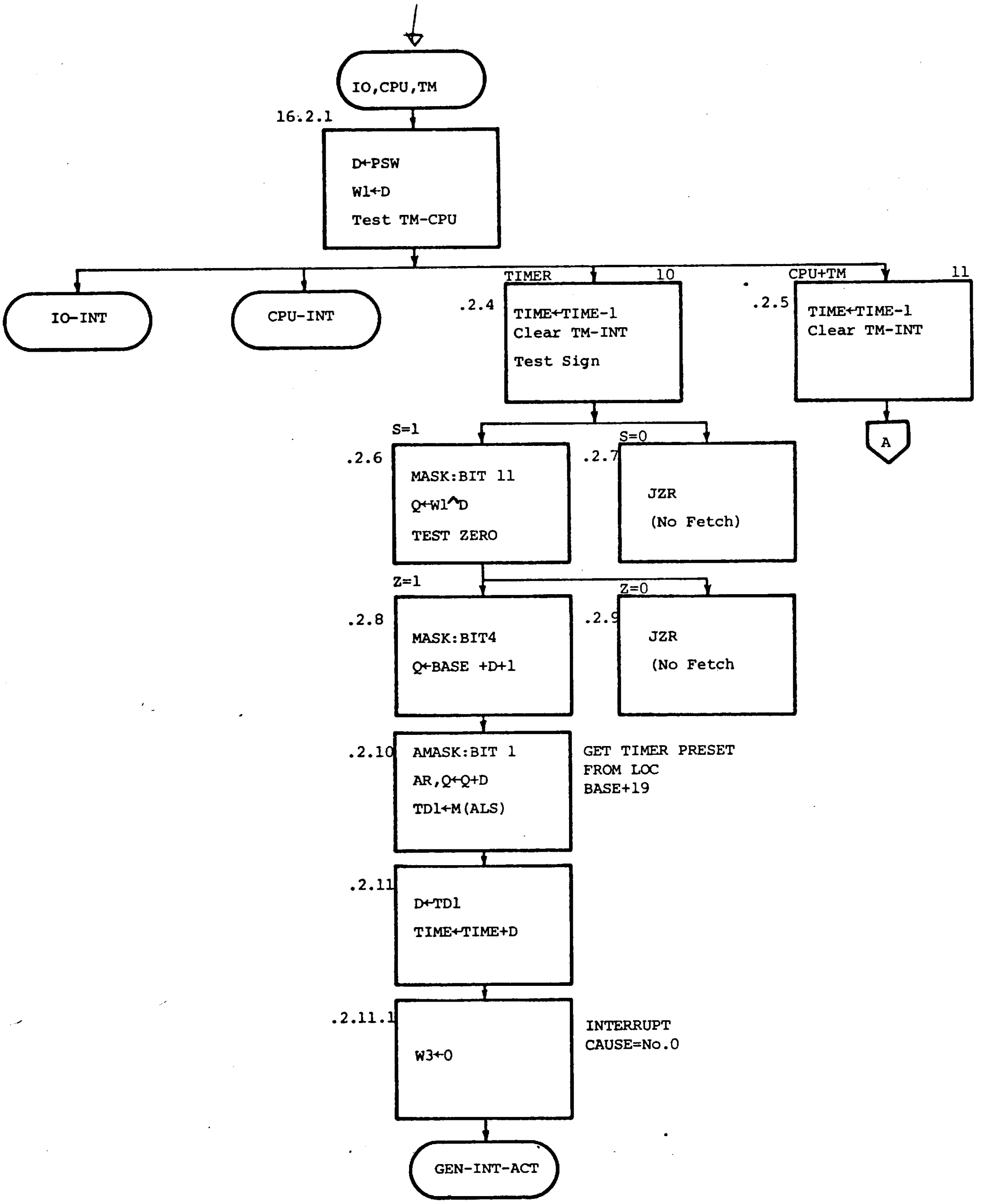


CHRISTIAN ROVSING A/S

CR8001 MP
CLASS XV

Scale		Approved		Issue	V6
Date				Date	770429
Drawn				Approved	JHØ
Parts no		3-1677			
Print no		Sheet 32 of 36 sheets			

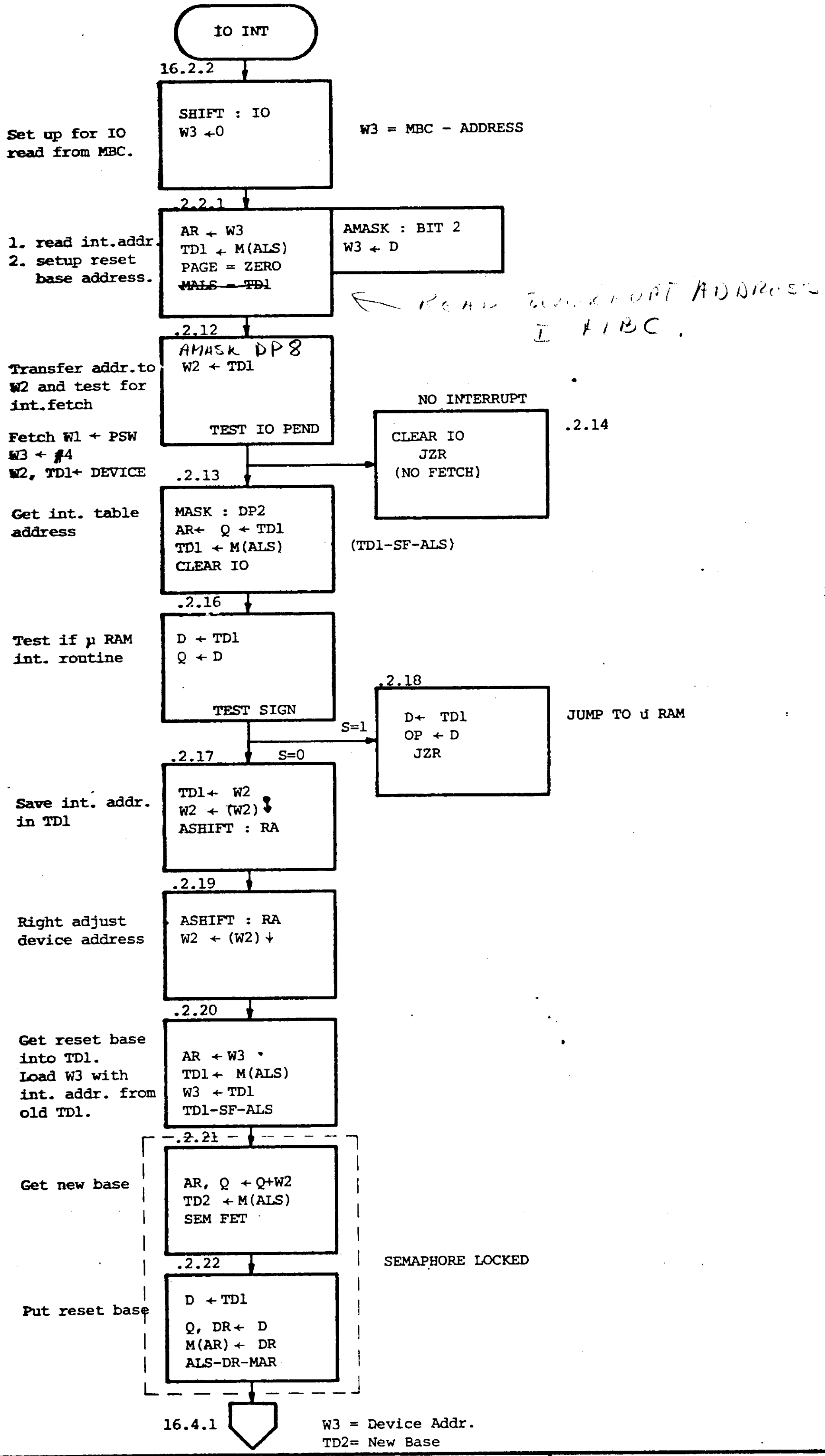
Interrupt klasse



CHRISTIAN ROVSING A/S

CR8001 MP
INTERRUPT

Scale		Approved		Issue	V6
Date	750822			Date	770429
Drawn	JHØ			Approved	JHØ
Parts no		3-1677			
Print no		Sheet 33 of 36			



CHRISTIAN ROVSING A/S

CR8001

IO INTERRUPT

Scale		Approved		Issue	V6
Date				Date	770429
Drawn				Approved	JHØ
Parts no		3-1677			
Print no		Sheet 34 of 36 sheets			

CPU MESSAGE

1) | 1 | 0 0 0 |

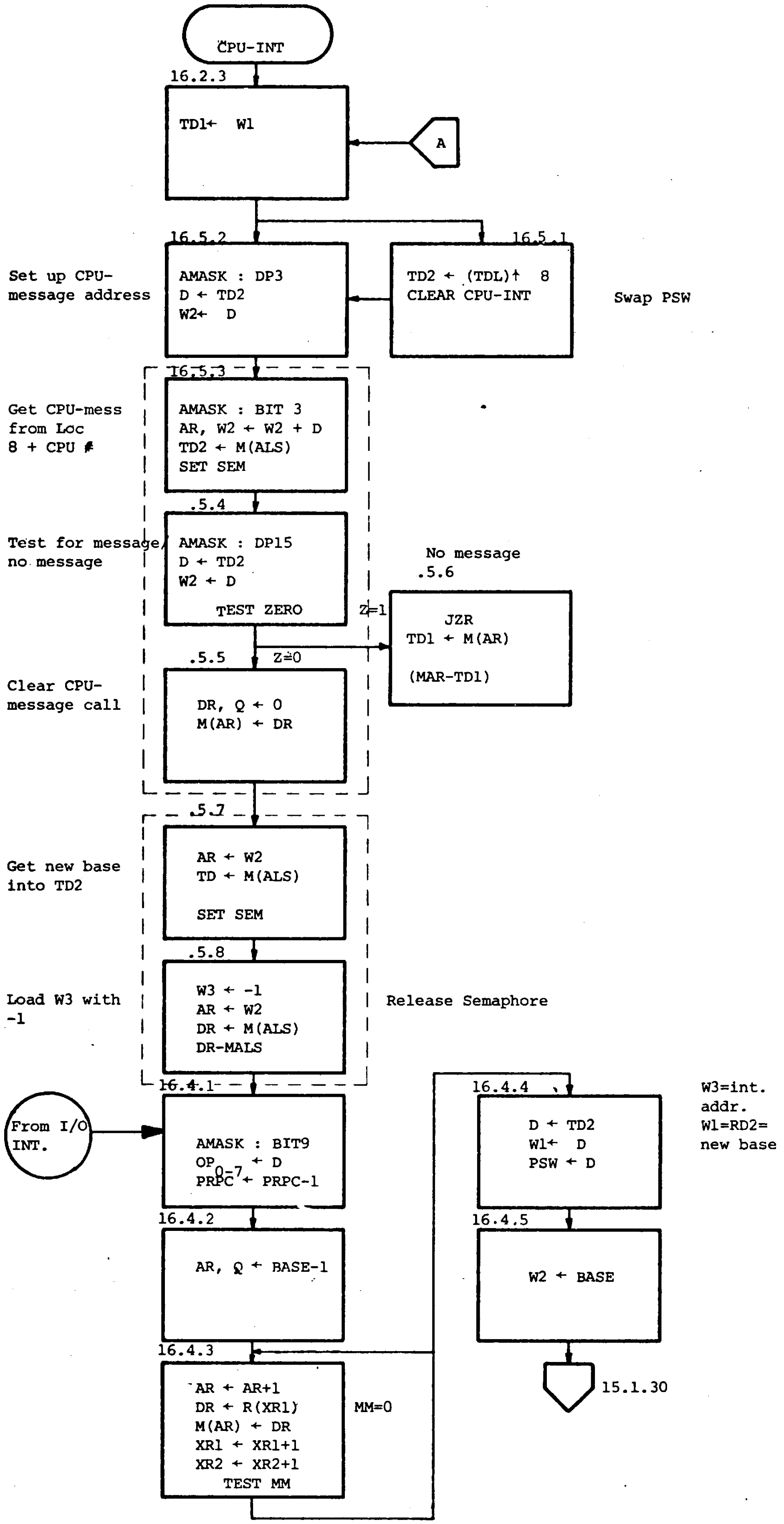
2) | 1 | -pointer≠0- |

3) | 0 | 0 0 |

ad 1.
Reserved call with no message.

ad 2.
Reserved call with message.

ad 3.
Unreserved call.

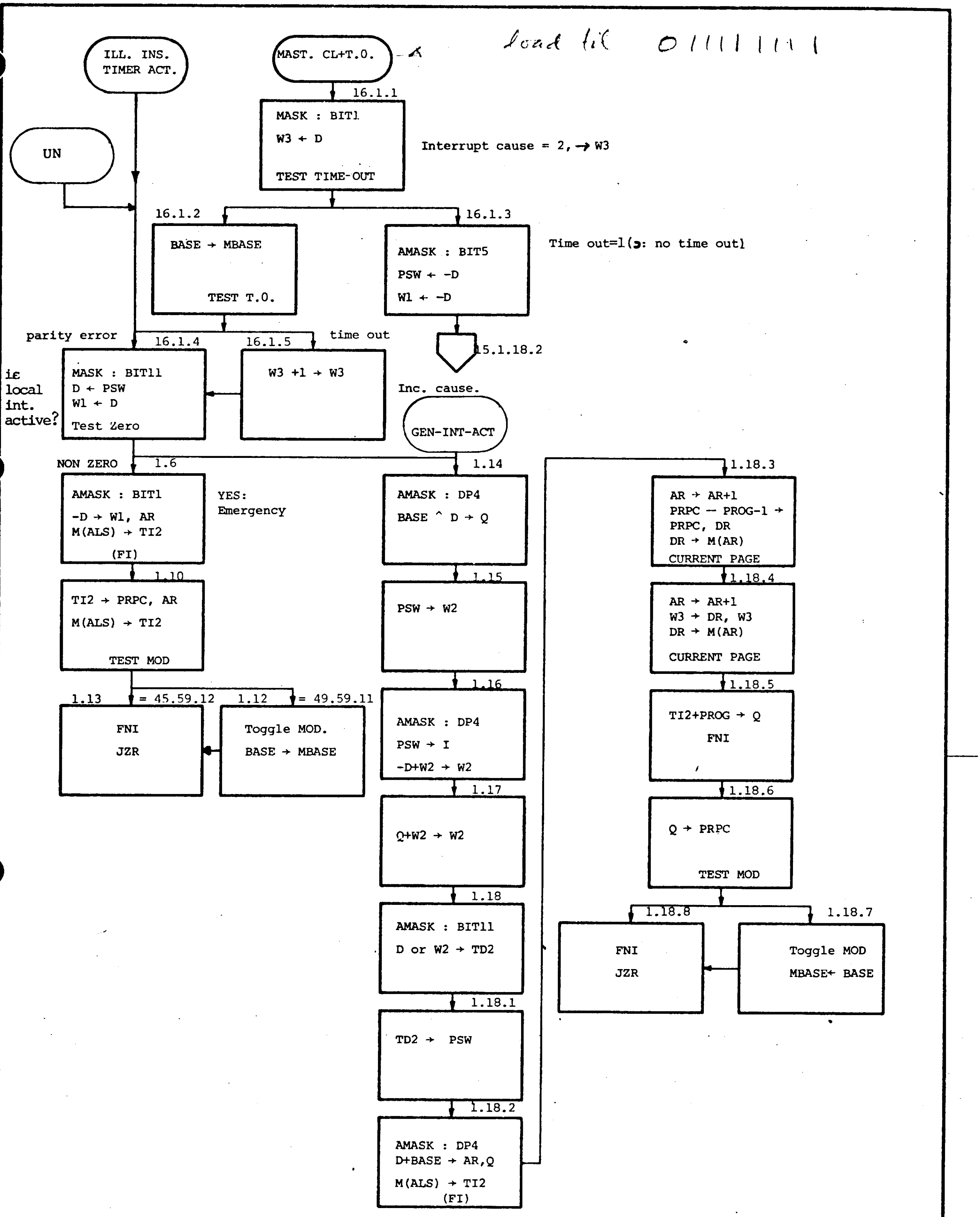


CHRISTIAN ROVSING A/S

CR8001

CPU INTERRUPT

Scale		Approved		Issue	V6
Date				Date	770429
Drawn				Approved	JHØ
Parts no		3-1677			
Print no		Sheet 35 of 36 sheets			



CHRISTIAN ROVSING A/S

CR8001 MP
INTERRUPT

Supersedes	Approved	Issue
Date		Date
Drawn		Approved
Parts no	3-1677	
Project	Sheet 36 of 36 sheets	

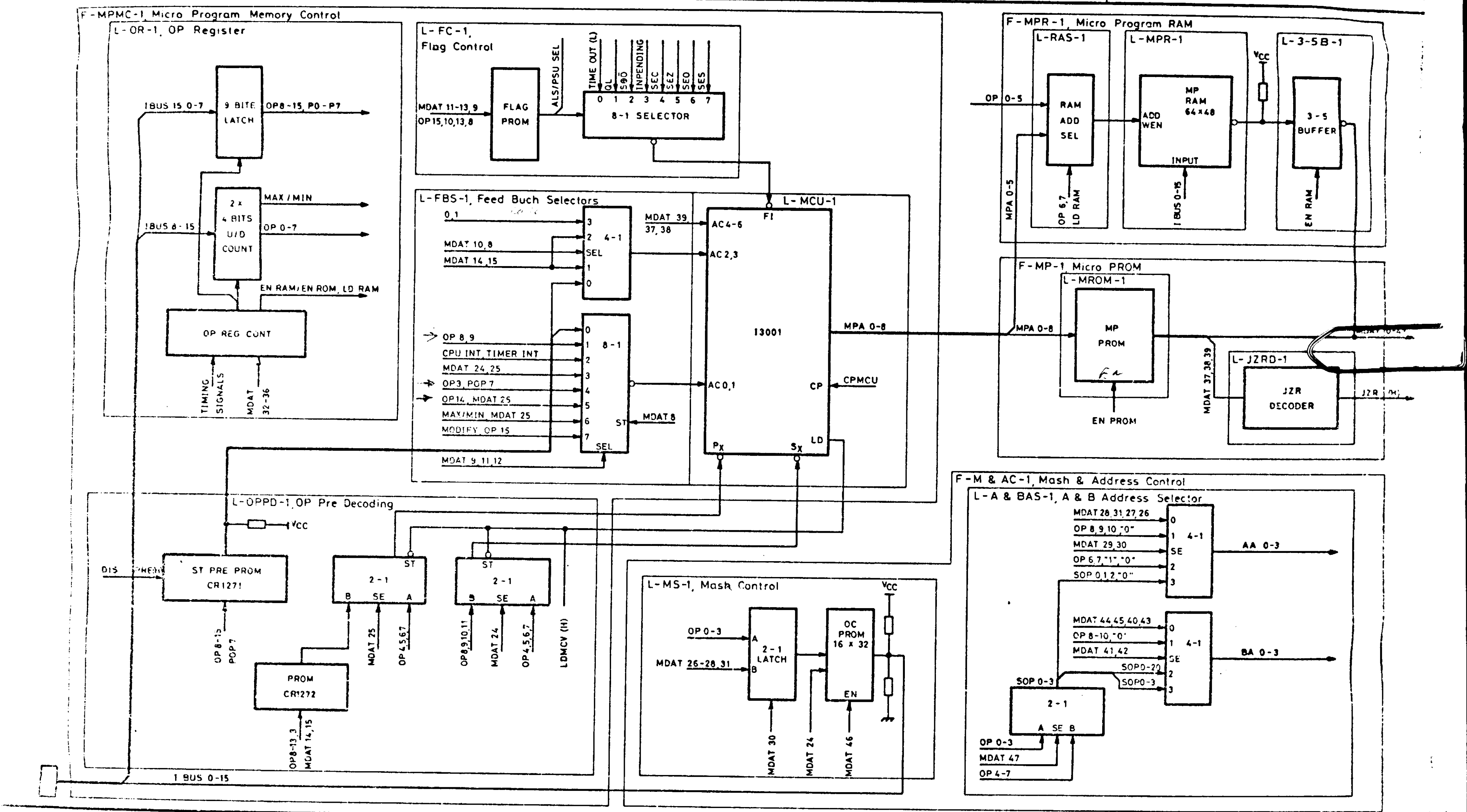
1. GENERAL DESCRIPTION

The MPB contain the circuit necessary for decoding of the CPU instructions into micro instructions and thereby controlling of the entire CPU.

The MPB is a standard CR80 PCB without edge connector for the Main Bus connection, because the connection to the other part of the CPU module is carried out by means of flat cables for the signal flow and two discreet wires for the power input +5V & GND. The MPB is connected to the Arithmetical Logical Board and the primary input to the board is the 16 bits width I-BUS and the different timing signals used for synchronization of the µ steps, the outputs are the Micro Program Data (MDAT) and signals determined from these. The MPB contain different functional and logical blocks ref Block Diagram. The instructions are stored in the OP register which consist of a counter section and a latch section. Decoding of the instruction, and thereby addressing of the MDAT is carried out by a Micro Program Control Unit(MCU), and different PROM's and selectors which are used for testing the different conditions for determining the next Micro Program Address (MPA). The MPA is the address input to the Micro Programm PROM or the optional Micro Program RAM. The address output from the MCU is 9 bits width corresponding to the number of µPROM words: 512 words, the µRAM contain only 64 words and use the 6 least significant bits of the address field when in the execution mode and the 9 least significant bits of the OP register for loading of the RAM. The micro word is 48 bits width, meaning that three 16 bits words from I-BUS have to be loaded into the µRAM for generation of one micro word.

MICRO PROGRAM BOARD (MPB)	sign/date GB/780520	page
	repl	project

Beside the function directly related to the Micro Program Control &-Memory the MPB contain a mask circuit which operate on the I-BUS and the selectors for selection of the 2 x 4 bits ALU addresses.



F-MPMC-1 Micro Program Memory Control
L-OR-1, OP Register
IBUS 15 0-7
9 BITE LATCH
OP8-15, P0-P7
IBUS 8-15
2 x 4 BITS U/D COUNT
MAX/MIN
OP 0-7
EN RAM/EN ROM, LD RAM
OP REG CONT
TIMING SIGNALS
MDAT 32-36
L-FC-1, Flag Control
MDAT 11-13, 9
OP15,10,13,8
FLAG PROM
ALS/PSU SEL
TIME OUT (L)
OL
SØØ
INPENDING
SEC
SEZ
SEO
SES
0 1 2 3 4 5 6 7
8-1 SELECTOR
L-FBS-1, Feed Buch Selectors
0,1
MDAT 10,8
MDAT 14,15
3
2
SEL
1
0
4-1
MDAT 39, 37, 38
OP 8,9
CPU INT, TIMER INT
MDAT 24,25
OP3, POP 7
OP14, MDAT 25
MAX/MIN, MDAT 25
MODIFY, OP 15
MDAT 9,11,12
8-1
ST
SEL
MDAT 8
L-MCU-1
FI
AC4-6
AC 2,3
13001
AC 0,1
MPA 0-8
CP
CPMCU
Px
Sx
LD
F-MPR-1, Micro Program RAM
L-RAS-1
OP 0-5
RAM ADD SEL
OP 6,7
LD RAM
MPA 0-5
L-MPR-1
MP RAM 64 x 48
ADD WEN
INPUT
I BUS 0-15
Vcc
L-3-5B-1
3-5 BUFFER
EN RAM
F-MP-1, Micro PROM
L-MROM-1
MPA 0-8
MP PROM
EN PROM
MDAT 37,38,39
L-JZRD-1
JZR DECODER
JZR (H)
L-OPPD-1, OP Pre Decoding
Vcc
DIS
PREH
ST PRE PROM CR1271
OP 8-15
POP 7
2-1
ST
B
SE
A
MDAT 25
OP 4,5,6,7
PROM CR1272
OP8-13,3
MDAT 14,15
OP8,9,10,11
MDAT 24
OP 4,5,6,7
LDMCV (H)
1 BUS 0-15
L-MS-1, Mash Control
OP 0-3
MDAT 26-28,31
A
B
2-1 LATCH
OC PROM 16 x 32
EN
Vcc
MDAT 30
MDAT 24
MDAT 46
F-M & AC-1, Mash & Address Control
L-A & BAS-1, A & B Address Selector
MDAT 28,31,27,26
OP 8,9,10,"0"
MDAT 29,30
OP 6,7,"1","0"
SOP 0,1,2,"0"
0
1
SE
2
3
4-1
AA 0-3
MDAT 44,45,40,43
OP 8-10,"0"
MDAT 41,42
SOP0-2
SOP0-3
BA 0-3
SOP 0-3
2-1
A SE B
OP 0-3
MDAT 47
OP 4-7

2. SPECIFICATION FOR MPB

This specification describe the MPB from a H/W point of view.

2.1 Input Power

+5V	:	± A	Without µRAM
+5V	:	± A	Including µRAM

The power to the PCB is feed through two discreet wires from the ALB. The wires are soldered on stand off-pins on the soldering side of the board.

2.2 Mechanical Dimension

The MPB is a standard CR80 PCB with the following dimensions : 183.4 x 280 mm.

Hight of component side	:	8 mm
Hight of soldering side	:	8 mm

2.3 Input/Output Signals

The input/output signals to the MPB are normal TTL logic levels. The signal are connected to the board via 16 wires flat cables mounted on the soldering side of the PCB. The signal lists section 5 specify the different flat cables.

2.4 Micro Memory Area

PROM	512 x 48 bits word
optional RAM	64 x 48 bits word

For the PROM contents ref version description document for the actual CPU P/N.

MICRO PROGRAM BOARD (MPB)	sign/date GB/780520	page
	repl	project

2.5 Timing

Cycle time for the MPB is :

minimum	375 ns
maximum	∞ ns

3. FUNCTIONAL DESCRIPTION

3.1 Introduction

This description covers the MPB with the optional µRAM feature included and the micro sequences included in the description are taken from the standard CR80 instruction set. If the optional µRAM is not included it is specified in the parts list. For the actual µPROM contents and specification ref section 4 in this document µ-PROM TABLES. During this description the Block Diagram for the MPB, has to be used as reference for the different functions and signals description.

3.2 General Description

The different µ steps, the MPB has to go through is determined by the contents of the µPROM/RAM, (by means of direct feed back from the output and/ or selection of different flag to be tested on) and the instruction loaded into the OP register from the internal CPU open collector bus: I BUS. When the power is switched on the CPU, the MPA will be determined by the signal LD MCU (H) which load the contents of the MCU's secondary & primary instruction bus SX & PX into the MCU address register. The signal LD MCU(H) will at the same time force SX & PX to "0" meaning that the µ Program start address is row add. 15 & column add. 15 (dec). LD MCU(H) can be forced active by the following conditions; CPU clear, Time out & Parity error, therefore the following µ step after a LD MCU (H) are used for determining the source for LD MCU. This determination is carried out by testing on the Time out flag and thereby determining the next µ step.

If the Time out flag is low it has to be tested once more because the flag contain information about both time out and parity error, in the second test it is time out without parity which is tested, the selection of time out in stead of both time out and parity error as test input, is specified by carry/page control lines from the µPROM, ref MDAT functional description. The µ steps which will be taken after the entry in MPA 15.15 is specified in µ - Program Flow Chart, which contain the actual µ Program included in the CPU.

If the µ program is the CR80 standard instruction set the LD MCU forced by a CPU clear, will load the ALU registers and PSW, and after that fetch an instruction specified during the register load. The process load will be terminated by loading, and start of execution of the first instruction from the main memory. The entry in the µ program in the first µ step of an instruction is determined by the latch part of the OP reg. These nine bits are feed to the PRE PROM, and in the same µ step the function code to the MCU AC4 - AC6 is set to JZR (jump to zero row). The remaining part of the function code AC0 - 3 is selected from the four PRE PROM output, meaning that the instructions is divided in 15 different classes, because one of the 16 possible entries is used for interrupt.

The MCU function code JZR is decoded to the signal JZR (H) and this is used to enable test for waiting interrupt (I/O, CPI & Timer).
The enabling is carried out on the ALB, and if there is an interrupt present, the signal DIS PRE (H) will go high and thereby force all one on the output of the PRE PROM and therefore will the interrupt routine be executed in stead of the instruction present in the OP reg. The entry for the interrupt is MPA 0.12 (dec)

because ACO & AC1 is the inverted output of the PRE PROM.

If the MPA is forced to 0.12 by an interrupt the next µstep is used to solve which of the possible interrupt there have generated DIS PRE (H). This is done by selecting CPU INT & TIMER INT as input to the two MCU function bits ACO & AC1, for the actual µstep used in the interrupt routine ref µ Program Flow Chart.

If the JZR function result in an instruction decoding, PRE PROM output determined by OP 8-15, POP7, the next µstep to be performed is either conditional or unconditional jumps determined by the feed back from the micro program output. The next MPA during instruction execution can be controlled by the OP reg. contents by means of the function input to the MCU ACO & AC1 or by the PX input either direct from OP4 - 7 or by table look up in PROM 2 where four tables for OP8 - 13 & OP3 are programmed. The SX input is used for jumping direct on either OP8 - 11 or OP4 - 7. When the flag input to the MCU is used for next µ MPA control, the input is selected by a part of the OP register 4 bits, and 3 output from the µ program. There are eight possible flag input, six containing the information about the ALU, the Time Out signal, and I/O pending specifying whether an interrupt fetch from the MBC is valid or not.

The MPB contain also circuit not directly related to the µ program sequences. These are a mask circuit used to enable one bit or bit strings on the I BUS and the selecter circuit used to select the source for the ALU register addresses.

MICRO PROGRAM BOARD (MPB)	sign/date GB/780520	page
	repl	project

The MPB is divided into the following functional blocks:

F-MPMC-1	Micro Program Memory Control
F-MP-1	Micro PROM
F-MPR-1	Micro RAM
F-M & AC - 1	Mask & Address Control

These functional blocks are described in details in section 3.4 to 3.7.
The micro program output MDAT signals are in section 3.3 described in details.

3.3 Description of Micro Program Output MDAT 0 - 47

The 48 outputs from the micro program MDAT 0 - 47 are used for controlling the entire CPU, CR8001/2 or CR8001/3. The signals are divided into the following functional groups.

1. ALU Instructions
2. ALU Address , Shift & Mask Control.
3. Bus & T File Control
4. OP reg & PSW Contol
5. Carry, Page & TO/PE Control
6. Next, MPA Control

The table overleaf shows the MDAT lines and function.

MDAT	FUNCTIONS		MDAT		
0	ALS INSTRUCTIONS				
1					
2					
3					
4					
5					
6					
7					
8	MCU INSTRUCTIONS F,B AC0-4 FB CONTROL AC0-4				
9			9	FLAG SELECT PROM	
10					
11			11		
12			12		
13			13		
14	(AC2)	MCU F.B			
15	(AC3)				
16	BUS AND T-FILE CONTROL				
17					
18					
19					
20					
21	CARRY, PAGE AND TIME OUT/PARITY SELECT CONTROL				
22					
23					
24	(AC0)	MCU F.B			
25	(AC1)				
26	(AA3)	ALS A. ADDRESS CONTROL	26	BIT SEL	MASK CONT.
27	(AA2)		27	BIT SEL	
28	(AA0)		28	BIT SEL	
29	SELA		29	MASK TYPE	
30	SELB		30	MASK SEL (OP/MDAT)	
31	(AA1)		31	BIT SEL	
32	OP-AND PSW CONTROL				
33					
34					
35					
36					
37	AC5	MCU INSTRUCTIONS			
38	AC6				
39	AC4				
40	(BA2)	ALS B. ADDRESS CONTROL			
41	SELA				
42	SELB				
43	(BA3)				
44	(BA0)				
45	(BA1)				
46	MASK ENABLE				
47	XR SEL (SEL SOP)				

3.3.1 ALS Instructions

The 8 ALU instruction bits is feed from the MPB to the ALB. The correspondance between the ALU instructions and the MDAT lines is specified in table below.

TABLE 3.3.1

MDAT BITS	5	4	1	6	7	0	2	3
ALU INSTRUCTION BITS	I0	I1	I2	I3	I4	I5	I6	I7
ALU FUNCTION	INSTRUCTION MODIFIERS			INSTRUCTIONS				

For more detailed specification ref ALB description.

3.3.2 ALU, Address & Shift Control, and Mask Control

The 14 bits used for controlling of the ALU addresses A & B and the ALU shift functions together with the mask control are specified in following 3 tables 3.3.2a - c.

ALU Register Addressing:

A address & shift control:
MDAT 26 - 31, 47

TABLE 3.3.2.a

A. ADDRESS SELECT			A. ADDRESS & SHIFT CONT.			
MDAT 47	MDAT 30	MDAT 29	AA3	AA2	AA1	AA0
Ø	0	0	MDAT 26	MDAT 27	MDAT 31	MDAT 28
Ø	0	1	"0"	OP10	OP9	OP8
Ø	1	0	"0"	"1"	OP7	OP6
0	1	1	"0"	OP2	OP1	OP0
1	1	1	"0"	OP6	OP5	OP4

B address:
MDAT 40 - 45, 47

TABLE 3.3.2.b

B. ADDRESS SELECT			B. ADDRESS			
MDAT 47	MDAT 42	MDAT 41	BA3	BA2	BA1	BA0
Ø	0	0	MDAT 43	MDAT 40	MDAT 45	MDAT 44
Ø	0	1	"0"	OP10	OP9	OP8
0	1	0	OP3	OP2	OP1	OP0
1	1	0	OP7	OP6	OP5	OP4
0	1	1	"0"	OP2	OP1	OP0
1	1	1	"0"	OP6	OP5	OP4

Mask Control:

MDAT 26 - 31, 46 (MDAT 26 - 31 are used for A address also).

TABLE 3.3.2.c

MDAT			BIT POINTER				MASK TYPE
46	29	30	2^3	2^2	2^1	2^0	
1	Ø	Ø	Ø	Ø	Ø	Ø	MASK DISABLED
0	0	0	OP3	OP2	OP1	OP0	LONG MASK
0	0	1	MDAT 26	MDAT 27	MDAT 31	MDAT 28	LONG MASK
0	1	0	OP3	OP2	OP1	OP0	BIT MASK
0	1	1	MDAT 26	MDAT 27	MDAT 31	MDAT 28	BIT MASK

3.3.3 Bus & T File Control

Five of the micro program output is used for controlling the CPU's internal bus's I-BUS + T-BUS and the transfer on the external bus Main- and/or Sub Bus. These five signals are: MDAT 16 - 20.
A detailed description of the signal is included in the ALB & BIB description.

3.3.4 OP Reg & PSW Control

The five bit used for controlling the OP register located on the MPB, are also used for control of the Process Status Word PSW which is placed on the ALB. The function description is covered in the OP register description and in the functional description of ALB.
The five bits are : MDAT 32 - 36.

3.3.5 Carry, Page & T0/PE Control

Three bits are used for controlling the input carry to the ALU and to make the proper selection of the 2 page bit used during bus access furthermore the same bits controls the selection of time out and parity error as test input to the MCU. The three bits are: MDAT 21 - MDAT 23.

3.3.6 Next MPA Control

For control of the next micro program address, either by direct feed back or by testing on different conditions, is carried out by thirteen bits from the micro program.

These bits are :

MDAT 8 - MDAT 15
MDAT 24 & MDAT 25
MDAT 37 - MDAT 39

The following tables gives a more detailed description of how the relationship and the function of the signals are.

MCU FUNCTION CONTROL AC0 - AC7

TABLE 3.3.6.a

FB CONTROL

								FB	
MDAT8	MDAT10	MDAT13	MDAT12	MDAT11	MDAT9	AC3	AC2	$\overline{AC1}$	$\overline{AC0}$
1	0	0	0	0	0	MDAT15	MDAT14	"0"	"0"
1	1	0	0	0	0	"1"	"0"	"0"	"0"
0	1 0	0	0	0	0	MDAT15 R1.3	MDAT14 R1.4	R1.2	R1.1
0	1 0	0	0	0	1	MDAT15 R1.3	MDAT14 R1.4	OP9	OP8
0	1 0	0	0	1	0	MDAT15 R1.3	MDAT14 R1.4	TIMERINT(H)	CPUINT (H)
0	1 0	0	0	1	1	MDAT15 R1.3	MDAT14 R1.4	MDAT25	MDAT24
0	1 0	0	1	0	0	MDAT15 R1.3	MDAT14 R1.4	POP7	R1.1
0	1 0	0	1	0	1	MDAT15 R1.3	MDAT14 R1.4	MDAT25	OP8
0	1 0	0	1	1	0	MDAT15 R1.3	MDAT14 R1.4	MDAT25	CPUINT (H)
0	1 0	0	1	1	1	MDAT15 R1.3	MDAT14 R1.4	OP15	MDAT24
0	1 0	1	0	0	0	MDAT15 R1.3	MDAT14 R1.4	R1.2	OP3
0	1 0	1	0	0	1	MDAT15 R1.3	MDAT14 R1.4	OP9	OP14
0	1 0	1	0	1	0	MDAT15 R1.5	MDAT14 R1.4	TIMERINT(H)	MAX/MIN (H)
0	1 0	1	0	1	1	MDAT15 R1.3	MDAT14 R1.4	MDAT25	MODIFY(H)
0	1 0	1	1	0	0	MDAT15 R1.3	MDAT14 R1.4	POP7	OP3
0	1 0	1	1	0	1	MDAT15 R1.3	MDAT14 R1.4	MDAT25	OP14
0	1 0	1	1	1	0	MDAT15 R1.3	MDAT14 R1.4	MDAT25	MAX/MIN(H)
0	1 0	1	1	1	1	MDAT15 R1.3	MDAT14 R1.4	OP15	MODIFY (H)

R 1.1 - R 1.4 _ Pre PROM output

AC4 : MDAT 39
AC5 : MDAT 37
AC6 : MDAT 38

Selection of flag input to the MCU is controlled of MDAT 9, 11-13 and the following four bits from the OP register OP 8, 10, 13, 15.

MCU Instruction bus's PX 0-3, SX 0-3.

TABLE 3.3.6.b

MDAT 24	MDAT 25	PX3	PX2	PX1	PX0	SX3	SX2	SX1	SX0
0	0	OP7	OP6	OP5	OP4	OP7	OP6	OP5	OP4
0	1	OP7	OP6	OP5	OP4	PXP3	PXP2	PXP1	PXP0
1	0	PXP3	PXP2	PXP1	PXP0	OP7	OP6	OP5	OP4
1	1	PXP3	PXP2	PXP1	PXP0	PXP3	PXP2	PXP1	PXP0

PXP0 - PXP3	are output from PROM 2
PXPU - PXP3	are determined by MDAT14, MDAT 15 & OP8 - 3.3.

For the function of AC0 - AC7. FI and PX0-3, SX 0-3 ref description of MCU.

3.4 Micro Program Memory Control F-MPMC-1

This functional block contain the circuit used for generating the micro program address.
The input to the F-MPMC-1 is the I-BUS for loading of the OP reg, feed back from the micro program output MDAT and timing signal for synchronization of the sequences. The block is divided in five logical block ref MPB Block Diagram.
These blocks are:

1. OP Register	L-OR-1
2. OP Pre Decoding	L-OPPD-1
3. Feed Back Selectors	L-FBS-1
4. Flag Control	L-FC-1
5. Micro Program Control, Unit.	L-MCU-1

3.4.1 OP Register L-OR-1

This logical block contain the instruction register and the circuit necessary for controlling the register and µRAM and µPROM.
The OP register consist of two ports, a 9 bits latch and a 2 x 4 bits up/down counter. The input to the OP register is the 16 bits open collector I-BUS. The outputs from the register are the signals OP0 - OP15 and POP7.
I-BUS 0 OP8 which means that the OP register is swaped with regard to the I-BUS. The signal POP7 is the same as OP, but because of the different load time of for the latch and counter part, it has been

necessary to include the signal in the latch port also (POP7). The PROM used to decode the MDAT lines MDAT32-35 exist in two different versions, one for MPB with µRAM CR1266-1 and one for MPB without µRAM CR1266-2. The PROM tables are included in section 4.

Beside the OP code output from the L-OR-1 there is two signal for cotrolling of whether the MDAT is sourced from the RAM or the PROM EN RAM (H) & EN ROM (H). An additional output is used to enable loading of the I-BUS into the µRAM. The last output is the MAX/MIN (H) which indicate that an all zero or all one have been reached by one of the two four bits U/D counters. The timing diagram fig 3.4.1 below specify the signals more detailed.

OP Register Timing Diagram

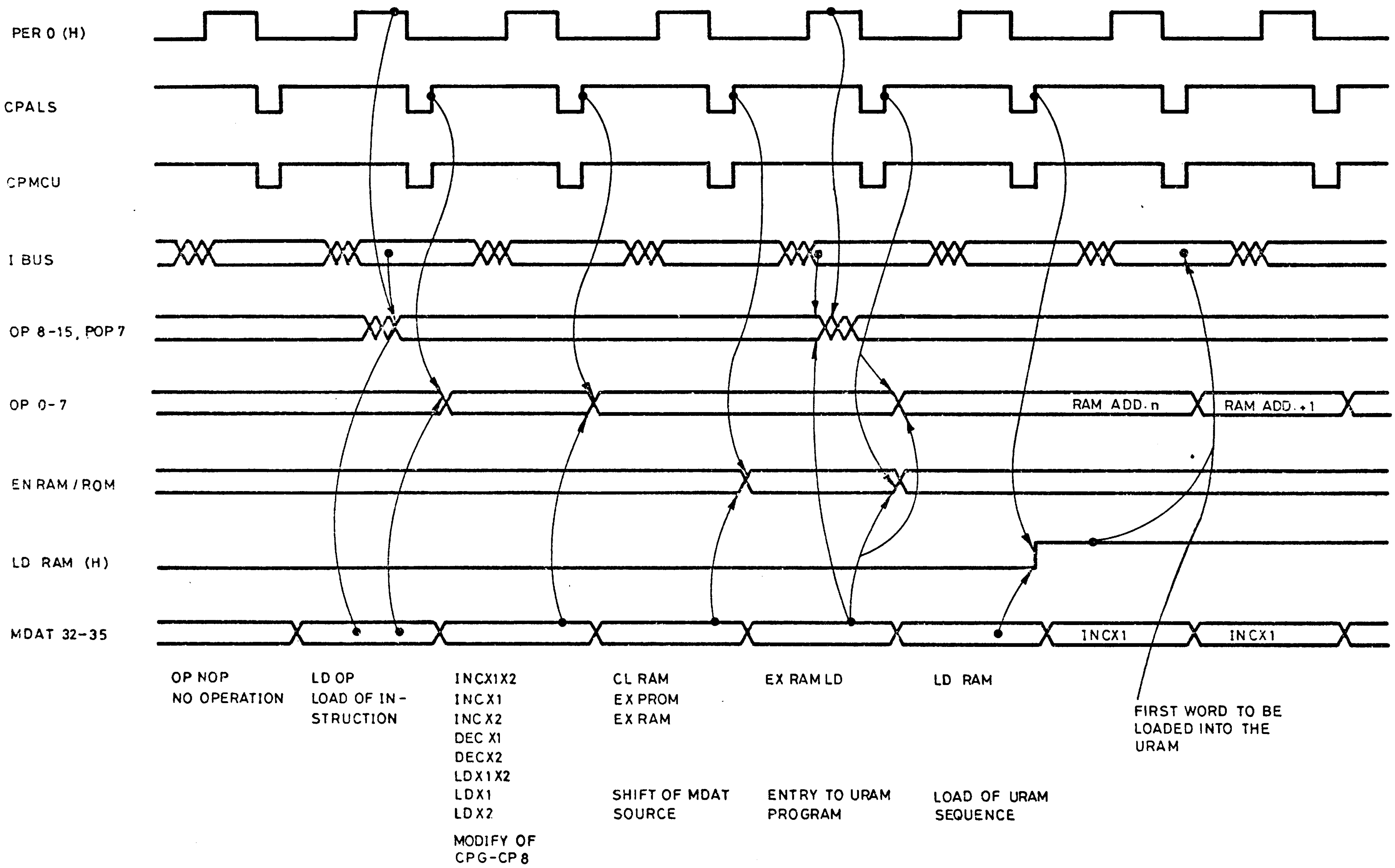


Fig. 3.4.1

3.4.2 OP Pre Decoding L-OPPD-1

This logical block consist of two 512 x 4 PROM's and two 4 x 2 to 1 selectors for controlling the input to the MCU secondary & primary instruction bus SX & PX.

PRE PROM 1 is the PROM which contain the instruction μ sequence to determining the μprogram entry (JZR). The signal DIS PRE (H) will force the output high if an interrupt is waiting for beeing serviced
The PRE PROM has the CR NO: CR1271 for the contents ref PROM tables section 4 .
Timing diagram fig 3.4.2 below shows the relations between the OP reg and the MPA.
The other PROM in the functional block is PROM 2 containing four tables for OP8 - 13.3, the tables are controlled by MDAT 14 & 15. The PROM has no. CR1270 and the contents is specified in section 4.

Fig 3.4.2

MICRO PROGRAM BOARD (MPB)	sign/date GB/780521	page
	repl	project

The function of the two MCU instruction bus selectors is specified in table below.

TABLE 4.3.2

MDAT 24	MDAT 25	PX3	PX2	PX1	PX0	SX3	SX2	SX1	SX0
0	0	OP7	OP6	OP5	OP4	OP7	OP6	OP5	OP4
0	1	OP7	OP6	OP5	OP4	PXP3	PXP2	PXP1	PXP0
1	0	PXP3	PXP2	PXP1	PXP0	OP7	OP6	OP5	OP4
1	1	PXP3	PXP2	PXP1	PXP0	PXP3	PXP2	PXP1	PXP0

PXPO - PXP3	are output from PROM 2
PXPU - PXP3	are determined by MDAT14 MDAT 15 & OP8 - 3.3.

When the signal LD MCU (H) is active the MCU instruction bus's are forced to all high and thereby determining the start address after a reset of the CPU.

As it is seen from the timing diagram, the latch part of the OP register can be used in the cycle where it is loaded, while the counter part first is valid in the following μ cycle.

3.4.3 Feed Back Selectors L-FBS-1

The L-FBS-1 consist of three selectors for controlling the 4 LS bits of the MCU function code AC0 -3.
The table below specify the different selection possibilities.

TABLE 3.4.3

MDAT8	MDAT10	MDAT13	MDAT12	MDAT11	MDAT9	AC3	AC2	$\overline{AC1}$	$\overline{AC0}$
1	0	0	0	0	0	MDAT15	MDAT14	"0"	"0"
1	1	0	0	0	0	"1"	"0"	"0"	"0"
0	1 0	0	0	0	0	MDAT15 R1.3	MDAT14 R1.4	R1.2	R1.1
0	1 0	0	0	0	1	MDAT15 R1.3	MDAT14 R1.4	OP9	OP8
0	1 0	0	0	1	0	MDAT15 R1.3	MDAT14 R1.4	TIMERINT(H)	CPUINT (H)
0	1 0	0	0	1	1	MDAT15 R1.3	MDAT14 R1.4	MDAT25	MDAT24
0	1 0	0	1	0	0	MDAT15 R1.3	MDAT14 R1.4	POP7	R1.1
0	1 0	0	1	0	1	MDAT15 R1.3	MDAT14 R1.4	MDAT25	OP8
0	1 0	0	1	1	0	MDAT15 R1.3	MDAT14 R1.4	MDAT25	CPUINT (H)
0	1 0	0	1	1	1	MDAT15 R1.3	MDAT14 R1.4	OP15	MDAT24
0	1 0	1	0	0	0	MDAT15 R1.3	MDAT14 R1.4	R1.2	OP3
0	1 0	1	0	0	1	MDAT15 R1.3	MDAT14 R1.4	OP9	OP14
0	1 0	1	0	1	0	MDAT15 R1.5	MDAT14 R1.4	TIMERINT(H)	MAX/MIN (H)
0	1 0	1	0	1	1	MDAT15 R1.3	MDAT14 R1.4	MDAT25	MODIFY(H)
0	1 0	1	1	0	0	MDAT15 R1.3	MDAT14 R1.4	POP7	OP3
0	1 0	1	1	0	1	MDAT15 R1.3	MDAT14 R1.4	MDAT25	OP14
0	1 0	1	1	1	0	MDAT15 R1.3	MDAT14 R1.4	MDAT25	MAX/MIN(H)
0	1 0	1	1	1	1	MDAT15 R1.3	MDAT14 R1.4	OP15	MODIFY (H)

R 1.1 - R 1.4 Pre PROM output.

3.4.4 Flag Control L-FC-1

The L-FC-1 supply the MCU with the flag test input FI. The circuit consist of a 256 x 4 PROM CR1269 ref section 4, and a 8 to 1 selector. The outputs from the PROM are used for control of the selector (3 bits) and the ALB for selecting the source for the ALB for the arithmetrics flags SEC, SEZ, SEO & SES, either the direct output from the ALU or the flags stored in PSW. The PROM table section 4 specify the relationship between the PROM input and the selector flag input FI.

Note: The flag input is not valid in the u cycles where the OP latch is loaded, meaning that the MCU function operating with the flag input is not allowed.

3.4.5 Micro Program Control Unit L-MCU-1

This logical block consist of one chip a intel 3001 MCU, and the description of it is covered on the following pages.

intel

SCHOTTKY BIPOLAR LSI MICROCOMPUTER SET

3001 MICROPROGRAM CONTROL UNIT

The INTEL Bipolar Microcomputer Set is a family of Schottky bipolar LSI circuits which simplify the construction of microprogrammed central processors and device controllers. These processors and controllers are truly microprogrammed in the sense that their control logic is organized around a separate read-only memory called the microprogram memory. Control signals for the various processing elements are generated by the microinstructions contained in the microprogram memory. In the implementation of a typical central processor, as shown below, the microprogram interprets a higher level of instructions called macroinstructions, similar to those found in a small computer. For device controllers, the microprograms directly implement the required control functions.

The INTEL 3001 Microprogram Control Unit (MCU) controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

Maintenance of the microprogram address register.

Selection of the next microinstruction based on the contents of the microprogram address register.

Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence.

Saving and testing of carry output data from the central processor (CP) array.

Control of carry/shift input data to the CP array.

Control of microprogram interrupts.

High Performance – 85 ns Cycle Time

TTL and DTL Compatible

Fully Buffered Three-State and Open Collector Outputs

Direct Addressing of Standard Bipolar PROM or ROM

512 Microinstruction Addressability

Advanced Organization
- **9-Bit Microprogram Address Register and Bus**
- **4-Bit Program Latch**
- **Two Flag Registers**

Eleven Address Control Functions
- **Three Jump and Test Latch Functions**
- **16-way Jump and Test Instruction Bus Function**

Eight Flag Control Functions
- **Four Flag Input Functions**
- **Four Flag Output Functions**

40 Pin DIP

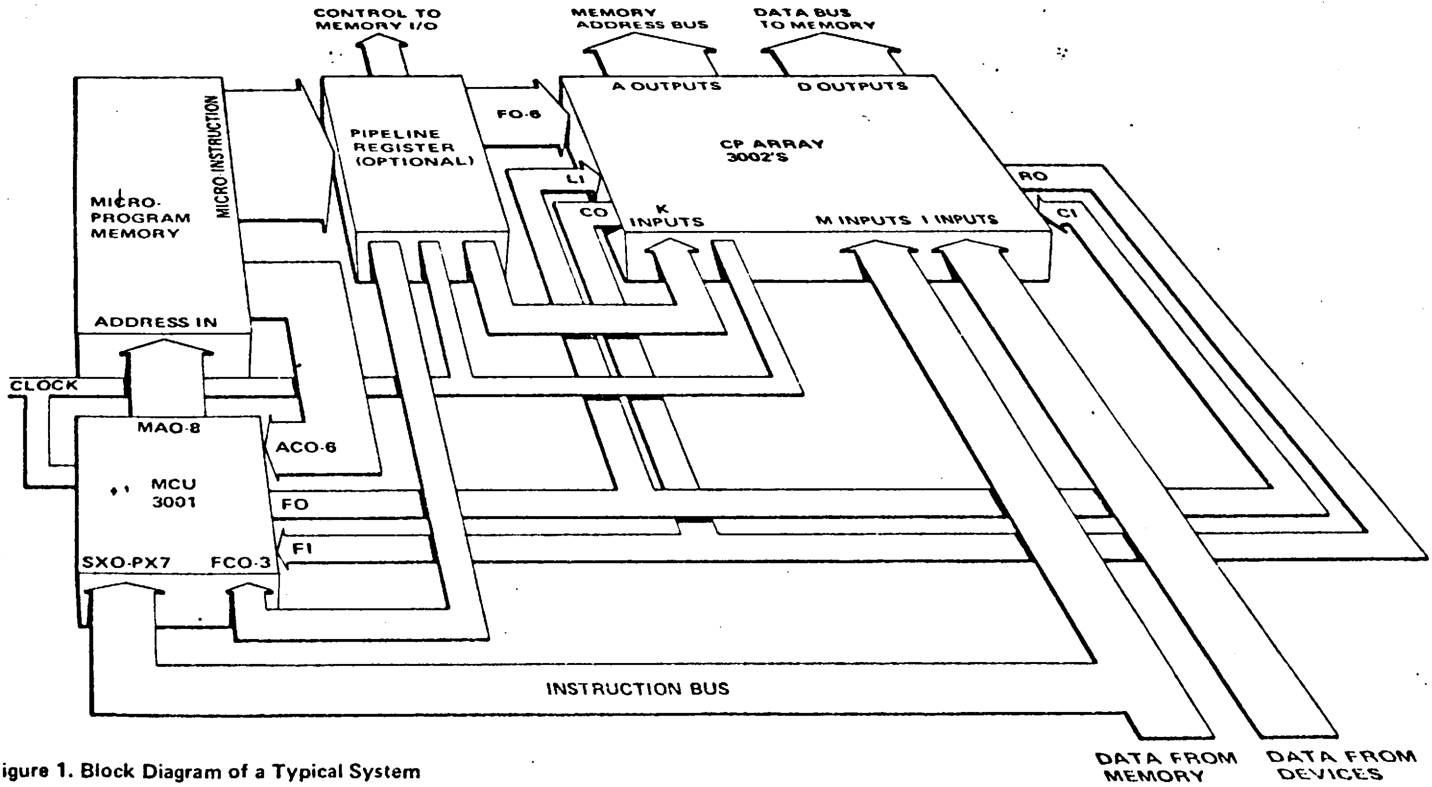


Figure 1. Block Diagram of a Typical System

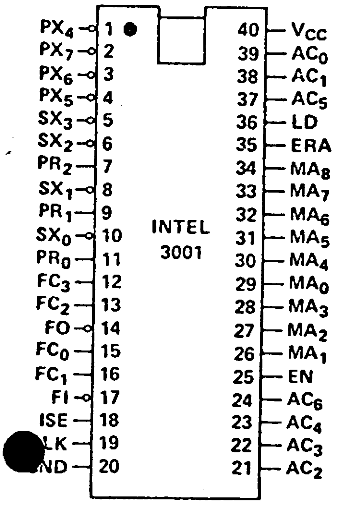
Other members of the INTEL Bipolar Microcomputer Set:

3002 Central Processing Element
3003 Look-Ahead Carry Generator
3212 Multi-Mode Latch Buffer
3214 Priority Interrupt Control Unit
3226 Inverting Bi-Directional Bus Driver
3301 Schottky Bipolar ROM (256 x 4)
3304A Schottky Bipolar ROM (512 x 8)
3601 Schottky Bipolar PROM (256 x 4)
3604 Schottky Bipolar PROM (512 x 8)

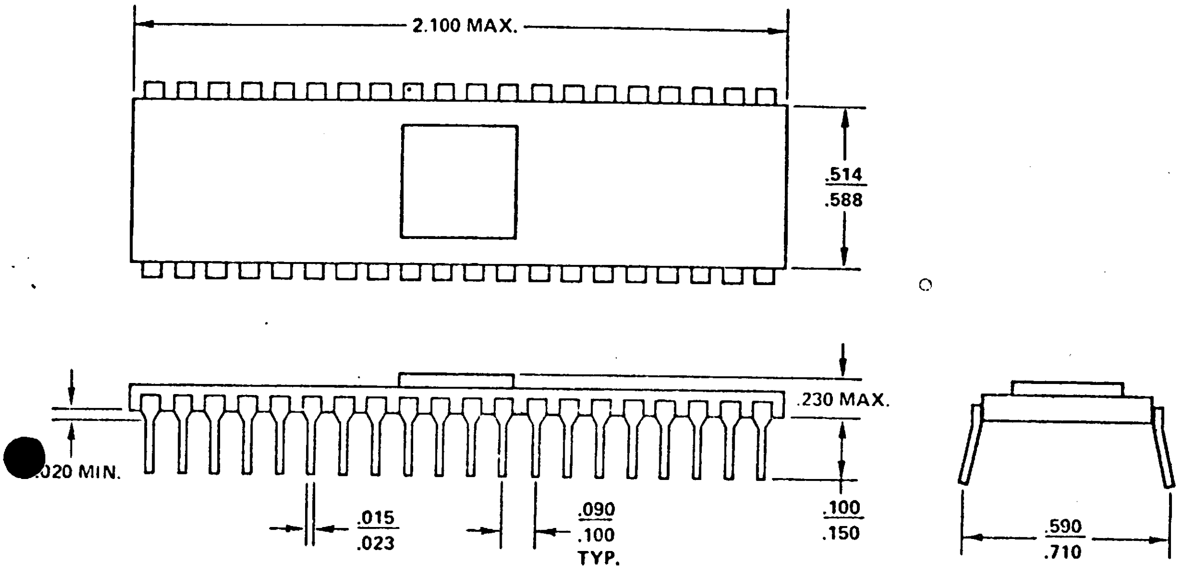
CONTENTS

APPENDICES

PACKAGE CONFIGURATION



PACKAGE OUTLINE



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1-4	PX_4-PX_7	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	active LOW
5, 6, 8, 10	SX_0-SX_3	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	active LOW
7, 9, 11	PR_0-PR_2	PR-Latch Outputs The PR-latch outputs are asynchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	open collector
12, 13, 15, 16	FC_0-FC_3	Flag Logic Control Inputs The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	
14	FO	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	active LOW three-state
17	FI	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: the flag input data is saved in the F-latch when the clock input (CLK) is low.	active LOW
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description, page 6). It can be used to provide the strobe signal required by the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits.	
19	CLK	Clock Input	
20	GND	Ground	
21-24 37-39	AC_0-AC_6	Next Address Control Function Inputs All jump functions are selected by these control lines.	
25	EN	Enable Input When in the HIGH state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26-29	MA_0-MA_3	Microprogram Column Address Outputs	three-state
30-34	MA_4-MA_8	Microprogram Row Address Outputs	three-state
35	ERA	Enable Row Address Input When in the LOW state, the enable row address input independently disables the microprogram row address outputs. It can be used with the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits to facilitate the implementation of priority interrupt systems.	
36	LD	Microprogram Address Load Input When in the active HIGH state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction busses into the microprogram register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	
40	VCC	+5 Volt Supply	

NOTE:

[1] Active HIGH unless otherwise specified.

LOGICAL DESCRIPTION

The MCU performs two major control functions. First, it controls the sequence in which microinstructions are fetched from the microprogram memory. For this purpose, the MCU contains a microprogram address register and the associated logic for selecting the next microinstruction address. The second function of the MCU is the control of the two flag flip-flops that are included for interaction with the carry input and carry output logic of the CP array. The logical organization of the MCU is shown in Figure 2.

NEXT ADDRESS LOGIC

The next address logic of the MCU provides a set of conditional and unconditional address control functions. These address control functions are used to implement a jump or jump/test operation as part of every microinstruction. That is to say, each microinstruction typically contains a jump operation field that specifies the address control function, and hence, the next microprogram address.

In order to minimize the pin count of the MCU, and reduce the complexity of the next address logic, the microprogram address space is organized as a two dimensional array or matrix. Each microprogram address corresponds to a unit of the matrix at a particular row and column location. Thus, the 9-bit microprogram address is treated as specifying not one, but two addresses — the row address in the upper five bits and the column address in the lower four bits. The address matrix can therefore contain, at most, 32 row addresses and 16 column addresses for a total of 512 microinstructions.

The next address logic of the MCU makes extensive use of this two component addressing scheme. For example, from a particular row or column address, it is possible to jump unconditionally in one operation anywhere in that row or column. It is not possible, however, to jump anywhere in the address matrix. In fact, for a given location in the matrix, there is a fixed subset of microprogram addresses that may be selected as the next address. These possible jump target addresses are referred to as a jump set. Each type of MCU address control (jump) function has a jump set associated with it. Appendix C illustrates the jump set for each function.

FLAG LOGIC

The flag logic of the MCU provides a set of functions for saving the current value of the carry output of the CP array and for controlling the value of the carry input to the CP array. These two distinct flag control functions are called flag input functions and flag output functions.

The flag logic is comprised of two flip-flops, designated the C-flag and the Z-flag, along with a simple latch, called the F-latch, that indicates the current state of the carry output line of the CP array. The flag logic is used in conjunction with the carry and shift logic of the CP array to implement a variety of shift/rotate and arithmetic functions.

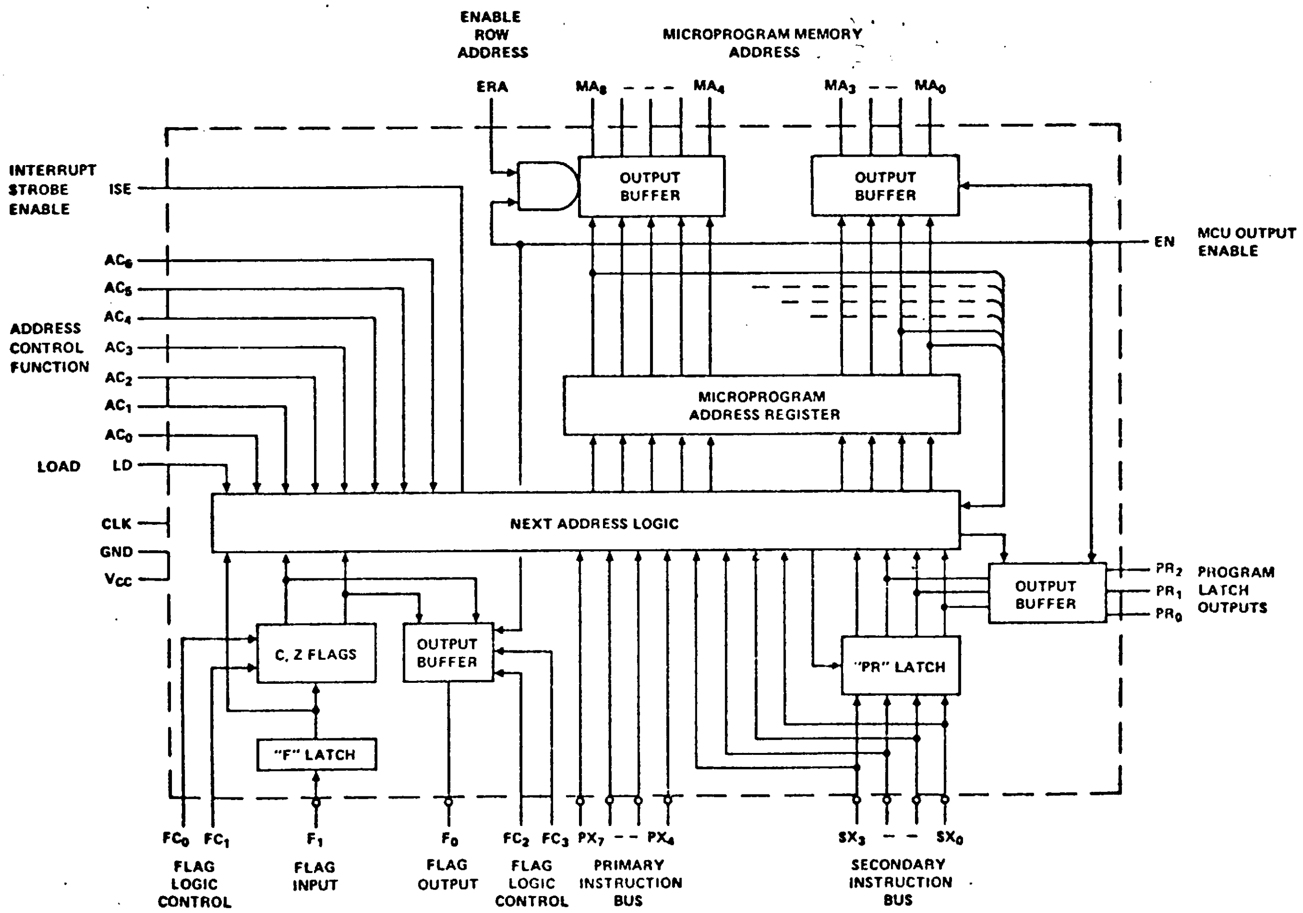


Figure 2. 3001 Block Diagram

ADDRESS CONTROL FUNCTIONS

The address control functions of the MCU are selected by the seven input lines designated AC_0-AC_6. On the rising edge of the clock, the 9-bit microprogram address generated by the next address logic is loaded into the microprogram address register. The next microprogram address is delivered to the microprogram memory via the nine output lines designated MA_0-MA_8. The microprogram address outputs are organized into row and column addresses as:

$$\underline{MA_8\ MA_7\ MA_6\ MA_5\ MA_4}$$

row address

$$\underline{MA_3\ MA_2\ MA_1\ MA_0}$$

column address

Each address control function is specified by a unique encoding of the data on [illegible] function input lines. From three to five bits of the data specify the particular function while the remaining bits are used to select part of either the row or column address desired. Function code formats are given in Appendix A, "Address Control Function Summary."

The following is a detailed description of each of the eleven address control functions. The symbols shown below are used throughout the description to specify row and column addresses.

Symbol	Meaning
row_n	5-bit next row address where n is the decimal row address.
col_n	4-bit next column address where n is the decimal column address.

UNCONDITIONAL ADDRESS CONTROL (JUMP) FUNCTIONS

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs to generate the next microprogram address.

Mnemonic Function Description

JCC Jump in current column. AC_0-AC_4 are used to select 1 of 32 row addresses in the current column, specified by MA_0-MA_3, as the next address

JZR Jump to zero row. AC_0-AC_3 are used to select 1 of 16 column addresses in row_0, as the next address.

JCR Jump in current row. AC_0-AC_3 are used to select 1 of 16 addresses in the current row, specified by MA_4-MA_8, as the next address.

JCE Jump in current column/row group and enable PR-latch outputs. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7-MA_8, as the next row address. The current column is specified by MA_0-MA_3. The PR-latch outputs are asynchronously enabled.

FLAG CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

Mnemonic Function Description

JFL Jump/test F-Latch. AC_0-AC_3 are used to select 1 of 16 row addresses in the current row group, specified by MA_8, as the next row address. If the current column group, specified by MA_3, is col_0-col_7, the F-latch is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the F-latch is used to select col_{10} or col_{11} as the next column address.

JCF Jump/test C-flag. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. If the current column group specified by MA_3 is col_0-col_7, the C-flag is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the C-flag is used to select col_{10} or col_{11} as the next column address.

JZF Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.

PX-BUS AND PR-LATCH CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The PX-bus jump/test function uses the data on the primary instruction bus (PX_4-PX_7), the current mircoprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

Mnemonic Function Description

JPR Jump/test PR-latch. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. The four PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.

Mnemonic Function Description

JLL Jump/test leftmost PR-latch bits. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_2 and PR_3 are used to select 1 of 4 possible column addresses in col_4 through col_7 as the next column address.

JRL Jump/test rightmost PR-latch bits. AC_0 and AC_1 are used to select 1 of 4 high-order row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_0 and PR_1 are used to select 1 of 4 possible column addresses in col_{12} through col_{15} as the next column address.

JPX Jump/test PX-bus and load PR-latch. AC_0 and AC_1 are used to select 1 of 4 row addresses in the current row group, specified by MA_6-MA_8, as the next row address. PX_4-PX_7 are used to select 1 of 16 possible column addresses as the next column address. SX_0-SX_3 data is locked in the PR-latch at the rising edge of the clock.

FLAG CONTROL FUNCTIONS

The flag control functions of the MCU are selected by the four input lines designated FC_0-FC_3. Function code formats are given in Appendix B, "Flag Control Function Summary."

The following is a detailed description of each of the eight flag control functions.

FLAG INPUT CONTROL FUNCTIONS

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line. Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Mnemonic	Function Description
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTIONS

The flag output control functions select the value to which the flag output (FO) line will be forced.

Mnemonic	Function Description
FF0	Force FO to 0. FO is forced to the value of logical 0.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

LOAD AND INTERRUPT STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active HIGH at the rising edge of the clock, the data on the primary and secondary instruction busses, PX_4-PX_7 and SX_0-SX_3, is loaded into the microprogram address register. PX_4-PX_7 are loaded into MA_0-MA_3 and SX_0-SX_3 are loaded into MA_4-MA_7. The high-order bit of the microprogram address register MA_8 is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

The interrupt strobe enable of the MCU is available on the output line designated ISE. The line is placed in the active high state whenever a JZR to col_{15} is selected as the address control function. Customarily, the start of a macroinstruction fetch sequence is situated at row_0 and col_{15} so that the INTEL 3214 Priority Interrupt Control Unit may be enabled at the beginning of the fetch/execute cycle. The priority interrupt control unit may respond to the interrupt by pulling the enable row address (ERA) input line down to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC_0-AC_6. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +160°C
All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to 70°C

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		−0.8	−1.0	V	$V_{CC} = 4.75V, I_C = -5$ mA
I_F	Input Load Current:					
	CLK Input		−0.075	−0.75	mA	$V_{CC} = 5.25V, V_F = 0.45V$
	EN Input		−0.05	−0.50	mA	
	All Other Inputs		−0.025	−0.25	mA	
I_R	Input Leakage Current:					
	CLK			120	μA	$V_{CC} = 5.25V, V_R = 5.25V$
	EN Input			80	μA	
	All Other Inputs			40	μA	
V_{IL}	Input Low Voltage			0.8	V	$V_{CC} = 5.0V$
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current		170	240	mA	$V_{CC} = 5.25V$[2]
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	$V_{CC} = 4.75V, I_{OL} = 10$ mA
V_{OH}	Output High Voltage (MA_0-MA_8, ISE, FO)	2.4	3.0		V	$V_{CC} = 4.75V, I_{OH} = -1$ mA
I_{OS}	Output Short Circuit Current (MA_0-MA_8, ISE, FO)	−15	−28	−60	mA	$V_{CC} = 5.0V$
$I_{O(off)}$	Off-State Output Current:					
	PR_0-PR_2, MA_0-MA_2, FO			−100	μA	$V_{CC} = 5.25V, V_O = 0.45V$
	MA_0-MA_8, FO			100	μA	$V_{CC} = 5.25V, V_O = 5.25V$

NOTES:
[1] Typical values are for T_A = 25°C and nominal supply voltage.
[2] EN input grounded, all other inputs and outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%

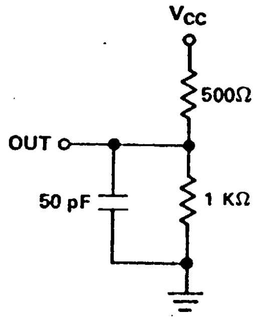
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT
t_{CY}	Cycle Time	85	60		ns
t_{WP}	Clock Pulse Width	30	20		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC_0-AC_6	10	0		ns
t_{SK}	FC_0, FC_1	0			ns
t_{SX}	SX_0-SX_3, PX_4-PX_7	35	25		ns
t_{SI}	FI	15	5		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC_0-AC_6	5	0		ns
t_{HK}	FC_0, FC_1	0			ns
t_{HX}	SX_0-SX_3, PX_4-PX_7	20	5		ns
t_{HI}	FI	20	8		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA_0-MA_8, FO)		30	45	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		16	30	ns
t_{FO}	Propagation Delay from Control Inputs AC_0-AC_6 to Latch Outputs (PR_0-PR_2)		26	40	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA_0-MA_8, FO, PR_0-PR_2)		21	32	ns
t_{FI}	Propagation Delay from Control Inputs AC_0-AC_6 to Interrupt Strobe Enable Output (ISE)		24	40	ns

NOTE:
[1] Typical values are for T_A = 25°C and nominal supply voltage.

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 10 mA and 50 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:

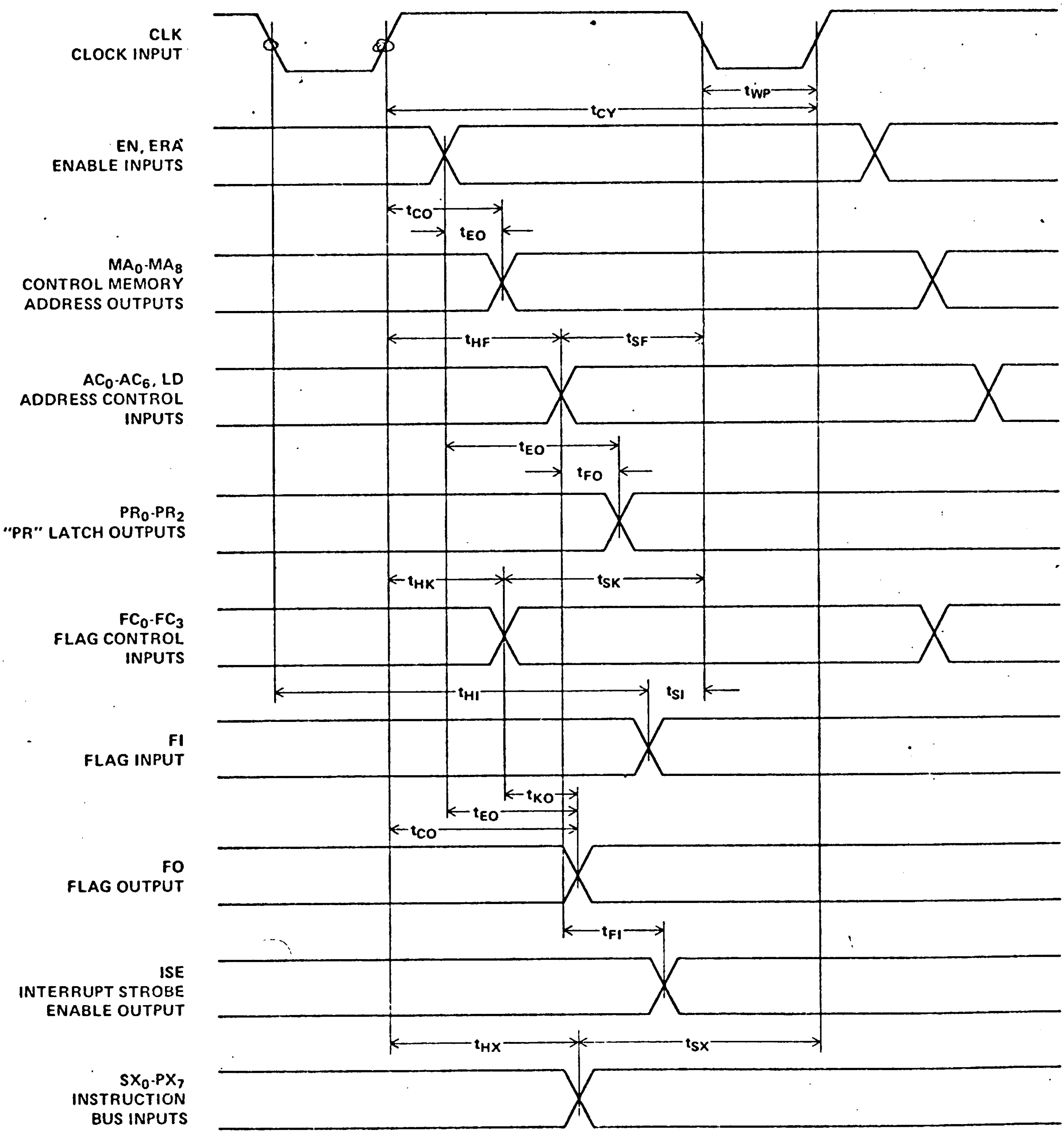


CAPACITANCE[2] T_A = 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance:				
	CLK, EN		11	16	pF
	All Other Inputs		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

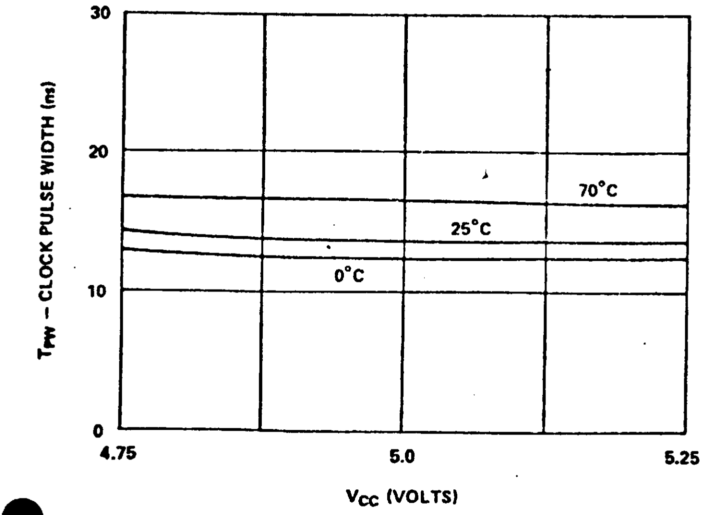
NOTE:
[2] This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V and T_A = 25°C.

3001 WAVEFORMS

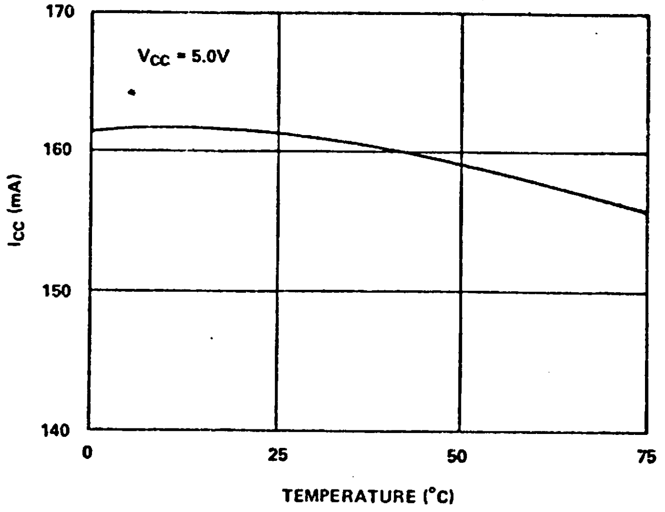


TYPICAL AC AND DC CHARACTERISTICS

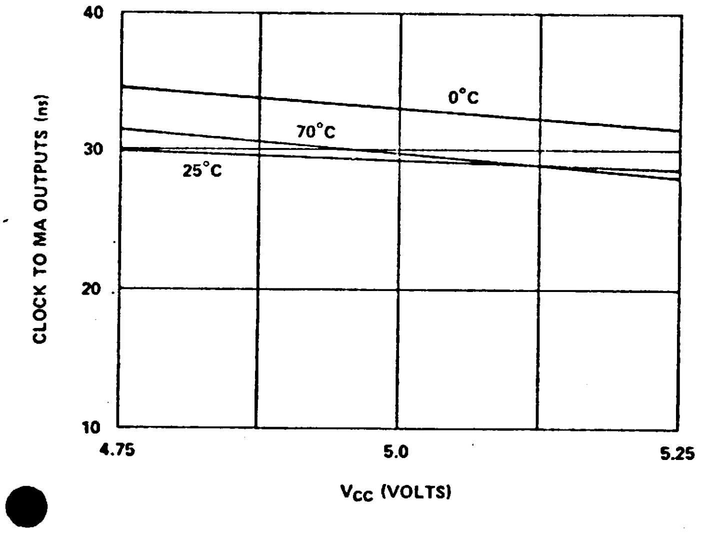
Clock Pulse Width vs V_{CC} and Temperature



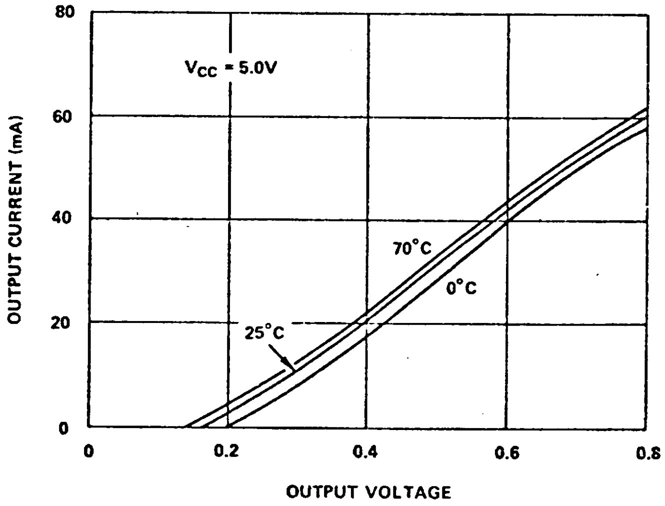
I_{CC} vs Temperature



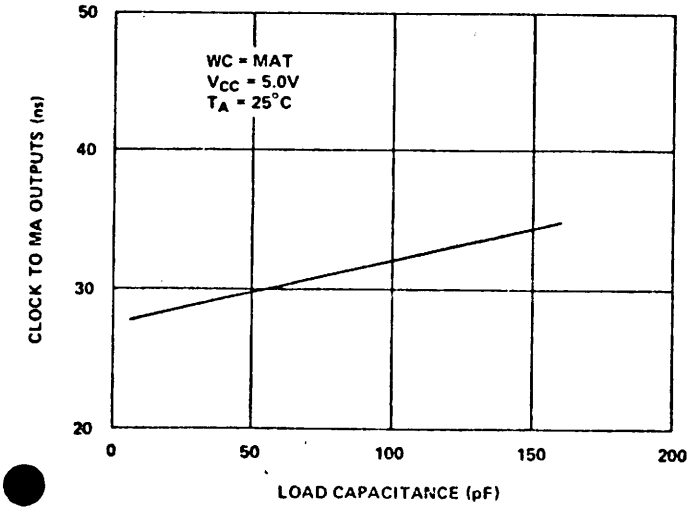
Clock to MA Outputs vs V_{CC} and Temperature



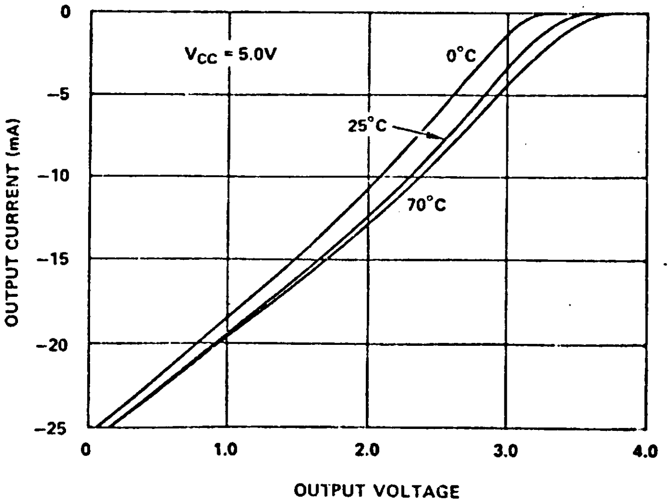
Output Current vs Output Low Voltage



Clock to MA Outputs vs Load Capacitance



Output Current vs Output High Voltage



MNEMONIC	DESCRIPTION	FUNCTION							NEXT ROW					NEXT COL			
		AC_6	5	4	3	2	1	0	MA_8	7	6	5	4	MA_3	2	1	0
JCC	Jump in current column	0	0	d_4	d_3	d_2	d_1	d_0	d_4	d_3	d_2	d_1	d_0	m_3	m_2	m_1	m_0
J[illegible]	Jump to zero row	0	1	0	d_3	d_2	d_1	d_0	0	0	0	0	0	d_3	d_2	d_1	d_0
JCR	Jump in current row	0	1	1	d_3	d_2	d_1	d_0	m_8	m_7	m_6	m_5	m_4	d_3	d_2	d_1	d_0
JCE	Jump in column/enable	1	1	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JFL	Jump/test F-latch	1	0	0	d_3	d_2	d_1	d_0	m_8	d_3	d_2	d_1	d_0	m_3	0	1	f
JCF	Jump/test C-flag	1	0	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	c
JZF	Jump/test Z-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	z
JPR	Jump/test PR-latches	1	1	0	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	p_3	p_2	p_1	p_0
JLL	Jump/test left PR bits	1	1	0	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	0	1	p_3	p_2
JRL	Jump/test right PR bits	1	1	1	1	1	d_1	d_0	m_8	m_7	1	d_1	d_0	1	1	p_1	p_0
JPX	Jump/test PX-bus	1	1	1	1	0	d_1	d_0	m_8	m_7	m_6	d_1	d_0	x_7	x_6	x_5	x_4

SYMBOL	MEANING
d_n	Data on address control line n
m_n	Data in microprogram address register bit n
p_n	Data in PR-latch bit n
x_n	Data on PX-bus line n (active LOW)
f, c, z	Contents of F-latch, C-flag, or Z-flag, respectively

APPENDIX B FLAG CONTROL FUNCTION SUMMARY

TYPE	MNEMONIC	DESCRIPTION	FC_1	0
Flag Input	SCZ	Set C-flag and Z-flag to f	0	0
	STZ	Set Z-flag to f	0	1
	STC	Set C-flag to f	1	0
	HCZ	Hold C-flag and Z-flag	1	1

TYPE	MNEMONIC	DESCRIPTION	FC_3	2
Flag Output	FF0	Force FO to 0	0	0
	FFC	Force FO to C-flag	0	1
	FFZ	Force FO to Z-flag	1	0
	FF1	Force FO to 1	1	1

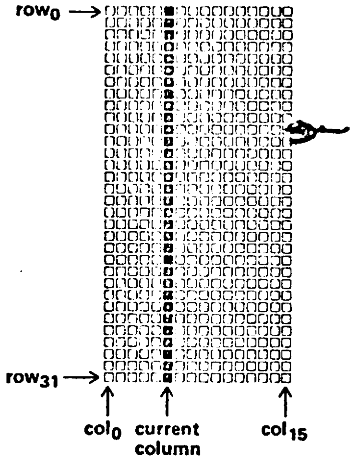
LOAD FUNCTION	NEXT ROW					NEXT COL			
LD	MA_8	7	6	5	4	MA_3	2	1	0
0	see Appendix A					see Appendix A			
1	0	x_3	x_2	x_1	x_0	x_7	x_6	x_5	x_4

SYMBOL	MEANING
f	Contents of the F-latch
x_n	Data on PX- or SX-bus line n (active LOW)

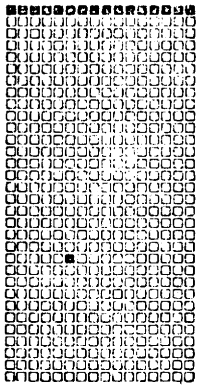
APPENDIX C JUMP SET DIAGRAMS

The following ten diagrams illustrate the jump set for each of the eleven jump and jump/test functions of the MCU. Location 341, indicated by the black square, represents one current row (row_{21}) and current column (col_5) address. The blue boxes indicate the microprogram locations that may be selected by the particular function as the next address.

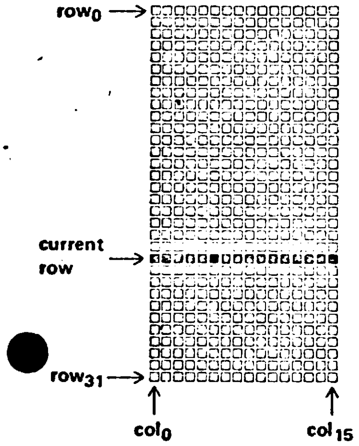
JCC
Jump in Current Column



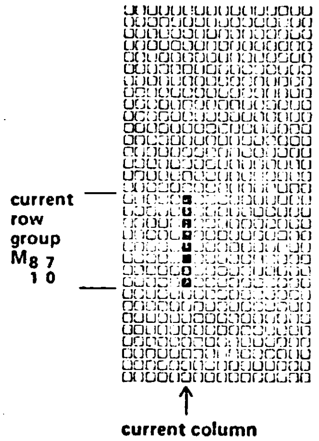
JZR
Jump to Zero Row



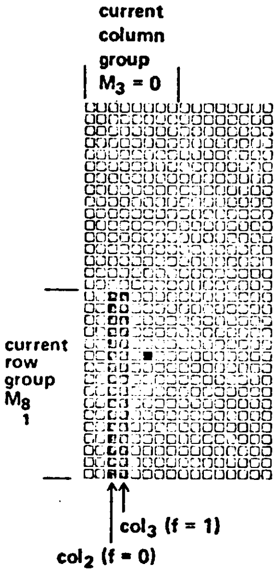
JCR
Jump in Current Row



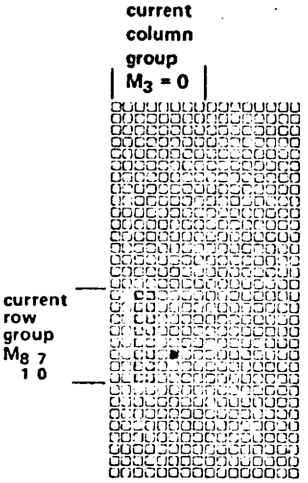
JCE
Jump Column/Enable



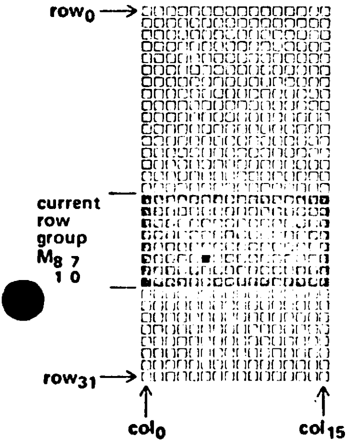
JFL
Jump/Test F-Latch



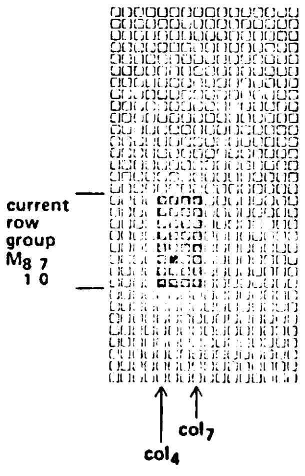
JCF, JZF
Jump/Test C-Flag
Jump/Test Z-Flag



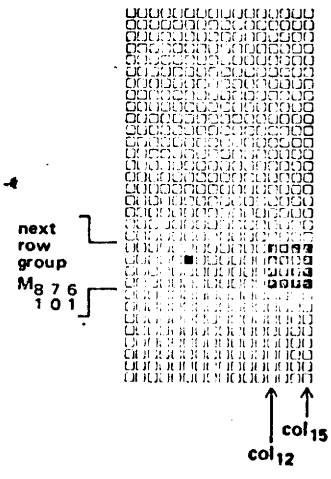
JPR
Jump/Test PR-Latch



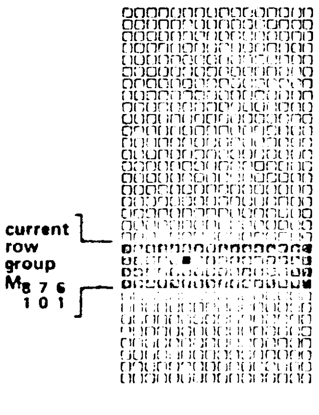
JLL
Jump/Test Left Latch

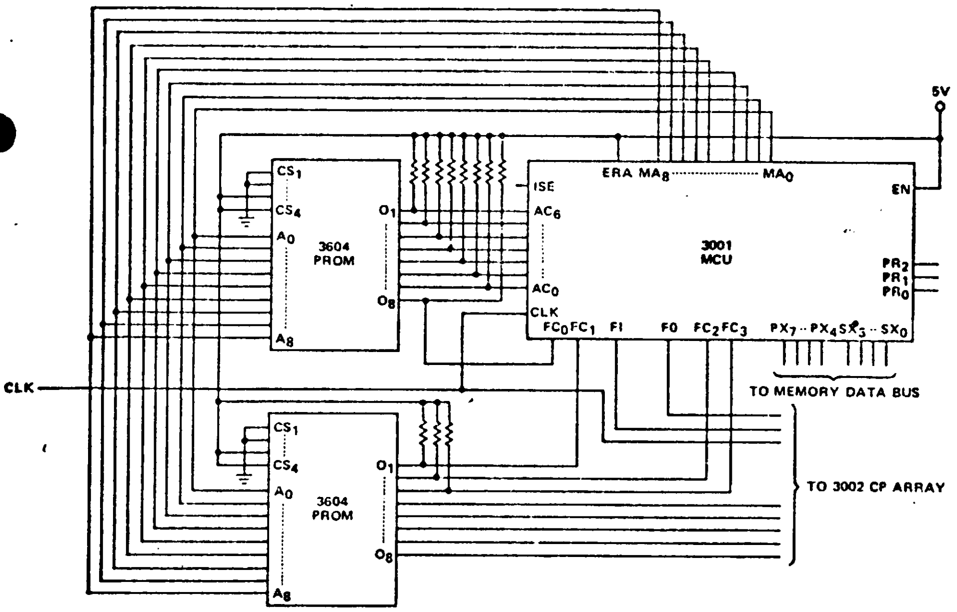


JRL
Jump/Test Right Latch

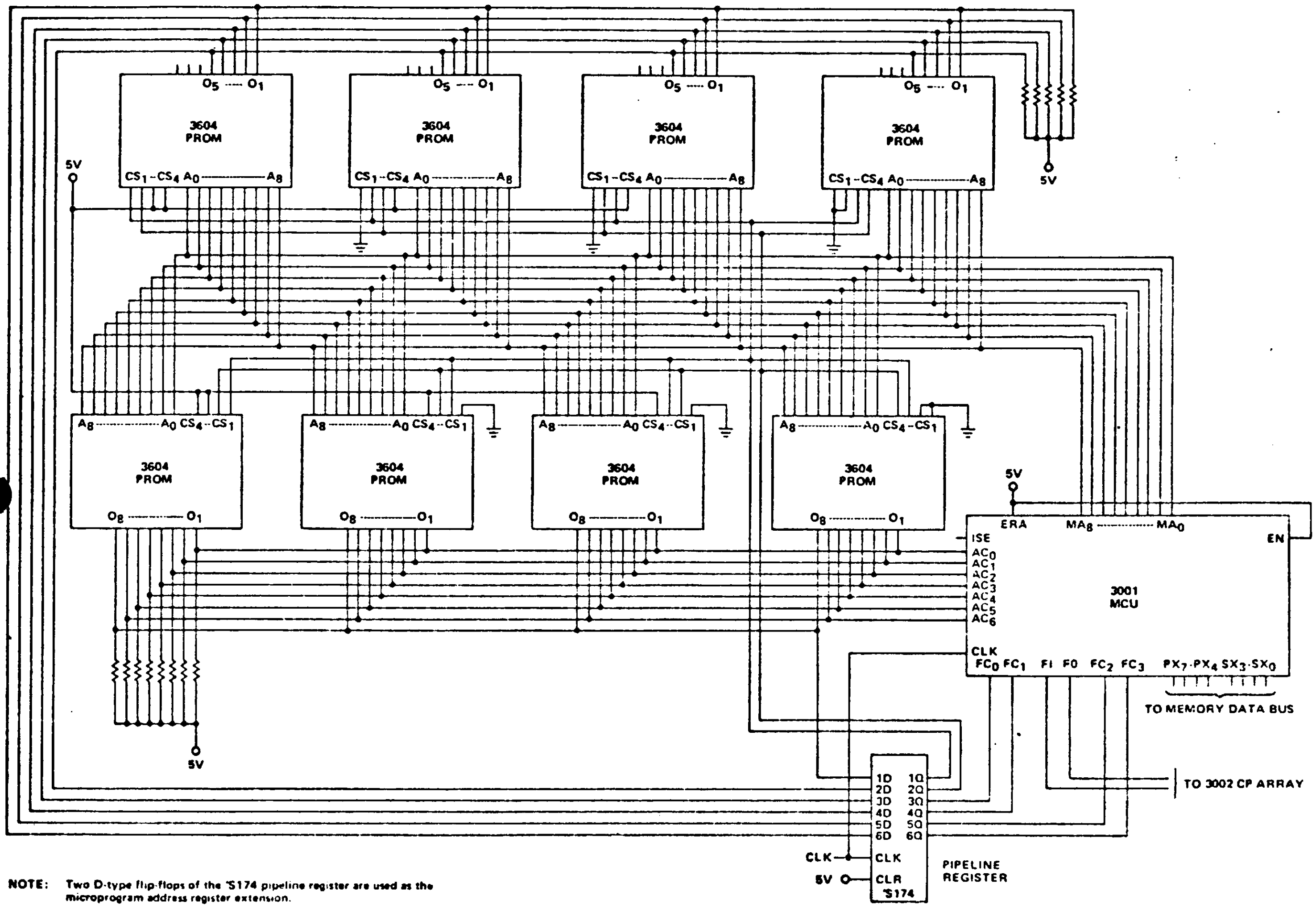


JPX
Jump/Test PX-Bus





Non-Pipelined Configuration with 512 Microinstruction Addressability



NOTE: Two D-type flip-flops of the 'S174 pipeline register are used as the microprogram address register extension.

Pipelined Configuration with 2048 Microinstruction Addressability

intel

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3065 Bowers Avenue
Santa Clara, California 95051
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TELEX: 34-6372

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Orient:
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TELEX: 781-28426

NOTE: This is a preliminary specification
and is subject to revision without notice.

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3.5 Micro PROM F-MP-1

The F-MP-1 consist of two logical blocks:

1. Micro ROM L-MROM-1

2. JZR Decoding L-JZRD-1

3.5.1 Micro ROM L-MROM-1

The micro program for the CPU is contained in the 512 + 48 bits from area (CR1272-CR1283), the actual contents is specified in section 5 PROM tables.
The memory area is build by 12pcs. 512 x 4, 3-state proms with an access time < 60ns. The input to the memory area is the MPA signal and the output is the 48 MDAT lines the functions of the output signals are specified in section 3.3.
The 3 - state outputs are connected together with the corresponding outputs from the μRAM and controlled by the signal EN ROM (H) from the OP register.

3.5.2 JZR Decoding L-JZRD-1

This logical block generate a high output JZR (H) when the MCU function code MDAT 37-39 is a JZR.

$$\text{JZR (H)} = \text{MDAT 37} \times \overline{\text{MDAT38}} \times \overline{\text{MDAT39}}$$

The signal is used for enabling of interrupt when the first step in the instruction decoding is performed.

3.6 Micro Program RAM F-MPRAM-1

This functional block contain the circuit used for controlling of loading and execution of the optional µRAM program. A 3-state buffer is included for termination of the output signals (MDAT) to the micro PROM output. The F-MPROM-1 includes the following three logic blocks:

1. RAM Address Selector	L-RAS-1
2. RAM Memory	L-RM-1
3. RAM Buffer	L-RB-1

3.6.1 RAM Address Selector L-RAS-1

The L-RAS-1 selects the RAM address from two different sources when the RAM is loaded or executed.
During the load sequence the address is selectded from the OP register OP0 - 5 and OP6, OP7 are used to select one of the 3 RAM sections to be loaded from the I-BUS. When in the execution mode the RAM address is the least significants bits of the micro program address MPA0-5. The selection of the address source is carried out by the signal EN RAM (H) so that source is the OP code when the µPROM is executed. Timing Diagram fig. 3.6.1 specify the function of the block and table 3.6 specify the relationship between the address input and the RAM output.

3.6.2 RAM Memory L-RM-1

The RAM memory is build by 6 PC 64 x 9 bit chips but only 8 of the inverted open collector output are used. Because the output is OC 1K pull up is included for each signal. The chip used has an access time 35 ns. The addressing and input/output relations is specified in.table 3.6.

RAM Address Selector Timing Diagram

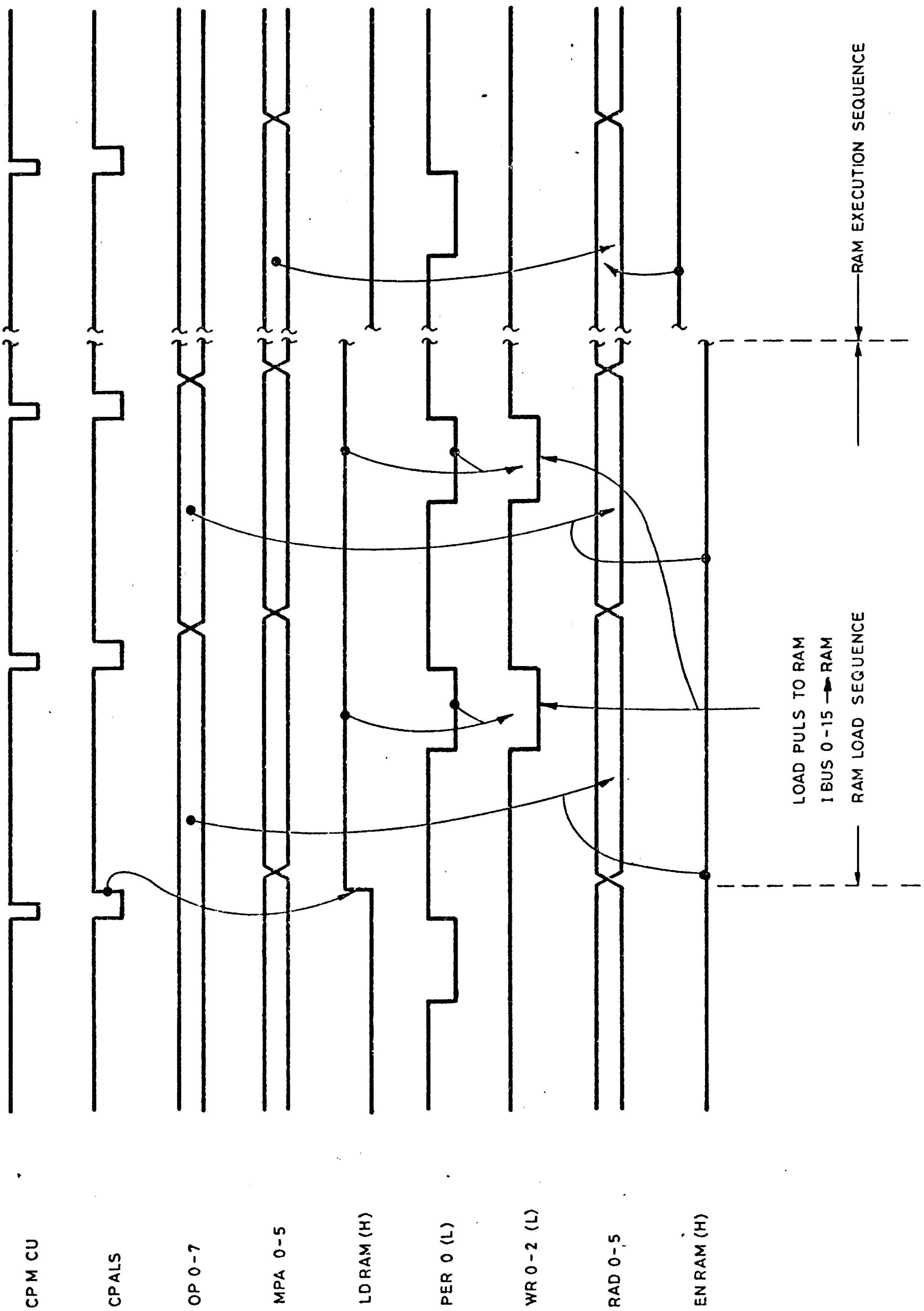
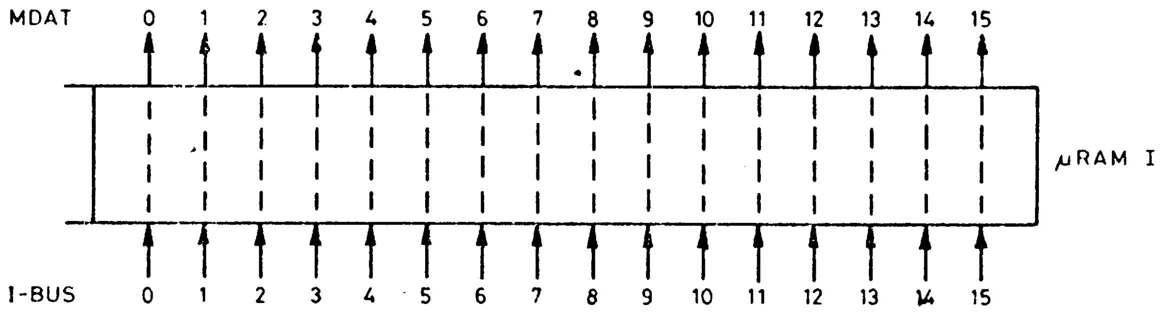
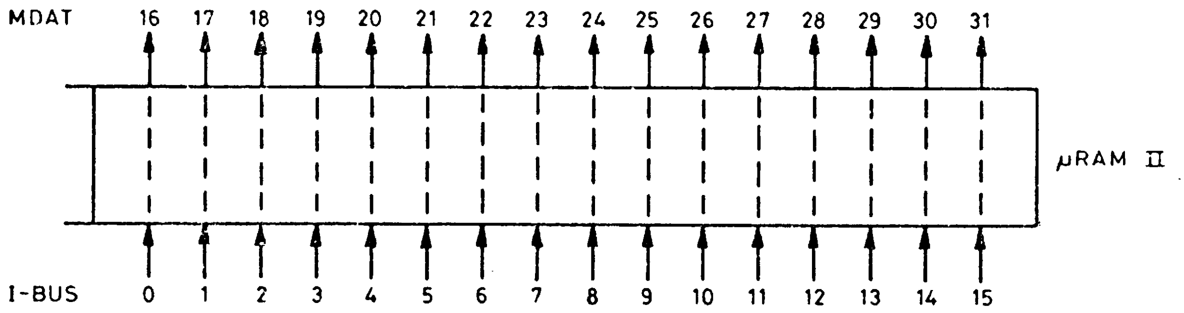


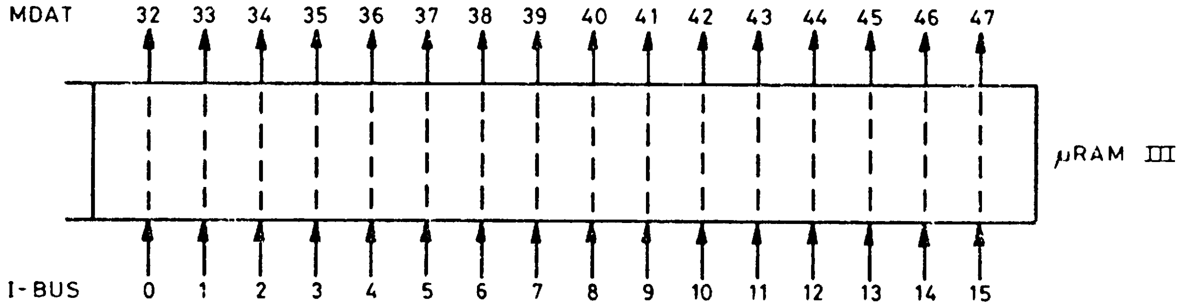
Fig. 3.6.1

TABLE 3.6

µ RAM







µ RAM LOAD

OP7	OP6	µ RAM
0	0	I
1	0	II
0	1	III

µ RAM ADDRESSING

Addr. bit	Read	Load
2^0	MPA0	OP0
2^1	MPA1	OP1
2^2	MPA2	OP2
2^3	MPA3	OP3
2^4	MPA4	OP4
2^5	MPA5	OP5

3.6.3 RAM Buffer L-RB-1

The function of L-RB-1 is to terminate the open collector RAM output to the 3-state MDAT lines. The output is enabled when the signal EN RAM (L) is active.

3.7 Mask & Address Control F- M&AC-1

By this functional blocks the ALU A & B address and the I-BUS mask is generated. The F-M & AC-1 is build of two logical blocks.

1. A and B Address Selector L-ABAS-1

2. Mask Control L-MC-1

3.7.1 A and B Address Selector L-ABAS-1

Five selector chips are used for selecting the A & B address source to the ALU register file. The addresses can either be selected from the OP register or direct from the µprogram output MDAT. Control of which source to be selected is carried by four MDAT signals; for A address MDAT 29 & 30 and for B address MDAT 41 & 42. Tables 3.7.1 a & b specify the signals.
Note: That the MDAT used for A address are used for mask control too.

3.7.2 Mask Control L-MC-1

The mask control circuit is used for masking of the contents on the open collector I-BUS, the L-MC-1 can generate to types of maskes either a bit mask or a long mask. In the bit mask mode the mask PROM's will force all the I-BUS lines except one (bit pointer) to zero. In the long mask mode the PROM's all the I-BUS lines above the bit pointer to zero. The PROM tables are included in section 4.

K

The table 3.7.2 specify the mask function and the signal used for mask generation. Note that the MDAT lines except MDAT 46 are used for ALU A addressing too.

For synchronication of the mask circuit to the I-BUS two 3 - state selectors are coupled together to give a combined latch and selector function, and the mask enable, mask type and mask source signals are stored in a latch.

The timing diagram fig. 3.7.2 define the timing for the circuit.

ALU Register Addressing:

A address & shift control:
MDAT 26 - 31, 47

TABLE 3.7.1.a

A. ADDRESS SELECT			A. ADDRESS & SHIFT CONT.			
MDAT 47	MDAT 30	MDAT 29	AA3	AA2	AA1	AA0
Ø	0	0	MDAT 26	MDAT 27	MDAT 31	MDAT 2
Ø	0	1	"0"	OP10	OP9	OP8
Ø	1	0	"0"	"1"	OP7	OP6
0	1	1	"0"	OP2	OP1	OP0
1	1	1	"0"	OP6	OP5	OP4

B address:
MDAT 40 - 45, 47

TABLE 3.7.1.b

B. ADDRESS SELECT			B. ADDRESS			
MDAT 47	MDAT 42	MDAT 41	BA3	BA2	BA1	BA0
Ø	0	0	MDAT 43	MDAT 40	MDAT 45	MDAT 44
Ø	0	1	"0"	OP10	OP9	OP8
0	1	0	OP3	OP2	OP1	OP0
1	1	0	OP7	OP6	OP5	OP4
0	1	1	"0"	OP2	OP1	OP0
1	1	1	"0"	OP6	OP5	OP4

K

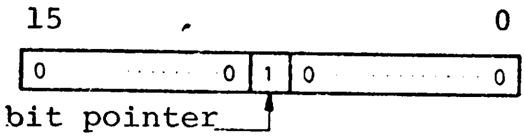
TABLE 3.7.2

MASK CONTROL

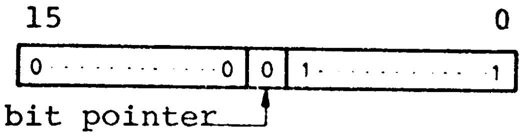
MDAT 26 - 31, 46 OP0 - 3.

MDAT			BIT POINTER				MASK TYPE
46	29	30	2^3	2^2	2^1	2^0	
1	0	0	0	0	0	0	MASK DISABLED
0	0	0	OP3	OP2	OP1	OP0	LONG MASK
0	0	1	MDAT 26	MDAT 27	MDAT 31	MDAT 28	LONG MASK
0	1	0	OP3	OP2	OP1	OP0	BIT MASK
0	1	1	MDAT 26	MDAT 27	MDAT 31	MDAT 28	BIT MASK

Bit Mask, I-BUS



Long Mask, I-BUS



Mask Control Timing Diagram

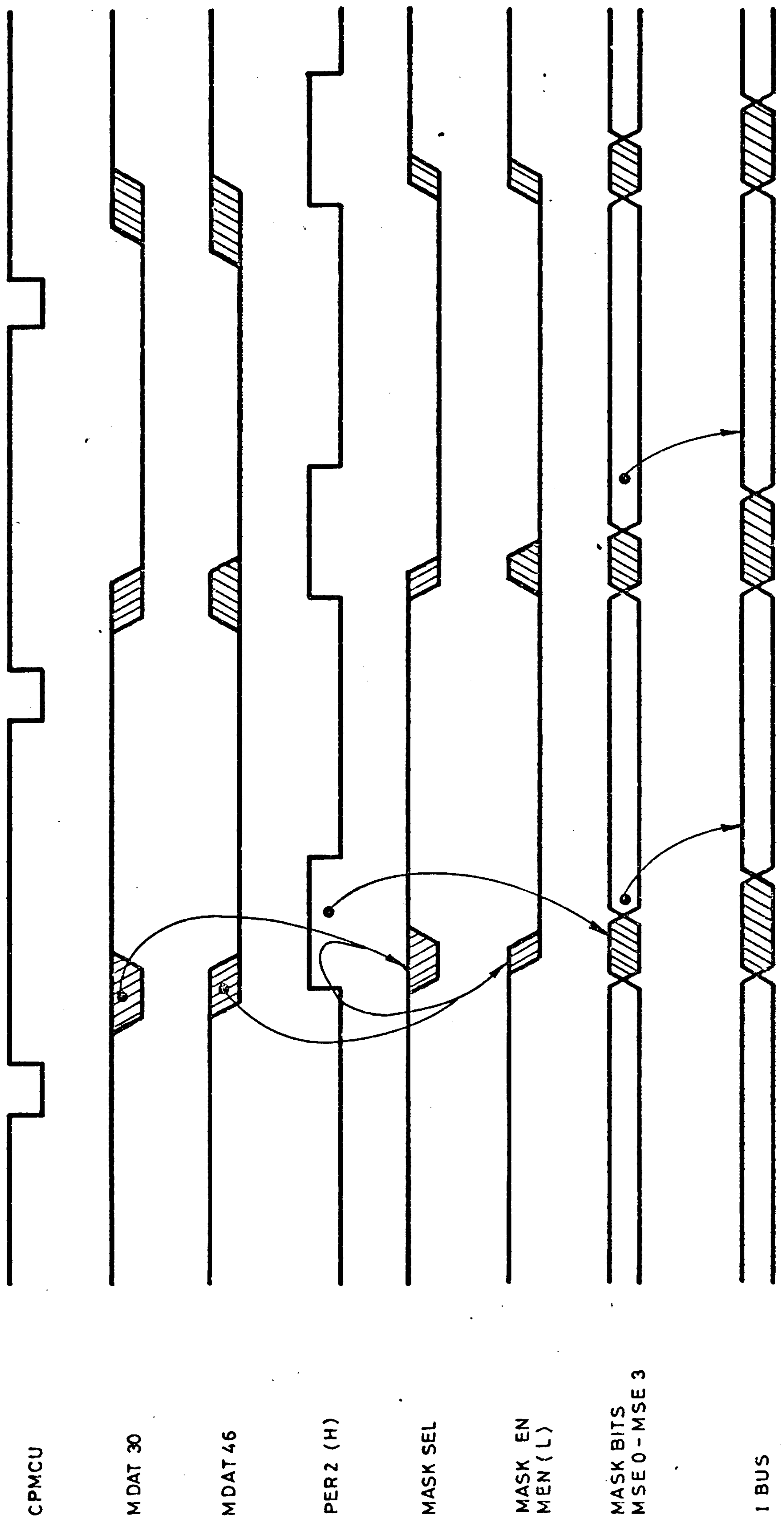


Fig. 3.7.2.

4

PROM TABLES

4. PROM TABLES

This section contain the tables for the PROM's located on the MPB or for the following PROM's CR1270 - CR1283 the VDD.

A summary of the PROM's and their function are given in table 4 overleaf.

				INPUT									OUTPUT			
NO.	REF. DES.	TYPE	FUNCTION	A8	A7	A6	A5	A4	A3	A2	A1	LSB A0	O4	O3	O2	LSB O1
CR1270	UA11	512 x 4 (-1) 3S	PROM 2	MDAT 14	OP 9	OP 3	MDAT 15	OP 8	OP 10	OP 12	OP 13	OP 11	PXP 3	PXP 2	PXP 0	PXP 1
CR1271	UA13	"	PRE PROM	OP 8	OP 9	OP 15	OP 14	POP 7	OP 10	OP 12	OP 13	OP 11	R1.4 (AC2)	R1.3 (AC3)	R1.2 (AC1)	R1.1 (AC0)
CR1272	UC13	"	µP	MPA 8	MPA 7	MPA 6	MPA 5	MPA 4	MPA 3	MPA 2	MPA 1	MPA 0	MDAT 12	MDAT 13	MDAT 11	MDAT 9
CR1273	UC15	"	"	"	"	"	"	"	"	"	"	"	8	10	15	14
CR1274	UC17	"	"	"	"	"	"	"	"	"	"	"	36	39	38	37
CR1275	UD17	"	"	"	"	"	"	"	"	"	"	"	34	35	32	33
CR1276	UE19	"	"	"	"	"	"	"	"	"	"	"	43	42	41	40
CR1277	UE21	"	"	"	"	"	"	"	"	"	"	"	46	47	45	44
CR1278	UF15	"	"	"	"	"	"	"	"	"	"	"	7	0	2	3
CR1279	UF17	"	"	"	"	"	"	"	"	"	"	"	6	4	5	1
CR1280	UF19	"	"	"	"	"	"	"	"	"	"	"	31	30	29	28
CR1281	UF21	"	"	"	"	"	"	"	"	"	"	"	24	25	26	27
CR1282	UG19	"	"	"	"	"	"	"	"	"	"	"	23	22	20	21
CR1283	UG21	"	"	"	"	"	"	"	"	"	"	"	17	18	19	16
CR1269	UB13	256 x 4 (-1) 3S	FLAG PROM		OP 8	OP 13	OP 10	OP 15	MDAT 9	MDAT 12	MDAT 13	MDAT 11	ALS/ PSWSE	FLSE 2	FLSE 1	FLSE 0
				INPUT					OUTPUT							
				E	D	C	B	LSB A	Y8	Y7	Y6	Y5	Y4	Y3	Y2	LSB Y1
CR1266	UB3	32 x 8 (-1) 3S	OP CONTROL	MDAT 36	MDAT 33	MDAT 32	MDAT 34	MDAT 35	EN OPL	U/D COUNT	LD OPL	LD OPH	EN OPH	G CP	GATE CP	RAM/ ROM
CR1267	UG5	32 x 8 (-1) OC	MASK PROM	SEL M	MSE 2	MSE 1	MSE 3	MSE 0	IBUS 15	IBUS 14	IBUS 13	IBUS 12	IBUS 11	IBUS 10	IBUS 9	IBUS 8
CR1268	UG7	"	MASK PROM	"	"	"	"	"	7	6	5	4	3	2	1	0

TABLE 4

MICRO PROGRAM BOARD OP. REG. CONTROL µ-RAM INCLUDED	sign/date GB/770328	page
	prom-type 32x8.3st	cr-no: 1266-1

			INPUT ADDRESSES.					OUTPUT										
			E MDAT 36	D MDAT 33	C MDAT 32	B MDAT 34	A MDAT 35			MSB ENOPL (L)	U/D COUNT	LD OPL (L)	LD OPH (L)	EN OPH (L)	GOP	GATE CP	LSB RAM/ROM	
DEC.	HEX		4	3	2	1	0	HEX		8	7	6	5	4	3	2	1	DESCRIPTION
0	00		0	0	0	0	0	F	9	1	1	1	1	1	0	0	1	OP NOP
1	01		0	0	0	0	1	C	D	1	1	0	0	1	1	0	1	CPU INT
2	02		0	0	0	1	0	B	A	1	0	1	1	1	0	1	0	CL RAM
3	03		0	0	0	1	1	7	9	0	1	1	1	1	0	0	1	INC X2
4	04		0	0	1	0	0	F	9	1	1	1	1	1	0	0	1	T MOP
5	05		0	0	1	0	1	F	9	1	1	1	1	1	0	0	1	PSW-I
6	06		0	0	1	1	0	B	A	1	0	1	1	1	0	1	0	EX PROM
7	07		0	0	1	1	1	D	9	1	1	0	1	1	0	0	1	LD X2
8	08		0	1	0	0	0	C	D	1	1	0	0	1	1	0	1	LD OP
9	09		0	1	0	0	1	F	9	1	1	1	1	1	0	0	1	I-PSW
10	0A		0	1	0	1	0	B	B	1	0	1	1	1	0	1	1	EX RAM
11	0B		0	1	0	1	1	E	9	1	1	1	0	1	0	0	1	LD X1
12	0C		0	1	1	0	0	D	A	1	1	0	1	1	0	1	0	LD RAM
13	0D		0	1	1	0	1	C	9	1	1	0	0	1	0	0	1	LD X1X2
14	0E		0	1	1	1	0	F	9	1	1	1	1	1	0	0	1	SET COND
15	0F		0	1	1	1	1	3	9	0	0	1	1	1	0	0	1	DEC X2
16	10		1	0	0	0	0	7	1	0	1	1	1	0	0	0	1	INC X1X2
17	11		1	0	0	0	1	F	F	1	1	1	1	1	1	1	1	
18	12		1	0	0	1	0	F	9	1	1	1	1	1	0	0	1	CL CPU
19	13		1	0	0	1	1	F	F	1	1	1	1	1	1	1	1	
20	14		1	0	1	0	0	B	1	1	0	1	1	0	0	0	1	DEC X1
21	15		1	0	1	0	1	F	F	1	1	1	1	1	1	1	1	
22	16		1	0	1	1	0	8	F	1	0	0	0	1	1	1	1	EX RAM LD
23	17		1	0	1	1	1	F	F	1	1	1	1	1	1	1	1	
24	1.8		1	1	0	0	0	F	1	1	1	1	1	0	0	0	1	INC X1
25	19		1	1	0	0	1	F	F	1	1	1	1	1	1	1	1	
26	1A		1	1	0	1	0	F	9	1	1	1	1	1	0	0	1	CL I/O
27	1B		1	1	0	1	1	F	F	1	1	1	1	1	1	1	1	
28	1C		1	1	1	0	0	F	9	1	1	1	1	1	0	0	1	CL TM
29	1D		1	1	1	0	1	F	F	1	1	1	1	1	1	1	1	
30	1E		1	1	1	1	0	F	F	1	1	1	1	1	1	1	1	
31	1F		1	1	1	1	1	F	F	1	1	1	1	1	1	1	1	
			4	3	2	1	0			8	7	6	5	4	3	2	1	

MICRO PROGRAM BOARD
OP: REG CONTROL µ-RAM NOT INCLUDED

sign/date GB/770328	page
prom-type 32x8.3st	cr-no: 1266-2

	INPUT	ADDRESSES.					OUTPUT										
		E MDAt 36	D MDAT 33	C MDAT 32	B MDAT 34	A MDAT 35			MSB ENOPL (L)	U/D COUNT	LD OPL (L)	LD OPH (L)	EN OPH (L)	G OP	GATE CP	LSB RAM/ROM	
DEC.	HEX	4	3	2	1	0	HEX		8	7	6	5	4	3	2	1	DESCRIPTION
0	00	0	0	0	0	0	F	9	1	1	1	1	1	0	0	1	OP NOP
1	01	0	0	0	0	1	C	D	1	1	0	0	1	1	0	1	CPU INT
2	02	0	0	0	1	0	B	A	1	0	1	1	1	0	1	0	CL RAM
3	03	0	0	0	1	1	7	9	0	1	1	1	1	0	0	1	INC X2
4	04	0	0	1	0	0	F	9	1	1	1	1	1	0	0	1	T MOD
5	05	0	0	1	0	1	F	9	1	1	1	1	1	0	0	1	PSW-I
6	06	0	0	1	1	0	B	A	1	0	1	1	1	0	1	0	EX PROM
7	07	0	0	1	1	1	D	9	1	1	0	1	1	0	0	1	LD X2
8	08	0	1	0	0	0	C	D	1	1	0	0	1	1	0	1	LD OP
9	09	0	1	0	0	1	F	9	1	1	1	1	1	0	0	1	I-PSW
10	0A	0	1	0	1	0	B	B	1	0	1	1	1	0	1	1	EX RAM
11	0B	0	1	0	1	1	E	9	1	1	1	0	1	0	0	1	LD X1
12	0C	0	1	1	0	0	D	A	1	1	0	1	1	0	1	0	LD RAM
13	0D	0	1	1	0	1	C	9	1	1	0	0	1	0	0	1	LD X1X2
14	0E	0	1	1	1	0	F	9	1	1	1	1	1	0	0	1	SET COND
15	0F	0	1	1	1	1	3	9	0	0	1	1	1	0	0	1	DEC X2
16	10	1	0	0	0	0	7	1	0	1	1	1	0	0	0	1	INC X1X2
17	11	1	0	0	0	1	F	F	1	1	1	1	1	1	1	1	
18	12	1	0	0	1	0	F	9	1	1	1	1	1	0	0	1	CL CPU
19	13	1	0	0	1	1	F	F	1	1	1	1	1	1	1	1	
20	14	1	0	1	0	0	B	1	1	1	0	1	0	0	0	1	DEC X1
21	15	1	0	1	0	1	F	F	1	1	1	1	1	1	1	1	
22	16	1	0	1	1	0	8	E	1	0	0	0	1	1	1	0	EX RAM LD
23	17	1	0	1	1	1	F	F	1	1	1	1	1	1	1	1	
24	1.8	1	1	0	0	0	F	1	1	1	1	1	0	0	0	1	INC X1
25	19	1	1	0	0	1	F	F	1	1	1	1	1	1	1	1	
26	1A	1	1	0	1	0	F	9	1	1	1	1	1	0	0	1	CL I/O
27	1B	1	1	0	1	1	F	F	1	1	1	1	1	1	1	1	
28	1C	1	1	1	0	0	F	9	1	1	1	1	1	0	0	1	CL TM
29	1D	1	1	1	0	1	F	F	1	1	1	1	1	1	1	1	
30	1E	1	1	1	1	0	F	F	1	1	1	1	1	1	1	1	
31	1F	1	1	1	1	1	F	F	1	1	1	1	1	1	1	1	
		4	3	2	1	0			8	7	6	5	4	3	2	1	

CPU CR8001/2/3
MP BOARD MASK PROM II CR 1267-1

sign / date GB/770422

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repl

project

		INPUT						OUTPUT									
		SEL M	MSEL	MSE 1	MSE 3	MSE 0		I BUS 15	I BUS 14	I BUS 13	I BUS 12	I BUS 11	I BUS 10	I BUS 9	I BUS 8		
ADDR. DEC.	OCT.	E 4	D 3	C 2	B 1	A 0		8	7	6	5	4	3	2	1	BIT#.	DESCRIPTION
0	00	0	0	0	0	0		0	0	0	0	0	0	0	0	0	
1	01	0	0	0	0	1		0	0	0	0	0	0	0	0	1	
2	02	0	0	0	1	0		0	0	0	0	0	0	0	0	8	
3	03	0	0	0	1	1		0	0	0	0	0	0	0	1	9	
4	04	0	0	1	0	0		0	0	0	0	0	0	0	0	2	
5	05	0	0	1	0	1		0	0	0	0	0	0	0	0	3	
6	06	0	0	1	1	0		0	0	0	0	0	0	1	1	10	
7	07	0	0	1	1	1		0	0	0	0	0	1	1	1	11	
8	10	0	1	0	0	0		0	0	0	0	0	0	0	0	4	LONGMASK
9	11	0	1	0	0	1		0	0	0	0	0	0	0	0	5	
10	12	0	1	0	1	0		0	0	0	0	1	1	1	1	12	
11	13	0	1	0	1	1		0	0	0	1	1	1	1	1	13	
12	14	0	1	1	0	0		0	0	0	0	0	0	0	0	6	
13	15	0	1	1	0	1		0	0	0	0	0	0	0	0	7	
14	16	0	1	1	1	0		0	0	1	1	1	1	1	1	14	
15	17	0	1	1	1	1		0	1	1	1	1	1	1	1	15	
16	20	1	0	0	0	0		0	0	0	0	0	0	0	0	0	
17	21	1	0	0	0	1		0	0	0	0	0	0	0	0	1	
18	22	1	0	0	1	0		0	0	0	0	0	0	0	1	8	
19	23	1	0	0	1	1		0	0	0	0	0	0	1	0	9	
20	24	1	0	1	0	0		0	0	0	0	0	0	0	0	2	
21	25	1	0	1	0	1		0	0	0	0	0	0	0	0	3	
22	26	1	0	1	1	0		0	0	0	0	0	1	0	0	10	
23	27	1	0	1	1	1		0	0	0	0	1	0	0	0	11	BITMASK
24	30	1	1	0	0	0		0	0	0	0	0	0	0	0	4	
25	31	1	1	0	0	1		0	0	0	0	0	0	0	0	5	
26	32	1	1	0	1	0		0	0	0	1	0	0	0	0	12	
27	33	1	1	0	1	1		0	0	1	0	0	0	0	0	13	
28	34	1	1	1	0	0		0	0	0	0	0	0	0	0	6	
29	35	1	1	1	0	1		0	0	0	0	0	0	0	0	7	
30	36	1	1	1	1	0		0	1	0	0	0	0	0	0	14	
31	37	1	1	1	1	1		1	0	0	0	0	0	0	0	15	
		4	3	2	1	0		8	7	6	5	4	3	2	1		

CPU CR8001/2/3 MP BOARD MASK PROM I CR 1268-1	sign / date GB/770422	page
	repl	project

		INPUT						OUTPUT									
ADDR.		SEL M	MSE 2	MSE 1	MSE 3	MSE 0		I BUS 7	I BUS 6	I BUS 5	I BUS 4	I BUS 3	I BUS 2	I BUS 1	I BUS 0		
DEC.	OCT.	E 4	D 3	C 2	B 1	A 0		8	7	6	5	4	3	2	1	BIT	DESCRIPTION
0	00	0	0	0	0	0		0	0	0	0	0	0	0	0	0	LONGMASK
1	01	0	0	0	0	1		0	0	0	0	0	0	0	1	1	
2	02	0	0	0	1	0		1	1	1	1	1	1	1	1	8	
3	03	0	0	0	1	1		1	1	1	1	1	1	1	1	9	
4	04	0	0	1	0	0		0	0	0	0	0	0	1	1	2	
5	05	0	0	1	0	1		0	0	0	0	0	1	1	1	3	
6	06	0	0	1	1	0		1	1	1	1	1	1	1	1	10	
7	07	0	0	1	1	1		1	1	1	1	1	1	1	1	11	
8	10	0	1	0	0	0		0	0	0	0	1	1	1	1	4	
9	11	0	1	0	0	1		0	0	0	1	1	1	1	1	5	
10	12	0	1	0	1	0		1	1	1	1	1	1	1	1	12	
11	13	0	1	0	1	1		1	1	1	1	1	1	1	1	13	
12	14	0	1	1	0	0		0	0	1	1	1	1	1	1	6	
13	15	0	1	1	0	1		0	1	1	1	1	1	1	1	7	
14	16	0	1	1	1	0		1	1	1	1	1	1	1	1	14	
15	17	0	1	1	1	1		1	1	1	1	1	1	1	1	15	
16	20	1	0	0	0	0		0	0	0	0	0	0	0	1	0	BITMASK
17	21	1	0	0	0	1		0	0	0	0	0	0	1	0	1	
18	22	1	0	0	1	0		0	0	0	0	0	0	0	0	8	
19	23	1	0	0	1	1		0	0	0	0	0	0	0	0	9	
20	24	1	0	1	0	0		0	0	0	0	0	1	0	0	2	
21	25	1	0	1	0	1		0	0	0	0	1	0	0	0	3	
22	26	1	0	1	1	0		0	0	0	0	0	0	0	0	10	
23	27	1	0	1	1	1		0	0	0	0	0	0	0	0	11	
24	30	1	1	0	0	0		0	0	0	1	0	0	0	0	4	
25	31	1	1	0	0	1		0	0	1	0	0	0	0	0	5	
26	32	1	1	0	1	0		0	0	0	0	0	0	0	0	12	
27	33	1	1	0	1	1		0	0	0	0	0	0	0	0	13	
28	34	1	1	1	0	0		0	1	0	0	0	0	0	0	6	
29	35	1	1	1	0	1		1	0	0	0	0	0	0	0	7	
30	36	1	1	1	1	0		0	0	0	0	0	0	0	0	14	
31	37	1	1	1	1	1		0	0	0	0	0	0	0	0	15	
		4	3	2	1	0		8	7	6	5	4	3	2	1		

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MICRO PROGRAM BOARD
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project

FLSE 2	FLSE 1	FLSE 0	
0	0	0	TIME OUT
0	0	1	SEC
0	1	0	$\overline{S\oplus O}$
0	1	1	SEO
1	0	0	QL
1	0	1	SEZ
1	1	0	I/O PENDING
1	1	1	SES

ADDR.		INPUT									OUTPUT				
		OP 8	OP 13	OP 10	OP 15	MDAT 9	MDAT 12	MDAT 13	MDAT 11		ALS/PSW SEL	FLSE 2	FLSE 1	FLSE 0	
DEC.	OCT.	7	6	5	4	3	2	1	0		4	3	2	1	DESCRIPTION
0	000	0	0	0	0	0	0	0	0		1	1	0	0	QL
1	001	0	0	0	0	0	0	0	1		0	0	1	1	SEO
2	002	0	0	0	0	0	0	1	0						
3	003	0	0	0	0	0	0	1	1		1	1	0	0	QL
4	004	0	0	0	0	0	1	0	0						
5	005	0	0	0	0	0	1	0	1		1	0	0	0	TIME OUT
6	006	0	0	0	0	0	1	1	0						
7	007	0	0	0	0	0	1	1	1		1	1	1	1	SES
8	010	0	0	0	0	1	0	0	0		1	1	1	0	I/O PENDING
9	011	0	0	0	0	1	0	0	1		1	1	0	1	SEZ
10	012	0	0	0	0	1	0	1	0		1	0	1	0	$\overline{S\oplus O}$
11	013	0	0	0	0	1	0	1	1		1	1	0	1	SEZ
12	014	0	0	0	0	1	1	0	0						
13	015	0	0	0	0	1	1	0	1						
14	016	0	0	0	0	1	1	1	0		1	1	0	1	SEZ
15	017	0	0	0	0	1	1	1	1						
16	020	0	0	0	1	0	0	0	0		1	1	0	0	QL
17	021	0	0	0	1	0	0	0	1		0	0	1	1	SEO
18	022	0	0	0	1	0	0	1	0						
19	023	0	0	0	1	0	0	1	1		1	1	0	0	QL
20	024	0	0	0	1	0	1	0	0						
21	025	0	0	0	1	0	1	0	1		1	0	0	0	TIME OUT
22	026	0	0	0	1	0	1	1	0						
23	027	0	0	0	1	0	1	1	1		1	1	1	1	SES
24	030	0	0	0	1	1	0	0	0		1	1	1	0	I/O PENDING
25	031	0	0	0	1	1	0	0	1		1	1	0	1	SEZ
26	032	0	0	0	1	1	0	1	0						
27	033	0	0	0	1	1	0	1	1		1	1	0	1	SEZ
28	034	0	0	0	1	1	1	0	0						
29	035	0	0	0	1	1	1	0	1						
30	036	0	0	0	1	1	1	1	0		1	1	0	1	SEZ
31	037	0	0	0	1	1	1	1	1						
		7		5	4	3	2	1	0		4	3	2	1	

CPU CR8001/2/3
MICRO PROGRAM BOARD
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ADDR.		INPUT									OUTPUT				
		OP 8	OP 13	OP 10	OP 15	MDAT 9	MDAT 12	MDAT 13	MDAT 11		ALS/PSW SEL	FLSE 2	FLSE 1	FLSE 0	
DEC.	OCT.	7	6	5	4	3	2	1	0		4	3	2	1	DESCRIPTION
32	040	0	0	1	0	0	0	0	0		1	1	0	0	QL
33	041	0	0	1	0	0	0	0	1		0	0	1	1	SEO
34	042	0	0	1	0	0	0	1	0						
35	043	0	0	1	0	0	0	1	1		1	1	0	0	QL
36	044	0	0	1	0	0	1	0	0						
37	045	0	0	1	0	0	1	0	1		1	0	0	0	TIME OUT (L)
38	046	0	0	1	0	0	1	1	0						
39	047	0	0	1	0	0	1	1	1		1	1	1	1	SES
40	050	0	0	1	0	1	0	0	0		1	1	1	0	I/O PENDING
41	051	0	0	1	0	1	0	0	1		1	1	0	1	SEZ
42	052	0	0	1	0	1	0	1	0		1	0	0	1	SEC
43	053	0	0	1	0	1	0	1	1		1	1	0	1	SEZ
44	054	0	0	1	0	1	1	0	0						
45	055	0	0	1	0	1	1	0	1						
46	056	0	0	1	0	1	1	1	0		1	1	0	1	SEZ
47	057	0	0	1	0	1	1	1	1						
48	060	0	0	1	1	0	0	0	0		1	1	0	0	QL
49	061	0	0	1	1	0	0	0	1		0	0	1	1	SEO
50	062	0	0	1	1	0	0	1	0						
51	063	0	0	1	1	0	0	1	1		1	1	0	0	QL
52	064	0	0	1	1	0	1	0	0						
53	065	0	0	1	1	0	1	0	1		1	0	0	0	TIME OUT (L)
54	066	0	0	1	1	0	1	1	0						
55	067	0	0	1	1	0	1	1	1		1	1	1	1	SES
56	070	0	0	1	1	1	0	0	0		1	1	1	0	I/O PENDING
57	071	0	0	1	1	1	0	0	1		1	1	0	1	SEZ
58	072	0	0	1	1	1	0	1	0						
59	073	0	0	1	1	1	0	1	1		1	1	0	1	SEZ
60	074	0	0	1	1	1	1	0	0						
61	075	0	0	1	1	1	1	0	1						
62	076	0	0	1	1	1	1	1	0		1	1	0	1	SEZ
63	077	0	0	1	1	1	1	1	1						
		7	6	5	4	3	2	1	0		4	3	2	1	

CPU CR8001/2/3 MICRO PROGRAM BOARD FLAG CONTROL PROM CR 1269-1	sign/date GB/770328	page 3	
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		INPUT									OUTPUT				
		OP 8	OP 13	OP 10	OP 15	MDAT 9	MDAT 12	MDAT 13	MDAT 11		ALS/PSW SEL	FLSE 2	FLSE 1	FLSE 0	
ADDR. DEC.	OCT.	7	6	5	4	3	2	1	0		4	3	2	1	DESCRIPTION
64	100	0	1	0	0	0	0	0	0		1	1	0	0	OL
65	101	0	1	0	0	0	0	0	1		0	0	1	1	SEO
66	102	0	1	0	0	0	0	1	0						
67	103	0	1	0	0	0	0	1	1		1	1	0	0	OL
68	104	0	1	0	0	0	1	0	0						
69	105	0	1	0	0	0	1	0	1		1	0	0	0	TIME OUT (L)
70	106	0	1	0	0	0	1	1	0						
71	107	0	1	0	0	0	1	1	1		1	1	1	1	SES
72	110	0	1	0	0	1	0	0	0		1	1	1	0	I/O PENDING
73	111	0	1	0	0	1	0	0	1		1	1	0	1	SEZ
74	112	0	1	0	0	1	0	1	0		1	1	0	1	SEZ
75	113	0	1	0	0	1	0	1	1		1	1	0	1	SEZ
76	114	0	1	0	0	1	1	0	0						
77	115	0	1	0	0	1	1	0	1						
78	116	0	1	0	0	1	1	1	0		1	1	0	1	SEZ
79	117	0	1	0	0	1	1	1	1						
80	120	0	1	0	1	0	0	0	0		1	1	0	0	OL
81	121	0	1	0	1	0	0	0	1		0	0	1	1	SEO
82	122	0	1	0	1	0	0	1	0						
83	123	0	1	0	1	0	0	1	1		1	1	0	0	OL
84	124	0	1	0	1	0	1	0	0						
85	125	0	1	0	1	0	1	0	1		1	0	0	0	TIME OUT (L)
86	126	0	1	0	1	0	1	1	0						
87	127	0	1	0	1	0	1	1	1		1	1	1	1	SES
88	130	0	1	0	1	1	0	0	0		1	1	1	0	I/O PENDING
89	131	0	1	0	1	1	0	0	1		1	1	0	1	SEZ
90	132	0	1	0	1	1	0	1	0		1	1	0	1	SEZ
91	133	0	1	0	1	1	0	1	1		1	1	0	1	SEZ
92	134	0	1	0	1	1	1	0	0						
93	135	0	1	0	1	1	1	0	1						
94	136	0	1	0	1	1	1	1	0		1	1	0	1	SEZ
95	137	0	1	0	1	1	1	1	1						
		7	6	5	4	3	2	1	0		4	3	2	1	

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CPU CR8001/2/3 MICRO PROGRAM BOARD FLAG CONTROL PROM CR 1269-1	sign/date GB/770328	page 4
	repl	project

		INPUT								OUTPUT				
		OP 8	OP 13	OP 10	OP 15	MDAT 9	MDAT 12	MDAT 13	MDAT 11	ALS/PSW SEL.	FLSE 2	FLSE 1	FLSE 0	
ADDR. DEC.	OCT.	7	6	5	4	3	2	1	0	4	3	2	1	DESCRIPTION
96	140	0	1	1	0	0	0	0	0	1	1	0	0	QL
97	141	0	1	1	0	0	0	0	1	0	0	1	1	SEO
98	142	0	1	1	0	0	0	1	0					
99	143	0	1	1	0	0	0	1	1	1	1	0	0	QL
100	144	0	1	1	0	0	1	0	0					
101	145	0	1	1	0	0	1	0	1	1	0	0	0	TIME OUT (L)
102	146	0	1	1	0	0	1	1	0					
103	147	0	1	1	0	0	1	1	1	1	1	1	1	SES
104	150	0	1	1	0	1	0	0	0	1	1	1	0	I/O PENDING
105	151	0	1	1	0	1	0	0	1	1	1	0	1	SEZ
106	152	0	1	1	0	1	0	1	0	1	1	0	1	SEZ
107	153	0	1	1	0	1	0	1	1	1	1	0	1	SEZ
108	154	0	1	1	0	1	1	0	0					
109	155	0	1	1	0	1	1	0	1					
110	156	0	1	1	0	1	1	1	0	1	1	0	1	SEZ
111	157	0	1	1	0	1	1	1	1					
112	160	0	1	1	1	0	0	0	0	1	1	0	0	QL
113	161	0	1	1	1	0	0	0	1	0	0	1	1	SEO
114	162	0	1	1	1	0	0	1	0					
115	163	0	1	1	1	0	0	1	1	1	1	0	0	QL
116	164	0	1	1	1	0	1	0	0					
117	165	0	1	1	1	0	1	0	1	1	0	0	0	TIME OUT (L)
118	166	0	1	1	1	0	1	1	0					
119	167	0	1	1	1	0	1	1	1	1	1	1	1	SES
120	170	0	1	1	1	1	0	0	0	1	1	1	0	I/O PENDING
121	171	0	1	1	1	1	0	0	1	1	1	0	1	SEZ
122	172	0	1	1	1	1	0	1	0	1	0	1	0	$\overline{S \oplus O}$
123	173	0	1	1	1	1	0	1	1	1	1	0	1	SEZ
124	174	0	1	1	1	1	1	0	0					
125	175	0	1	1	1	1	1	0	1					
126	176	0	1	1	1	1	1	1	0	1	1	0	1	SEZ
127	177	0	1	1	1	1	1	1	1					
		7	6	5	4	3	2	1	0	4	3	2	1	

CPU CR8001/2/3
MICRO PROGRAM BOARD
FLAG CONTROL PROM

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ADDR.		INPUT									OUTPUT				
		OP 8	OP 13	OP 10	OP 10	OP 15	MDAT 9	MDAT 12	MDAT 13	MDAT 11	ALS/PSW SEL	FLSE 2	FLSE 1	FLSE 0	
DEC.	OCT.	7	6	5	4	3	2	1	0		4	3	2	1	DESCRIPTION
128	200	1	0	0	0	0	0	0	0		1	1	0	0	QL
129	201	1	0	0	0	0	0	0	1		0	0	1	1	SEO
130	202	1	0	0	0	0	0	1	0						
131	203	1	0	0	0	0	0	1	1		1	1	0	0	QL
132	204	1	0	0	0	0	1	0	0						
133	205	1	0	0	0	0	1	0	1		1	0	0	0	TIME OUT (L)
134	206	1	0	0	0	0	1	1	0						
135	207	1	0	0	0	0	1	1	1		1	1	1	1	SES
136	210	1	0	0	0	1	0	0	0		1	1	1	0	I/O PENDING
137	211	1	0	0	0	1	0	0	1		1	1	0	1	SEZ
138	212	1	0	0	0	1	0	1	0		1	0	1	0	$\overline{S\oplus O}$
139	213	1	0	0	0	1	0	1	1		1	1	0	1	SEZ
140	214	1	0	0	0	1	1	0	0						
141	215	1	0	0	0	1	1	0	1						
142	216	1	0	0	0	1	1	1	0		1	1	0	2	SEZ
143	217	1	0	0	0	1	1	1	1						
144	220	1	0	0	1	0	0	0	0		1	1	0	0	QL
145	221	1	0	0	1	0	0	0	1		0	0	1	1	SEO
146	222	1	0	0	1	0	0	1	0						
147	223	1	0	0	1	0	0	1	1		1	1	0	0	QL
148	224	1	0	0	1	0	1	0	0						
149	225	1	0	0	1	0	1	0	1		1	0	0	0	TIME OUT
150	226	1	0	0	1	0	1	1	0						
151	227	1	0	0	1	0	1	1	1		1	1	1	1	SES
152	230	1	0	0	1	1	0	0	0		1	1	1	0	I/O PENDING
153	231	1	0	0	1	1	0	0	1		1	1	0	1	SEZ
154	232	1	0	0	1	1	0	1	0						
155	233	1	0	0	1	1	0	1	1		1	1	0	1	SEZ
156	234	1	0	0	1	1	1	0	0						
157	235	1	0	0	1	1	1	0	1						
158	236	1	0	0	1	1	1	1	0		1	1	0	1	sez
159	237	1	0	0	1	1	1	1	1						
		7	6	5	4	3	2	1	0		4	3	2	1	

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MICRO PROGRAM BOARD
FLAG CONTROL PROM CR 1269-1

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ADDR.		INPUT									OUTPUT				
		OP 8	OP 13	OP 10	OP 15	MDAT 9	MDAT 12	MDAT 13	MDAT 11		ALS/PSW sel	FLSE 2	FLSE 1	FLSE 0	
DEC.	OCT.	7	6	5	4	3	2	1	0		4	3	2	1	DESCRIPTION
160	240	1	0	1	0	0	0	0	0		1	1	0	0	QL
161	241	1	0	1	0	0	0	0	1		0	0	1	1	SEO
162	242	1	0	1	0	0	0	1	0						
163	243	1	0	1	0	0	0	1	1		1	1	0	0	QL
164	244	1	0	1	0	0	1	0	0						
165	245	1	0	1	0	0	1	0	1		1	0	0	0	TIME OUT
166	246	1	0	1	0	0	1	1	0						
167	247	1	0	1	0	0	1	1	1		1	1	1	1	SES
168	250	1	0	1	0	1	0	0	0		1	1	1	0	I/O PENDING
169	251	1	0	1	0	1	0	0	1		1	1	0	1	SEZ
170	252	1	0	1	0	1	0	1	0		1	0	0	1	SEC
171	253	1	0	1	0	1	0	1	1		1	1	0	1	SEZ
172	254	1	0	1	0	1	1	0	0						
173	255	1	0	1	0	1	1	0	1						
174	256	1	0	1	0	1	1	1	0		1	1	0	1	SEZ
175	257	1	0	1	0	1	1	1	1						
176	260	1	0	1	1	0	0	0	0		1	1	0	0	QL
177	261	1	0	1	1	0	0	0	1		0	0	1	1	SEO
178	262	1	0	1	1	0	0	1	0						
179	263	1	0	1	1	0	0	1	1		1	1	0	0	QL
180	264	1	0	1	1	0	1	0	0						
181	265	1	0	1	1	0	1	0	1		1	0	0	0	TIME OUT
182	266	1	0	1	1	0	1	1	0						
183	267	1	0	1	1	0	1	1	1		1	1	1	1	SES
184	270	1	0	1	1	1	0	0	0		1	1	1	0	I/O PENDING
185	271	1	0	1	1	1	0	0	1		1	1	0	1	SEZ
186	272	1	0	1	1	1	0	1	0						
187	273	1	0	1	1	1	0	1	1		1	1	0	1	SEZ
188	274	1	0	1	1	1	1	0	0						
189	275	1	0	1	1	1	1	0	1						
190	276	1	0	1	1	1	1	1	0		1	1	0	1	SEZ
191	277	1	0	1	1	1	1	1	1						
		7	6	5	4	3	2	1	0		4	3	2	1	

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		INPUT									OUTPUT				
ADDR.		OP 8	OP 13	OP 10	OP 15	MDAT 9	MDAT 12	MDAT 13	MDAT 11		ALS/PSW SEL	FLSE 2.	FLSE 1	FLSE 0	
DEC.	OCT.	7	6	5	4	3	2	1	0		4	3	2	1	DESCRIPTION
192	300	1	1	0	0	0	0	0	0		1	1	0	0	QL
193	301	1	1	0	0	0	0	0	1		0	0	1	1	SEO
194	302	1	1	0	0	0	0	1	0						
195	303	1	1	0	0	0	0	1	1		1	1	0	0	QL
196	304	1	1	0	0	0	1	0	0						
197	305	1	1	0	0	0	1	0	1		1	0	0	0	TIME OUT
198	306	1	1	0	0	0	1	1	0						
199	307	1	1	0	0	0	1	1	1		1	1	1	1	SES
200	310	1	1	0	0	1	0	0	0		1	1	1	0	I/O PENDING
201	311	1	1	0	0	1	0	0	1		1	1	0	1	SEZ
202	312	1	1	0	0	1	0	1	0		1	1	0	1	SEZ
203	313	1	1	0	0	1	0	1	1		1	1	0	1	SEZ
204	314	1	1	0	0	1	1	0	0						
205	315	1	1	0	0	1	1	0	1						
206	316	1	1	0	0	1	1	1	0		1	1	0	1	SEZ
207	317	1	1	0	0	1	1	1	1						
208	320	1	1	0	1	0	0	0	0		1	1	0	0	QL
209	321	1	1	0	1	0	0	0	1		0	0	1	1	SEO
210	322	1	1	0	1	0	0	1	0						
211	323	1	1	0	1	0	0	1	1		1	1	0	0	QL
212	324	1	1	0	1	0	1	0	0						
213	325	1	1	0	1	0	1	0	1		1	0	0	0	TIME OUT
214	326	1	1	0	1	0	1	1	0						
215	327	1	1	0	1	0	1	1	1		1	1	1	1	SES
216	330	1	1	0	1	1	0	0	0		1	1	1	0	I/O PENDING
217	331	1	1	0	1	1	0	0	1		1	1	0	1	SEZ
218	332	1	1	0	1	1	0	1	0		1	1	0	1	SEZ
219	333	1	1	0	1	1	0	1	1		1	1	0	1	SEZ
220	334	1	1	0	1	1	1	0	0						
221	335	1	1	0	1	1	1	0	1						
222	336	1	1	0	1	1	1	1	0		1	1	0	1	SEZ
223	337	1	1	0	1	1	1	1	1						
		7	6	5	4	3	2	1	0		4	3	2	1	

CPU CR8001/2/3
MICRO PROGRAM BOARD
FLAG CONTROL PROM CR 1269-1

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		INPUT									OUTPUT				
ADDR.		OP 8	OP 13	OP 10	OP 15	MDAT 9	MDAT 12	MDAT 13	MDAT 11		ALS/PSW SEL	FLSE 2	FLSE 1	FLSE 0	
DEC.	OCT.	7	6	5	4	3	2	1	0		4	3	2	1	DESCRIPTION
224	340	1	1	1	0	0	0	0	0		1	1	0	0	QL
225	341	1	1	1	0	0	0	0	1		0	0	1	1	SEO
226	342	1	1	1	0	0	0	1	0						
227	343	1	1	1	0	0	0	1	1		1	1	0	0	QL
228	344	1	1	1	0	0	1	0	0						
229	345	1	1	1	0	0	1	0	1		1	0	0	0	TIME OUT
230	346	1	1	1	0	0	1	1	0						
231	347	1	1	1	0	0	1	1	1		1	1	1	1	SES
232	350	1	1	1	0	1	0	0	0		1	1	1	0	I/O PENDING
233	351	1	1	1	0	1	0	0	1		1	1	0	1	SEZ
234	352	1	1	1	0	1	0	1	0		1	1	0	1	SEZ
235	353	1	1	1	0	1	0	1	1		1	1	0	1	SEZ
236	354	1	1	1	0	1	1	0	0						
237	355	1	1	1	0	1	1	0	1						
238	356	1	1	1	0	1	1	1	0		1	1	0	1	SEZ
239	357	1	1	1	0	1	1	1	1						
240	360	1	1	1	1	0	0	0	0		1	1	0	0	QL
241	361	1	1	1	1	0	0	0	1		0	0	1	1	SEO
242	362	1	1	1	1	0	0	1	0						
243	363	1	1	1	1	0	0	1	1		1	1	0	0	QL
244	364	1	1	1	1	0	1	0	0						
245	365	1	1	1	1	0	1	0	1		1	0	0	0	TIME OUT
246	366	1	1	1	1	0	1	1	0						
247	367	1	1	1	1	0	1	1	1		1	1	1	1	SES
248	370	1	1	1	1	1	0	0	0		1	1	1	0	I/O PENDING
249	371	1	1	1	1	1	0	0	1		1	1	0	1	SEZ
250	372	1	1	1	1	1	0	1	0		1	0	0	1	SEC
251	373	1	1	1	1	1	0	1	1		1	1	0	1	SEZ
252	374	1	1	1	1	1	1	0	0						
253	375	1	1	1	1	1	1	0	1						
254	376	1	1	1	1	1	1	1	0		1	1	0	1	SEZ
255	377	1	1	1	1	1	1	1	1						
		7	6	5	4	3	2	1	0		4	3	2	1	

5

SIGNAL LISTS

MICRO PROGRAM BOARD (MPB) WIRE LIST W1	sign/date GB/780315	page
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PLUG TYPE :

CABEL TYPE: 16 WIRES FLAT CABLE

P/N 5.58102-04

LENGTH :

REFERENCE DESIGNATION	MPB P1 (E1)
	ALB J1

PIN NO.	SIGNAL NAME	INPUT/OUTPUT
1	CPALS	I
2	PER2(H)	I
3	PER0(H)	I
4	GIBUSCONT	O
5	LDMCU(L)	I
6	CPALS	I
7	CPMCU	I
8	LDMCU(H)	I
9	GND	
10	GND	
11	GND	
12	GND	
13	GND	
14	PER0(L)	I
15	GND	
16	GND	

MICRO PROGRAM BOARD (MPB) WIRE LIST W2	sign/date GB/780315 repl	page project
PLUG TYPE :	P/N 5.58102-04	
CABEL TYPE : 16 WIRES FLAT CABLE		
LENGTH :		
REFERENCE DESIGNATION	MPB P2 (H2) ALB J2	

PIN NO.	SIGNAL NAME	INPUT/OUTPUT
1	GND	
2	DIS PRE(H)	I
3	JZR(H)	0
4	GND	
5	I BUS 4	I/O
6	PSW/ALS SEL	0
7	I BUS 5	I/O
8	I BUS	I/O
9	GND	
10	I BUS 14	I/O
11	I BUS 13	I/O
12	I BUS 12	I/O
13	I BUS 11	I/O
14	I BUS 10	I/O
15	I BUS 9	I/O
16	I BUS 8	I/O

MICRO PROGRAM BOARD (MPB)
WIRE LIST W3

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project

PLUG TYPE :

CABEL TYPE: 16 WIRES FLAT CABLE

P/N 5.58102-08

LENGTH :

REFERENCE DESIGNATION
MPB P3 (H4)
ALB J3

PIN NO.	SIGNAL NAME	INPUT/OUTPUT
1	MDAT 20	0
2	MDAT 7	0
3	MDAT 16	0
4	MDAT 19	0
5	GND	
6	MDAT 17	0
7	MDAT 18	0
8	GND	
9	GND	
10	I BUS 0	I/O
11	I BUS 1	I/O
12	I BUS 2	I/O
13	I BUS 3	I/O
14	I BUS 15	I/O
15	I BUS 7	I/O
16	GND	

MICRO PROGRAM BOARD (MPB) WIRE LIST W4	sign/date GB/770315	page
	repl	project

PLUG TYPE :

CABEL TYPE : 16 WIRES FLAT CABLE

P/N 5.58102-02

LENGTH :

REFERENCE DESIGNATION	MPB P4 (I1)
	ALB J4

PIN NO.	SIGNAL NAME	INPUT/OUTPUT
1	MDAT 35	0
2	MDAT 34	0
3	GND	
4	MDAT 32	0
5	MDAT 33	0
6	GND	
7	MDAT 36	0
8	GND	
9	SES	I
10	SEO	I
11	SEZ	I
12	SEC	I
13	I/O PENDING	I
14	SOO	I
15	Q1	I
16	TIME OUT	I

MICRO PROGRAM BOARD (MPB)
WIRE LIST W5

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page
repl
project

PLUG TYPE :

CABEL TYPE: 16 WIRES FLAT CABLE

P/N 5.58102-04

LENGTH :

REFERENCE DESIGNATION	´MPB P5 (I3)
	ALB J5

PIN NO.	SIGNAL NAME	INPUT/OUTPUT
1	MDAT 0	0
2	GND	
3	MDAT 5	0
4	MDAT 4	0
5	MDAT 6	0
6	MDAT 22	0
7	TIMER INT	I
8	MODIFY	I
9	POWER DETECT	I
10	CPU INT	I
11	GND	
12	OP8	0
13	GND	
14	OP0	0
15	OP2	0
16	OP1	0

MICRO PROGRAM BOARD (MPB) WIRE LIST W6	sign/date GB/770315	page
	repl	project
PLUG TYPE :	P/N 5.58102-07	
CABEL TYPE : 16 WIRES FLAT CABLE		
LENGTH :		

REFERENCE DESIGNATION	
	MPB P6 (I5)
	ALB J6

PIN NO.	SIGNAL NAME	INPUT/OUTPUT
1	BA1	0
2	BA0	0
3	GND	
4	MDAT 1	I
5	BA3	0
6	BA2	0
7	AA1	0
8	AA0	0
9	GND	
10	AA2	0
11	AA3	0
12	GND	
13	MDAT 2	0
14	MDAT 3	0
15	MDAT 21	0
16	MDAT 23	0

ARITHMETICAL LOGICAL BOARD (ALB)	sign/date GB/780521	page
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1. INTRODUCTION

The ALB is one of the 3 PCB belonging to the CPU CR8001/2 & CR8001/3. The ALB is the middle board of the 3 CPU boards and the connection to the two other the MPB and the BIB are carried out by means of flat cables for the signals and two desired wires to each of the two other boards for the power +5V and GND.

2. GENERAL DESCRIPTION

The ALB perform the aritmetics and logical function in the CPU under control of the micro program located on the MPB. The interconnection of the two internal busses the I-BUS and the T-BUS interrupt and process status word (PSW) are also located on the ALB.

The data input/output to the board comes from the BIB via the 16 bits T-BUS. The T-BUS is a 3-state multiplexed bus where the bus access is shared between the ALS output, the 4/8 shifter and the BIB. The multiplexing of the bus is H/W controlled meaning that it is taken out from the master timing on the BIB. The other internal bus, the I-BUS, is an open collector bus with a cycle time corresponding to the μ step cycle time 375 ns and the sources to it , is controlled by the μ program. the source for the I-BUS is either the 4 words T-File, PSW or the Mask circuit located on the MPB. The I-BUS is input to the ALU & the PSW.

The data input from the BIB on the T-BUS is always loaded into the T-File, which have two registers for data TFD1-2, and two registers for instructions TFI1-2, one for the current swaped instruction, and one for the next "Advantage Instruction Fetch". The T-File output is input to the ALU, PSW and the 4/8 shifter.

When the data from the BIB has to be loaded into the ALS, it can go direct through the T-File and the ALS ALU and to the ALS's internal registers or the address or data register located on the BIB.

The destination of the data is determined by the µ program, ALS B address and/or bus control functions. If e.g the operation on the data was to And it with a register and store the result in another register the following was specified by the µ program.

Destination register	:	B address
Register to be	:	A address
And data input with A	:	I0-I7 ALS func.
Bus In to TD1 → to Data In	:	Bus Control func. T-File Control.

When the instruction is loaded into the OP register located on the MPB, the instruction is transferred to the I-BUS from the T-File output and in the same µ cycle the instruction is swaped by the 4/8 shifter and loaded back into the T-File in the other instructions register TFI. If the instructions is of the type with displacement it can be fetched from the T-File to the ALS data input and at the same time force a mask on the I-BUS and thereby set the I-BUS to zero except for the displacement, this feature is used for e.g. base relative instructions where the masked displacement is added to the MBASE register to give the memory address.
The shift circuit located above the ALS in the block diagram, is used in shift instruction to perform shift of 16 bits or 32 bits word with the shift input controlled from the µ program via the A address. The shift circuit is also used for generation of the addressing mode byte/word or I/O. The data fetch from the main memory is checked for correct parity, and when data is transferred to the memory parity bits is added. This function is performed in the Parity & Time out circuit.

ARITHMETICAL LOGICAL BOARD (ALB)	sign/date GB/780521	page
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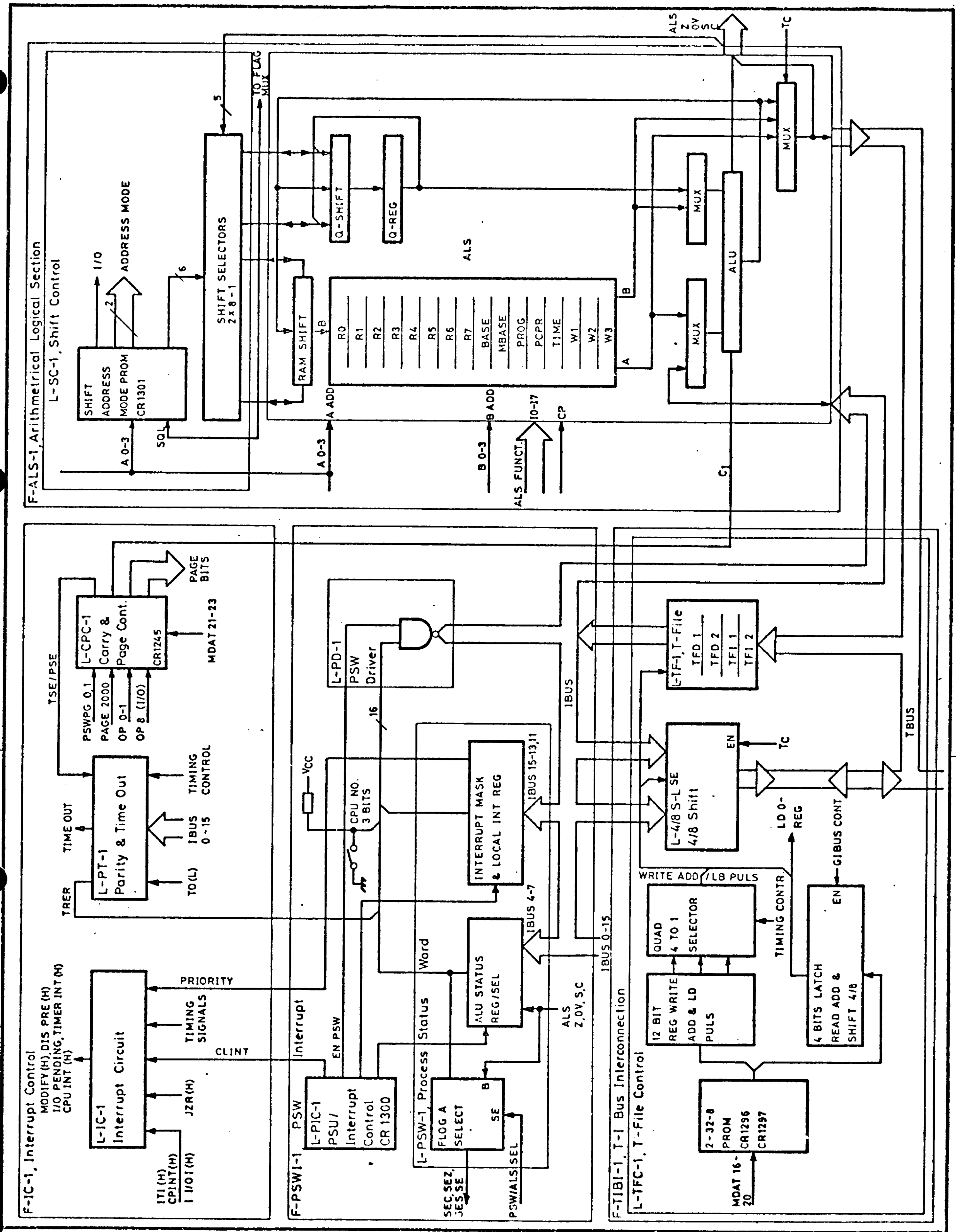
If parity error or ar addressing time out is recognized the CPU will be reset. The interrupt signals are only enabled to the MPB when a JZR(H) occurs. If an interrupt is waiting and the corresponding mask bit in PSW is not set the signal DIS PRE(H) will go active and thereby force the μ program to the interrupt routine DIS PRE (H) will stay active if the preceding instruction was a modify MODIFY (H) active.

The process status word PSW contain different status bits relevant for the process. Some of the bit are under S/W control and can be loaded from the I-BUS.

The output from PSW is available in the I-BUS, and thereby for the ALS, if specified by the μ program.

Some of the bits are used for controlling the H/W e.g. the three interrupt mask bits and page bits.

The contents of PSW is specified in the ALB block diagram.



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3. SPECIFICATIONS

The ALB is a standard CR80 PCB described to fit into the CPU CR8001/2 and CPU CR8001/3. The connection to the other two boards MPB & BIB is carried out by 16 wires flat cables ref signal lists section 6. All input and output signals are normal TTL logic levels i.e.

High level: $2.0 < V_H < 5V$
Low level : $0 < V_L < 0.8V$

3.1 Memory & I/O Addressing with 20 Bits

2 mode bits : word, U byte, L byte and I/O
2 page bits from PSW, OP0,1 zero or OP8 (I/O)
16 word address bits

3.2 Operate on 16 bits data

3.3 Parity check and generation when communicates with main memory.

3.4 22 x 16 bits registers, all available for the µ programmer.

3.5 3 interrupt types : Timer, I/O & CPU
Mask bits in PSW for disabling of interrupt.

3.6 Cycle time min. 375 ns.

3.7 Mechanical dimensions

CR80 standard PCB without edge connector 220 x 280 mm
High of component side : 8 mm
High of soldering side : 8 mm

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3.8 Power consumption

+5V ± A

4. FUNCTIONAL DESCRIPTION

This section gives a detailed description of the circuit located on the ALB. The description of the board is bused upon the block diagram and the blocked schematic.

The ALB is divided into the following four functional blocks:

1.	T - I-BUS Interconnection	F-TIBI-1
2.	PSW & Interrupt	F-PSW-1
3.	Interrupt Control	F-IC-1
4.	Aritmetical Logical Section	F-ALS-1

These functional blocks are described in the following.

4.1 T - I-BUS Interconnection F-TIBI-1

The function of F-TIBI-1 is to make the connection between the T-BUS and the I-BUS so, that the data on the T-BUS (ALS out/4/8 shift out and BUS In) can be synchronized to the μ cycles before it is feed to the ALS via the I-BUS. This synchronization is carried out by a four words register file (T-File) which at the same time is used as temporary storages for the data and the instructions.

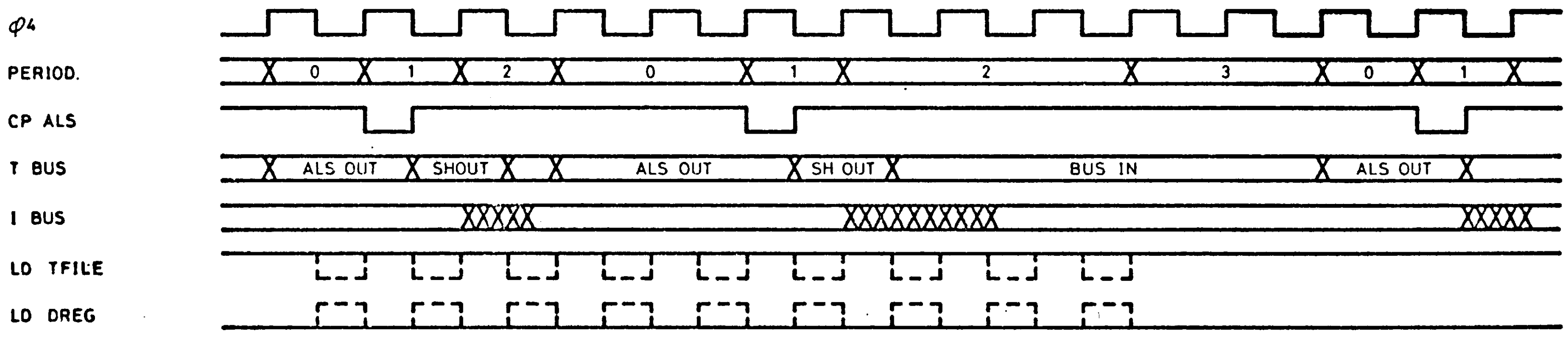
Beside the T-File a 4 or 8 shift selector is included, so that the I-BUS can go via the T-BUS to the T-File, Address Register and Data Register, the two last are present on the BIB. The timing of the two internal CPU bus's and the decoding of the function code to the block MDAT 16-20 is specified in Functional Table 4.1. Note that the MDAT signals are used for controlling the CR80 Bus's also.

TABLE 4.1

FUNCTION	NO.	MDAT					T-FILE FUNCTIONS													D REG INPUT : T-BUS		
							OUTPUT I-BUS			INPUT∽T-BUS										ALS OUT	SHIFT OUT	BUS IN
										ALS OUT			SHIFT OUT			BUS IN			SHIFT 4/8 (1/0)			
		20	19	18	17	16	REN (L)	RA1	RA0	LD (L)	WA1	WA0	LD (L)	WA1	WA0	LD (L)	WA1	WA0		LD (H)	LD (H)	LD (H)
BCNOP	0	0	0	0	0	0	1			1			1			1				0	0	0
FNI	1	0	0	0	0	1	0	0	1	1			0	0	0	0	0	1	0	0	0	0
INS1	2	0	0	0	1	0	0	0	0	1			1			1				0	0	0
TD1	3	0	0	0	1	1	0	1	0	1			1			1				0	0	0
INC OUT	4	0	0	1	0	0	1			1			1			1				1	0	0
ARSF TD1	5	0	0	1	0	1	0	0	0	1			1			0	1	0		0	0	1
TD2	6	0	0	1	1	0	0	1	1	1			1			1				0	0	0
INS1 FI	7	0	0	1	1	1	0	0	0	1			1			0	0	1		0	0	0
LAR	8	0	1	0	0	0	0	0	0	1			1			1				1	0	0
ALS TD1	9	0	1	0	0	1	0	0	0	0	1	0	1			1				1	0	0
FI	10	0	1	0	1	0	1			1			1			0	0	1		0	0	0
MAR TD1	11	0	1	0	1	1	0	0	0	1			1			0	1	0		0	0	1
ALS DR MAR	12	0	1	1	0	0	0	1	0	1			1			1				1	0	0
TI1 S8 TD1	13	0	1	1	0	1	0	0	0	1			0	1	0	1			0	0	0	0
TI1 S4 TD1	14	0	1	1	1	0	0	0	0	1			0	1	0	1			1	0	0	0
TD1 FI	15	0	1	1	1	1	0	1	0	1			1			0	0	1		0	0	0
TD1 SW TD2	16	1	0	0	0	0	0	1	0	1			0	1	1	1			0	0	0	0
TD1 SW MAR	17	1	0	0	0	1	0	1	0	1			1			1			0	0	1	0
INC IN	18	1	0	0	1	0	0	1	0	1			1			0	1	0		0	0	1
DR MALS	19	1	0	0	1	1	1			1			1			1				0	0	0
ALS TD2	20	1	0	1	0	0	1			0	1	1	1			1				0	0	0
SEM FET	21	1	0	1	0	1	1			1			1			0	1	1		0	0	1
SEM STO	22	1	0	1	1	0	1			1			1			1				1	0	0
MALS TD1	23	1	0	1	1	1	1			1			1			0	1	0		0	0	0
TD2 SP ALS	24	1	1	0	0	0	0	1	1	1			1			1				1	0	0
TD1 SF ALS	25	1	1	0	0	1	0	1	0	1			1			0	1	0		0	0	1
FUNC MAR	26	1	1	0	1	0	1			1			1			1				0	0	1
MAR FUNC	27	1	1	0	1	1	1			1			1			1				0	0	1
MALS FUNC	28	1	1	1	0	0	1			1			1			1				0	0	1
ALS FUNC	29	1	1	1	0	1	1			1			1			1				1	0	0
FUNC MALS	30	1	1	1	1	0	1			1			1			1				0	0	1
FUNC TD1	31	1	1	1	1	1	0	1	0	1			1			0	1	0		0	0	1

T-FILE

ADDRESS		CONTENTS
A1	A0	
0	0	TI1
0	1	TI2
1	0	TD1
1	1	TD2



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A.L. Board
T-File Control
Functional Table

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The T - I-BUS Interconnection is divided in three logical blocks.

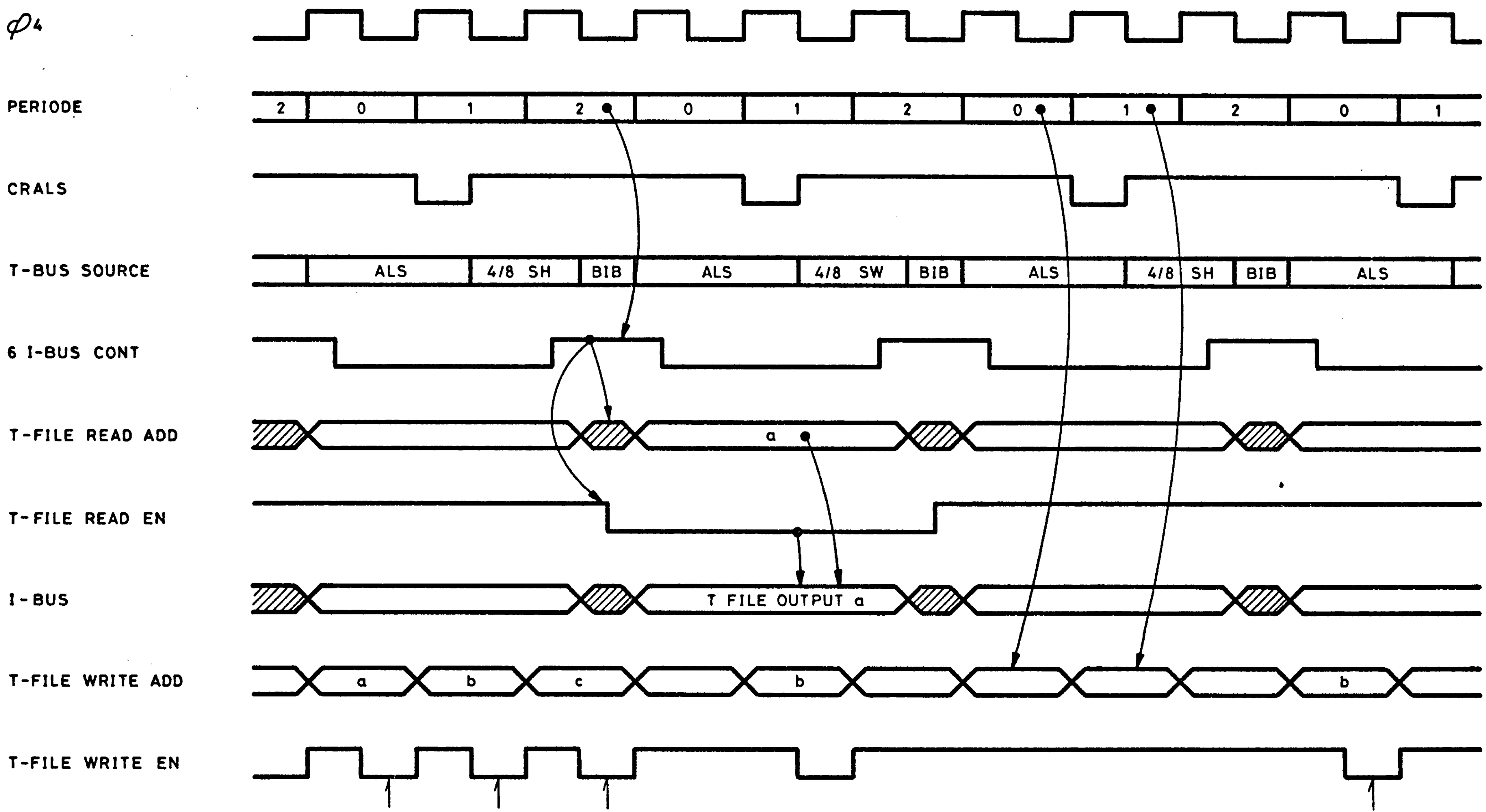
1.	T-File	L-TF-1
2.	4/8 Shift Selector	L-4/8SS-1
3.	T-File Control	L-TFC-1

4.1.1 T-File L-TF-1

The T-File consist of four 4 x 4 bit OC register files with the input connected to the T-BUS and the output connected to the I-BUS.
The input/output configuration is so that I-BUS 0 correspond to T-BUS 0 etc.
The read address and the output enable is controlled from the T-File Control in synchronous with the μ cycle while the input address and load pulse is synchronized to the multiplexed T-BUS.
Timing Diagram fig. 4.1.1 specify the read and write timing for the T-File.

T-File Address & Load Signals Timing Diagram

Fig. 4.1.1



ALS OUTPUT
→T-FILE
ADDRESS a

4/8 SHIFT
→T-FILE
ADDRESS b

BIB
→T-FILE
ADDRESS c

T-FILE REG a IS FEED
THROUGH THE 4/8 SHIFT
AND STORED IN T-FILE
ADD b

ALS OUT →
T-FILE ADD b

Reset Control Timing Diagram

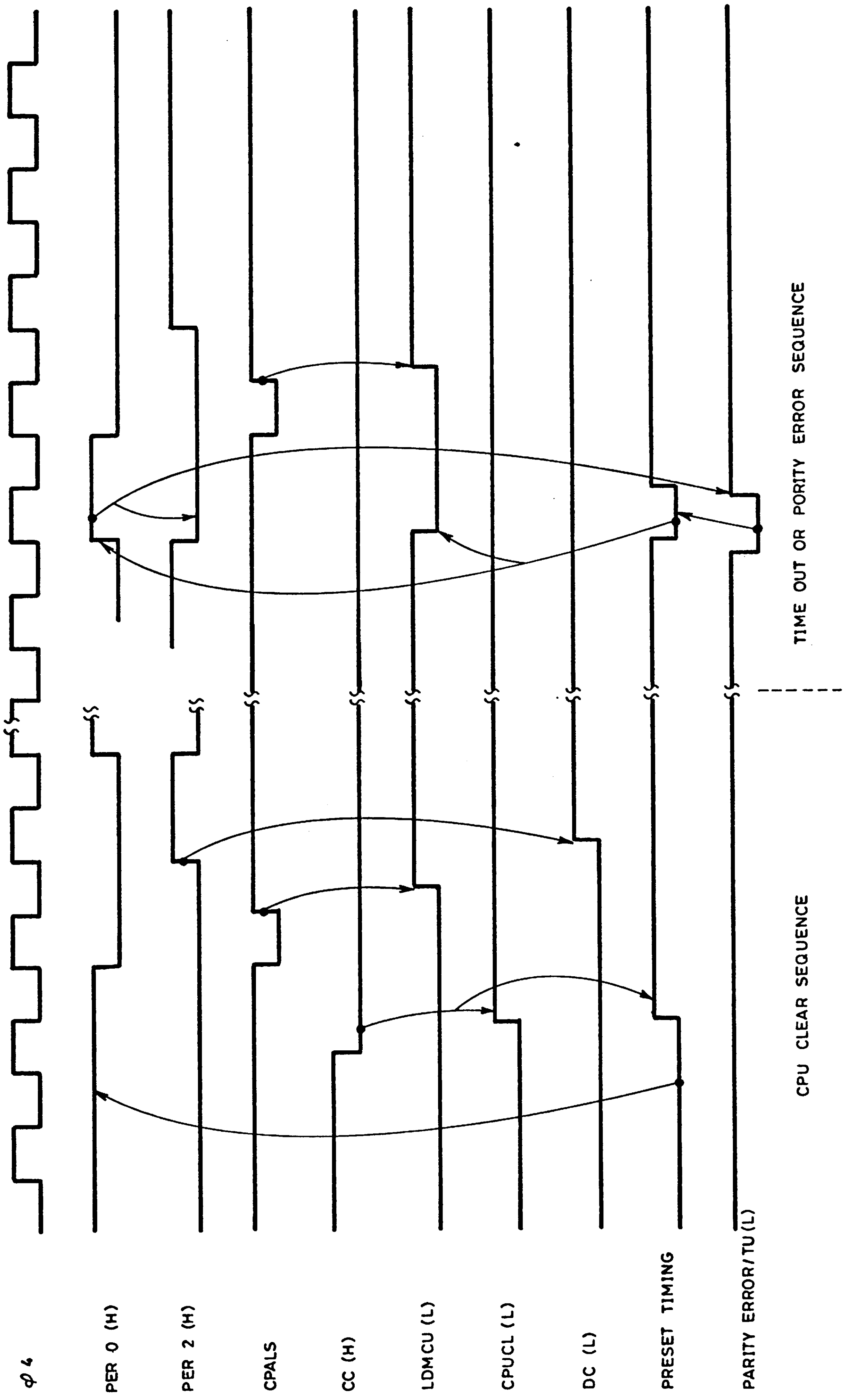


Fig. 4.1.2.

4.1.2 4/8 Shift Selector L-4/8SS-1

This logical blocks consist of four Quad 2 to 1 selectors with 3-state outputs connected to the T-BUS and enabled synchronous with the internal CPU timing ref. fig. 4.1.1.
The 2 x 16 bits input is connected so that the I-BUS is shifted left either 4 or 8 as shown in table 4.1.2.
The 4/8 shift is controlled from the T-File Control (SHIFT 8 (L).

Table 4.1.2
Shift Selector.

SHIFT8(L)	T-BUS															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8
1	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12

4.1.3 T-File Control L-TFC-1

Control of the T-File and the shift selector is carried out by means of a PROM and register circuit. The input to the two 32 x 8 PROM's is MDAT 16 - 20 from the MPB. 12 of the PROM outputs are stored in a register on the rising edge of the signal D PER0(H), and the outputs are selected in groups of four lines, synchronous with the timing signals D PER0 (H), PER1 (H) & PER2 (H) from the BIB to generate the three different address pattern used during one μ cycle for the T-File input address. Two of the four selected signals are stroped with 8 MHZ to give the correct address hold time for the T-File Load pulse LDT-File and the data register load pulse LD D-REG-

The four last outputs from the PROM's are latched on the signal GI BUS CONT (~delayed PER2 (H)) for controlling the I-BUS T-File read and enable and the SHIFT 8 (L).

Table 4.1.3 specify the PROM output selection scheme and fig. 4.1.3 specify the timing of the circuit and the PROM contents. The PROM tables for CR1296 & CR1297 are included in section 5.

TABLE 4.1.3

PER0	PER1	PER2	WAITF	WAOTF	LDT-FILE	LDD-REG	TBUS
1	0	0	R1.5	R2.6	$\overline{\text{R2.4}}$	R2.8	ALS
0	1	0	R1.8	R2.5	$\overline{\text{R2.1}}$	R2.2	4/8 SHIFT
0	0	1	R1.4	R1.3	$\overline{\text{R2.3}}$	R2.7	BIB
0	0	0	0	0	1	0	BIB

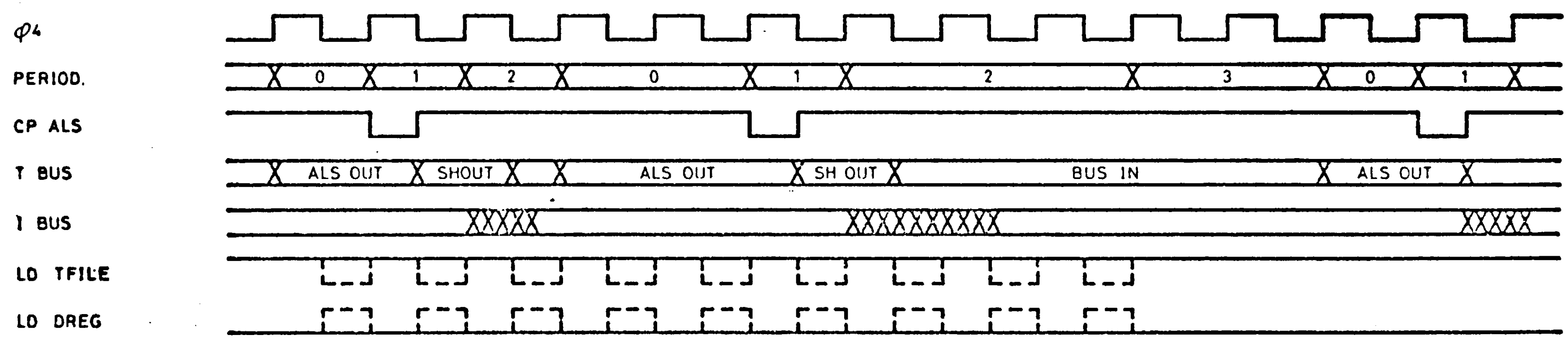
This condition is period 3 which is only used when the special func. instructions Func Mem is executed and the addressed memory is located on the CR80 Main Bus.

Fig. 4.1.3

FUNCTION	NO.	MDAT 20	MDAT 19	MDAT 18	MDAT 17	MDAT 16	T-FILE FUNCTIONS OUTPUT I-BUS REN (L)	RA1	RA0	INPUT∼T-BUS ALS OUT LD (L)	WA1	WA0	SHIFT OUT LD (L)	WA1	WA0	BUS IN LD (L)	WA1	WA0	SHIFT 4/8 (1/0)	D REG INPUT : T-BUS ALS OUT LD (H)	SHIFT OUT LD (H)	BUS IN LD (H)
BCNOP	0	0	0	0	0	0	1			1			1			1				0	0	0
FNI	1	0	0	0	0	1	0	0	1	1			0	0	0	0	0	1	0	0	0	0
INS1	2	0	0	0	1	0	0	0	0	1			1			1				0	0	0
TD1	3	0	0	0	1	1	0	1	0	1			1			1				0	0	0
INC OUT	4	0	0	1	0	0	1			1			1			1				1	0	0
ARSF TD1	5	0	0	1	0	1	0	0	0	1			1			0	1	0		0	0	1
TD2	6	0	0	1	1	0	0	1	1	1			1			1				0	0	0
INS1 FI	7	0	0	1	1	1	0	0	0	1			1			0	0	1		0	0	0
LAR	8	0	1	0	0	0	0	0	0	1			1			1				1	0	0
ALS TD1	9	0	1	0	0	1	0	0	0	0	1	0	1			1				1	0	0
FI	10	0	1	0	1	0	1			1			1			0	0	1		0	0	0
MAR TD1	11	0	1	0	1	1	0	0	0	1			1			0	1	0		0	0	1
ALS DR MAR	12	0	1	1	0	0	0	1	0	1			1			1				1	0	0
TI1 S8 TD1	13	0	1	1	0	1	0	0	0	1			0	1	0	1			0	0	0	0
TI1 S4 TD1	14	0	1	1	1	0	0	0	0	1			0	1	0	1			1	0	0	0
TD1 FI	15	0	1	1	1	1	0	1	0	1			1			0	0	1		0	0	0
TD1 SW TD2	16	1	0	0	0	0	0	1	0	1			0	1	1	1			0	0	0	0
TD1 SW MAR	17	1	0	0	0	1	0	1	0	1			1			1			0	0	1	0
INC IN	18	1	0	0	1	0	0	1	0	1			1			0	1	0		0	0	1
DR MALS	19	1	0	0	1	1	1			1			1			1				0	0	0
ALS TD2	20	1	0	1	0	0	1			0	1	1	1			1				0	0	0
SEM FET	21	1	0	1	0	1	1			1			1			0	1	1		0	0	1
SEM STO	22	1	0	1	1	0	1			1			1			1				1	0	0
MALS TD1	23	1	0	1	1	1	1			1			1			0	1	0		0	0	0
TD2 SP ALS	24	1	1	0	0	0	0	1	1	1			1			1				1	0	0
TD1 SF ALS	25	1	1	0	0	1	0	1	0	1			1			0	1	0		0	0	1
FUNC MAR	26	1	1	0	1	0	1			1			1			1				0	0	1
MAR FUNC	27	1	1	0	1	1	1			1			1			1				0	0	1
MALS FUNC	28	1	1	1	0	0	1			1			1			1				0	0	1
ALS FUNC	29	1	1	1	0	1	1			1			1			1				1	0	0
FUNC MALS	30	1	1	1	1	0	1			1			1			1				0	0	1
FUNC TD1	31	1	1	1	1	1	0	1	0	1			1			0	1	0		0	0	1

T-FILE

ADDRESS A1	A0	CONTENTS
0	0	TI1
0	1	TI2
1	0	TD1
1	1	TD2



CHRISTIAN ROVSING A/S

A.L. Board
T - File Control
Functional Table

Scale		Approved		Issue	1
Date	78 - 04 - 05	E		Date	78-04-05
Drawn	GB/LJA			Approved	
Parts no		3-1674			
Print no		Sheet 1 of 1 sheets			

4.2 PSW & Interrupt F-PSWI-1

All the circuit necessary for the process status word (PSW) and the control circuit for interrupt receiving are in F-PSWI-1. The input to PSW comes from the I-BUS for the S/W controller part, and the other bits comes from the H/W direct, e.g. the 3 bit CPU NO is from a 3 bit DIL switch. The control of the I/O interrupts, Timer & CPU and PSW is included in the F-PSWI-1 and consist of a 32 x 8 PROM with some of the outputs synchronized to the master timing by gates. The functional block consist of three logical blocks:

1.	PSW Interrupt Control	L-PIC-1
2.	Process Status Word	L-PSW-1
3.	PSW Driver	L-PD-1

4.2.1 PSW Interrupt Contol L-PIC-1

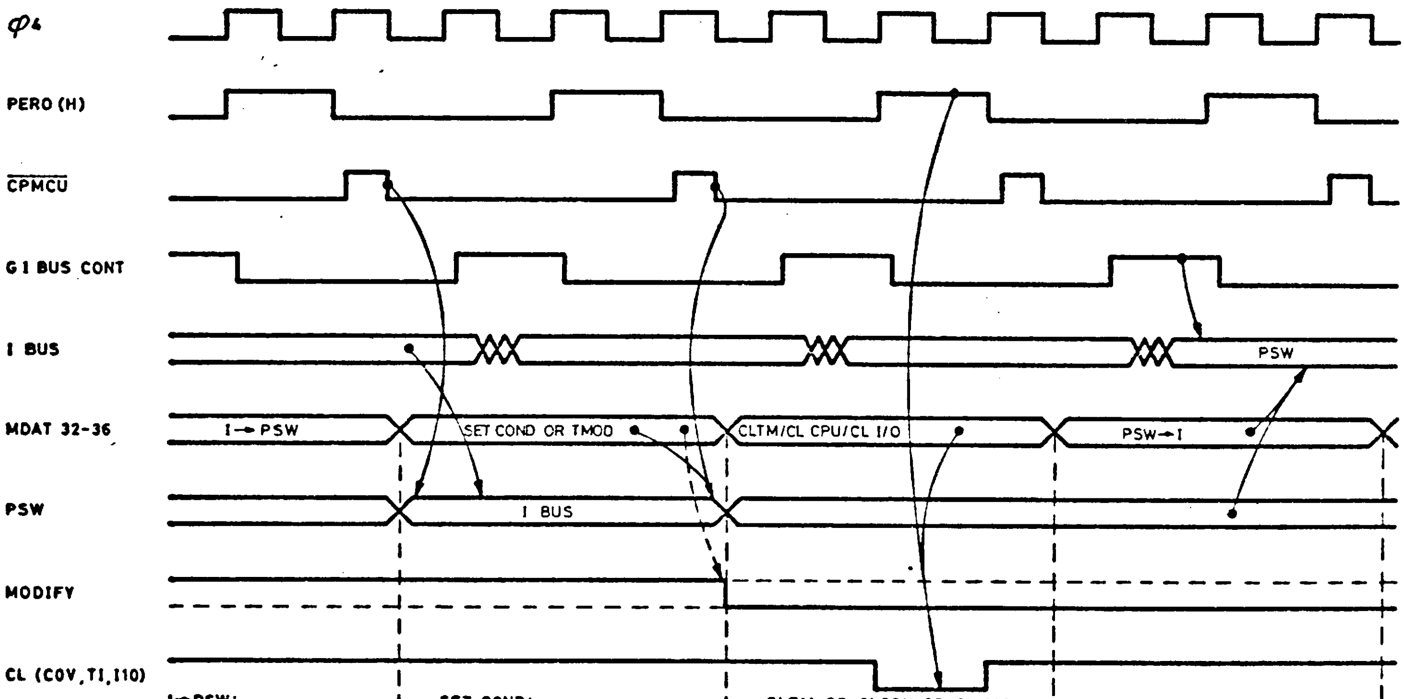
Input to the L-PIC-1 is u program lines MDAT 32 - MDAT 36 which also are used for controlling the OP register on MPB. These func signals are decoded by a 32 x 8 PROM CR1300 (ref. PROM tables section 5) and the output from CR1300 control loading of the PSW, transfer of the PSW, I-BUS and the modify and interrupt bits. Table 4.2.1 specify the functions and the timing for the signals derived from the PROM.

Table 4.2.1

FUNCTION	NO.	MDAT					PROM OUTPUTS								DESCRIPTION
		35	34	32	33	36	FORCE CPU INT (H)	SEL ARLD	EN MOD	SU EN PSW	INT CL 1	INT CL 0	G CPAR PSW	G CP PSW	
TMOD	4	0	0	1	0	0	0	1	1	1	1	1	1	0	TOGGLING OF THE MODIFY FLIP FLOP
CLTM	7	0	0	1	1	1	0	1	0	1	1	0	0	0	TIMER INTERRUPT FLIP FLOP IS CLEARED
CLCPV	9	0	1	0	0	1	0	1	0	1	0	0	0	0	CPU INTERRUPT FLIP FLOP IS CLEARED
CL I/O	11	0	1	0	1	1	0	1	0	1	0	1	0	0	I/O INTERRUPT FLIP FLOP IS CLEARED
SETCOND	14	0	1	1	1	0	0	1	0	1	1	1	1	0	ALS OUTPUT FLOGS ZERO OVERFLOW, CARRY & SIGN→PSW
CPUINT	16	1	0	0	0	0	1	1	0	1	1	1	0	0	TRANSFER OF CPU INTERRUPT TO ALL THE CPU's IN THE SYSTEM
I→PSW	18	1	0	0	1	0	0	0	0	1	1	1	1	1	PSW IS LOADED WITH THE I BUS EXCEPT THE CPU ADDRESS SWITCH
PSW→I	20	1	0	1	0	0	0	1	0	0	1	1	0	0	PSW IS TRANSFERED TO THE I BUS
NOT USED							1	1	1	1	1	1	1	1	THESE BITPATTERN MAY NOT BE USED
REMAINING							0	1	0	1	1	1	0	0	NO OP FOR THE PSW & INTERRUPT CIRCUIT

PSW CONTENTS

BIT NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TIMER MASK	CPU MASK	I/O MASK	TRANSFER ERROR	LOCAL INTERRUPT	CPU ADD 0	CPU ADD 1	CPU ADD 2	ALL ZEROR	SIGN	OVER FLOW	CARRY	PG 0	PG 1	PRI 1	PRI 0



I→PSW:
I BUS 0-7 &
I BUS 11-15
ARE LOADED INTO
THE CORRESPONDING
BITS IN PSW

SET COND:
PSW BITS 4-7 IS
UPDATED WITH THE
ALS STATUS
TMOD:
THE MODIFY BIT
IS TOGGLED

CLTM OR CLCPU OR CL I/O
A TAPE "0" ON
ONE OF THE SIGNALS
WILL RESET THE
CORRESPONDING INTERRUPT
BIT

PSW→I
THE CONTENTS OF
PSW IS TRANSFERED
TO THE I BUS

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A.L. Board
PSW & Interrupt Circuit
Functional Table

Scale		Approved		Issue	1
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Drawn	GB/LP			Approved	
Parts no		3-1679			
Print no		Sheet 1 of 1 sheets			

4.2.2 Process Status Word L-PSW-1

The PSW contain the 16 bits which constitute the CPU CR8001's status word. PSW and the control of it is specified in the table overleaf.
The timing specification for the PSW operation is specified in table 4.2.1

The priotity bits PRI0 & PRI1 are in the I/O interrupt circuit compared with the priority code from the interrupt present in the MBC, so that an interrupt only will be serviced if the PSW priority are less or equal to the MBC priority.

The page bits PG1 & PG0 are feed to the carry/page control circuit and used for to provide an off-set to the data addresses.

BIT NUMBER	NAME	load able	CONTROLLED BY	DESCRIPTION
15	Timer mask	Y	Software	High means: fast timer disabled
14	CPU mask	Y	Software	High means: CPU interrupts disabled
13	IO mask	Y	Software	High means: IO interrupts disabled
12	Time-out	Y	Hardware	Set when a time-out condition occurs
11	Local-int	Y	Firmware	Set when a local interrupt is generated
10	CPU NMB2	N	Hardware	CPU number. Set by switches
9	CPU NMB1	N	Hardware	
8	CPU NMB0	N	Hardware	
7	Z	Y	Firmware	The all zeroes condition of some arithmetic operations (1 = all zeroes).
6	S	Y	Firmware	The sign bit of the result of some arithmetic operations
5	V	Y	Firmware	The overflow condition of some arithmetic operations (1 means no overflow)
4	C	Y	Firmware	The carry of some arithmetic operations (1 means carry)
3 LSB	PGO	Y	Software	Page indication. Provides an off-set in multiples of 64K to data addresses PG1 is most significant.
2 MSB	PG1	Y	Software	
1 MSB	PRI1	Y	SOFTWARE	Process priority PRI 1 is most significant.
0 LSB	PRIO	Y	Software	

NOTE:
The only bits which cannot be controlled by a LOAP PSW instruction are 8,9,10.

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CR8001
PROGRAM STATUS WORD, PSW.

Scale		Approved	
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Drawn	JHØ		
Parts no		FIG 1	
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Issue	
Date	76
Approved	

The Z, S, V & C bits are feed to a selector together with the corresponding ALS output and used on the MPB for flag test. The selection of PSW or ALS as source is controlled from the MPB (PSW/ALS SEL). The bits can be updated from the I-BUS or the ALS.
The 3 bits CPU number is switch selectable, the address bit 0 is furthermore used for the authority control during Sub Bus transfer.

The local interrupt bit is set by the firmware, e.g. illegal instruction.

The three mask bits (Timer, CPU & I/O) will disable the corresponding interrupt in the interrupt circuit.

4.2.3 PSW Driver L-PD-1

The PSW Driver is open collector NAND gates for transferring the contents of PSW to the I-BUS.

4.3 Interrupt Control F-IC-1

Synchronization and masking of the incoming interrupt from the system (Timer, CPU & I/O) is carried out in this functional block. Treatment of the internal H/W generated interrupts, time out and parity error are also performed in F-IC-1 together with the carry/page control function.
The functions block is divided in the following three logical blocks.

1.	Parity & Time Out	L-P&TO-1
2.	Carry & Page Control	L-C&PC-1
3.	Interrupt Circuit	L-IC-1

4.3.1 Parity & Time Out L-P&TO-1

The data received from the CR80 main memory is checked for correct parity (ODD), and when data is transferred to the memory the parity is added to the data word when it is loaded from the T-BUS into the data register located on the BIB. When the communication is I/O the parity is not checked. If a parity error is recognized a pulse is transferred to the BIB and to a FF (Parity Error) is set. The signal will via the BIB reset the CPU by the signal LD MCU, and during the start up sequence a test of time out FF and parity error FF will be executed under control of the Carry & Page Control (TSE,PSE). The two FF's are reset when PSW is loaded. Timing diagram fig. 4.3.1 specify the L-P&TO-1 signal sequences.

Parity & Timing Out Timing Diagram

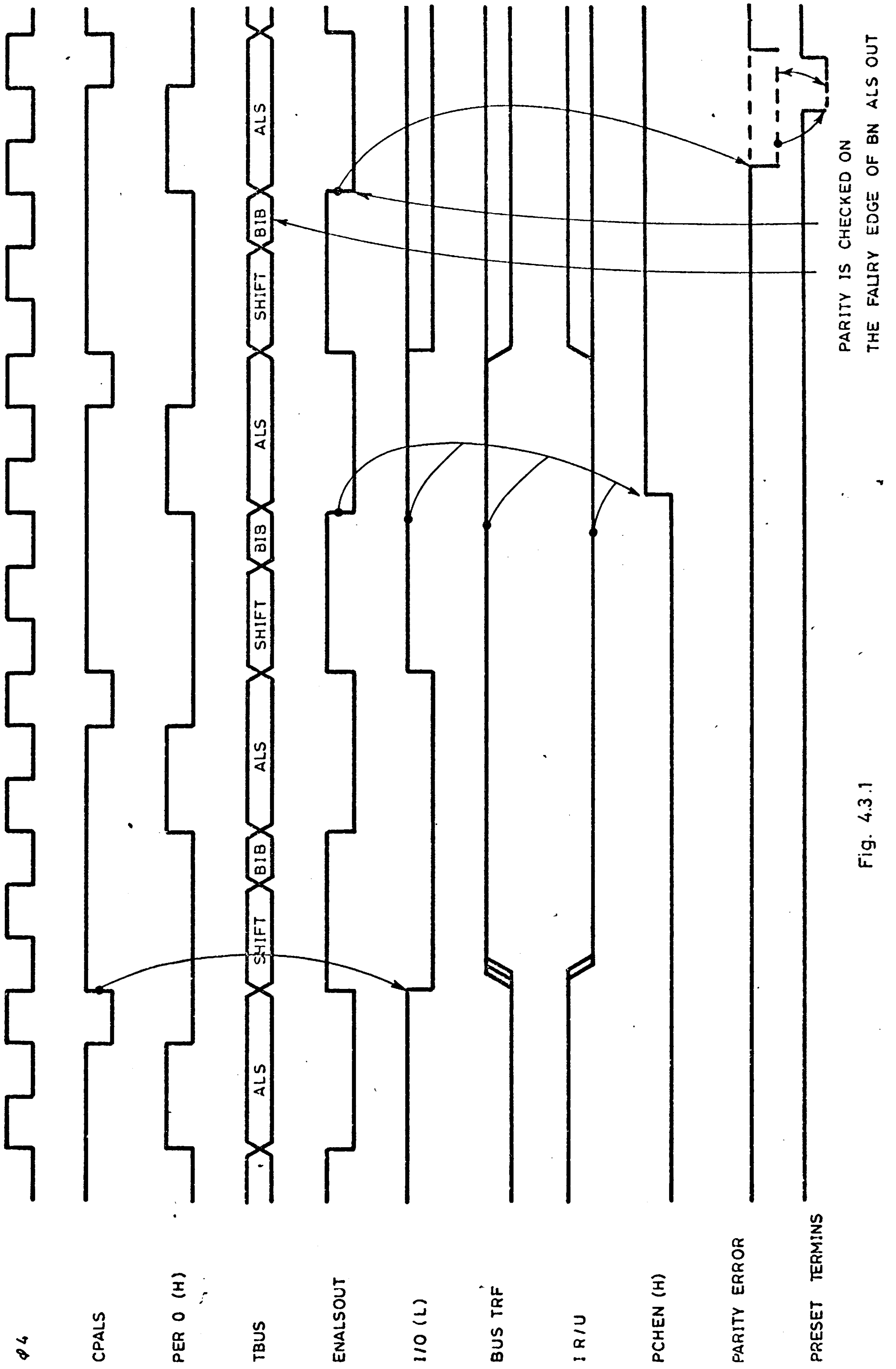


Fig. 4.3.1

4.3.2 Carry & Page Control L-C&PC-1

Control of the two page bits SEA16 and SEA17 used to specify which of the four 64 K word pages the data are located in, is carried out by a PROM CR1295 which control a dual 4 to 1 selector. For the contents of the 32 x 8 CR1295 ref. section 5 PROM tables.

The input carry to the ALS and the two signal used for selecting parity error/time out as test input for the MPB is controlled by CR1295 also.

Input to CR1295 are MDAT 21-23 and the carry stored in PSW (PSWC). Table 4.3.2 specify the function of L-C&PC-1.

TABLE 4.3.2

Carry & Page Control

FUNCTION	NO DEC	INPUT MDAT 21	22	23	PSUC	TIMEOUT (L)	SEA 17	SEA 16	CARRY IN
CPZ	0	0	0	0	0	TOVPE	OP1	OP0	1
CCP	1	0	0	1	0	TOVPE	PG1	PG0	1
PZ	2	0	1	0	0	TOVPE	0	0	0
CP		0	1	1	0	TOVPE	PG1	PG0	0
I/O		1	0	0	0	TOVPE	OP8	0	0
PSWCP		1	0	1		TOVPE	PG1	PG0	PSWC
TOF		1	1	1		PE	NA	NA	1

4.3.3 Interrupt Circuit

Storing and synchronization of the three interrupt timer, CPU & I/O to the first step of the instruction decoding (JZR(H): active) is performed in L-IC-1.

The timer interrupt signal from the BIB is used as clock for a FF and the FF is locked afterwards by a feed back from the Q output to the S input.
Reset of timer interrupt is controlled from L-PIC-1 ref table 4.2.1 or from the PSW Mask bit.
I/O interrupt is a combination of the PSW priority bits PRI0 & 1 and the interrupt queue status from the MBC module P0. P1 & INT (L).
The signal I/O INT(L) is active when the levels of PSW priority is less or equal to the MBC priority.
When the CPU access the Main Bus for fetching of the interrupt in the MBC, the interrupt condition is stored in a FF (I/O PENDING), because the interrupt could have been fetched from an other CPU. By testing the I/O pending the validity of the fetched interrupt is checked. I/O INT (L) is reset by the L-PIC-1 ref table 4.2.1 and the PSW mask bit.

When a CPU Interrupt is received a FF is cloked and the signal CPU I (L) goes active. The FF is cleared of the internal master clear signal DCL (L) because the PSW mask bit only gates the FF output without resetting the FF meaning that a CPU interrupt always will be serviced.

The three stored interrupts is synchronized to the internal timing by a latch enabled of GI BUS CUNI.
The signal DIS PRE (H) used by the MPB for start up of interrupt routine will be disabled if the preceding instruction was a modify (MODIFY (H)) if the

modify flag is passive DIS PRE (H) will be forced high by JZR, and one or more stored interrupts.

4.4 Arithmetical Logical Section F-ALS-1

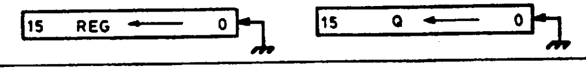
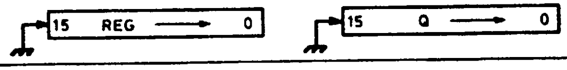
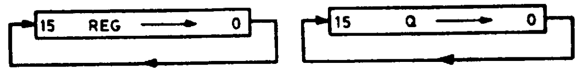
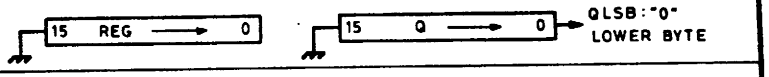
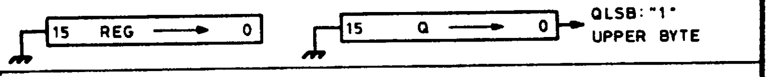
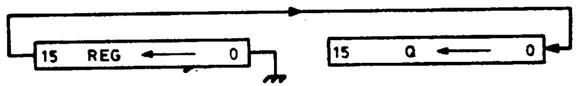
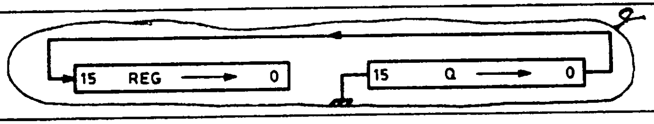
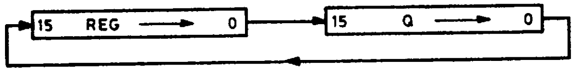
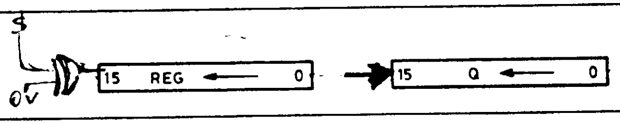
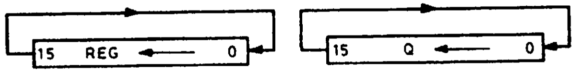
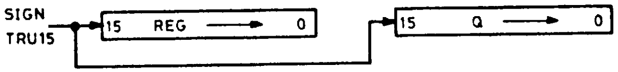
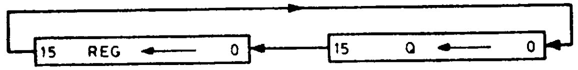
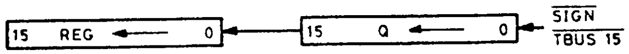
All the arithmetical , logical and shift operation are performed by the arithmetical logical section. There is to logical blocks in F-ALS-1.

1. Shift Control

2. Arithmetical Logical Section L-ALS-1

4.4.1 Shift Control L-SC-1

The four shift in/out to the ALL registers (RAM & Q) are set up controlled by the A address used for addressing of the ALS registers. Beside the shift function this logical block generate the two address mode bits IA18, IA19 used for specifying word byte/L byte/u & I/O. The two mode bits are clocked into two FF from the shift control PROM CR 1301 (PROM table ref section 5) on the rising edge of the ALU clock (CP ALS). When the contents of the address mode bits is different from word address ("1", "1") the clock pulse will be disabled. It means that the mode bits will stay stable during more µ cycles until a bus transfer occurs where they are reset, ref. table 4.4.1.
This set up scheme for I/O & byte addressing put restrictions on the addressing because it has to be set up and cycle before the bus transfer take place.
The four shift input are controlled by a 3-state selector circuit with the 3-state output controlled by the MDAT 5 which at the same time are used by the ALV to enable/disable the correspond shift out/in. The selection is carried out by CR1301.
For more details ref table 4.4.1.

FUNCTION	CR1301 INPUT GS01	AA1	AA0	AA3	AA2	IA19	IA18	LSB OR MSB DETERMINATED BY MDRT 5: 0~MSB, 1~LSB REG SHIFT IN	Q SHIFT IN	DESCRIPTION OF SHIFT CONTROL FUNCTION
LL	0	0	0	0	0	1	1	"0"	"0"	
RL	0	0	0	0	1	1	1.	"0"	"0"	
RC	0	0	0	1	0	1	1	SRL	SQL	
BYTE	0	0	0	1	1	1	0	"0"	"0"	
BYTE	1	0	0	1	1	0	1	"0"	"0"	
LLL	0	0	1	0	0	1	1	"0"	SRM	
RCL	0	0	1	0	1	1	1	SQL	"0"	
MUL	0	0	1	1	1	1	1	S⊕OV	SRL	
LC	0	1	0	0	0	1	1	SRM	SQM	
RA	0	1	0	0	1	1	1	SIGN	SIGN	
LCL	0	1	1	0	0	1	1	SQM	SRM	
DIV	0	1	1	1	0	1	1	SQM	$\overline{\text{SIGN}}$	
I/O	0	1	1	1	1	0	0	"0"	"0"	
										15 NA 0 15 NA 0

CHRISTIAN ROVSING A/S

A.L. Board
Shift Control
Functional Table

Scale		Approved	
Date	78 - 05 - 31	E	
Drawn	GB/LP		
Parts no		3-1678	
Print no		Sheet 1 of 2 sheets	

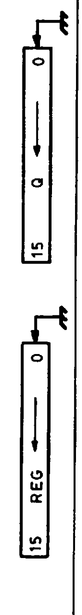
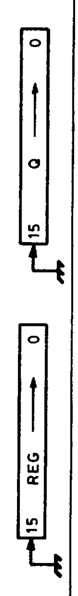
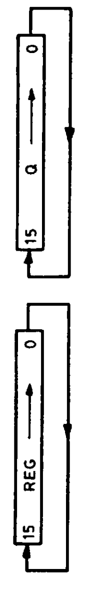
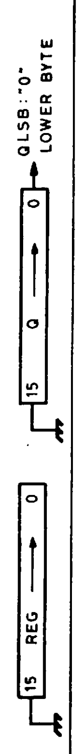
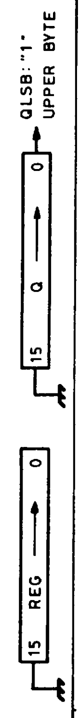
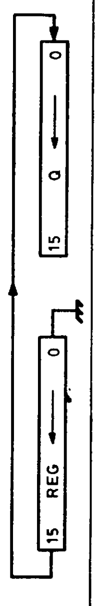
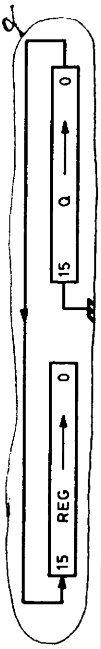
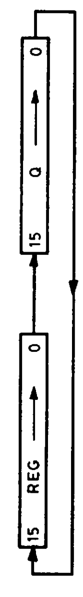
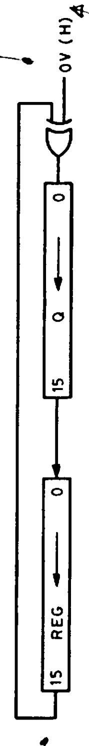
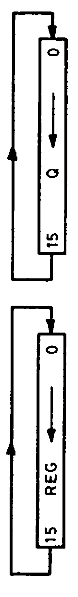
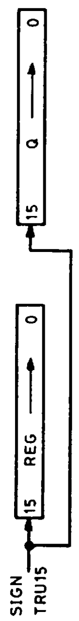
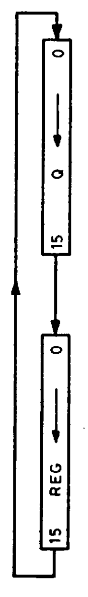
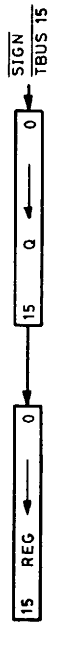
Issue	1
Date	78-05-31
Approved	

326.

GB 4 - Hafi

[illegible]

(H) Kuniro, June 1978

FUNCTION	CR1301 INPUT							LSB OR MSB DETERMINATED BY MDRT 5: 0~MSB, 1~LSB		DESCRIPTION OF SHIFT CONTROL FUNCTION
	GS01	AA1	AA0	AA3	AA2	IA19	IA18	REG SHIFT IN	Q SHIFT IN	
LL	0	0	0	0	0	1	1	"0"	"0"	
RL	0	0	0	0	1	1	1	"0"	"0"	
RC	0	0	0	1	0	1	1	SRL	SQL	
BYTE	0	0	0	1	1	1	0	"0"	"0"	 QLSB: "0" LOWER BYTE
BYTE	1	0	0	1	1	0	1	"0"	"0"	 QLSB: "1" UPPER BYTE
LLL	0	0	1	0	0	1	1	"0"	SRM	
RCL	0	0	1	0	1	1	1	SQL	"0"	
MUL	0	0	1	1	1	1	1	S⊕OV	SRL	
LC	0	1	0	0	0	1	1	SRM	SQM	 OV (H)
RA	0	1	0	0	1	1	1	SIGN	SIGN	
LCL	0	1	1	0	0	1	1	SQM	SRM	 SIGN TRU15
DIV	0	1	1	1	0	1	1	SQM	$\overline{\text{SIGN}}$	
ILO	0	1	1	1	1	0	0	"0"	"0"	 $\overline{\text{SIGN}}$ TBUS 15

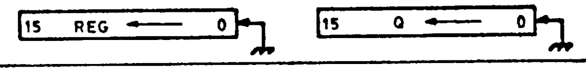
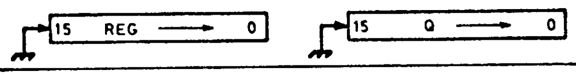
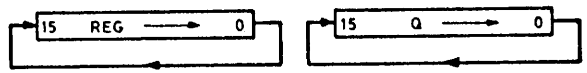
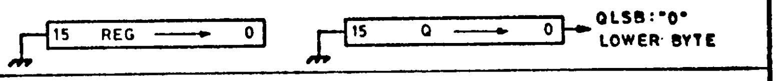
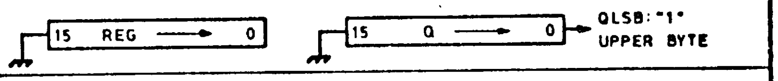
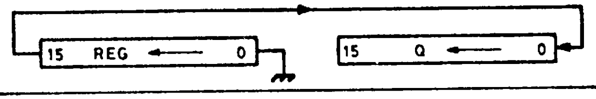
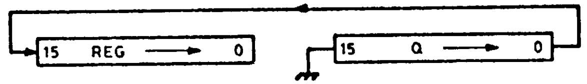
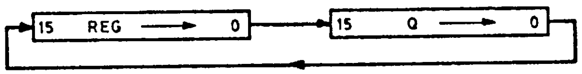
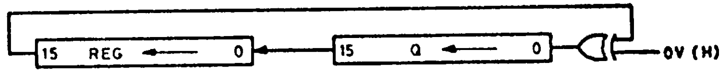
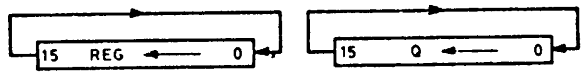
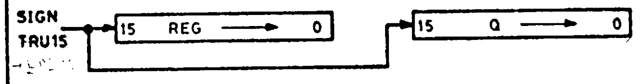
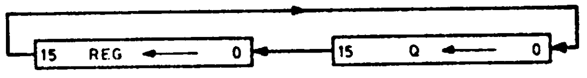
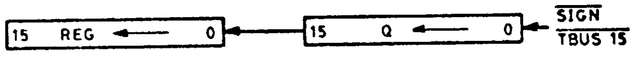
CHRISTIAN ROVSING A/S

A.L. Board
Shift Control
Functional Table

Scale		Approved	
Date	78 - 05 - 31	E	
Drawn	GB/LP		
Parts no		3-1678	
Print no		Sheet 1 of 2 sheets	

Issue	1
Date	78-05-31
Approved	

Table 4.4.1

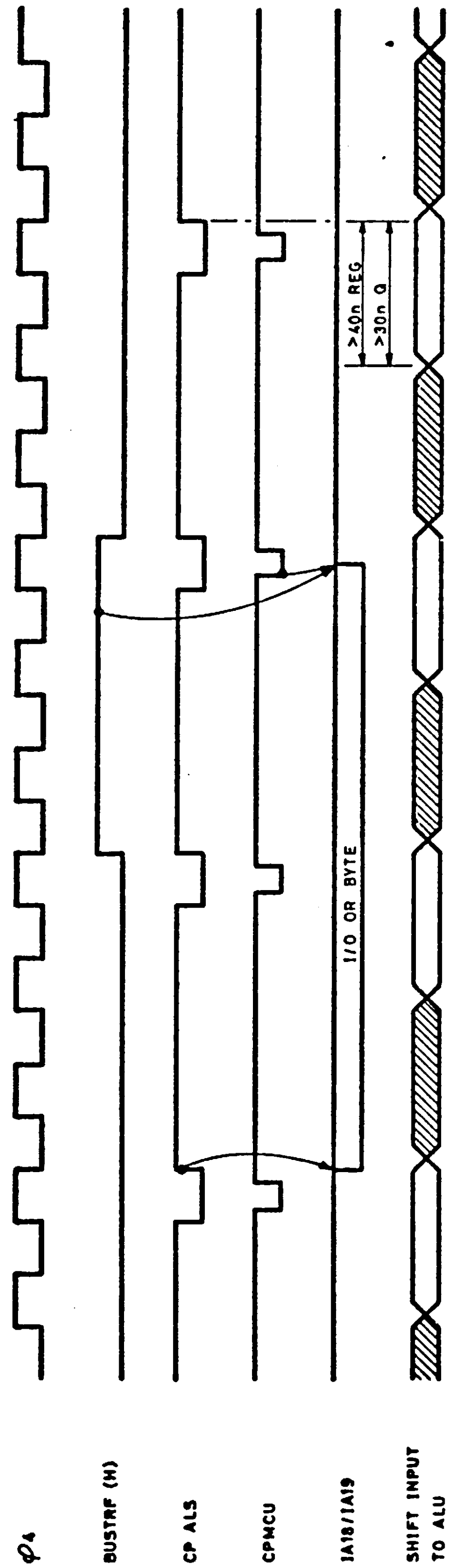
FUNCTION	CR1301 INPUT							LSB OR MSB DETERMINATED BY MORT 5: 0~MSB, 1~LSB		DESCRIPTION OF SHIFT CONTROL FUNCTION
	GS01	AA1	AA0	AA3	AA2	IA19	IA18	REG SHIFT IN	Q SHIFT IN	
LL	0	0	0	0	0	1	1	"0"	"0"	
RL	0	0	0	0	1	1	1	"0"	"0"	
RC	0	0	0	1	0	1	1	SRL	SQL	
BYTE	0	0	0	1	1	1	0	"0"	"0"	 QLSB: "0" LOWER BYTE
BYTE	1	0	0	1	1	0	1	"0"	"0"	 QLSB: "1" UPPER BYTE
LLL	0	0	1	0	0	1	1	"0"	SRM	
RCL	0	0	1	0	1	1	1	SQL	"0"	
MUL	0	0	1	1	1	1	1	S0OV	SRL	
LC	0	1	0	0	0	1	1	SRM	SQM	 OV (H)
RA	0	1	0	0	1	1	1	SIGN	SIGN	
LCL	0	1	1	0	0	1	1	SQM	SRM	 SIGN TRU15
DIV	0	1	1	1	0	1	1	SQM	$\overline{\text{SIGN}}$	
ILO.	0	1	1	1	1	0	0	"0"	"0"	 $\overline{\text{SIGN}}$ TBUS 15
										15 NA 0 15 NA 0

CHRISTIAN ROVSING A/S

A.L. Board
Shift Control
Functional Table

Scale		Approved		Issue	1
Date	78 - 05 - 31	E		Date	78-05-31
Drawn	GB/LP			Approved	
Parts no		3-1678			
Print no		Sheet 1 of 2 sheets			

Table 4.4.1



CHRISTIAN ROVSING A/S

A.L. Board
Shift Control
Functional Table

Scale		Approved		Issue	1
Date	78 - 06 - 01	E		Date	78-06-01
Drawn	GB/LP			Approved	
Parts no		3-1678			
Print no		Sheet 2 of 2 sheets			

4.4.2 Arithmetical Logical Section L-ALS-1

The arithmetical and logical operations in the CPU CR8001 are performed by four MM6701 chips with a carry load ahead generator for improving of the cycle time to 375 ns.
The 16 bits input word is the I-BUS and the output is the T-BUS the function control is carried out from the MPB µ program direct for the 8 bit instruction bys MDAT 0-7 and indirect via the address selectors for the register A- and B addressing located on the MPB too.
The following data sheets specify the ALU chips.

4-BIT EXPANDABLE BIPOLAR MICROCONTROLLER

5701/6701

Monolithic Memories
INCORPORATED

KNUD KAMUK A/S
Bredebovej 31 . 2800 Lyngby
☎ (02) *88 33 33

	MILITARY	COMMERCIAL
5701	X	
6701		X

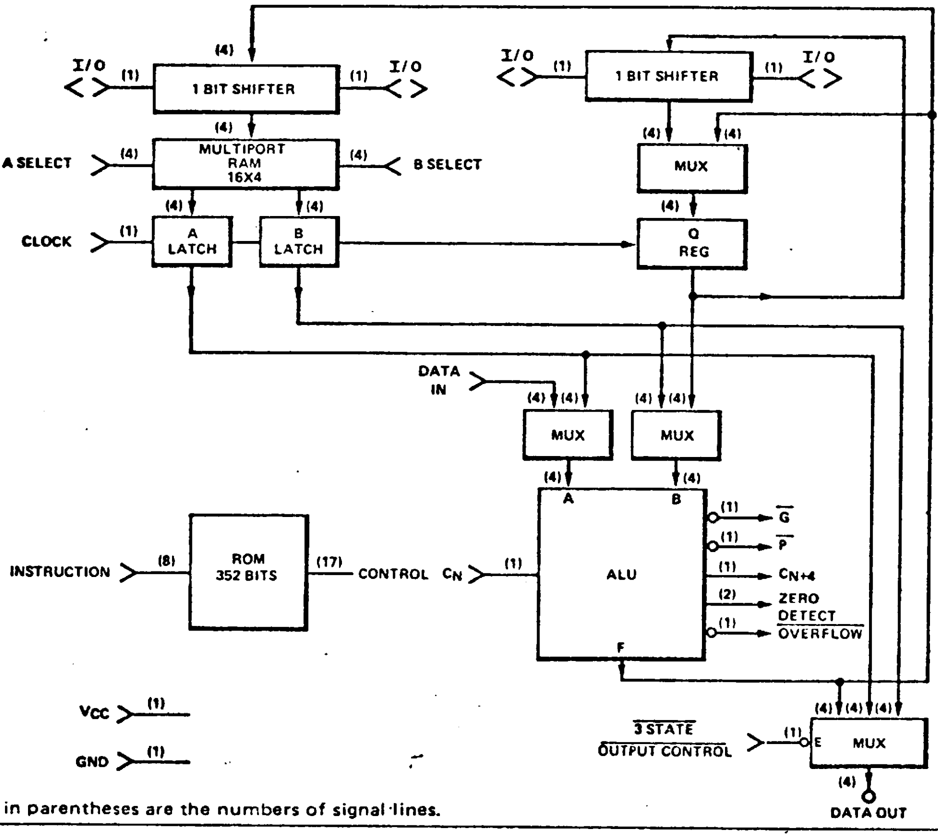
PRODUCT FEATURES

- Complete 4-Bit Bipolar LSI Processor Slice on a Single Chip.
- Replaces 25 TTL MSI Packages and Saves 5.5 Watts.
- 1000 Gate Complexity Schottky LSI – Single Layer Metal.
- 36 Instructions – Arithmetic, Logic, and Shifting Capability with Overflow Detection. Active High or Active Low Logic.
- 16 Directly Addressable, Two-Port, General Purpose Accumulators – Full 2 Address Capability, Some 3 Register Operations
- A Separate Q-Register Useful as a Scratchpad or Accumulator Extension. Direct Data in and Accumulator Operations.
- Separate Low Fan in Input Bus and 3 State Output Bus.
- Expandable to Handle N Bit Words with Full Carry Look-Ahead.
- 175 ns Cycle (6701) Which Can Perform Multiple Nanoinstructions such as Subtract, Shift, and Store in One Cycle.

APPLICATIONS

- The Ideal Product for Upgrading or Replacing Existing Central Processing Units and Maintaining the Existing Software. The 5701/6701 can be Microprogrammed to Efficiently Emulate (Simulate) Most Machines.
- Hard Wired Controllers – Tape and Disk Controllers – Data Concentrators.
- Point of Sale Terminals, Special Purpose Processors.
- Process and Machine Control.
- Word Processing and Navigation Systems.
- Intelligent Terminals and Game Machines.
- Traffic Control and Communications Systems.
- Upgrade Systems Using the 74181, 9340, 9341, 74S281 Arithmetic Logic Units

BLOCK DIAGRAM – 5701/6701



Note: The numbers in parentheses are the numbers of signal lines.

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

OCTOBER 1975

EXPANDABLE 4 BIT SLICE — 40 PIN PKG.

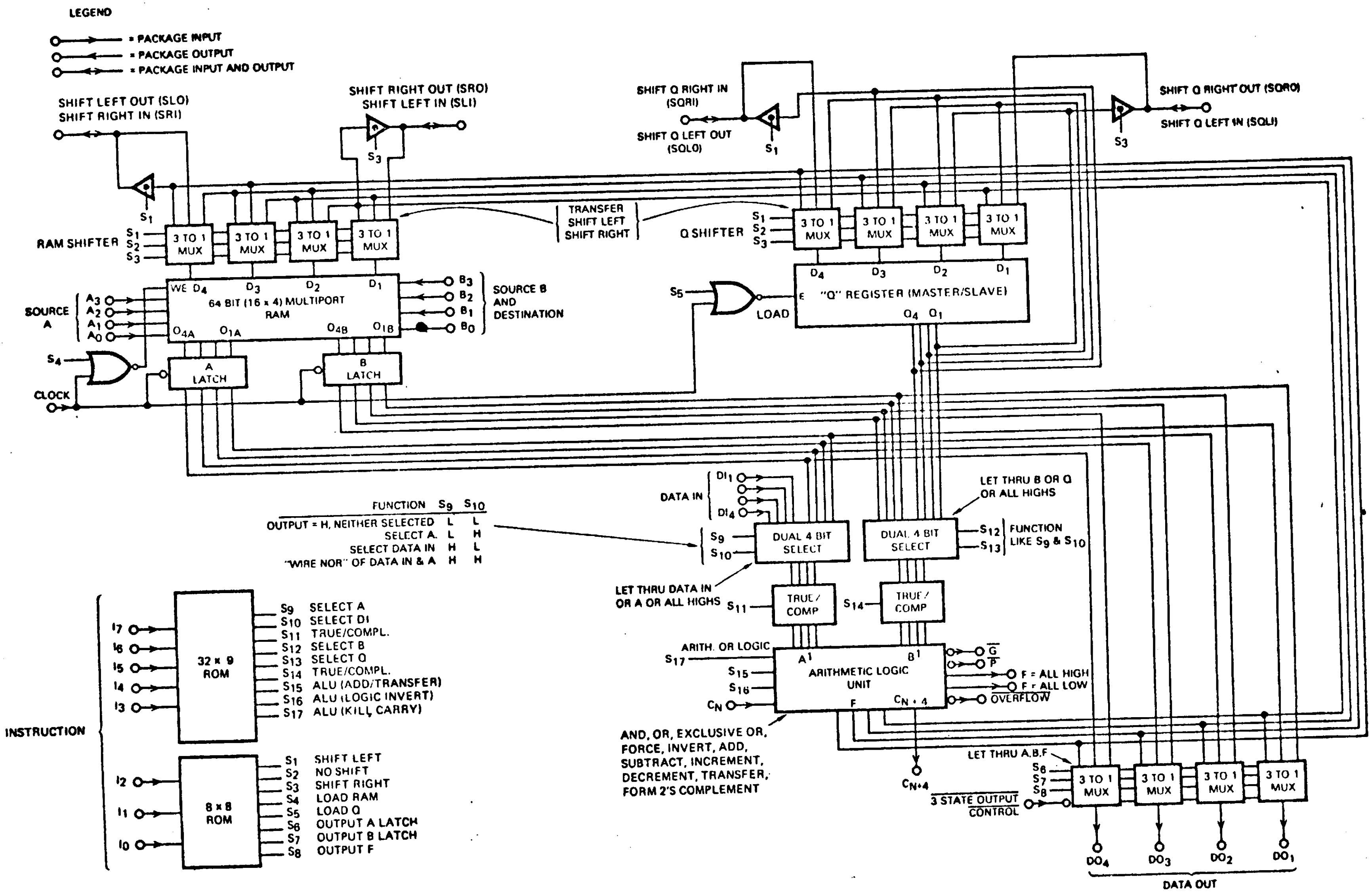


Figure 1

I. INTRODUCTION

GENERAL DESCRIPTION

The 5701/6701 is designed to be used as a 4-bit processor slice of a conventional central processing unit (C.P.U.). It can also be used in peripheral controllers, (tape, disk, etc.,) or as the heart of a microprocessor, terminal, or computer. It is a single chip bipolar LSI device which replaces more than 1000 TTL gates.

The two address capability (ability to work on two accumulators at once) and the powerful nano-instructions permit design of sub 1 microsecond cycle time hard wired C.P.U.'s or efficient emulation (imitation) of conventional machines using off chip ROMs for microprogramming.

The 5701/6701 will handle the data flow section of most computers since it is expandable to handle any word length in increments of 4 bits without significant speed degradation (look-ahead outputs are available). The 16 on-chip general purpose accumulators implement the type of C.P.U. usually found only in high performance top of the line 16-bit minicomputers or 24 or 32-bit computers. It can be thought of as a general purpose 4-bit register and arithmetic logic unit with a separate A operand, B operand, data-in, and data-out ports. Additional accumulators or registers if required can be added with off chip packages tied to the data in pins.

B) TTL EQUIVALENT

The 5701/6701 is similar in function to the 25 TTL MSI packages listed below. It saves 375 I/O pins, 5.6 watts and 30 square inches of board area.

TABLE 1

Function	TTL#	#14 Pin or #16 Pin Pkgs.	#24 Pin Pkgs.	Advertised Gate Complexity (Each Pkg.)	Gate Complexity Total	Typical Power Each (Watts)	Total Power (Watts)
32 x 9 & 8 x 8 ROMs	7488	3		70	210	.50	1.50
16 x 4 Multiport RAM	74172		4	110*	440	.56	2.24
Arithmetic Logic Unit	74181		1	75	75	.55	.55
Storage Latches	7475	2		28	56	.16	.32
J-K Flip Flop (Q Reg)	74107	2		22	44	.10	.20
4 to 1 MUX	74153	6		16	96	.20	1.20
O/I True Complement	74H87	2		18	36	.27	.54
Dual 4 Bit Select	74157	2		15	30	.15	.30
Quad 2 to 1 MUX with 3 State Outputs	74S257	2		15	30	.30	.60
3 State Buffer	DM8094	1		5	5	.18	.18
Totals		20	5		1022		6.63

*The 74172 is advertised at 201 gate complexity but we are using only 2 of the 3 address capability, hence we have counted it as 110 gates.

C) PROCESS AND PACKAGING

The 5701/6701 is manufactured by an advanced Schottky bipolar single layer metal process. The chip requires only 5 volts and ground and all inputs and outputs are totally TTL compatible. The chip is packaged in a standard 40-pin dual in-line ceramic package.

D) POWER

The chip is designed to dissipate maximum power at low temperature. The power is minimum at high temperature. This feature permits full military range parts and easier power supply design.

E) PERFORMANCE

A single 5701/6701 can execute one instruction every 175ns (230ns for the 5701). The instructions are more complex than normal micro-instructions permitting multiple operations in one cycle without timing problems.

II. OPERATION — See Figure 1 — Expandable 4-Bit Slice

A) BLOCK DIAGRAM

A detailed block diagram of the chip is shown in Figure 1. Note the legend used in the upper left hand corner for package inputs and outputs. The logic and control ones are shown as they are implemented on the chip even though fewer control inputs might be required by discrete logic devices. The dual 4-bit selects, at the input to the arithmetic logic unit, for example, have two "S" input control lines rather than the 74157 TTL equivalent which has one control line for letting through the left four bits or the right four bits on the output 4 bits.

B) ROM (LOWER LEFT CORNER)

Two on chip ROMs (352 bits total) are used to translate the eight (8) instruction lines I_O to I_7 into 17 on chip control lines (labelec S_1 through S_{17}) which open and close data paths required to execute an instruction.

C) MULTIPORT RAM (UPPER LEFT CORNER)

A 16 word by 4 bit multiple port memory is used to fetch two operands at the same time. The RAM is double decoded (4 A address pins and 4B address pins and has one set of 64 storage cells). We could, for example, read from 0101 on the A address (file #5) and read from 0001 on the B address (file #1) at the same time. The B side of the RAM can be read out or written into independent of the address on the A side. The A side can only be read. The RAM must be loaded via the B side. The RAM, if it is enabled, is loaded when the clock is low. The duration of time the clock is low, is the write enable pulse width required to switch the RAM. If the clock is held high, operations can be performed and the results examined, but no results are stored.

D) LATCHES (CENTER LEFT)

The latches on the RAM outputs are the zero delay type (like 7475) which let the data into the latches appear on the latch outputs until the clock goes low and then hold the data. The latches permit parallel accessing of the RAM and ROM without two delays (one for the ROM and one for the RAM), since the access time of the ROM is masked by the delay through the RAM. The latches eliminate race conditions when the RAM data is fetched and updated in one cycle.

E) ARITHMETIC LOGIC UNIT (LOWER CENTER)

Input multiplexers into the arithmetic logic unit (A.L.U.) under ROM control permit the entry of data in or the A channel of the RAM into the A port of the ALU, and the B channel of the RAM or the Q register into the B port of the ALU.

The ALU is of the conventional type except 0/1 true complement elements have been put in the input ports permitting the realization of a totally symmetrical ALU (i.e., A minus B or B minus A). Overflow detection and two zero detect pin (one for positive and one for negative logic) are also included.

F) OUTPUT MULTIPLEXERS (LOWER RIGHT HAND CORNER)

The 3 to 1 output multiplexers under ROM control let through the ALU output, the A latch output, the B latch output on the data out pins. The output multiplexers are three-state outputs controlled by the three-state output control pin. The three-state outputs permit processing to be performed in the 5701/6701 without tying up the data out bus and allow one bus system to tie 5701/6701 data in pins to data out pins. The outputs are enabled when the three-state enable pin is low.

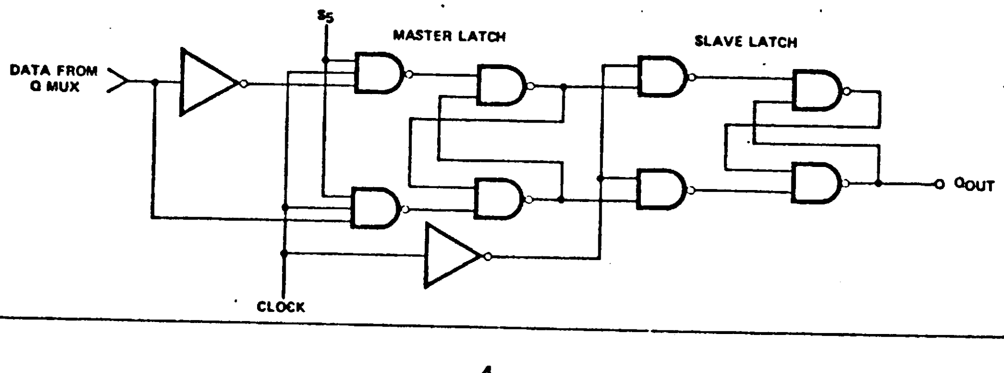
G) SHIFT MULTIPLEXERS (UPPER LEFT AND UPPER RIGHT)

The four 3 to 1 mux's on top of the Q register permit the ALU output bus F to be loaded into the Q register. The Q register can also be shifted on itself one place left or right. The four 3 to 1 multiplexers above the RAM permit a transfer or 1 bit left or right shift of the F bus before storage in the RAM. Both the RAM shifter and the Q shifter employ bi-directional shift in/shift out pins to permit expansion to more than 4 bits.

H) Q REGISTER (UPPER RIGHT)

The Q register can function as an accumulator extension register. It would normally be used to hold the least significant half of the double length product of a multiplication or as a storage register to catch the bits shifted off the beginning or end of a word during left or right shifting. In this mode of operation, the shift out pin of the least significant bit of the RAM shifter would be tied to the shift in pin of the most significant bit of the Q register. The Q register can be shifted on itself or be loaded from the ALU bus. The Q shift control pins are in common with RAM shift controls permitting simultaneous RAM and Q shifting. It can also be used as a program counter or scratchpad.

The Q register is a master slave flip-flop. Data is loaded into the master while the clock is low (assuming it is enabled by the ROM) and transferred from the master to the slave when the clock goes high. The Q register is not an edge-triggered latch. Whatever data is present before the clock goes high (assuming the setup time is obeyed) will be loaded into Q. If the clock is held high operations can be performed but no results are stored.



III. PACKAGE PINS

Figure 2 shows a listing of the 40 pin I/O. The 5701/6701 uses a standard 40 lead ceramic dip approximately 2.00 inches long and 0.60 inch wide. See Figure 3 for the package details. NOTE THAT V_{CC} AND GROUND ARE NOT ON THE CONVENTIONAL END PINS. This was necessary because the package current would produce too high a voltage drop in the package lead resistance out to the end pins to meet the V_{OL} requirements.

PIN CONFIGURATION

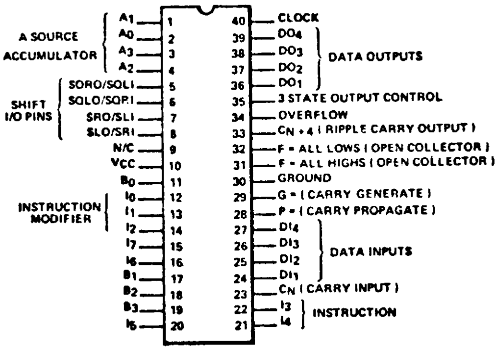


Figure 2.

PACKAGE OUTLINE

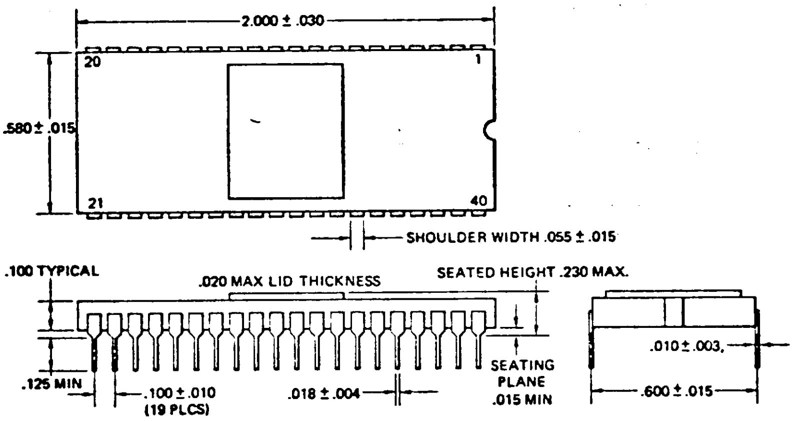


Figure 3.

40 Pin Ceramic (Side Braze)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 35° C/watt

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20° C/watt

BURN-IN CIRCUIT

The circuit in Figure 4 below puts the device in an instruction where the state of all outputs is known. Any other set of levels on the inputs may result in undefined output states and possible damage to the device under burn-in conditions. The other instructions involve the use of internal register whose initial conditions, after power-up, are undefined. The burn-in circuit shown comes closest to the usual reverse burn-in circuits of logic devices. The unit is in the force LLLL mode with the shift I/O pins disabled, the data outputs disabled, and with a single accumulator always selected.

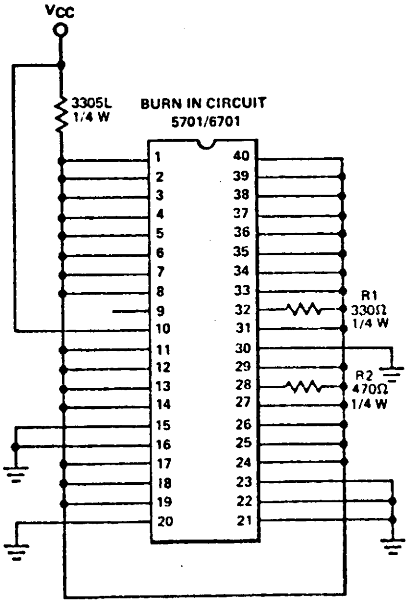


Figure 4.

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.5 to 7.0 V
Input Voltage	-1.0 to 5.5 V
Output Current	100 mA
Input Current	-20 to 5 mA
Storage Temperature	-65 to +150 C

Stresses above or extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.

D.C. CHARACTERISTICS – Unless otherwise indicated, all limits for the 6701 are guaranteed for 5 V ± 5% in a free air temperature of 0 to 75°C; all limits for the 5701 are guaranteed for 5 V ± 10% in a free air temperature of -55° to 125°C.

PARAMETER	DEVICE PINS	CONDITIONS	5701			6701			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F Input Load Current	Any A, B, or I	V_{CC} = Max, V_F = .45 V			-250			-250	µA
	Clock or $\overline{\text{3 State Control}}$	V_{CC} = Max, V_F = .45 V			-250			-250	µA
	Shift I/O & Data In	V_{CC} = Max, V_F = .45 V			-0.80			-0.80	mA
	C_N	V_{CC} = Max, V_F = .45 V			-4.80			-4.80	mA
I_R Input Leakage Current	Any A, B, or I	V_{CC} = Max, V_R = 2.40 V			40			25	µA
	Clock or $\overline{\text{3 State Control}}$	V_{CC} = Max, V_R = 2.40 V			40			25	µA
	Shift I/O .	Used as an Input			100			100	µA
	Data Inputs	Used as an Input			20			20	µA
	C_N	Used as an Input			120			120	
I_{RB} Input Leakage Current	Any A, B, or I	V_{CC} = Max, V_{RB} = 5.50 V			1.0			1.0	mA
	Clock or 3 State Control	V_{CC} = Max, V_{RB} = 5.50 V			1.0			1.0	mA
	Shift I/O	V_{CC} = Max, V_{RB} = 5.50 V			1.0			1.0	mA
	Data Input	V_{CC} = Max, V_{RB} = 5.50 V			1.0			1.0	mA
	C_N	V_{CC} = Max, V_{RB} = 5.50 V			1.0			1.0	mA
V_{OL} Low Level Output Voltage	Data Outputs, $\overline{G}$,	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.50	V
	C_{N+4}, F = All High, F = All Low $\overline{P}$, Overflow	V_{CC} = Min, I_{OL} = 10 mA		0.35	0.50		0.35	0.50	V
	Shift I/O	V_{CC} = Min, I_{OL} = 3.2 mA Used as an Output		0.35	0.50		0.35	0.50	V
I_{CC} Power Supply Current	V_{CC}, Grd	All inputs ground (worst case), All Outputs Open, Shift I/O Open Temp = Max		215	250		215	250	mA
		All inputs ground (worst case), All Outputs Open, Shift I/O Open Temp = Min		230	280		230	280	mA
V_{IL} Low Level Input Voltage	All Inputs and Shift I/O	V_{CC} = 5.00 V			0.80			0.80	V
V_{IH} High Level Input Voltage	All Inputs and Shift I/O	V_{CC} = 5.00 V	2.0			2.0			V
V_{IC} Input Clamp Voltage	All Inputs and Shift I/O	V_{CC} = Min, I_{IC} = -5.0 mA		-1.0	-1.5		-1.0	-1.5	V
I_{CEX} Output Leakage Current	All Outputs and Shift I/O	V_{CC} = Max, V_{CEX} = 2.40 V, High Stored or Disabled			100			100	µA
		V_{CC} = Max, V_{CEX} = 0.45 V Disabled			-100			-100	µA
I_{CEXB} Output Leakage Current	All Outputs and Shift I/O	V_{CC} = Max = V_{CEXB} High Stored or Disabled			1			1	mA
I_{SC} Output Short Circuit Current	DO_1, DO_2, DO_3, DO_4, $\overline{G}$, $\overline{P}$, $\overline{OVFL}$	V_{OUT} = 0 V, V_{CC} = 5 V Only one Output at a time should be Shorted	5	15	90	5	15	90	mA
V_{OH} Output Voltage "High"	DO_1, DO_2, DO_3, DO_4, $\overline{G}$, C_{N+4}	I_O = -3.2 mA, V_{CC} = Min High Stored	2.4	3.5		2.4	3.5		V
	Shift I/O, $\overline{P}$, $\overline{OVFL}$	I_O = -500 µA, V_{CC} = Min High Stored	2.4	3.5		2.4	3.5		V
C_I Input Capacitance	All Inputs	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		8			8		pF
C_O Output Capacitance	All Outputs	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz		8			8		pF

[1] Typical values are measured at 5.0 V and 25°C.

A.C. CHARACTERISTICS*

PARAMETER	SYMBOL/CONDITIONS	TIME IN NANOSECONDS					
		5 V ± 10% -55° TO 125°C 5701			5 V ± 5% 0° TO 75°C 6701		
		MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.
Delay from RAM Address (A_N or B_N) to	Figure 5A Clock High						
$\overline{G}$			85	130		85	100
$\overline{P}$			85	130		85	100
C_{N+4}			95	140		95	110
Zero Detect			120	170		120	140
$\overline{\text{Overflow}}$			100	155		100	125
RAM Shifter Outputs			110	165		110	135
Data Outputs (bypass ALU)	T_{C1}	20	85	130	20	85	100
Data Outputs (through ALU)	T_{AA}	40	110	170	40	110	140
Delay from Instruction Input (I_N) to	Figure 5A						
$\overline{G}$			55	95		55	75
$\overline{P}$			55	95		55	75
C_{N+4}			60	100		60	80
Zero Detect			80	120		80	105
$\overline{\text{Overflow}}$			75	100		75	95
RAM Shifter Outputs			75	125		75	95
Q Shifter Outputs			25	60		25	40
Data Outputs	T_{ID}	30	85	120	15	85	100
Delay from Data Inputs (D_{IN}) to	Figure 5A						
$\overline{G}$			25	60		25	40
$\overline{P}$			25	60		25	40
C_{N+4}			25	65		25	45
Zero Detect			20	95		20	75
$\overline{\text{Overflow}}$			40	75		40	55
RAM Shifter Outputs			50	90		50	70
Data Outputs	T_{DD}	20	50	95	10	50	75
Delay from Carry In (C_N) to	Figure 5A						
C_{N+4}			15	30		15	25
Zero Detect			30	45		30	40
$\overline{\text{Overflow}}$			25	40		25	35
RAM Shifter Outputs			25	40		25	35
Data Outputs		5	30	45	5	30	40
Delay from Clock (low to high) to	A_N, B_N, I_N, D_{IN} constant						
$\overline{G}$				145		95	115
$\overline{P}$				145		95	115
C_{N+4}				115		105	125
Zero Detect				170		120	140
$\overline{\text{Overflow}}$				165		115	135
RAM Shifter Outputs				165		110	135
Q Shifter Outputs				60		30	40
Data Outputs (bypass ALU)	T_{C2}	20	60	145	20	95	115
Data Outputs (through ALU)				170	30	115	140
Delay from $\overline{\text{3 State Control}}$ to	All Inputs constant						
Low Data Outputs	T_{EA}	10	20	30	10	20	25
High Impedance Outputs	T_{ER}	5	14	25	5	15	20

*The maximum of all possible input and output conditions is specified with outputs sinking maximum current through a resistor to V_{CC} and driving a 30 pF load (15 pF on Shift I/O) to ground.

[1] Typical values are measured at 5.0 V and 25°C.

A.C. CHARACTERISTICS* – Cont'd.

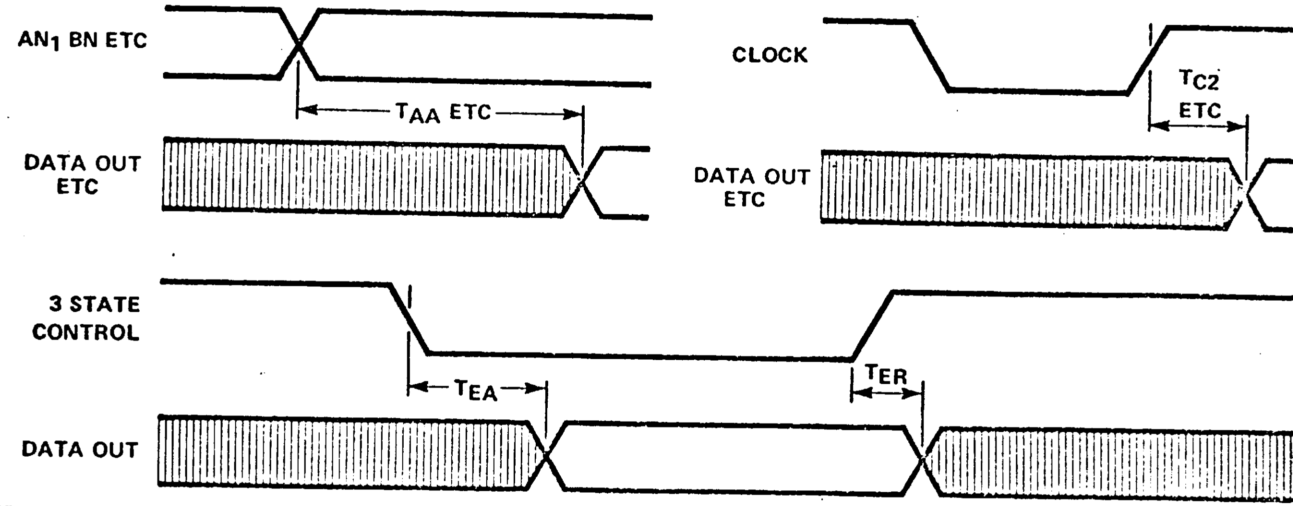
PARAMETER	SYMBOL/CONDITIONS	TIME IN NANOSECONDS				
		5 V ± 10% -55° TO 125°C 5701			5 V ± 5% 0° TO 75° 6701	
		MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]
Setup Time Before the High to Low Transition of Clock	Figure 5B					
A_N	T_{AS}	115	60		85	60
B_N	T_{BS1}	120	60		90	60
I_0, I_1, I_2	T_{IS1}	30	5		15	5
Setup Time Before the Low to High Transition of Clock	Figure 5B					
A_N, B_N	T_{BS2}	240	130		185	130
C_N	T_{CNS}	95	45		70	45
I_3, I_4, I_5, I_6, I_7	T_{IS2}	150	90		120	90
Data Inputs (D_{IN})	T_{DS}	95	50		70	50
RAM Shifter Inputs	T_{RS}	60	30		45	30
Q Shifter Inputs	T_{QS}	45	15		30	15
Hold Time After the Low to High Transition of Clock	Figure 5B					
A_N	T_{AH}	$-T_{CW}-10$	$-T_{CW}-25$		$-T_{CW}-15$	$-T_{CW}-10$
B_N	T_{BH}	-10	-20		-10	-20
I_0, I_1, I_2	T_{IH1}	-20	-40		-20	-40
I_3, I_4, I_5, I_6, I_7	T_{IH2}	-30	-60		-30	-60
C_N	T_{CNH}	-20	-40		-20	-40
Data Inputs (D_{IN})	T_{DH}	-25	-50		-25	-50
RAM Shifter Inputs	T_{RH}	-25	-50		-25	-50
Q Shifter Inputs	T_{QH}	-15	-30		-15	-30
System Parameters	Figure 5B					
Clock Pulse Width (Low Time)	T_{CW}	80	25		50	25
Minimum Microinstruction Cycle Time	$T_{CYCLE} = T_{BS2} + T_{BH}$	230	110	∞	175	110

*The maximum of all possible input and output conditions is specified with outputs sinking maximum current through a resistor to V_C driving a 30 pF load (15 pF on Shift I/O) to ground.

[1] Typical values are measured at V_{CC} = 5.0 V and 25°C.

TIMING DIAGRAMS

Figure 5A — Delays



LEGEND: Shaded areas indicate don't care conditions or permitted timing tolerances.

TIMING DIAGRAMS – Cont'd.

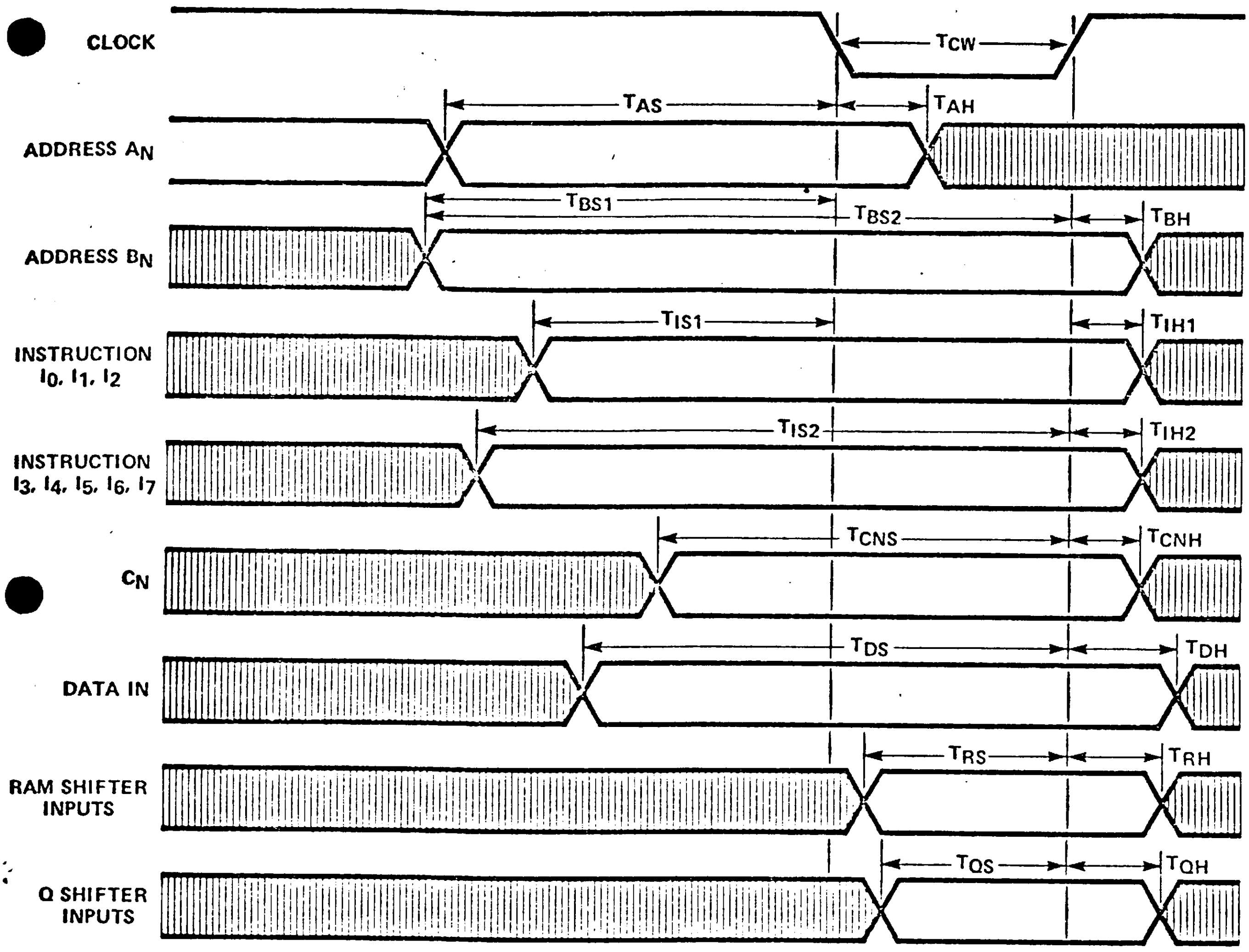


Figure 5B – Set-up and Hold Times

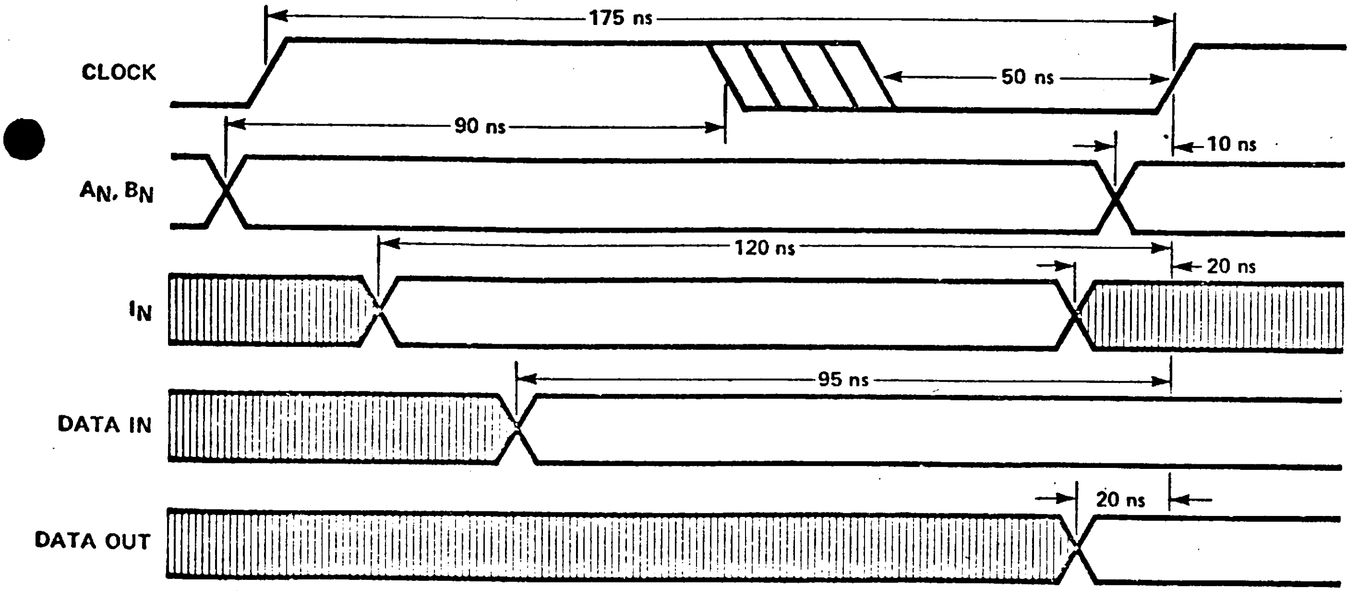


Figure 5C – Sample Minimum Cycle Time for 6701

INSTRUCTIONS LOCATED IN·THE ON CHIP ROMS

SYMBOL DEFINITIONS

A_I = Any of the 16 four bit registers in the multiport RAM (I = 0 to 15)

B_J = " " (J = 0 to 15)

$A_I + B_J$ = A_I plus B_J (arithmetic addition)

$A_I \forall B_J$ = A_I exclusive OR'ed with B_J

$A_I \vee B_J$ = A_I or B_J (logic inclusive or)

$A_I \wedge B_J$ = A_I and B_J (logic and)

$\overline{A_I}$ = The complement of A_I

$A_I \rightarrow Q$ = Transfer A_I to Q, A_I saved, Old Q is lost

$A_I \rightarrow OUT$ = Transfer A_I to the output pins, A_I is saved

$\overrightarrow{A_I}$ = A_I shifted right one bit

$\overleftarrow{A_I}$ = A_I shifted left one bit

$B_J - A_I$ = B_J minus $A_I = B_J + \overline{A_I} + C_N = B_J$ + 2's compl. of A_I

POSITIVE (ACTIVE HIGH) VS. NEGATIVE (ACTIVE LOW) LOGIC

The Microcontroller will work with either positive or negative logic. Positive logic defines a TTL High Level (≈ 3V) to be a "I" and a Low TTL Level (≈ GRD) to be a "O". Negative logic defines a TTL High to be A "O" and a TTL Low to be a "I". Consider a a classical "AND" function in TTL Logic

OUTPUT	INPUTS	
	B	A
L	L	L
L	L	H
L	H	L
H	H	H

in positive logic this becomes

OUTPUT	INPUTS	
	B	A
O	O	O
O	O	I
O	I	O
I	I	I

In negative logic the "AND" becomes an "OR" function since:

OUTPUT	INPUTS	
	B	A
I	I	I
I	I	O
I	O	I
O	O	O

Thus an "AND" in positive logic is an "OR" in negative logic. Similar reasoning yields the following transformations.

POSITIVE LOGIC	NEGATIVE LOGIC
AND	OR
OR	AND
EXCLUSIVE OR	EXCLUSIVE NOR
EXCLUSIVE NOR	EXCLUSIVE OR
TRANSFER	DECREMENT
DECREMENT	TRANSFER
INCREMENT	TRANSFER
TRANSFER	INCREMENT

CARRY IN (C_N)

The carry in pin is high when a carry is desired in positive logic, and a low when a carry is desired in negative logic.

TWO ROMS

All of the instructions in the 32 x 9 ROM can be modified in 8 different ways by the 8 x 8 ROM. Any instruction for example can be shifted left or right with the data out pins showing A, B, or F and the shifted result stored in the RAM or Q Register or both. If the clock is gated OFF by external logic it will be impossible to load the RAM or Q Register, and the controlled use of C_N in many instructions further raises the instruction count.

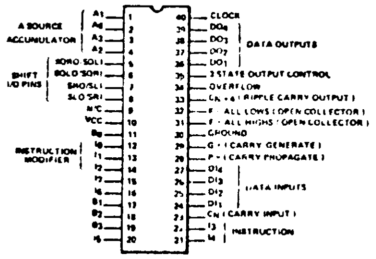
INSTRUCTIONS IN THE 32 x 9 ROM – POSITIVE LQGIC (1 = H ≈ 3 V) INTERPRETATION

ROM WORD							ALU Instruction	ALU OUTPUT		TYPICAL USES	
I_7	I_6	I_5	I_4	I_3	Decimal	Octal	(See Pg. 10 for Symbology)	No Carry In (C_N = L)	With Carry In (C_N = H)		
L	L	L	L	L	0	00	LLLL + HHHH + C_N	Force 1111	Force 0000	Initialization (Force 1's or 0's)	
L	L	L	L	H	· 1	01	AND A_I & B_j	$A_I \wedge B_j$	$A_I \wedge B_j$	AND	A_I & B_j
L	L	L	H	L	2	02	AND D_1 & B_j	$D_I \wedge B_j$	$D_I \wedge B_j$	"	D_I & B_j
L	L	L	H	H	3	03	OR A_I & B_j	$A_I \vee B_j$	$A_I \vee B_j$	OR	A_I & B_j
L	L	H	L	L	4	04	OR D_I & B_j	$D_I \vee B_j$	$D_I \vee B_j$	"	D_I & B_j
L	L	H	L	H	5	05	Exclusive OR A_I & B_j	$A_I \veebar B_j$	$A_I \veebar B_j$	Exclusive Or	A_I & B_j
L	L	H	H	L	6	06	Exclusive OR D_I & B_j	$D_I \veebar B_j$	$D_I \veebar B_j$	"	D_I & B_j
L	L	H	H	H	7	07	$\overline{A_I}$ + HHHH + C_N	$\overline{A_I}$ + 1111	$\overline{A_I}$	Invert	A_I
L	H	L	L	L	8	10	$\overline{D_I}$ + HHHH + C_N	$\overline{D_I}$ + 1111	$\overline{D_I}$	"	D_I
L	H	L	L	H	9	11	$\overline{B_j}$ + HHHH + C_N	$\overline{B_j}$ + 1111	$\overline{B_j}$	"	B_j
L	H	L	H	L	10	12	$\overline{Q}$ + HHHH + C_N	$\overline{Q}$ + 1111	$\overline{Q}$	"	Q
L	H	L	H	H	11	13	$\overline{A_I}$ + LLLL + C_N	$\overline{A_I}$	$\overline{A_I}$ + 0001	2's Complement Of	A_I
L	H	H	L	L	12	14	$\overline{D_I}$ + LLLL + C_N	$\overline{D_I}$	$\overline{D_I}$ + 0001	"	D_I
L	H	H	L	H	13	15	$\overline{B_j}$ + LLLL + C_N	$\overline{B_j}$	$\overline{B_j}$ + 0001	"	B_j
L	H	H	H	L	14	16	$\overline{Q}$ + LLLL + C_N	$\overline{Q}$	$\overline{Q}$ + 0001	"	Q
L	H	H	H	H	15	17	A_I + LLLL + C_N	A_I	A_I + 0001	Transfer Or Increment	A_I
H	L	L	L	L	16	20	D_I + LLLL + C_N	D_I	D_I + 0001	"	D_I
H	L	L	L	H	17	21	B_j + LLLL + C_N	B_j	B_j + 0001	"	B_j
H	L	L	H	L	18	22	Q + LLLL + C_N	Q	Q + 0001	"	Q
H	L	L	H	H	19	23	A_I + HHHH + C_N	A_I + 1111	A_I	Decrement Or Transfer	A_I
H	L	H	L	L	20	24	D_I + HHHH + C_N	D_I + 1111	D_I	"	D_I
H	L	H	L	H	21	25	B_j + HHHH + C_N	B_j + 1111	B_j	"	B_j
H	L	H	H	L	22	26	Q + HHHH + C_N	Q + 1111	Q	"	Q
H	L	H	H	H	23	27	A_I + B_j + C_N	A_I + B_j	A_I + B_j + 0001	Add	A_I & B_j
H	H	L	L	L	24	30	D_I + B_j + C_N	D_I + B_j	D_I + B_j + 0001	"	D_I & B_j
H	H	L	L	H	25	31	A_I + Q + C_N	A_I + Q	A_I + Q + 0001	"	A_I & Q
H	H	L	H	L	26	32	D_I + Q + C_N	D_I + Q	D_I + Q + 0001	"	D_I & Q
H	H	L	H	H	27	33	A_I + $\overline{B_j}$ + C_N	A_I - B_j - 0001	A_I - B_j	Subtract	A_I & B_j
H	H	H	L	L	28	34	B_j + $\overline{A_I}$ + C_N	B_j - A_I - 0001	B_j - A_I	"	B_j & A_I
H	H	H	L	H	29	35	D_I + $\overline{B_j}$ + C_N	D_I - B_j - 0001	D_I - B_j	"	D_I & B_j
H	H	H	H	L	30	36	B_j + $\overline{D_I}$ + C_N	B_j - D_I - 0001	B_j - D_I	"	B_j & D_I
H	H	H	H	H	31	37	D_I + $\overline{Q}$ + C_N	D_I - Q - 0001	D_I - Q	"	D_I & Q

INSTRUCTION MODIFIERS IN THE 8 x 8 ROM – POSITIVE LOGIC (1 = H ≈ 3 V) INTERPRETATION

Rom Word			Rom Word	Load Control		Shift Control			Data Out Control		
I_2	I_1	I_0	Decimal	Load Ram B_j	Load Q	Shift Left	Shift Right	Don't Shift	A Latch	B Latch	ALU Output F
L	L	L	0	X				X			X
L	L	H	1	X				X	X		
L	H	L	2	X				X		X	
L	H	H	3	X		X					X
H	L	L	4	X			X				X
H	L	H	5	X	X	X					X
H	H	L	6	X	X		X				X
H	H	H	7		X			X			X

PIN CONFIGURATION



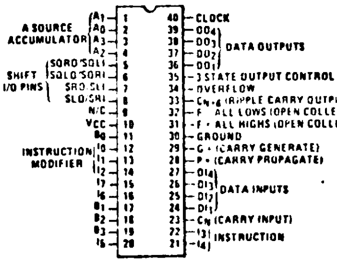
INSTRUCTIONS IN THE 32 x 9 ROM – NEGATIVE LOGIC (1 = L ≈ 0 V) INTERPRETATION

ROM WORD							ALU Instruction (See Pg.10 for Symbology)	ALU OUTPUT		TYPICAL USES	
I_7	I_6	I_5	I_4	I_3	Decimal	Octal		No Carry In (C_N = H)	With Carry In (C_N = L)		
L	L	L	L	L	31	37	LLLL + HHHH + C_N	Force 1111	Force 0000	Initialization (Force 1's or 0's)	
L	L	L	L	H	30	36	OR A_I & B_j	$A_I \vee B_j$	$A_I \vee B_j$	OR	A_I & B_j
L	L	L	H	L	29	35	OR D_I & B_j	$D_I \vee B_j$	$D_I \vee B_j$	"	D_I & B_j
L	L	L	H	H	28	34	AND A_I & B_j	$A_I \wedge B_j$	$A_I \wedge B_j$	AND	A_I & B_j
L	L	H	L	L	27	33	AND D_I & B_j	$D_I \wedge B_j$	$D_I \wedge B_j$	"	D_I & B_j
L	L	H	L	H	26	32	Exclusive NOR A_I & B_j	$\overline{A_I \veebar B_j}$	$\overline{A_I \veebar B_j}$	Exclusive Nor	A_I & B_j
L	L	H	H	L	25	31	Exclusive NOR D_I & B_j	$\overline{D_I \veebar B_j}$	$\overline{D_I \veebar B_j}$	"	D_I & B_j
L	L	H	H	H	24	30	$\overline{A_I}$ + HHHH + C_N	$\overline{A_I}$	$\overline{A_I}$ + 0001	2's Complement Of	A_I
L	H	L	L	L	23	27	$\overline{D_I}$ + HHHH + C_N	$\overline{D_I}$	$\overline{D_I}$ + 0001	"	D_I
L	H	L	L	H	22	26	$\overline{B_j}$ + HHHH + C_N	$\overline{B_j}$	$\overline{B_j}$ + 0001	"	B_j
L	H	L	H	L	21	25	$\overline{Q}$ + HHHH + C_N	$\overline{Q}$	$\overline{Q}$ + 0001	"	Q
L	H	L	H	H	20	24	$\overline{A_I}$ + LLLL + C_N	$\overline{A_I}$ + 1111	$\overline{A_I}$	Invert	A_I
L	H	H	L	L	19	23	$\overline{D_I}$ + LLLL + C_N	$\overline{D_I}$ + 1111	$\overline{D_I}$	"	D_I
L	H	H	L	H	18	22	$\overline{B_j}$ + LLLL + C_N	$\overline{B_j}$ + 1111	$\overline{B_j}$	"	B_j
L	H	H	H	L	17	21	$\overline{Q}$ + LLLL + C_N	$\overline{Q}$ + 1111	$\overline{Q}$	"	Q
L	H	H	H	H	16	20	A_I + LLLL + C_N	A_I + 1111	A_I	Decrement Or Transfer	A_I
H	L	L	L	L	15	17	D_I + LLLL + C_N	D_I + 1111	D_I	"	D_I
H	L	L	L	H	14	16	B_j + LLLL + C_N	B_j + 1111	B_j	"	B_j
H	L	L	H	L	13	15	Q + LLLL + C_N	Q + 1111	Q	"	Q
H	L	L	H	H	12	14	A_I + HHHH + C_N	A_I	A_I + 0001	Transfer Or Increment	A_I
H	L	H	L	L	11	13	D_I + HHHH + C_N	D_I	D_I + 0001	"	D_I
H	L	H	L	H	10	12	B_j + HHHH + C_N	B_j	B_j + 0001	"	B_j
H	L	H	H	L	9	11	Q + HHHH + C_N	Q	Q + 0001	"	Q
H	L	H	H	H	8	10	$A_I + B_j + C_N$	$A_I + B_j$	$A_I + B_j$ + 0001	Add	A_I & B_j
H	H	L	L	L	7	07	$D_I + B_j + C_N$	$D_I + B_j$	$D_I + B_j$ + 0001	"	D_I & B_j
H	H	L	L	H	6	06	$A_I + Q + C_N$	$A_I + Q$	$A_I + Q$ + 0001	"	A_I & Q
H	H	L	H	L	5	05	$D_I + Q + C_N$	$D_I + Q$	$D_I + Q$ + 0001	"	D_I & Q
H	H	L	H	H	4	04	$A_I + \overline{B_j} + C_N$	$A_I - B_j$ - 0001	$A_I - B_j$	Subtract	A_I & B_j
H	H	H	L	L	3	03	$B_j + \overline{A_I} + C_N$	$B_j - A_I$ - 0001	$B_j - A_I$	"	B_j & A_I
H	H	H	L	H	2	02	$D_I + \overline{B_j} + C_N$	$D_I - B_j$ - 0001	$D_I - B_j$	"	D_I & B_j
H	H	H	H	L	1	01	$B_j + \overline{D_I} + C_N$	$B_j - D_I$ - 0001	$B_j - D_I$	"	B_j & D_I
H	H	H	H	H	0	00	$D_I + \overline{Q} + C_N$	D_I - Q - 0001	D_I - Q	"	D_I & Q

INSTRUCTION MODIFIERS IN THE 8 x 8 ROM – NEGATIVE LOGIC (1 = L ≈ 0 V) INTERPRETATION

ROM Word				Load Control			Shift Control			Data Out Control		
					Load Q							
I_2	I_1	I_0	Decimal	Load RAM with RAM Shifter Output	with Q Shifter Output	with ALU Output	Shift Left	Shift Right	Don't Shift	A Latch	B Latch	ALU Output F
L	L	L	7	X					X			X
L	L	H	6	X					X	X		
L	H	L	5	X					X		X	
L	H	H	4	X			X					X
H	L	L	3	X				X				X
H	L	H	2	X	X		X					X
H	H	L	1	X	X			X				X
H	H	H	0			X			X			X

PIN CONFIGURATION



APPLICATION TRICKS WITH SOME INSTRUCTIONS

1) $A_I \wedge B_J$ or $A_I \vee B_J$ can be used as a no operation if $A_I = B_J$ and only the RAM is loaded since we are loading a register with itself.

2) $A_I \veebar B_J$ can be used to load LLLL if $A_I = B_J$ regardless of the state of C_N.

3) $A_I + B_J + C_N$ gives $A_I + A_I + C_N$ if $A_I = B_J$, forming twice "A" or twice (A + I). IF $A_I + B_J + C_N$ is shifted left with $A_I = B_J$, we get a double left shift since adding a number to itself is a multiply by 2 which in binary is a shift left.

4) Q can be shifted and stored back in Q during any instruction involving HLH or HHL on I_2, I_1, I_0 permitting simultaneous RAM and Q shifting. Operations involving 3 registers (A, B, and Q) are also possible since we can perform A + B → Q.

5) $B_J + \text{LLLL} + C_N \rightarrow B_J$
$B_J + \text{HHHH} + C_N \rightarrow B_J$ can be used as a NO OP if there is no carry

6) $B_J + \text{LLLL} + C_N \rightarrow B_J,\ A_I \rightarrow \text{OUT}$
$B_J + \text{HHHH} + C_N \rightarrow B_J,\ A_I \rightarrow \text{OUT}$

Permits use of one of the B_J for a program counter (P.C) while looking at one of the A_I which might be an accumulator on the output pins. If there is a carry, $B_O + 0001 \rightarrow B_O$ (Increment P.C)
$A_I \rightarrow$ OUT (Old P.C → OUT)

Might be used to increment the program counter while having the old value of the program counter addressing memory (via the data out pins) in one microcontroller cycle.

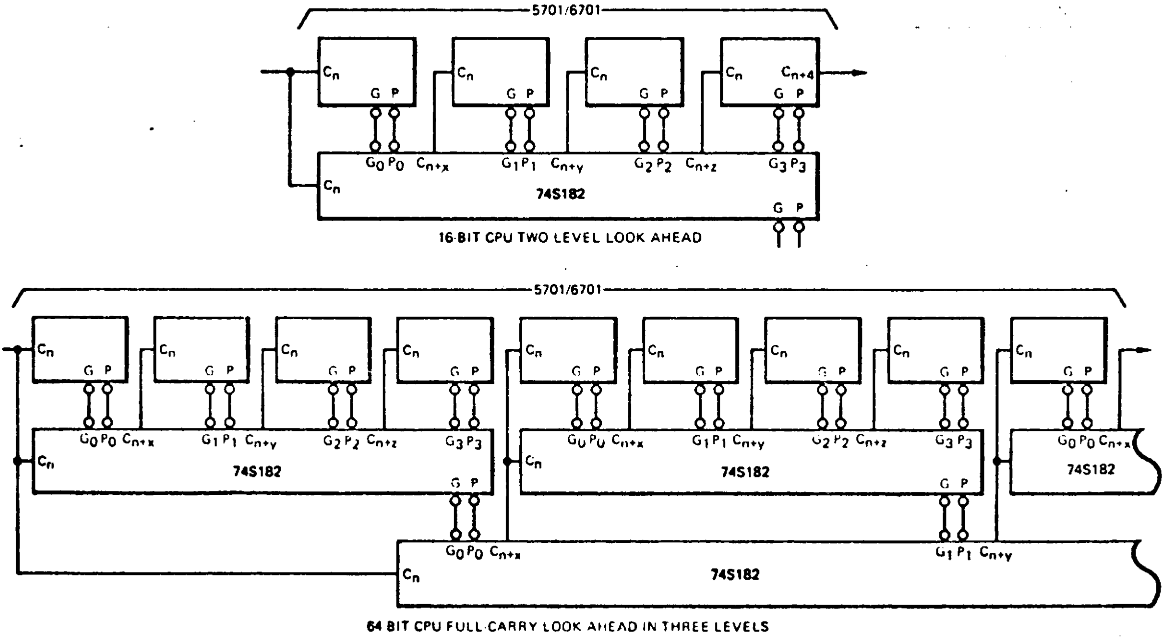
CARRY GENERATE ($\overline{G}$) AND CARRY PROPAGATE ($\overline{P}$)

A) THEORY

The $\overline{G}$ and $\overline{P}$ pins of the microcontroller are designed to be used with the TTL 54182/74182 look-ahead carry generator. The look-ahead techniques predict whether or not there will be a carry generated from the microcontroller and whether the input carry (C_N) will be propagated through the microcontroller, based on the input operands rather than waiting for the carry to ripple through each internal stage of the microcontroller. The add times of larger word length machines are significantly faster with these techniques.

B) ACTIVE HIGH AND ACTIVE LOW LOGIC

$\overline{G}$ and $\overline{P}$ are sometimes called X and Y in active HIGH (Positive) logic terminology since the generate and propagate terminology are pertinent only to active LOW (Negative) logic. The microcontroller and look-ahead carry generator will produce the correct results in both active HIGH and active LOW logic. Figure 6 shows how to hook-up the look-ahead carry generator (74182 or 74S182).



16 BIT CPU TWO LEVEL LOOK AHEAD

64 BIT CPU FULL-CARRY LOOK AHEAD IN THREE LEVELS

Figure 6

C) LOGIC EQUATION

In logic symbology where · is a logic "AND" and + is a logic "OR" and where the subscript L means a low TTL logic level; P can be expressed as follows:

$$Y = P_L = (A'_{3H} + B'_{3H}) \cdot (A'_{2H} + B'_{2H}) \cdot (A'_{1H} + B'_{1H}) \cdot (A'_{0H} + B'_{0H})$$

This equation is interpreted to mean that propagate is a low level if A'_3 or B'_3 is high and A'_2 or B'_2 is high, and A'_1 or B'_1 is high, and A'_0 or B'_0 is high. A'_3, A'_2, A'_1, A'_0, and B'_3, B'_2, B'_1, B'_0 refer to the four bit number applied at the input A' and B' of the microcontroller ALU.

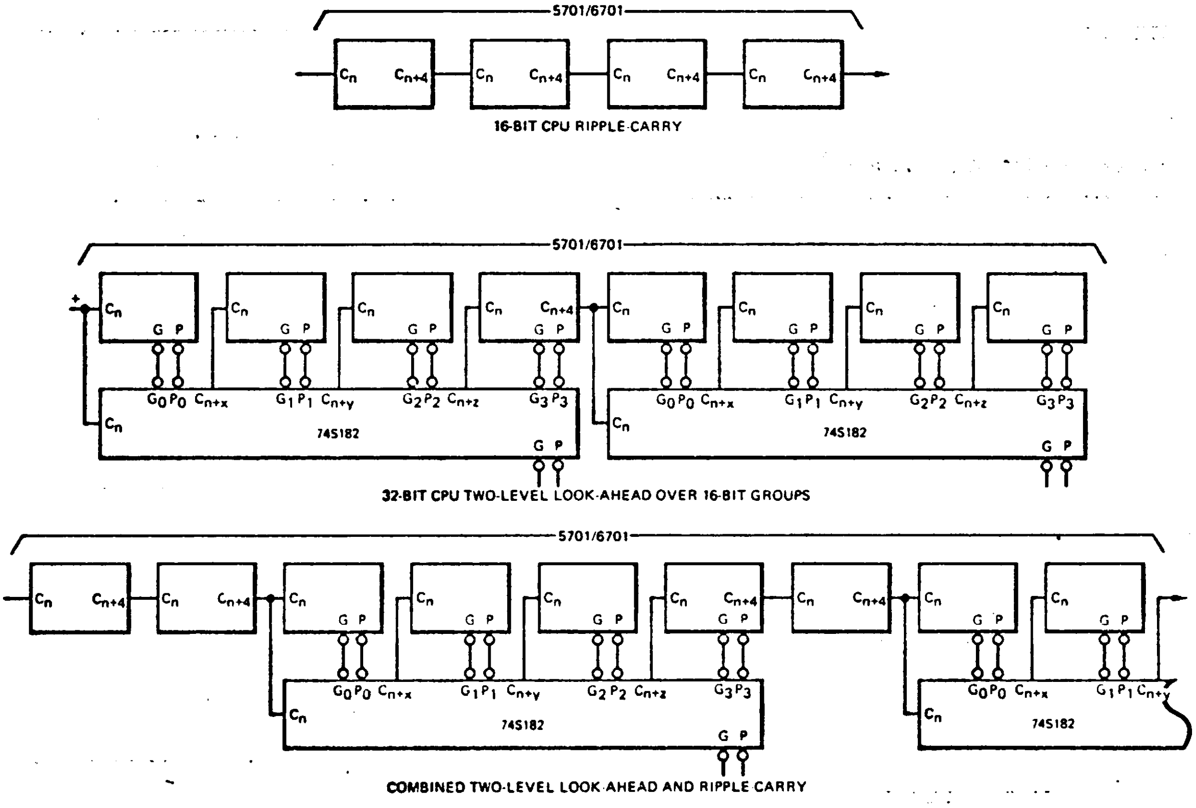
In the same symbology:

$$X = G_L = (A'_{3H} \cdot B'_{3H}) + (A'_{3H} + B'_{3H}) \cdot (A'_{2H} \cdot B'_{2H}) + (A'_{3H} + B'_{3H}) \cdot (A'_{2H} + B'_{2H}) \cdot$$
$$(A'_{1H} \cdot B'_{1H}) + (A'_{3H} + B'_{3H}) \cdot (A'_{2H} + B'_{2H}) \cdot (A'_{1H} + B'_{1H}) \cdot (A'_{0H} \cdot B'_{0H})$$

RIPPLE CARRY (C_{N+4})

In systems not requiring the speed of look-ahead addition the 74S182 look-ahead carry generator can be eliminated and the ripple carry C_{N+4} can be used instead. Simply tie the ripple carry output C_{N+4} of the least significant 5701/6701 package to the carry input C_N of the more significant 5701/6701 package. Figure 7 shows some examples of ripple carry and combined ripple and look-ahead carry.

The ripple carry output will be a TTL high level when a carry out occurs in the active HIGH (Positive) logic convention. The ripple carry output will be a TTL low level when a carry out occurs in the active LOW (Negative) logic convention. The ripple carry is not gated off during logic operations since the conditions defining whether it should be off or on are not the same in positive and negative logic.



16-BIT CPU RIPPLE CARRY

32-BIT CPU TWO-LEVEL LOOK-AHEAD OVER 16-BIT GROUPS

COMBINED TWO-LEVEL LOOK-AHEAD AND RIPPLE CARRY

Figure 7

WORST CASE MINIMUM CYCLE TIMES OVER THE V_{CC} AND TEMPERATURE RANGE FOR CPU'S LARGER THAN 4 BITS

CPU Word Length (# Bits)	Minimum Cycle with Ripple Carry (ns)	6701 Minimum Cycle* with Look Ahead		Minimum Cycle with Ripple Carry (ns)	5701 Minimum Cycle* with Look Ahead	
		# Look Ahead 74S182s	Cycle Time (ns)		# Look Ahead 74S182s	Cycle Time (ns)
4	175			230		
8	175			230		
		1	175		1	230
12	195			255		
		1	175		1	230
16	220			285		
		1	175		1	230
24	270			345		
		1	220		1	290
32	320			405		
		1	270		1	350
		2	205		2	275
		3	190		3	260
48	420			525		
		1	370		1	470
		2	305		2	395
		3	240		3	320
		4	190		4	260
64	520			645		
		1	470		1	590
		2	405		2	515
		3	340		3	440
		4	275		4	365
		5	190		5	260

*The minimum look-ahead cycle times assume a 74S182 with a delay of 10ns maximum for 5 V ± 5%, 0° to 75°C or a 54S182 with a delay of 15ns maximum for 5 V ±10%, –55° to 125°C.

NOTE

The worst case instruction from a cycle time consideration is an add, shift, and store instruction in one cycle. The cycle times above are based on this instruction.

THEORY

The delay from A_I or B_J to data output can be assumed to equal the delay from A_I or B_J to the data inputs of the on chip RAM. The increase in the delay from A_I or B_J to data out due to waiting for the carry in, over the case where the carry in is present early is a direct cycle time adder.

SAMPLE CALCULATION OF THE CYCLE FOR A 32 BIT MACHINE AND THE REQUIRED CLOCK TIMING

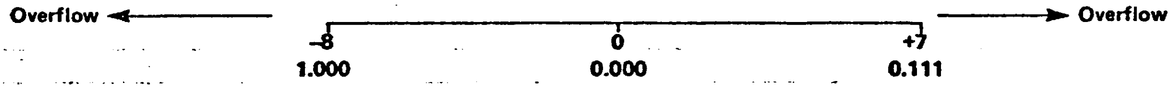
Calculate the minimum cycle time of the 6701 in a 32 bit configuration. Two 74S182's will be used to look ahead over the two 16 bit section with ripple carry between the two 16 bit sections (see the center drawing of Figure 7 page 14).

From page 7, the accumulator address to $\overline{G}$ or $\overline{P}$ delay is 100ns. It will then take another 10ns in the 74S182 to generate C_{N+X}, C_{N+Y}, and C_{N+Z}, 25ns for the C_N to C_{N+4} delay between sections, and a further 10ns for the C_N to C_{N+X}, C_{N+Y}, C_{N+Z} delay of the second 74S182. The sum of the set up and hold times $T_{CNS} + T_{BH}$ is 60ns to give a cycle time of 205ns. This delay is greater than the single 6701 cycle time and is the governing cycle time.

OVERFLOW

THEORY

When the result of a binary addition or subtraction requires more bits than the arithmetic unit can accommodate overflow can occur. For example, consider a 4-bit system (3 bits + sign) where the most significant bit is defined on a zero for positive numbers and a one for negative numbers. This system has a maximum value of 7 and a minimum value of −8 as indicated on the line graph below:



If we list all the addition and subtraction conditions which will give an answer not in the number system (beyond the ends of the line graph above), four conditions result in overflow and are listed below with examples:

OVERFLOW CONDITIONS

1. ADD TWO LARGE POSITIVE NUMBERS

   7 plus 7 = 14, which is larger than our largest number (+7) on the line graph, therefore, overflow occurs
   2 plus 1 = 3, which is smaller than +7, therefore, no overflow

2. ADD TWO LARGE NEGATIVE NUMBERS

   −7 plus −7 = −14, which is beyond the end of the line graph, therefore, overflow occurs.
   −2 plus −1 = −3, no overflow since −3 is within the bounds of the number system.

3. SUBTRACT A LARGE NEGATIVE NUMBER FROM A LARGE POSITIVE NUMBER

   −7 minus +7 = −14, overflow occurs
   −2 minus +1 = −3, no overflow

4. SUBTRACT A LARGE POSITIVE NUMBER FROM A LARGE NEGATIVE NUMBER

   +7 minus −7 = +14, overflow occurs
   +2 minus −1 = +3, no overflow

OVERFLOW PIN

A conventional binary number system has the most significant bit defined as the sign bit (0 is a positive number, 1 is a negative number by definition) and negative numbers are represented in a 2's complement form (the 2's complement of a number can be formed by inverting the number and adding one, for example, 0101 = +5, −5 = 1010 plus 1 or 1011.

The four overflow conditions shown above can be detected by exclusive ORing the carry-in and carry-out of the sign bit. If the carry's disagree, overflow has occurred. The overflow output will only be meaningful on the most significant 5701/6701 package in systems larger than four bits. Since the overflow is implemented with an exclusive nor gate the 5701/6701 will also give overflow outputs during logic as well as arithmetic operations requiring that external logic decide when the overflow output is meaningful. The overflow pin will be low when overflow occurs.

HARDWARE MULTIPLY AND DIVIDE

I. GENERAL DISCUSSION

The microcontroller's capability of adding and shifting or subtracting and shifting within one microinstruction cycle, and having the accumulator extension register Q on chip permits fast microprogrammed multiply and divide. Less than 20 cycles are required for a 16 bit multiply or divide.

Figure 8 shows how to connect the microcontroller for a 16 bit multiply/divide. The least significant bit of the RAM shifter is shifted into the most significant bit of Q.

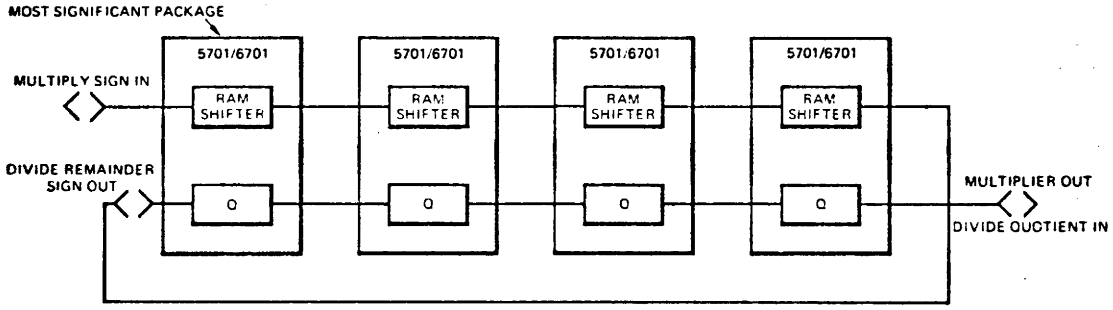


Figure 8

II. HARDWARE MULTIPLY – EXAMPLE FOR A 16 BY 16 MULTIPLY

A. INITIAL CONDITIONS

Put the multiplier in Q, multiplicand on the RAM A output, and clear the RAM B output to zero.

B. FINAL CONDITIONS

The most significant 16 bit half of the 32 bit product will be in RAM B and the least significant 16 bit half in Q. The multiplicand in A is undisturbed.

C. THEORY

A 16 by 16 multiply in the microcontroller requires 16 reduction steps. Each reduction step consists of an add (A+B), if the least significant bit or the multiplier emerging from Q is a one, or a transfer (0+B) if the least significant bit of Q is a zero, and then a right shift of the result into B and Q.

D. TWO'S COMPLEMENT

Two's complement multiplication requires sign bit manipulation and an additional correction cycle for negative multipliers. The sign inserted into the most significant bit of B during the reduction cycles is the exclusive OR of overflow and the most significant bit of the ALU output. After 16 reduction cycles, an additional correction cycle is required if the multiplier was negative. The correction cycle consists of subtracting the multiplicand from the product without shifting.

III. HARDWARE DIVIDE

Example for a 16 bit divisor and 32 bit dividend giving a 16 bit quotient and 16 bit remainder.

A. INITIALIZATION

Put the divisor on the RAM A output, and the dividend's most significant half on the RAM B output and the least significant half in Q.

B. FINAL CONDITION

The 16 bit quotient is on the RAM B output and the 16 bit remainder is in Q. The divisor is in the RAM A output undisturbed.

C. THEORY

A non-restoring two's complement division requires 16 reduction steps for negative quotients. In non-restoring division, the divisor is successively subtracted from the dividend and the result shifted left until the remainder changes sign. At this point the divisor has been subtracted one too many times and is added back until the original sign is restored.

Negative quotients are generated in one's complement notation (the one's complement of a number is its inverse). The two correction cycles provide a remainder correction if required so that the remainder sign is the same as the original dividend and quotient correction from one's complement to two's complement form for negative quotients.

Each of the 16 reduction cycles consists of a subtract (B–A) or an add (A+B) operation plus a left shift of the result. The most significant bit of Q propagates into the least significant bit of B and the quotient bit is shifted into the least significant vacated position of Q. The case of zero remainder will not require quotient correction but may require sign correction of the remainder.

SIGN EXTENSION

A common operation in computers is the calculation of an effective address. In a 16 bit computer, for example, we may have program counter relative addressing, where the addition of an 8 bit displacement to a 16 bit program counter is the effective memory address. This 8 bit displacement is a signed displacement with a value between +127 and −128.

In using the 5701/6701 to calculate on effective address, the displacement will be brought into the unit with the data in pins, and added to the program counter which is stored in one of the internal registers. The problem arises when adding on 8 bit number to a 16 bit number in that the upper 8 bits of the displacement must be ignored and the sign of the 8 bit displacement (a 0 in bit 8 is a plus and a 1 is a minus) must be extended into bits 9 thru 16 to make a signed 8 bit number into a proper signed 16 bit number. For example the 8 bit displacement 01111111 is +127 and must be translated into the 16 bit number 0000000001111111 before adding it to the 16 bit program counter.

Several techniques can be used to extend the sign. Figure 9 shows dual 4 bit selects (74157) which are used to duplicate the sign bit (bit 8) into the upper 8 bits. The 74157's either let the normal upper 8 bits of the data in bus or the sign bit extended into the upper 8 bits of the 5701/6701's data in depending on whether the multipler's select line is high or low. The instruction lines of the 5701/6701's required for 16 bits can be wired to common pins in the 4 packages with this approach. Bit 8 can be buffered if the loading of the 74157 would be a problem.

Another technique is shown in Figure 10, and is applicable only when ripple carry is employed. It requires that the two low order packages execute a data in plus register operation and that the 2 high order package execute a LLLL plus HHHH plus C_N instruction. If C_N is low and the 7451 is in the sign extend mode, then highs will be forced into the upper two packages. If C_N is a high and the 7451 is in the extend sign mode, then lows will be forced into the high order packages. When the sign is not to be extended the 7451 will pass the C_{N+4} ripple carry into C_N. This method requires that the lower two 5701/6701's execute a different instruction than the upper two 5701/6701's. This particular case will require changing the state of two of the 8 instruction lines which go into the upper two 5701/6701's, namely the I_6 and I_7 lines. Note that in the instruction on page 10, these instruction were purposely mapped so that few I_N lines must be changed to go from LLLL + HHHH + C_N to $D_I + B_J + C_N$.

A third alternative is to microprogram the sign extension with off chip ROMs by masking or forcing the upper 8 bits.

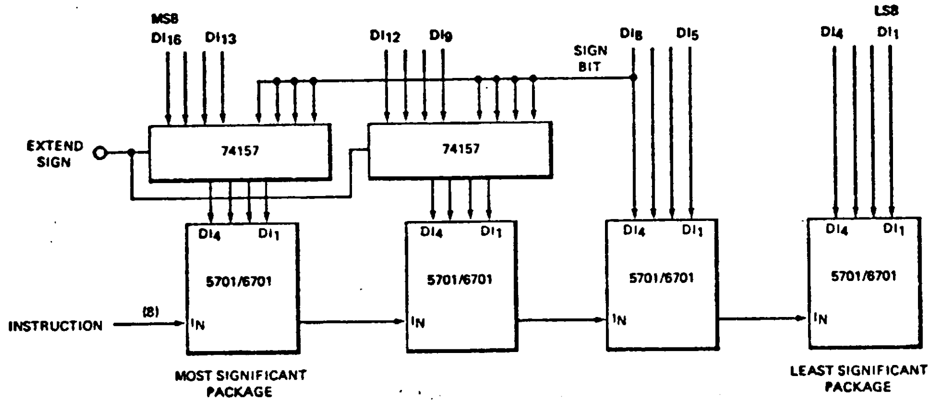


Figure 9

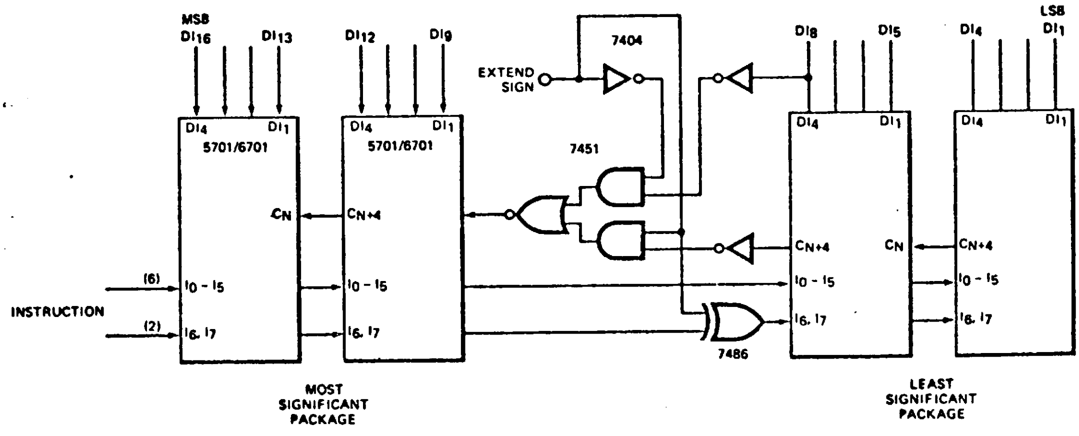


Figure 10

MICROPROGRAMMED EMULATION

Figure 11 shows a 16 bit microprogrammed CPU built from 4 microcontrollers, a few ROMs and some TTL. This CPU performs about the same function as most 16 bit minicomputer's CPU which take 110 to 225 TTL MSI packages, and require one or two 15" x 15" printed circuit boards. The CPU of Figure 11 requires 18 packages and will fit on 5" x 7" board.

HOW IT WORKS

The four microcontrollers form the data flow section of the CPU. The zero detect (F = LLLL and F = HHHH) pins of the 6701 are open collector and are tied together to detect zero on the 16 bit CPU. The 3 state output control and clock lines as well as the instruction and accumulator addresses are tied to the same pins in all 4 6701's. The data flow section has 16 bits of data in and 16 bits of data out on 2 independent busses.

A programmable ROM is used to detect the various conditions which cause branching (i.e., overflow, negative, zero, etc.) and this information is fed into the sequence control section of the CPU to alter the next state when necessary.

The instruction register of the computer is the address input to the target address ROM. It points to the starting address of a group of addresses in the 1K x 24 ROM which handles the function indicated by the operation code (op-code). The instruction register is assumed to have an instruction format comprised of an 8 bit op-code, a 4 bit operand #1 select and a four bit operand #2 select like the RR format of the IBM 360.

For example, an instruction register containing might mean add file 3 to file 5 and store the result in file 5. The add assembly language instruction might point to decimal address 25 (0011001) in the target address ROM which would then output the starting address of the sequence in the emulation ROM for performing addition. A typical assembly language instruction might take 4 to 10 words in the 1K x 24 ROM.

Op Code	File	File
00011001	0101	0011

The microinstruction cycle time of the 16 bit CPU shown will be in the 350ns range. Since the microcontroller executes several operations in one cycle this CPU will execute instructions faster than most 16 bit minicomputers if semiconductor RAM is used.

The sequence of operations is programmed into the 1K x 24 for each instruction. A typical sequence for a memory reference instruction is shown below:

1. Calculate the effective address and latch it into the memory address register.

2. Fetch the contents of the memory location and latch it into the instruction register. If the memory has a 160ns or less access time, this step will not cost a microcontroller cycle.

3. Execute the instruction which is now present in the instruction register. Each clock pulse will output the required instruction to the microcontroller. When the sequence is ended the 1K x 24 ROM will disable the dual 10 bit select multiplexer gate which has been forming its next address and allow the next op-code in via the starting address ROM.

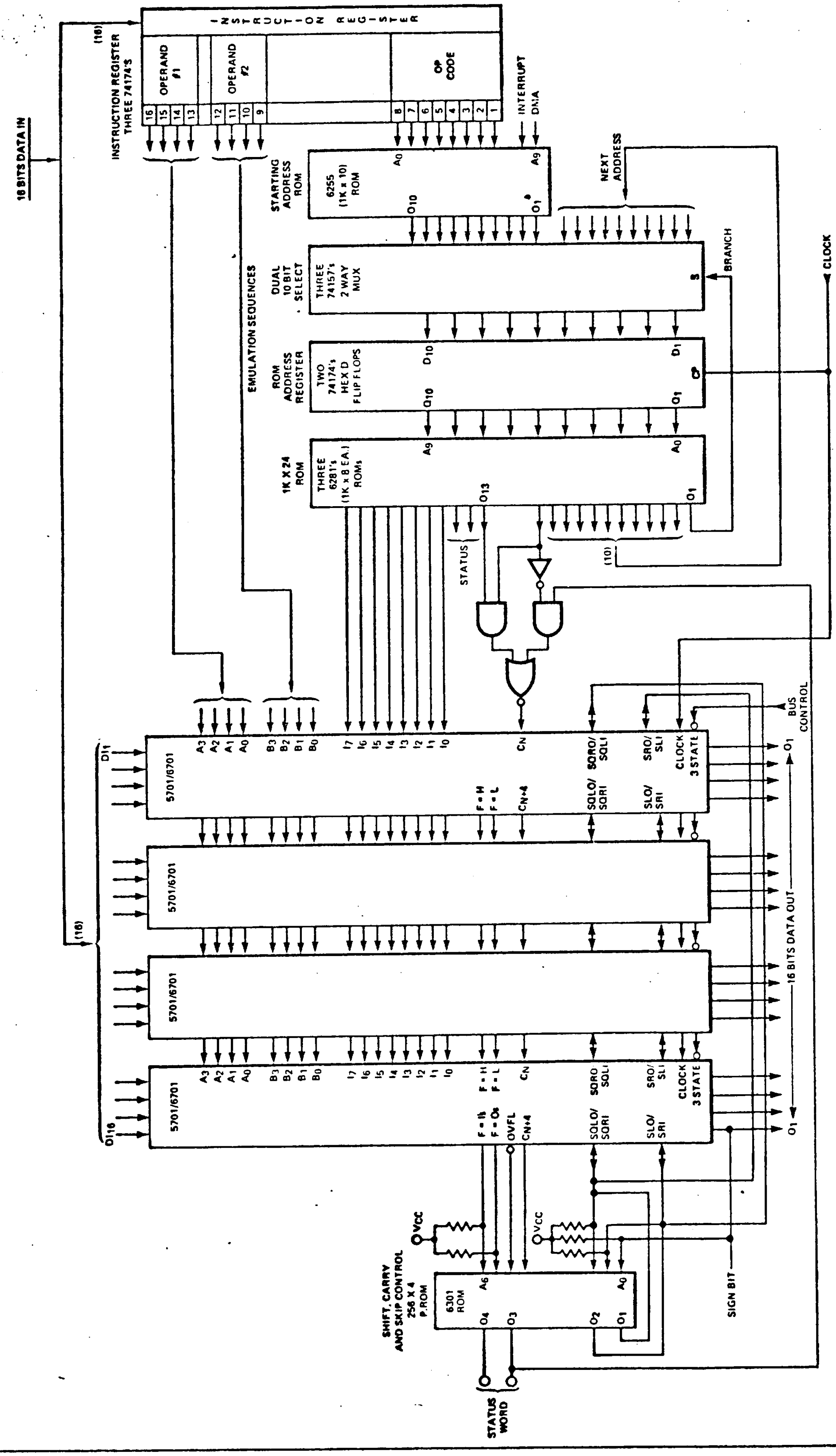
4. Increment the program counter and fetch the next instruction. A typical memory reference instruction will take 3 microcycles which includes most addressing modes, except indirect addressing. A 160ns access time, or less access time memory is required for emulation in 3 microcycles.

EMULATION

The advantage of the microprogrammed CPU described above is that it readily permits a machine designed with a new technology to be software compatible with an existing machine. The hardware technique is called emulation. Emulation protects the manufacturer's and customer's large investment in software.

The CPU configuration shown in Figure 11 can be used in many design applications where microprogrammed control might be thought of as too complicated, now that the package count has been reduced by the LSI microcontroller.

APPLICATION INFORMATION (Cont'd)



16 BIT MICROPROGRAMMED CPU

Figure 11

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ARITHMETICAL LOGICAL BOARD (ALB)	sign/date GB/780524	page
	repl	project

5

PROM TABLES

K

CPU CR8001/2/3 A.L. BOARD CARRY & PAGE CONTROL	sign/date GB/770328	page
	prom-type 32x8.3st	cr-no: 1295-1

			INPUT ADDRESSES.					OUTPUT										
			E GND	D MDAT 21	C MDAT 22	B MDAT 23	A PSWC			PSE MSB	TSE	.			SP0	SP1	CARRY IN LSB	
DEC.	HEX		4	3	2	1	0	HEX		8	7	6	5	4	3	2	1	DESCRIPTION
0	00		0	0	0	0	0	F	B	1	1	1	1	1	0	1	1	CPZ
1	01		0	0	0	0	1	F	B	1	1	1	1	1	0	1	1	CPZ
2	02		0	0	0	1	0	F	9	1	1	1	1	1	0	0	1	CCP
3	03		0	0	0	1	1	F	9	1	1	1	1	1	0	0	1	CCP
4	04		0	0	1	0	0	F	A	1	1	1	1	1	0	1	0	PZ
5	05		0	0	1	0	1	F	A	1	1	1	1	1	0	1	0	PZ
6	06		0	0	1	1	0	F	8	1	1	1	1	1	0	0	0	CP
7	07		0	0	1	1	1	F	8	1	1	1	1	1	0	0	0	CP
8	08		0	1	0	0	0	F	E	1	1	1	1	1	1	1	0	I/O
9	09		0	1	0	0	1	F	E	1	1	1	1	1	1	1	0	I/O
10	0A		0	1	0	1	0	F	8	1	1	1	1	1	0	0	0	PSW CP
11	0B		0	1	0	1	1	F	9	1	1	1	1	1	0	0	1	PSW CP
12	0C		0	1	1	0	0	F	F	1	1	1	1	1	1	1	1	
13	0D		0	1	1	0	1	F	F	1	1	1	1	1	1	1	1	
14	0E		0	1	1	1	0	D	F	1	1	0	1	1	1	1	1	TO FLAG
15	0F		0	1	1	1	1	D	F	1	1	0	1	1	1	1	1	TO FLAG
16	10		1	0	0	0	0	F	F	1	1	1	1	1	1	1	1	
17	11		1	0	0	0	1	F	F	1	1	1	1	1	1	1	1	
18	12		1	0	0	1	0	F	F	1	1	1	1	1	1	1	1	
19	13		1	0	0	1	1	F	F	1	1	1	1	1	1	1	1	
20	14		1	0	1	0	0	F	F	1	1	1	1	1	1	1	1	
21	15		1	0	1	0	1	F	F	1	1	1	1	1	1	1	1	
22	16		1	0	1	1	0	F	F	1	1	1	1	1	1	1	1	
23	17		1	0	1	1	1	F	F	1	1	1	1	1	1	1	1	
24	18		1	1	0	0	0	F	F	1	1	1	1	1	1	1	1	
25	19		1	1	0	0	1	F	F	1	1	1	1	1	1	1	1	
26	1A		1	1	0	1	0	F	F	1	1	1	1	1	1	1	1	
27	1B		1	1	0	1	1	F	F	1	1	1	1	1	1	1	1	
28	1C		1	1	1	0	0	F	F	1	1	1	1	1	1	1	1	
29	1D		1	1	1	0	1	F	F	1	1	1	1	1	1	1	1	
30	1E		1	1	1	1	0	F	F	1	1	1	1	1	1	1	1	
31	1F		1	1	1	1	1	F	F	1	1	1	1	1	1	1	1	
			4	3	2	1	0			8	7	6	5	4	3	2	1	

CPU CR8001/2/3 A.L. BOARD T-FILE CONTROL PROM 1	sign/date GB/770328	page
	prom-type 32x8.3st	cr-no: 1296-1

INPUT ADDRESSES.								OUTPUT										
			E MDAT 16	D MDAT 17	C MDAT 18	B MDAT 19	A MDAT 20			MSB R 1.8	R 1.7	R.1.6	R 1.5	R 1.4	R 1.3	R 1.2	LSB R 1.1	
DEC.	HEX		4	3	2	1	0	HEX		8	7	6	5	4	3	2	1	DESCRIPTION
0	00		0	0	0	0	0	F	F	1	1	1	1	1	1	1	1	BCNOP
1	01		0	0	0	0	1	B	C	1	0	1	1	1	1	0	0	TD1 SW TD2
2	02		0	0	0	1	0	9	D	1	0	0	1	1	1	0	1	LAR
3	03		0	0	0	1	1	F	D	1	1	1	1	1	1	0	1	TD2 SP ALS
4	04		0	0	1	0	0	F	F	1	1	1	1	1	1	1	1	INC OUT
5	05		0	0	1	0	1	F	F	1	1	1	1	1	1	1	1	ALS TD2
6	06		0	0	1	1	0	B	D	1	0	1	1	1	1	0	1	ALS DR MAR
7	07		0	0	1	1	1	F	F	1	1	1	1	1	1	1	1	MALS FUNC
8	08		0	1	0	0	0	9	D	1	0	0	1	1	1	0	1	INS 1
9	09		0	1	0	0	1	B	9	1	0	1	1	1	0	0	1	INC IN
10	0A		0	1	0	1	0	F	7	1	1	1	1	0	1	1	1	FI
11	0B		0	1	0	1	1	F	F	1	1	1	1	1	1	1	1	FUNC MAR
12	0C		0	1	1	0	0	F	D	1	1	1	1	1	1	0	1	TD 2
13	0D		0	1	1	0	1	F	F	1	1	1	1	1	1	1	1	SEM STO
14	0E		0	1	1	1	0	9	D	1	0	0	1	1	1	0	1	TI1 S4 TD1
15	0F		0	1	1	1	1	F	F	1	1	1	1	1	1	1	1	FUNC MALS
16	10		1	0	0	0	0	5	4	0	1	0	1	0	1	0	0	FNI
17	11		1	0	0	0	1	B	C	1	0	1	1	1	1	0	0	TD 1 SF ALS
18	12		1	0	0	1	0	1	D	0	0	0	1	1	1	0	1	ALS TD1
19	13		1	0	0	1	1	B	9	1	0	1	1	1	0	0	1	TD1 SF ALS
20	14		1	0	1	0	0	9	9	1	0	0	1	1	0	0	1	ARSF TD1
21	15		1	0	1	0	1	F	F	1	1	1	1	1	1	1	1	SEM FET
22	16		1	0	1	1	0	9	C	1	0	0	1	1	1	0	0	TI1 S8 TD1
23	17		1	0	1	1	1	F	F	1	1	1	1	1	1	1	1	ALS FUNC
24	18		1	1	0	0	0	B	D	1	0	1	1	1	1	0	1	TD1
25	19		1	1	0	0	1	F	F	1	1	1	1	1	1	1	1	DR MALS
26	1A		1	1	0	1	0	9	9	1	0	0	1	1	0	0	1	MAR TD1
27	1B		1	1	0	1	1	F	F	1	1	1	1	1	1	1	1	MAR FUNC
28	1C		1	1	1	0	0	9	5	1	0	0	1	0	1	0	1	INS1 FI
29	1D		1	1	1	0	1	F	B	1	1	1	1	1	0	1	1	MALS TD1
30	1E		1	1	1	1	0	B	5	1	0	1	1	0	1	0	1	TD1 FI
31	1F		1	1	1	1	1	B	9	1	0	1	1	1	0	0	1	FUNC TD1
			4	3	2	1	0			8	7	6	5	4	3	2	1	

CPU CR8001/2/3
A.L. BOARD
T-FILE CONTROL PROM 2

sign/date	page
GB/770328	
prom-type 32x8.3st	cr-no: 1297-1

INPUT	ADDRESSES.							OUTPUT									
			E MDAT 20	D MDAT 19	C MDAT 18	B MDAT 17	A MDAT 16		MSB R 2.8 *	* R 2.7	R 2.6	R 2.5	R 2.4	R 2.3	* R 2.2	LSB R 2.1	
DEC.	HEX		4	3	2	1	0	HEX	8	7	6	5	4	3	2	1	DESCRIPTION
0	00		0	0	0	0	0	30	0	0	1	1	0	0	0	0	BCN OP
1	01		0	0	0	0	1	25	0	0	1	0	0	1	0	1	FN1
2	02		0	0	0	1	0	30	0	0	1	1	0	0	0	0	INS1
3	03		0	0	0	1	1	30	0	0	1	1	0	0	0	0	TD1
4	04		0	0	1	0	0	B0	1	0	1	1	0	0	0	0	x INC OUT
5	05		0	0	1	0	1	74	0	1	1	1	0	1	0	0	ARS FTD1
6	06		0	0	1	1	0	30	0	0	1	1	0	0	0	0	TD2
7	07		0	0	1	1	1	34	0	0	1	1	0	1	0	0	INS1 FI
8	08		0	1	0	0	0	B0	1	0	1	1	0	0	0	0	LAR
9	09		0	1	0	0	1	98	1	0	0	1	1	0	0	0	ALS TD1
10	0A		0	1	0	1	0	34	0	0	1	1	0	1	0	0	FI
11	0B		0	1	0	1	1	74	0	1	1	1	0	1	0	0	MAR TD1
12	0C		0	1	1	0	0	B0	1	0	1	1	0	0	0	0	ALS DR MAR
13	0D		0	1	1	0	1	21	0	0	1	0	0	0	0	1	TI1 S8 TD1
14	0E		0	1	1	1	0	21	0	0	1	0	0	0	0	1	TI1 S4 TD1
15	0F		0	1	1	1	1	34	0	0	1	1	0	1	0	0	TD1 FI
16	10		1	0	0	0	0	31	0	0	1	1	0	0	0	1	TD1 SW TD2
17	11		1	0	0	0	1	32	0	0	1	1	0	0	1	0	* TD1 SW MAR
18	12		1	0	0	1	0	74	0	1	1	1	0	1	0	0	INC in
19	13		1	0	0	1	1	30	0	0	1	1	0	0	1	0	DR MALS
20	14		1	0	1	0	0	38	0	0	1	1	1	0	0	0	ALS TD2
21	15		1	0	1	0	1	74	0	1	1	1	0	1	0	0	SEM FET
22	16		1	0	1	1	0	B0	1	0	1	1	0	0	0	0	SEM STO
23	17		1	0	1	1	1	34	0	0	1	1	0	1	0	0	MALS TD1
24	18		1	1	0	0	0	B0	1	0	1	1	0	0	0	0	TD2 SP ALS
25	19		1	1	0	0	1	74	0	1	1	1	0	1	0	0	TD1 SF ALS
26	1A		1	1	0	1	0	70	0	1	1	1	0	0	0	0	PUNCH MAR
27	1B		1	1	0	1	1	70	0	1	1	1	0	0	0	0	MAR FUNC
28	1C		1	1	1	0	0	70	0	1	1	1	0	0	0	0	MALS FUNC
29	1D		1	1	1	0	1	B0	1	0	1	1	0	0	0	0	x ALS FUNC
30	1E		1	1	1	1	0	70	0	1	1	1	0	0	0	0	FUNC MALS
31	1F		1	1	1	1	1	74	0	1	1	1	0	1	0	0	FUNC TD1
			4	3	2	1	0		8	7	6	5	4	3	2	1	

CPU CR 8001/2/3 A.L. BOARD PSW : CONTROL PROM	sign/date GB/770328	page
	prom-type 32x8.3st	cr-no: 1300-1

INPUT ADDRESSES.									OUTPUT									
			MDAT 35 E	MDAT 34 D	MDAT 32 C	MDAT 33 B	MDAT 36 A			M S B FORCE CPU INT(H)	SEL ARLD	EN MOD	SUEN PSW	INT CL 1	INT CL 0	CC PAR PSW	CCP PSW L S B	
DEC.	HEX		4	3	2	1	0	HEX		8	7	6	5	4	3	2	1	DESCRIPTION
0	00		0	0	0	0	0	5	C	0	1	0	1	1	1	0	0	OP NOP ✓
1	01		0	0	0	0	1	5	C	0	1	0	1	1	1	0	0	INC X1X2 ✓
2	02		0	0	0	1	0	5	C	0	1	0	1	1	1	0	0	LD OP ✓
3	03		0	0	0	1	1	5	C	0	1	0	1	1	1	0	0	INC X1 ✓
4	04		0	0	1	0	0	7	C	0	1	1	1	1	1	1	0	TM OD O
5	05		0	0	1	0	1	5	C	0	1	0	1	1	1	0	0	DEC X1 ✓
6	06		0	0	1	1	0	5	C	0	1	0	1	1	1	0	0	LD RAM
7	07		0	0	1	1	1	5	8	0	1	0	1	1	0	0	0	CL TM
8	08		0	1	0	0	0	5	C	0	1	0	1	1	1	0	0	CL RAM
9	09		0	1	0	0	1	7	0	0	1	0	1	0	0	0	0	CL CPU
10	0A		0	1	0	1	0	5	C	0	1	0	1	1	1	0	0	EX RAM
11	0B		0	1	0	1	1	5	4	0	1	0	1	0	1	0	0	CL I/O
12	0C		0	1	1	0	0	5	C	0	1	0	1	1	1	0	0	EX PROM
13	0D		0	1	1	0	1	5	C	0	1	0	1	1	1	0	0	EX RAM LD
14	0E		0	1	1	1	0	5	E	0	1	0	1	1	1	1	0	* SET COND O
15	0F		0	1	1	1	1	F	F	1	1	1	1	1	1	1	1	
16	10		1	0	0	0	0	D	C	1	1	0	1	1	1	0	0	CPU INT
17	11		1	0	0	0	1	F	F	1	1	1	1	1	1	1	1	
18	12		1	0	0	1	0	I	F	0	0	0	1	1	1	1	1	Ô I-PSW
19	13		1	0	0	1	1	F	F	1	1	1	1	1	1	1	1	
20	14		1	0	1	0	0	4	C	0	1	0	0	1	1	0	0	PSW-I
21	15		1	0	1	0	1	F	F	1	1	1	1	1	1	1	1	
22	16		1	0	1	1	0	5	C	0	1	0	1	1	1	0	0	LD X1X2 ✓
23	17		1	0	1	1	1	F	F	1	1	1	1	1	1	1	1	
24	18		1	1	0	0	0	5	C	0	1	0	1	1	1	0	0	INC X2 ✓
25	19		1	1	0	0	1	F	F	1	1	1	1	1	1	1	1	
26	1A		1	1	0	1	0	5	C	0	1	0	1	1	1	0	0	LD X1 ✓
27	1B		1	1	0	1	1	F	F	1	1	1	1	1	1	1	1	
28	1C		1	1	1	0	0	5	C	0	1	0	1	1	1	0	0	LD X2 ✓
29	1D		1	1	1	0	1	F	F	1	1	1	1	1	1	1	1	
30	1E		1	1	1	1	0	5	C	0	1	0	1	1	1	0	0	DEC X2 ✓
31	1F		1	1	1	1	1	F	F	1	1	1	1	1	1	1	1	
			4	3	2	1	0			8	7	6	5	4	3	2	1	

CPU CR 8001/2/3
A.L. BOARD
SHIFT CONTROL PROM

sign/date	page
GB/770328	
prom-type 32x8.3st	cr-no: 1301-1

R SEL/Q SEL	R SEL	Q SE
2 1 0	RAM	Q REG
0 0 0	SQL	SQL
0 0 1	SQM	SQM
0 1 0	SRL	SRL
0 1 1	SRM	SRM
1 0 0	SIGN	SIGN
1 0 1	SOOV	SIGN
1 1 0	NC	NC
1 1 1	"0"	"0"

INPUT ADDRESSES.								OUTPUT										
		A3,2,1,0	GSQL E	AA1 D	AA0 C	AA3 B	AA2 A			RESET IA 19 MSB	RESET IA 18	R SEL 2	R SEL 1	R SEL 0	Q SEL 2	Q SEL 1	Q SEL 0 LSB	
DEC.	HEX	HEX	4	3	2	1	0	HEX		8	7	6	5	4	3	2	1	DESCRIPTION
0	00	[illegible]	0	0	0	0	0	F	F	1	1	1	1	1	1	1	1	LL [illegible]
1	01	4	0	0	0	0	1	F	F	1	1	1	1	1	1	1	1	RL [illegible]
2	02	2	0	0	0	1	0	D	0	1	1	0	1	0	0	0	0	RC
3	03	C	0	0	0	1	1	7	F	0	1	1	1	1	1	1	1	BYTE UB
4	04	1	0	0	1	0	0	F	B	1	1	1	1	1	0	1	1	LLL [illegible]
5	05	5	0	0	1	0	1	C	7	1	1	0	0	0	1	1	1	RLL [illegible]
6	06	9	0	0	1	1	0	C	2	1	1	0	0	0	0	1	0	RCL
7	07	D	0	0	1	1	1	E	A	1	1	1	0	1	0	1	0	MUL
8	08	[illegible]	0	1	0	0	0	D	9	1	1	0	1	1	0	0	1	LC [illegible]
9	09	6	0	1	0	0	1	E	5	1	1	1	0	0	1	0	1	RA [illegible]
10	0A	A	0	1	0	1	0	F	F	1	1	1	1	1	1	1	1	
11	0B	[illegible]	0	1	0	1	1	F	F	1	1	1	1	1	1	1	1	
12	0C	[illegible]	0	1	1	0	0	C	B	1	1	0	0	1	0	1	1	LCL [illegible]
13	0D	7	0	1	1	0	1	F	A	1	1	1	1	1	0	1	0	RLL ?
14	0E	E	0	1	1	1	0	C	C	1	1	0	0	1	1	0	0	DIV
15	0F	F	0	1	1	1	1	3	F	0	0	1	1	1	1	1	1	I/O
16	10		1	0	0	0	0	F	F	1	1	1	1	1	1	1	1	LL
17	11		1	0	0	0	1	F	F	1	1	1	1	1	1	1	1	RL
18	12		1	0	0	1	0	D	0	1	1	0	1	0	0	0	0	RC
19	13		1	0	0	1	1	B	F	1	0	1	1	1	1	1	1	BYTE LB
20	14		1	0	1	0	0	F	B	1	1	1	1	1	0	1	1	LLL
21	15		1	0	1	0	1	C	7	1	1	0	0	0	1	1	1	RLL
22	16		1	0	1	1	0	C	2	1	1	0	0	0	0	1	0	RCL
23	17		1	0	1	1	1	E	A	1	1	1	0	1	0	1	0	MUL
24	1.8		1	1	0	0	0	D	9	1	1	0	1	0	0	1	1	LC
25	19		1	1	0	0	1	E	5	1	1	1	0	0	1	0	1	RA
26	1A		1	1	0	1	0	F	F	1	1	1	1	1	1	1	1	
27	1B		1	1	0	1	1	F	F	1	1	1	1	1	1	1	1	
28	1C		1	1	1	0	0	C	B	1	1	0	0	1	0	1	1	LCL
29	1D		1	1	1	0	1	F	A	1	1	1	1	1	0	1	0	RLL
30	1E		1	1	1	1	0	C	C	1	1	0	0	1	1	0	0	DIV
31	1F		1	1	1	1	1	3	F	0	0	1	1	1	1	1	1	I/O
			4	3	2	1	0			8	7	6	5	4	3	2	1	

ARITHMETICAL LOGICAL BOARD (ALB)	sign/date GB/780524	page
	repl	project

6

SIGNAL LISTS

MICRO PROGRAM BOARD (MPB) WIRE LIST W3	sign/date GB/780315	page
	repl	project
PLUG TYPE :	P/N 5.58102-08	
CABEL TYPE: 16 WIRES FLAT CABLE		
LENGTH :		

REFERENCE DESIGNATION	MPB P3 (H4)
	ALB J3

PIN NO.	SIGNAL NAME	INPUT/OUTPUT
1	MDAT 20	0
2	MDAT 7	0
3	MDAT 16	0
4	MDAT 19	0
5	GND	
6	MDAT 17	0
7	MDAT 18	0
8	GND	
9	GND	
10	I BUS 0	I/O
11	I BUS 1	I/O
12	I BUS 2	I/O
13	I BUS 3	I/O
14	I BUS 15	I/O
15	I BUS 7	I/O
16	GND	

MICRO PROGRAM BOARD (MPB) WIRE LIST W4	sign/date GB/770315	page
	tepl	project
PLUG TYPE :	P/N 5.58102-02	
CABEL TYPE : 16 WIRES FLAT CABLE		
LENGTH :		

REFERENCE DESIGNATION	MPB P4 (I1)
	ALB J4

PIN NO.	SIGNAL NAME	INPUT/OUTPUT
1	MDAT 35	0
2	MDAT 34	0
3	GND	
4	MDAT 32	0
5	MDAT 33	0
6	GND	
7	MDAT 36	0
8	GND	
9	SES	I
10	SEO	I
11	SEZ	I
12	SEC	I
13	I/O PENDING	I
14	SOO	I
15	Q1	I
16	TIME OUT	I

MICRO PROGRAM BOARD (MPB) WIRE LIST W5		sign/date GB/770315	page
		repl	project
PLUG TYPE :		P/N 5.58102-04	
CABEL TYPE: 16 WIRES FLAT CABLE			
LENGTH :			
REFERENCE DESIGNATION	MPB P5 (I3)		
	ALB J5		

PIN NO.	SIGNAL NAME	INPUT/OUTPUT
1	MDAT 0	0
2	GND	
3	MDAT 5	0
4	MDAT 4	0
5	MDAT 6	0
6	MDAT 22	0
7	TIMER INT	I
8	MODIFY	I
9	POWER DETECT	I
10	CPU INT	I
11	GND	
12	OP8	0
13	GND	
14	OP0	0
15	OP2	0
16	OP1	0

MICRO PROGRAM BOARD (MPB) WIRE LIST W6	sign/date GB/770315	page
	repl	project

PLUG TYPE :	P/N 5.58102-07
CABEL TYPE : 16 WIRES FLAT CABLE	
LENGTH :	

REFERENCE DESIGNATION	MPB P6 (I5)
	ALB J6

PIN NO.	SIGNAL NAME	INPUT/OUTPUT
1	BA1	0
2	BA0	0
3	GND	
4	MDAT 1	I
5	BA3	0
6	BA2	0
7	AA1	0
8	AA0	0
9	GND	
10	AA2	0
11	AA3	0
12	GND	
13	MDAT 2	0
14	MDAT 3	0
15	MDAT 21	0
16	MDAT 23	0

ALB TO BIB INTERCONNECTIONS SIGNAL LIST	sign/date GB/780524	page 1/5
	tepl	project

PLUG TYPE :	P/N
CABEL TYPE: 16 WIRES FLAT CABLE	
LENGTH :	

REFERENCE DESIGNATION	ALB P1 (C3)
	BIB J1 (C1)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE:ALB
1	T-BUS 11	I/O
2	T-BUS 10	I/O
3	T-BUS 9	I/O
4	T-BUS 8	I/O
5	I CPU INT (H)	I
6	ENSH (L)	I
7	EN ALS OUT (L)	I
8	GND	
9	T-BUS 12	I/O
10	T-BUS 13	I/O
11	T-BUS 14	I/O
12	T-BUS 15	I/O
13	T-BUS 3	I/O
14	T-BUS 2	I/O
15	T-BUS 1	I/O
16	T-BUS 0	I/O

ALB TO BIB INTERCONNECTIONS
SIGNAL LIST

sign/date GB/0524

page 2/5

repl

project

PLUG TYPE :

CABEL TYPE : 16 WIRES FLAT CABLE

P/N

LENGTH :

REFERENCE DESIGNATION	ALB	P2	(C5)
	BIB	J2	(C3)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE : ALB
1	T-BUS 7	I/O
2	T-BUS 6	I/O
3	T-BUS 5	I/O
4	T-BUS 4	I/O
5	CPALS	I
6	$\overline{\text{CPALS}}$	I
7	CPMCU	I
8	GND	
9	GND	
10	PER0 (L)	I
11	PER0 (H)	I
12	PER2 (H)	I
13	GND	
14	LDMCU (L)	I
15	LDMCU (H)	I
16	GND	

400-741

ALB TO BIB INTERCONNECTION SIGNAL LIST	sign/date GB/780524	page 3/5
	repl	project

PLUG TYPE :	P/N
CABEL TYPE: 16 WIRES FLAT CABLE	
LENGTH :	

REFERENCE DESIGNATION	ALB P3 (D1)
	BIB J3 (D1)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE: ALB
1	GND	
2	FORCE CPU INT (H)	0
3	II/OI (H)	I
4	ITI (H)	I
5	$\overline{\mathrm{P0}}$	I
6	$\overline{\mathrm{P1}}$	I
7	ITRQ (H)	I
8	GND	
9	GND	
10	$\overline{\mathrm{CPMCU}}$	I
11	DCL (L)	I
12	PARITY ERROR	0
13	$\overline{\mathrm{8MHz}}$	I
14	$\overline{\mathrm{8MHz}}$	I
15	$\overline{\mathrm{2MHz}}$	I
16	GND	

ALB TO BIB INTERCONNECTION SIGNAL LIST	sign/date GB/780524	page 4/5
	repl	project

PLUG TYPE :		P/N
CABEL TYPE :	16 WIRES FLAT CABLE	
LENGTH :		

REFERENCE DESIGNATION	ALB	P4	(D3)
	BIB	J4	(D3)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE: ALB
1	AA1	0
2	OP2	0
3	OP0	0
4	AA2	0
5	AA0	0
6	OP1	0
7	DPER0 (H)	I
8	GND	
9	DPER1 (H)	I
10	LD-DREG (H)	0
11	RLP	I
12	RUP	I
13	IUP	0
14	ILP	0
15	SEA17	0
16	SEA16	0

ALB TO BIB INTERCONNECTION SIGNAL LIST	sign/date GB/780524	page 5/5
	repl	project
PLUG TYPE :	P/N	
CABEL TYPE: 16 WIRES FLAT CABLE		
LENGTH :		
REFERENCE DESIGNATION	ALB P5 (J7)	
	BIB J5 (G1)	

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE: ALB
1	TO (L)	I
2	POWER DET MP	I
3	POWER DET AL	0
4	PRESET TIMING (L)	I
5	$\overline{\text{ADDO}}$	0
6	I/O (L)	0
7	BUSTRF (H)	I
8	GND	
9	I R/W	I
10	MDAT 16	0
11	MDAT 17	0
12	MDAT 18	0
13	MDAT 19	0
14	MDAT 20	0
15	IA 19	0
16	IA 18	0

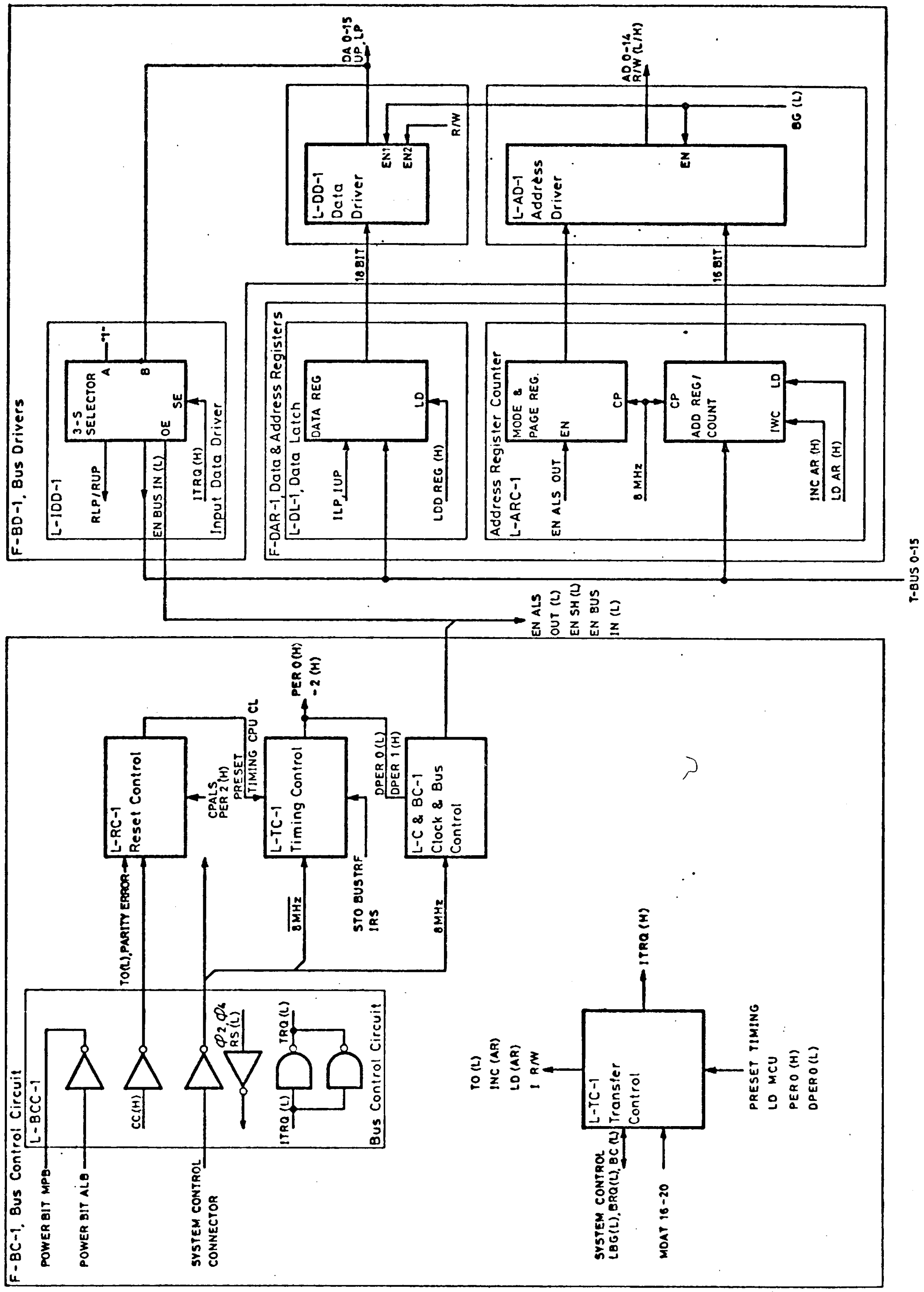
BUS INTERFACE BOARD (BIB) MB	sign/date GB/780524	page
	repl	project

1. INTRODUCTION

The BIB is the bus interface for the CPU CR8001/2. The board contain the circuit necessary for transferring of data on the CR80 Main Bus.
The BIB is connected to the CR80 system by a 86 pins edge connector for the Main Bus and a 48 pins connector for the system control connections the communication between the BIB and the two other board in the CPU ALB & MPB is carried out on flat cables and discreet wires for the power.

2. GENERAL DESCRIPTION

The BIB has different function in the CPU. The board supply the module with the necessary timing signals derived from the CR80 system master timing signal Ø4. All the receivers and drivers for the external connections are located on the board together with the 20 bits address register/counter and temporary storage for the data and corresponding parity bits (DATA Reg).
The data and addresses transferred to/from the ALB is done via the internal 16 bits CPU bus T-BUS.
The set up of the BIB to execute the different bus transfers is from the µ program output. The handshaking circuit related to the MBC communication for Main Bus authority control is on the BIB also.



CHRISTIAN ROVSING A/S

Scale		Approved	Issue	
Date			Date	
Drawn			Approved	
Parts no				
Print no		Sheet of sheets		

3. SPECIFICATIONS

The BIB is one of the 3 PCB in the CPU CR8001/2 and interface the module to the CR80 Main Bus and system control connections.

3.1 Main Bus Connection

The Main Bus connection is a CR80 standard 86 poles edge connector with the pin configuration and signal specification as described in table 3.1 a & b.

3.2 System Control Connection

The connector used for the system control signal is a CR80 standard 48 pin connector mounted above the 86 poled edge connector.
The pin configuration and signal specifications is described in table 3.2 a & b.

3.3 Power Interface

Input power +5V is from the Main Bus connector power to ALB & MPB is supplied through two discreet wires soldered on the board.

Power Consumption:

+5V : ± A

3.4 Mechanical Dimension

Standard CR80 PCB 183.4 x 305mm with two connectors one 86 pin Main Bus edge connector & one 48 pin system control connector.

Height of component side : 8 mm
Height of soldering side : 8 mm

3.5 Data Transfer Rate

Max. transfer : 2.7 M word
Min. Bus time : 250 ns

3.6 Main Bus Addressing

Control 20 bits address including 2 mode bits for : I/O, L Byte, U Byte & Word.
Memory addressing of 256 K word or 512 K byte.

3.7 Data Word

16 bits word plus one parity bit for each byte LB & UB, ODD parity.

3.8 Internal Connections

The BIB is connected to the ALB with five pcs. 16 wires flat cables ref. signal lists section 5.

TABLE 3.1.a

- MAIN BUS CONNECTOR - PIN LAYOUT

2 x 43 pin edge connector rear view

	A		B	
	gnd	1	gnd	
DATA (DA)	0	2	1	DATA (DA)
	2	3	3	
	4	4	5	
	6	5	7	
	8	6	9	
	10	7	11	
	12	8	13	
	14	9	15	
	gnd	10	gnd	
	Auxiliary power	11	auxiliary power (same as All)	
	-12V	12	-12V	
	gnd	13	gnd	
	+12V	14	+12V	
	gnd	15	gnd	
ASSRESS (AD)	0	16	1	ADDRESS (AD)
	2	17	3	
	4	18	5	
	6	19	7	
	gnd	20	gnd	
	8	21	9	
	10	22	11	
	12	23	13	
	14	24	15	
	16	25	17	
	18	26	19	
	gnd	27	gnd	
UP	16	28	17	LP
	AUX	29	MC(H)	
	RS(L)	30	gnd	
	TRQ(L)	31	gnd	
	INA(H)	32	gnd	
	INR(L)	33	gnd	
	R/W(L/H)	34	gnd	
	Ø 1	35	gnd	
	Ø 2	36	gnd	
	Ø 3	37	gnd	
	Ø 4	38	gnd	
	gnd	39	gnd	
	+5V	40	+5V	
	+5V	41	+5V	
	gnd	42	gnd	
	gnd	43	gnd	

K

TABLE 3.1.b

MAIN BUS ELECTRICAL INTERFACE SPECIFICATION POWER LINES

Aux. power	pin A11, B11
$-12V \, ^{+\,0.2V}_{-\,0V}$	pin A12, B12
Gnd	pin A13, B13
$+12V \, ^{+\,0.2V}_{-\,0V}$	pin A14, B14
$+5V \, ^{+\,0.2V}_{-\,0V}$	pin A40, A41, B40, B41
Gnd	pin A42, A43, B42, B43

The power lines are not feed through the Main Bus Extension and therefore different power supplies are used for the different Mother Boards.

The max. currents supplied through one connector are as specified below:

+12V, -12V,	I max:	2 A
+ 5V ,	I max:	12 A

SIGNAL LINES

The levels for all the Main Bus signals are normal TTL logic levels. i.e.:

High level: $2.0V \leq V_H \leq 5.0V$

Low level : $0V \leq V_L \leq 0.8V$

The load on the different signal lines for one module are as specified on the next page, (all currents are numerical values).

TABLE 3.1.b

DATA LINES & ADDRESS LINES

DA0 - DA15, UP & LP, AD0 - AD19 & R/W (L/H).

3 - state signals with the followings requirements:

Drivers:		$I_{0H} \geq 5.2$ mA
		$I_{0L} \geq 16.0$ mA
		$I_{0\ off} \leq 100$ uA
Receivers:		$I_{IH} \leq 100$ uA
		$I_{IL} \leq 0.5$ mA
	(1)	$I_{IL} \leq 2$ mA

Note 1: This low level input current is only allowed when the module is addressed.

MASTER CLEAR

MC(H):
Open collector with the following requirements.

Driver:		$I_{0L} \geq 60$ mA
		$I_{0H} \leq 250$ uA
Receiver Schmitt Trigger:		$I_{IH} \leq 100$ uA
		$I_{IL} \leq 0.5$ mA
	(1)	$I_{IL} \leq 2$ mA

Note 1: I_{IL} 2 mA is only allowed for the Main Bus Controller & Main Bus Terminatio

TRANSFER REQUEST

TRQ (L):

Open collector or 3 - state signal with the following

TABLE 3.1.b

requirements:

Driver:	$I_{0L} \geq$	80	mA
	$I_{0H} \leq$	250	uA
Receiver Schmitt Trigger:	$I_{IH} \leq$	100	uA
	$I_{IL} \leq$	0.5	mA
	(1) $I_{IL} \leq$	2	mA

Note 1: I_{IL} 2 mA is only allowed for the Main Bus Controller & RAM modules with a memory area of 8K word or more.

CLOCK SIGNALS

Ø4 - Ø1:

Driver:	$I_{0L} \geq$	120	mA
	$I_{0H} \geq$	80	mA
Receiver Schmitt Trigger:	$I_{IL} \leq$	2	mA
	$I_{IH} \leq$	100	uA

TABLE 3.2.a

SYSTEM CR 8001/2 SYSTEM CONTROL CONNECTIONS BIB (MB) 48 Pin Connector Pin Assignment	sign/date GB/780525	page
	repl	project

Pin no.	Signal Description	Pin no.	Signal Description	Pin no.	Signal Description
1a	BG (L)	1b	GND	1c	BRQ (L)
2a		2b		2c	
3a		3b		3c	
4a		4b		4c	
5a		5b		5c	
6a		6b		6c	
7a		7b		7c	
8a		8b		8c	
9a		9b		9c	
10a	GND	10b	GND	10c	CC (H)
11a	LBG (L)	11b	P0	11c	INT (L)
12a	CPI (L)	12b	TI (L)	12c	P1
13a		13b		13c	
14a		14b		14c	
15a		15b	GND	15c	GND
16a		16b		16c	

TABLE 3.2.b

SYSTEM CONTROL CONNECTIONS ELECTRICAL INTERFACE SPECIFICATION

The levels for all the System Control Connections are normal TTL logic levels i.e.

High level: $2.0V < V_H < 5.0V$
Low level: $0 \ V < V_L < 0.8V$

The specifications below are for the numerical current values for one module connected with the signals.

Main Bus Authority Control Signals

BRQ (L), BG (L)

Driver: $I_{OL} \geq 48mA$

Receiver: $I_{IH} \leq 100uA$
$I_{IL} \leq 2mA$

LBG (L)
Open collector signal:

Driver: $I_{OL} \geq 48mA$
$I_{OH} \leq 100uA$

Reciever: $I_{IH} \leq 100uA$
$I_{IL} \leq 2mA$

TABLE 3.2.b

CPU Interrupt

CPI (L)

Open collector signal:

Driver:	$I_{OL} \geq$ 60mA
	$I_{OH} \leq$ 100uA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 2mA

CPU Clear

CC (H)

Open collector signal:

Driver:	$I_{OL} \geq$ 60mA
	$I_{OH} \leq$ 100uA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 2mA

I/O Interrupt Signals & Timer Interrupt

INT (L), P0, P1, TI (L)

Driver:	$I_{OL} \geq$ 60mA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 2mA

4. FUNCTIONAL DESCRIPTION

This section gives a detailed description of the CR8001/2 Bus Interface Board.
The board contain the circuit necessary for interfacing the ALB to the CR80 system Main Bus and system control connections. Synchronization of the internal CPU sequences, storage of data and addresses and receiver/driver circuit for the external connections are located on the BIB.

The BIB is divided in the following functional blocks.

1.	Bus Control Circuit	F-BC-1
2.	Data & Address Register	F-DAR-1
3.	Bus Drivers	F-BF-1

4.1 Bus Control Circuit F-BC-1

Synchronization of the whole CPU is controlled from F-BC-1 by means of different timing & handshaking signals, derived from the CR80 master clock Ø4.
The F-BC-1 controls the handshaking procedure for the system control connections, e.g Main Bus authority control, and for the data transfer on the Main Bus.
Five logical blocks are contained in these functional block, they are:

1.	Bus Control Circuit	L-BCC-1
2.	Reset Control	L-RC-1
3.	Timing Control	L-TC-1
4.	Clock & Bus Control	L-C&BC-1
5.	Transfer Control	L-TC-1

4.1.1 Bus Control Circuit L-BCC-1

The control and timing signals from the system control module MBC, SCM and from the Main Bus are received by schmitt triggers located in L-BCC-1.
The detector and driver for the front panel led is also included.

4.1.2 Reset Control L-BC-1

When the BIB recognize a CPU clear CC(H) the whole CPU will be reset by the signals:
PRESET TIMING, CPU CL & LD MCU.
To make a qualified reset the reset signal is synchronized to the CPU timing signals CPALS & PER2(H) ref. timing diagram fig. 4.1.2.
If a parity error is detected on the ALB the signal PARITY ERROR will go low and force a reset of the module. The same function has the time out detection in the Transfer Control (TO(L)). Ref. fig. 4.1.2 for detailed signal relationship.

Timing Control L-TC-1

4.1.3 The internal CPU timing is divided in three periodes PER 0, PER 1 & PER 2.
The width of the periodes is nominal 125 ns, but when accessing the Main Bus PER 2 will be extended until the module respons RS(L) arrive from the addressed module. If a CPU Clear, time out or parity error occurs the circuit will be reset to PER 0 ref. timing diagram fig. 4.1.3 and fig. 4.1.2.

4.1.4 Clock & Bus Control L-CBC-1

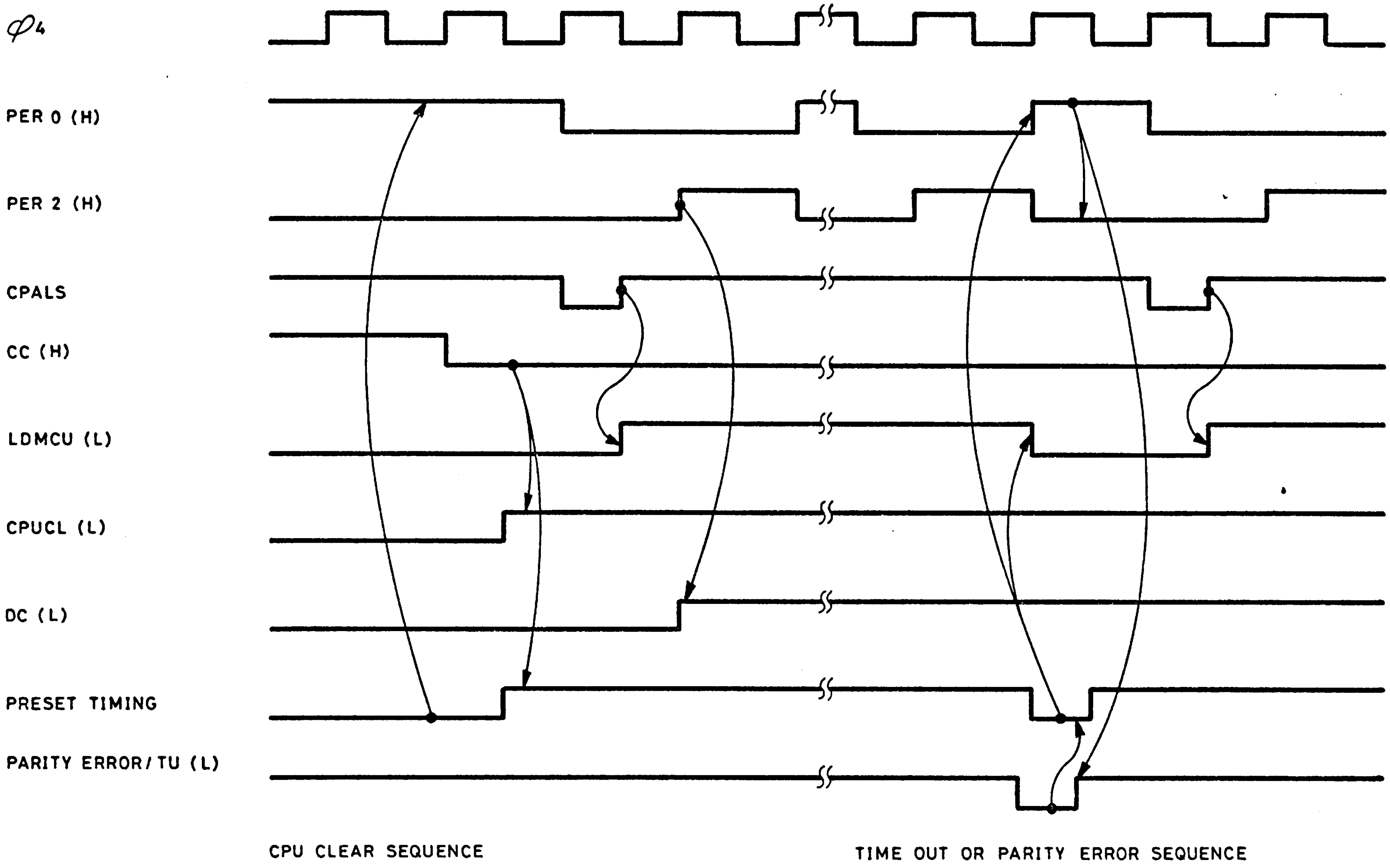
Synchronization of the internal bus, the T-BUS is carried out in these logical blocks, and the generation of the two clocks CPMCU & CPALS is decoded from the timing signals from the Timing Control. Fig. 4.1.4 specify the relationship between the timing signals and the outputs CPALS, CPMCU & the T-BUS enable signals.

4.1.5 Transfer Control L-TC-1

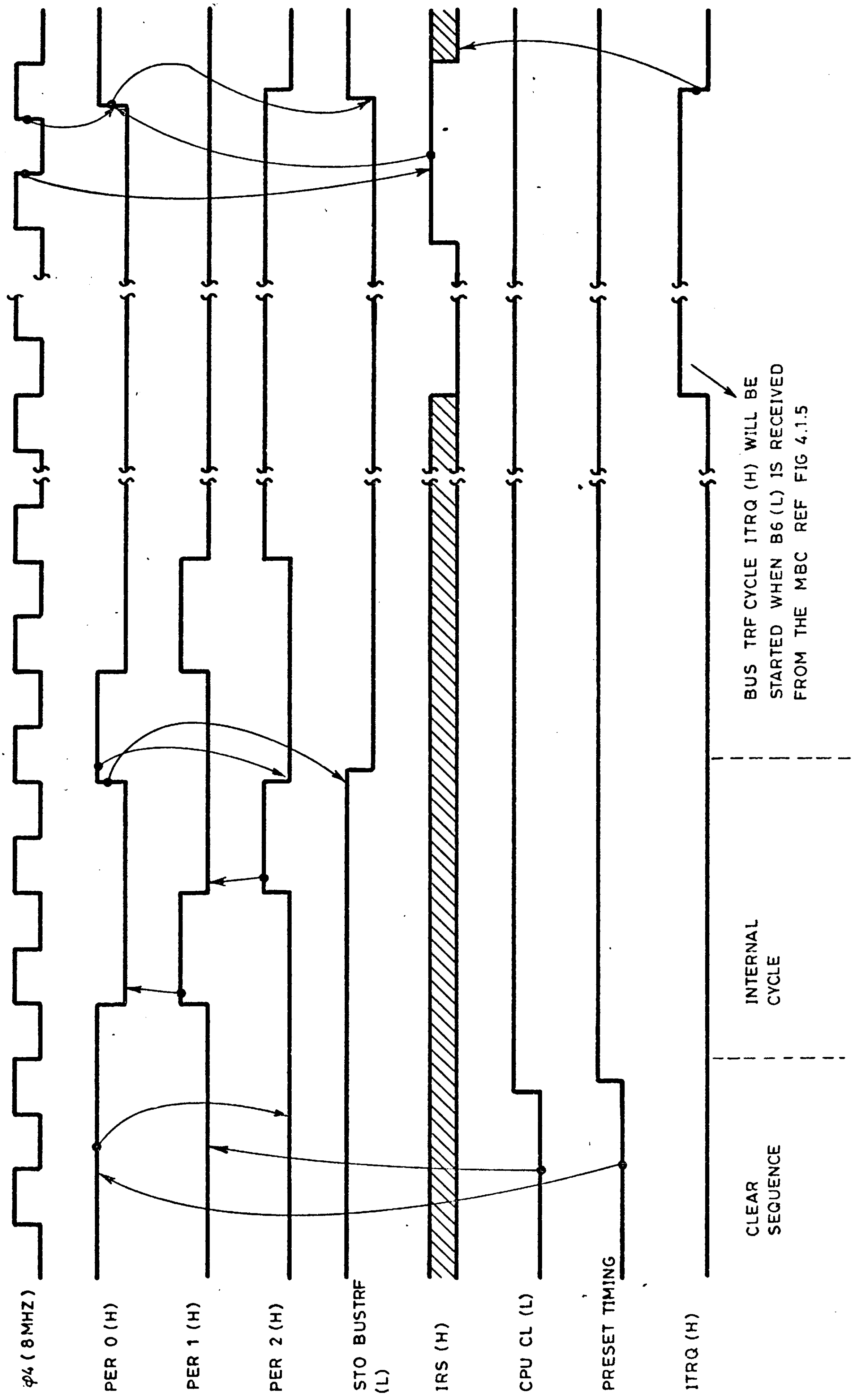
The bus controlling μprogram outputs MDAT 16-20 are input to a PROM CR1290 where a conversion to the relevant signals for the BIB is carried out. The output control the Main Bus authority signals, Main Bus transfer signals and the internal R/W signal used for specifying the transfer CPU Module and thereby the enabling of the data drivers. For more detailed timing relations ref. fig. 4.1.5.
PROM table for CR1290 ref. section 5.

Reset Control Timing Diagram

Fig. 4.1.2



Timing Control Timing Diagram



BUS TRF CYCLE ITRQ (H) WILL BE STARTED WHEN B6 (L) IS RECEIVED FROM THE MBC REF FIG 4.1.5

Fig. 4.1.3

Clock & Bus Control Timing Diagram

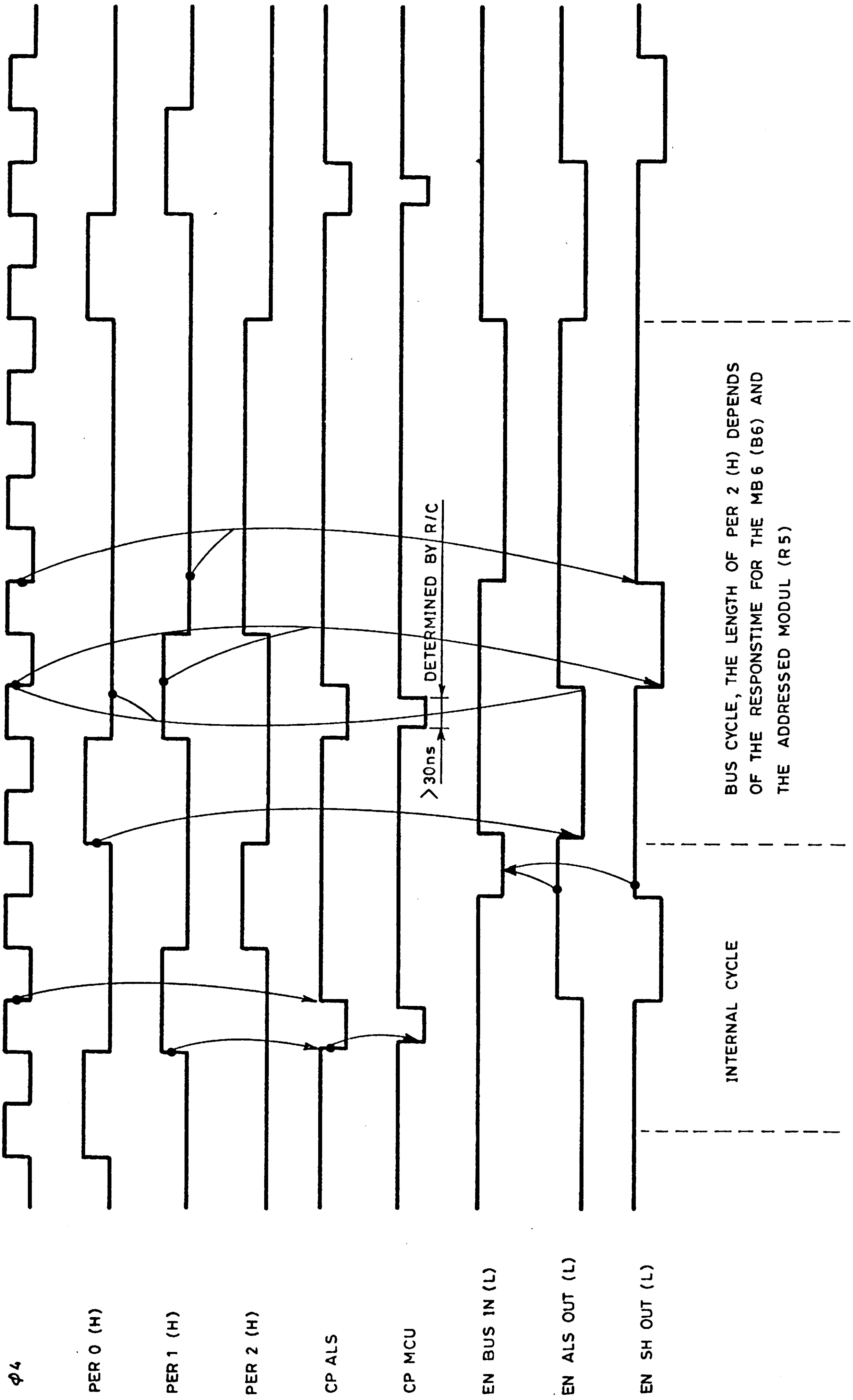


Fig. 4.1.4

Transfer Control Timing Diagram

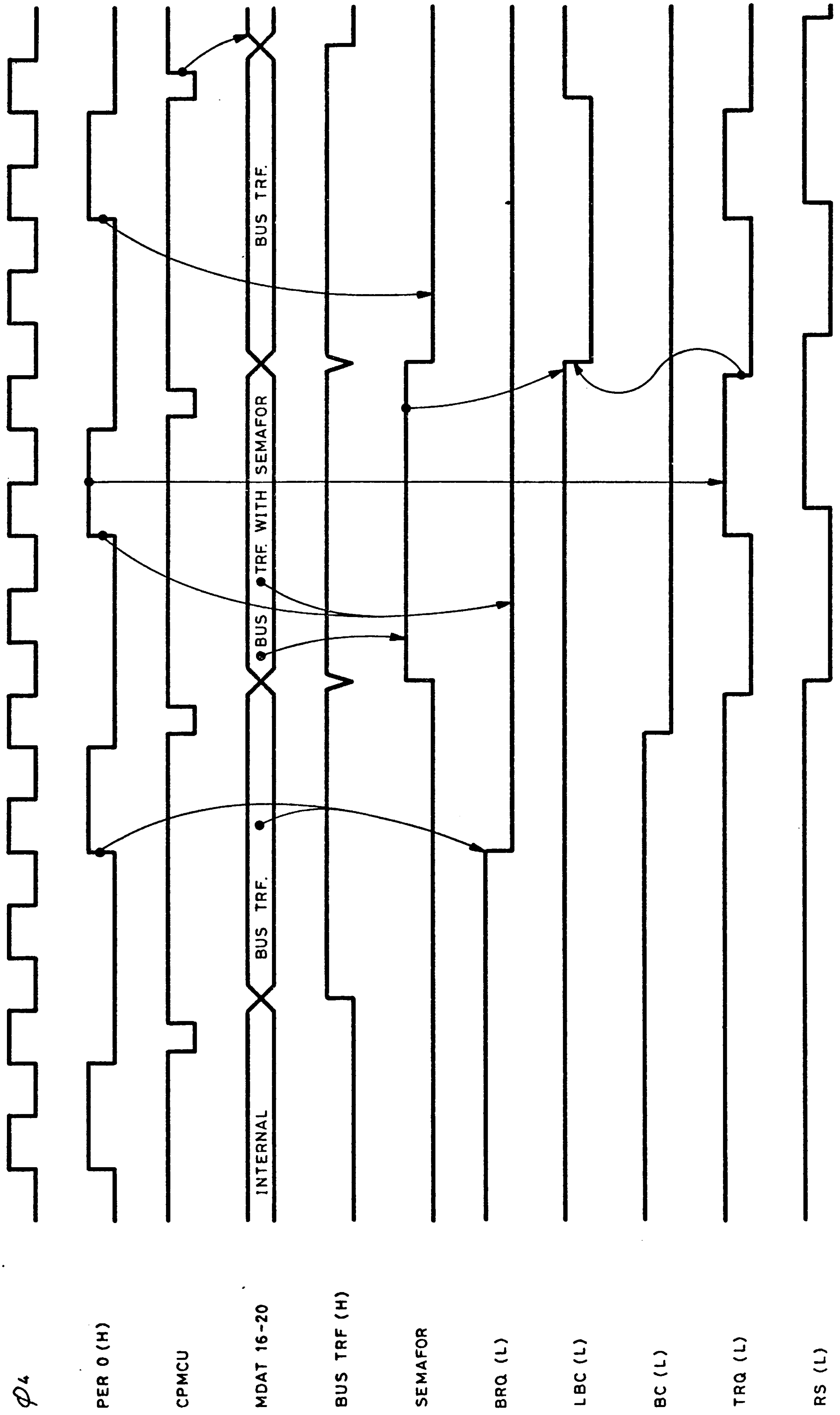


Fig. 4.1.5

4.2 Data. & Addressing Registers F-DAR-1

The contents on the T-BUS are stored in the Data or Address Register, when it shall be used for transfer on the Main Bus. The control of the data register loading is carried out from the BIB (T-File control) while the address register is controlled from the bus control PROM CR1290 located in the Bus Control Circuit. Beside the loading function the 16 least significate bits of the address register can be controlled as a counter from CR1290.
F-DAR-1 consist of two logic blocks.

1.	Data Latch	L-DL-1
2.	Address Register/Counter	L-ARC-1

4.2.1 Data Latch L-DL-1

The input to the Data Latch is the T-BUS and the two parity bits generated on the ALB one for each byte, upper byte & lower byte. The output is input to the Main Bus data drivers.
Timing diagram 4.2.1 specify the three possible load times for the latch.

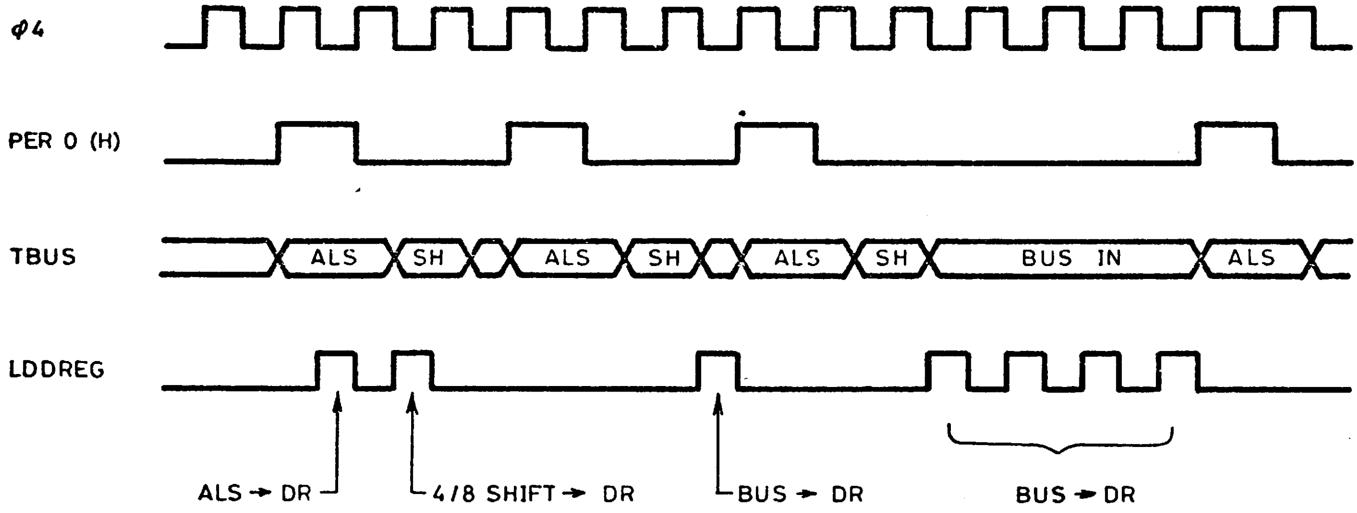
4.2.2 Address Register/Counter L-ARC-1

The 16 bits word address for the Main Bus transfer is always loaded into the address counter section in the T-BUS ALS Out time. When the register is incremented it is done in the same time slot.
This part of the address register is controlled from bus controlling PROM CR1290.
The remaining part of the address field the SR/W mode & page bits is stored in a separate register

in the EN ALS output period. The input comes from the AL Board.

Control of the address register is illustrated in timing diagram fig. 4.2.2.

Data Latch Timing Diagram



ALS → DR

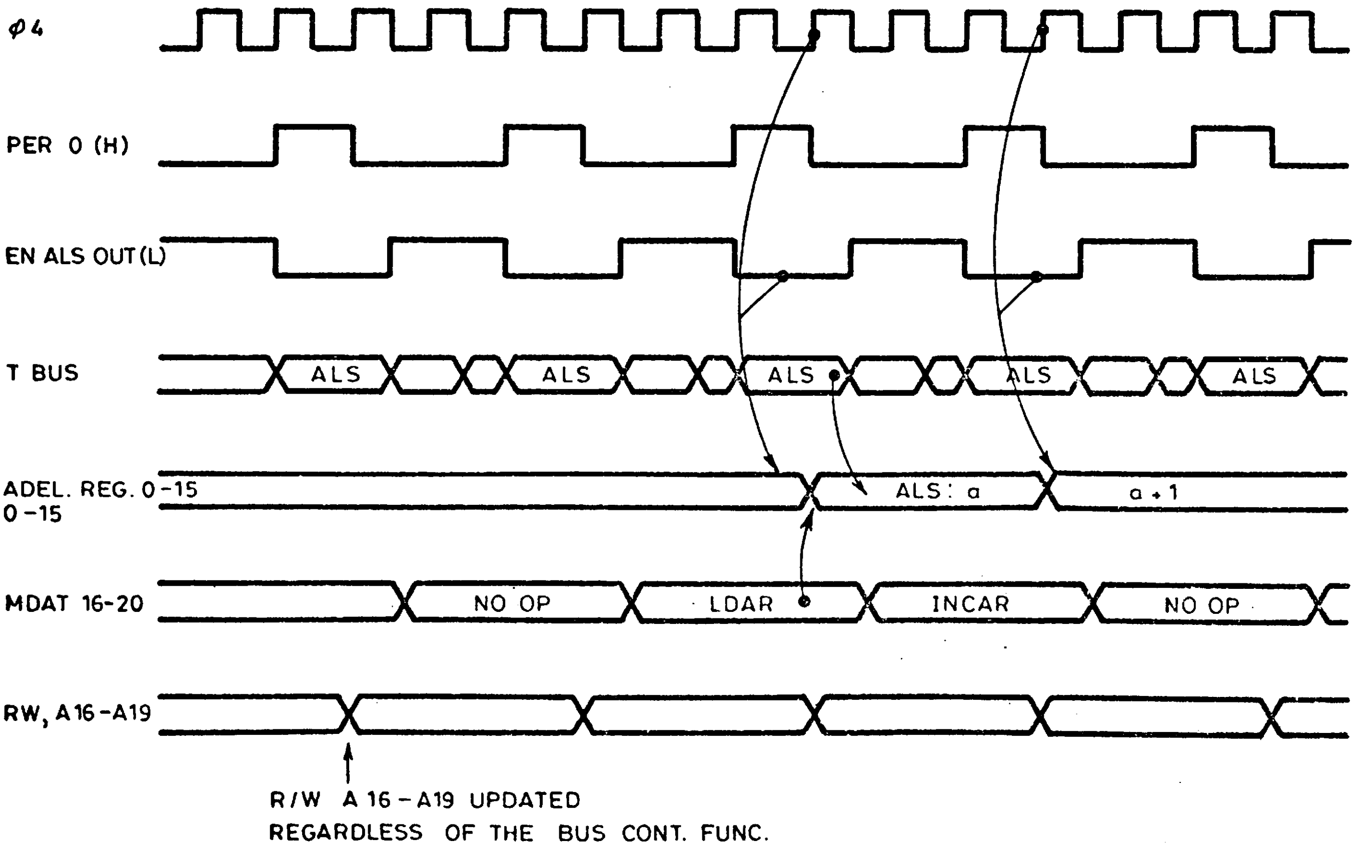
4/8 SHIFT → DR

BUS → DR

BUS → DR

Fig. 4.2.1

Address Register / Counter Timing Diagram



R/W A16-A19 UPDATED
REGARDLESS OF THE BUS CONT. FUNC.

Fig. 4.2.2

4.3 Bus Drivers F-BD-1

This functional block consist of the 3-state driver for the Main Bus data- and address lines and for the interface between the Main Bus to T-BUS drivers. There are three logical blocks in F-BD-1.

1. Address Drivers L-AD-1
2. Data Drivers L-DD-1
3. Input Data Drivers L-IDD-1

4.3.1 Address Drivers L-AD-1

The L-AD-1 consist of 3 state drivers for interfacing the 20 address lines and the R/W signal to the Main Bus lines. The output are enabled direct by the BG signal from the MBC, SCM.

4.3.2 Data Drivers L-DD-1

The circuit for interfacing the data register to the Main Bus data lines consist of inverting 3-state drivers. The outputs are enabled when BG from the MBC is active (low) and the transfer to be executed is a write operation R/W : "1".

4.3.3 Input Data Drivers L-IDD-1

The L-IDD-1 consist of a 16 bits 3-state selector for transferring of the Main Bus data line contents to the T-BUS. The output from the selector is enabled synchronous with the CPU's internal timing (EN BUS IN (L)) but the selection of the Main Bus and input is only when the CPU is accessing the bus in the other cycles, and all one is transferred to the T-BUS controlled by the signal ITRQ (H).

ALB TO BIB INTERCONNECTION	sign/date GB/780524	page
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5.

SIGNAL LISTS

ALB TO BIB INTERCONNECTIONS SIGNAL LIST	sign/date GB/780524	page 1/5
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PLUG TYPE :

CABEL TYPE: 16 WIRES FLAT CABLE

P/N

LENGTH :

REFERENCE DESIGNATION	ALB P1 (C3)
	BIB J1 (C1)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE:ALB
1	T-BUS 11	I/O
2	T-BUS 10	I/O
3	T-BUS 9	I/O
4	T-BUS 8	I/O
5	I CPU INT (H)	I
6	ENSH (L)	I
7	EN ALS OUT (L)	I
8	GND	
9	T-BUS 12	I/O
10	T-BUS 13	I/O
11	T-BUS 14	I/O
12	T-BUS 15	I/O
13	T-BUS 3	I/O
14	T-BUS 2	I/O
15	T-BUS 1	I/O
16	T-BUS 0	I/O

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ALB TO BIB INTERCONNECTIONS SIGNAL LIST	sign/date GB/0524	page 2/5
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PLUG TYPE :	P/N
CABEL TYPE: 16 WIRES FLAT CABLE	
LENGTH :	

REFERENCE DESIGNATION	ALB P2 (C5)
	BIB J2 (C3)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE : ALB
1	T-BUS 7	I/O
2	T-BUS 6	I/O
3	T-BUS 5	I/O
4	T-BUS 4	I/O
5	CPALS	I
6	$\overline{\text{CPALS}}$	I
7	CPMCU	I
8	GND	
9	GND	
10	PER0 (L)	I
11	PER0 (H)	I
12	PER2 (H)	I
13	GND	
14	LDMCU (L)	I
15	LDMCU (H)	I
16	GND	

ALB TO BIB INTERCONNECTION SIGNAL LIST	sign/date GB/780524	page 3/5
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PLUG TYPE :	P/N
CABEL TYPE: 16 WIRES FLAT CABLE	
LENGTH :	

REFERENCE DESIGNATION	·ALB P3 (D1)
	BIB J3 (D1)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE: ALB
1	GND	
2	FORCE CPU INT (H)	0
3	II/OI (H)	I
4	ITI (H)	I
5	$\overline{\text{P0}}$	I
6	$\overline{\text{P1}}$	I
7	ITRQ (H)	I
8	GND	
9	GND	
10	$\overline{\text{CPMCU}}$	I
11	DCL (L)	I
12	PARITY ERROR	0
13	$\overline{\text{8MHz}}$	I
14	$\overline{\text{8MHz}}$	I
15	$\overline{\text{2MHz}}$	I
16	GND	

ALB TO BIB INTERCONNECTION SIGNAL LIST	sign/date GB/780524	page 4/5
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PLUG TYPE :	P/N
CABEL TYPE: 16 WIRES FLAT CABLE	
LENGTH :	

REFERENCE DESIGNATION	ALB	P4	(D3)
	BIB	J4	(D3)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE: ALB
1	AA1	0
2	OP2	0
3	OP0	0
4	AA2	0
5	AA0	0
6	OP1	0
7	DPER0 (H)	I
8	GND	
9	DPER1 (H)	I
10	LD-DREG (H)	0
11	RLP	I
12	RUP	I
13	IUP	0
14	ILP	0
15	SEA17	0
16	SEA16	0

ALB TO BIB INTERCONNECTION
SIGNAL LIST

ALB TO BIB INTERCONNECTION SIGNAL LIST	sign/date GB/780524	page 5/5
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PLUG TYPE :

CABEL TYPE: 16 WIRES FLAT CABLE

P/N

LENGTH :

REFERENCE DESIGNATION	ALB P5 (J7)
	BIB J5 (G1)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE: ALB
1	TO (L)	I
2	POWER DET MP	I
3	POWER DET AL	0
4	PRESET TIMING (L)	I
5	$\overline{\text{ADDO}}$	0
6	I/O (L)	0
7	BUSTRF (H)	I
8	GND	
9	I R/W	I
10	MDAT 16	0
11	MDAT 17	0
12	MDAT 18	0
13	MDAT 19	0
14	MDAT 20	0
15	IA 19	0
16	IA 18	0

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6.

PROM TABLES

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BUS INTERFACE BOARD BIB MB PROM TABLES	GB/780524	
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There is one PROM in the CPU CR8001/2 BIB, the function description cover also the CPU CR8001/3 and therefore many of the bus control function specified in the table are identical.

CPU CR8001/2
BUS TRF CONTROL PROM

CR 1290-1

sign/date GB/770305 | page
repl | project

ADDR.		INPUT						OUTPUT								DESCRIPTION
DEC.	OCT.	MDAT 20 E 4	MDAT 19 D 3	MDAT 18 C 2	MDAT 17 B 1	MDAT 16 A 0		SEMAFOR S/CL (H/L) 8	BUSTRF (H) 7	6	5	4	INCAR (H) 3	LDAR (H) 2	I R/W 1	
0	00	0	0	0	0	0		0	0				0	0		BCNOP
1	01	0	0	0	0	1		0	1				0	1	0	FNI
2	02	0	0	0	1	0		0	0				0	0		INS 1
3	03	0	0	0	1	1		0	0				0	0		TD 1
4	04	0	0	1	0	0		0	1				1	0	1	INC OUT
5	05	0	0	1	0	1		0	1				0	1	0	AR-SF-TD 1
6	06	0	0	1	1	0		0	0				0	0		TD 2
7	07	0	0	1	1	1		0	1				0	1	0	INS 1-FI
8	10	0	1	0	0	0		0	0				0	1		LAR
9	11	0	1	0	0	1		0	0				0	0		ALS-TD 1
10	12	0	1	0	1	0		0	1				0	1	0	FI
11	13	0	1	0	1	1		0	1				0	0	0	MAR-TD 1
12	14	0	1	1	0	0		0	1				0	0	1	ALS-DR-MAR
13	15	0	1	1	0	1		0	0				0	0		TI 1-S8-TD 1
14	16	0	1	1	1	0		0	0				0	0		TI 1-S4-TD 1
15	17	0	1	1	1	1		0	1				0	1	0	TD 1-FI
16	20	1	0	0	0	0		0	0				0	0		TD 1-SW-TD 2
17	21	1	0	0	0	1		0	1				0	0	1	TD 1-SW-MAR
18	22	1	0	0	1	0		0	1				1	0	0	INC IN
19	23	1	0	0	1	1		0	1				0	1	1	DR-MALS
20	24	1	0	1	0	0		0	0				0	0		ALS-TD 2
21	25	1	0	1	0	1		1	1				0	1	0	SEM-FET
22	26	1	0	1	1	0		1	1				0	0	1	SEM-STO
23	27	1	0	1	1	1		0	1				0	1	0	MALS-TD 1
24	30	1	1	0	0	0		0	1				0	0	1	TD 2-SP-ALS
25	31	1	1	0	0	1		0	1				0	1	0	TD 1-SF-ALS
26	32	1	1	0	1	0		0	0				0	0		BCNOP
27	33	1	1	0	1	1		0	0				0	0		BCNOP
28	34	1	1	1	0	0		0	0				0	0		BCNOP
29	35	1	1	1	0	1		0	0				0	0		BCNOP
30	36	1	1	1	1	0		0	0				0	0		BCNOP
31	37	1	1	1	1	1		0	0				0	0		BCNOP
		4	3	2	1	0		8	7	6	5	4	3	2	1	

1. INTRODUCTION

The Bus Interface Board is the interface for CPU CR8001/3 to the CR80 Main Bus and Sub Bus. The BIB is a standard CR80 PCB equipped with a 86 pins edge connector for the Main Bus and a 48 pins connector for the Sub Bus and the system control connection. The connection to the two other boards in the CPU are carried out by means of 16 wires flat cables for the signals and two discreet soldered wires for the power to the ALB & MPB.

2. GENERAL DESCRIPTION

The BIB interface the ALB & MPB to the CR80 Main Bus and Sub Bus. The board contain the circuits necessary for supplying of the synchronization signal to the two other boards, these timing signals are derived from the Main Bus master timing Ø4. The handshaking procedure with the MBC, for the Main Bus authority control and for the Main- & Sub Bus transfer is handled by the board. Address register/counter and data register is included, and temporary storages for the data and addresses transferred to the CR80 busses. The interfaces beside the synchronization signals from the BIB, is the internal CPU bus T-BUS for data/address communication and five output from the MPB µprogram for set up of the bus circuit.

3. SPECIFICATIONS

The BIB constitute the interface between the CPU's CR8001/3.
ALB & MPB and the Main Bus and Sub Bus and System Control Connections.

3.1 Main Bus Connection

The Main Bus connection is a CR80 standard 86 poles edge connector with the pin configuration and signal specification as described in table 3.1 a & b.

3.2 System Control Connection & SuB Bus

The connector used for system control and Sub Bus is a standard CR80 48 pins connector mounted above the 86 poles edge connector. The pin configuration and signal specification is described in table 3.2 a, b & c.

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3.3 Power Interface

Input power +5V is from the Main Bus connector
Power to MPB & ALB is supplied through two discreet wires soldered on the board

Power consumption:
+5V : ± A

3.4 Mechanical Dimenstions

Standard CR80 PCB 183.4 x 305 mm with two connectors one 86 pins Main Bus edge connector & one 48 pins Sub Bus connector.

Height of component side : 8 mm
Height of soldering side : 3 mm.

3.5 Data Transfer Rates

Main Bus:
Max. transfer rate: 2.7 M Word
Min. bus time: 250 ns

Sub Bus:
Max. transfer rate: 2.7 M Word
Min. bus time: 375 ns

3.6 Addressing

20 bits address including two modes bit for:
I/O, L Byte, U Byte & Word
Memory addressing og 256 K Word or 512 K Byte.

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3.7 Data Word

16 bits word plus parity for each byte : LB & UB. ODD parity.

3.8 Internal Connections

The BIB is connected to the ALB with five pcs. 16 wires flat cables ref. signal lists section 5.

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Table 3.1 a

- MAIN BUS CONNECTOR - PIN LAYOUT

2 x 43 pin edge connector rear view

	A		B	
	gnd	1	gnd	
DATA (DA)	0	2	1	DATA (DA)
	2	3	3	
	4	4	5	
	6	5	7	
	8	6	9	
	10	7	11	
	12	8	13	
	14	9	15	
	gnd	10	gnd	
	Auxiliary power	11	auxiliary power (same as All)	
	-12V	12	-12V	
	gnd	13	gnd	
	+12V	14	+12V	
	gnd	15	gnd	
ASSRESS (AD)	0	16	1	ADDRESS (AD)
	2	17	3	
	4	18	5	
	6	19	7	
	gnd	20	gnd	
	8	21	9	
	10	22	11	
	12	23	13	
	14	24	15	
	16	25	17	
	18	26	19	
	gnd	27	gnd	
UP	16	28	17	LP
	AUX	29	MC(H)	
	RS(L)	30	gnd	
	TRQ(L)	31	gnd	
	INA(H)	32	gnd	
	INR(L)	33	gnd	
	R/W(L/H)	34	gnd	
	Ø 1	35	gnd	
	Ø 2	36	gnd	
	Ø 3	37	gnd	
	Ø 4	38	gnd	
	gnd	39	gnd	
	+5V	40	+5V	
	+5V	41	+5V	
	gnd	42	gnd	
	gnd	43	gnd	

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Table 3.1 b

MAIN BUS ELECTRICAL INTERFACE SPECIFICATION POWER LINES

Aux. power	pin A11, B11
$-12\text{V}\ ^{+\,0.2\text{V}}_{-\ \ 0\text{V}}$	pin A12, B12
Gnd	pin A13, B13
$+12\text{V}\ ^{+\,0.2\text{V}}_{-\ \ 0\text{V}}$	pin A14, B14
$+5\text{V}\ ^{+\,0.2\text{V}}_{-\ \ 0\text{V}}$	pin A40, A41, B40, B41
Gnd	pin A42, A43, B42, B43

The power lines are not feed through the Main Bus Extension and therefore different power supplies are used for the different Mother Boards.

The max. currents supplied through one connector are as specified below:

+12V, -12V,	I max:	2 A
+ 5V ,	I max:	12 A

SIGNAL LINES

The levels for all the Main Bus signals are normal TTL logic levels. i.e.:

High level: $2.0\text{V} \leq V_H \leq 5.0\text{V}$
Low level : $0\text{V} \leq V_L \leq 0.8\text{V}$

The load on the different signal lines for one module are as specified on the next page, (all currents are numerical values).

Table 3.1 b

DATA LINES & ADDRESS LINES

DA0 - DA15, UP & LP, AD0 - AD19 & R/W (L/H).

3 - state signals with the followings requirements:

Drivers:		$I_{0H} \geq 5.2$ mA
		$I_{0L} \geq 16.0$ mA
		$I_{0\ off} \leq 100$ uA
Receivers:		$I_{IH} \leq 100$ uA
		$I_{IL} \leq 0.5$ mA
	(1)	$I_{IL} \leq 2$ mA

Note 1: This low level input current is only allowed when the module is addressed.

MASTER CLEAR

MC(H):
Open collector with the following requirements.

Driver:		$I_{0L} \geq 60$ mA
		$I_{0H} \leq 250$ uA
Receiver Schmitt Trigger:		$I_{IH} \leq 100$ uA
		$I_{IL} \leq 0.5$ mA
	(1)	$I_{IL} \leq 2$ mA

Note 1: I_{IL} 2 mA is only allowed for the Main Bus Controller & Main Bus Termination.

TRANSFER REQUEST

TRQ (L):

Open collector or 3 - state signal with the following

Table 3.1 b (cont.)

requirements:

Driver:		I_{OL}	$\geq$ 80	mA
		I_{OH}	$\leq$ 250	uA
Receiver Schmitt Trigger:		I_{IH}	$\leq$ 100	uA
		I_{IL}	$\leq$ 0.5	mA
	(1)	I_{IL}	$\leq$ 2	mA

Note 1: I_{IL} 2 mA is only allowed for the Main Bus Controller & RAM modules with a memory area of 8K word or more.

CLOCK SIGNALS

Ø4 - Ø1:

Driver:	I_{OL}	$\geq$ 120	mA
	I_{OH}	$\geq$ 80	mA
Receiver Schmitt Trigger:	I_{IL}	$\leq$ 2	mA
	I_{IH}	$\leq$ 100	uA

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TABLE 3.2 a

CR80 SUB BUS

48 Pin Connector Pin Assignment

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Pin no.	Signal Description	Pin no.	Signal Description	Pin no.	Signal Description
1a	BG (L)	1b	GND	1c	BRQ(L)
2a	SB2	2b	SB1	2c	SB0
3a	SB5	3b	SB4	3c	SB3
4a	SB8	4b	SB7	4c	SB6
5a	SB11	5b	SB10	5c	SB9
6a	SB14	6b	SB13	6c	SB12
7a	SB17	7b	SB16	7c	SB15
8a	SB20	8b	SB19	8c	SB18
9a	SB23	9b	SB22	9c	SB21
10a	GND	10b	GND	10c	CC(H)
11a	LBG(L)	11b	PO	11c	INT(L)
12a	CPI(L)	12b	TI(L)	12c	P1
13a	SRQ2	13b	FRS(L)	13c	MRS(L)
14a	DTR(L)	14b	FEN(L)	14c	SRQ1
15a	ATR(L)	15b	GND	15c	GND
16a		16b		16c	

Table 3.2 b

SUB BUS ELECTRICAL INTERFACE SPECIFICATIONS

The levels for all the Sub Bus signals are normal TTL logic levels i.e. :

High level: $2.0V < V_H < 5.0V$
Low level: $0 \;\; V < V_L < 0.8V$

The specifications below are for the numerical current values allowed for one module connected to the Sub Bus:

ADDRESS & DATA LINES

SB0 - SB23

3 - state signals with the following requirements:

Drivers:	I_{0H}	$\geq$ 5.2mA
	I_{0L}	$\geq$ 16.0mA
	$I_{0\ off}$	$\leq$ 100 uA
Receivers:	I_{IH}	$\leq$ 100 uA
	I_{IL}	$\leq$ 0.5mA
	(1) I_{IL}	$\leq$ 2.0mA

Note: This low level input current is only allowed when the module is addressed or if it is an address sourcing module i.e. CPU or DMA.

Table 3.2 b (cont.)

TRANSFER CONTROL SIGNALS

ATR(L), DTR(L), MRS(L), FEN(L), FRS(L).

Open collector or 3 - state enabled when active signals with the following requirements:

Drivers: $I_{0L} \geq 40$ mA
$I_{0H} \leq 100$ uA

Receivers:
Schmitt Trigger: $I_{IH} \leq 100$ uA
$I_{IL} \leq 2.0$mA

SUB BUS AUTHORITY SIGNALS

SRQ 1(L) & SRQ 2(L)

Open collector - or 3 - state enabled when active, signals with the following requirements:

Drivers: $I_{0L} \geq 40$ mA
$I_{0H} \leq 100$ uA

Receivers:
Schmitt Trigger: $I_{IH} \leq 100$ uA
$I_{IL} \leq 4.0$mA

AUXILIARY SIGNALS

The three auxiliary signals Aux 1 - Aux 3 is available for special use in the system and therefore not specified in this document.

Table 3.2 c (cont.)

SUB BUS INTERFACE FUNCTIONAL DISCRIPTION

The following paragraphs describes the interface from a functional point of view. Furthermore the timing specification for the signals are included in the timing diagrams.

The communication on the Sub Bus is devided in two phases; the address - and the data phase. When data is communicated between a memory module and a DMA/CPU the address is transferred to the memory in the address phase and the data to/from the memory in the data phase. If the communication is between a func module and a CPU module only the data phase is used.
Control of the Sub Bus lines SB0 - SB23 is carried out by the signals ATR(L) (address phase) and DTR(L) or FEN(L) (data phase).

Table 3.2 c

SYSTEM CONTROL CONNECTIONS ELECTRICAL INTERFACE SPECIFICATION

The levels for all the System Control Connections are normal TTL logic levels i.e.

High level: $2.0V < V_H < 5.0V$
Low level: $0\ V < V_L < 0.8V$

The specifications below are for the numerical current values for one module connected with the signals.

Main Bus Authority Control Signals

BRQ (L), BG (L)

Driver: $I_{OL} \geq 48mA$

Receiver: $I_{IH} \leq 100uA$

$I_{IL} \leq 2mA$

LBG (L)

Open collector signal:

Driver: $I_{OL} \geq 48mA$

$I_{OH} \leq 100uA$

Reciever: $I_{IH} \leq 100uA$

$I_{IL} \leq 2mA$

Table 3.1c (cont.)

CPU Clear

CC (H)
Open collector signal:

Driver:	$I_{OL} \geq$ 60mA
	$I_{OH} \leq$ 100uA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 2mA

I/O Interrupt Signals & Timer Interrupt

INT (L), P0, P1, TI (L)

Driver:	$I_{OL} \geq$ 60mA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 2mA

CPU Interrupt

CPI (L)
Open collector signal:

Driver:	$I_{OL} \geq$ 60mA
	$I_{OH} \leq$ 100uA
Receiver	$I_{IH} \leq$ 100uA
Schmitt Trigger:	$I_{IL} \leq$ 2mA

4. FUNCTIONAL DESCRIPTION

The address, calculated during instruction execution in the CPU CR8001/3, can be transferred directly via the internal T-BUS, as the address parts for the Sub Bus transfer, when the address is pressed on the T-BUS it is loaded into the address register/counter, so that it can be used for Main Bus addressing, if the addressed memory isn't located on the Sub Bus. If the Sub Bus addressing gives a response, the cycle will be continued with the transfer of data to the CPU or from the CPU. The CPU include a counter which calculate the length of the data phase, so that a time out will be initiated internal in the module if the data phase is more than 4 us.
The special CR80 func modules can be controlled by these BIB. The func address and control "6 bits" can be sourced either direct from the µprogram or from the standard CR80 instruction set. If there in the special func module memory transfer isn't a memory respons from the Sub Bus the BIB will automatical access the memory on the Main Bus, and control the data transfer from/to func without involving the CPU's internal registers except the data register located on the BIB. When accessing consecutive memory addresses the address register can be incremented instead of making the address calculation in the ALB, and then use the address for the Sub Bus & Main Bus. The BIB can control the system control signal LBG (L) and thereby access the memory times without interruption (semaphore). The semaphore transfer will as the I/O transfer not access the Sub Bus but only the Main Bus.

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The address field consist of 16 bits corresponding to the T-BUS plus 2 page bits and 2 mode bits used for Word/L Byte/U Byte/I/O, the later four bits comes from ALB and are loaden into corresponding register in the BIB each µ cycle, while the 16 bits field is controlled directly by the µprogram.

The data communicated on the T-BUS from/to the BIB consist of 16 bits + 2 parity bits (ODD).
Data to be transferred from the CPU is always loaded into the BIB data register before transmission, data to the CPU is transferred from the CR80 Main- & Sub Bus to the T-BUS and dependent of the µ instruction to the address register too.

The BIB is divided in the following functionals blocks ref. block diagram:

1.	Data- and Address Register	F-DAR-1
2.	Sub Bus Drivers	F-SBD-1
3.	Main Bus Drivers	F-MBD-1
4.	Sub Bus Transfer Control	F-SBTC-1
5.	Timing Control	F-TC-1
6.	Main Bus Transfer Control	F-MBTC-1

4.1 Data and Address Register F-DAR-1

The storages for the bus data and bus addresses are contained in these functional block.
Input to registers is the T-BUS, parity bits and 6 OP reg. & Address bits for the func modules.
Outputs from the registers are to the Main Bus and Sub Bus drivers. Control of the load and for the 16 LSB of the address register, count pulses is carried out by bus control PROM CR1289 located in the Sub Bus Transfer Control Circuit.

F-DAR-1 consist of two logical blocks:

1. Data Register L-DR-1
2. Address Register L-AR-1

4.1.1 Data Register L-DR-1

Input to the data part of the data register (latch data and the two parity bits) is the T-BUS.
The loading of the latch is controlled by the signal LDDREC (H) coming from the ALB (T-File Control).
Inputs to the remaining part of the L-DR-1 are OP0-OP2 & AA0-AA2 from the ALB corresponding to func address & func control. The func register is updated each u cycle DPER1(H) indipendent of the µ program output, which the data part load is controlled by the bus control wires via the T-File control meaning that it can be updated in each of the T-BUS's 3 cycles.
The timing diagram fig. 4.1.1 specify the sequences in more detailes.

4.1.2 Address Register L-AR-1

The lower 16 bits of the address field (20 bits) is always loaded into the counter part of the address register in the T-BUS ALS time when set up by the bus control function. Incrementation of the 16 bits is also executed in the ALS out time.
The remaining part of the address register, the 5 bits for pages, mode & read write, addressing is updated in synchronous with the CPU cycles independent of the bus control function (MDAT 16-20)
Timing diagram fig. 4.1.2 shows in detail the sequences for operation of the L-AR-1.
Note that the address register can not be used as source for the Sub Bus address in the same cycle as it is loaded, it is only the T-BUS directly.

Data Register Timing Diagram

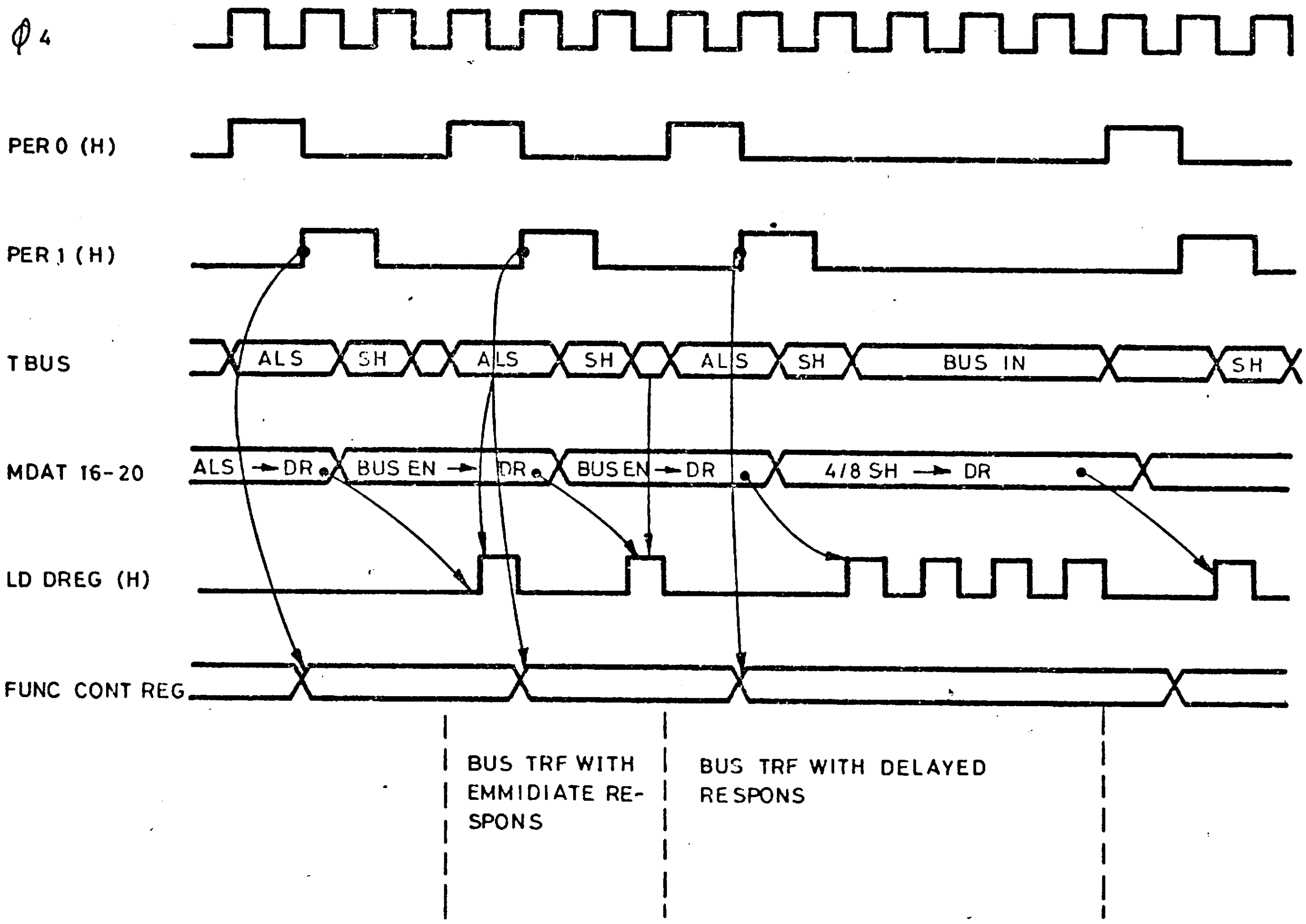
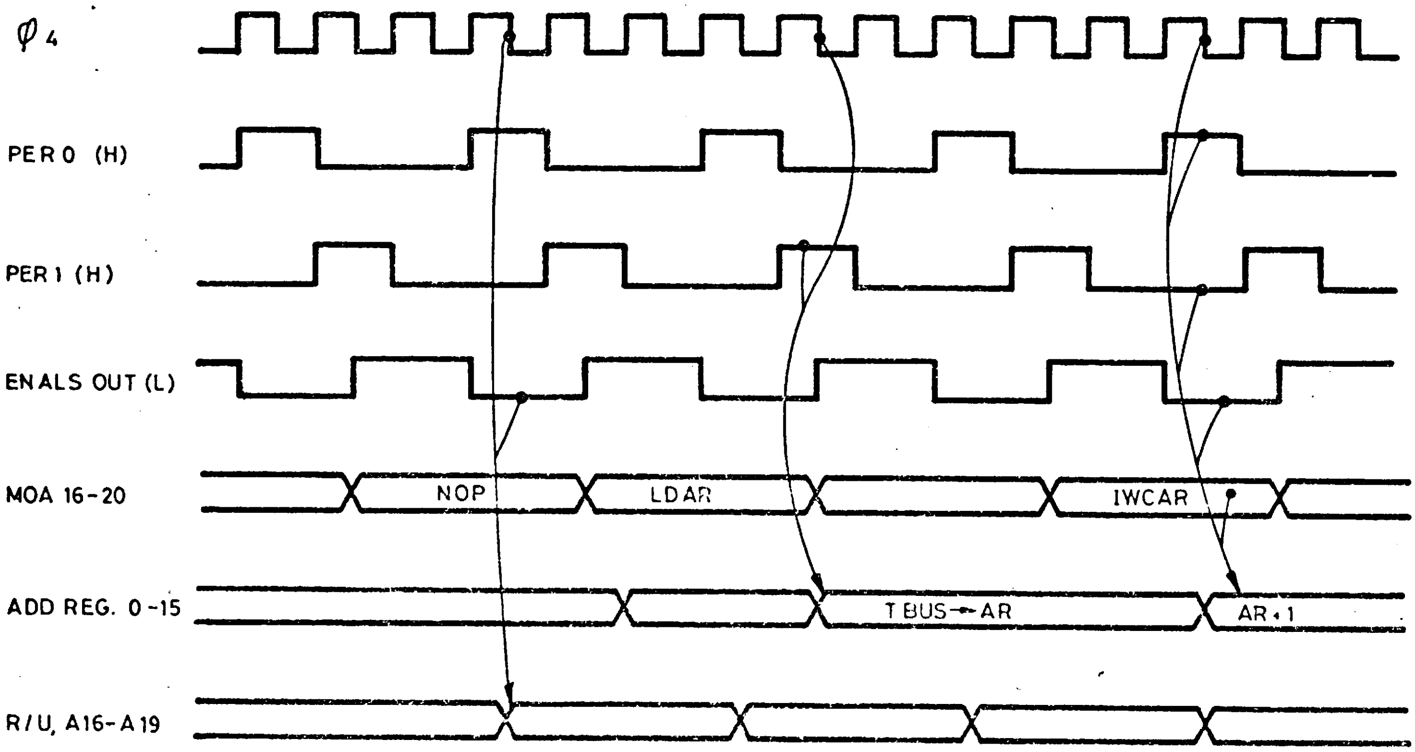


Fig. 4.1.1

Address Register Timing Diagram



R/U, A16-A19 UPDATED REGARDLESS OF BUSFUNKTION

Fig. 4.1.2

4.2 Sub Bus Drivers F-SBD-1

The driver circuits for the Sub Bus lines SB0-23 are located in these functional block.
There are three sets of drivers; one for the data phase and two for the address phase. The address drivers are used for transferring the T-BUS contents direct to the Sub Bus or for transferring the address register contents as address to the Sub Bus.
F-SBD-1 is divided in three logical blocks:

1.	Sub Bus Data Driver	
2.	Address Sub Bus Driver	L-ASBD-1
3.	T-BUS Sub Bus Driver	L-TSBD-1

For the Sub Bus address and data phase ref. table 4.2.

4.2.1 Sub Bus Data Driver L-SBDD-1

The data driver consist of two parts, one part is used as driver for the data register and one for the func control and address.
The data part is enabled when data is transferred from (ENSBDAT(L)) IDTR (L) the CPU to the Sub Bus which the other part always is enabled during the Sub Bus data phase IDTR (L) regardless of the transfer direction, because these signals are used as func module control.

4.2.2 Address Sub Bus Driver L-ASBD-1

L-ASBD-1 control the Sub Bus during the address phase, when the address source is the address register/counter. The 16 LSB is from the register/ counter which the R/W, mode & page bits are sourced from the corresponding register in the address register block L-AR-1. The signal EN AR from Sub Bus Transfer Control F-SBTC-1 is used as output enable.

4.2.3 T-BUS Sub Bus Driver L-TSBD-1

When the address source for the Sub Bus is the T-BUS (ALS out) this driver block is used.
The inputs are T-BUS 0-15 for the 16 LSB and the five bits: R/W, mode and page are the input signal to the corresponding register in the address register block L-AR-1. The outputs are enabled by the signal EN T-BUS from Sub Bus Transfer Control F-SBTC-1.

TABLE 4.2

PIN NO.	SIGNAL NAME	FUNCTION		
		ADDRESS PHASE	DATA PHASE	
c2	SB 0	Add. 0 (LSB)	DAT 0	(LSB)
b2	SB 1	Add. 1	DAT 1	
a2	SB 2	Add. 2	DAT 2	
c3	SB 4	Add. 3	DAT 3	LB
b3	SB 4	Add. 4	DAT 4	
a3	SB 5	Add. 5	DAT 5	
c4	SB 6	Add. 6	DAT 6	
b4	SB 7	Add. 7	DAT 7	
a4	SB 8	Add. 8	DAT 8	
c5	SB 9	Add. 9	DAT 9	
b5	SB 10	Add. 10	DAT 10	
a5	SB 11	Add. 11	DAT 11	UP
c6	SB 12	NV	DAT 12	
b6	SB 13	NV	DAT 13	
a6	SB 14	NV	DAT 14	
c7	SB 15	Add. 18	DAT 15	
b7	SB 16	Add. 19	LP	
a7	SB 17	R/W (L/H)	UP	
c8	SB 18	Add. 12	FAdd. 0	
b8	SB 19	Add. 13	FAdd. 1	
a8	SB 20	Add. 14	FAdd. 2	
c9	SB 21	Add. 15	FCont. 0	
b9	SB 22	Add. 16	FCont. 1	
a9	SB23	Add. 17	FCont. 2	

4.3 Main Bus Drivers F-MBD-1

The Main Bus data and address interface circuits are located in F-MBD-1.
The address driver is controller by BG(L) from the MBC module while the data driver is controlled by BG(L) and R/W. The input circuit for the T-BUS from the Main Bus and Sub Bus is a part of F-MBD-1.
Main Bus Drivers are divided in three logical blocks:

1.	Address Drivers	L-AD-1
2.	Data Drivers	L-DD-1
3.	T-BUS Drivers	L-TD-1

4.3.1 Address Drivers L-AD-1

L-AD-1 consist of 3-state drivers for interfacing the address register/counter L-AR-1 to the CR80 Main Bus. The outputs from the drivers are enabled by the signal BG(L) one of the system control signals from the MBC module.

4.3.2 Data Drivers L-DD-1

The inverting 3-state driver used for transferring the data register contents to the Main Bus and signals are located in L-DD-1. The outputs are enabled by BG(L) and R/W, so that data only is transferred in a write cycle.

4.3.3 T-BUS Drivers L-TD-1

The interface for transferring of data from the Main Bus and Sub Bus to the internal CPU bus T-BUS, consist of a 3-state selector circuit which is

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enabled synchronous with the CPU's internal cyclus EN BUS IN. The selection of Main or Sub Bus as the source for the T-BUS is controlled from the Main Bus Transfer Control F-MBTC-1 by the signal ITRQ so that the source is the Main Bus when the signal is active.

4.4 Sub Bus Transfer Control F-SBTC-1

Set up of the CPU CR8001/3 for making bus transfer, either on the Sub Bus or the Main Bus is controlled by F-SBTC-1.
The circuit necessary for handling Sub Bus authority and the Sub Bus handshaking procedure is also located in this functional block.

Inputs are beside the timing signals, the five bus control lines from the μ program MDAT 16-20.
The bus control signals are decoded by a 32 x 8 PROM and distributed all over, for controlling the different four bus functions. Two of the PROM outputs are used as mode bits and determined the bus function as CPU↔Mem, CPU↔Func, Mem↔Func or Func↔Mem the different transfer modes, and these relationship to the control signals are defined in timing diagram fig. 4.4 a-g

The Sub Bus Transfer Control is divived in to the following three logical blocks:

1.	Transfer Set up	L-TSU-1
2.	Sub Bus Authority Control	L-SAC-1
3.	Sub Bus Transfer Control	L-STC-1

4.4.1 Transfer Set up L-TSU-1

Set up of the BIB, to make a bus transfer is carried out by decoding of the bus control function MDAT 16-20 by a 32 x 8 PROM CR1289 (ref. section 6 for actual contents).
Four of the outputs are synchronized on the timing signal PERO(H) by a register while the other four are used directly by the other parts of the BIB.

The functional table 4.4.1 define the signals more detailed.

4.4.2 Sub Bus Authority Control L-SAC-1

When the BIB is set up for a bus transfer and the transfer isn't an I/O or semaphore the L-SAC-1 will issue a Sub Bus request SRQ on the rising edge of PERO(H) and when the request is accepted the signal AC(L) will go low on the falling edge of Ø4 meaning that the CPU can start the Sub Bus transfer. If the transfer is an I/O or Semaphore the L-SAC-1 will not be initiated because the transfer has to take place on the Main bus.
Disabling of SRQ can be done from three signals, either when a new cycle start without bus transfer, or when a Main Bus transfer is started. One of the two SRQ signals is driven from the BIB while the other is sensed. Control of SRQ 1&2 is carried out by means of the CPU address $\overline{\text{ADDO}}$ bit.
Timing diagram 4.4.a specify the logical block in more details.

4.4.3 Sub Bus Transfer Control L-STC-1

When a Sub Bus transfer is started by the signal AC(L) from L-SAC1. an internal address transfer will be set up ENTBUS or ENAR, which of the two FF is determined by the signal ENTBUS/AR(H/L) from L-TSU-1. The internal ATR will be issued on the falling edge of Ø4 and taken down on the next falling edge of Ø4. If the transfer is a func↔CPU the signal ATR on the bus will be disabled (DIS ATR) and only the signal FEN will be active in the data phase (IDTR(H)). If the transfer is a memory access both ATR, and if a respons on the ATR is recognized, DTR will be issued. If the bus transfer is a Mem←→Func both FEN and DTR is transferred on the condition of the respons signals MRS or FRS. For more details ref. fig. 4.4. a-g.

The outputs from the block are used for enabling of the Sub Bus drivers.

FUNCTION	NO.	MDAT 20	19	18	17	16	ADDRESS REG.	R/W L/H	FM1, FM2		ADDRESS SOURCE	SEMAFOR
FNI	1	0	0	0	0	1	TBUS → AR	"0"	0	0	T-BUS	CLEAR
INCOUT	4	0	0	1	0	0	AR.1 → AR	1	0	0	AR	CLEAR
ARSFTD1	5	0	0	1	0	1	TBUS → AR	0	0	0	T-BUS	CLEAR
INS1 - FI	7	0	0	1	1	1	TBUS - AR	0	0	0	T-BUS	CLEAR
LAR	8	0	1	0	0	0	TBUS - AR	0	0	0	NO BUS TRF	CLEAR
FI	10	0	1	0	1	0	TBUS - AR	0	0	0	T-BUS	CLEAR
MAR ID1	11	0	1	0	1	1	NO OP	0	0	0	AR	CLEAR
ALS-DR-MAR	12	0	1	1	0	0	NO OP	1	0	0	AR	CLEAR
TD1 FI	15	0	1	1	1	1	TBUS - AR	0	0	0	T-BUS	CLEAR
TD1-SW-MAR	17	1	0	0	0	1	NO OP	1	0	0	AR	CLEAR
INC IN	18	1	0	0	1	0	AR.1 - AR	0	0	0	AR	CLEAR
DR-MALS	19	1	0	0	1	1	TBUS - AR	1	0	0	T-BUS	CLEAR
SEM-FET	21	1	0	1	0	1	TBUS - AR	0	0	0	T-BUS	SET
SEM-SIO	22	1	0	1	1	0	NO OP	1	0	0	AR	SET
MALS-TD1	23	1	0	1	1	1	TBUS - AR	0	0	0	T-BUS	CLEAR
TD2-SP-ALS	24	1	1	0	0	0	NO OP	1	0	0	AR	CLEAR
TD1-SF-ALS	25	1	1	0	0	1	TBUS - AR	0	0	0	T-BUS	CLEAR
FUNC-MAR	26	1	1	0	1	0	AR.1-AR	1	1	1	AR	CLEAR
MAR-FUNC	27	1	1	0	1	1	AR.1-AR	0	0	1	AR	CLEAR
MALS-FUNC	28	1	1	1	0	0	TBUS - AR	0	0	1	T-BUS	CLEAR
ALS-FUNC	29	1	1	1	0	1	NO OP	1	1	0	Ø	CLEAR
FUNC-MALS	30	1	1	1	1	0	TBUS - AR	1	1	1	T-BUS	CLEAR
FUNC-TD1	31	1	1	1	1	1	NO OP	0	1	0	Ø	CLEAR
REMAINING							NO OP	0	0	0	NO BUS TRF	CLEAR

NOTE: (1) IF THERE IS NO RESPONS ON AN ATR THE BIB WILL SWITCH TO THE MAIN BUS AND EXECUTE THE TRANSFER, THE ADDRESS SOURCE FOR MAIN BUS IS THE ADDRESS REGISTER AR

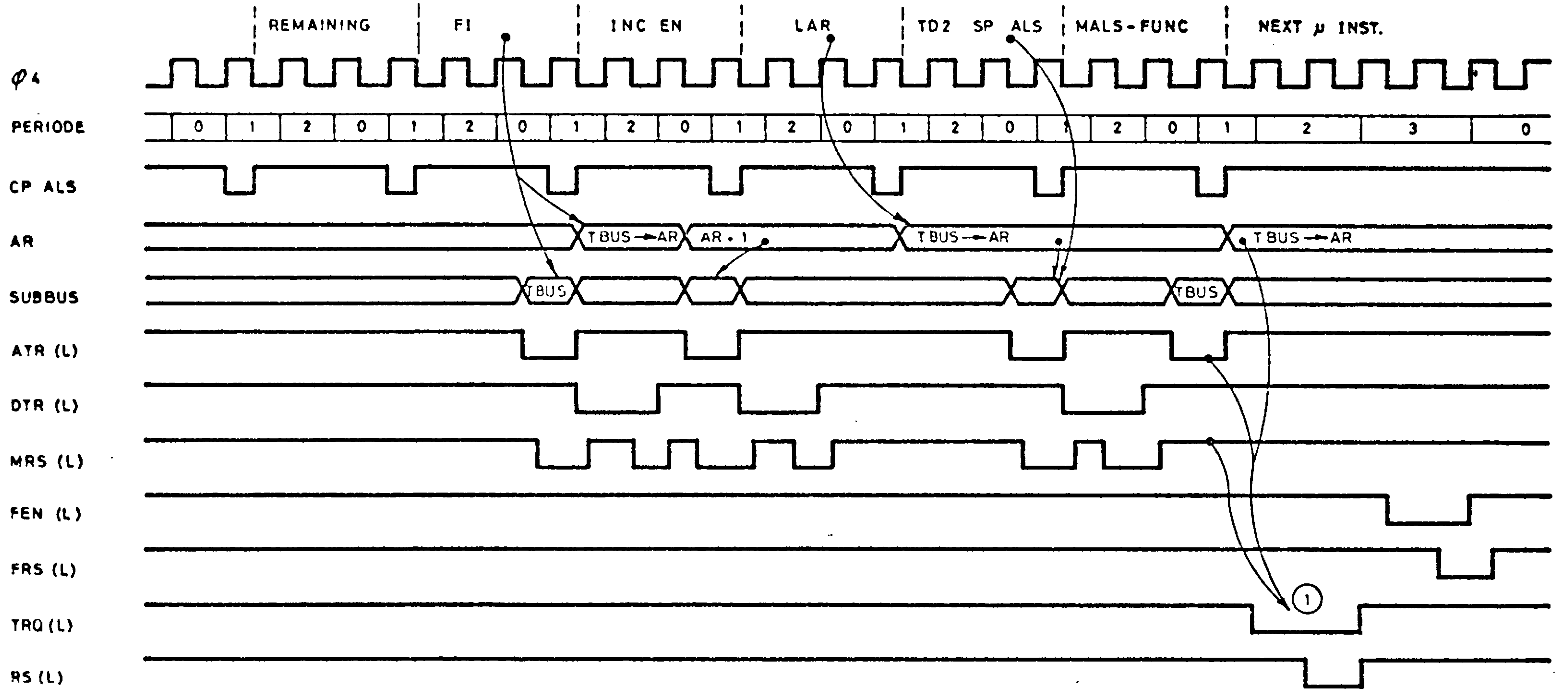

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TABLE 4.4.1

Bus I/F Board

Transfer Set Up

Functional Table

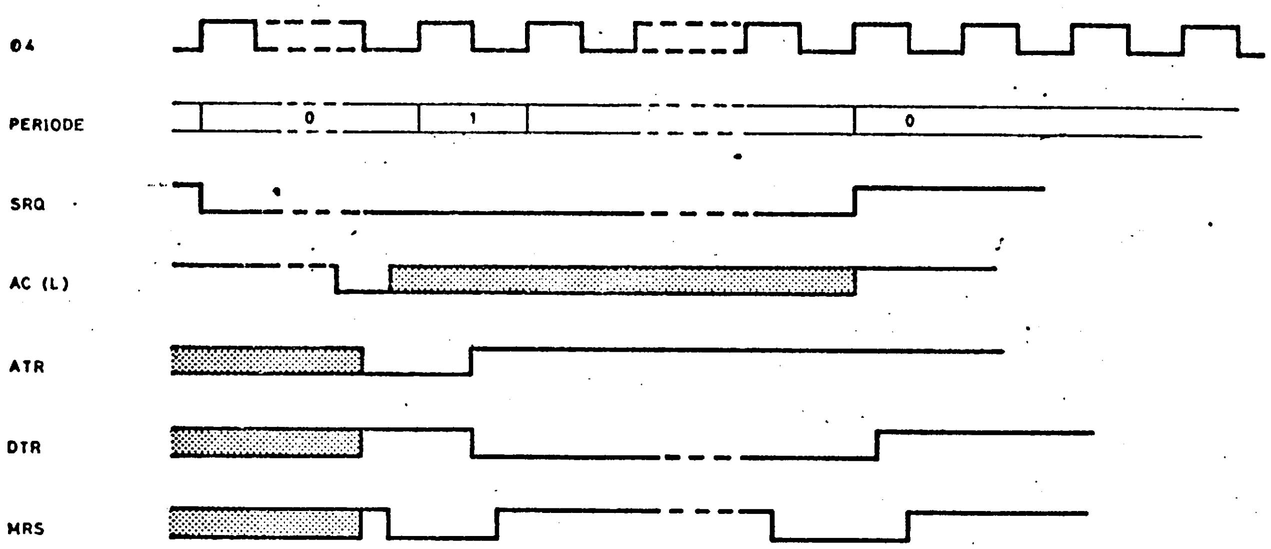
Date	78-06-02	Approved	E
Drawn	GB/IDA		
Parts no		3-1680	
Print no		Sheet 1 of 1 sheets	

Issue	1
Date	78-06-02
Approved	

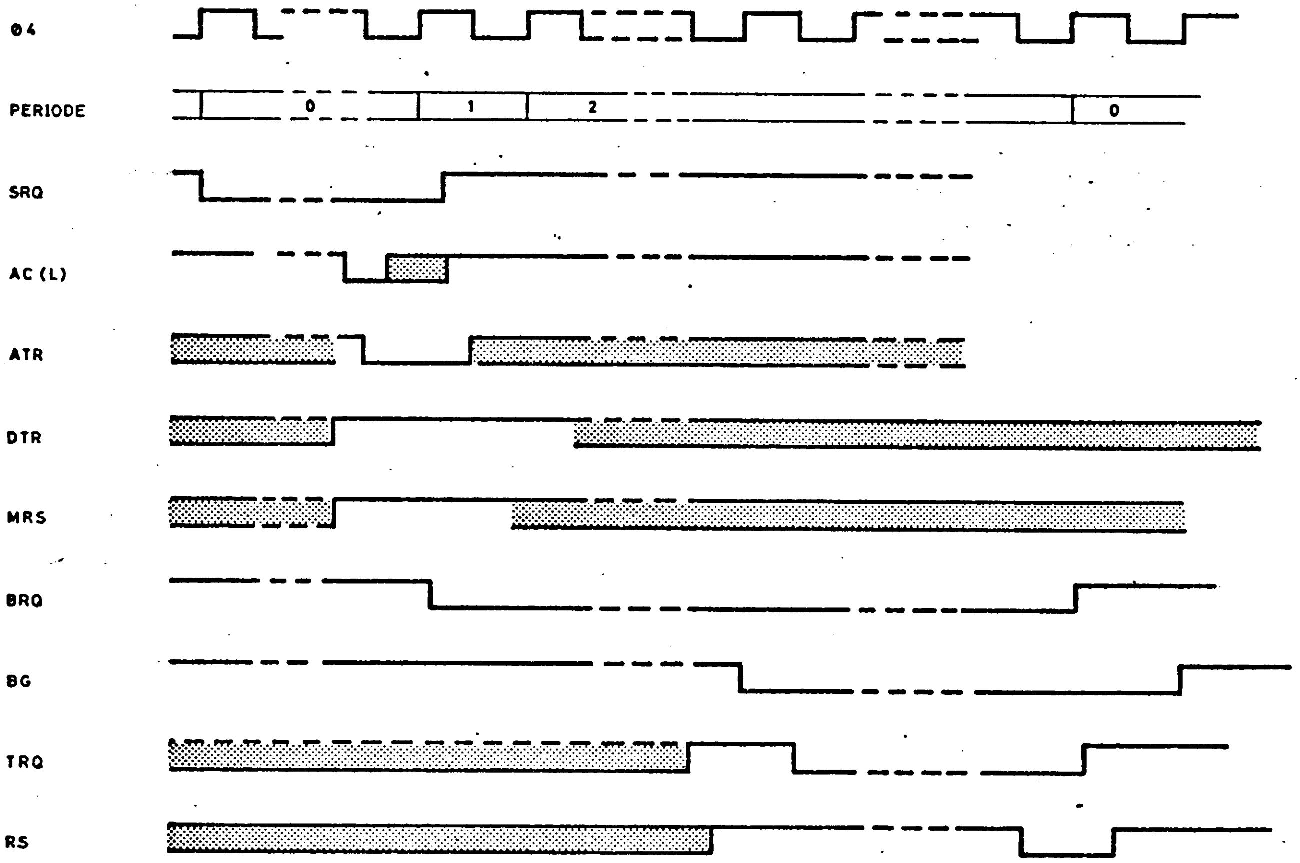
FEs 4.4a

STO FM 1 : 0
STO FM 2 : 0

CPU ↔ MEM (SUB BUS)



CPU ↔ MEM (MAIN BUS)



CHRISTIAN ROVSING A/S

CPU CR 8001/3
Transfer Control Signals

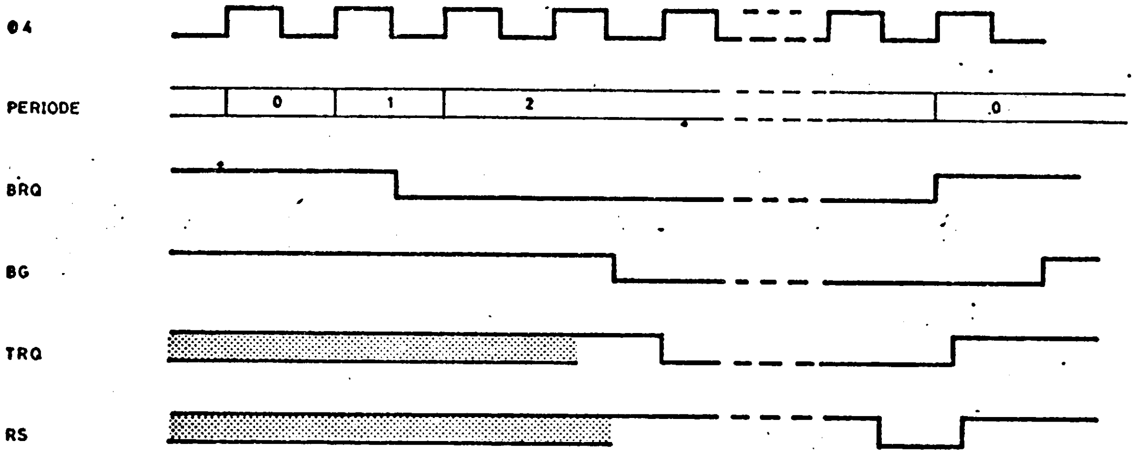
Timing Diagram

Scale		Approved		Issue	1
Date	78-05-19	E		Date	78-05-19
Drawn	GB/AMS			Approved	
Parts no		3-1675			
Print no		Sheet 1 of 7 sheets			

Fa. 4,4 b

<u>CPU → I/O SEMAFOR</u>

STO FM1 : 0
STO FM2 : 0



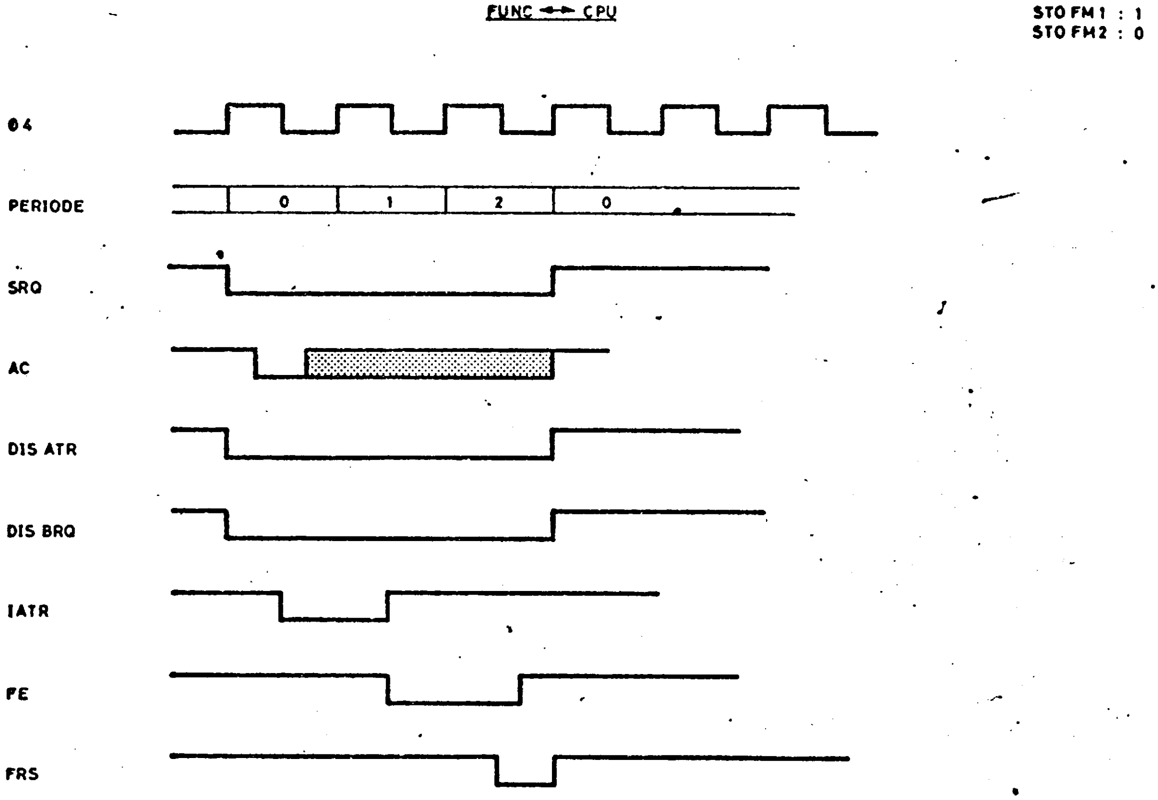
CHRISTIAN ROVSING A/S

CPU CR 8001/3
Transfer Control Signals

Timing Diagram

Scale		Approved	Issue 1
Date	78 - 05 - 19	E	Date 78 - 05 - 19
Drawn	GB/AMS		Approved
Parts no		3-1675	
Print no		Sheet 2 of 7 sheets	

Fig 44.c



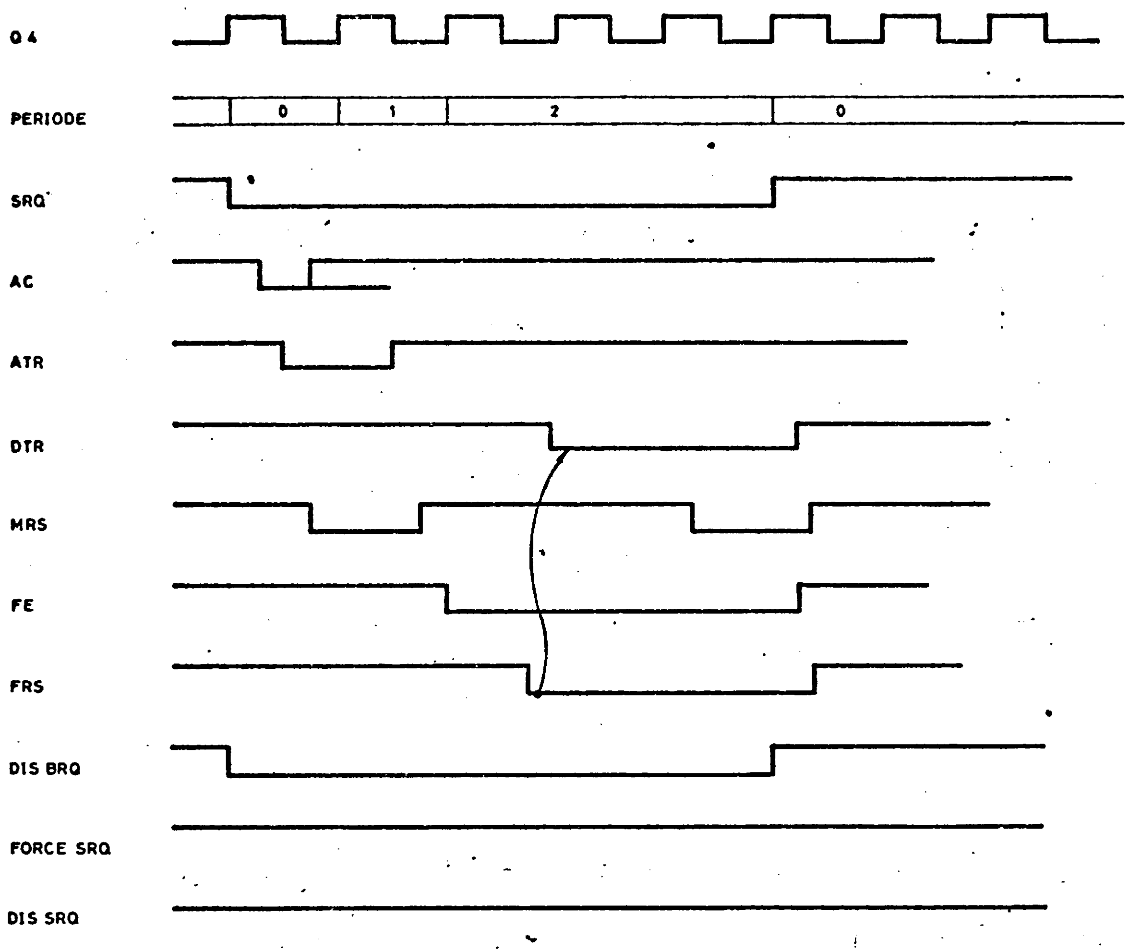
CHRISTIAN ROVSING A/S

CPU CR 8001/3 Transfer Control Signals Timing Diagram	Scale		Approved	Issue	1
	Date	78-05-22	E	Date	78-05-22
	Drawn	GB/AMS		Approved	
	Parts no		3-1675		
	Print no		Sheet 3 of 7 sheets		

Fig 4.4.d

FUNC → MEM (SUB BUS)

STO FM1 : 1
STO FM2 : 1



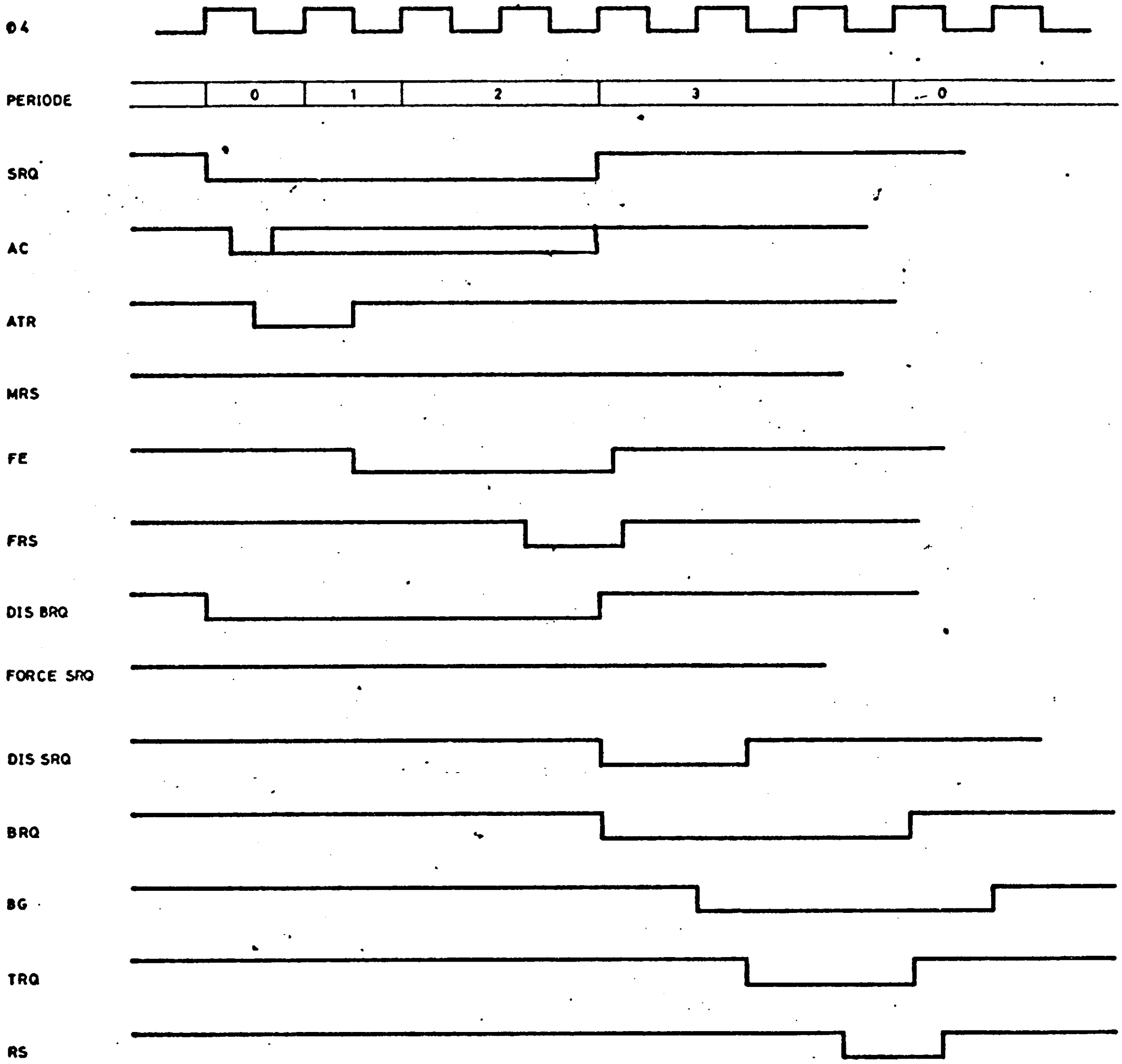
CHRISTIAN ROVSING A/S

CPU CR 8001/3 Transfer Control Signals Timing Diagram	Scale		Approved	Issue	1
	Date.	78-05-22	E	Date	78-05-22
	Drawn	GB/AMS		Approved	
	Parts no		3-1675		
	Print no		Sheet 4 of 7 sheets		

e

FUNC → MEM (MAIN BUS)

STO FM 1 : 0 1
STO FM 2 : 0 1



CHRISTIAN ROVSING A/S

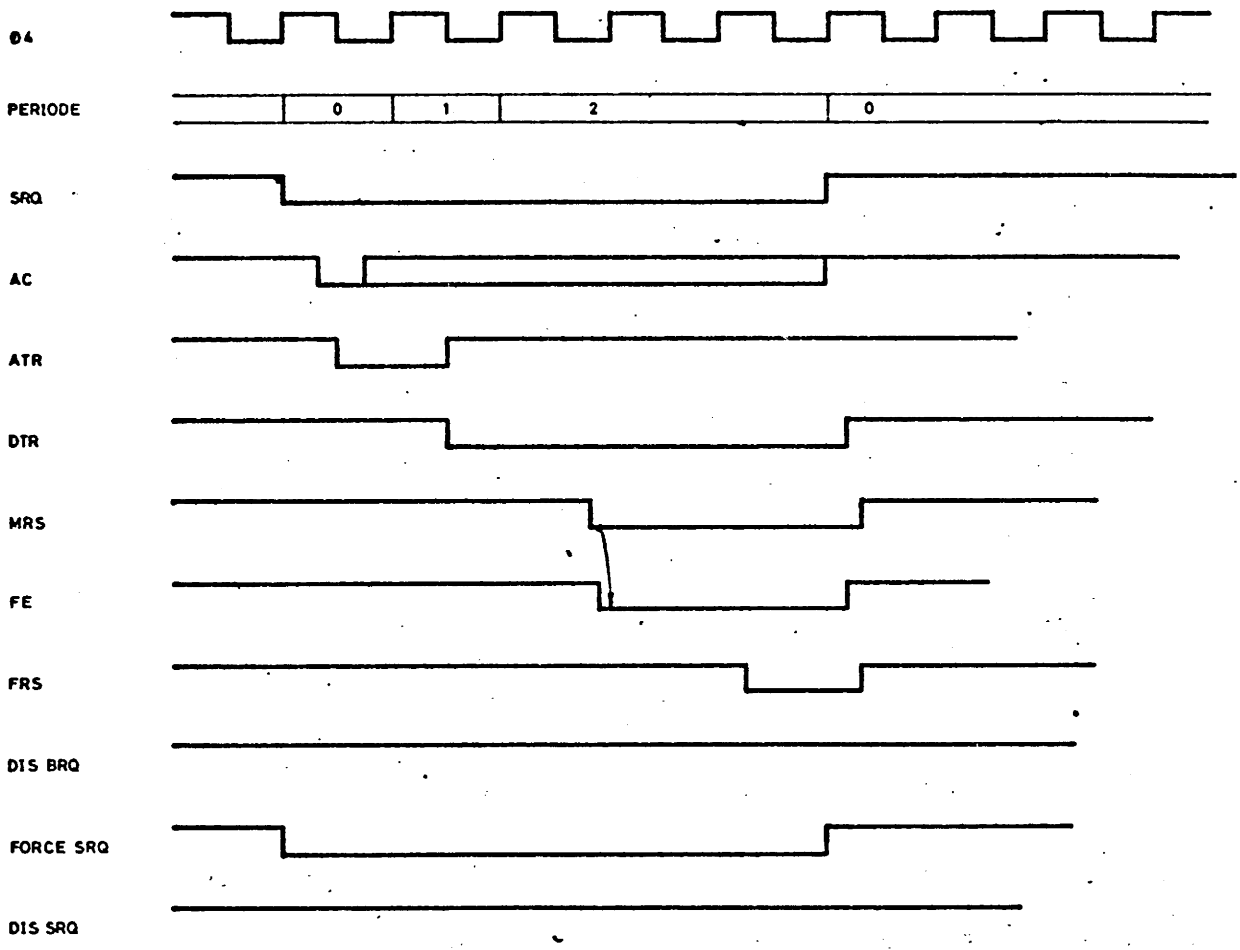
CPU CR 8001/3
Transter Control Signals

Timing Diagram

Scale		Approved	Issue	1
Date	78 - 05 - 22	E	Date	78-05-22
Drawn	BG / AMS		Approved	
Parts no		3-1675		
Print no		Sheet 5 of 7 sheets		

MEM (SUB BUS) → FUNC

STO FM 1 : 0
STO FM 2 : 1

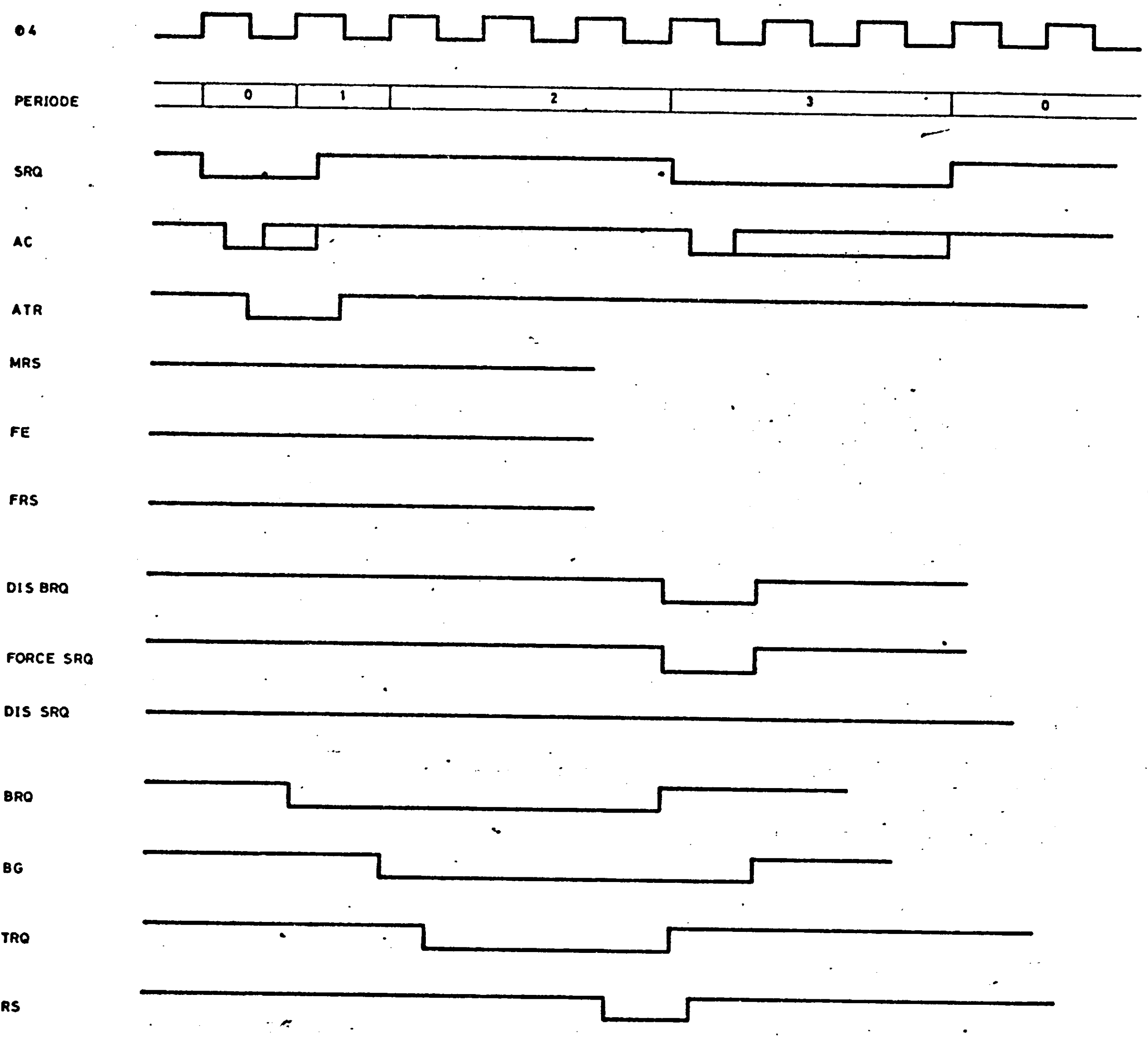


CHRISTIAN ROVSING A/S						
CPU CR 8001/3	Scale		Approved		Issue	1
Tranfer Control Signals	Date	78 - 05 - 22	E		Date	78-05-22
	Drawn	GB / AMS			Approved	
Timing Diagram	Parts no		3-1675			
	Print no		Sheet 6 of 7 sheets			

9

MEM (MAIN BUS) → FUNC

STO FM1 : 0
STO FM2 : 1



CHRISTIAN ROVSING A/S

CPU CR 8001/3
Transfer Control Signals
Timing Diagram

Scale		Approved		Issue	1	
Date	78 - 05 - 22	E		Date	78-05-22	
Drawn				Approved		
Parts no		3-1675				
Print no		Sheet 7 of 7 sheets				

4.5 Timing Control F-TC-1

Generation of the different timing signals, and the T-BUS enable control is carried out by the Timing Control. The input to the block is the master timing signals from the Main Bus, and signals from Sub Bus - and Main Bus transfer control used to select the source, which has to be active before the timing sequence PER0 - PER3 can continue.
There are five logical blocks in the Timing Contol:

1.	Main Bus Receiver	L-MR-1
2.	Clear Control	L-CC-1
3.	Master Timing Control	L-MTC-1
4.	Master Timing	L-MT-1
5.	Enable & Clock Generator	L-E&CG-1

4.5.1 Main Bus Receiver L-MR-1

The receiver for the Main Bus signals Ø4, Ø2 & RS(L) are located in L-MR-1 together with the CPU Clear (CC(H)) receiver. The interface circuit is schmitt triggers.

4.5.2 Clear Control L-CC-1

When the CPU detects a CPU Clear it has to reset all the circuit so the start up is well defined, this procedure is controlled by L-CC-1 which also generate a reset when a time out or parity error is recognized. There exixt two types of time out, one for the Main Bus, which is detected in the Main bus Transfer Control F-MBTC-1, and one for the Sub Bus, which is detected by a counter, so that a time out is generated if the width of IDTR(H) exceed 4 μs.
Timing diagram fig. 4.5.2 specify the Clear Control more detailed.

4.5.3 Master Timing Control L-MTC

The input signal to the Master Timing L-MT-1 comes from a selector circuit which selects the propper signals from the two CR80 busses as the input used to continue the CPU's cycles Per0 - Per3. The selector is controlled from the Master Timing, and from the Sub Bus and Main Bus Transfer Control in accordance with table 4.5.3.

4.5.4 Master Timing L-MT-1

The Master Timing logic generates the timing signals used throughout the whole CPU, PER0, 2 and the signal Per3 which only is used on the BIB for control when the transfer is a Mem. ↔ Func and the memory is located on the Main Bus. The timing diagram fig. 4.5.4 specify the signals.

4.5.5 Enable & Clock Generator L-E&CG-1

Control of the T-BUS enable signals and the MCU & ALS clock is generated in these logical block. Timing diagram fig. 4.5.5 specify the signals.

Table 4.5.3

PER 0 (L)	PER 1 (L)	PER 2 (H)	MRQ (H)	STOFM 1	STOFM 2	IDTR (H)	ITRQ (H)	BUS FUNCTION	"J" INPUT TO PER 3 FF	"J" INPUT TO PER 0 FF		DESCRIPTION
1	1	1	1	0	0	0	1		CPU↔MEM/ I/O MAIN BUS	0	$\overline{RS}$	WAITING FOR RS (L) ON MAIN BUS
1	1	1	1	1	0	1	0		CPU↔FUNC	0	$\overline{FRS}$	WAITING FOR FRS (L) ON SUB BUS
1	1	1	0	0	1	1	0		MEM→FUNC MEM: SUB BUS	0	$\overline{FRS}$	WAITING FOR FRS (L) ON SUB BUS
1	1	1	0	0	0	1	0		CPU↔MEM SUB BUS	0	$\overline{MRS}$	WAITING FOR MRS (L) ON SUB BUS
1	1	1	0	0	0	0	0		NO OP	0	"1"	STO BUS TRF (H) "0" IS SELECTED
1	1	1	1	0	0	0	0		CPU↔MEM/I/O MAIN BUS	0	"0"	STO BUS TRF (H) "1" IS SELECTED MAIN BUS NOT AVAILABLE
1	1	1	1	1	1	0	1		MEM→FUNC MEM: MAIN BUS	$\overline{RS}$	0	WAITING FOR RS (L) ON MAIN BUS
1	1	1	1	1	1	1	0		FUNC→MEM MEM: MAIN BUS	$\overline{FRS}$	0	WAITING FOR FRS (L) ON MAIN BUS
1	1	0	1	1	1	1	1		FUNC→MEM MEM: MAIN BUS	0	RS	WAITING FOR RS (L) ON MAIN BUS
1	1	0	1	0	1	1	0		MEM→FUNC MEM: MAIN BUS	0	FRS	WAITING FOR FRS (L) ON SUB BUS
BIT PATTERN ABOVE					0	0			0	0		WAITING FOR BUS ACCESS
0								ALL	0	0		NEXT PERIODE IS NOT 0 OR 3
	0							ALL	0	0		NEXT PERIODE IS NOT 0 OR 3
REMAINING												INVALID

Clear Control Timing Diagram

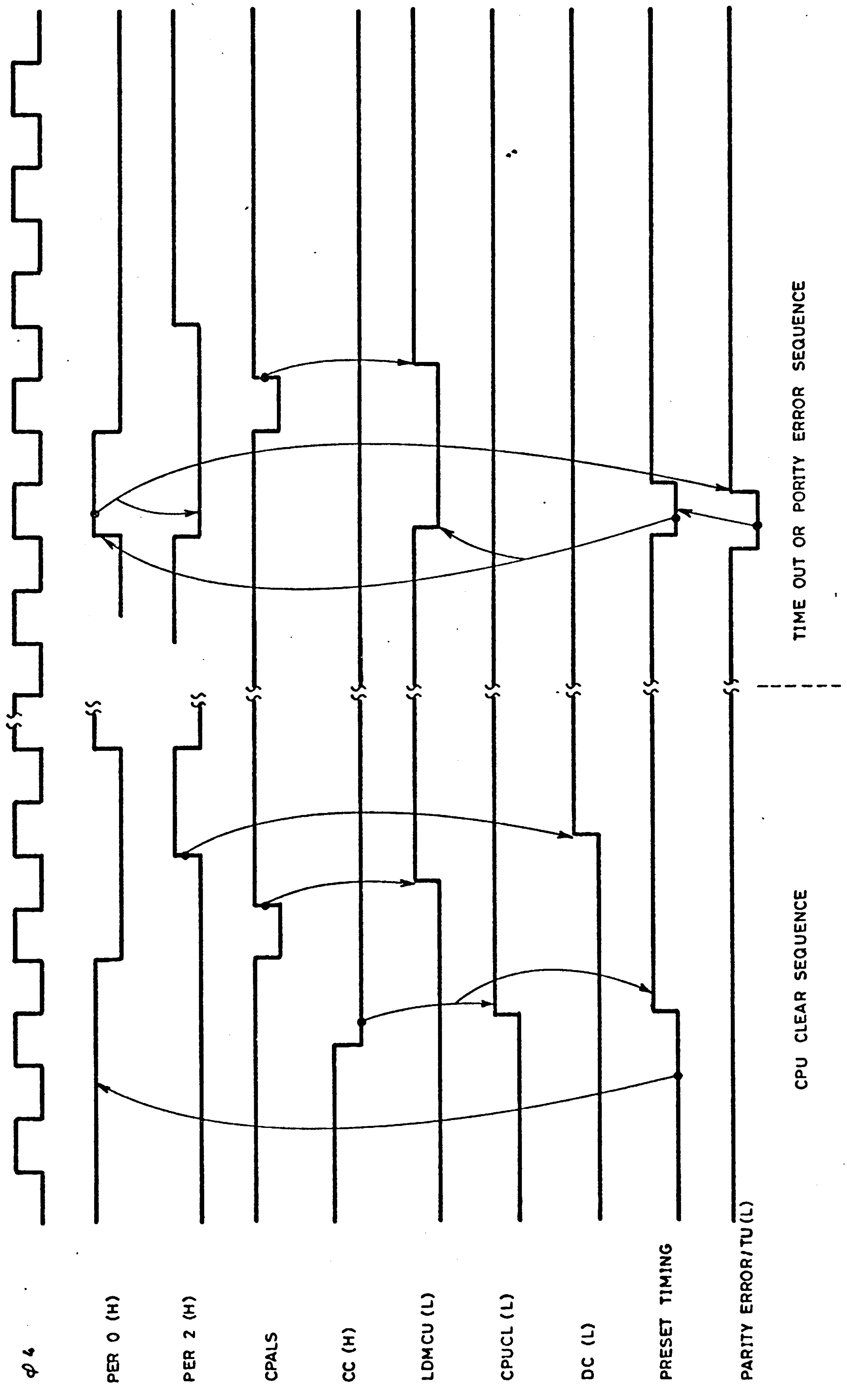
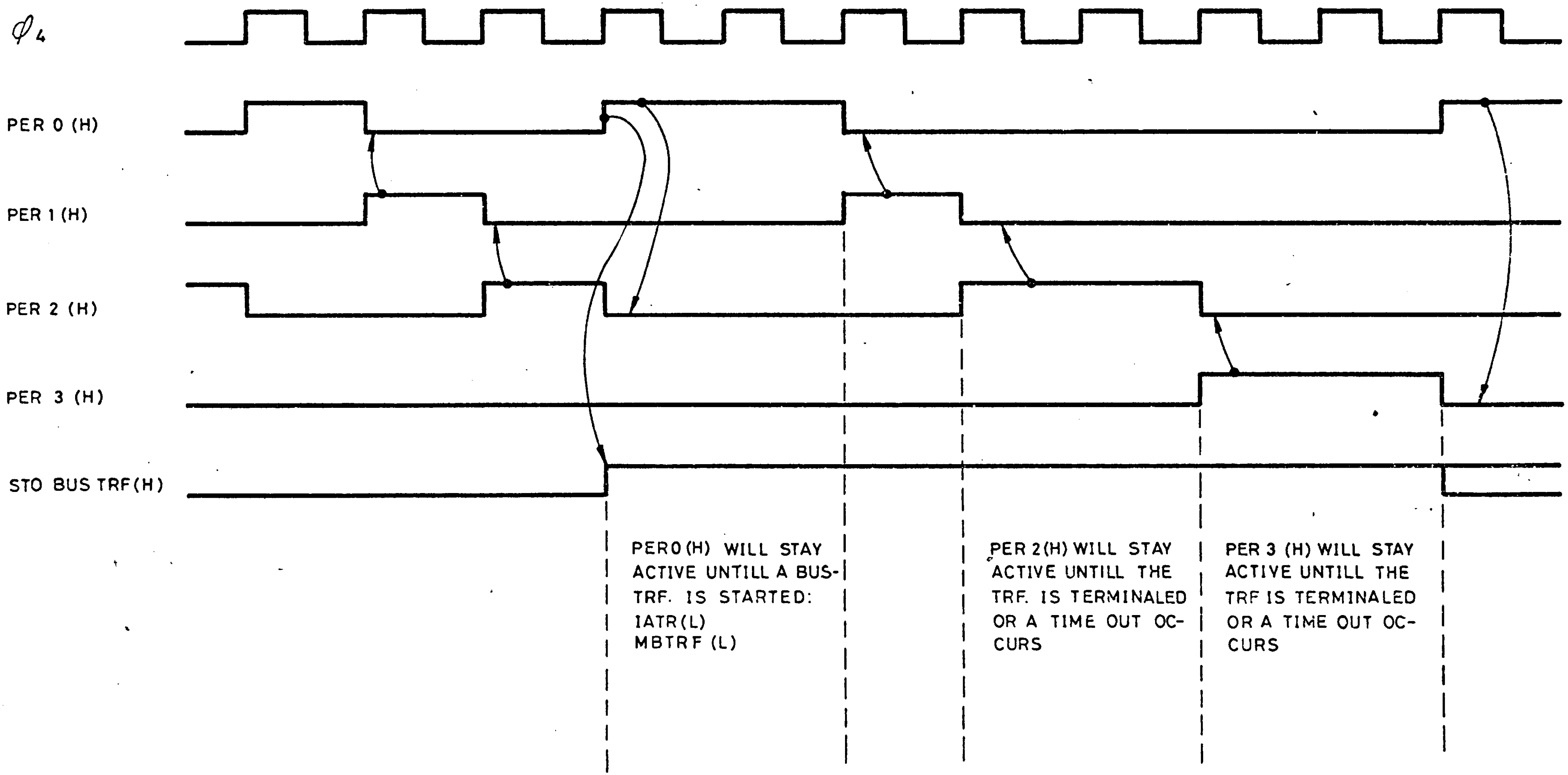


Fig. 4.5.2

Master Timing



Ø4
PER 0 (H)
PER 1 (H)
PER 2 (H)
PER 3 (H)
STO BUS TRF(H)
PER0(H) WILL STAY ACTIVE UNTILL A BUS-TRF. IS STARTED:
IATR(L)
MBTRF (L)
PER 2(H) WILL STAY ACTIVE UNTILL THE TRF. IS TERMINALED OR A TIME OUT OC-CURS
PER 3 (H) WILL STAY ACTIVE UNTILL THE TRF IS TERMINALED OR A TIME OUT OC-CURS

Fig. 4.5.4.

Clock & Bus Control Timing Diagram

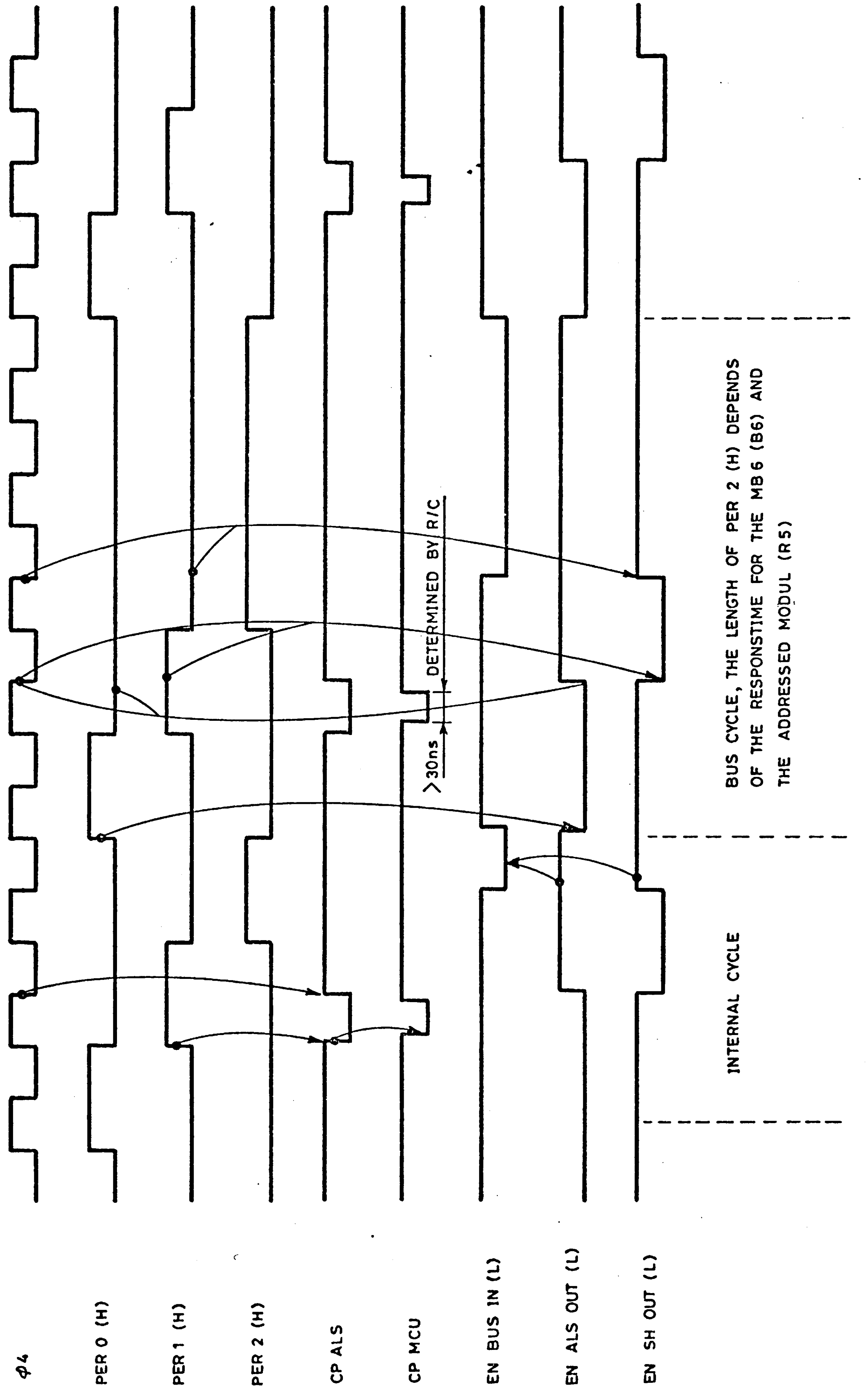


Fig. 4.3.0

4.6 Main Bus Transfer Control F-MBTC-1

The handshaking procedure during Main Bus Communication is controlled by F-MBTC-1.
There are four logical blocks in the Main Bus Transfer Control.

1.	Transfer Control	L-TC-1
2.	Semaphore Control	L-SC-1
3.	Interrupt Receiver	L-IR-1
4.	Voltage Error Detection	L-VED-1

4.6.1 Transfer Control L-TC-1

The handshaking procedure with the Main Bus authority signals and Main Bus transfer signal, are carried out in these logical blocks.
Set up of the circuit for making a Main Bus transfer is done by the one of the two signals:
MBTRF (L): used for Semaphore I/O Transfer.
IMRS (H): used for Memory Transfer.

The bus request signal BRQ can in the Func ↔ Memory mode be delayed until the func module has responded (STOFM 1, PER 3 (L)).
When the CPU has got the authority BG(L) it will issue a TRQ (L) and terminate the transfer when the master timing signal PER (L) occurs, RS (L) or time out detection MTO (L).
Timing diagram fig. 4.6.1 specify the L-TC-1 timing.

4.6.2 Semaphore Control L-SC-1

When more than one transfer to/from memory have to be carried out without interruption the PROM output signal SEMAF S/CL goes high and thereby the signal LBG (L) will be transferred to the MBC module and lock the BG (L) to the CPU until it is released by a bus transfer where SEMAF S/CL is low.
Timing diagram fig. 4.6.2 shows the sequence.

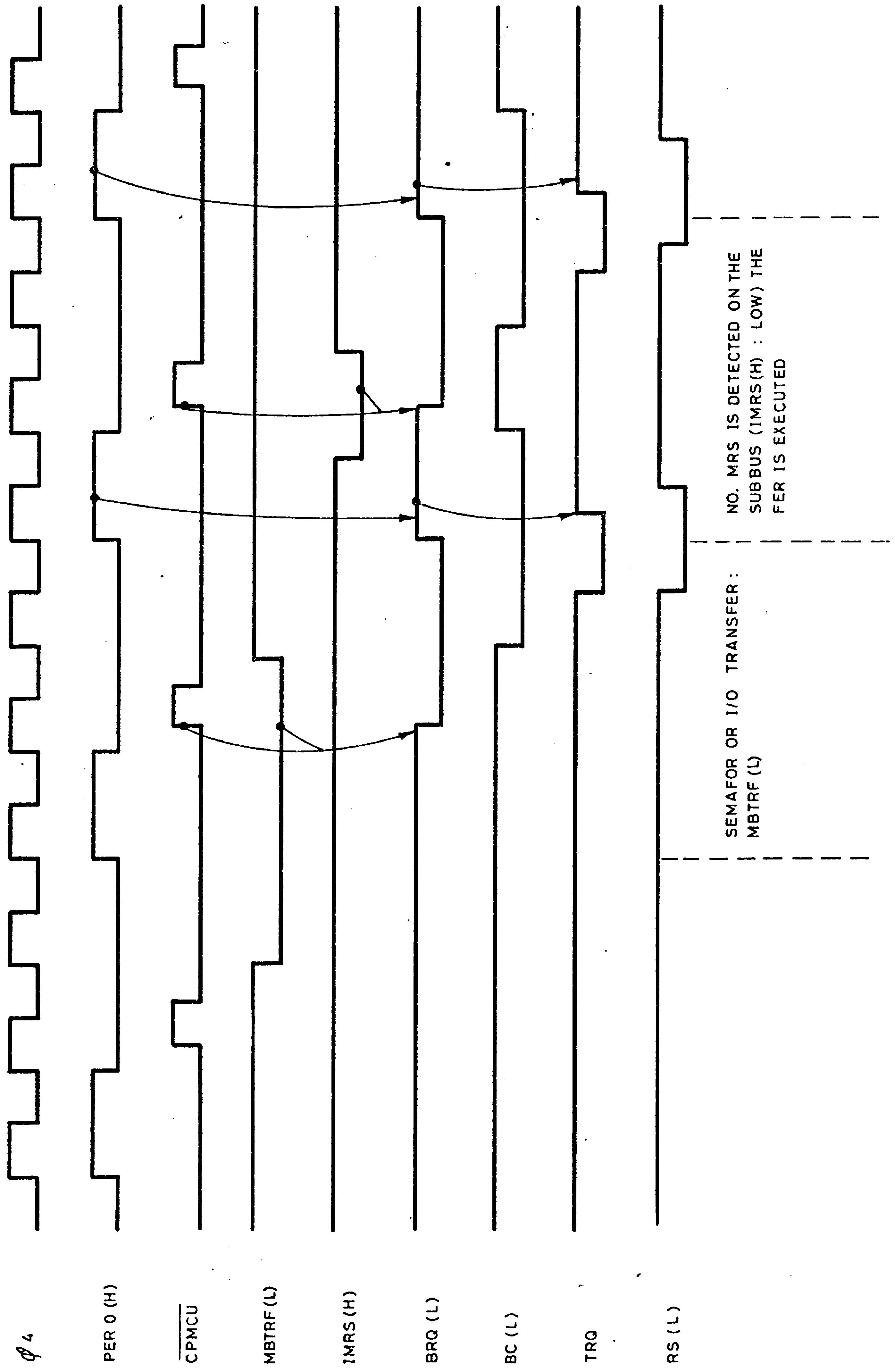
4.6.3 Interrupt Receiver L-IR-1

The L-IR-1 consist of schmitt triggers for receiving of the system control signals related to the three different interrupt types. The generated CPU Interrupt which force CPU INT (H) will also cause, that the CPU receives a CPU interrupt.

4.6.4 Voltage Error Detection L-VED-1

This circuit consist of a gate with the output low if the power is O.K. on the ALB & BIB.

<u>Transfer Control Timing Diagram</u>



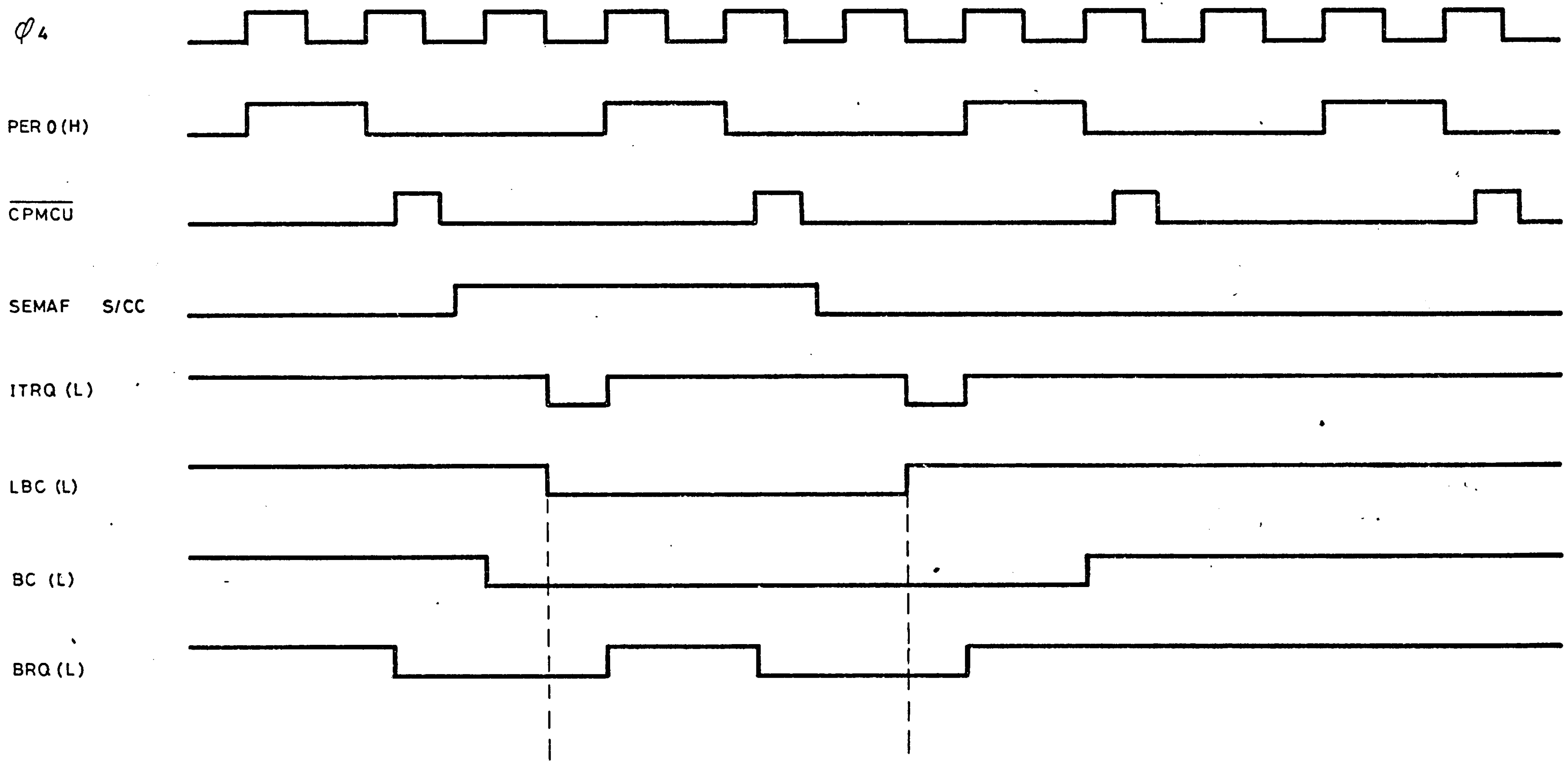
NO. MRS IS DETECTED ON THE SUBBUS (IMRS(H) : LOW) THE FER IS EXECUTED

SEMAFOR OR I/O TRANSFER : MBTRF (L)

Fig. 4.6.1

Fig. 4.6.2.

Semafor Control Timing Diagram



BC (L) IS LOCKED TO THE CPU
WHEN LBC IS ACTIVE

BUS INTERFACE BOARD (BIB)	sign/date GB/780530	page
	repl	project

5
SIGNAL LISTS

K

ALB TO BIB INTERCONNECTIONS SIGNAL LIST	sign/date GB/780524	page 1/5
	repl	project

PLUG TYPE :	P/N
CABEL TYPE: 16 WIRES FLAT CABLE	
LENGTH :	

REFERENCE DESIGNATION	ALB	P1	(C3)
	BIB	J1	(C1)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE:ALB
1	T-BUS 11	I/O
2	T-BUS 10	I/O
3	T-BUS 9	I/O
4	T-BUS 8	I/O
5	I CPU INT (H)	I
6	ENSH (L)	I
7	EN ALS OUT (L)	I
8	GND	
9	T-BUS 12	I/O
10	T-BUS 13	I/O
11	T-BUS 14	I/O
12	T-BUS 15	I/O
13	T-BUS 3	I/O
14	T-BUS 2	I/O
15	T-BUS 1	I/O
16	T-BUS 0	I/O

ALB TO BIB INTERCONNECTIONS SIGNAL LIST	sign/date GB/0524	page 2/5
	repl	project
PLUG TYPE :	P/N	
CABEL TYPE: 16 WIRES FLAT CABLE		
LENGTH :		
REFERENCE DESIGNATION	ALB P2 (C5) BIB J2 (C3)	

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE : ALB
1	T-BUS 7	I/O
2	T-BUS 6	I/O
3	T-BUS 5	I/O
4	T-BUS 4	I/O
5	CPALS	I
6	$\overline{\text{CPALS}}$	I
7	CPMCU	I
8	GND	
9	GND	
10	PER0 (L)	I
11	PER0 (H)	I
12	PER2 (H)	I
13	GND	
14	LDMCU (L)	I
15	LDMCU (H)	I
16	GND	

ALB TO BIB INTERCONNECTION SIGNAL LIST	sign/date GB/780524	page 3/5
	repl	project

PLUG TYPE :	P/N
CABEL TYPE: 16 WIRES FLAT CABLE	
LENGTH :	

REFERENCE DESIGNATION	ALB	P3	(D1)
	BIB	J3	(D1)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE: ALB
1	GND	
2	FORCE CPU INT (H)	0
3	II/OI (H)	I
4	ITI (H)	I
5	$\overline{\text{P0}}$	I
6	$\overline{\text{P1}}$	I
7	ITRQ (H)	I
8	GND	
9	GND	
10	$\overline{\text{CPMCU}}$	I
11	DCL (L)	I
12	PARITY ERROR	0
13	$\overline{\text{8MHz}}$	I
14	$\overline{\text{8MHz}}$	I
15	$\overline{\text{2MHz}}$	I
16	GND	

ALB TO BIB INTERCONNECTION SIGNAL LIST	sign/date GB/780524	page 4/5
	repl	project

PLUG TYPE :	P/N
CABEL TYPE: 16 WIRES FLAT CABLE	

LENGTH :

REFERENCE DESIGNATION	ALB	P4	(D3)
	BIB	J4	(D3)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE: ALB
1	AA1	0
2	OP2	0
3	OP0	0
4	AA2	0
5	AA0	0
6	OP1	0
7	DPER0 (H)	I
8	GND	
9	DPER1 (H)	I
10	LD-DREG (H)	0
11	RLP	I
12	RUP	I
13	IUP	0
14	ILP	0
15	SEA17	0
16	SEA16	0

ALB TO BIB INTERCONNECTION SIGNAL LIST	sign/date GB/780524	page 5/5
	repl	project

PLUG TYPE :	P/N
CABEL TYPE: 16 WIRES FLAT CABLE	
LENGTH :	

REFERENCE DESIGNATION	ALB P5 (J7)
	BIB J5 (G1)

PIN NO.	SIGNAL NAME	SIGNAL REFERENCE: ALB
1	TO (L)	I
2	POWER DET MP	I
3	POWER DET AL	0
4	PRESET TIMING (L)	I
5	$\overline{\text{ADDO}}$	0
6	I/O (L)	0
7	BUSTRF (H)	I
8	GND	
9	I R/W	I
10	MDAT 16	0
11	MDAT 17	0
12	MDAT 18	0
13	MDAT 19	0
14	MDAT 20	0
15	IA 19	0
16	IA 18	0

BUS INTERFACE BOARD (BIB)	sign/date GB/780530	page
	repl	project

6

PROM TABLES

K

CPU CR8001/3
BUS I/F BOARD
TRANSFER SET UP CR 1289-1

GB/770412

repl

project

ADDR.		INPUT						OUTPUT								
		MDAT 20	MDAT 19	MDAT 18	MDAT 17	MDAT ~~18~~ 16		I R/W (L/H)	IWCAR (H)	BUSTRF (H)	LDAR (H)	FUNCMODE 1	FUNCMODE 2	EN TBUS/AR (H/L)	SWAFOR S/CL(H/L)	
DEC.	OCT.	E 4	D 3	C 2	B 1	A 0		8	7	6	5	4	3	2	1	DESCRIPTION
0	00	0	0	0	0	0			0	0	0	0	0		0	BC NOP
1	01	0	0	0	0	1		0	0	1	1	0	0	1	0	FNI
2	02	0	0	0	1	0			0	0	0	0	0		0	INS 1
3	03	0	0	0	1	1			0	0	0	0	0		0	TD 1
4	04	0	0	1	0	0		1	1	1	0	0	0	0	0	INC OUT
5	05	0	0	1	0	1		0	0	1	1	0	0	1	0	AR-SF-TD 1
6	06	0	0	1	1	0			0	0	0	0	0		0	TD 2
7	07	0	0	1	1	1		0	0	1	1	0	0	1	0	INSI-FI
8	10	0	1	0	0	0			0	0	1	0	0		0	LAR
9	11	0	1	0	0	1			0	0	0	0	0		0	ALS-TD 1
10	12	0	1	0	1	0		0	0	1	1	0	0	1	0	FI
11	13	0	1	0	1	1		0	0	1	0	0	0	0	0	MAR- TD 1
12	14	0	1	1	0	0		1	0	1	0	0	0	0	0	ALS-DR-MAR
13	15	0	1	1	0	1			0	0	0	0	0		0	TI 1-S8-TD 1
14	16	0	1	1	1	0			0	0	0	0	0		0	TI 1-S4-TD 1
15	17	0	1	1	1	1		0	0	1	1	0	0	1	0	TD 1-FI
16	20	1	0	0	0	0			0	0	0	0	0		0	TD 1-SW-TD 2
17	21	1	0	0	0	1		1	0	1	0	0	0	0	0	TD 1-SW-MAR
18	22	1	0	0	1	0		0	1	1	0	0	0	0	0	INC IN
19	23	1	0	0	1	1		1	0	1	1	0	0	1	0	DR-MALS
20	24	1	0	1	0	0			0	0	0	0	0		0	ALS-TD 2
21	25	1	0	1	0	1		0	0	1	1	0	0	1	1	SEM-FET
22	26	1	0	1	1	0		1	0	1	0	0	0	0	1	SEM-STO
23	27	1	0	1	1	1		0	0	1	1	0	0	1	0	MALS-TD 1
24	30	1	1	0	0	0		1	0	1	0	0	0	0	0	TD 2-SP-ALS
25	31	1	1	0	0	1		0	0	1	1	0	0	1	0	TD 1-SF-ALS
26	32	1	1	0	1	0		1	1	1	0	1	1	0	0	FUNC-MAR
27	33	1	1	0	1	1		0	1	1	0	0	1	0	0	MAR-FUNC
28	34	1	1	1	0	0		0	0	1	1	0	1	1	0	MALS-FUNC
29	35	1	1	1	0	1		1	0	1	0	1	0		0	ALS-FUNC
30	36	1	1	1	1	0		1	0	1	1	1	1	1	0	FUNC-MALS
31	37	1	1	1	1	1		0	0	1	0	1	0		0	FUNC-TD 1
		4	3	2	1	0		8	7	6	5	4	3	2	1	