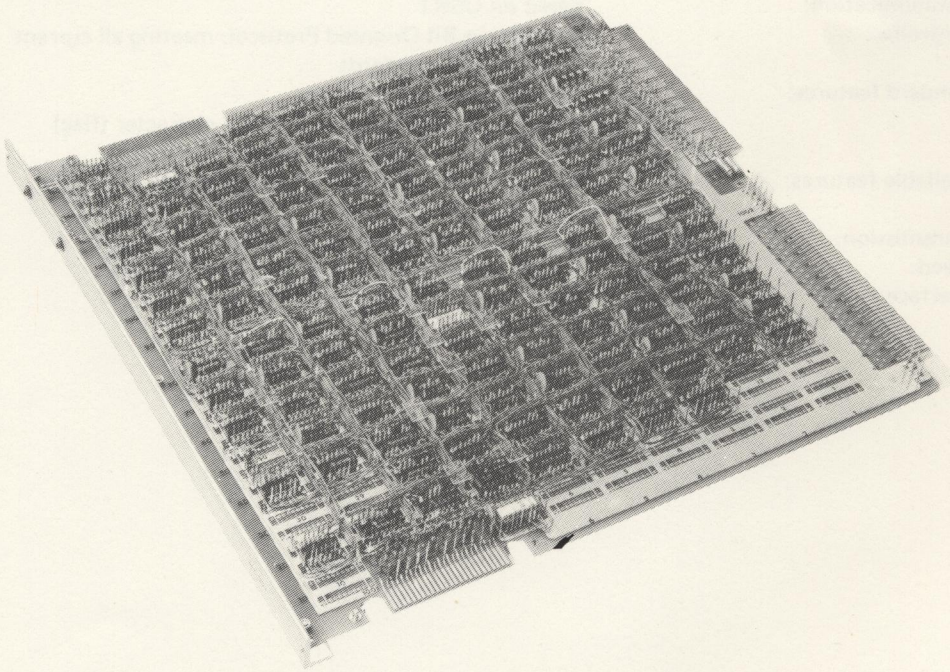
RC 3684
HDLC Multiplexer

- MICROPROGRAMMED
- 4 CHANNELS
- SYNCHRONOUS TRANSMISSION
- UP TO 48,000 BITS PER SECOND/CHANNEL
- ACCORDING TO CCITT RECOMMENDATIONS
- FULL DUPLEX



GENERAL

The RC 3684 High-level Data Link Controller (HDLC) Multiplexer implements CCITT recommendations regarding the interconnection of computers and different kinds of communication lines. Supporting full duplex synchronous communication.

Connected to an RC NET, or any public packet switched data network, the HDLC multiplexer is defined as the Data Terminal Equipment (DTE). The network being the Data Communication Equipment (DCE).

In any case the HDLC multiplexer interfaces communication facilities to an RC 3600 computer used as a node in a network, as a remote device controller, or as a front-end of a host computer. The HDLC multiplexer takes over communication protocol and other control functions. Due to this intelligence the HDLC multiplexer relieves the RC 3600 CPU from trivial communication tasks.

The HDLC multiplexer acts towards the network structure as a part of the RC 3600, and towards the RC 3600 as a part of the network structure.

CHARACTERISTICS

The RC 3684 HDLC multiplexer consists of three parts: a synchronous line adaptor, a microprogrammed HDLC controller, and a HDLC microprogram.

The synchronous line adaptor supports 4 full duplex modem connections according to CCITT recom. V24 and V35. Transmitter and receiver clock may be supplied from either the connected modem or from an internal clock generator. Possible bit rates: 800 to 48000 bps. The maximum summarized speed for all connected lines is 100 kbps.

The HDLC controller executes the HDLC microprogram stored in local memory, actually making up an extension of the instruction facilities found in the RC 3600 CPU. The microprogram facilitates local buffering of data, block transfer of data between RC 3600 memory and local memory, and is controlled by the RC 3600 by means of channel programs. Communication protocol is supported according to CCITT recom. X25 level 2 lap B.

SPECIFICATIONS

CPU:	microprocessor, extending (and compatible with) RC 3603 CPU
Memory:	1 KW RAM, 1 KW PROM
Communication:	based on USRT
Controller:	performing Bit Oriented Protocol; meeting all current international standards
Standard features:	zero insertion and deletion detection and generation of frame character (flag) error control (CRC 16 generation/control)
Available features:	internal clock generator (modem-clock) internal real time clock
Transmission:	800 to 48000 bps per channel
Speed:	100 kbps summarized for all connected lines
Interface:	synch., CCITT recom. V24 and V35

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This datasheet is of a summary nature and specifications are subject to change without prior notice.