## RC 4000 COMPUTER

## General

The RC 4000 is a general-purpose, digital computer of medium size. Instructions are 24-bit words with a single address allowing direct addressing of a primary store of up to 128 K words of 24 bits. The cycle time is 1.5 microseconds, operation times typically 3 to 4 microseconds. Operands are of 12, 24 , or 48 bits with fixed-point or floating-point aritmetic. The protection system is based on a 3-bit code (protection key) attached to each 24-bit word of the internal store.

## Instruction Format

The RC 4000 instruction format includes an operation byte of 12 bits and an address byte of 12 bits. The operation byte specifies: one of 58 basic operations; a result register, $W$; an addressing mode, $M$; and an index register, X . An index designator equal to zero indicates no indexing. The address byte specifies a displacement, D, of from - 2048 to 2047 bytes within the program, which is adequate for most addresses.

OPCODE W M X DISPLACEMENT

| 6 | 2 | 2 | 2 | 12 |
| :--- | :--- | :--- | :--- | :--- |

For direct addressing of the entire store, an effective address of 24 bits, $A$, is generated as follows (where M indicates addressing mode, $X$ index register, D displacement, and IC instruction counter):
$M=00 \quad A=X+D$
$M=01 \quad A=$ word $(X+D) \quad$ indirect
$M=10 \quad A=X+I C+D \quad$ relative
$M=11 \quad A=$ word $(X+I C+D)$ relative indirect


## Arithmetic Operands

The basic arithmetic operand is a 24 -bit word, a word length sufficient for most integer arithmetic. The RC 4000 also includes as standard double-length operands of 48 bits to satisfy the requirements of scientific computation and administrative data processing.

## Byte Handling

Direct addressing of 12-bit bytes not only provides a powerful tool for manipulating character strings encountered in file maintenance activities and program translation, but ensures efficient storage of small integers in process control applications, where the computer must handle large quantities of analog input data of 10 to 12 bits.

## Register Structure

The RC 4000 has four accumulator registers, three of which also function as index registers. By removing the distinction between index and accumulator registers, and by extending the number of the latter to four, the full instruction set is made available for immediate address modification, whereas empty transfers of registers to the store are considerable lessened. The registers are adressable as the first four words of the internal store, which makes interregister operations possible.

## RC 4000 TIME-SHARING FEATURES

The RC 4000 is designed for time-sharing operation under the control of a monitor program. Features that facilitate time-sharing are storage protection, privileged instructions, and program interruption.

## Program Protection System

To prevent an erroneous user program from destroying data or parts of the monitor program, each storage word contains 3 protection bits called the protection key. A special register of 8 bits specifies which protec-

tion keys are accessible within the current program. Storage locations that are inaccessible to the current program can be neither altered nor jumped to.

## Privileged Instructions

All input/output operations as well as the interruption system and storage protection are handled by privileged instructions, which can only be executed within the monitor. Attempts to violate the protection system cause program interruption.

## Program Interruption System

A computer used for real-time time-sharing applications must respond quickly to exceptional internal and external events. In the RC 4000 this is achieved by means of a program interruption system, which is capable of registering up to 24 signals simultaneously. Depending on priority status, any of these signals can interrupt the current task program at once.

RC 4005 CENTRAL PROCESSOR



RC 2000 Paper Tape Reader


RC 315 Input/Output Typewriter


RC 150 Paper Tape Punch

## RC 4005 CENTRAL PROCESSOR I RC 4081 CORE STORE MODULES / RC 4082 STORE EXPANSION FRAME

## Central Processor

The main frame includes: an arithmetic unit, control unit, internal core store of 16 K 24 -bit words, data channels for the connection of peripheral controllers, controllers for the standard peripherals (RC 315 Input/ Output Typewriter, RC 150 Paper Tape Punch, RC 2000 Paper Tape Reader), interrupt unit, digital clock, maintenance panel, power supplies, ventilators, and air filters. A number of error alarms is also included. Parity, temperature, and supply voltages are constantly supervised.

## Core Store Modules and Store Expansion Frame

The internal store can be expanded in core store modules of 16 K words. Whereas the main frame itself allows expansion up to 64 K words, further expansion up to a total of 128 K words is possible in the store expansion frame. Modules of 4 K and 8 K words are available for small systems.

## Connection of Peripherals

With the exception of the three standard peripheral devices mentioned above, peripherals are connected by means of one or more input/output controller cabinets, in which the individual controllers are placed. The central processor and the input/output controllers are connected by means of cables with standardized plugs allowing fast and trouble-free field changes in existing RC 4000 systems.

## Interrupt Unit Expansion

The interrupt unit, which contains 24 maskable levels, can be expanded by combining a number of buffered digital inputs (logical or) in one interrupt signal. A

## CHARACTERISTICS

Operation Times
See complete list on back of specification.

## Internal Store

Cycle time: $1.5 \mu \mathrm{~s}$.
Capacity, general: 4 K to 128 K words.
Capacity, RC 4005 processor: 16 K words.
Capacity, RC 4081 module: 16 K words.
Word size: 24 bits +3 protection bits +1 parity bit.

## Data Formats

Fixed-point operands: 12, 24, and 48 bits.
Floating-point operands: 48 bits.

## Instruction Set

Instruction word length: 24 bits.
Number of operation codes: 58.
Effective address: 24 bits
Address displacement: 12 bits.
Number of accumulator registers: 4.
Number of index registers: 3 .
Relative and indirect addressing modes are available.
Protection System
Protection key: 3 bits/word.
Number of privileged instructions: 8.

## Interrupt System

Number of maskable interrupt levels: 24.
Interrupt response time: $7.5 \mu \mathrm{~s}$ on completion of current instruction,
response program reads and clears the contents of the digital input registers.

## Operator's Console

The separate console contains the operator's panel with keys for reset, start, and autoload along with indicators for device status (local/remote) and alarms. The three standard peripherals can be placed on the console. Facilities for handling paper tape and the like are included.

## Technology and Construction

Components are exclusively integrated circuits and silicon types. True modular construction enables repair by means of plug-in modules. Spare parts comprising a complete set of modules are available at reasonable cost.
The main frame cabinet has three sections. The middle section contains the arithmetic unit in a fixed frame, whereas the control unit and the controllers for the standard peripherals are placed on hinged, swing-out frames. On each side of the middle section there are 19 -inch sections, one containing power supplies, the other up to 4 core store modules of 16 K words each. The store expansion frame constitutes another 19 -inch section.
Ventilators take in cooling air through filters, either at the sides or at the bottom of the cabinet from beneath the floor. (This must be specified prior to delivery). Air escapes at the top. The cabinet is covered with easily removable panels and top.
The maintenance panel enables manual operation, and includes execution of instructions step by step as well as display and alteration of the contents of all registers.

## Digital Clock

Selectable intervals: 1.6 ms to 1.6 sec .
Time resolution: 0.1 ms .
Frequency stability: 1 part in $10^{6}$.

## Input/Output Systent

Direct access channel, max. speed: 500,000 words/sec
(RC 4005).
Single word channel, speed: program-dependent.
Max. number of device: 64 .
The controllers RC 4121, 4171, and 4161 for the standard peri pherals (typewriter, punch, tape reader) are included in the
RC 4005 processor.

* This limitation is physical/electrical, not logical.

Size and Weight
Width: 234 cm .
Depth: 71 cm
Height: 145 cm .
Weight: 500 kg .

## Power

$220 \mathrm{~V} \pm 10 \%, 50 \mathrm{~Hz} \pm 4 \%$, max. 15 A .

## Amblent Alr

Temperature: 0 to $45^{\circ} \mathrm{C}$.
Relative humidity: 30 to $70 \%$
Cooling air flow:
max. 64 K core store: $1800 \mathrm{~m}^{3} / \mathrm{hour}$.
$\max .128 \mathrm{~K}$ core store: $2800 \mathrm{~m}^{3} /$ hour .
Heat dissipation:
with 16 K core store: $1900 \mathrm{kcal} /$ hour.
addition per 16 K module: $550 \mathrm{kcal} / \mathrm{hour}$.

This list gives numerical code, Slang designation, and execution time in microseconds for all instructions. The times apply to direct addressing; for address modification add the following:

| Relative addressing: | $0.5 \mu \mathrm{~s}$ |
| :--- | :--- |
| Indexing: | 0.5 |
| Relative addressing | 1.5 |
| and indexing: | Indirect addressing |
| numeric codes 0-31, 48-63: | 1.5 |
| numeric codes 32-47: | 1.0 |

The execution time for an interrupt response is $7.5 \mu \mathrm{~s}$.

## Address Handling

| 9 AM | Modify Next Address | 2.0 |
| :--- | :--- | :--- |
| 11 AL | Load Address | 1.5 |
| 33 AC | Load Address | 2.5 |

Register Transfer

| 3 HL | Load Half Register | 3.0 |
| :---: | :---: | :---: |
| 26 HS | Store Half Register | 4.0 |
| 20 RL | Load Register | 3.0 |
| 23 RS | Store Register | 4.0 |
| 25 RX | Exchange Register and |  |
|  | Store | 4.5 |
| 54 DL | Load Double Register | 5.0 |
| 55 DS | Store Double Register | 7.0 |
| Integer Byte Arithmetic |  |  |
| 19 BZ | Load Byte with Zeros | 3.0 |
| 2 BL | Load Integer Byte | 3.0 |
| 18 BA | Add Integer Byte | 3.5 |
| 17 BS | Subtract Integer Byte | 3.5 |
| Integer Word Arithmetic |  |  |
| 7 WA | Add Integer Word | 3.0 |
| 8 WS | Subtract Integer Word | 3.0 |
| 10 WM | Multiply Integer Word | 15.5 |
| 24 WD | Divide Integer Word | 17.0 |
| Integer Double Word Arithmetic |  |  |
| 56 AA | Add Integer Double Word | 5.0 |
| 57 SS | Subtract Integer Double Word | 5.0 |
| Arithmetic Conversion |  |  |
| 32 Cl | Convert Integer to Floating | $\begin{aligned} & 3.0+0.5 \times \text { shifts } \\ & \text { (address }=0 \text { ) } \end{aligned}$ |
|  |  | $\begin{aligned} & 4.0+0.5 \times \text { shifts } \\ & \text { (address } \neq 0 \text { ) } \end{aligned}$ |
| 53 CF | Convert Floating to Integer | $\begin{aligned} & 4.5+0.5 \times \text { shifts } \\ & \text { (address }=0 \text { ) } \end{aligned}$ |
|  |  | $\begin{aligned} & 5.0+0.5 \times \text { shifts } \\ & \text { (address } \neq 0 \text { ) } \end{aligned}$ |

Floating-Point Arithmetic
48 FA Add Floating
11.0

49 FS Subtract Floating 11.0 50 FM Multiply Floating 26.0 52 FD Divide Floating 27.0

## Logical Operations

| 4 LA | Logical And | 3.0 |
| :--- | :--- | :--- |
| 5 LO | Logical Or | 3.0 |
| 6 LX | Logical Exclusive Or | 4.0 |

## Shift Operations

36 AS Shift Single
Arithmetically $\quad 3.0+0.5 \times$ shifts
37 AD Shift Double
Arithmetically
38 LS Shit
$\begin{array}{ll}38 \text { LS } & \text { Shift Double Logically } \\ 39 & 3.5+0.5 \times \text { shifts }\end{array}$
34 NS Normalize Single $\quad 5.0+0.5 \times$ shifts
35 ND Normalize Double
$5.5+0.5 \times$ shifts

Sequencing
13 JL Jump with Register Link
2.5 or 3.0 (with link)

40 SH Skip if Register High
41 SL Skip if Register Low
43 SN Skip if Register Not Equal
44 SO Skip if Register Bits One 3.5
45 SZ Skip if Register Bits Zero $\quad 3.0$
46 SX Skip if No Exceptions $\quad 3.0$
$\begin{array}{lll}46 \text { SX } & \text { Skip if No Exceptions } & 3.0 \\ 21 \text { SP } & \text { Skip if No Protection } & 3.0\end{array}$

| Monitor Control |  |  |
| :---: | :---: | :---: |
| * 15 JE | Jump with Interrupt Enable | 2.5 or 3.0 (with link) |
| * 14 JD | Jump with Interrupt | 2.5 or 3.0 (with link) |
|  | Disable | 2.5 or 3.0 (with link) |
| $\begin{aligned} & \text { * } 47 \text { IC } \\ & 31 \text { IS } \end{aligned}$ | Clear Interrupts Bits | 2.5 |
|  | Store Interrupt |  |
|  | Register | 4.0 |
| * 12 ML30 MS16 XL | Load Mask Register | 3.0 |
|  | Store Mask Register | 4.0 |
|  | Load Exception |  |
|  | Register | 3.0 |
| 27 XS | Store Exception |  |
|  | Register | 4.0 |
| * 28 PL | Load Protection Register | 3.0 |
| 29 PS | Store Protection | 3.0 |
|  | Register | 4.0 |
| 22 KL | Load Protection Key | 3.0 |
| $\begin{array}{r} 22 \mathrm{KL} \\ * \\ * \\ * \\ 110 \end{array}$ | Store Protection Key | 4.0 (reiected) |
|  | Input/Output | 4.0 (rejected) <br> 5.0 (read) |
| 0 AW |  | 7.0 (sense) |
|  | Autol | 6.5 (write or control) |
|  | Auto | tape reader |

