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Specification of the RC9000 Computer.

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RC Computer, December 6, 1985.

Contents:

1 Introduction.

The purpose of the project outlined in the following is to provide a new product, with the listed characteristics:

- high degree of fault tolerance
- high performance
- flexibility through multiprocessing
- (industri) standard compatible operating system, i.e. UNIX based
- distributed operating and file system
- expansion possibility for existing RC8000 customers.

By entering a joint venture with TOLERANT SYSTEMS the project is given a starting platform, which is considerably higher and more well defined than the one offered in a totally new development project.

On the other hand, the cooperation with TOLERANT SYSTEMS will remove some degrees of freedom in the system design. This project description does not contain any evaluations of the loss suffered by the cooperation.

Chapter 2 offers an overview of the system architecture, whereas chapter 3 and 4 identify the system components and the activities involved in the project.

Chapter 5 outlines the project strategy and gives estimates of the development costs incurred by the individual steps. Furthermore, some sample configurations, showing the state of the product at the completion of the project steps, are provided.

Chapter 6 lists production cost estimates of all new hardware system components.

2 System Architecture.

The RC9000 system architecture is shown i figure 2.1. The CPU's are connected the to main memory, controllers and other elements in the system through one system bus, while the disk units, tape stations, terminals etc. are connected through an I/O channel.

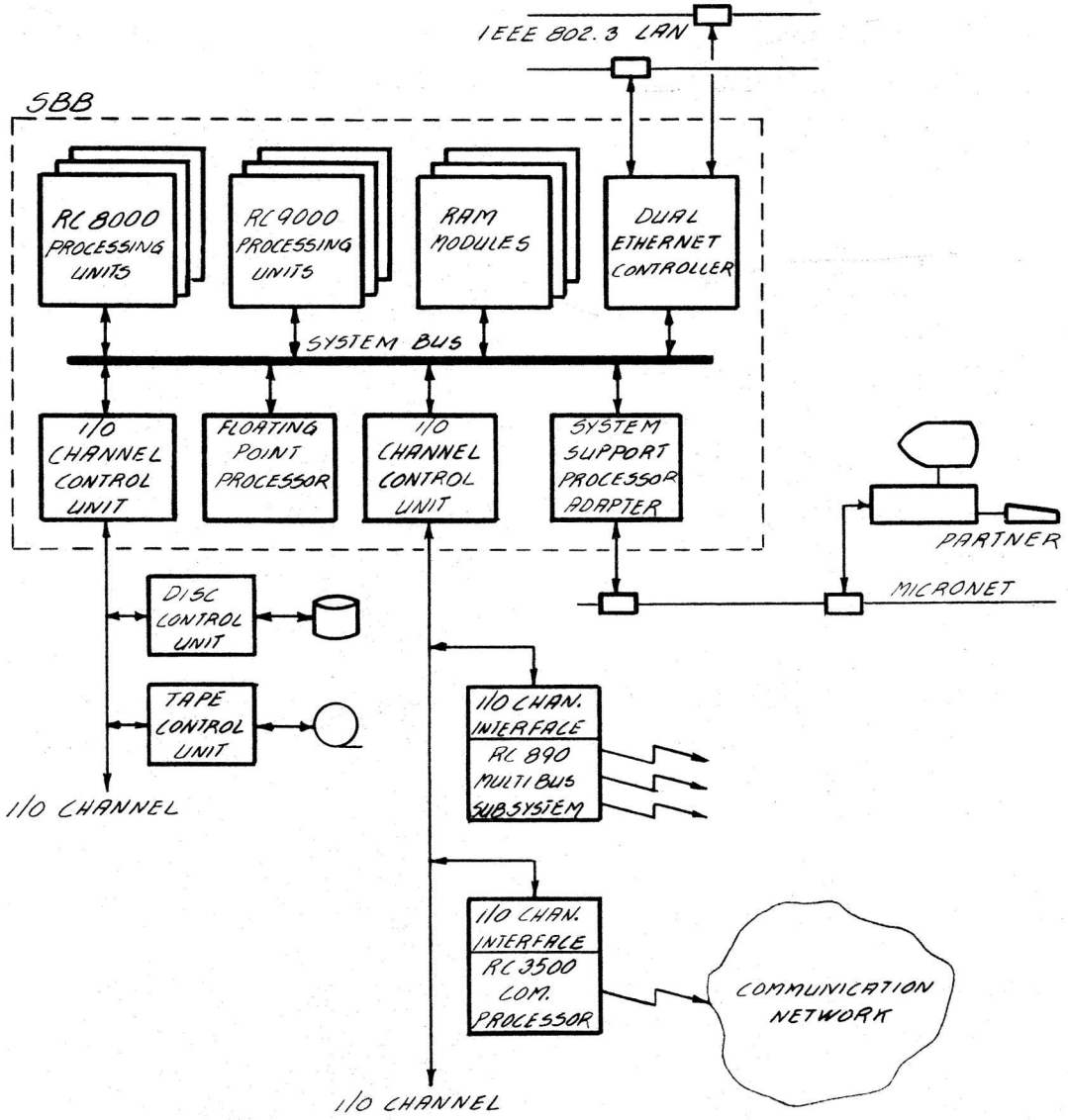


fig 2.1

The RC9000 system operates either as a RC8000 in the usual RC8000 operating environment with a word length of 24 bits, or as a **RISC** based computer operating in an **UNIX** environment with a word length of 32 bits, or as both.
The memory is 32 bits wide, where the RC8000 uses 24 bits of each word. The controllers on the system bus takes care of the conversion when accessing the memory.

The RC9000 system is collected in a unit called a System Building Block (SBB). The SBB contains the CPU, the main memory, I/O channel controller (IOP), LAN controller (IEEE 802.3), system support processor (SSP), and floating point unit (FPU).

The CPU part of a SBB may contain a number of RC8000 CPU's and a number of RC9000 CPU's, all working in parallel.

Peripheral devices like disks, tape stations, and terminals are connected through the I/O channel. The I/O channel interfaces to a local area network through a Multibus adapter and to a wide area network through a RC3502 communication processor.
The disk drives may be connected to two disk controllers and thereby to two I/O channels in different SBB's. If this feature is used, only one of the channels is active at a time.

The SSP is responsible for the initialization of the system, i.e. power up diagnostics on the elements, configuration, autoload and the like.
While the system is running, it performs load measurements and acts as a watchdog, which, in case of failures, is responsible for re-configuration of the system.

A number of SBB's may be connected through the LAN-controller on the system bus. This connection is one of the fundamental parts of the **fault tolerant** system.

As an option, a floating point unit (FPU) may be attached to the system. This will increase the performance of floating point operation and it will support BCD operations as well.

2.1 RC9000 Cluster and Fault Tolerance.

Through the LAN controller a number of RC9000 (SBB's) may be loosely connected.
The **extended UNIX** operating system (running on the RC9000 CPU's) supports a distributed file system which allows a UNIX user to run on an arbitrary SBB in the system. Furthermore the UNIX operating system has been extended with a **transaction executive** for high performance transaction applications. The transaction executive includes facilities for fault tolerant execution of programs through the system calls 'begin transaction' and 'commit transaction'.
The prerequisite of using the fault tolerant mode is, that the system contains at least two SBB's connected through a LAN and that important disks are connected to two SBB's (by using dual access disks).
A dual access disk is 'owned' by a master SBB which controls any access to the disk. Access to the disk from another SBB goes through the LAN and the master SBB.
If the master SBB fails, the alternative SBB becomes the master of the disk, and the failed SBB is de-allocated from the system.

3 Identification of Hardware System Components.

3.1 RC9000 System Bus.

The RC9000 System Bus is a high speed backplane bus, which connects the Processing Units, the I/O Channel Controllers, the LAN Controllers, the System Support Processor, the Floating Point Units, and the Main Memory Modules. The System Bus has the following main characteristics:

Synchronous 10 Mhz bus.

Multiplexed address/data lines. 32 address bits and 64 data bits.

Transfer of the following data formats are supported:

Single words: 4 bytes
Double words: 8 bytes
Blocks: 2, 4, 6, and 8 double words

Transfer rates (no idle bus cycles):

13 Mbytes/s for single words.
26 Mbytes/s for double words.
64 Mbytes/s for blocks (8 double words).

Bus operations are limited to read and write in a single 4096 Mbytes memory address space. I/O and interrupts are implemented by means of these operations.

Up to 20 card positions in a backplane.

A small part of the large address space is reserved for addressing of the individual slots (1M byte / slot). This feature makes it possible for the System Support Processor to detect which modules are available in the system and to replace address switches with control registers controlled by the SSP (automatic system configuration).

Distributed parallel bus master arbitration (no daisy chains).

3.2 RC8000/90 Processing Unit.

The RC8000/90 processor is instruction set compatible with the current line of RC8000 Processing Units. It interfaces to the RC9000 System Bus and can be used as a processing unit in a RC9000 system. The main characteristics are:

24-bit word length. 4 accumulators, 3 of which may be used as index registers.

24-bit single address instruction format with 64 basic instructions and 16 addressing modes. The smallest addressable unit is a half-word (12 bits).

Data formats: 12, 24, and 48-bit integers (2's complement). 48-bit floating point numbers with a 36-bit fraction and a 12-bit exponent.

8 Mwords (24-bit) logical memory address space per process, divided into 4 segments of maximum 2 Mwords. Memory protection is provided on a segment basis, and the access rights includes: no access, read only, and read and write. The logical segment address is translated into a 32-bit physical RC9000 memory address, providing a total physical adress space of 1024 Mwords. A RC8000 24-bit word occupies one RC9000 32-bit word.

The processor has separate instruction and data caches, 4 Kwords each. The cache memories are direct mapped and uses store through updating.

The cycle time of the processor is 125 ns. Instructions are executed in a four stage pipeline. The average instruction execution time for a typical mix of instructions is approximately 250 ns, coresponding to 4 MIPS.

3.3 RC9000 Processing Unit.

The RC9000 is a 32-bit processor with Reduced Instruction Set Computer (RISC) architecture providing an estimated performance of 11-12 MIPS. The processor may be employed in a multiprocessor configuration for higher performance.

The instruction set comprises simple three-address instructions that operate on registers in one cycle and load and store instructions that move data between memory and registers. Data and instructions are 32 bits long. Addresses are byte addresses, but memory only handles words on word boundaries. Loading and storing of bytes require multiple instructions including byte extraction and insertion, respectively.

The registers are split up into a set of 128 registers for global data and a stack of 128 registers for procedure local data (activation records). All registers in the stack are accessible and are addressed relative to a stack pointer. Software maintains an overflow stack in memory. The activation records may overlap allowing instantaneous transfer of parameters between procedures. Use of a stack allows data to be assigned absolute addresses at run-time facilitating linking of modules and use of recursive procedures.

A technique called delayed branching is used to allow branches to occur in a single cycle. Multiplication and division are supported with step instructions that proceed one bit at a time.

Demand page virtual memory is supported with 32-bit logical and physical addresses. The transformation is done by a memory management unit (MMU) - presumably MC68851. The protection is accomplished through the MMU and the states user and supervisor.

There are separate instruction and data caches, both 4 Kwords and direct mapped. The instruction cache operates on logical addresses. The data cache operates on physical addresses allowing snooping and employs store through updating.

The processor has four pipeline stages and will be implemented using Advanced Schottky TTL providing an estimated cycle time of 70ns. The earlier quoted figure of 11-12 MIPS takes into account load/store instructions and cache misses.

The processor occupies one or two slot positions in the SSB cabinet.

3.4 System Support Processor.

The System Support Processor (SSP) resides on the SBB systembus.

The SSP provides the following system support facilities:

- Selftest initiation on the SBB components. The SSP initiates a selftest on all individual SBB components after power up, reset, and on request.

- Configuration of SBB.
  After power up, at reset, and on request the SSP will "read" all slots of the SBB to identify all boards in the crate. After identification the SSP will set up the configuration, such as defining the address space for each memory board.

- Monitoring.
  The monitoring contains tasks like
  performance measurements,
  load measurements,
  logging of errors, and specified events.

- System autoload.
  The SSP holds all basic software (kernel, drivers, andoperating system) necessary for the controllers, memory boards and CPU's in the SBB. The software which is placed on the Winchester disk will be loaded after power up, reset and on request.

- Reconfiguration.
  In case of faults detected on an SBB component (board) the SBB will reconfigure, if possible, the SBB without the faulty component.

- CPU/kernel debugging.
  It is possible from the SSP to run the RC9000 CPUs in single step and to read the registres and the memory after each step.

- System Time.
  Any SBB component may 'read' the system time from SSP.

The SSP user interfaces are achieved via a V.24/V.28 interface and a 1 MBit/s LAN (micronet) interface. SSP's from a cluster of SBB's may be interconnected via the LAN as may the LAN be used for interfacing the SSP to a PC used for graphic presentation of SSP data.

The SSP is build around a 32-bit microprocessor (INTEL 80386). The SSP has 1 MByte of local memory.

The SSP has a SCSI interface for Winchester disk. The Winchester disk is used as a boot-load medium and for data logging during statistical measurements.

The SSP occupies one slot position in the SBB cabinet.

The software will be based on the PI-3 kernel, modified for the Intel 386 CPU and Real Time Pascal.

3.5 Main Memory.

The module contains 4 Mbytes of dynamic RAM. It is possible to read or write either 32-bit words or 64-bit words. The memory is connected to the RC9000 synchronous system bus. The clock cycle time is asumed to be 100 ns in the following data.

- Access time:
  Read 32/64 bits: 4 cycles if ready.
  Write 32/64 bits: 2 cycles if ready.
  In block mode, add one cycle for each 32- or 64-bit word.
  The memory will not be ready for a maxmium of 3 clock cycles after refresh and after write.

- Size 4 Mbytes; 1 Mword by 32 bits or 512 Kwords by 64 bits.

- Error correction; corrects single bit error, detects double bit error.

- Selftest and configuration by an on-board microprocessor.

3.6 Input/Output Processor.

The Input/Output Processor (IOP) resides on the RC9000 systembus and interfaces to a number of peripherals.
The I/O channel supports up to 15 I/O controllers. The maximum transfer rate of the I/O channel is approx. 6 MBytes/s.

The IOP is an intelligent controller capable of performing chained channel programs, which previously have been set up in main memory by CPU(s) attached to the RC9000 systembus.

The IOP is built around a microprocessor with an external DMA controller. The microprocessor translates channel programs into I/O controller commands.

The DMA controller is a sequential machine controlled by the IOP onboard microprocessor. After being initialized with a start address and a word count the DMA controller transports of data between main memory and the I/O channel without intervention from the microprocessor on-board the IOP.

When the I/O controller commands involve data transfers between I/O controllers and main memory the data are concatenated/scattered onboard the IOP to/from 16 bytes blocks to utilize the block transfer mode of the RC9000 systembus. In case of RC8000/90 initiated data transfers the IOP also performs the 24-bit/32-bit word transformation needed by the RC8000/90 CPU.

The IOP occupies one slot position in the SBB cabinet.

3.7 Disk Controller.

The RC9000 System has a high performance disk subsystem, which matches the power of the RC9000 CPU. The disk subsystem consists of the disk drives and the disk controller, which interfaces the drives to the RC9000 I/O Channel.

The disk controller/subsystem has the following specifications:

Continuous requests to the disk, using single stream I/O to consequtive segments, is able to deliver one segment for every rotation of the disk (approximately 16 ms).

Enhanced SMD interface to disk.

Controls up to 4 disk drives, each with a capacity up to 800 Mbytes.

Supports disk drives with dual port interface.

Accepts disk data rates up to 20 Mbit/s

Overlapped seeks.

Disk controller has full sector buffering.

Automatic error correction. Data errors are corrected before they are transferred via the I/O Channel.

Maximum overhead in disk controller for transfer of a single sector: 5ms.

3.8 Tape Controller.

The Tape Controller supports tape stations with a Pertec interface. The interface to the Pertec bus is equipped with a FIFO, which is large enough to ensure streaming operation of the tape in situations where the I/O channel or system bus is temporarily occupied.

The following recording techniques are available:

- 1600 BPI Phase Encoded (PE). Start/stop as well as streaming mode. The transfer rate is 160 kbytes/s in streaming mode (100 inch/s), and 40 kbytes/s (25 inch/s) in start/stop mode.

- 6250 BPI Group Coded Recording (GCR). Start/stop as well as streaming mode. The transfer rate is 450 kbytes/s (75 inch/s) in streaming mode.

  The GCR mode is mandatory for backup of fixed media disks. A 500 Mbyte disk can be backed up in about 20 minutes, plus time for changing of tapes.

The tape controller accepts the following operations:

- Position
- Read / Write
- Set mode (PE, GCR, Start/Stop and Streaming)

With I/O operations the controller performs the necessary actions in connection with error corrections:

- Write: Backspace and erase. Up to 5 times
- Read: Repeat 5 times

3.9 Network Connection Controller.

The Network Connection Controller (NCC) for RC9000 is known as a RC3502/2. It contains one or two I/O channel interfaces. Two I/O controllers are used if the NCC should be a dual ported controller (two SBB's connected) and one is used if the duality is made by duplicating the NCC.

The NCC provides the services of the communications network PAXNET.

This includes:

- ISO OSI level 1 to level 5
- Session Control
- Network Management System (NMS)
- Virtual Terminal Concept (VT)
- File Transfer and Access Management (FTAM)

The OSI level 5 - Session Layer - , FTAM, and VT will be accessible from RC9000 applications.

The Session Control and Network Management System are accessed at the RC3502 by using the Network Management Centre, which supports the daily operation of the complete network.

Terminals and hosts may be connected to PAXNET in a varity of ways:

- X.25 PAD (TRIPLE X)

- BSC

- LAN (Ethernet)

- X.25 DTE

The specifications for the I/O channel interface are identical to those of the I/O channel used on the Intel Multibus except for the RC3502 bus interface and the physical layout.

The channel interface contains a DMA controller, arbitration logic and drivers for the two buses, and a microprocessor used tohandle events such as errors, attentions, interrupts, reset, test and execution of channel programs.

The RC3502 NCC:

- 16-bits bit slice processor.

- Context switch 2 - 10 micro sec.

- Main memory max. 3 Mbytes.

- Controllers:
  2 channels HDLC max. 64 kbits/s.
  8 channels async max. 19.2 kbits/s.
  8 channels BSC max. 40 kbits/s.
  LAN
  SCSI
  TPI

- Standard 19" crate.

- PAXNET

3.10 Multibus Adapter.

The Multibus Adapter (MBA) is used to connect Multibus subsystems to the I/O Channel (TPI). The MBA has two interfaces to the I/O channel, and may be connected to two different SBB's.

The specifications for the MBA are identical to those of the channel interface for RC3502, except for the Multibus interface and the physical layout.

The MBA contains a DMA controller, arbitration logic and drivers for the two buses, and a microprocessor.

The microprocessor controls the channel interface and maintains a logical connection between programs on the Multibus subsystem and the channel.

Operations to the MBA is on a high level in order to avoid changes in the operating system when a Multibus Subsystem is attached. The operations are:

- Creating and deleting logical paths from the Multibus to the SBB. (Similar to Protocol and Endpoints on the CIB).

- Sending and receiving messages on the channel.

The operations are exchanged between the MBA and the Multibus Master by writing the commands in the dual port memory of the MBA.

In that way it is possible to make a interface library to be linked to user programs on the Multibus Master. The library includes procedures for opening and closing connections, and sending and receiving channel messages.

If more than one kind of processor must be Multibus Master, a libray may be tailored to each kind of processor.

3.11 Communication Interface Processor.

This existing component of ETERNITY SERIES provides

- two I/O channel interfaces (TPI)
- one parallel port (printer or 16-bit parallel I/O)
- two general serial ports (RS-232/RS-422, full duplex DMA, up to 56 Kb, Bit sync/Byte sync/Async)
- ten serial ports (RS-232, half duplex DMA, up to 19.2 Kb, Async)

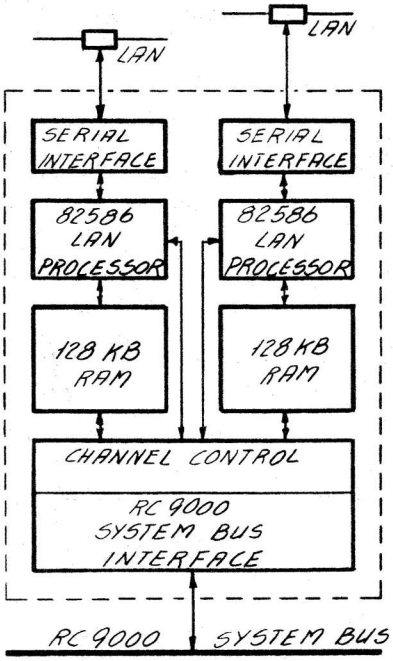
The CIP is based on an NS-32016 microprocessor with 512Kb-1MB RAM. This allows custom protocols and special interfaces, besides the industri standard protocols provided by TOLERANT.

- Async Point-to-point with Echo Negotiation
- Virtual Terminal (?)
- 2780/3780 HASP RJE
- 3270 SNA/SDLC (3274/3278/328x PU2)
- X.25 Network Interface (?)

User programming is supported by a full Realtime Executive, standard development tools, the C programming language, and an interactive debugger.

3.12 LAN Controller.

The dual LAN-controller is shown in the figure below:



It has two independent IEEE 802.3 channels with a common RC9000 bus interface. The bus interface includes a DMA for fast access to the main memory.

Each channel is equipped with a microprocessor, a 128 KB data buffer, and an Intel 82586 LAN processor.

The programmers interface to the LAN controller is the same as to the IOP. The microprocessor reads a channel programs from the main memory, interprets the commands and initializes the LAN-processor accordingly.

The transmission speed of the channel is 10 Mbit/s, and under normal circumstances the load is shared between the two channels.

The operating system may correct one error in the network by excluding the erroneous channel, and continue with one channel.

The two channels are almost duplicated, and a single point error on the controller can be corrected if it does not involve the common bus interface. If an error occurs in the bus interface the SBB will be disconnected from the network.

3.13 FPU/BCD Coprocessor.

Floating point and binary coded decimal (BCD) arithmetic may be accellerated for the RC9000 with an optional FPU/BCD coprocessor which occupies a separate board in the system. Its capabilities may be summarized as follows:

FPU:

- IEEE Standard 754 Draft 10.0.
- Single and double precision.
- 2.5 MFLOPS single precision add., sub., mul.
- 2.5 MFLOPS double precision addition and subtraction.
- 1.6 MFLOPS double precision multiply.
- Microprogrammed division.

BCD:

- Packed BCD addition and subtraction.
- Operates on variable length strings in memory.

4 Identification of Basis Software Components.

4.1 RC8000/90 Basis SW Modifications.

The RC8000 is going to be included in a System Building Block. By doing this the environment of the RC8000 is totally changed compared to the RC8000 of today.
The I/O part of the RC8000 monitor has to be substituted with drivers for the new family of controllers, and a few monitor procedures must be changed as the I/O part is changed.
Because the RC8000 must operate in an 32-bit environment, an address conversion from 24 to 32 bits may be introduced in the RC8000/90 microprogram. If so, the core allocation and process activation may be affected.
At the same time it will be convenient to introduce some improvements concerning the monitor initialization, where a dynamic allocation of resources is wanted (it should be possible to change the number of message buffers, externals etc. without re-compiling the system).

Because the RC8000 CPU is included in a SBB the RC8000 and the RC9000 must share the devices.
To simplify the controllers the two CPU systems must communicate with the devices in the same way.
The communication must be controlled by a common data structure (semaphore) between the RC8000 and the RC9000 CPU-systems. The semaphore controls the access to a common channel program area. There must be a semaphore for each device controller (channel program area).

Each CPU system must contain drivers for the different devices. The way in which communication takes place between the CPU systems and the controllers must be suitable for the RC8000 monitor and for the RC9000 TX-kernel.

The driver to the System Support Processor will support operations concerning:

- system time
- error reports
- alternations in the configuration and other control informations (see section 4.2.).

4.1.1 Sharing of devices.

The device descriptions for the shared devices between the RC8000 and the RC9000 system are not shared. This implies that certain operations on the devices must be executed by the controller instead of by the monitor. The operations are 'reserve device', 'release device' and the like.

The controllers must be able to select the right CPU system to interrupt when an operation (answer) has to be send to the computer. It is important that the CPU system which requersted an operation, is the one that will receive the answer. Furthermore the controller must know which mode a data transfer should use (see section 3.6).

When the system is initialized, the controllers must receive the physical addresses of the CPU's and their kinds. This will enable the controllers to interrupt the proper CPU system without having received a request from the CPU's. This is important in connection with terminals where an attention must cause a link to be created to one of the CPU systems (at least in the RC8000 part).

It must be possible at the same time to have a link from both CPU systems to the same device. When an attention from the device (for instance a state change on a magnetic tape station) has to be sent to the CPU system, both systems must receive the attention. This enable both kernels (monitors) to have an updated description of all connected devices.

4.2 TX Kernel for RC9000.

The current version of the Transaction Executive (TX) operating system does not support a multiprocessor configuration within a single SBB.
To get a higher performance a dual processor solution is selected where the TX operating system is parted in two with each part running on a dedicated processor. This solution will not dynamicly adapt a change in load-pattern.

The RC9000 is provided with a process based real time kernel which supports a multiprocessor system within the SBB.None of the processors in the system is dedicated to the kernel or operating system and user processes may run on any processor.

The kernel is responsible for time slicing of the processes (and coroutines), virtuel memory management, message/answer exchange, input/output and the like. Furthermore the kernel contains primitives for pre-image logging, transaction backout etc., that are necessary in an efficient fault tolerant system like RC9000.

4.3 RC9000 Compilers.

The RC9000 System offers a wide selection of high level languages for application and system developers:

- C (incl. AT & T's system V enhancements)
- Pascal (ISO standard)
- COBOL (Level II)
- FORTRAN 77 (ANSI standard)

The TX facilities and primitives for debugging, fault tolerance, transaction and application management, and inter-process communication are integrated in the language systems by the support of a general interface.

An optimizing code generation, shared by all compilers, increases the performance of the system by exploiting the RISC architecture of the RC9000 CPU.

Other languages, that might be supported in the future, are

- Real Time Pascal
- Ada
- PROLOG.

4.4 Software Tools.

The TX operating system provides a transaction environment with fundamental tools for implementing applications

- interprocess communication
- transaction management
- distributed file system.

Integrated into this environment are primitives for fault tolerant implementations, to be used by the applications if needed:

- 'transaction begin' and 'transaction commit' system calls
- n-plexing of files
- concurrency control
- preimage logging and process control.

Furthermore, application productivity is increased by

- development tools (editors, debuggers)
- forms definition and management system
- on-line application manager
- Structured Query Language (SQL)

New tools to be offered are

- DBMS (ORACLE?)
- 4th Generation Tools

and by exploiting the UNIX-compatibility of TX, several new utilities and supporting systems can be included.

5. Project Requirements, Time Estimates, and Costs.

A strategy, based on four separate projects is outlined below. This allows a stepwise development with intermediate products, that are usable from a marketing point of view. Furthermore, it provides a more flexible plan, where the experience gained in previous steps are taken into account before new steps are initiated.

Project A consists of the necessary activities to introduce Tolerant's Eternity Series in RC's organisation and to provide the necessary know-how within RC to market and support these products. Hence, the main activities of this project are analysis and training.

Project B is the development of the new SBB architecture, the new HW components (excluding RC9000 PU), the new SW modules for these components and the portation of RC8000 Basis SW. This is by far the most critical step in the overall project, as most of the new components are results of this phase. A RC8000/90 Supermini is one product that emerges during this period.

Project C's concern is the merging of the two existing systems: a new fast RISC-based processor to replace the PU's of the Eternity Series, and incorporating these into the new SBB. Furthermore, the TX operating system must be ported to the new HW and necessary modifications of compilers etc. carried out.
A fast Unix-based fault tolerant system is the product of this project.

Project D leads to the target of the overall project: the multiprocessing RC9000 system.
The activities of project D are centered around TX modifications to allow real multiprocessing instead of the RPU/UPU dual PU concept. Besides this, a higher performance is obtained by inclusion of the FPU/BCD coprocessor.

The time schedule for these projects should take into consideration that project A forms the basis of project B. Several components and fundamental characteristics will survive the "transformation" from Tolerant's SBB to the new architecture (e.g. CIP, I/O-channel). After ensuring a sufficient in depth knowledge of the Eternity Series, project B may be carried out independently of A.

Projects C and D could be merged into one, if it is considered more appropriate to skip the intermediate step (a dual-PU RC9000 with the existing RPU/UPU concept) and head for the multi-PU based system at once.

5.1 Project A: Introduction of Existing System.

During this phase, the activities will be centered around analysis and training related to TOLERENT products. There is given no estimate of the costs involved.

5.2 Project B: RC8000/90 and New SBB Architecture.

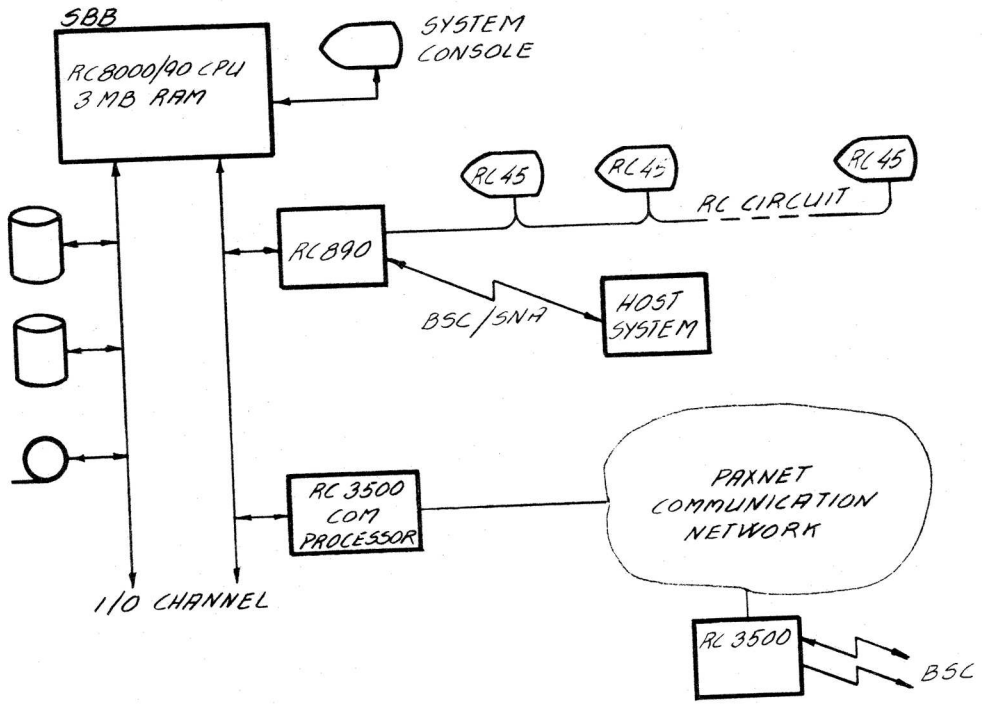
The individual system components and activities as identified above are listed below, with estimates of the mantime (in man years) involved.

COMPONENT/ACTIVITY	HW	SW	TOTAL	NOTES
SBB BUS,POWER,CRATE	2.0	-	2.0	
RC8000/90	1.5	0.5	2.0	(SW is uprg)
SSP	1.5	3.0	4.5	
MAIN MEMORY	2.0	-	2.0	
IOP	1.0	1.0	2.0	
GENERAL TPI INTERFACE	0.5	1.0	1.5	
DISC CONTROLLER	1.0	0.5	1.5	based on above
TAPE CONTROLLER	0.5	0.5	1.0	- - -
CONTROLLER FOR NCC	0.5	0.5	1.0	- - -
MULTIBUS ADAPTER	0.5	0.5	1.0	- - -
ETC	1.0	1.0	2.0	
RC8000 BASIS SW	-	1.5	1.5	

TOTAL FOR PROJECT B: 22.0 man year

Special requirements (equipment etc.) needed during this phase of the project are not specified.

Sample Configuration Resulting From Project B.



5.3 Project C: RC9000 RISC PU in New SBB.

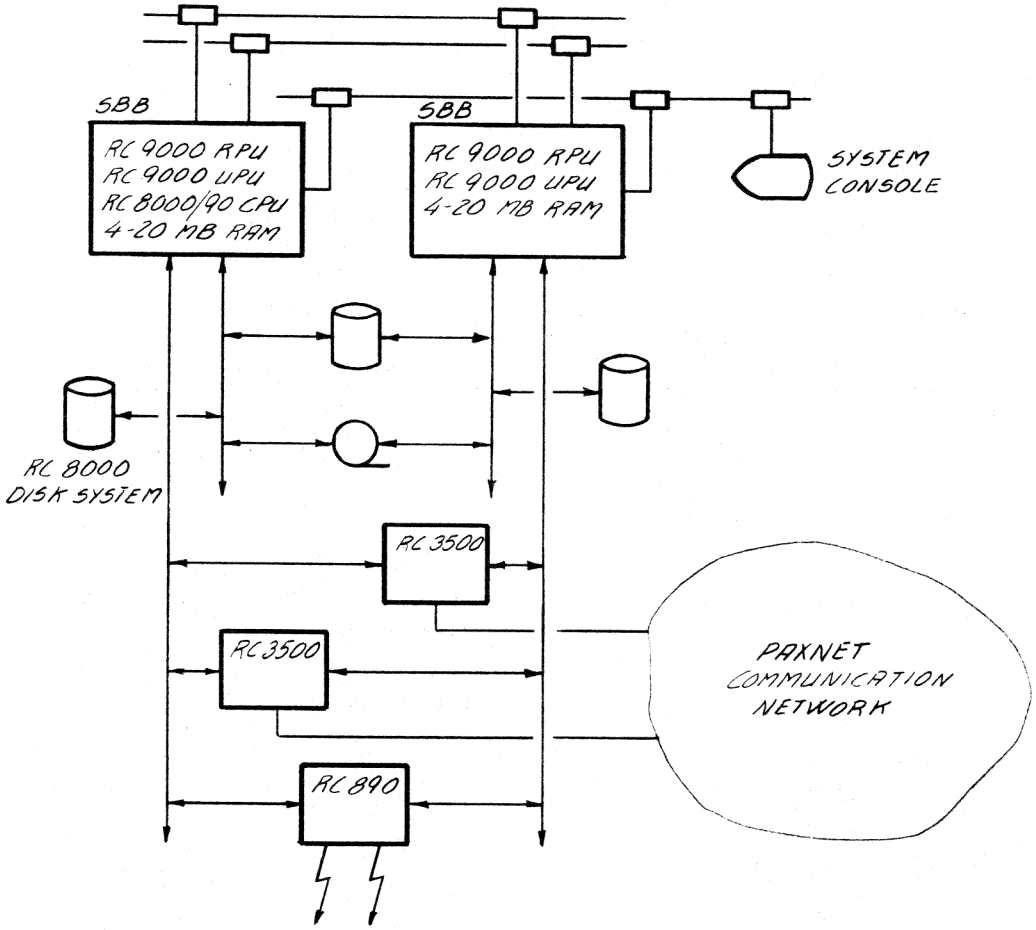
COMPONENT/ACTIVITY	HW	SW	TOTAL	NOTES
RC9000 RISC PU	1.5	-	1.5	
TX PORTATION	-	5.0	5.0	
COMPILER CODE GENERATION		7.0-17.0	7.0-17.0	
TX NETWORK INTERFACE		1.0	1.0	

TOTAL FOR PROJECT C : 14.5-24.5 man years

The interval given for compiler portation indicates the need for further analysis, based on the design of RC9000 PU and the compilers available.

The costs besides the mantime are dominated by the fees for obtaining the TX system and the compilers. Development systems will be needed for the SW activities that dominate this phase.

Sample Configuration Resulting From Project C:

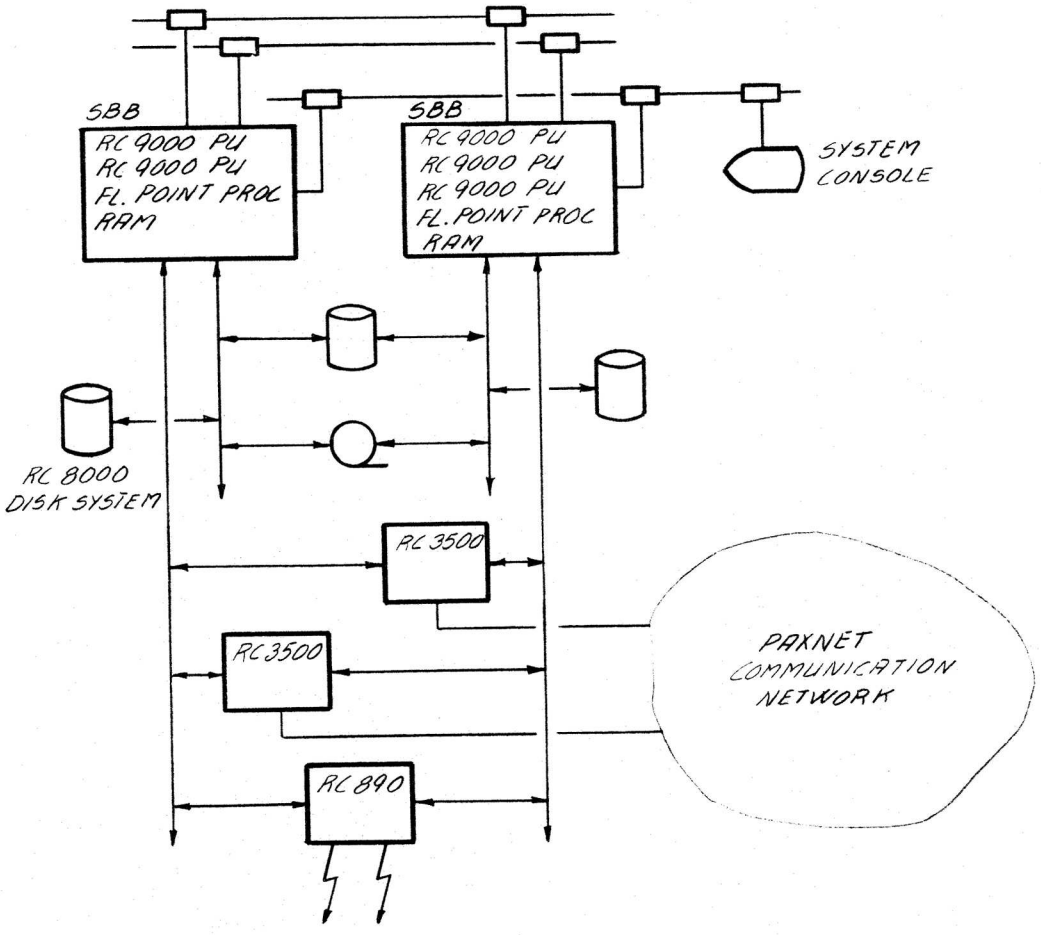


5.4 Project D: Extended RC9000 (Multiprocessor).

COMPONENT/ACTIVITY	HW	SW	TOTAL	NOTES
FPU/BCD COPROCESSOR	0.5	0.5	1.0	
TX MODIFICATIONS	-	?	?	see below
TOTAL FOR PROJECT D :			1.0 + ? manyears	

It is not possible to give an estimate of the efforts involved in creating a true multiprocessor-based version of TX at this point.

Sample Configuration Resulting From Project D:



6 Production Cost Estimates.

The following sections hold estimates of the production costs for the new hardware components, developed during the project.

6.1 SBB Bus, -Power, -Crate.

Mecanics	:	2.000 DKR
Backplane	:	4.500 DKR
Power Supply	:	7.000 DKR
Mounting, Test	:	500 DKR
TOTAL		14.000 DKR

6.2 RC8000/90 PU.

PCB (2)	:	5.000 DKR
Components	:	13.000 DKR
Mounting, Test	:	2.000 DKR
TOTAL		20.000 DKR

6.3 Main Memory Module.

DRAMs (170)	:	8.500 DKR
Controller	:	2.400 DKR
ECC	:	1.200 DKR
Other	:	2.000 DKR
PCB, Connectors	:	2.500 DKR
TOTAL		16.600 DKR

6.4 SSP.

ICs	:	7.500 DKR
PCB, Connectors	:	2.500 DKR
TOTAL		10.000 DKR

6.5 IOP.

ICs	:	5.500 DKR
PCB, Connectors	:	2.500 DKR
TOTAL		8.000 DKR

6.6 Disc Controller.

PCB	:	1.500 DKR
Components	:	4.500 DKR
Mounting, Test	:	1.000 DKR
TOTAL		7.000 DKR

6.7 Tape Controller.

PBC	:	1.500 DKR
Components	:	3.500 DKR
Mounting, Test	:	1.000 DKR
TOTAL		6.000 DKR

6.8 Network Connection Controller.

(only bus adapter component of RC3502)

Microprocessor	:	1.500 DKR
Other	:	2.000 DKR
PCB, Connectors	:	1.500 DKR
TOTAL		5.000 DKR

6.9 Multibus Adapter

(only bus adapter component of RC890)

Microprocessor	:	1.500 DKR
Other	:	2.000 DKR
PCB, Connectors	:	1.500 DKR
TOTAL		5.000 DKR

6.10 LAN-Controller.

PBC	:	2.500 DKR
Components	:	7.500 DKR
Mounting, Test	:	1.000 DKR
TOTAL		11.000 DKR

6.11 RC9000 PU.

ICs (approx. 300)	:	6.000 DKR
RAMs	:	7.000 DKR
MMU	:	5.000 DKR
PCB (2), Connectors	:	5.000 DKR
TOTAL		23.000 DKR

6.12 FPU/BCD Coprocessor.

ICs (approx. 100)	:	2.000 DKR
Floating point ALU	:	4.000 DKR
Floating point MPU	:	4.000 DKR
PCB, Connectors	:	2.500 DKR
TOTAL		10.500 DKR