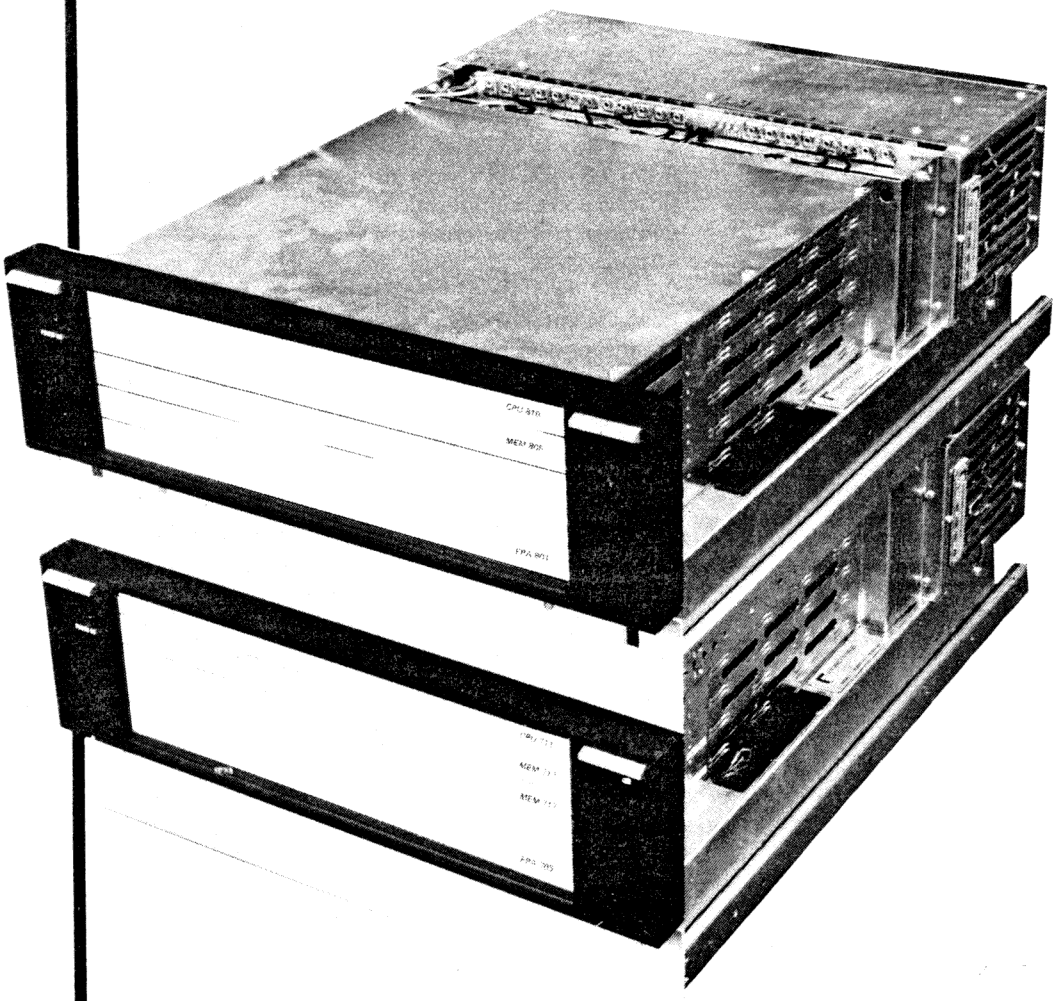
RC 8000/35S

Central Unit System

- 24-BIT WORD LENGTH
- LSI TECHNOLOGY
- MICROPROGRAMMED
- CONNECTED TO UNIFIED BUS
- MULTIPLY & DIVIDE
- FLOATING POINT ARITHMETIC
- REAL TIME CLOCK
- SEMICONDUCTOR MEMORY



GENERAL

The RC 8000/35-S Central Unit System provides a medium size general purpose processor based on 24-bit words. The 64 basic instructions can work on 4 registers, and each instruction has a 12-bit displacement and 16 address modifications including relative, indexed and indirect addressing modes. A program protection system combined with a real time clock and a powerful interrupt system makes RC 8000/35-S well suited for multiprogramming. The main memory size ranges from 64 K words to 512 K words.

The unified asynchronous RC 8000 System Bus connects the central unit, the main memory and the peripheral controllers. All peripherals are connected to the bus by means of intelligent controllers which perform routine tasks pertaining to input/output operation thereby increasing the computing power of the central unit. The bus is an independent system unit and no connected unit has special status.

The RC 8000/35-S System includes one input/output device controller, based on an RC 3600 minicomputer, by which a variety of peripheral devices can be connected. The system provides an option for additional device controllers.

CHARACTERISTICS

The combination of LSI technology and microprogrammed inplementation of most CPU functions has made RC 8000/35-S a very compact yet powerful central unit system. The main memory access width is 1 word consisting of 24 data bits and a 6-bit correction code. Single bit error correction and double bit error detection are incoorporated for increased storage reliability.

Integer arithmetic uses 24-bit-words, floating point and extended range integer arithmetic use 48-bit double words. 12-bit halfwords are directly addressable by special halfword instructions. Typical instruction execution time is 3 to 20 μsec. Data manipulation is aided by halfword operations and word comparison functions. Logical operations permit setting and testing of single bits. An escape facility causes programmed action on preselected instructions. Program protection is obtained by means of memory limit registers and privileged instructions executable only in monitor mode. Dynamic program relocation is possible through use of modified base register technique.

Transmission speed between system and input/output device controller is 600 Kbytes per second.

SPECIFICATIONS

CENTRAL PROCESSOR

Instruction exec. time:	From 2.8 μsec. for simple instructions to 46 μsec. for floating point multiplication
Interrupt system:	8 internal and 8 external levels
Interrupt response:	10 μsec.
Real time clock:	0.1 msec. resolution, 4 sec./24 hours stability
Standard features:	Power Monitor, 6-bit correction code, Autoload via disc channel or device controller, Interrupt generating, 25.6 msec. interval timer

MEIN MEMORY

Type:	Semiconductor (dynamic 16 K MOS RAM)
Word length:	24 data bits, 6-bit correction code
Capacity:	65,536 (64 K) to 524,288 (512 K) words
Speed:	Access 600 nsec., cycle time 700 nsec.

ELECTRICAL AND ENVIRONMENTAL

Power requirements:	220 V, 50 Hz, 900 W
Ambient temperature:	10 - 27 ^{o}C (50 - 80 ^{o}F)
Relative humidity:	20 - 80%, non condensing
Heat dissipation:	780 kcal/h (3070 BTU/h)
Mounting:	Any 19" cabinet

DIMENSIONS

Height:	444 mm (17.5 inches)
Weight:	55 kg (121 lbs)