DANSK DATA ELEKTRONIK

ID-7030 CPU MODULE

for the

SPC-1 MICROCOMPUTER SYSTEM

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1. DESCRIPTION.

The ID-7030 CPU module is the CPU module in the SPC-1 microcomputer. The CPU module drives the address bus and generates all the necessary control signals. The ID-7030 module works with the other modules in the ID-7000 series. In the SPC-1 it normally works with:

ID-7037:	32 K Dynamic RAM with bank switching.
ID-7038:	Refresh for the ID-7037 dynamic RAM.
ID-7045:	Floppy disk controller.
ID-7009:	DMA controller.
ID-7003:	Interrupt priority module.
ID-7012:	4-port communication module.
ID-7018:	General purpose I/O module.

The ID-7030 CPU module contains an 8085A microprocessor and the following peripherial units:

Communication port 0.
Communication port 1.
Arithmetic processing Unit.
Boot loader PROM.
Baud rate generator.

2. MICROPROCESSOR 8085A.

The 8085A is the key component on the CPU module. It drives the address bus and generates all the necessary control signals.

The SOD output signal from the 8085A is used in a special way which is described later.

The odd interrupt levels 5.5, 6.5, and 7.5 are used by the communication ports and the timer on the CPU module while the odd interrupt level TRAP is used as a DEBUG CALL.

3. COMMUNICATION INTERFACES.

The CPU module contains two programmable communication interfaces type 8251A. In the following text these are referred to as port 0 and port 1.

In the SPC-1 microcomputer port 0 is normally used for the CRT terminal and port 1 is used for the printer.

The interface to each port consists of:

RxD: Receiver data.
TxD: Transmitter data.
CTS: Clear to send.
GND: Ground.

The baud rate can be strapped individually for port 0 and port 1. The interfaces to port 0 and port 1 are found in two 16 pin DIP sockets at the top of the module; see figure 2.

Addresses and interrupt levels for port 0 and port 1:

	BASE ADDRESS	INTERRUPT LEVEL
PORT 0	E2	6.5
PORT 1	E4	5.5

PORT 0 generates an interrupt request when TxRDY or RxRDY is true. PORT 1 generates an interrupt request when TxRDY or RxRDY is true and PORT 1 has CLEAR to SEND.

4. Arithmetic Processing Unit AM 9511.

The arithmetic processing unit, APU, is connected to the 8085A in order to facillitate calculations with floating point numbers and to facillitate calculations of mathematical functions

The base address of the APU is E8. The APU is not connected to the interrupt system.

The reset pin of the APU is connected to SOD inverted. SOD is an output pin from 8085 A.

5. Boot Loader PROM.

The CPU module contains an UV erasable PROM type 2708.
The boot loader PROM is enabled when ADR(15:10)=0 and SOD=0.
When the boot loader PROM is enabled the external memory modules are disabled.

During power up the reset signal is generated. This signal resets the CPU, port 0, port 1, and all the modules connected to the SPC-1 bus.

After power up SOD equals zero, and the CPU starts reading its first instruction in address zero. As SOD equals zero the instruction is read from the boot loader PROM. Notice that the APU is reset when SOD=0, so the program in the boot loader PROM cannot use the APU.

It is the responsibility of the boot loader program to reset the APU properly as described in the data sheet and to disable the PROM when the boot loader program has finished.

6. BAUD RATE GENERATOR AND TIMER.

The CPU module contains a 16 MHz crystal controlled oscillator The oscillator drives the 16 MHz clock lines in the SPC-1 bus. The signal form the oscillator is divided down to 2 MHz which drives the 8085A, the communication ports, and the APU. The signal is divided further down to give the various baud rates for port 0 and port 1. The baud rate is selected by means of a strap at the top af the CPU module.

The strapping possibilities are shown in figure 1. The baud rates are as shown in the figure when the communication ports are programmed to divide by 16.

The baud rate counters is divided further down to be used as a timer interrupt. The timer interrupt is connected to the odd interrupt level 7.5. The possibilities for the timer interrupt are shown in figure 1.

7. DEBUG CALL.

The odd interrupt level TRAP can be connected to a switch through a debouncing flip flop. When the switch is activated a TRAP interrupt is generated. The CPU stacks its instruction counter and fetches its next intruction from location 24 hex. This location should contain a jump to the debug program. Notice that the TRAP interrupt cannot be disabled so the only reason why a debug call cannot be performed is that the jump intruction in location 24 hex has been destroyed.

Baud Rate Position

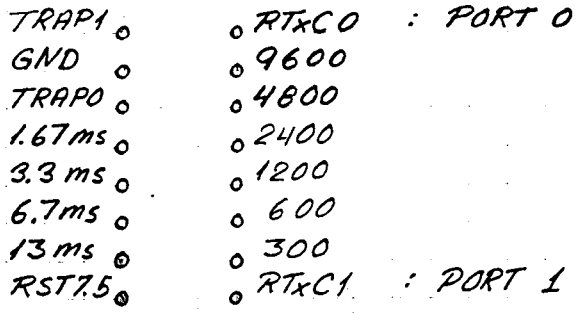


Figure 1

Communication Port Interface

PORT 0 : Position 34. PORT 1 : Position 35.

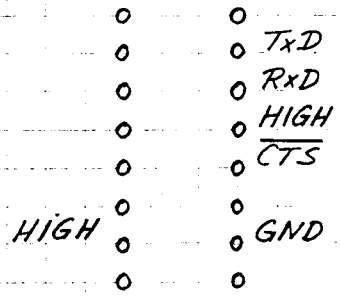
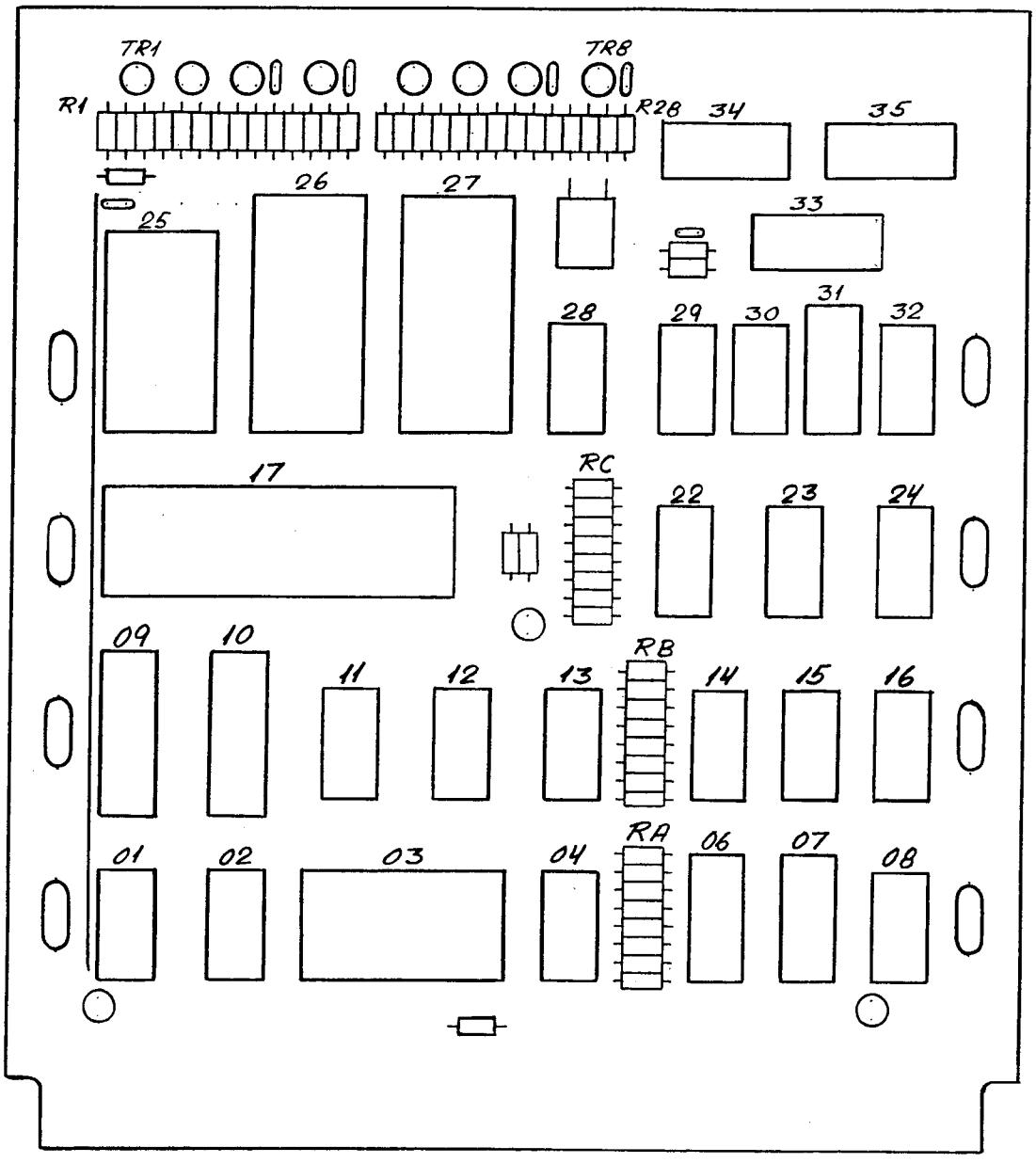
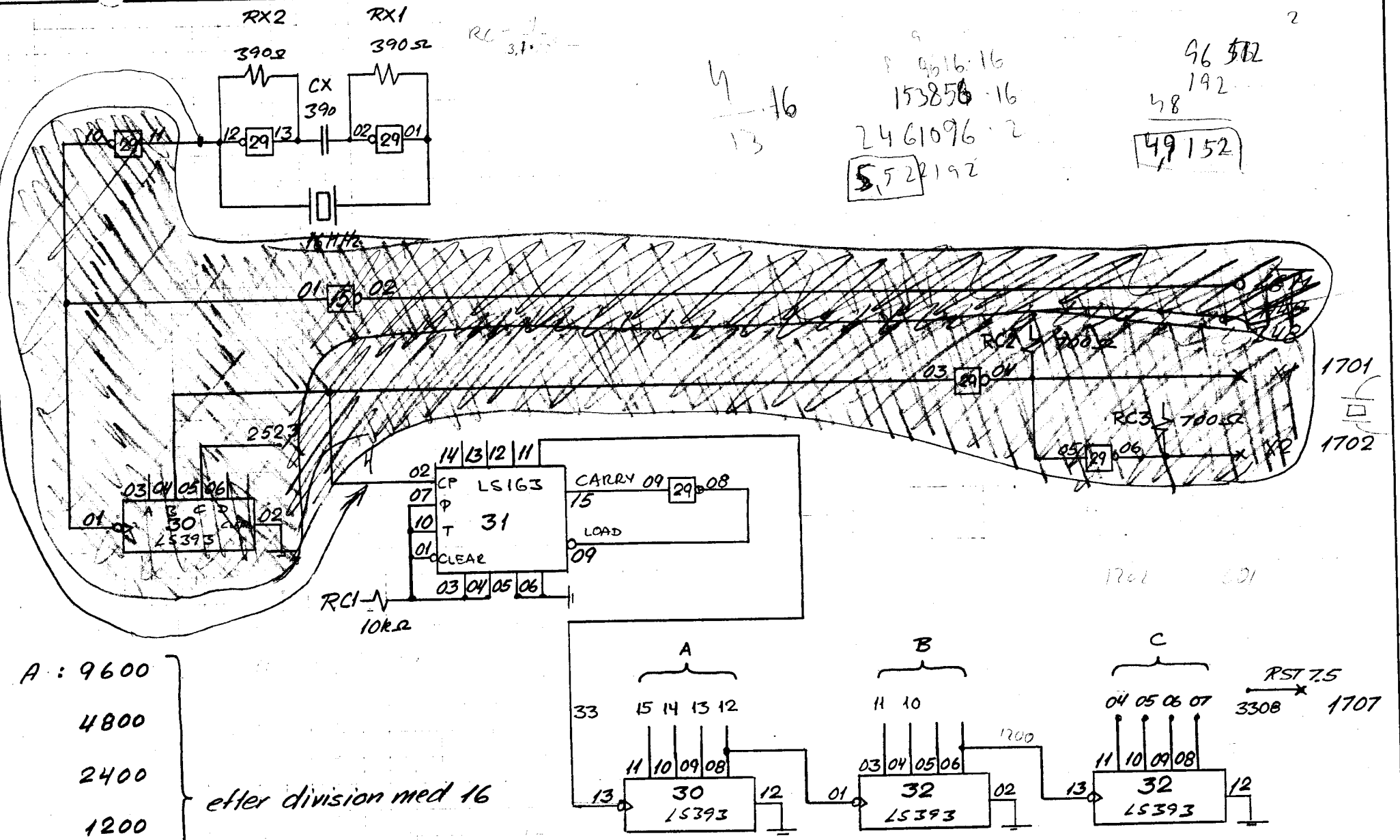


Figure 2

ID-7030


TR1
TR8
R1
R28
34
35
25
26
27
33
28
29
30
31
32
17
RC
22
23
24
09
10
11
12
13
RB
14
15
16
01
02
03
04
RA
06
07
08



A : 9600
4800
2400
1200
B : 600
300

efter division med 16

C : 1.67 ms
: 3.3 ms
: 6.7 ms
: 13 ms

Wokgenerator

dansk data elektronik aps

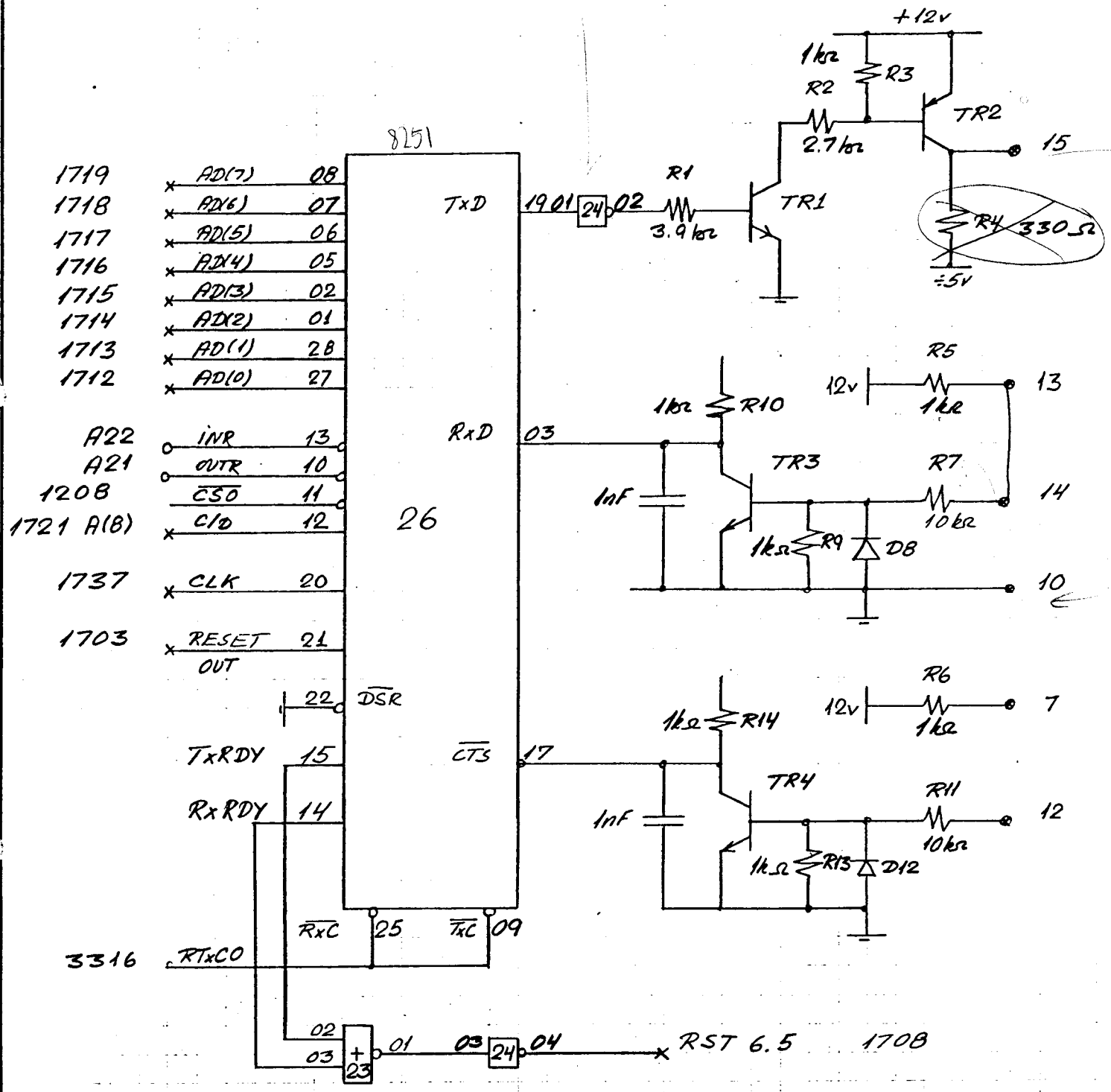
Initialer/dato KEN 15/12

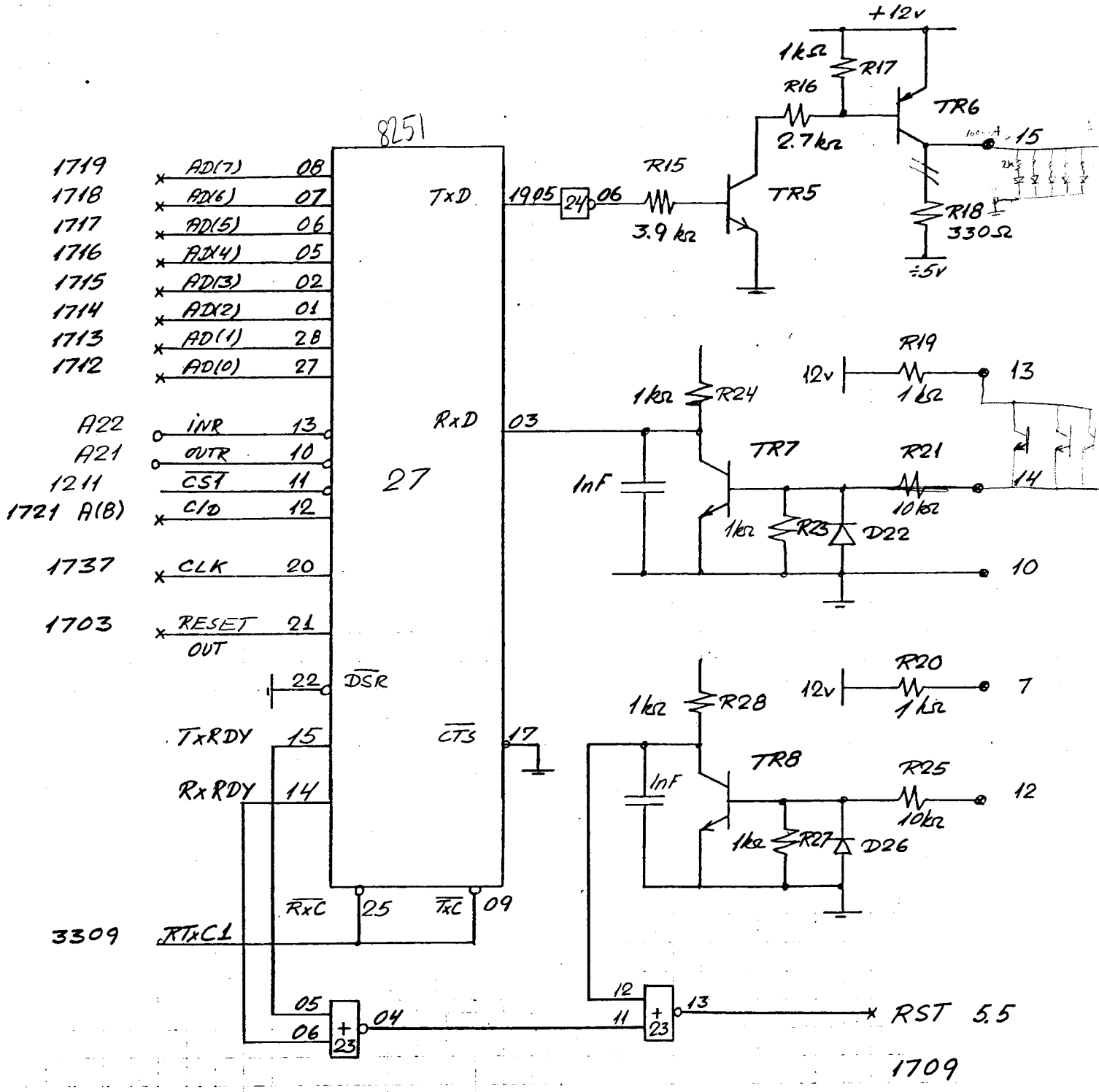
Revideret

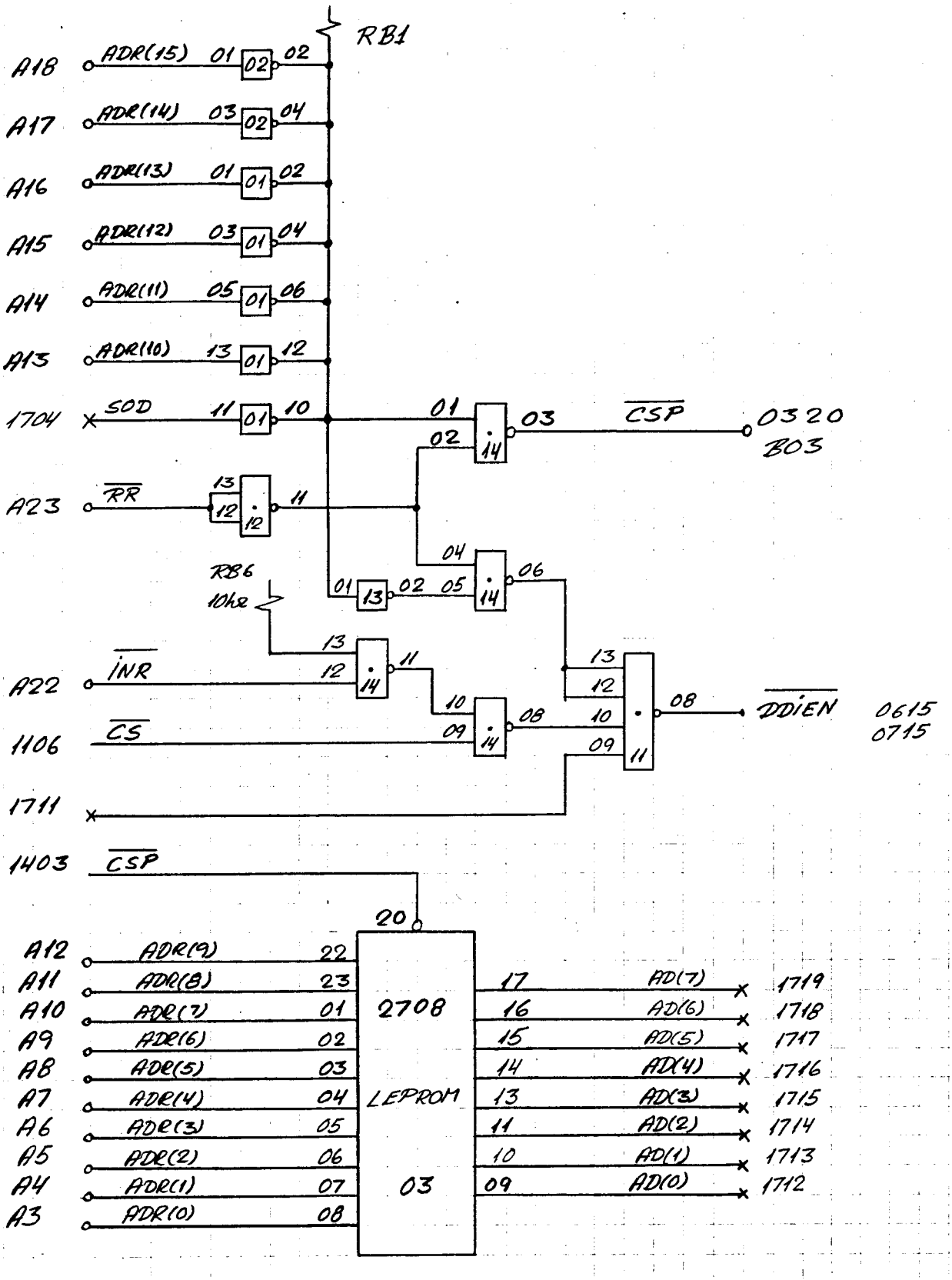
Side 1

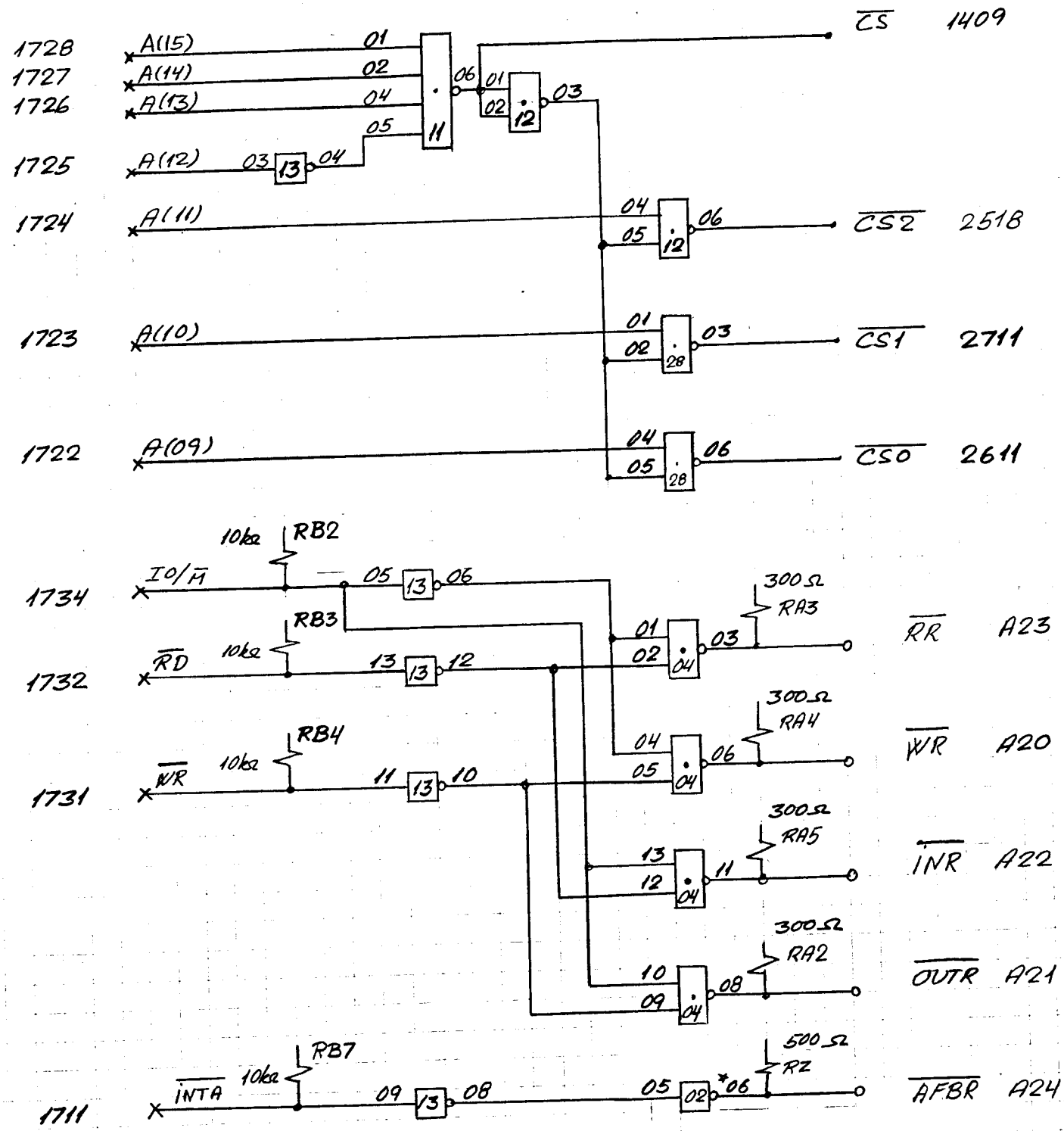
Projekt 7030

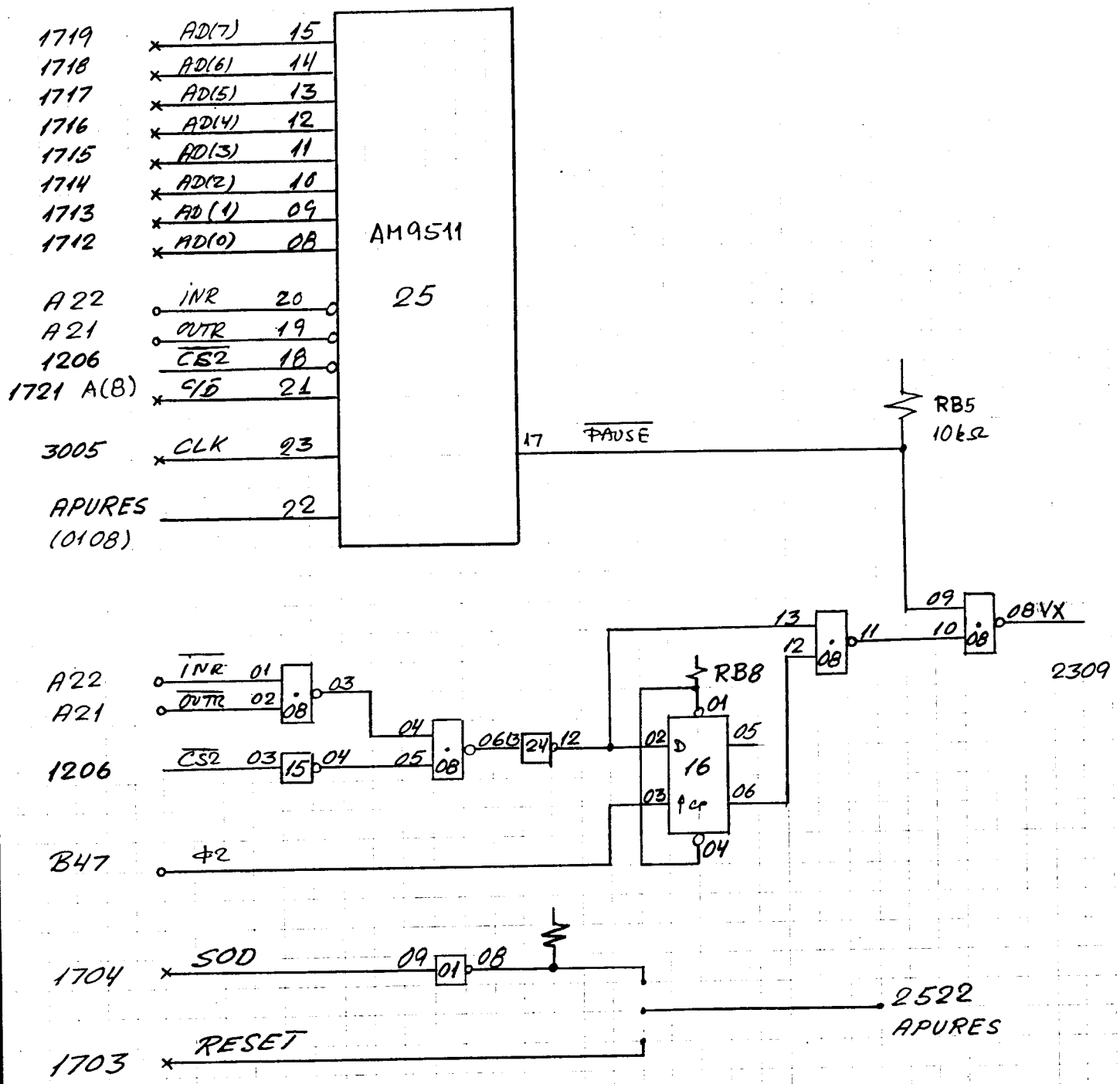
henrik schouw reklame a-s · Form. 4505

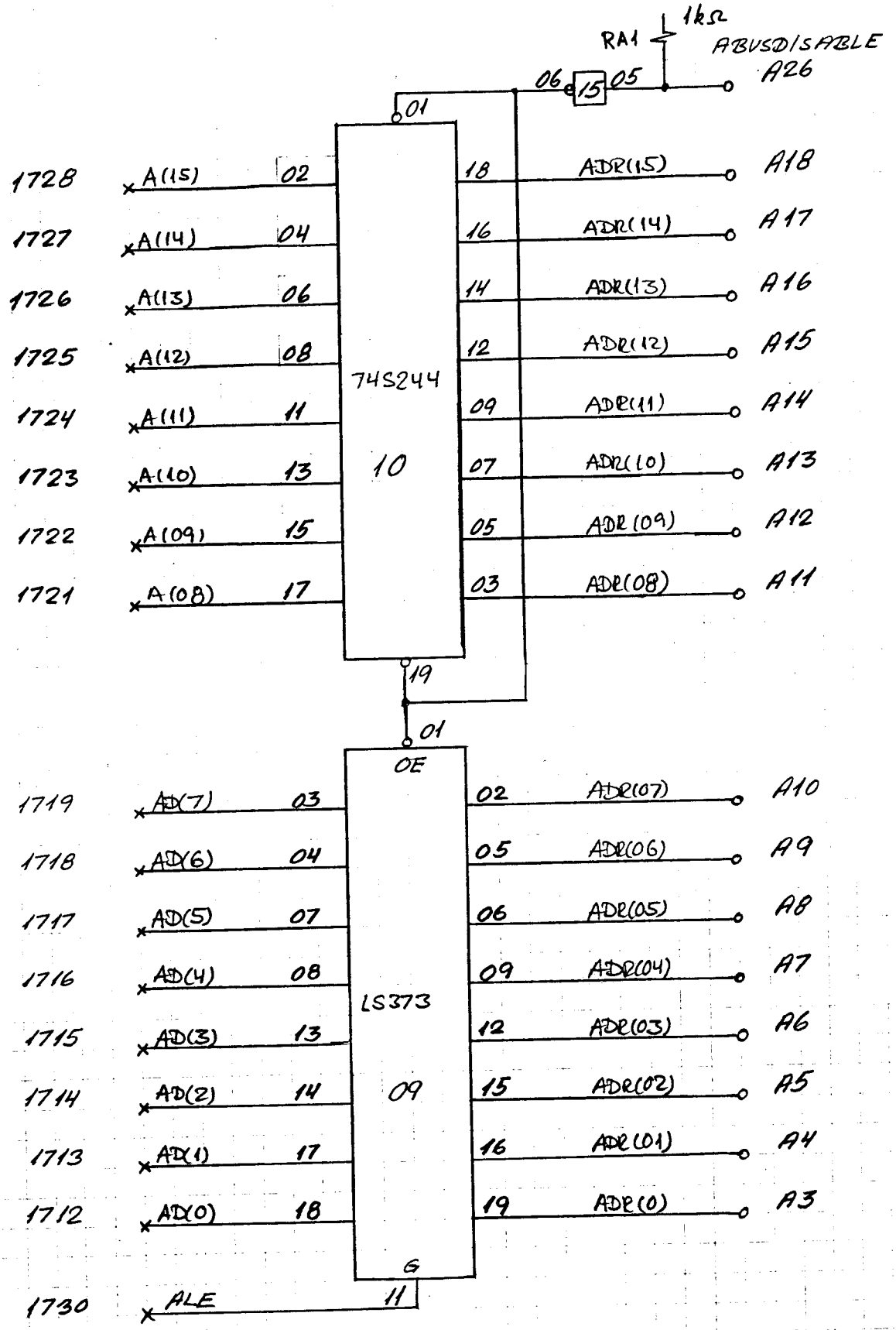

8251
1719 AD(7) 08
1718 AD(6) 07
1717 AD(5) 06
1716 AD(4) 05
1715 AD(3) 02
1714 AD(2) 01
1713 AD(1) 28
1712 AD(0) 27
A22 INR 13
A21 OUTR 10
1208 CS0 11
1721 A(8) C/D 12
1737 CLK 20
1703 RESET OUT 21
22 DSR
TxRDY 15
RxRDY 14
RxC 25
TxC 09
3316 RTxCO
TxD
RxD 03
CTS 17
26
19 01 24 02
+12v
1kΩ R3
R2 2.7kΩ
TR2
15
R1 3.9kΩ
TR1
R4 330Ω
-5v
R5
12v 1kΩ 13
1kΩ R10
TR3
R7 10kΩ 14
1nF
1kΩ R9
D8
10
R6
12v 1kΩ 7
1kΩ R14
TR4
R11 10kΩ 12
1nF
1kΩ R13
D12
02 03 23 01 03 24 04
RST 6.5
1708

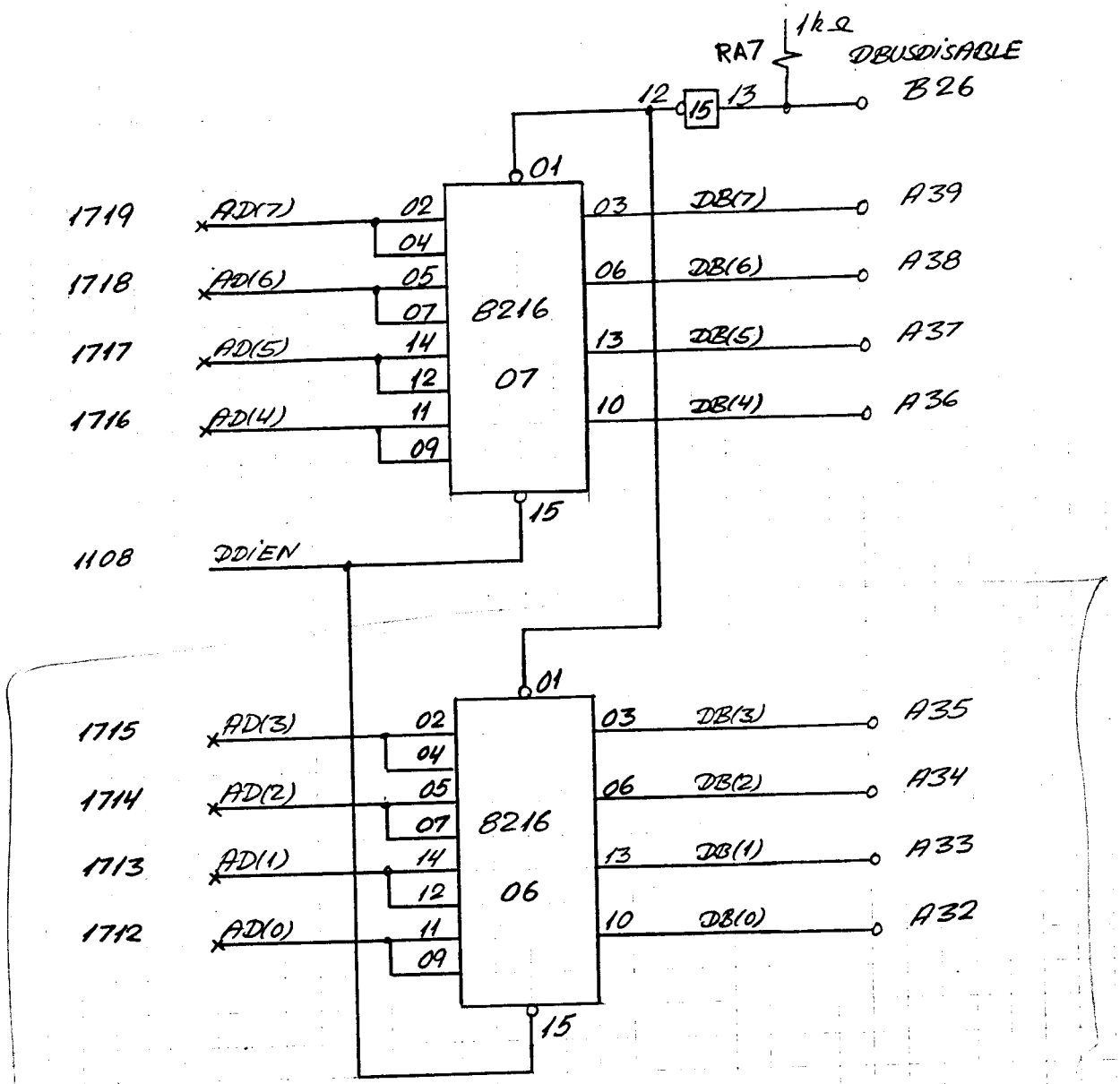

8251
27
1719 AD(7) 08
1718 AD(6) 07
1717 AD(5) 06
1716 AD(4) 05
1715 AD(3) 02
1714 AD(2) 01
1713 AD(1) 28
1712 AD(0) 27
A22 INR 13
A21 OUTR 10
1211 CS1 11
1721 A(8) C/D 12
1737 CLK 20
1703 RESET OUT 21
22 DSR
TxRDY 15
RxRDY 14
3309 RTxC1
TxD
RxD
CTS
RxC 25
TxC 09
1905 24 06
03
17
05 06 +23 04
12 11 +23 13
RST 5.5
1709
+12v
1kΩ R17
R16 2.7kΩ
TR6
15
R15 3.9kΩ
TR5
R18 330Ω
÷5v
R19 1kΩ
13
1kΩ R24
TR7
R21 10kΩ
14
1nF
1kΩ R23 D22
10
R20 1kΩ
7
1kΩ R28
TR8
R25 10kΩ
12
1nF
1kΩ R27 D26

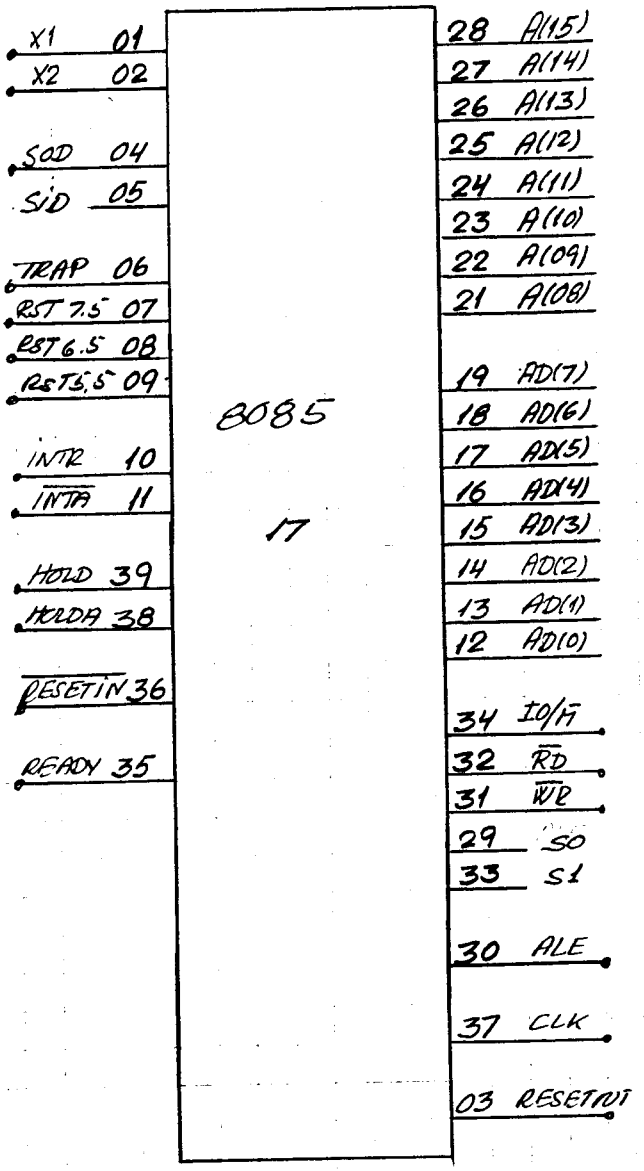

RB1
A18
ADR(15)
A17
ADR(14)
A16
ADR(13)
A15
ADR(12)
A14
ADR(11)
A13
ADR(10)
1704
SOD
A23
RR
RB6
10hz
A22
INR
1106
CS
1711
1403
CSP
0320
B03
DDIEN
0615
0715
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
ADR(9)
ADR(8)
ADR(7)
ADR(6)
ADR(5)
ADR(4)
ADR(3)
ADR(2)
ADR(1)
ADR(0)
2708
LEPROM
03
AD(7)
AD(6)
AD(5)
AD(4)
AD(3)
AD(2)
AD(1)
AD(0)
1719
1718
1717
1716
1715
1714
1713
1712

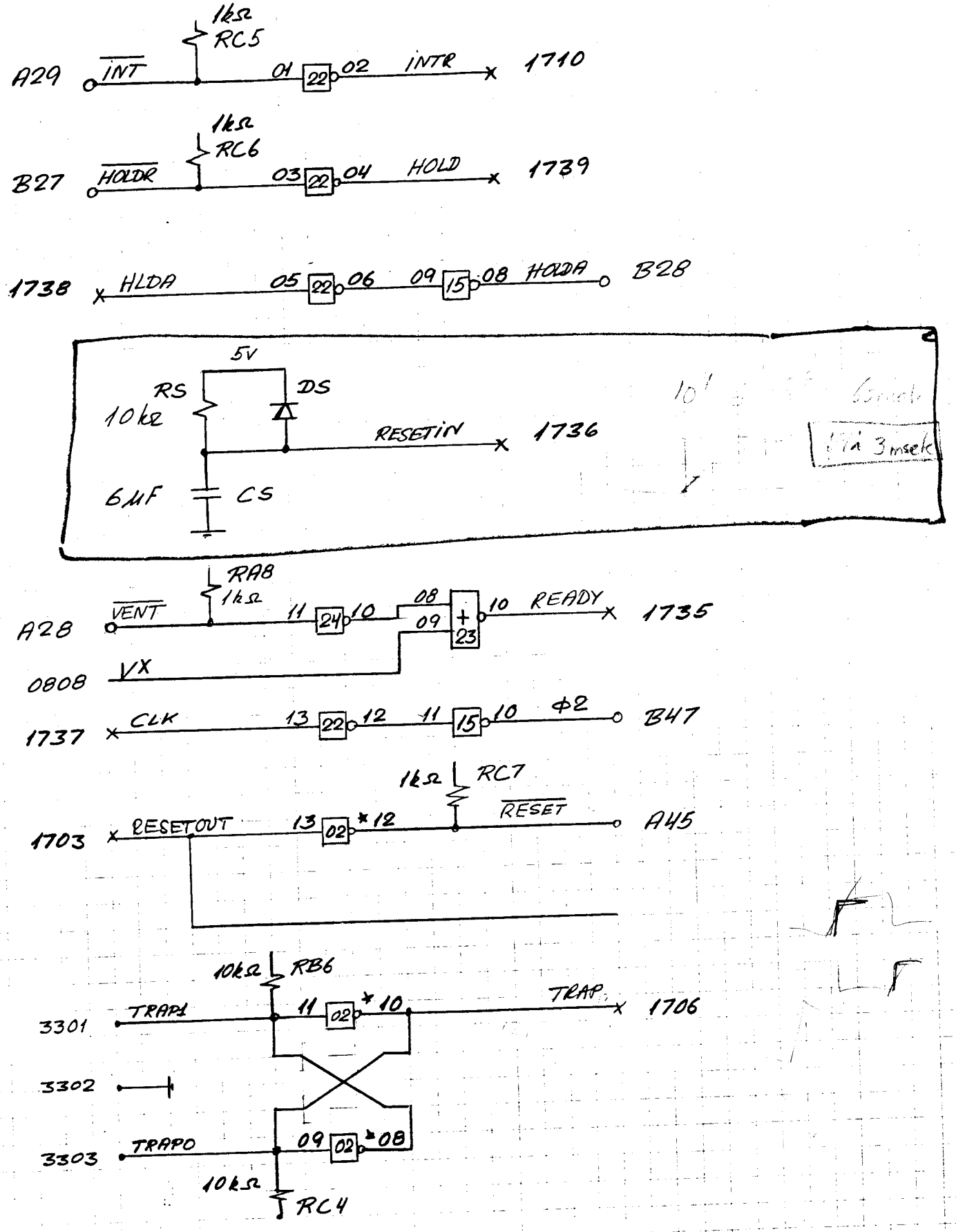

1728 A(15)
1727 A(14)
1726 A(13)
1725 A(12)
1724 A(11)
1723 A(10)
1722 A(09)
CS 1409
CS2 2518
CS1 2711
CS0 2611
10kΩ RB2
RB3
RB4
RB7
I0/M
RD
WR
INTA
1734
1732
1731
1711
300Ω RA3
300Ω RA4
300Ω RA5
300Ω RA2
500Ω RZ
RR A23
WR A20
INR A22
OUTR A21
AFBR A24


1719 AD(7) 15
1718 AD(6) 14
1717 AD(5) 13
1716 AD(4) 12
1715 AD(3) 11
1714 AD(2) 10
1713 AD(1) 09
1712 AD(0) 08
AM9511
25
A22 INR 20
A21 OUTR 19
1206 CS2 18
1721 A(8) C/D 21
3005 CLK 23
APURES (0108) 22
17 PAUSE
RB5 10kΩ
09
08 VX
13
12
11
10
2309
A22 INR 01
A21 OUTR 02
03
04
1206 CS2 03
15
04
05
06
24
12
RB8
01
02
05
16
03
06
04
B47 Φ2
1704 SOD 09
01
08
2522 APURES
1703 RESET


1kΩ
RA1
ABUSDISABLE
A26
06
15
05
01
1728
A(15)
02
18
ADR(15)
A18
1727
A(14)
04
16
ADR(14)
A17
1726
A(13)
06
14
ADR(13)
A16
1725
A(12)
08
12
ADR(12)
A15
74S244
1724
A(11)
11
09
ADR(11)
A14
10
1723
A(10)
13
07
ADR(10)
A13
1722
A(09)
15
05
ADR(09)
A12
1721
A(08)
17
03
ADR(08)
A11
19
01
OE
1719
AD(7)
03
02
ADR(07)
A10
1718
AD(6)
04
05
ADR(06)
A9
1717
AD(5)
07
06
ADR(05)
A8
1716
AD(4)
08
09
ADR(04)
A7
LS373
1715
AD(3)
13
12
ADR(03)
A6
1714
AD(2)
14
09
15
ADR(02)
A5
1713
AD(1)
17
16
ADR(01)
A4
1712
AD(0)
18
19
ADR(0)
A3
G
1730
ALE
11


1k Ω
RA7
DBUSDISABLE
B26
12
15
13
01
1719
AD(7)
02
04
03
DB(7)
A39
1718
AD(6)
05
07
06
DB(6)
A38
8216
07
1717
AD(5)
14
12
13
DB(5)
A37
1716
AD(4)
11
09
10
DB(4)
A36
15
1108
DDIEN
01
1715
AD(3)
02
04
03
DB(3)
A35
1714
AD(2)
05
07
06
DB(2)
A34
8216
06
1713
AD(1)
14
12
13
DB(1)
A33
1712
AD(0)
11
09
10
DB(0)
A32
15


X1 01
X2 02
SOD 04
SID 05
TRAP 06
RST 7.5 07
RST 6.5 08
RST 5.5 09
INTR 10
INTA 11
HOLD 39
HLDA 38
RESETIN 36
READY 35
8085
A
28 A(15)
27 A(14)
26 A(13)
25 A(12)
24 A(11)
23 A(10)
22 A(09)
21 A(08)
19 AD(7)
18 AD(6)
17 AD(5)
16 AD(4)
15 AD(3)
14 AD(2)
13 AD(1)
12 AD(0)
34 IO/M
32 RD
31 WR
29 SO
33 S1
30 ALE
37 CLK
03 RESETOUT


1kΩ
RC5
A29
INT
01
22
02
INTR
1710
1kΩ
RC6
B27
HOLDR
03
22
04
HOLD
1739
1738
HLDA
05
22
06
09
15
08
HOLDA
B28
5V
RS
DS
10kΩ
RESETIN
1736
6μF
CS
RA8
1kΩ
A28
VENT
11
24
10
08
09
+
23
10
READY
1735
0808
VX
1737
CLK
13
22
12
11
15
10
Φ2
B47
1kΩ
RC7
1703
RESETOUT
13
02
*12
RESET
A45
10kΩ
RB6
3301
TRAP1
11
02
*10
TRAP
1706
3302
3303
TRAP0
09
02
*08
10kΩ
RC4