DANSK DATA ELEKTRONIK

ID-7037D 48K DYNAMIC RAM MODULE

for the

SPC-1 MICROPROCESSOR SYSTEM

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Author: Knud Arne Nielsen

1. INTRODUCTION.

The ID-7037D Dynamic RAM Module contains 48K bytes of dynamic memory. The memory module is desigend to be used in single or multi user MIKADOS systems but the module can be used in in other memory configurations as well.

The module can be strapped to use two different implementations of bank switching. The ID-7037D is designed to be controlled by the ID-8538 Refresh Module.

2. BANK SWITCHING.

In order to expand the addressing capability of 8085A the memory module is equipped with bank switching. In a bank switched memory system a bank can be enabled or disabled. When a bank is enabled it occupies space in the address space of the computer and can be accessed by the CPU and various DMA units. When a bank is disabled it does not occupy space in the address space and it cannot be accessed. The module can be strapped to use one of two different implementations of bank switching which are described in the following text.

2.1. BANK SWITCHING IMPLEMENTATION 1.

When the strap between pos. 9 and pos. 10 is placed in the upper position bank switching implementation 1 is used.

A memory bank is identified by a bank control address which is FC or FD and a bit number between 0 and 7. In this way it is possible to differentiate between 16 memory banks. A memory bank with control addres AA and bit number n is enabled when the CPU executes an OUT AA instruction and the bit number n in the data word is a one. The bank is disabled if bit number N is zero.

The control address and the bit number is called the bank address and should not be confused with the memory starting address.

2.2. BANK SWITCHING IMPLEMENTATION 2.

When the strap between pos. 9 and pos. 10 is placed in the lower position bank switching implementation 2 is used.

The address bus is expanded with four extra address lines from ADR(15:0) to to ADR(19:0). A memory bank is enabled when ADR(19:16) matches the bank address of the memory bank.

The extra address lines ADR(19:16) are driven by the ID-8537 Memory Register Module. This module contains one four bit register for the CPU and one four bit register for each of the seven possible DMA channels. When the CPU accesses memory the register corresponding to the CPU drives ADR(19:16). When one of the DMA channels accesses memory its corresponding register drives the extra address lines. In this way the CPU can execute a program in one memory bank while the DMA channels are transferring data to or from other memory banks. The Memory Register Module is loaded by the CPU. See the manual for this module.

3. The SWITCH REGISTER.

In order to use the module in different memory configurations the module is equipped with a seven bits switch register S(7:1). The most significant bit of the switch register S(7) is closest to the edge connector of the module. A bit in the switch register is a logic one when the switch is on that is when the switch is closed.

The switch register is divided into an upper four bit part S(4:1) which determines the bank address of the module and a lower three bit part S(7:5) which determines the function af the module.

If a memory module has an eight bit switch installed instead of the usual seven bit switch S(8) is not used.

3.1. THE BANK ADDRESS.

When bank switching implementation 1 is used S(4) determines wheather the bank control address is FC or FD. When S(4) is off the bank control address is FC and when S(4) is on the bank control address is FD. S(3:1) selects the bit number in the data word. When S(3:1) is off bit zero is selected. When S(3:1) is on bit seven is selected.

When bank switching implementation 2 is used S(4:1) is compared to address ADR(19:16). If there is a match the bank is enabled.

3.2. THE FUNCTION.

S(7:5) determines how the module is configured. The different functions are listed in the table below. The functions can be divided into three different groups. These are:

System memory with MIKADOS bank; FCT= 0.
Bank switched memory; FCT= 3, 4, 7.
Non bank switched memory; FCT= 1, 2, 5, 6.

By choosing the proper function it is possible to place a debugger program in a non bank switced memory with starting address C000.

A multi user MIKADOS system uses one module with FCT=0 for the MIKADOS operating system and one module with FCT=3 for each user in the system. When a debugger is placed in this system the function of the user modules is changed from FCT=3 to FCT=4.

NOTICE: All bank switched memory is disabled after POWER UP RESET when bank switching inplementation 1 is used.

When bank switching implementation 2 is used the content of the registers on ID-8537 is unknown after POWER UP.

FUNCTION	M0	M1	M2
0:	F0	B1	B2
1:	F0	F1	F2
2:	F3	OUT	OUT
3:	B3	B1	B2
4:	OUT	B1	B2
5:	F3	F1	F2
6:	F0	OUT	OUT
7:	OUT	B1	B2

EXPLANATION:

F0: Non bank switched memory. Starting address 0000.
F1: Non bank switched memory. Starting address 4000.
F2: Non bank switched memory. Starting address 8000.
F3: Non bank switched memory. Starting address C000.

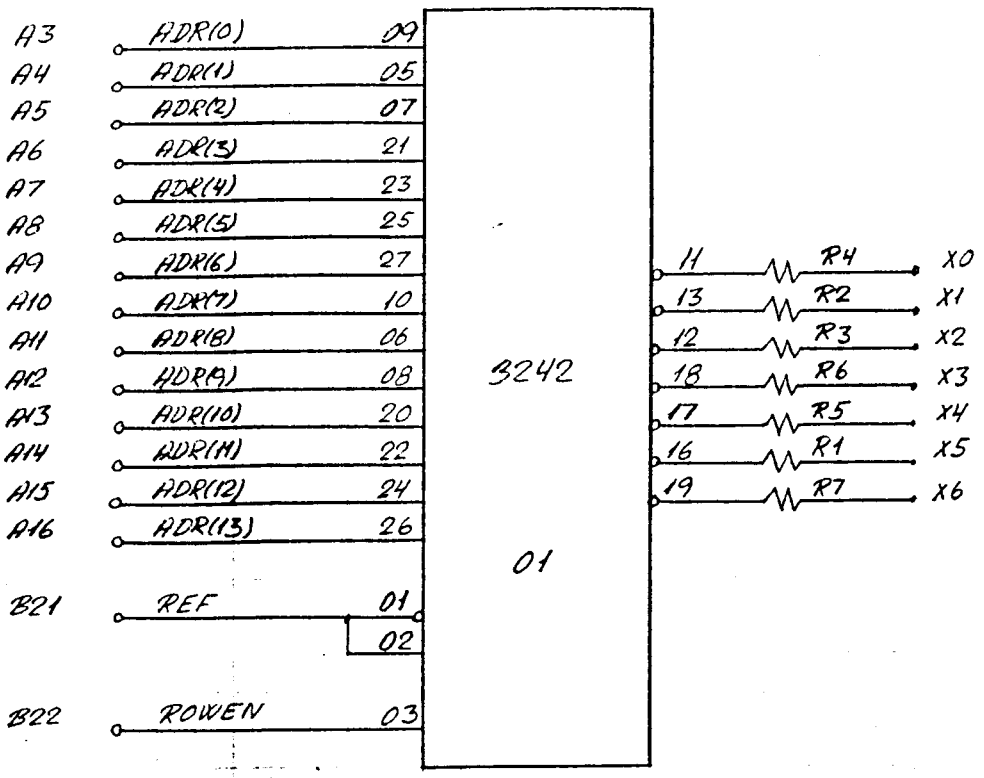
B0: Bank switched memory. Starting address 0000.
B1: Bank switched memory. Starting address 4000.
B2: Bank switched memory. Starting address 8000.
B3: Bank switched memory. Starting address C000.

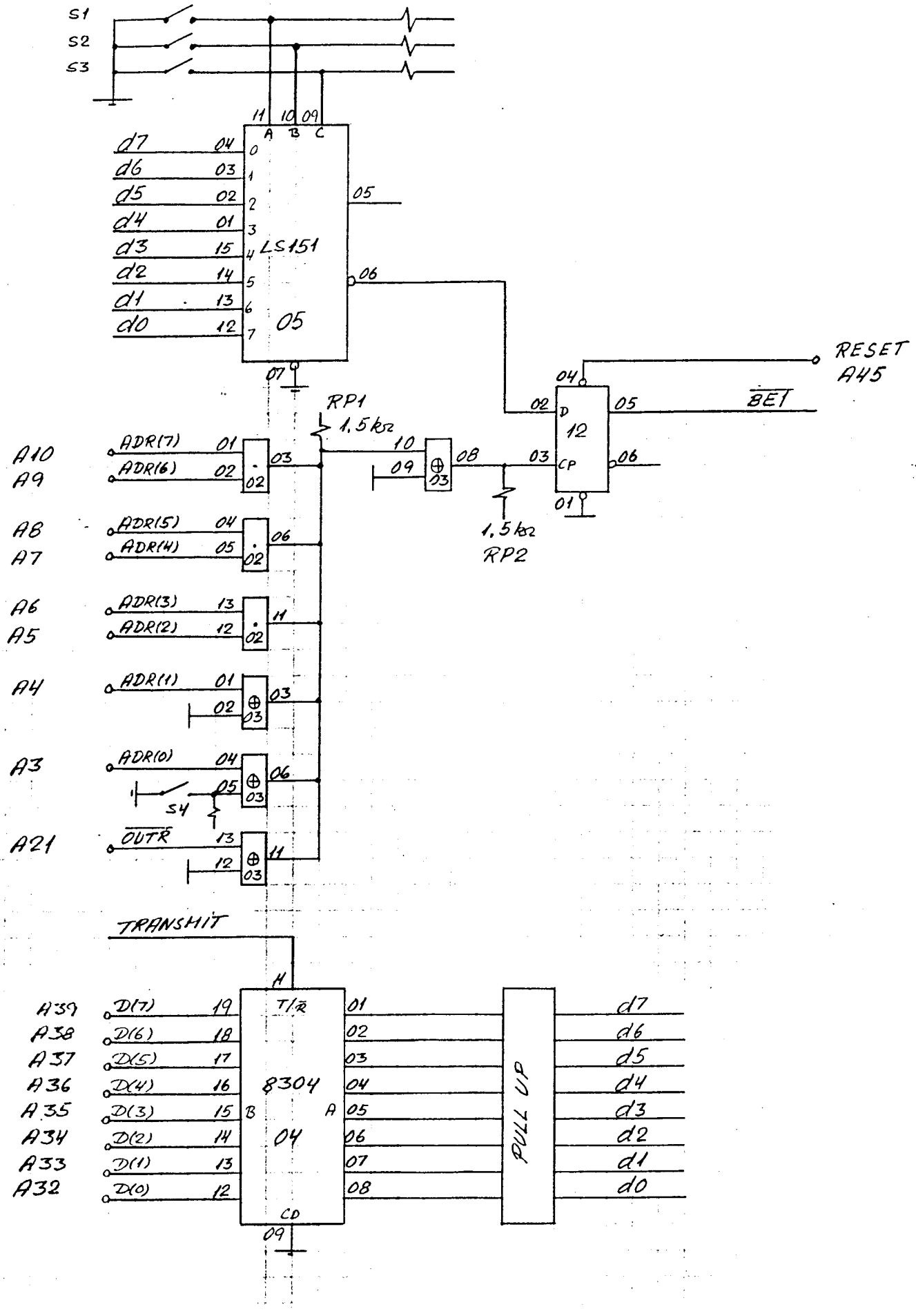
M0: 16K dynamic memory placed in the upper row on the module.
M1: 16K dynamic memory placed in the middle row on the module.
M2: 16K dynamic memory placed in the lower row on the module.

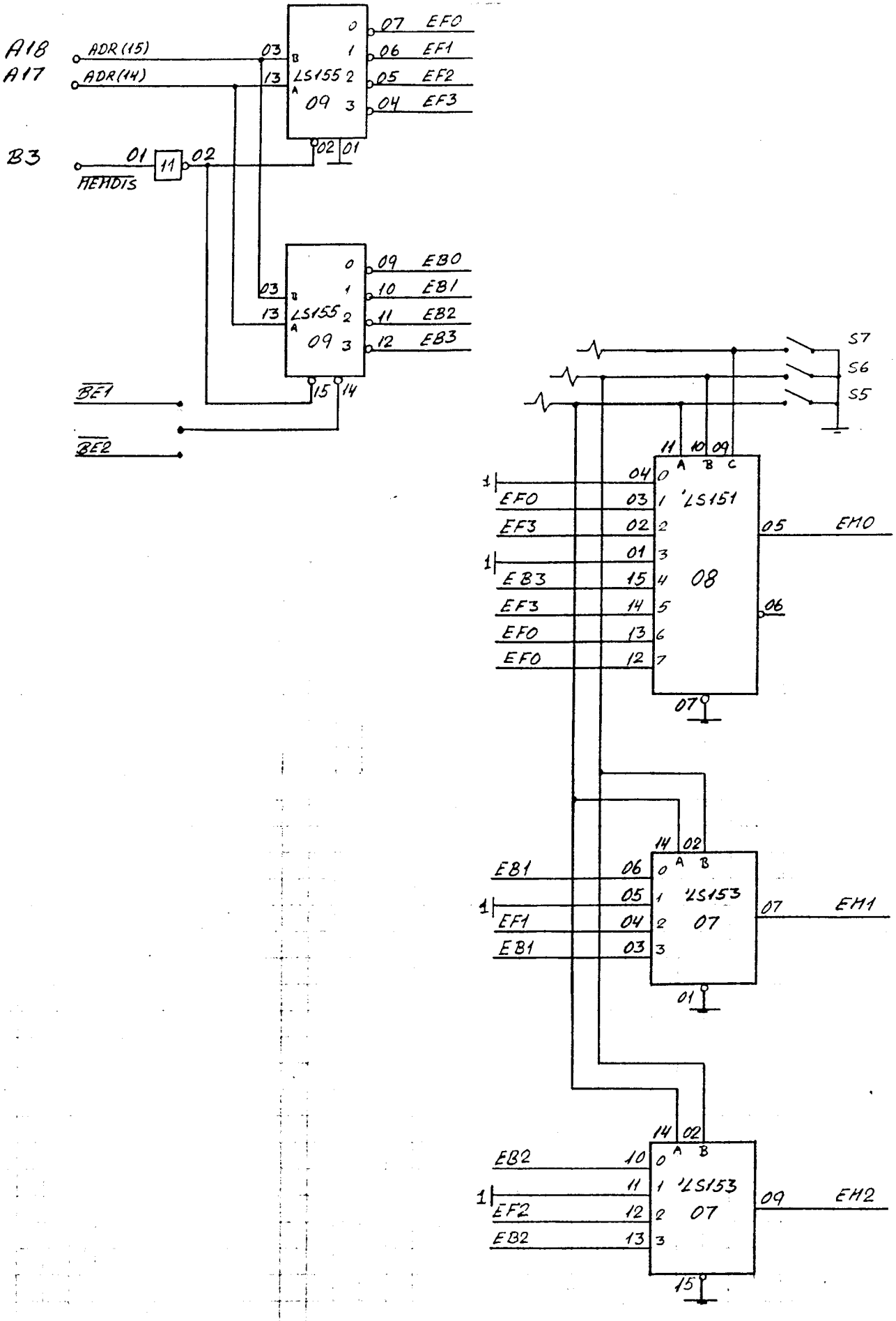
OUT: Disabled 16K memory bank.

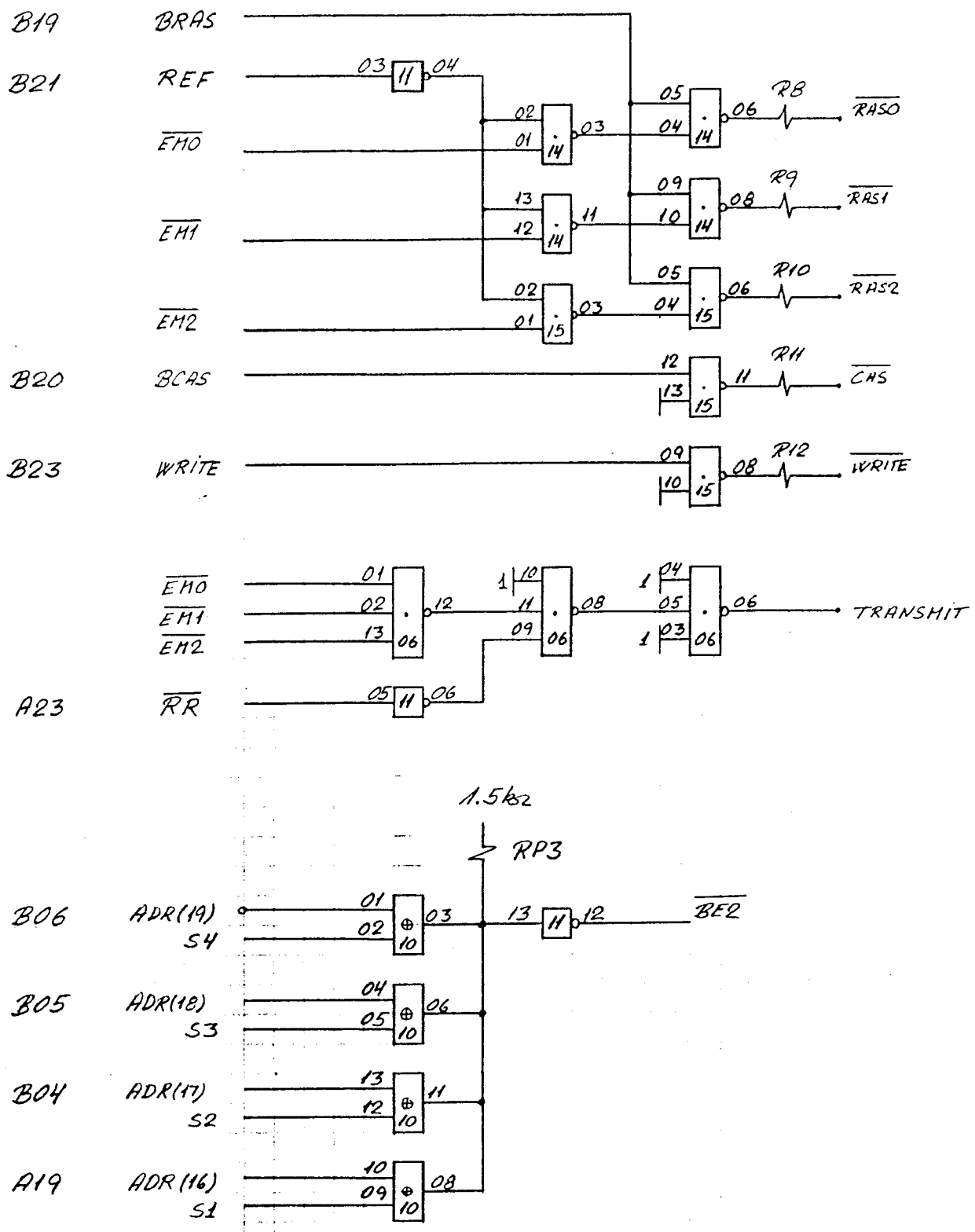
dansk data elektronik aps

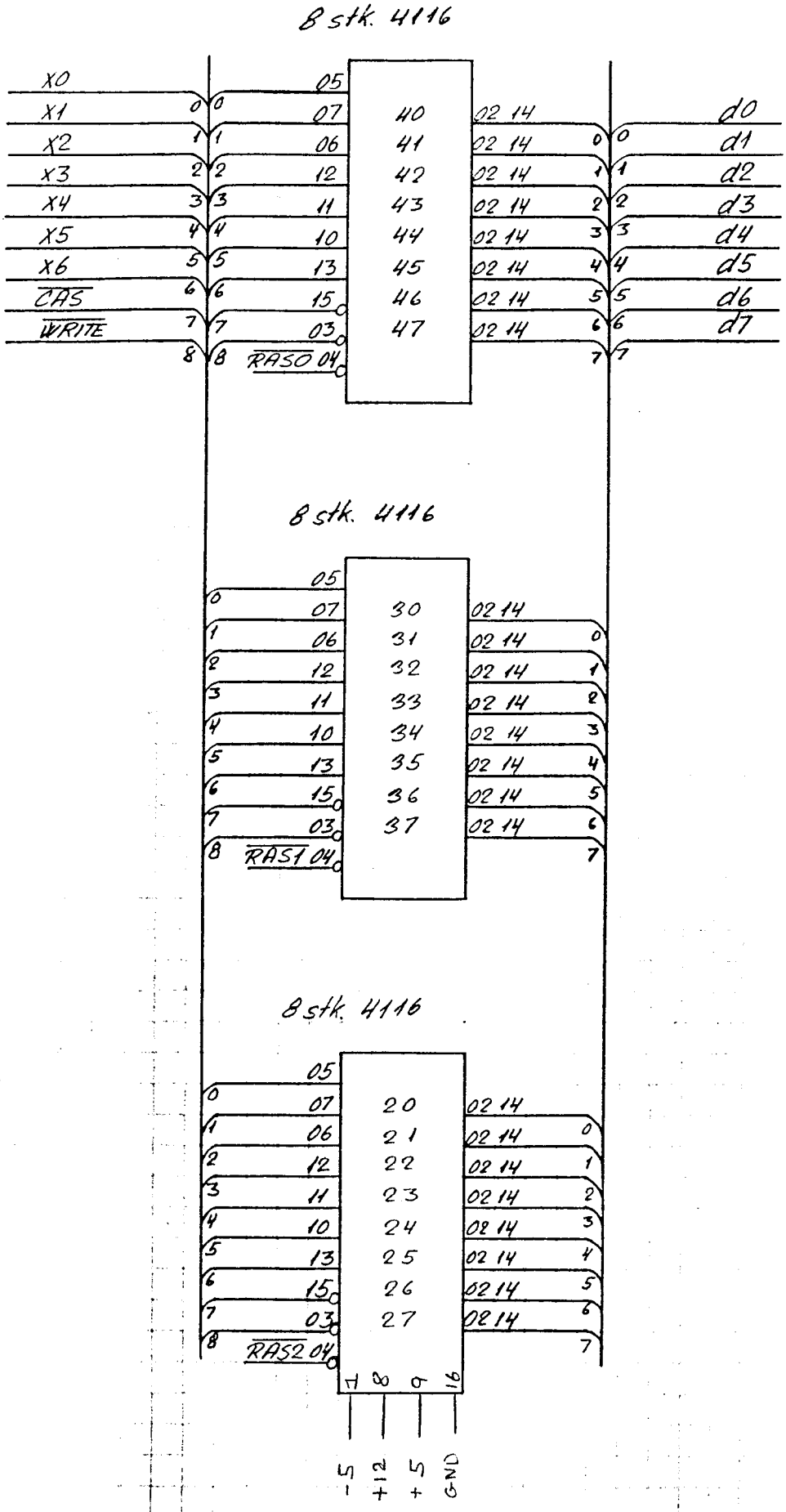
	Initialer/dato	Side
7037D	KHN 810107	1
	Revideret	Projekt




S1
S2
S3
11 10 09
A B C
d7 04
d6 03
d5 02
d4 01
d3 15
d2 14
d1 13
d0 12
0 1 2 3 4 5 6 7
LS151
05
05
06
07
RESET
A45
04
02 D
05
BET
12
03 CP
06
01
RP1
1.5 kΩ
10
09
08
03
1.5 kΩ
RP2
A10
A9
ADR(7) 01
ADR(6) 02
03
02
A8
A7
ADR(5) 04
ADR(4) 05
06
02
A6
A5
ADR(3) 13
ADR(2) 12
11
02
A4
ADR(1) 01
02
03
03
A3
ADR(0) 04
05
06
03
S4
A21
OUTR 13
12
11
03
TRANSMIT
H
A39
A38
A37
A36
A35
A34
A33
A32
D(7) 19
D(6) 18
D(5) 17
D(4) 16
D(3) 15
D(2) 14
D(1) 13
D(0) 12
T/R
8304
04
B
A
CD
09
01
02
03
04
05
06
07
08
PULL UP
d7
d6
d5
d4
d3
d2
d1
d0

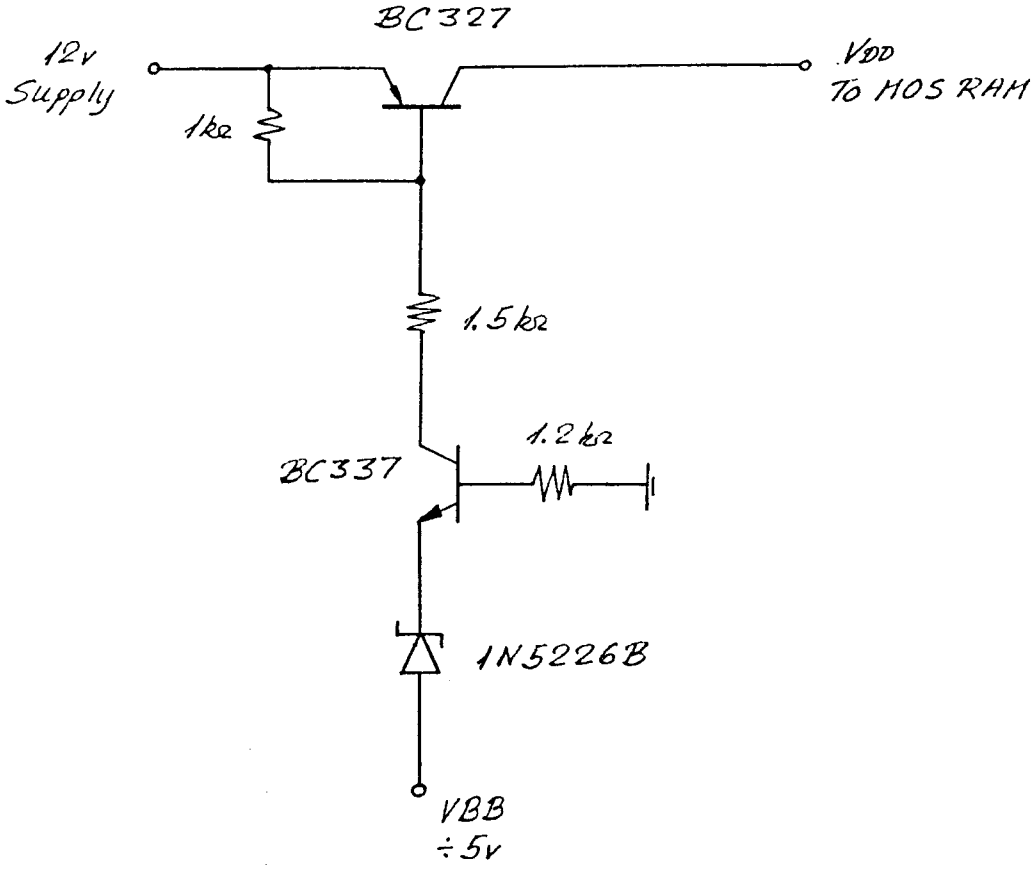

A18
A17
ADR(15)
ADR(14)
LS155
09
07 EF0
06 EF1
05 EF2
04 EF3
B3
01
11
02
MEMDIS
09 EB0
10 EB1
11 EB2
12 EB3
BE1
BE2
S7
S6
S5
'LS151
08
05 EM0
06
EF0
EF3
EB3
EF3
EF0
EF0
'LS153
07
07 EM1
EB1
EF1
EB1
'LS153
07
09 EM2
EB2
EF2
EB2


B19
BRAS
B21
REF
EM0
EM1
EM2
B20
BCAS
B23
WRITE
R8
R9
R10
R11
R12
RAS0
RAS1
RAS2
CAS
WRITE
EM0
EM1
EM2
A23
RR
TRANSMIT
1.5kΩ
RP3
B06
ADR(19)
S4
B05
ADR(18)
S3
B04
ADR(17)
S2
A19
ADR(16)
S1
BE2


8 stk. 4116
X0
X1
X2
X3
X4
X5
X6
CAS
WRITE
RAS0
40
41
42
43
44
45
46
47
d0
d1
d2
d3
d4
d5
d6
d7
8 stk. 4116
RAS1
30
31
32
33
34
35
36
37
8 stk. 4116
RAS2
20
21
22
23
24
25
26
27
-5
+12
+5
GND

Protective Circuit 7037D

Initialer/dato	Side
KAN 22/5-81	6
Revideret	Projekt
	7037D



MOTOROLA

MCM4116B

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

MOS

(N-CHANNEL)

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4116B is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

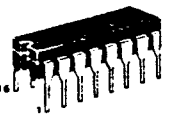
By multiplexing row and column address inputs, the MCM4116B requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116B is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

The MCM4116B incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

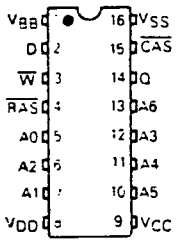
- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 X 1 Organization
- ±10% Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation — 463 mW Active, 20 mW Standby (Max)
- Fast Access Time Options 150 ns — MCM4116BP-15, BC-15
  200 ns — MCM4116BP-20, BC-20
  250 ns — MCM4116BP-25, BC-25
  300 ns — MCM4116BP-30, BC-30
- Easy Upgrade from 16-Pin 4K RAMs

P SUFFIX
PLASTIC PACKAGE
CASE 648



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



PIN NAMES	
A0-A6	Address Inputs
CAS	Column Address Strobe
D	Data In
Q	Data Out
RAS	Row Address Strobe
W	Read/Write Input
VBB	Power (−5 V)
VCC	Power (+5 V)
VDD	Power (+12 V)
VSS	Ground

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.5 to +20	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DS9806/10-79