REGNECENTRALEN
Danish Institute of Computing Machinery

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Process Unit to GIER.

Foreword.

As a result of cooperation between Instituttet for Reguleringsteknik, The Technical Highschool of Norway (NTH), Trondheim, and Regnecentralen, The Danish Institute of Computing Machinery, there has in Copenhagen been developed a process unit to GIER with regard to research within the field of process control at NTH. The unit exists at present only as a prototype on one of the GIER-computers in Trondheim. The process unit represents in its present form an extension of GIER's input/output system to comprise also a number of in- and outputs for analogue signals as well as digital information including an interrupt system for syncronizing GIER with real-time phenomenons. (Regnecentralen plans within the nearest months a further development of this unit, so that off-line running with registrating and processing of data can be realized).

Introduction.

Process GIER comprises a standard GIER supplemented with the following parts,

an interrupt unit
a data channel
an external process unit

The interrupt system which is built inside the GIER cabinet comprises 12 interrupt channels with associating masking register. An interrupt which passes the mask will cause a jump from the running program to a sub-routine which will take care of the interrupt. After this the running program will continue as if nothing had happened. The interrupt system is administrated by means of two new orders, PC and GC, place in masking register C and store masking register C (op. no. 48 and 47). Concurrent interrupt calls will be processed in a fixed built-in order.

The data channel also built inside the GIER-cabinet is used for transferring of data between GIER and the external process unit.
The data channel is designed for transport of one word at a time (42 bit parallel transport) at a transfer time of about 5 microsec. Transfer of data between GIER and the outer process unit takes place in 10 or 20-bits groups by means of two new orders, IL and US, read-in and write-out (op-no. 44 and 45). All transfers will be carried out to and from the R-register in GIER.

The external process unit comprises the following parts,

30 inputs for analogue signals including multiplex and common A/D converter with buffer register

12 inputs for digital signals (9 10-bits and 3 20-bits registers)

15 outputs for analogue signals with individual buffer registers and D/A converters

6 outputs for digital information (6 10-bits registers).

All in- and outputs have been wired to cable plugs and further to a plugboard.

The interrupt system and the data channel are also used for connection between GIER and the magnetic tape stations via 4096 words core memory buffer store and is available in a nearly completed form.

The Interrupt Unit.

A) Programming Technique in connection with the interrupt unit.

When a demand arises for interrupt inside an external unit it will send a signal via one of the 12 interrupt channels to GIER. This will happen at a completely random instance in GIER's running program, as the process in the external unit will run quite freely in relation to GIER (a measuring point, an output on a mechanical curve plotter, or the like).

In case the channel is not blocked by the mask the signal has a consequence that GIER jumbs to a program corresponding to the number of the interrupt channel after having finished the running orders. This program, which has been programmed and placed in the core memory of the user, represents the answer to the mentioned interrupt and may for instance result in the fact that one number is read from one of the inputs for analogue signals, i.e. a measuring point is registrated. After having finished this response program GIER will continue the main program from the step where breaking-in happened without any influence on the main program, besides that it has been delayed by the time that was spent to finish up the response program. If GIER is stopped at a time where an interrupt signal occurs the signal causes under certain circumstances that GIER starts running and in this way responds to the interrupt.

Before the response program to an interrupt is started GIER will somplete a special microprogram, mode 5, which results in the following administrative operations,

1) The program sequence counter is stored in the counting part of the cell no. a (the number can be chosen quite free of the users by means of a plugboard).

2) The number of the interrupt channel concerned is stored in the adress part of cell no. a.

3) The program sequence counter rl is put equal to a+1.

4) All further interrupts are blocked by means of a flip-flop M which is set to 1. This blocking is released during execution of the order which follows immediately after a PC oder, place in mask register C.

All further functions performed in connection with the registers IR and C will be described in section B.

After this GIER will start the running of the response program beginning with execution of the order in cell a+1. If the last performed order is a left half-word order it will start with a right half-word in cell a+1, otherwise with left half-word in cell a+1.

No matter from which channel the interrupt occurs the following administrative operations must be performed as introduction to the response program,

1) the contents of all registers are stcred

2) a new mask is put up by means of operation PC (or VY if the HP-switch has caused the interrupt)

3) a jumb is performed to a response program for the interrupt concerned.

By the end of the response program a series of standard operations have to be done, viz.,

1) the contents of all registers must be re-established

2) a new mask must be put up

3) a jumb return to the order which would have been performed if the program had not been interrupted.

These operations are performed by means of IAS sub-routine for administration of interrupts. This routine will also give a correct administration if GIER has not yet finished one interrupt response program when a new interrupt signal breaks in at the same or another channel. The number of interrupt signals which in this way may arrive inside each other is only limited by the core memory place you will reserve to the necessary storing cells.

There exist papertapes containing the IAS with possibility for 1/2/3/4 and 5 interrupts respectively inside each other. In any case you can read-in the one of these 5 paper tapes you want to use for the present purpose. Another parameter for IAS is the adress of the cell a in the core memory. The adress can be chosen by a manual plugging at one of the printed circuits in GIER. The address chosen in this way must of course correspond to the address of cell a, with which IAS is working. The correspondance is procured as follows,

During reading-in of one of the 5 paper tapes containing IAS the typewriter in GIER is chosen as input channel and you have to type in

' a = the adress of cell a 1

hv-orders are placed in the right half cell of cells 15-31 of the administration sequence "IAS". In the counting parts of these cells the user must place the start adresses of his interrupt responses by means of pt-orders as the interrupt channel 0 corresponds to cell 15 in the sequence and channel 6 to cell 21.

The interrupt response programs must end with the orders,

pc -1, hv 22a

The mask in the C-register is blocked to prevent interrupts from breaking in during re-establishment of the registers. This will happen in IAS's cell 22 and the following cells. All registers are re-established and the used storing cells are made free.

Finally a jumb is performed from the re-establishment sub-routine to the order which would have been performed if the interrupt in question had not occured.

B) Description of the Logic in the Interrupt System.

The interrupt system can be divided into two parts comprising HP-switch and its masking and the interrupt channels 0-11 and there masking respectively.

The mutual priority of the two systems is such that in case of coinciding calls from these the response program for the HP-switch will be run at first. The two systems are by the way in principle built-up in the same way, the HP-switch calls being registrated in a flip-flop HP and masked by means of by-register pos 3 (masking means a blocking of the present interrupt) while the interrupt channel calls are registrated in a series of flip-flops IR pos. 0-11 and masked by means of C-register pos. 0-7.

This must be understood that way that an interrupt - when it occurs - is registrated in the HP-flip-flop if it came from the HP-switch or in the IR-register pos. N if the interrupt occurred in interrupt-channel N.

If the channel in question is blocked by masking nothing will happen until the blocking is released by means of a PC or VY order which opens for the channel concerned. After that an eventually registrated interrupt will be able to break in if another mask M, mutual to both systems, is open i.e. equal to 0. M is set to 1 when an interrupt breaks through no matter from which channel it happens. In this way there is blocked for further interrupts so that the necessary storing of registers and so on can be done before new interrupts are able to break in. M is reset to 0 in the order that follows immediately after a PC or a VY-order. (This order might be a jumb order which is the end of a short response program and which returns the control to the main program).

The interrupt masking register C's pos. 0-7 comprises in total 8 masking bits while you have 12 interrupt channels. Which bits, choosed to mask which channels, is decided by means of plugs upon a printed circuit board in GIER. If you want to mask all 12 channels you have to use the same masking-bit for several channels. The configuration of masking bits can be chosen freely of the user. Pos. 8 in the C-register has the fixed built-in function to block all 12 interrupt-channels at a point before the registration i.e. all calls upon interrupt-channel 0-11 will be lost as long as position 8 of the C-register is equal to one. At last position 9 of the C-register has the fixed function to clear the IR-register. During the execution of a PC-order, which sets a 1 in position 9 of the C-register, there will happen a clearing of position 0-11 of the IR-register. Position 9 of the C-register is again cleared at the finish of the PC-order i.e. position 9 is generally allways equal to 0.

The C-register is administrated as mentioned before by means of two new orders PC and GC. The exact description of these orders will be given in the next part, which is built up as an appendix to the operation list in "Lærebog i kodning af GIER". It should be mentioned here that the PC-order is a non counting order and that it places the resulting address in the C-register with the counting part as a mask (compare with the PI- and VY-orders). GC stores the content of the C-register in the cell, specified by the resulting address.

The IR-registers is not accessible for the user, as it has the only task to store information on interruptcalls, which is not immediately performed because the mask is blocking. There is a possibility to act on the contents of IR namely to clear the hole IR-register by executing a PC-order, which puts a 1 in pos. 9 in the C-register. When an interrupt occurs the position in IR belonging to the channel number will be set, and the interrupt is performed as a consequence of this. A clearing of the present position of the IR-register will happen at the same time as the interrupt is being performed.

Under some conditions an interrupt-signal may start GIER if it occurs while the machine is not running. There are two possible stop-situations viz.

1) Stop as a consequence of performing the ZQ-order

2) " " " " " activating the "normal stop" key or
" " " " reading a character with parity failure from the papertape-reader.

In the former stopsituation the machine will start, when there is occuring an interrupt which moreover pass the masks. It is however possible to prevent any of the interrupt channels from starting the machine by means of a plug upon a printed circuit in the machine. In this case no registration of interrupt-calls will happen in the IR-register, while GIER is not running. In stopsituation 2) the machine cannot be started without activating the HP-button or the "normal start" button.

The Data Channel.

As mentioned the data channel is designed for parallel transport of one word (42 bits) at a time. The transfer time for 1 word is 5 μsec.

The data channel is so far utilized as a transfer line between GIER and two external systems viz. the external process unit and the external 4o96 words core memory (YFL).

The process unit includes as mentioned a number of in- and outputs for analogue signals as well as digital information. The address constant of the IL- and US-commands indicates the number of the in- or output from which one reads in or to which one writes out. Each command can release a transfer of a 10 or 20- bits group between the R-register in GIER and the particular in- or output. The in- and outputs of the processunit are further connected to external signalsources in processes which run independently of the data channel in the sense that none of these processes can appear as an address in the commands IL and US.

The external 4096-words core memory is further connected to magnetic tape stations. Contrary to what is the case in the process unit, these units are addressable by means of the commands IL and US. An IL-command whose address indicates a magnetic tape unit causes a transfer of data from the particular magnetic tape unit to the external 4096 words core memory (YFL).

If an IL-command has the address 0 it will cause a transfer of data from YFL to GIER's internal core memory. Accordingly a US-command whose address indicates a magnetic tape unit will cause a transfer of data from YFL to the particular magnetic tape unit. If the address is 0 data are transferred from GIER's internal core memory to the external core-memory. Any IL- or US-command whose address refers to a unit around YFL and YFL ifself will cause the transfer of a whole group of words, a block. The parameters for this blocktransfer must be placed in the R-register before the IL/US-command is executed.

The operationtimes for IL/US depends upon which unit is chosen. In the process-unit the times are 43 µsec except for IL in case an inputchannel for analog-signals is chosen. In this case the operationtime is about 100 µsec.

The external process-unit.

This unit consists as shown in the diagram "Oversigt over Procesdataenhed ind- og udgange" of a number of outputs for digital signals, and 15 outputs for analog signals of which 6 are combined in pairs so as to be able to change two outputs for analog signals at the same time.The conversion time for the D/A-converters is 4 µsek.

There are 30 inputchannels for analogsignals all of which are connected to the same A/D-converter via a multiplexer. The conversiontime for converting an analogsignal to a binary number of 10 digits is about 60 µsec.

The precision of both A/D- and D/A-conversion is better than 1 °/oo.
The comparator in the A/D-converter is selfadjusting towards drift of zero-point

Betegnelse	Virkning	Registrering		Mærke-operation	Ind. af tegn	Specielle bemærkninger
		Mærk.	Overløb			
IL	Fra PD-enheden overføres data til R-registret på følgende måde:	+	+		+	
	$512 \leq c \leq 541$:					
	Analogsignalet på indgang nr. c-512 omsættes i A/D-omformeren, indlæses i buffer-registret ADB pos 0-9 og overføres derfra til R pos 10-19.					Det registrerede overløb angiver situationen på analog-indgangen.
	R pos 00-9 sættes lig med R pos 10.					
	R pos 40-41 sættes lig med ADB pos 40-41.					
	R pos 20-39 uændret.					
	$768 \leq c \leq 797$:					
	Analogsignalet på indgang nr. c-(512+256) omsættes, indlæses i ABD pos 0-9 og overføres derfra til R pos 0-9.					Det registrerede overløb angiver situationen på analog-indgangen.
	R pos 00 sættes lig med R pos 0.					
	R pos 40-41 sættes lig med ADB pos 40-41.					
	R pos 10-39 uændret.					

Betegnelse	Virkning	Registrering		Mærke-operation	Ind. af tegn	Specielle bemærkninger
		Mærk.	Overløb			
IL	547 = c ≦ 549: Informationen, der står i indlæseregistret nr. c-512 pos 0-17 og pos 40-41, overføres til hhv. R pos 0-17 og pos 40-41. R pos 00 sættes lig med R pos 0. R pos 18-19 nulstilles. R pos 20-39 uændret.	+	+		+	
	550 ≦ c ≦ 555: Informationen, der står i indlæseregistret nr. c-512 pos 0-9, overføres til R pos 0-9. R pos 00 sættes lig med R pos 0. R pos 10-19 og R pos 40-41 nulstilles. R pos 20-39 uændret.					
	544 ≦ c ≦ 546: Informationen, der står i kontrolregistret nr. c-512 pos 0-9, overføres til R pos 0-9. R pos 00 sættes lig med R pos 0. R pos 10-19 og R pos 40-41 nulstilles					Kontrolregistrets indhold kan sættes fra GIER med US-ordren.

Betegnelse	Virkning	Registrering		Mærke-operation	Ind- af tegn	Specielle bemærkninger
		Mærk.	Overløb			
IL	R pos 20-39 uændret.					
IL D	Som ovenfor, idet D-adressen træder i stedet for den modificerede adresse.					
US	Fra GIER overføres data til PD-enheden på følgende måde:					
	512 ≦ c ≦ 514:					
	Informationen, der står i R pos 0-19, overføres til udlæseregistret nr. c-512 pos 0-19. R uændret.					Hvert af de 3 registre er forsynet med 2 ciffer-analog omformere, idet den ene omformer informationen, der står i pos 0-9, og den anden omformer informationen, der står i pos 10-19.
	515 ≦ c ≦ 523:					
	Informationen, der står i R pos 0-9, overføres til udlæseregistret nr. c-512 pos 0-9.					Udlæseregistrene er forsynet med ciffer-analog omformere.
	533 ≦ c ≦ 535:					
	Informationen, der står i R pos 0-9, overføres til udlæseregistret nr. c-512 pos 0-9.					Udlæseregistrene styrer digitale potentiometre.

Betegnelse	Virkning	Registrering Mærkn.	Registrering Overl	Mærke-oper.	Specielle bemærkninger
pc	Den modificerede adresse placeres i C-registeret (interruptkontrolregisteret) med ordrens tælletal som maske, idet de positioner i C-registeret, der er angivet ved ettaller i ordrens tælletal(binært),ikke ændres: for i:=0 step 1 until 9 do C [i]:= (C[i] ∧ Ftæl [i])∨(Hpos[i] ∧ ¬ Ftæl [i]);				Ordren er statisk. Står pc som halvordsordre, opfattes tælletallet som nul, d.v.s. at hele den modificerede adresse overføres til C-registeret. Mellem en pc-ordre og den efterfølgende ordre vil et interrupt ikke kunne bryde ind.
pc D	Som ovenfor, idet D-adressen træder i stedet for den modificerede adresse.				Ordren er statisk. Normalt uden interesse.
gc	C-registerets (interruptkontrolregisteret) indhold lagres i pos. 0-9 i celle c, mens resten af cellen er uændret: adressetal [c]:= C-register;				Ved en absolut mærkeoperation et-stilles R_{40} og R_{41} (som ellers er uændrede).
gc D	C-registerets indhold lagres i pos. 0-9 i den celle, hvis adresse angives ved D-adressen,mens resten af denne celle er uændret:adressetal[Dadr]:=C-register;				Ved en absolut mærkeoperation et-stilles R_{40} og R_{41} (som ellers er uændrede).

Tilføjelse til operationslisten:

I rubrikken "Specielle bemærkninger" for satellitordrerne is, ns, it og nt indsættes følgende:

Mellem denne ordre og den følgende
vil interrupt ikke kunne bryde ind.

Operation	talværdi	
	decimal	oktal
il (tidl. ze)	44	54
us (tidl. zf)	45	55
gc (tidl. zh)	47	57
pc (tidl. zi)	48	60