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Title:

General Information on RC 35-221

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Abstract:

This manual contains general information on the Front Processor Adaptor, FPA 100

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CONTENTS

MAIN CHARACTERISTICS 1.1

Short Description. 1.1.1

The FPA 100 is an asynchronous controller intended for use as interconnecting medium between the RC 3500 computer and the RC 8000/ RC 3600 computer.

FPA 100 contains two devices called the WRITE CHANNEL and the READ CHANNEL.

FPA 100 is physically contained within a 4 positions standard RC 3500 module cassette.

Communication with RC 3500. 1.1.2

Communication with RC 3500 takes place via two standard I/O channels, the write channel and the read channel.

All standard I/O instructions can be ordered to the write channel as well as the read channel. There are only few differences in the interpretation of the instructions, which appear in the "programming specifications", section 2.

Normally, the write channel of FPA 100 is used to transmit a data block to the opposite controller and to receive a single status character as a respond to the transmitted block.

The read channel is used to receive a data block from the opposite controller and to transmit a single status character as a respond to the transmitted block.

Communication with the Opposite Controller. 1.1.3

The communication with the opposite controller takes place via a set of output and a set of input lines. The output and input lines are completely symmetrical, each set consisting of:

9 data lines incl. a parity line, and
7 control lines, refer to fig. 1.3.2.

For further specifications of the lines refer to section 3.

Included in the control lines is an autoload request line, which is necessary to be able to initiate an autoload procedure in the opposite controller under RC 3500 program control and vice versa.

The communication is asynchronous on character basis. 8-bits characters are used.

The timing of character transfers are under control of two types of request signals and one request acknowledge signal. The request signals are named:

1. DATA REQUEST
2. STATUS REQUEST

The data request is used as a request signal when the write channel transmits data to the opposite controller, and the status request is used when the read channel transmits status to the opposite controller.

The communication with the opposite controller utilizes the asynchronous, fully interlocked technique. Each request signal issued by FPA 100 must be acknowledged by the opposite controller to complete the transfer.

When FPA 100 wants to transmit a character, the character is placed on the data output lines, and the request signal is set to logical 1. When the opposite controller has stored the character it responds to the request by setting the request acknowledge signal to logical one, indicating the reception of the character. Upon the reception of the acknowledge signal FPA 100 clears the request signal, which also causes the opposite controller to clear the acknowledge signal.

Fig. 1.3.2 illustrates the handshake technique.

At FPA 100 End

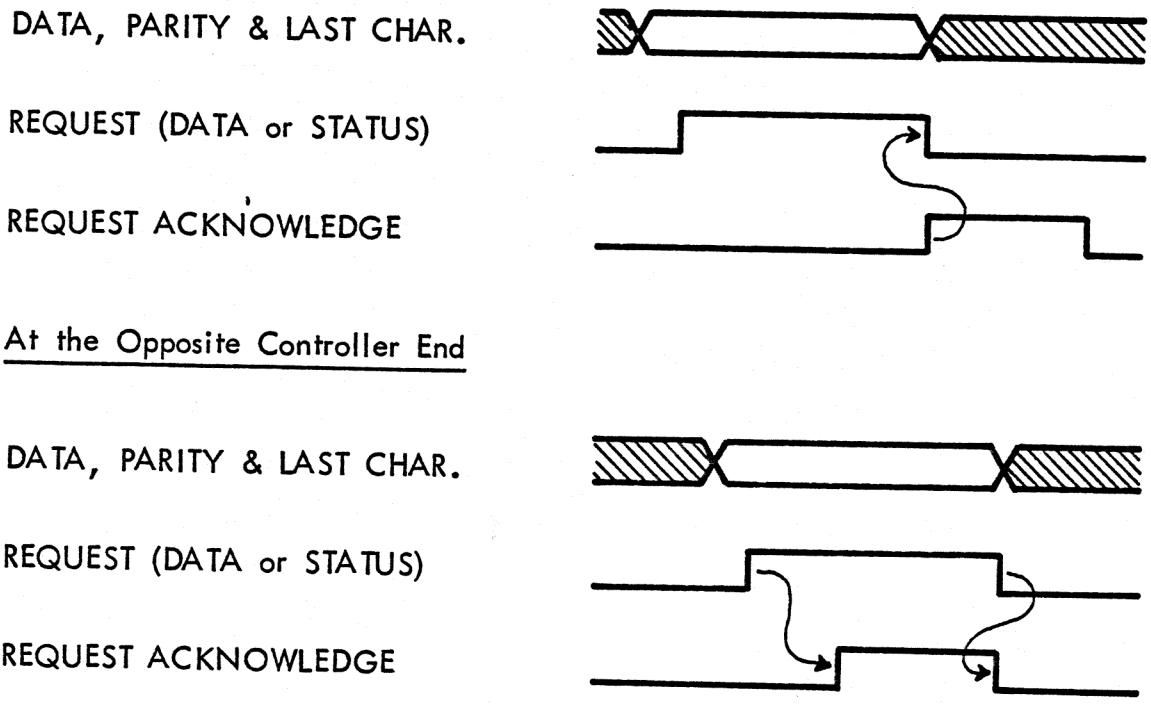
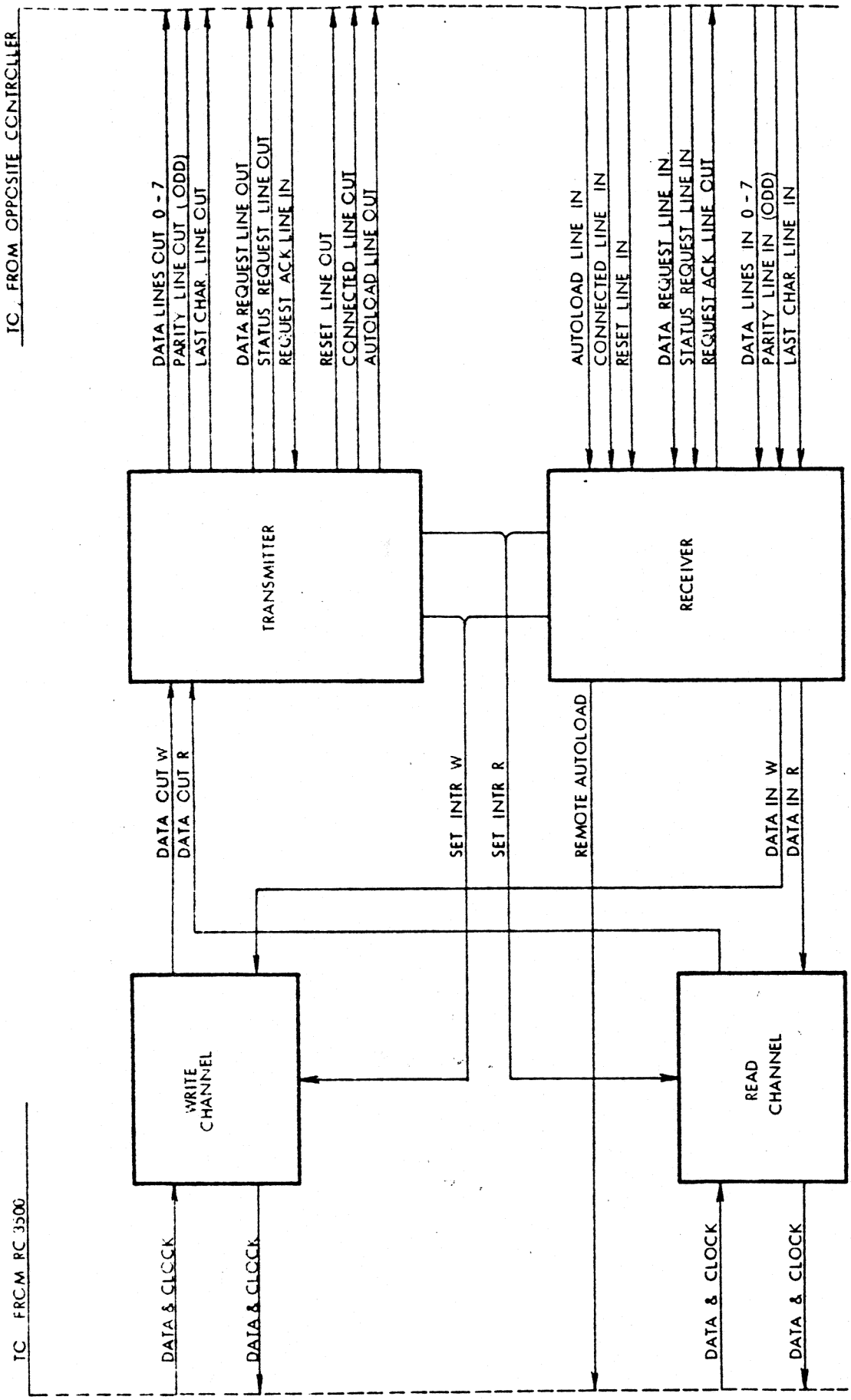


Fig. 1.3.1

Simultaneously with the emission of the last character in a block the LAST CHAR signal is sent to the opposite controller.

Also provided in the control lines is a RESET signal which notifies the opposite controller when the write channel is reset. Likewise, the read channel receives a reset signal from the opposite controller when the transmitter in this controller is reset.


TC FROM OPPOSITE CONTROLLER
DATA LINES OUT 0 - 7
PARITY LINE OUT (ODD)
LAST CHAR. LINE OUT
DATA REQUEST LINE OUT
STATUS REQUEST LINE OUT
REQUEST ACK LINE IN
RESET LINE OUT
CONNECTED LINE OUT
AUTOLOAD LINE OUT
AUTOLOAD LINE IN
CONNECTED LINE IN
RESET LINE IN
DATA REQUEST LINE IN
STATUS REQUEST LINE IN
REQUEST ACK LINE OUT
DATA LINES IN 0 - 7
PARITY LINE IN (ODD)
LAST CHAR. LINE IN
TRANSMITTER
RECEIVER
DATA OUT W
DATA OUT R
SET INTR W
SET INTR R
REMOTE AUTOLOAD
DATA IN W
DATA IN R
WRITE CHANNEL
READ CHANNEL
TC FROM RC 3500
DATA & CLOCK
DATA & CLOCK
DATA & CLOCK
DATA & CLOCK

INTERFACE BETWEEN FPA 100 AND THE OPPOSITE CONTROLLER 1.2

Timing (refer to fig. 3.1). 1.2.1

As mentioned in section 1, "Main Characteristics", the communication with the opposite controller utilizes the handshake technique.

Note that the transmitting unit is allowed to raise the request signal even if the request acknowledge signal is not lowered, which means that it is the rise of the leading edge of the request acknowledge that indicates the reception of the character.

This is done to speed up the transmission, since the transmitting unit does not need to wait for the propagation of the high to low transition of the acknowledge signal.

Upon the reception of the low to high transition of the request acknowledge signal the transmitting unit must lower the request signal. The request signal must be low for at least 100 ns.

The pulse width of request acknowledge must not be less than 30 ns.; however, the signal must not be lowered until the request signal has been lowered. The pulse width of request acknowledge depends on cable delay, driver/receiver propagation delays, and propagation delays in circuits, which utilizes the acknowledge signal. When using FPA 100 interface circuits and principle the width of request acknowledge, measured at the output of the line driver, will not be less than 30 ns.

When measured at the outputs of line drivers, data must lead request with at least 20 ns.; the same specification is valid for the last character signal. Data must not change as long as the request signal is true.

To compensate for max. cable and receiver skew, the receiving unit must delay the request signal at least 100 ns. before the character is stored.

The pulse width of RESET and AUTOLOAD signals shall be at least 300 ns.

Line Drivers and Receivers.

The following line drivers and receivers are recommended:

Drivers:

TEXAS	:	SN 75183
NATIONAL	:	DM 8830
FAIRCHILD	:	9612 E

Receivers:

TEXAS	:	SN 75182
NATIONAL	:	DM 8820 A
FAIRCHILD	:	9613

The line drivers provide differential output signals and are used to drive a twisted pair line with an impedance of app. 120 Ω . The drivers are single supplied and use only + 5V.

SN 75183 and DM 8830 are compatible and include gates, which are useful when it is necessary to gate the signals; therefore this type of driver is used for the control signals.

9612 E is used for the data, parity, and last character signals since these signals need no gating.

The line receivers are designed to sense small differential signals in the presence of large common-mode noise; up to $\pm$ 15V common mode input voltage can be tolerated. The receivers are single supplied and use only + 5V.

SN 75182 and DM 8820 A are compatible and include strobe and terminating resistor (170 Ω). The strobe input is used to strobe all of the control signal receivers with the disconnected signal from the opposite end. This assures that the output of the control signal receivers is always logical 0, if the opposite computer is disconnected (power off or no cable installed etc.).

9613 is used as receiver for the data parity and last character signals, since these signals need no gating. No terminating resistor is included in the 9613.

Cable Characteristics. 1.2.3

The cable to be used should have the following characteristics:

Type: Shielded cable,
min. 16 pairs of twisted wires 0.25 mm^2.

Impedance: App. 120 Ω .

Max.
length: 20 m.

The shield of the cable must be connected to the common zero voltage. Refer to fig. 3.2. The cable should only be terminated in the receiving unit.

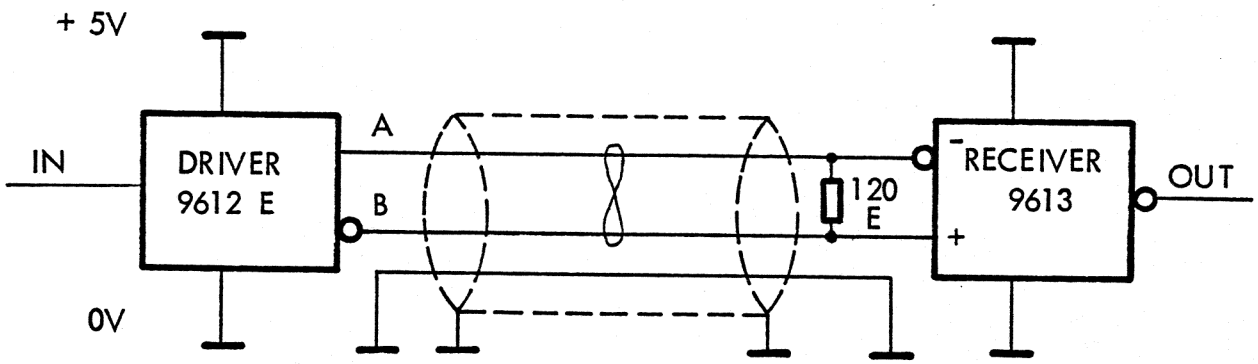


Fig. 3.2

When a logical 1 exists on the line, A shall be positive in relation to B.

Signal Description. 1.2.4

DATA LINES 0 : 7 : Data line 0 is the most significant bit, and data line 7 the least significant bit.

PARITY LINE : This line is the parity line making the parity odd.

LAST CHAR LINE : When logical 1 this line indicates the end of the block. The LAST CHAR signal is generated simultaneously with the emission of the last character in the block. The last char. signal must also be generated during status character transmission.

DATA REQUEST LINE : This signal when logical 1 indicates to the receiving unit that a data character is ready on the data lines 0 : 7. The signal is generated by the transmitter in the transmitting unit.

STATUS REQUEST LINE : This signal when logical 1 indicates to the receiving unit that a status character is ready on the data lines 0 : 7. The signal is generated by the receiver in the transmitting unit.

REQUEST ACKNOWLEDGE LINE : When this signal changes from false to true state, it indicates to the transmitting unit that the character on the data lines have been stored in the receiving unit. Upon the reception of the rising edge of the acknowledge signal the transmitting unit is allowed to fetch the next character and place it on the data lines.

RESET LINE : This line when logical 1 indicates to the receiver in the receiving unit that the transmitter in the transmitting unit has been reset.

CONNECTED LINE : This line when logical 1 indicates to the receiving unit that power is on. The connected signal is used to strobe the following control signals:

RESET
REQUEST ACK
DATA REQUEST
STATUS REQUEST
AUTO LOAD

This assures that the output of these receivers is at logical 0 when power in the transmitting unit is turned off.

AUTOLOAD LINE : This line is necessary to be able to initiate an autoload procedure in the opposite computer under RC 3500 program control. Likewise, the opposite computer may use the line to initiate an autoload procedure in RC 3500.

LINE CHARACTERISTICS
TIMING

AT FPA 100

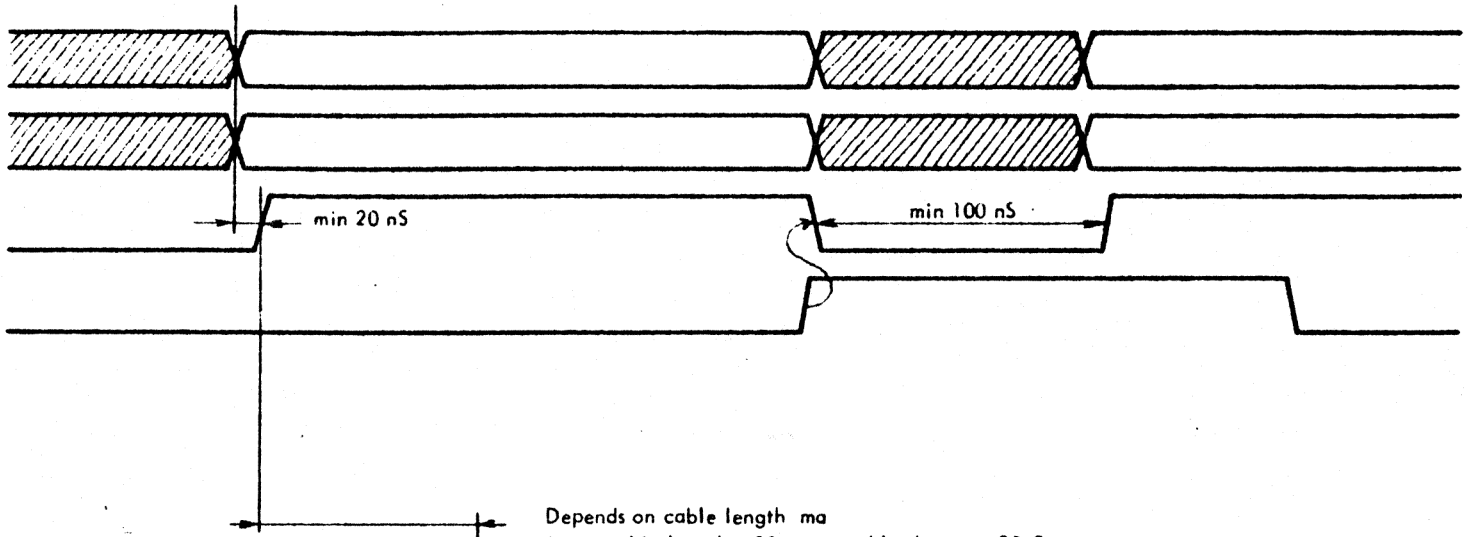
Shaded areas undefined condition

DATA & PARITY LINE

LAST CHAR. LINE

REQUEST LINE (DATA or STATUS)

REQUEST ACKNOWLEDGE LINE



Depends on cable length ma
Max. cable length = 20 m cable skew 20nS

AT OPPOSITE CONTROLLER

DATA & PARITY LINE

LAST CHAR LINE

REQUEST LINE (DATA or STATUS)

REQUEST ACKNOWLEDGE LINE

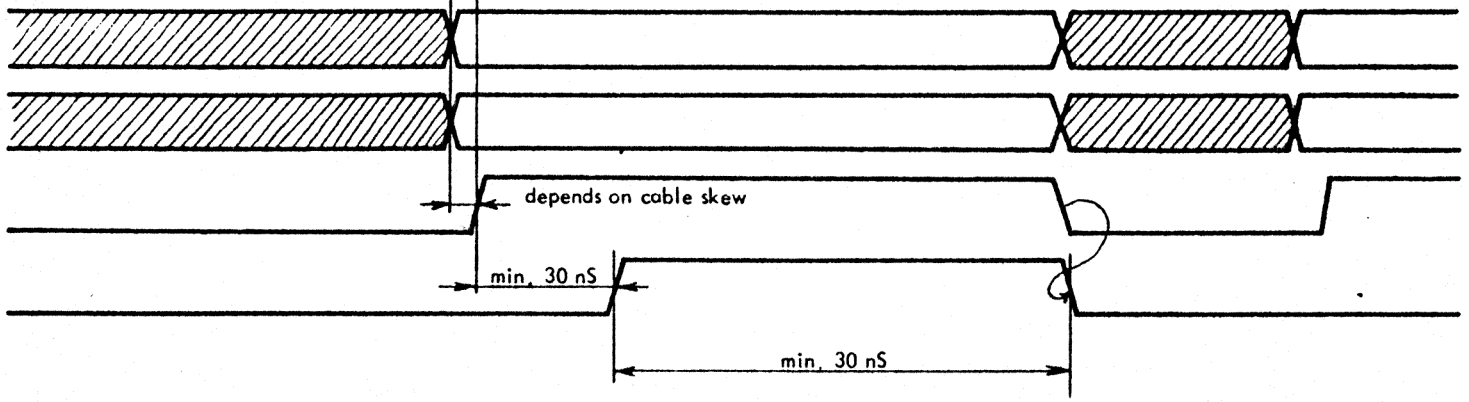


Fig 3

Cables. 1.3.1

Up to three CBL 410 are required to connect FPA 100 to RC 3500. Two CBL 410 are used to connect the WRITE and the READ CHANNEL to two RC 3500 I/O channels. One CBL 410 is used to relay the autoload signal received from the opposite controller to the RC 3500. If FPA 100 is not placed inside the RC 3500 cabinet, shielded cables CBL 466 must be used instead of CBL 410.

Two CBL 817 are required to connect FPA 100 to the RC 8000 front processor adaptor FPA 801.

If FPA 100 is used to connect RC 3500 to RC 3600 or another RC 3500, two CBL 259 are required.

One CBL 439 dc-power cable is used between FPA 100 and the power supply unit MKP 104, and one CBL 432 ac-power cable is used to supply ac-power to MKP 104. When FPA 100 is placed inside the RC 8000 or RC 3600 I/O cabinet, CBL 065 must be used instead of CBL 432.

Refer also to the interconnection diagrams fig. 4.1, 4.2, and 4.3.

Power Requirements. 1.3.2

The MKL 104 housing the logic of FPA 100 requires two voltages:

$+ 5V \pm 5\%/4.5A,$

$- 5V \pm 5\%/250mA.$

These dc-voltages are supplied from the MKP 104 power supply unit, which requires 220V/100W ac-input.

Jack/Plugs.

J1: Std RC 3500 I/O Jack, Type CANNON DEC - 9S.
Used to connect the WRITE CHANNEL to RC 3500.

J2: Std RC 3500 I/O Jack, Type CANNON DEC - 9S.
Used to connect the READ CHANNEL to RC 3500.

J3: Autoload Jack, Type CANNON DEC - 9S.
Used to relay the remote autoload signal to RC 3500.

J4: Data-out to opposite controller, Type CANNON 2 DB 52 S.

J5: Data-in from opposite controller, Type CANNON 2 DB 52 S.

P0: DC POWER SUPPLY PLUG, Type CANNON DB 25 P.

For further information concerning the individual JACKS/PLUGS, refer to Drawings for FPA 100, RCSL: 52-AA 568 .

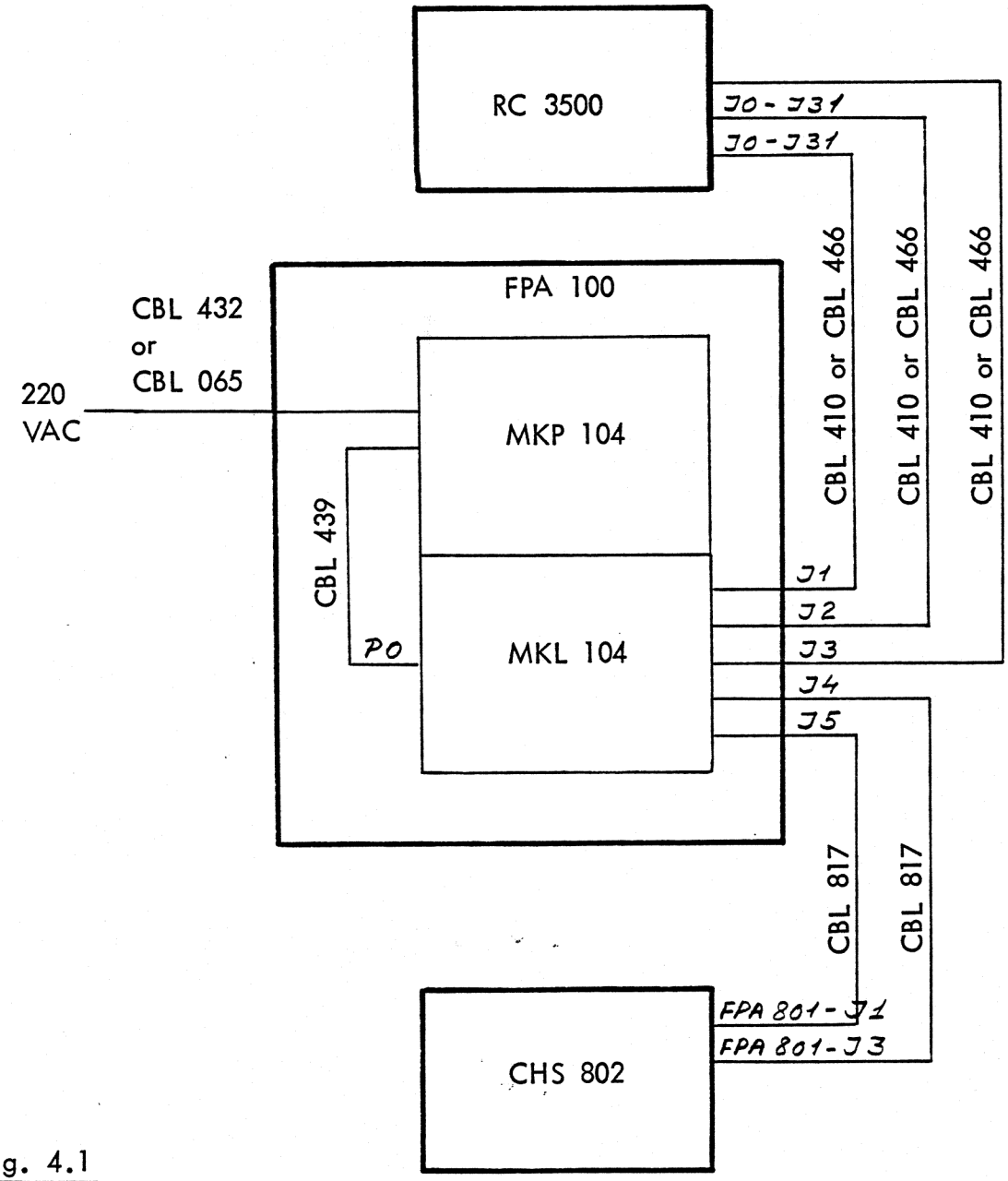


Fig. 4.1

FPA 100 RC 3500 connected to
FPA 801 RC 8000

Interconnection Diagram

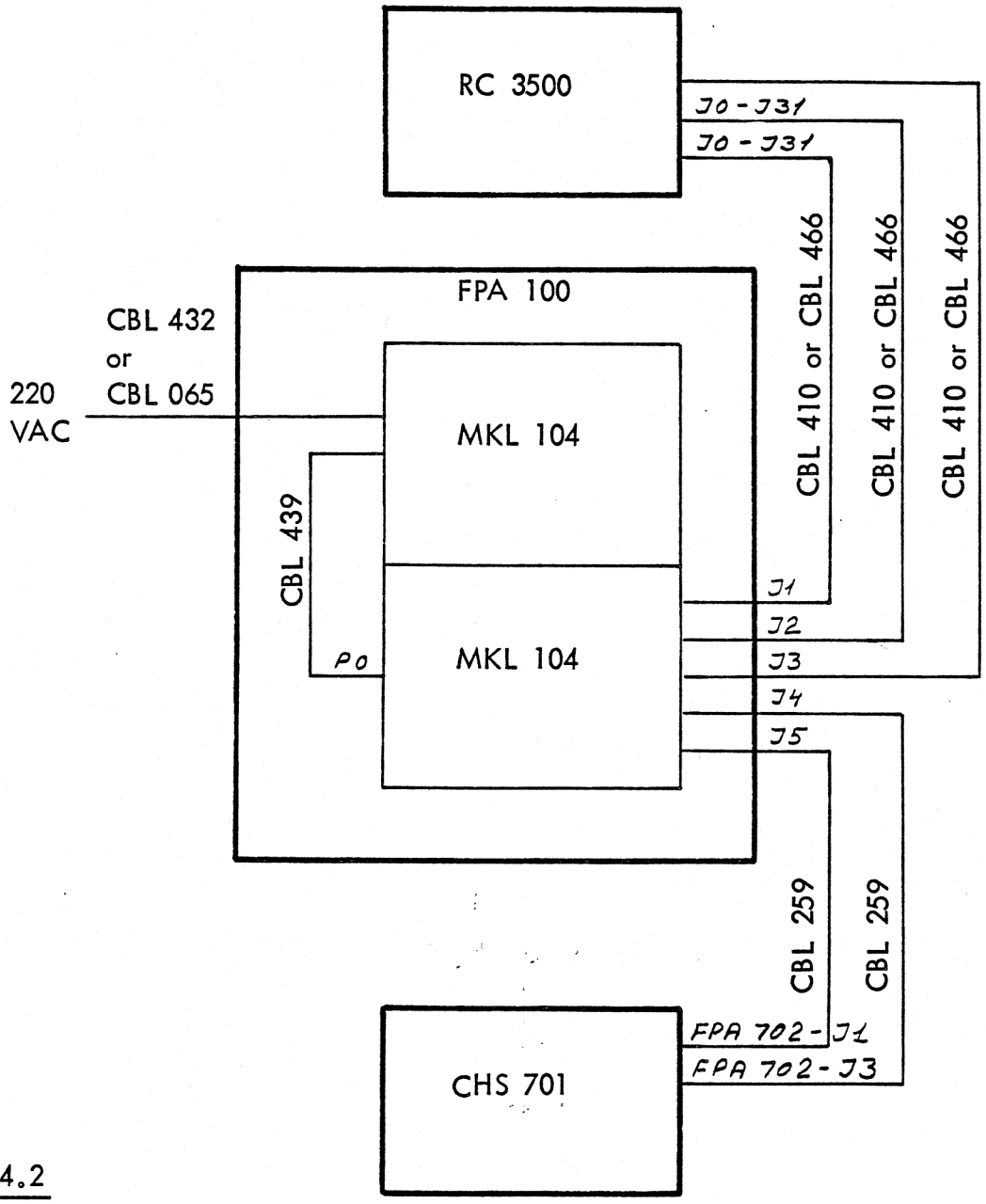


Fig. 4.2

FPA 100 RC 3500 connected to
FPA 702 RC 3600

Interconnection Diagram

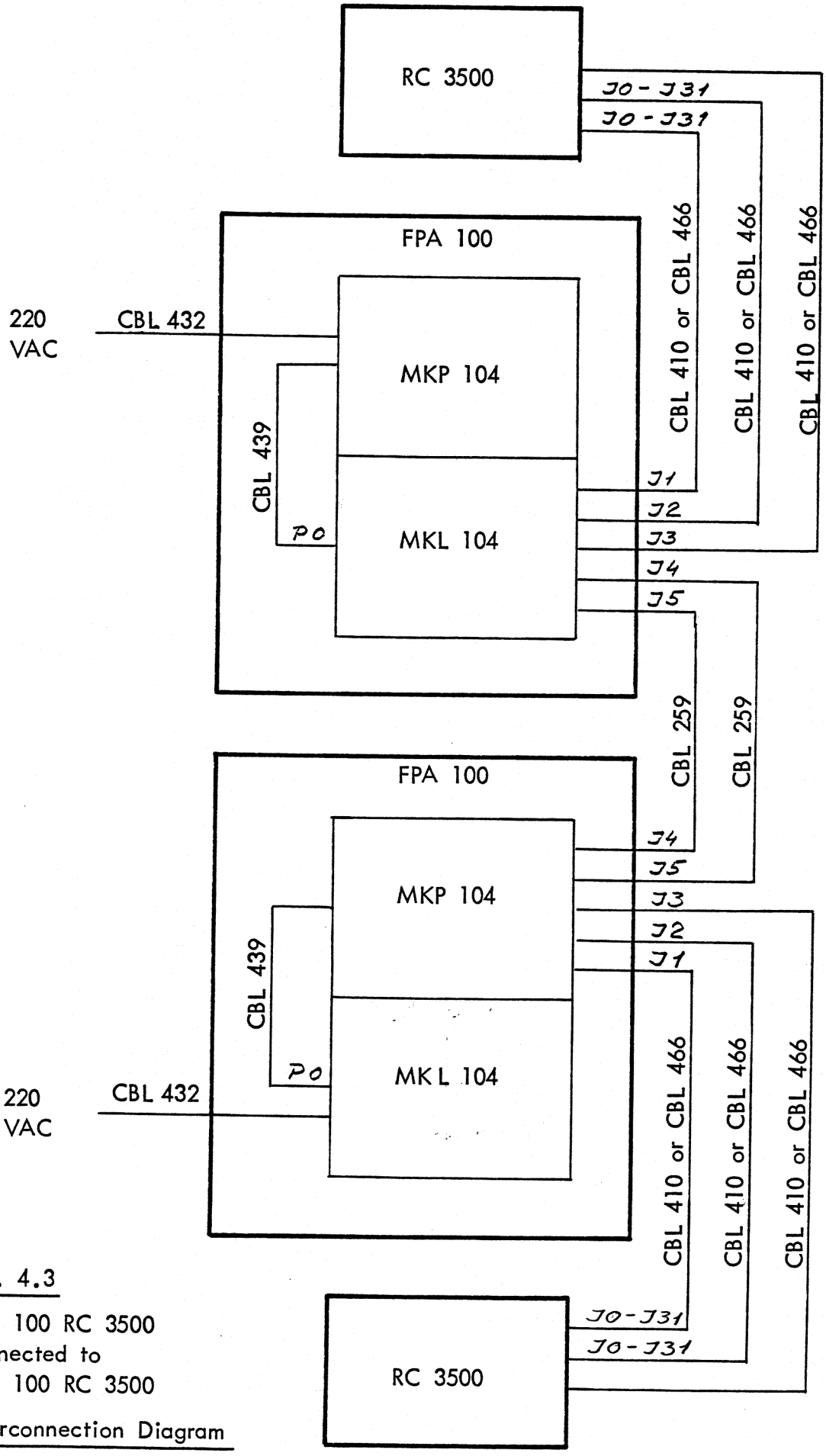


Fig. 4.3

FPA 100 RC 3500
connected to
FPA 100 RC 3500

Interconnection Diagram

RETURN LETTER

Title: General Information on RC 35-221

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