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FPA 100 in connection with RC 8000/3600

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Abstract:

This paper describes the logical structure of the FPA 100 Front Processor Adaptor used as interconnecting medium between RC 3500 and RC 8000/RC 3600

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CONTENTS

The following sections describe the four possible I/O instructions for the write and the read channel.

WRITE CHANNEL. 2.1

This channel uses the following I/O instructions:

Write data

Read data

Write control

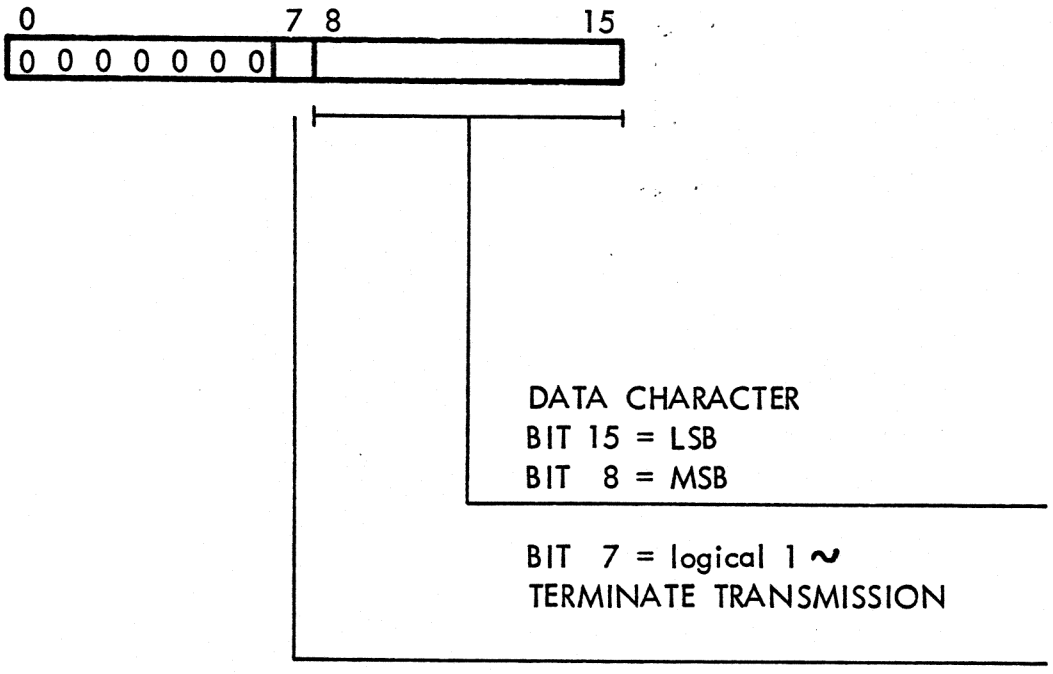
Read status

The write channel is normally used to transmit a data block to the opposite controller and to receive a single status character from the opposite controller as a respond to the transmitted data block.

Write Data. 2.1.1

From RC 3500 to FPA 100.

Output register is interpreted as follows:



This instruction terminates the reception of characters on the write channel and places the channel in the write mode. Bits 8-15 of output register are interpreted as a character, which is transferred to the opposite controller using the data request signal.

Since the write channel and the read channel share transmission lines and transmission circuits, a write data instruction to the write channel cannot be terminated as long as a block is being written on the read channel. Likewise, a write data instruction to the read channel cannot be terminated as long as a block is being written on the write channel, i.e. transmission of status character can only take place between blocks.

A block may consist of one or more characters. The last character in the block is identified by a last character signal, which is sent to the opposite controller simultaneously with the last character. A block consisting of only one character is by definition a single character accompanied by the last character signal equal to logical 1. A block consisting of more than one character is by definition a chain of characters each accompanied by a last character signal = 0, and terminated with a character accompanied by a last character signal = 1.

When the character to be transmitted has been loaded into the transmitter character buffer, RC 3500 is notified by means of an interrupt indicating that the next character is required for transmission. Full double buffering allows one full character period to fetch the next character. A last character signal is sent to the opposite controller, if the write data instruction contains bit 7 equal to 1. When the last character has been acknowledged by the opposite controller status bit 9, transmit block end is set to logical 1, and an interrupt is generated indicating the end of the transmission. Characters in the block may be transmitted using the wbb instruction, since bit 7 will be automatically 0 in this instruction. The last character must be transmitted using the wwc instruction.

Every character transmitted to the opposite controller is automatically equipped with a parity bit. Odd parity is used.

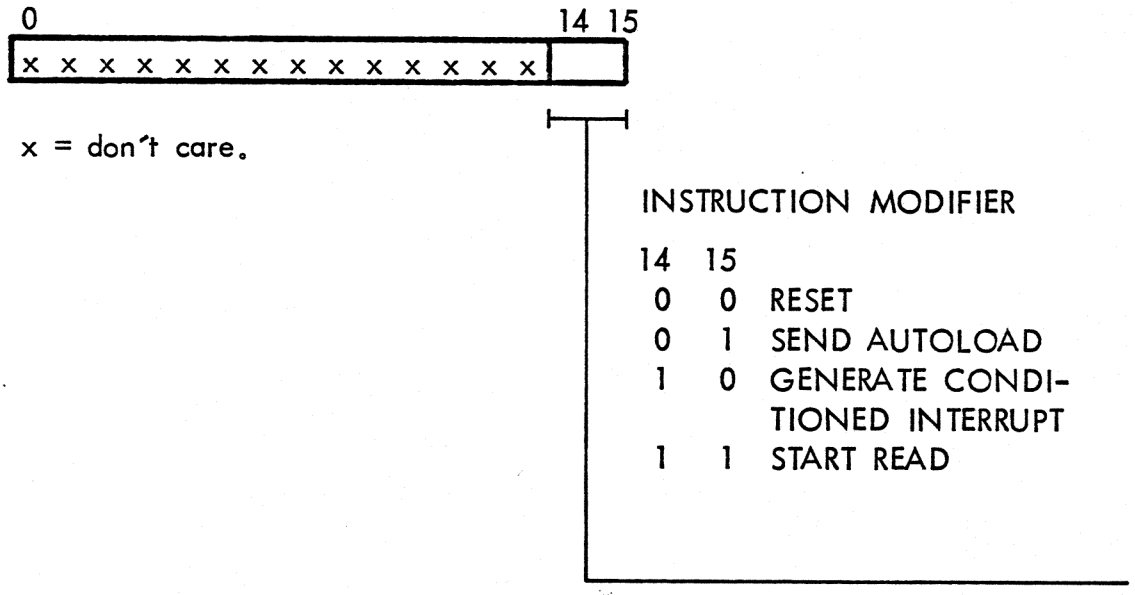
Time out may occur during the transmission if an acknowledge signal is not returned from the opposite controller within a certain time after the emission of the data request signal. If time out occurs, an interrupt is generated and status bit 10 is set to logical 1.

A write control reset instruction terminates the transmission immediately regardless to the terminate transmission parameter.

Write Control. 2.1.2

From RC 3500 to FPA 100.

W1 is interpreted as follows:



Reset.

This instruction terminates write channel instructions immediately and forces the write channel into a well defined and idle condition, and simultaneously a reset signal is sent to the receiver of the opposite controller. No interrupt is generated when the reset instruction is terminated, and no status information is cleared.

Send Autoload.

By means of this instruction it is possible to send an autoload signal to the opposite controller, which may re-lay the signal to the computer. The computer may use the signal to initiate an autoload procedure. No interrupt is generated when the send autoload instruction is terminated.

Generate Conditioned Interrupt.

The generate conditioned interrupt instruction directs the write channel to return an interrupt to RC 3500 if a write data, read data, or read status instruction has not been ordered as a respond to a previously generated interrupt.

Start Read.

This instruction terminates transmission on the write channel, places the channel in read mode, and causes the channel to wait for a status request from the opposite controller.

Since the write channel and the read channel share receive lines and receive circuits, the start read instruction to the write channel cannot be terminated as long as a block is being read on the read channel, i.e. status transfer between the write channel and the opposite receiver can only take place between blocks.

If a status request signal from the opposite controller is not present at the time of the start read instruction, it is possible for the read channel to take control over the receive circuits, and the write channel must wait until the read channel has finished.

Provided a block is not being read by the read channel, and a status request signal is received, the start read instruction is terminated with an interrupt, which indicates to RC 3500 that a character is available. The character can be transferred to RC 3500 using the read data instruction.

There is nothing to prevent status from consisting of more than one character as long as the characters are transferred using the status request signal. If this is the case, every character received causes generation of an interrupt. When the last character in the block has been read by RC 3500 the receive block end status is set to logical 1 and an interrupt generated. Upon the following read data instruction, the write channel transfers a dummy character to RC 3500 accompanied by end of information. If only a single character is used as status, this character shall be considered as a status block consisting of one character.

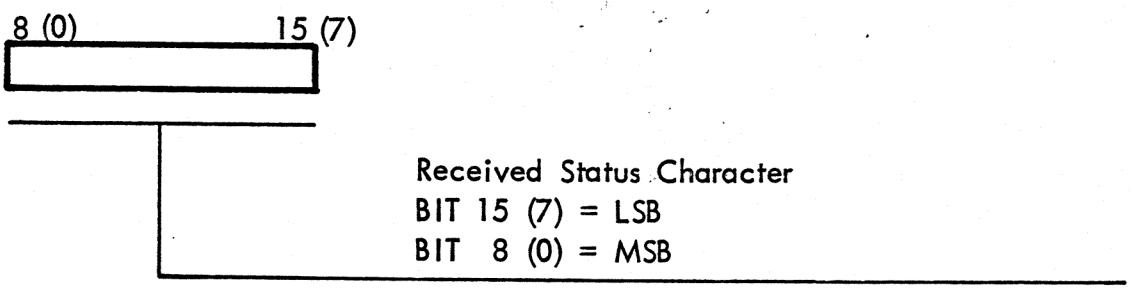
Characters received are automatically checked for correct parity. Odd parity is used. If a parity error is detected, the parity error status is set to logical 1.

Full double buffering allows one full character period for RC 3500 to store the character.

Read Data. 2.1.3

From FPA 100 to RC 3500.

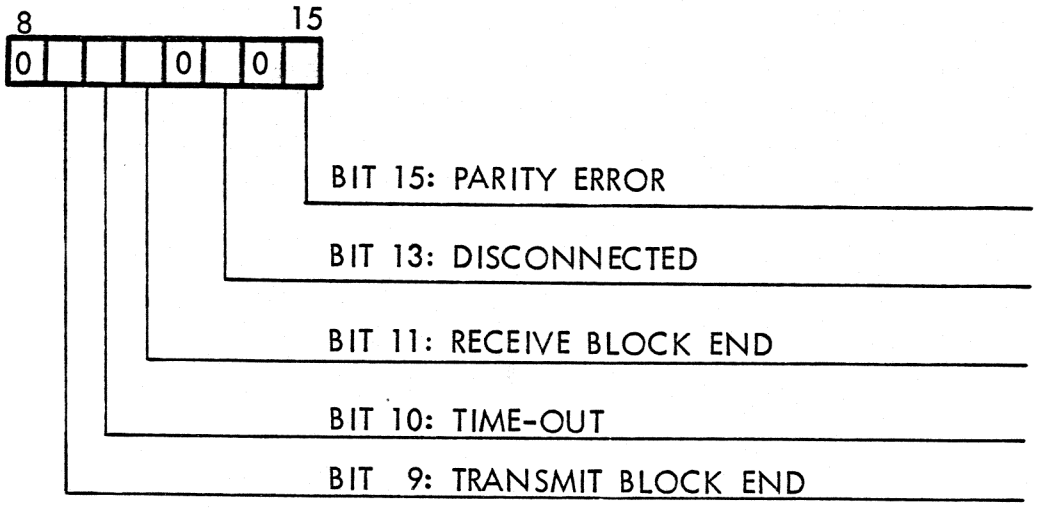
Input register shall be interpreted as follows:



This instruction is used to transfer status characters to RC 3500. Refer to section 2.1.2: "Start Read". The read data instruction terminates transmission on the write channel, but the channel is not set into read mode.

From FPA 100 to RC 3500.

Input register shall be interpreted as follows:



All status bits are cleared by either:

1. Power turn on
2. Termination of the read status instruction

If a read data or write data instruction is ordered, while status bit 9, 10, or 11 is already present, an interrupt will be generated. If the instruction ordered was a read data, a dummy character accompanied by end of information is transferred to RC 3500 in addition to the interrupt.

BIT 9: TRANSMIT BLOCK END.

This status bit is set to logical 1, when the last character in the block has been acknowledged by the opposite control (the character accompanied by the last character signal). Simultaneously with the transmit block end status an interrupt is generated, indicating the end of the transmission.

BIT 10: TIME-OUT.

Every character sent from the write channel to the receiver of the opposite controller must be acknowledged within a certain time; if this is not the case, time-out occurs and status bit 10 is set to logical 1 simultaneously with the generation of an interrupt.

BIT 11: RECEIVE BLOCK END.

This status bit is set to logical 1, when the last character in the block has been read by RC 3500. Simultaneously with receive block end status, an interrupt is generated, and upon the reception of the following read data instruction, the write channel transfers a dummy character to RC 3500 accompanied by end of information.

BIT 13: DISCONNECTED.

This status bit when logical 1, indicates to RC 3500 that the opposite controller is or has been disconnected, i.e.:

1. Power off or
2. No interconnecting cables installed.

BIT 15: PARITY ERROR.

This status bit when logical 1 indicates that a parity error in a received status character has been detected.

READ CHANNEL. 2.2

This channel makes use of the following I/O instructions:

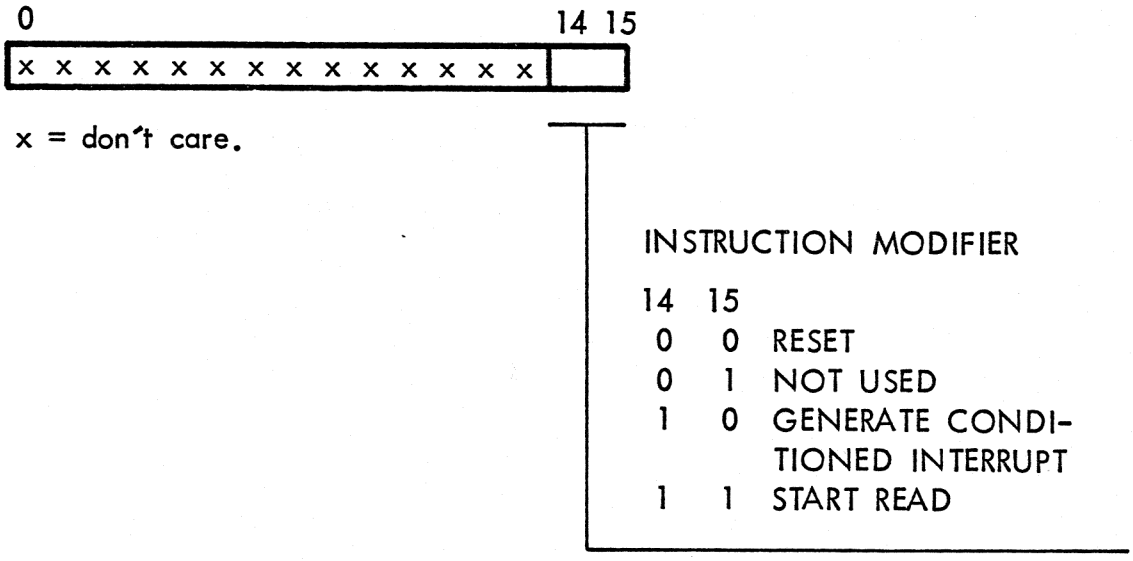
Write control
Read data
Write data
Read status

The read channel is normally used to receive a data block from the opposite controller and to transmit a single status character to the opposite controller as a respond to a received data block.

Write Control.

From RC 3500 to FPA 100.

W1 is interpreted as follows:



By means of the instruction modifier field, 4 different write control instructions can be ordered to the read channel; however, only 3 of the 4 possible instructions are utilized.

Ordering modification 1 has no effect, the instruction is a dummy instruction.

Reset.

This instruction terminates read channel instructions immediately and forces the read channel into a well defined and idle condition.

No interrupt is generated when the reset instruction is terminated, and no status information is cleared.

Generate Conditioned Interrupt.

This instruction directs the read channel to return an interrupt to RC 3500, if a write data, read data, or read status instruction has not been ordered as a respond to a previously generated interrupt.

Start Read.

This instruction terminates transmission on the read channel, places the channel in read mode, and causes the channel to wait for the reception of a data request from the opposite controller.

Since the read channel and the write channel share receive lines and receive circuits, the start read instruction to the read channel cannot be terminated as long as a block is being read on the write channel. If a data request is not present at the time of the start read instruction, it is possible for the write channel to take control over the receive circuits, and the read channel must wait until the write channel has finished.

Provided a block is not being read by the write channel, and a data request signal received, the start read instruction is terminated with an interrupt, which indicates to RC 3500 that the first character is available. The character can be transferred to RC 3500 using the read data instruction.

For every character received hereafter, an interrupt is generated, and when the last character in the block has been read by RC 3500, the receive block end status is set to logical 1, and an interrupt generated. Upon the reception of the following read data instruction, the read channel transfers a dummy character to RC 3500 accompanied by end of information.

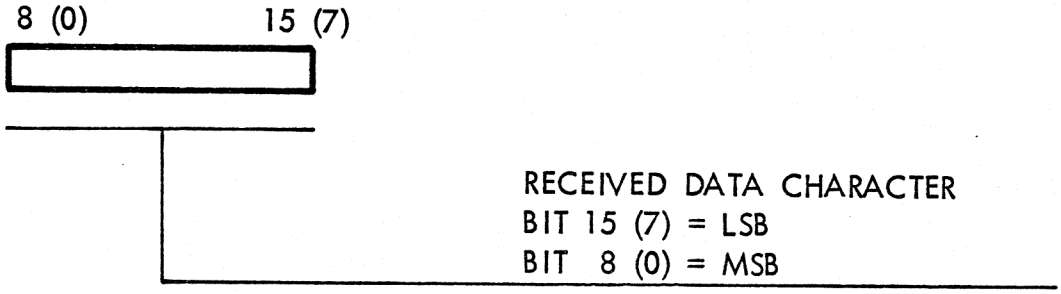
Full double buffering allows one full character period for RC 3500 to store the character.

Characters received are automatically checked for correct parity. Odd parity is used. If a parity error is detected, the parity error status is set to logical 1.

Read Data. 2.2.2

From FPA 801 to RC 3500.

Input register shall be interpreted as follows:

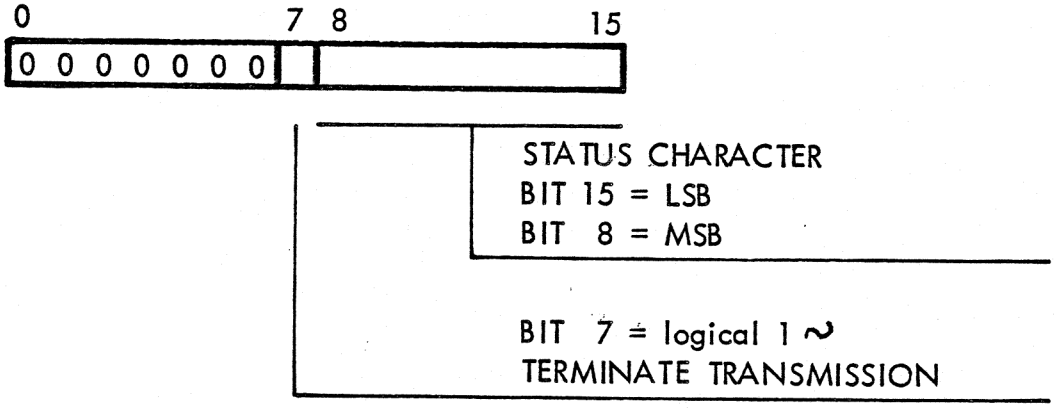


This instruction is used to transfer data characters to RC 3500. Refer to section 2.2.1: "Start Read". The read data instruction terminates transmission on the read channel, but the channel is not set into read mode.

Write Data. 2.2.3

From RC 3500 to FPA 100.

Output register is interpreted as follows:



This instruction terminates the reception of characters on the read channel and places the channel in the write mode. Bits 8-15 of output register are interpreted as a status character, which is transferred to the opposite controller using the status request signal.

Since the read channel and the write channel share transmission lines and transmission circuits, a write data instruction to the read channel cannot be terminated as long as a block is being written on the write channel. Likewise, a write data instruction to the write channel cannot be terminated as long as characters are being written on the read channel, i.e. transmission of status character can only take place between blocks.

There is nothing to prevent status from consisting of more than one character. When the character to be transmitted has been loaded into the character buffer, RC 3500 is notified by means of an interrupt indicating that the next character is required for transmission. Full double buffering allows one full character time to fetch the next character. A last character signal indicating the end of the block is sent to the opposite controller simultaneously with the character if the write data instruction contains bit 7 equal to logical 1. When the last character has been acknowledged by the opposite controller status bit 9, transmit block end, is set to logical 1, and an interrupt is generated indicating the end of the transmission. A single status character transfer is considered as a block consisting of only one character.

Characters in the block may be transmitted using the wbb instruction, since bit 7 will be automatically 0 in this instruction. The last character must be transmitted using the wwc instruction.

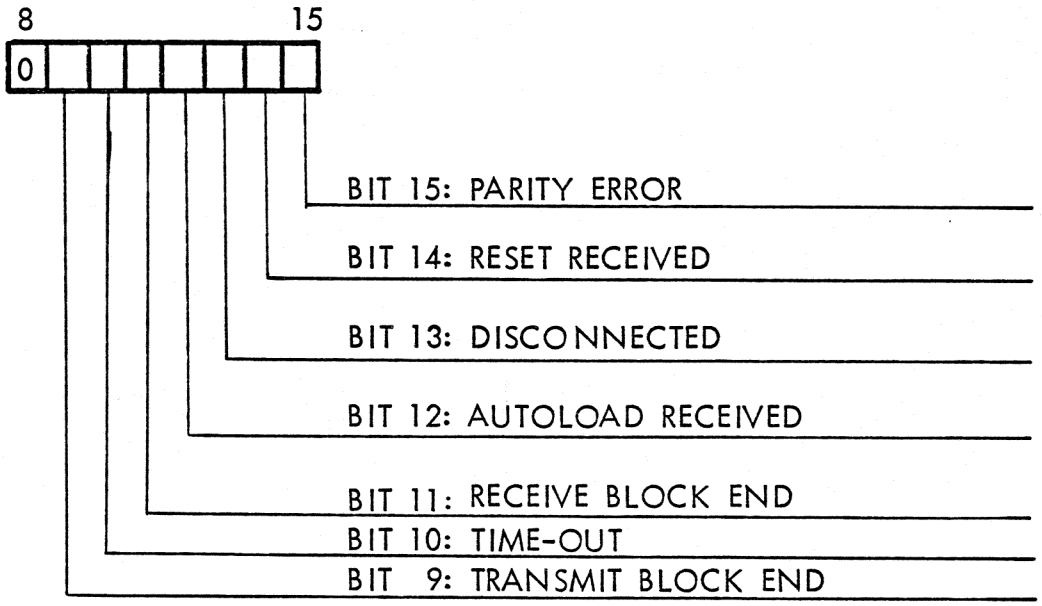
Every character transmitted to the opposite controller is automatically equipped with a parity bit. Odd parity is used.

Time-out may occur during the transmission if an acknowledge signal is not returned from the opposite controller within a certain time after the emission of the status request signal. If time-out occurs, an interrupt is generated and status bit 10 is set to logical 1.

A write control reset instruction terminates the transmission independent of the terminate transmission parameter.

From FPA 100 to RC 3500.

Input register shall be interpreted as follows:



All status bits are cleared by either:

1. Power turn on or
2. Termination of the read status instruction.

If a read data or write data instruction is ordered, while status bits 9, 10, 11, 12, or 14 are already present, an interrupt will be generated. If the instruction ordered was a read data, a dummy character accompanied by end of information is transferred to RC 3500 in addition to the interrupt.

BIT 9: TRANSMIT BLOCK END.

This status bit is set to logical 1, when the last character in a block has been acknowledged by the opposite controller (the character accompanied by the last character signal). Simultaneously with the transmit block end status an interrupt is generated, indicating the end of the transmission.

BIT 10: TIME-OUT.

Every character sent from the read channel to the transmitter of the opposite controller must be acknowledged within a certain time. If this is not the case, time-out occurs and status bit 10 is set to logical 1 simultaneously with the generation of an interrupt.

BIT 11: RECEIVE BLOCK END.

Receive block end status is set to logical 1 when the last character in the block has been read by RC 3500. Simultaneously with receive block end status, an interrupt is generated, and upon the reception of the following read data instruction, the read channel transfers a dummy character to RC 3500 accompanied by end of information.

BIT 12: AUTOLOAD RECEIVED.

This status bit, when logical 1, indicates that an autoload signal from the opposite controller has been received. The autoload received status causes generation of an interrupt, and upon the reception of a possible following read data instruction, the read channel transfers a dummy character to RC 3500 accompanied by end of information.

BIT 13: DISCONNECTED.

This status bit when logical 1 indicates to RC 3500 that the opposite controller is or has been disconnected, i.e.:

1. Power off or
2. No interconnecting cables installed.

BIT 14: RESET RECEIVED.

Reset received indicates that a reset signal from the opposite controller has been detected. Reset received causes generation of an interrupt, and upon the reception of a possible following read data instruction, the read channel transfers a dummy character to RC 3500 accompanied by end of information.

BIT 15: PARITY ERROR.

This status bit, when logical 1, indicates that a parity error in a received character has been detected.

RETURN LETTER

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FPA 100

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