RCSL No: 99 0 00772

Edition: November 1984

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Title:

ETC601/611

Hardware Reference Manual

RCSL No 42-i 2164

A/S REGNECENTRALEN
af 1979

Keywords: ETC601, ETC611, Hardware Reference Manual.

Abstract: This Manual describes the ETC601/611 LAN controller, which is an intelligent communication module.
The ETC601/611 is designed to connect to a Multibus backplane and can operate as either master or slave.

(188 printed pages)

RCSL Nr. 46-F 0087

Printed by A/S Regnecentralen af 1979, Copenhagen

TABLE OF CONTENTS PAGE

TABLE OF CONTENTS (continued) PAGE

TABLE OF CONTENTS (continued) PAGE

1. INTRODUCTION 1.

This manual describes the ETC board which is an intelligent communication module. The ETC is designed to communicate with other system modules through a Multibus backplane. In a Multibus backplane the ETC can operate as either master or slave.

In addition to the above mentioned Multibus connection the ETC provides a 16-bit iSBX interface, an interface to an Ethernet or RC micronet, a full duplex bit-or bytesynchronous communicationchannel with V.24 and X.21 interface, and a V.24/V.28 consolinterface.

The manual is divided into basically three parts. The first part contains a general description of the board. This part provides the user with information necessary in the start-up and check-out phase. Chapter three provides the user with information which is necessary to program the ETC board. The last chapter contains a detailed hardware description of the board.

The ETC is mainly based on highly integrated VLSI devices. It is therefore advisable to read the data sheets in conjunction with reading this manual (see appendix A).

2. GENERAL INFORMATION 2.

2.1 Short Description 2.1

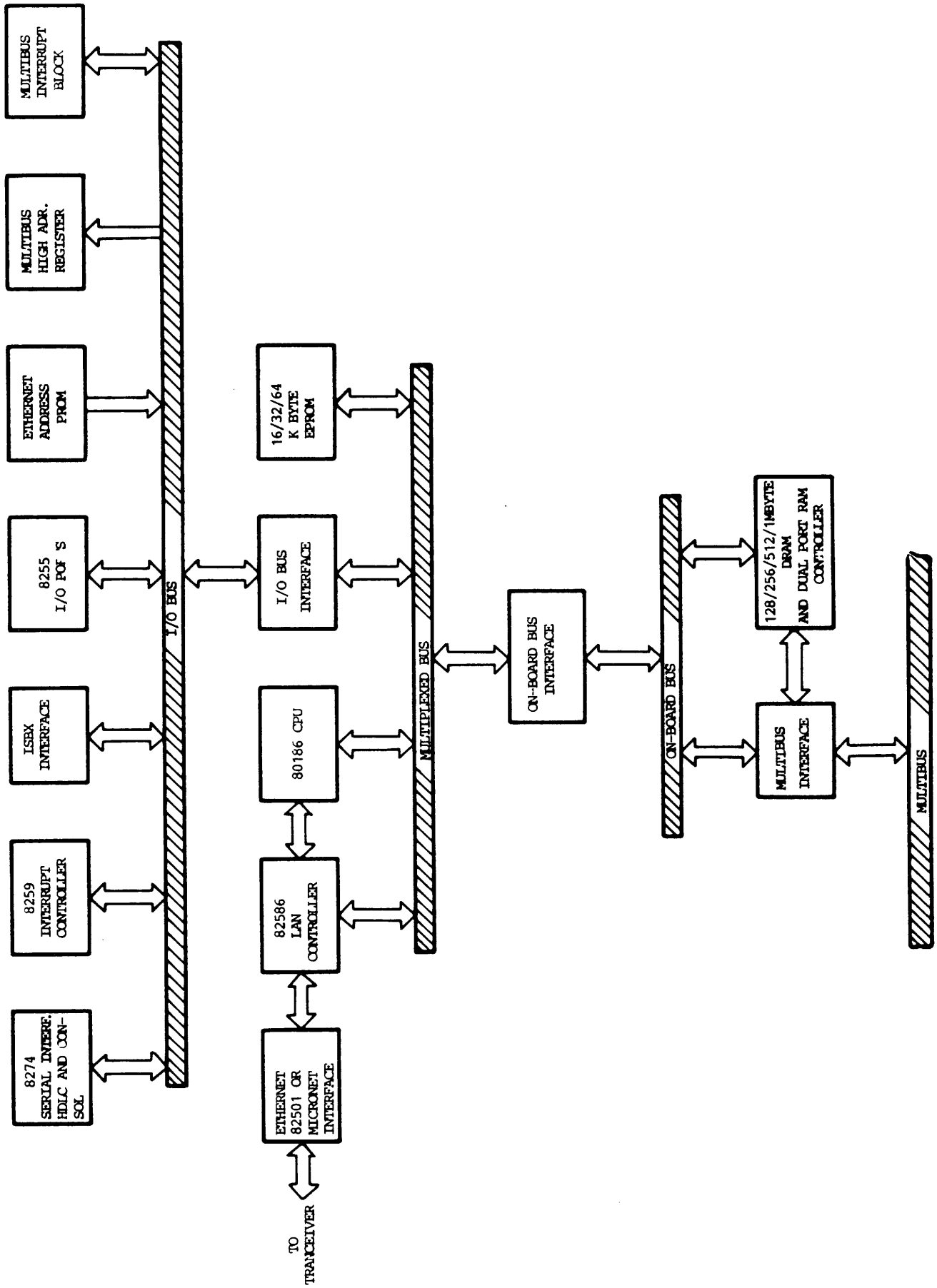
Figure 1 shows a simplified system architecture block-diagram of the ETC Controller.

The control processor is an 8 MHz INTEL 80186, which is a high-integration 16-bit microprocessor (ref. 1). This CPU onchip holds

- Programmable chipselect lines
- Programmable waitstate generator
- 2 independant DMA channels
- Programmable interrupt controller
- 3 programmable timers

The 82586 LAN controller is a coprocessor operating parallel to the CPU. The 82586 handles datatransmission determined by RAM resident parameters set up by the CPU. The interface to transmissionline is selectable by the use of an extension board to be either Ethernet (IEEE802.3) or RC micronet.

The onboard memory consists of both EPROM and RAM. The EPROM memory, which at least must hold the initialization code for the ETC board, is located in the topmost portion of the 1M byte onboard address space. Two 28-pin sockets are available for two EPROM chips offering upto 64 Kbytes of EPROM. The EPROM is accessible from both the CPU and the 82586 LAN controller.



ETC601/611

ETHERNET CONTROLLER
SYSTEM BLOCK DIAGRAM

Fig. 1

The onboard RAM area is expandable from 128K bytes and upto 1M bytes. The expansion is accomplished by use of an expansion piggy-back board and/or by changing 64 Kbit DRAM chips with 256 Kbit DRAM chips. The RAM is accessible by the CPU and the 82586 LAN controller. Via the multibus interface it is also accessible from other SBC boards contained in the multibus system. The location of the RAM area in the onboard address space and in the total 16Mbytes Multibus address space is selectable by jumper settings.

When the RAM is extended to 1 Mbytes the topmost portion is shadowed by the EPROM and therefore not visible to the onboard 80186 CPU, although it can be accessed from the multibus, and the 82586 coprocessor.

Through the Multibus interface it is possible for the onboard CPU to access Memory and I/O devices on system contained Multibus devices. All accesses to Memory and I/O addresses not found onboard generates a Multibus request.

The MPSC (Multi-Protocol Serial Controller) 8274 provides two independent communications channels. Channel A is used as a general purpose serial channel providing both bit-and bytesynchronous protocols. The channel A is interfaced via a V.11 and a V.28 interface. Which of the interfaces that is used is determined by the linecable connected to channel A. Channel A may be driven in DMA, interrupt, or polled mode. Channel B is used as a V.24/V.28 consol interface. Channel B may be either interrupt or polled mode driven.

The iSBX interface allows expansion of the functionality of the ETC board by installing an iSBX (8 or 16 bit buswidth) Multimodule board. The iSBX interface is connected to onboard interruptsystem by two interrupt lines. The interface also offers one DMA channel.

The 8255 I/O ports is used to control a number of onboard signals (e.g. iSBX optional signals, console modem signals). The 8255 also has an output for controlling 4 external LED´s.

The ethernet address PROM is located in I/O space and provide the current ETC board with a unique address. This address can be read by the CPU to identify the

ETC board when connected to a local area network.

The Multibus mega-byte address register in I/O space holds the 4 most significant addressbits in the 16Mbytes Multibus address space. This address is written by the onboard CPU.

The Multibus interrupt block provides the ETC with an opportunity to activate 4 of the Multibus interrupt lines. After being set by onboard CPU these interrupt are cleared from multibus device recognizing the interrupt.

The interruptsystem on the ETC board is built around the 8259 interrupt controller. Interrupts may be generated from iSBX interface, 82586 LAN controller, RAM parity error logic, MPSC 8274, 8 Multibus interruptlines, and a flagbyte interrupt. The flagbyte interrupt is generated when system contained Multibus devices writes a dedicated RAM location.

2.2 Specification 2.2

2.2.1 Performance Specifications 2.2.1

80186 CPU Clock Rate:	8MHz or 6MHz jumper selectable.
Word Size:	8 or 16 bits.
Data Bus Size:	16 bits.
EPROM Capacity:	Upto 64 Kbytes depending on EPROM type installed.
RAM Capacity:	Basically 128 Kbytes expandable to 512 Kbytes by exchanging 64Kbit RAM chips with 256Kbit RAM chips. By use of RAM expansion board MEX 601/611 the total onboard RAM area is extended to 256K/1Mbytes. All RAM contains 1 parity bit for error detection.

EPROM Addres: Range:

Size	Address range
16Kbytes	FC000H-FFFFFH
32Kbytes	F8000H-FFFFFH
64Kbytes	F0000H-FFFFFH

RAM Address : nge:

RAM memory start location is always 00000H. The 1Mbytes address space is then filled continous upwards with expansions.

Onboard RAM . cessible from Multibu

Selectable in 128 Kbytes portions. Always starting with lower most 128 Kbytes portion.

Multibus Add ss Space Accessible f m ETC:

All Multibus memory address space (16 Mbytes) and I/O address space (64 Kbytes) not contained onboard ETC can be accessed.

Flag Byte:

The flagbyte is located in RAM location 00402H. Writing this location from Multibus activates an onboard interruptline.

Board Reset:

The ETC can be reset from Multibus devices by writing RAM location 00400H. This option is enabled by a jumper.

Interrupts:

The 8 vectored interrupts from MPSC 8274 is connected to INT1 on CPU.
By jumpers it is possible to strap the CPU non maskable interrupt plus eight 8259 interrupt inputs from proceeding sources:
2 iSBX interrupts, 82586 LAN controller interrupt, RAM parity error interrupt, flagbyte interrupt, 8 Multibus Interrupts.

The ETC board is capable of

	generating up to 4 interrupt requests on the Multibus.
LAN Interface:	Logical interface provided by the 82586 LAN controller. Electrical interface according to Ethernet (IEEE802.3) or the RC specified Micronet. If Ethernet is selected the 82501 ESI must be installed in the interface socket. If Micronet is selected the MSI601 piggy-back board must be installed.
General Purpose Serial Channel:	Bit- and bytesynchronous protocols (BSC, HDLC, SDLC etc.) V.28 or V.11 electrical interface selectable by jumper in linecable. Max. datarate 20Kbit/s for V.28. Max. datarate 880Kbit/s for V.11.
Console Interface:	V.24/V.28 asynchronous.
Connectors Multibus:	P1 (bussed on backplane) P2 (4 most significant addresses bussed on backplane).
General Purpose Serial Channel:	J4
Console interface:	J3
LAN interface:	J5
iSBX Interface:	J1
4 External LED´s:	J2 (includes pull-up resistors)

2.2.2 Environmental Specifications 2.2.2

Operating Temperature:	0 degree C - 40 degree C
Relative Humidity:	20% - 80% (non condensing)

2.2.3 Physical Specifications 2.2.3

width:	304.8mm
length:	179.1mm
height:	29.5 mm incl. exp. modules

2.2.4 Power Specifications 2.2.4

Power Dissipation:	32,8W (max.)
Vcc:	+5V +/- 5% (6A max.)
Vdd+:	+12V +/- 10% (60mA max.)
Vdd-:	-12V +/- 10% (45mA max.)
	If an iSBX Multimodule board is used additional power requirements are: Icc: 3A Idd+: 1A Idd-: 1A

2.3 Installation 2.3

This section explains how the ETC board shall be prepared for use.

The ETC is designed for installation in a standard Intel Multibus backplane with a 86-pin connector (P1) and a 60-pin connector (P2). The ETC board installation is shown in figure 2.

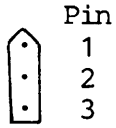
The +5Volt, +12Volt, and -12Volt power sources required by the ETC board, are supplied through the Multibus backplane.

2.3.1 Jumper Configuration

The ETC board is provided with a number of jumpers. The location and orientation of the jumpers are shown in figure 3.

The jumper fields are orientated like IC´s and in references to jumper pin numbers the pins are regarded as IC pins.

In case of single row jumper fields the pins are read as:



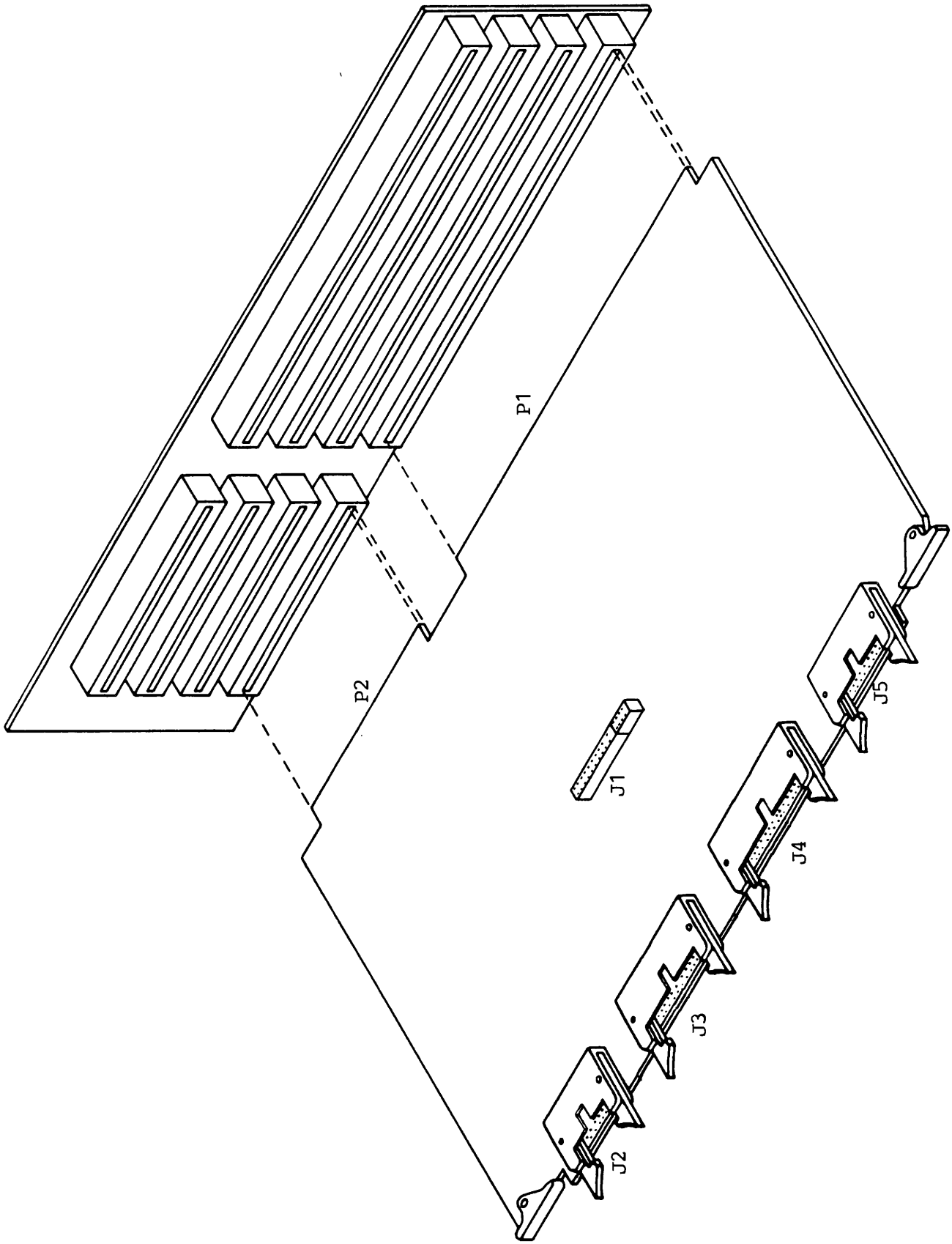
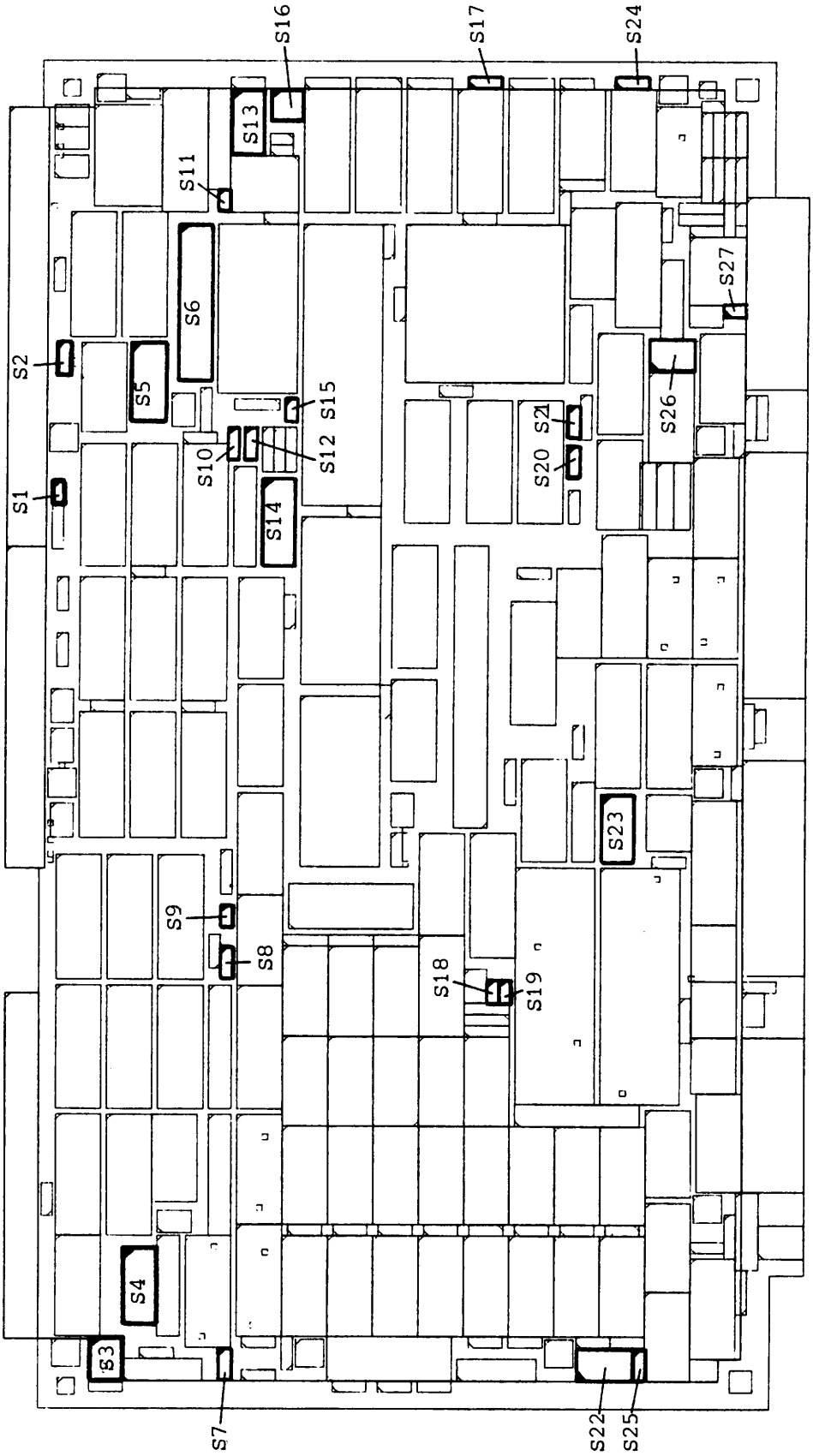


Figure 2: ETC board interconnections.



Figur 3 ETC STRAPS

In the following it is shown how to configure the ETC jumper fields.

S1 2 1

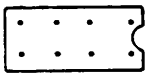
If jumper S1 is installed address bit F hexadecimal is connected to the EPROM sockets. This is necessary when 64 Kbytes EPROM is needed.

Default: No jumper installed.

S2 3 2 1

This jumper in conjunction with jumper field S17 determines the Multibus interface arbitration options. Refer to figure 4.

S3 4 3 2 1



5 6 7 8

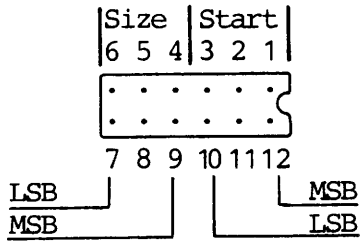
This jumper field makes it possible to decode the 4 topmost Multibus addressbits. When the 4 jumpers are installed the ETC board can be placed in a 1 Mbyte Multibus address segment according to the basevalue obtained from strap area S22. If the total system addressspace is 1Mbyte no jumpers are installed.

Default: No jumpers installed.

Interface State	Jumper Connect	CBRQ/ State	ANYRQST State	Description
1	S2 1->2 S17 2->3	LOW	LOW	The bus Arbiter that has control of the Multibus interface retains control unless a higher priority master deactivates BPRN/ or unless the next machine cycle does not require the use of the Multibus interface. It may then relinquish to a lower priority device.
		HIGH	LOW	The Bus Arbiter that has control of the Multibus interface retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
2 Default Value	S2 1->2 S17 1->2	LOW	HIGH	The Bus Arbiter that controls the Multibus interface surrenders control to the Bus Arbiter that is pulling CBRQ/ low, regardless of its priority, upon completion of the current bus cycle.
		HIGH	HIGH	The Bus Arbiter controlling the Multibus interface retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low the conditions are as described above.
3	S2 2->3 S17 1->2	LOW	HIGH	The Bus Arbiter controlling the Multibus interface surrenders the use of the Multibus interface after each transfer cycle.

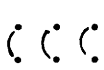
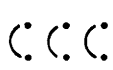
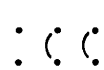
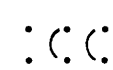
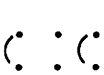
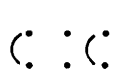
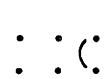
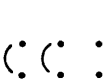
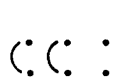
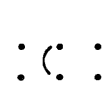
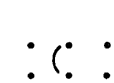
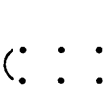
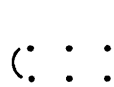
Fig. 4. Multibus Interface Arbitration Options

S4



This jumper fields determines where in the 1 Mbyte Multibus segment the on-board RAM is located if accessed from Multibus. The 1Mbyte segment concerned is determined by S22, and is considered consisting of 8x128 Kbytes segments.

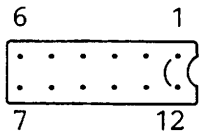
S4 is divided into two functions. The START value chooses a 128 Kbyte start segment. SIZE selects from 1 to 8 segments each consisting of 128 Kbytes.

	SIZE			START	
Jumper Value	Jumper setting	Number of 128Kb segments	Jumper value	Jumper setting	Start addr. within 1Mb base segment
0		1	0		0 0 0 0
1		2	1		2 0 0 0
2		3	2		4 0 0 0
3		4	3		6 0 0 0
4		5	4		8 0 0 0
5		6	5		A 0 0 0
6		7	6		C 0 0 0
7		8	7		E 0 0 0

Size value + START value must always be $\leq$ 7 (see also ex. fig. 8).

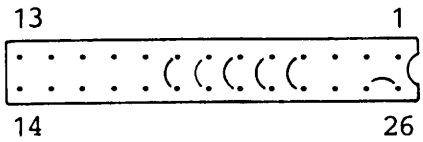
Default value is size = 1 (256 Kbytes), START = 4 (8000H)

S5

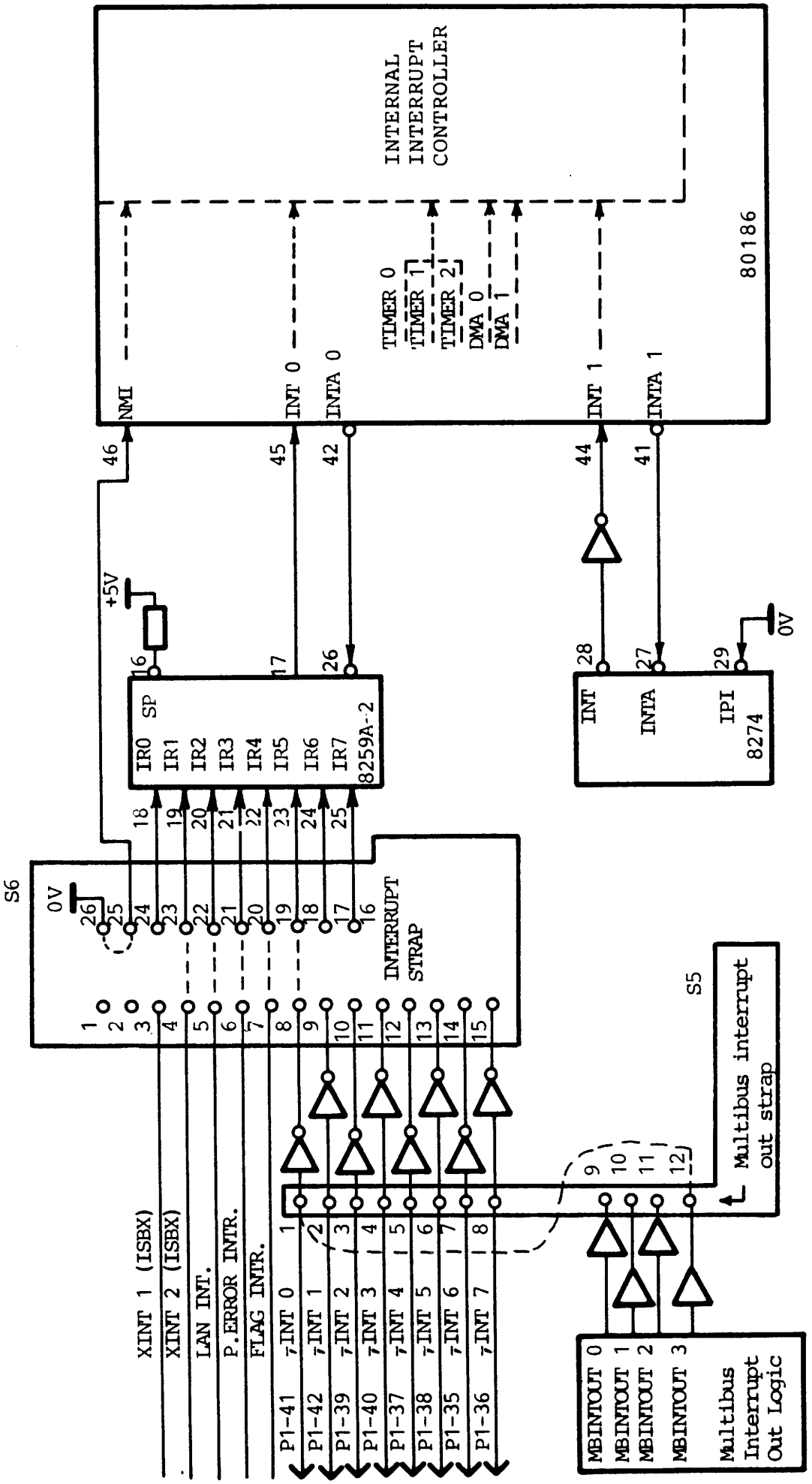


Multibus interrupt out jumpers see figure 5.
Default jumpers shown as dotted lines.

S6

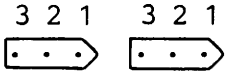


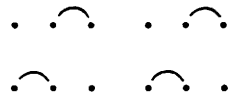
Interrupt jumpers; see figure 5.
Default jumpers shown as dotted lines.



Figur 5 Interrupt Strap og Multibus interrupt out Strap

S7 and S8





64Kx1 chips

256Kx1 chips

These jumper fields controls the memory bank select lines dependent whether the ETC is equipped with 64Kx1 memory chips or 256Kx1 chips.

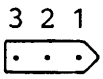
Default value is set in accordance with mounted kind of chips.

S9

When jumper S9 is installed the decoding of reset address xxxx:0400 hex is connected to the CPU reset circuit. This implies that writing the reset location from multibus, resets the ETC board.

Default: S9 is installed.

S10



Multimodule chip select for the iSBX interface. See figure 6.

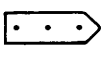
Default: 1 is connected to 2, which is used to connect FDC601.

S11

With this jumper installed the BUS PRIORITY OUT (BPRO) signal is connected to Multibus. The jumper is only removed in systems with parallel priority.

Default: S11 is installed.

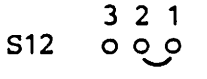
S12



Multimodule chipselect for the iSBX interface. See figure 6.

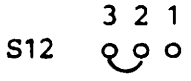
Default: 1 is connected to 2, which is used to connect FDC601.

PCS 4 active and Address bits 5, 4 used



PCS 4 Interval	ADDRESS BITS 6 5 4 3 2 1 0	FUNKTION
0200H to 027FH	X 0 0 M M M X	MCS0, MCS1 for 16-bits transfers (16 Bits boards).
	X 0 1 M M M X	MCS0 for byte/word transfers (8/16 Bits boards).
	X 1 0 M M M X	MCS1 for byte/word transfers (8/16 Bits boards).
	X 1 1 M M M X	No Function

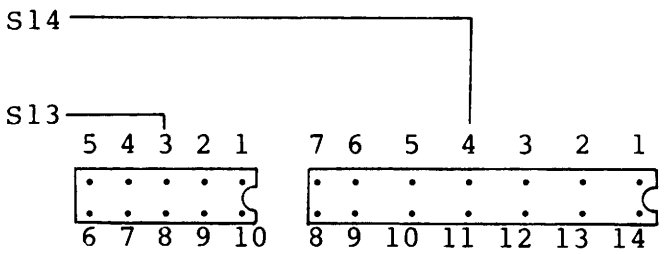
PCS 4 active and Address bit 0, $\overline{LBHE}$ used



PCS 4 Interval	ADDRESS BITS 6 5 4 3 2 1 0 $\overline{LBHE}$	FUNKTION
0200H to 027FH	X X X M M M 0 0	MCS0, MCS1 for 16-bits transfers (16 Bits boards).
	X X X M M M 0 1	MCS0 for low byte transfers (8/16 Bits boards).
	X X X M M M 1 0	MCS1 for high byte transfers (16 Bits boards)
	X X X M M M 1 1	No Function

Figure 6 Strap S10 and S12

Multimodul Chip Select



S13 and S14 select the Multibus addresses, which in an I/O write operation clears the ETC Multibus interrupt out latches.

When a jumper is installed it means that the address bit concerned must be "1" to activate the reset of the latches.

The function of the S13 and S14 jumper fields is shown in the following examples:

S13	S14	Reset addresses
. . . . .	. . . . .	0000 -> 000F
. . . . .	. . . . .	
. . . . .	. . . . .	2000 -> 200F
. . . . .	. . . . .	
. . . . .	. . . . .	AB20 -> AB2F
. . . . .	. . . . .	

Note that it is the Multibus data lines 0:1 that select which Multibus interrupt out latch is cleared on a I/O write (refer to sec. 3)

Default reset address is 2000H.

S15

When jumper is installed the 80186 CPU HOLD signal is tied to 0 Volt. The jumper must be installed if the ETC board is used without the 82586 LAN controller installed.

Default: No jumper installed.

S16

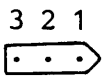
If 1 -> 4 is connected the Multibus Bus Clock is supplied from the ETC board.

If 2 -> 3 is connected the Multibus Constant Clock is supplied from the ETC board

This jumper field must be left empty if other multibus masters supplies these clock signals.

Default: 1 -> 4 connected
2 -> 3 connected

S17



This jumper in conjunction with jumperfield S2 determines the Multibus interface arbitration options.

Refer to figure 4.

S18

If jumper is installed the iSBX signal OPT1 is controlled from the 8255 PPI (Port C bit 1).

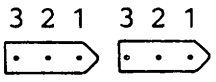
Default: Jumper installed.

S19

If jumper is installed the iSBX signal OPT0 is controlled from the 8255 PPI (port C bit 0)

Default: Jumper installed.

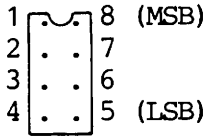
S20
S21



S20 and S21 selects the transmit and receive clock signals for the MPSC 8274 channel A. These clocks may be supplied from either on-board Timer (2 -> 3) or from the connected line (1 -> 2). Refer to figure 7.

Default: 1->2 connected.

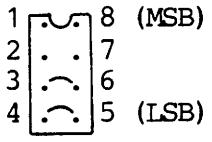
S22



The S22 jumper fields determines in which 1 Mbyte segment (out of 16) in total Multibus address space the RAM memory is located, when accessed from Multibus.

If S22 is treated as a 4 bit number and jumper installed means 1, the S22 jumper field directly selects the 1 Mbyte segment.

EX:



Here Megabyte segment number 3 is selected.

Default: Mbyte segment 0 (S22 empty).

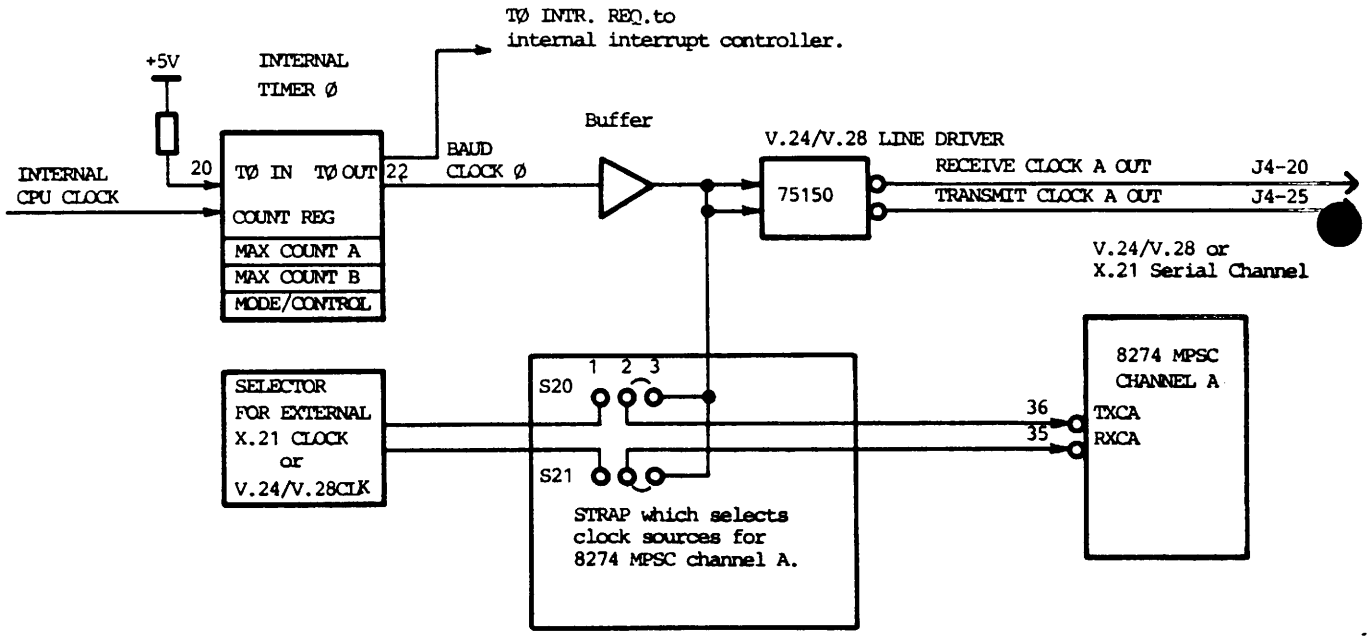
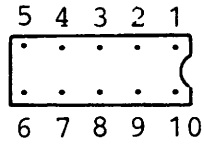


Figure 7 Strap 20 and 21

S23



This is a selftest configuration jumper field used by the power up selftest.

Pins 5,6 and 4,7:

128Kbytes RAM installed.

256 Kbytes RAM installed.

512 Kbytes RAM installed.

1Mbyte RAM installed.

Pins 3,8:

Master selftest board.

Slave Selftest board.

Pins 2,9:

Normal test mode

Chip select test mode.

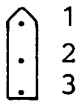
Pins 1,10:

80186 is a 6 MHz CPU

80186 is a 8 MHZ CPU

Default: 256 Kbytes RAM, Master board, Normal test mode, 8 MHz CPU.

S24



1 -> 2 connected if MSI601 micronet expansion board or 82501 ESI steps B, C installed.

2 -> 3 only if 82501 ESI step A installed.

Default: 1 -> 2 connected.

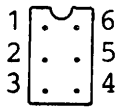
S25

If 1 -> 2 connected the iSBX signal MDRQT (Multimodule DMA request) is able to request the 80186 DMA channel 0. The request is only recognized if 8255 PPI Port C bit 2 = "0". This feature is used by the FPD601 iSBX board.

2 -> 3 must be connected when no iSBX board is installed.

Default: 1 -> 2 connected.

S26



This jumper field determines which 64 Kbytes segments are considered onboard when making RAM accesses. Access of not onboard RAM generates a Multibus access.

Jumper Value	Jumper Setting	Onboard 64K Segments
0		0-1
1		0-1-2-3
2		0-1-2-3-4-5
3		0-1-2-3-4-5-6-7
4		0-1-2-3-4-5-6-7 8-9
5		0-1-2-3-4-5-6-7 8-9-A-B
6		0-1-2-3-4-5-6-7 8-9-A-B-C-D
7		0-1-2-3-4-5-6-7 8-9-A-B-C-D-E-F

All RAM is onboard, segment F is EPROM.
To get a Multibus window min. 64 Kbytes (segment E) the jumper value must not exceed 6.
Default: Jumper value 1 which gives 4 64Kbytes segments onboard.

NOTE: If S26 strapvalue considers onboard segments that does not actual exist, (not physically installed) this may cause wraparound errors in RAM accesses, and an erronous Multibus configuration table during power up.

S27 

If jumper is present the shield in the Local Area Network cable is connected to 0 Volt. Otherwise the shield is left open in the ETC board end.

Default: No jumper installed.

2.3.2 Memory Resource Configuration

The onboard 80186 CPU total address space is 1M byte. This address space is divided into 4 parts as shown in figure 8:

- EPROM
- Multibus window
- Private memory
- Dualport memory

The installed onboard RAM (128 Kbytes, 256 Kbytes, 512 Kbytes, or 1 Mbytes) is divided into dualport and private RAM.

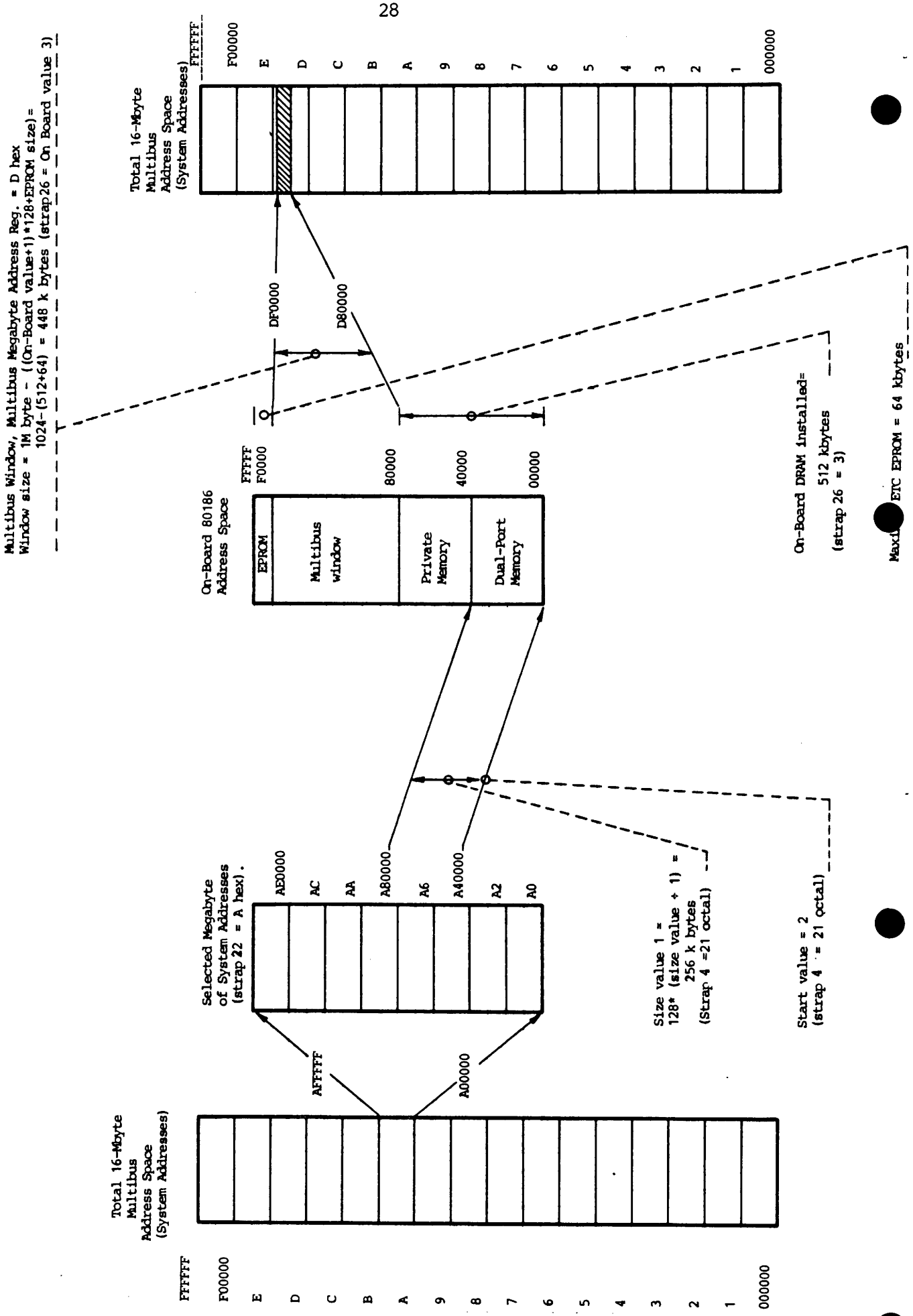
The dualport RAM can be accessed from both the Multibus and the 80186 CPU. The dualport RAM is onboard located from address 0 and upwards. The onboard RAM that can only be accessed from either 80186 CPU or Multibus is called private memory. The EPROM is always located from address FFFFFH and downwards. The rest of the 1Mbyte address space not occupied by EPROM, 80186 private memory, and dualport memory gives the Multibus window for offboard accesses.

Jumper Field S26 (see section 2.3.1) determines the amount of 80186 accessible onboard RAM (dualport + 80186 private). If number of segments here selected are less than number of RAM segments installed, it gives the special possibility of Multibus private RAM; that means onboard RAM that can only be accessed from offboard devices.

Jumper Field S22 (see section 2.3.1) determines in which (out of 16) 1 Mbyte Multibus segment the dualport memory (and in special case the Multibus private RAM) is located. Note that S22 is only effective if S3 (see section 2.3.1) has jumpers installed.

Jumper field S4 (see section 2.3.1) determines where in the 1 Mbyte Multibus segment the dualport memory (and in special case the Multibus private RAM) is located.

Although figure 8 refers to the 80186 CPU, it is also valid for the 82586 coprocessor, with the exception that the 82586 is capable of addressing the entire 1Mbyte RAM address space i.e. also the portion shadowed by the EPROM´s (since 82586 accesses EPROM using its address bit 14H ="1"). This does also imply that the multibus window as seen from the 82586 includes the EPROM space shown in figure 8.



Figur 8 Strap 22, 4, 26
Memory resource
configuration example

2.3.3 EPROM Installation 2.3.3

The ETC board can be configured with one of three EPROM types 2764 (8 Kbytes), 27128 (16 Kbytes), and 27256 (32 Kbytes). The ETC board must be installed with two EPROM of the same kind.

If 27256 types are installed the jumper field S1 must have jumper installed otherwise not.

The EPROM´s are inserted in sockets u34 and u35. Odd byte EPROM (Bits F:8) is installed in u35.

2.3.4 RAM Expansion Module Installation 2.3.4

The ETC board may be supplied with a RAM expansion module as shown in figure 9.

The following procedure should be followed:

1. Remove RAM chips located at sockets u100 and u101. Remove latches 74S373 located at sockets u11 and u20.

2. Insert the RAM expansion module MEX601/611 in the sockets u100, u101 and u20. Fix the MEX board to the ETC board by use of six 3 mm screws and three spacers.

3. Insert the previous removed components into the corresponding sockets (RAM chips in u21 and u22, 74S373 in u19 and u20) on the MEX601/611.

The configuration of the jumper-fields S7 and S8 (see section 2.3.1) must be maintained according to the RAM chips in use.

2.3.5 LAN Interface Installation 2.3.5

The interface to the Local Area Network can be either a micronetinterface MSI601 or an Ethernet (IEEE802.3) interface 82501 ESI.

The Ethernet interface chip 82501 is installed in socket u69. Observe that the orientation of the chip is correct.

The MSI601 expansion board is installed in u69 and fixed by the use of four spacers and eight 3 mm nylon screws. (see figure 10).

Jumper field S24 (see section 2.3.1) must be configured according to the interface installed in u69.

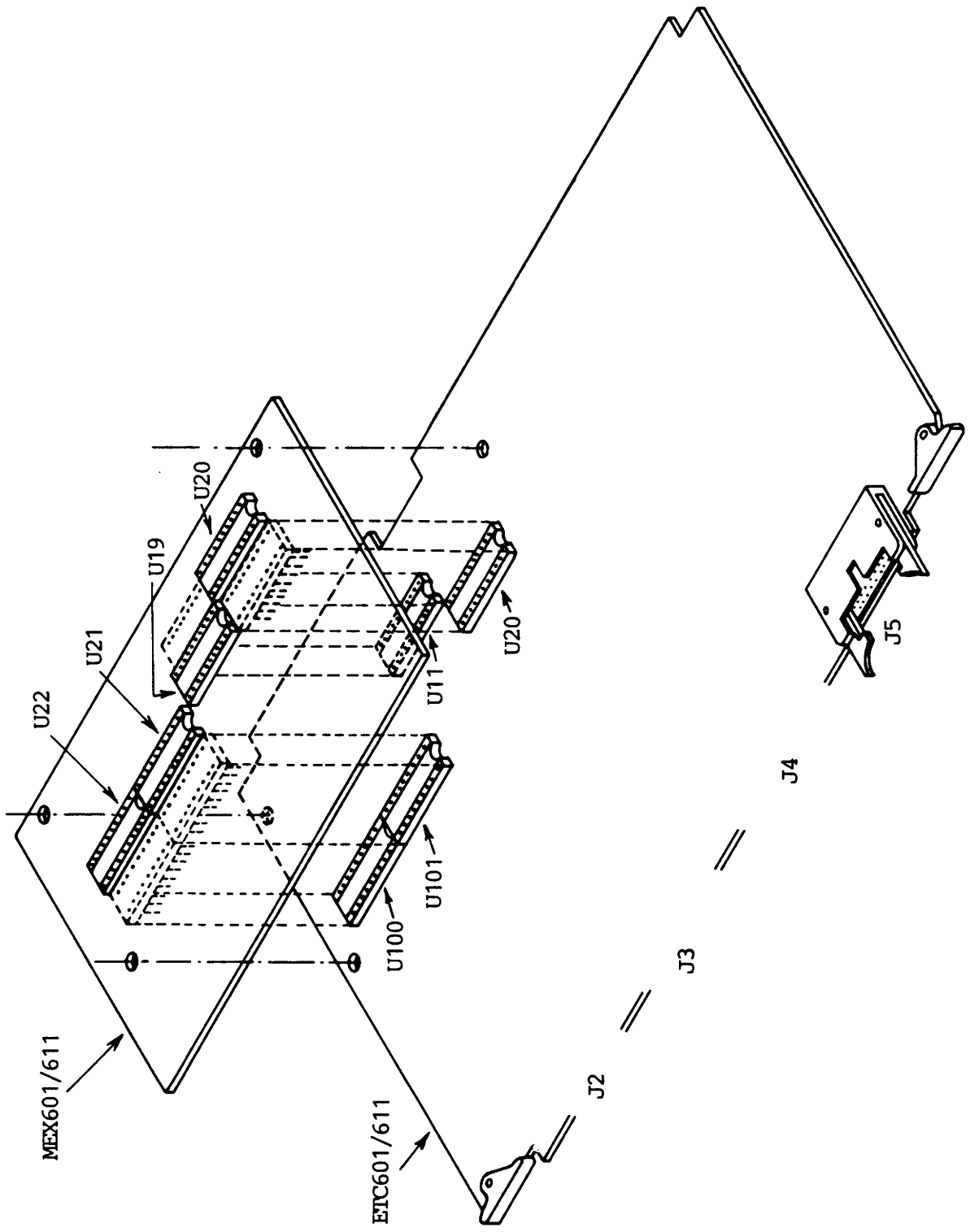
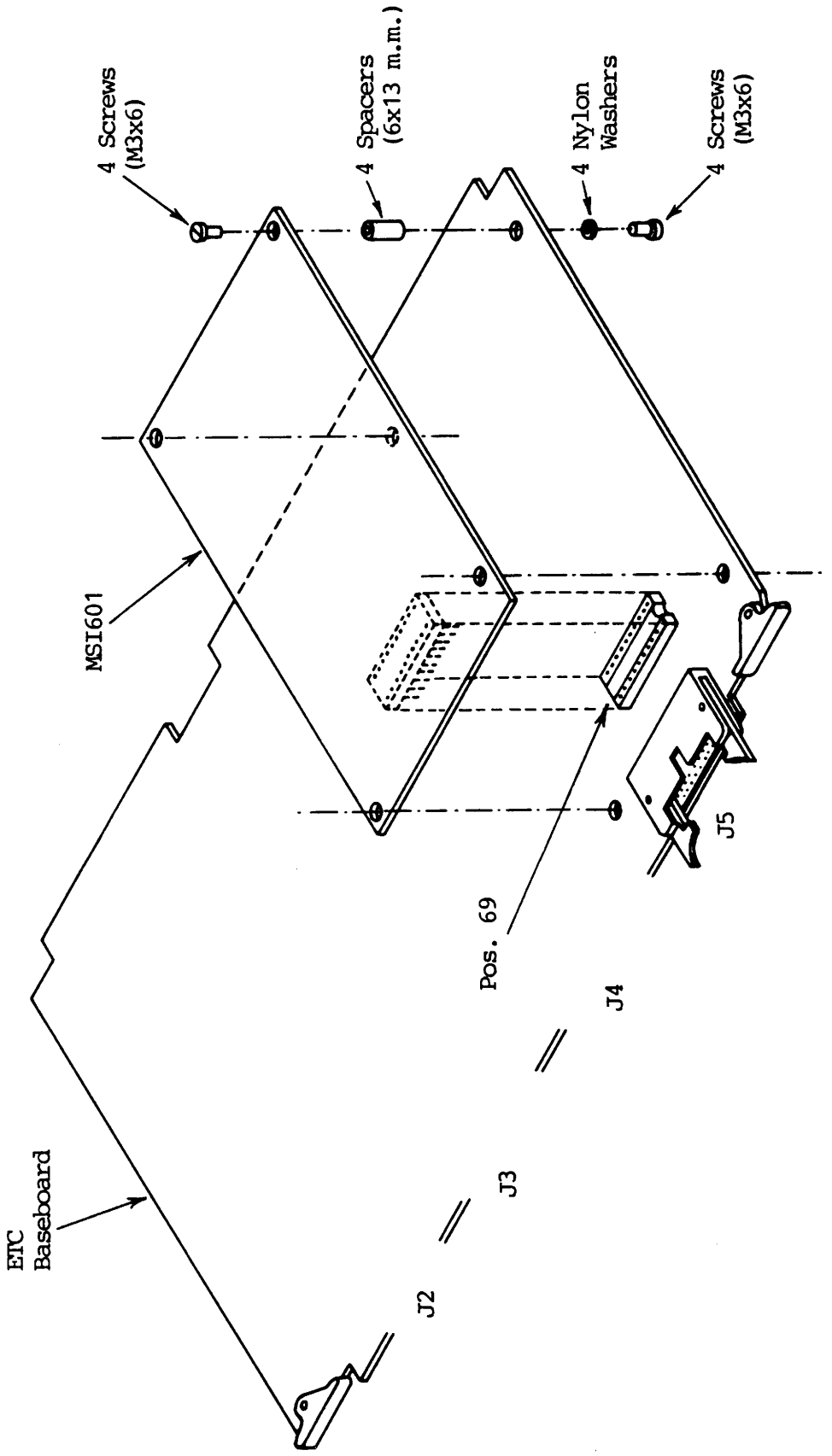


Fig.9 Inserting Memory Expansion Module



Micronetinterface Installation

Fig. 10

2.3.6 iSBX Multimodule Installation 2.3.6

The ETC board is provided with an iSBX multimodule connector, J1. A single wide or a double wide iSBX multimodule may be installed. It must be ensured that the increased power requirements are satisfied. The iSBX multimodule manual should be consulted. Both 8-bit and 16-bit wide iSBX boards may be installed.

The following installation procedure should be followed:

1. Locate pin 1 on the iSBX bus connector (P1) and align it with pin 1 of the iSBX connector J1 on the ETC board. Press the two boards together.

2. Fix the iSBX board to the ETC board by the use of a spacer and two nylon screws. In case of a double wide iSBX board to additional spacers and 4 screws are needed to fix the board.

After installing the iSBX module the jumper fields S6, S10, S12, S18, S19 and S25 (see sec. 2.3.1) must be configurated according to the iSBX module installed.

2.4 Selftest 2.4

The ETC board may be equipped with an EPROM contained selftest program as described in ref. (7). Including this selftest-program as a power up test in the EPROMS installed, is a convenient way of checking the ETC board before use.

The testprogram includes the following tests:

Simple Bustest	a part of the initialisation.
Prom Checksum Test	a simple PROM checksum is calculated.
RAM Memory Test	a modulus 3 patterns test of the board resident memory.
Chip Select Test	a test that generates chip selects to all peripheral devices.
RAM refresh Test	a test that verifies the function of the RAM refresh logic.
80186 Timer Test	a test of the onchip 80186 timers.
80186 DMA Test	a test of the two 80186 DMA channels.
Interrupt test	a test of the onboard interrupt system by generating a flagbyte and a timer interrupt.
Multibus Interrupt Test	a test that generates an onboard interrupt via Multibus.
iSBX Test	a test of the iSBX interface by driving a floppydisk interface FDC601.
i8274 Test	a test of the 8274 channel A.
Ethernet Test	a test of the LAN interface including the 80586 LAN controller.

For detailed description of the selftest program refer to (7).

3. PROGRAMMING INFORMATION 3.

3.1 Introduction 3.1

The ETC601/611 Ethernet Controller contains several programmable devices, including an INTEL 80186 microprocessor and an INTEL 82586 local communications controller. The 80186 and 82586 are the key elements of the Ethernet Controller. Section 3.2 and 3.3. contains information on the use of the 80186 and 82586 which is relevant for the programmer of the Ethernet Controller. Detailed programming information may be found in "Microprocessor and Pheripheral Handbook, Intel 1983", ref. (1) and "LAN Components User's Manual", ref. (2). The programmable peripheral devices, which are also described in detail in ref. (1), are:

- Intel 8259A-2 Interrupt Controller
- Intel 8274 Multi-Protocol Serial Controller
- Intel 8255A-5 Programmable Peripheral Interface

Section 3.5 to 3.8 provides the necessary programming information for the above mentioned devices, however, programming information is not given in detail, only the information which is relevant for the application of these devices in connection with the Ethernet Controller. It is therefore recommended to consult ref. (1) and (2) while reading this paper.

Section 3.4 describes memory configuration, memory addressing of the Ethernet Controller and how to access these resources.

3.2 Intel 80186 Processing Unit 3.2

The Ethernet Controller is equipped with an Intel 80186 microprocessor (8MHz), ref. (1). The 80186 is a high integration 16-bit microprocessor. On the chip is integrated:

- Exchanged 8086-2 CPU.
- Clock generator.
- Programmable Memory and Peripheral Chip-Select Logic with programmable Wait State Generator.
- 2 Independent, High-Speed DMA channels.
- Programmable Interrupt Controller.
- 3 Programmable 16-bit Timers.

3.2.1 Internal Control Block

All of the 80186 integrated peripherals are controlled via 16-bits registers contained within an internal 256-byte CONTROL BLOCK.

The control block base address is programmed via a 16-bit RELOCATION REGISTER also contained within the control block at offset FEH from the base address of the control block. The relocation register provides 12-bits of the base address of the control block, i.e. bits 19 through bits 8. The base address of the control block must be on an even 256-byte boundary, i.e. the lower 8 bits (bit 7-0) of this address are all zeroes. The control block may be mapped into memory or I/O space controlled by bit 12 of the relocation register.

After reset of 80186, the relocation register is set to:

20FFH.

This causes the base address of the control block to become:

FFOOH in I/O space.

Bits 19-16 of control block base address must be programmed as 0 if the control block shall be located in I/O space. The location of any register contained within the control block is determined by the current base address of the control block. An offset map of the control block is shown in figure 11.

DEVICE	REGISTER	HEX ADDRESS
BASE ADR	RELOCATION REGISTER	FE
DMA CHANNEL 1	CONTROL WORD	CA
	TRANSFER COUNT	C8
	DESTINATION POINTER (UPPER 4 BITS)	C6
	DESTINATION POINTER	C4
	SOURCE POINTER (UPPER 4 BITS)	C2
	SOURCE POINTER	C0
DMA CHANNEL 0	CONTROL WORD	DA
	TRANSFER COUNT	D8
	DESTINATION POINTER (UPPER 4 BITS)	D6
	DESTINATION POINTER	D4
	SOURCE POINTER (UPPER 4 BITS)	D2
	SOURCE POINTER	D0
MEMORY AND PERIPHERAL CHIP SELECT	MEMORY/PHERIPHERAL CHIP SEL.	A8
	MID-RANGE MEMORY CHIP SEL (BASE ADR)	A6
	PERIPHERAL ADR. CHIP SEL. (START ADR)	A4
	LOWER MEMORY CHIP SEL.	A2
	UPPER MEMORY CHIP SEL.	A0
TIMER 2	MODE/CONTROL WORD	66
	NOT AVAILABLE	64
	MAX COUNT A	62
	COUNT REGISTER	60
TIMER 1	MODE/CONTROL WORD	5E
	MAX COUNT B	5C
	MAX COUNT A	5A
	COUNT REGISTER	58
TIMER 0	MODE/CONTROL WORD	56
	MAX COUNT B	54
	MAX COUNT A	52
	COUNT REGISTER	50
INTERRUPT CONTROLLER NON-IRMX 86 MODE	INT 3 CONTROL REGISTER	3E
	INT 2 CONTROL REGISTER	3C
	INT 1 CONTROL REGISTER	3A
	INT 0 CONTROL REGISTER	38
	DMA 1 CONTROL REGISTER	36
	DMA 0 CONTROL REGISTER	34
	TIMER CONTROL REGISTER	32
	INTERRUPT STATUS REGISTER	30
	INTERRUPT REQUEST REGISTER	2E
	IN-SERVICE REGISTER	2C
	PRIORITY MASK REGISTER	2A
	MASK REGISTER	28
	POLL STATUS REGISTER	26
	POLL REGISTER	24
	EOI REGISTER	22
	NOT USED	20
	NOT USED	00

Figure 11 INTERNAL CONTROL BLOCK REGISTER MAP.

Note , in connection with the ETC, the internal control register block must not be mapped into memory space. The ETC is designed to have the internal control register block mapped into I/O space. Following base addresses of the internal control block are available:

FC00, FD00, FE00 and FF00

Note that the default value after power on or reset is also available (FF00H corresponding to relocation register equal to 20FFH).

3.2.2 Memory Space/Memory Chip Select

80186 access of memory resources is done using a two component address composed of a 16-bit base segment and a 16-bit offset. Base values are contained in one of four internal segment registers of the 80186. A 20-bit physical address is calculated by shifting the base value left by four bits and adding the offset value to the shifted base value. A 20 - bit physical address allows for 1-Mbyte physical address size. In connection with the Ethernet Controller, this address space can be partitioned into:

- ON-BOARD EPROM SPACE
- ON-BOARD DRAM SPACE
- OFF-BOARD MULTIBUS WINDOW

80186 provides memory chip select for 3 address areas:

- UPPER MEMORY
- MID-RANGE MEMORY
- LOWER MEMORY

Only upper Memory Chip Select (UMCS) is used with the ETC. UMCS is used as chip select for the EPROM memory area. The EPROM may start in 3 different start addresses depending on the type of EPROM mounted in the two 28-pins EPROM sockets of the ETC. The upper memory chip select register - offset AOH in internal control block - should be programmed as indicated in figure 12. Note that upper limit of UMCS is always FFFFFH.

UMCS HEX VALUE	EPROM START ADDR HEX VALUE	EPROM BLOCK SIZE IN K-BYTES	EPROM TYPE	WAIT STATES
FC38	FC000	16	2764	0
F838	F8000	32	27128	0
F038	F0000	64	27256	0

Fig. 12. ETC upper memory chip select

Note that after RESET of 80186 the UMCS register is set to:

FFFBH

This corresponds to start address

FFF00H and 3 wait states

The number of wait steps inserted when accessing on-board RAM is 1. (Determined by hardware and not programmable). The number of wait steps inserted when accessing multibus resources is depending on the accessed slave-device and the time required to gain access to the Multibus. The Multibus is requested and surrendered via an INTEL 8289 bus arbiter.

3.2.3 I/O Space/Peripheral chip Select 3.2.3

The I/O space of the ETC consists of 64K 8-bit or 32K 16-bit ports. The I/O space can be partitioned into 3 sub I/O spaces.

HEX I/O ADDRESS	SUB I/O SPACE ADDRESSED
0000 - 03FF	On-board peripheral devices. Note that addresses from 00F8H to 00FFH are reserved by Intel.
0400 - FBFF	Off-board peripheral devices addressed via multibus interface
FC00 - FFFF	Available I/O space for 80186 internal devices i.e. internal control block.

Fig. 13. ETC SUB - I/O SPACES

The 80186 can generate chip select for up to seven peripheral devices, which are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address must be programmed into the Peripheral Address Chip Select register of the internal Control block (PACS-offset A4H). Some bits in the Memory/Peripheral Chip Select register of the internal control block (MPCS-offset A8H) relates to peripheral functionality, and these bits must also be programmed. The 80186 can also generate a READY signal internally for each of the Peripheral Chip Select lines (PCS0 to PCS6). The number of wait states to be inserted is programmable to provide 0-3 wait states. In addition it is possible to either ignore external READY or to operate the external ready generator in parallel with the internal ready generator. The three least significant bits of PACS sets the PSCO-PSC3 ready mode, the three least significant bits of MPCS sets the PCS4-PCS6 ready mode. After power on or reset both PACS and MPCS must be accessed before the peripheral chips select lines will become active. In connection with the ETC, the PACS and MPCS registers must be programmed as follows:

MPCS = 80BAH which corresponds to

- MPCS bits 14-8 all zero = Mid-range block size 0 (not used in the ETC).

- MPCS bit 7 = EXT = "1", 7 PCS lines available.
- MPCS bit 6 = MS = "0", Peripherals mapped into I/O space.
- MPCS bits 2-0 = 0,1,0 = ready mode for PCS 4-6, 2 wait states and external ready used.

PACS = 0039H which corresponds to

- PACS bits 15-6 all zero = Base address 0000H.
  PCS 0 active from 0000H to 007F H
  PCS 1 active from 0000H to 00FF H
  PCS 2 active from 0100H to 017F H
  PCS 3 active from 0180H to 01FF H
  PCS 4 active from 0200H to 027F H
  PCS 5 active from 0280H to 02FF H
  PCS 6 active from 0300H to 037F H
- PACS bits 2-0 = 0,0,1 = ready mode for PCS 0-3, 1 wait state and external ready used.

Section 3.5 in this chapter describes the use of the peripheral select lines.

3.2.4 DMA Channels

3.2.4

The 80186 DMA controller provides two independent DMA channels. Each channel have six registers in the internal control block (fig. 11), which defines the operation of the channels.

The registers are:

- Source Pointer 20 Bits
- Destination Pointer 20 Bits
- Transfer Counter (Byte count) 16 Bits
- Control Word 16 Bits

Each DMA channel control word determines the mode of operation for the channel in question.

Data transfers can occur between memory and I/O space or within the same space. Typical in the ETC the transfer is between Memory and I/O space. Each data transfer consumes 2 bus cycle, one cycle to fetch data (4 clocks + min. 1 wait step) and one cycle to store data (4 clocks + min. 1 wait step).

Source, Destination and Transfer Count registers must be programmed before the start/stop bit in the Con-

trol Word is set to start.

Upon reset of the 80186, the start/stop bit for each DMA channel is reset to stop, and eventually transport in progress is aborted.

In the ETC the DMA channels are used by the Intel 8274 Multi-Protocol Serial Controller and the iSBX interface. DMA channel 0 is shared between the 8274 channel A transmitter and the iSBX interface. DMA channel 1 is used by the 8274 channel A receiver. A select signal, which originates from the INTEL 8255A-5 Programmable Peripheral Interface, assigns DMA channel 0 to either the 8274 channel A transmitter or the iSBX interface. Provided the 8255A-5 is correctly initialized, typical routines for the assignment of DMA channel 0 is given in figure 14 and 15.

```
;       XDMA1 assigns DMA 0 to 8274
;       Destroys DX and AL
 XDMA1 : MOV DX, 106H   ;  Point DX at 8255
                           Control word

          MOV AL, 05H   ;  Output control word =
          OUT DX, AL    ;  Set Port C bit 2 = "1"
```

Fig. 14. Assign DMA channel 0 to 8274

```
;       XDMA0 assigns DMA 0 to iSBX
;       Destroys DX and AL
 XDMA0  :  MOV DX, 106H; Point DX at 8255
                         Control word

            MOV AL, 04H ; Output control wrd =
            OUT DX, AL  ; Set Port C bit 2 = "0"
```

Fig. 15. Assign DMA channel 0 to iSBX

3.2.5 Interrupts/Internal Interrupt Controller 3.2.5

The interrupt pointer table occupies up to the first 1 kbyte of low memory. The table may contain up to 256 pointers, which defines an interrupt routine for each interrupt. The interrupt pointer table is indexed by using the interrupt vector, multiplexed by four.

Table entries 0 through 31 are reserved. Within this area resides:

*	Divide Error	interrupt vector type 0
*	Single Step	interrupt vector type 1
	Non Maskable	interrupt vector type 2
*	Breakpoint	interrupt vector type 3
*	Overflow	interrupt vector type 4
*	Array Bounds	interrupt vector type 5
*	Unused-Upcode	interrupt vector type 6
*	ESC Opcode	interrupt vector type 7
	Timer 0	interrupt vector type 8
	Timer 1	interrupt vector type 18
	Timer 2	interrupt vector type 19
	DMA 0	interrupt vector type 10
	DMA 1	interrupt vector type 11

The 80186 can service interrupts generated by SOFTWARE (marked *) or HARDWARE . Software interrutps are not described in this paper at all. Vector types within the reserved area cannot be changed, they are fixed. The internal peripheral devices generate the vector code through the 80186 internal interrupt controller, while the software interrutps and the non-maskable hardware interrupt (NMI) use internally supplied vectors.

The 80186 internal interrupt controller can receive interrupt from both internal and external sources. Internal interrupt sources are Timers and DMA channels. External interrupt sources are NMI-interrupt and 4 interrupt pins. In connection with the ETC the internal interrupt controller must be set to cascade mode, in this mode the 4 interrupt pins are configured into interrupt input/dedicated acknowledge pairs. One pair is used to interface to an 8259 A Programmable Interrupt Controller (PIC), while the other pair is used for the 8274 Multi-Protocol Serial Controller (MPSC). Refer to fig.16. In the ETC interrupt system two levels of priority are created, requiring priority resolution in the 80186 internal

interrupt controller and the external 8259A PIC or the 8274 MPSC. If an external interrupt is serviced one IN-SERVICE bit (IS bit) is set at each of the two levels, and when the interrupt service routine is completed two end-of-interrupt commands must be issued by the programmer, i.e. one to the internal interrupt controller (Internal Control Block EOI reg. offset 22H) and one to the external interrupt controller. Refer also to section 3.6 for description of 8259A PIC and section 3.7 for description of the 8274 MPCC.

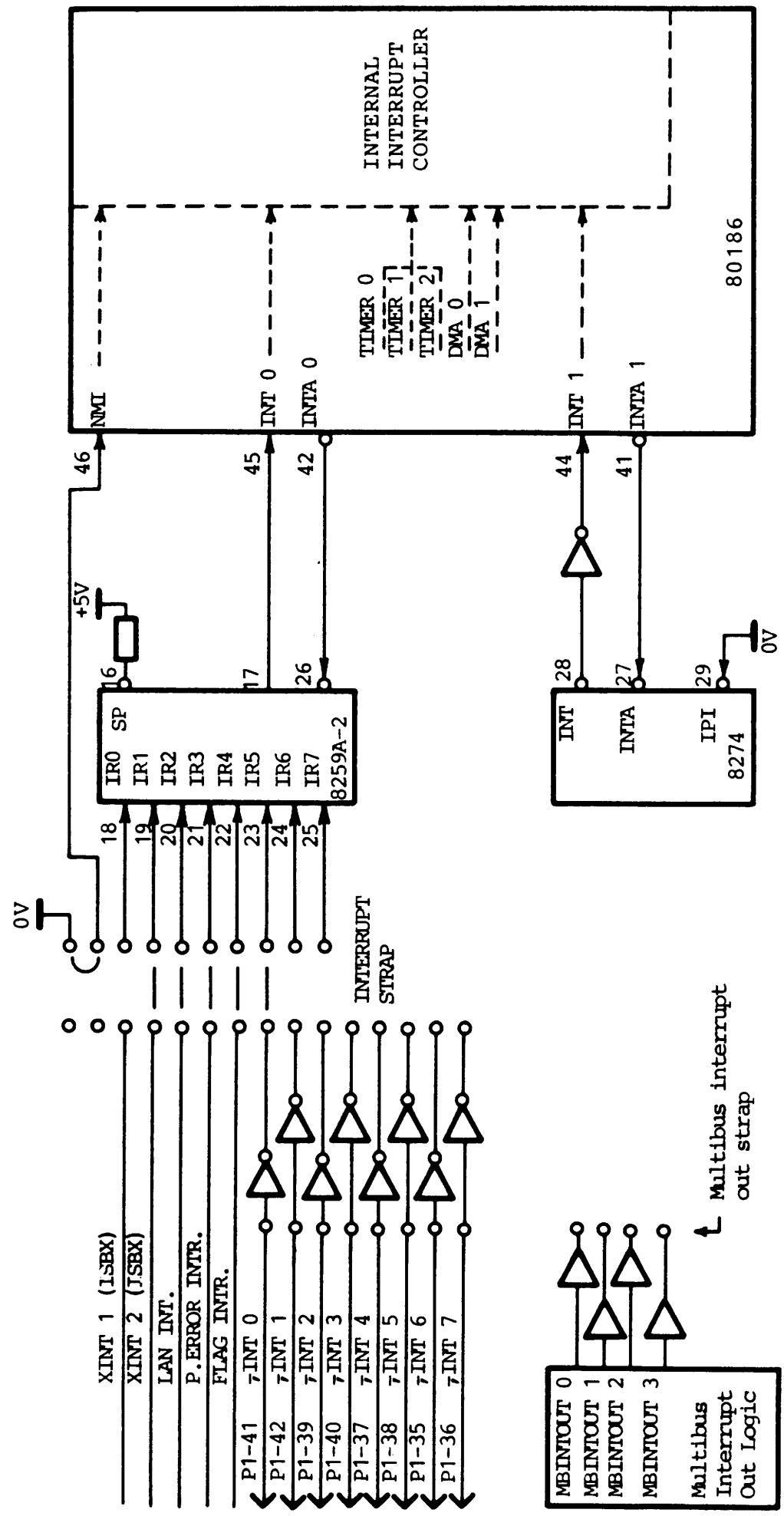


Fig. 16 ETC Interrupt System

As mentioned above the internal interrupt controller must be set to cascade mode, which implies that control registers for INT2 and INT3 are not used. Control registers for INT0 and INT1 must be set to:

- INT0 CONTROL REGISTER = 002XH
- INT1 CONTROL REGISTER = 002YH

This corresponds to:

- Not special fully nested mode.
- Cascade mode.
- Edge triggered, (it is also possible to use level triggered mode).

X and Y denotes mask and priority information for INT0 and INT1. The priority levels of interrupt sources to the internal interrupt controller are all programmable except for the Non-Maskable interrupt (NMI). The NMI interrupt prevent the maskable interrupts from being serviced.

3.2.6 Internal Timers

3.2.6

The 80186 provide three internal 16-bit programmable timers. Two of the timers each have four registers in the internal control block, while the third timer has three registers. The registers are:

- Mode/Control Word.
- Max Count B (not present in timer2)
- Max Count A.
- Count Register.

Any access to the timer register add one wait state to the four-clock bus cycle.

The value of the Count Register is incremented for each timer event, and after reaching the Max Count, the Count Register is reset. The timer can be programmed either to run continously or to halt upon maximum count. If only a single Max Count regiser is used, timer output pin will become low for one clock period, 2 clock periods after reaching max count. Timer 0 and 1 have two Max Count registers, and can be programmed to alternate between Max Count A and Max Count B. Swithching occurs when Count Register reaches max count. The timer output pin will indicate

which Max Count register is currently in use (high level if A). The Two Max Count registers makes it possible to generate square waves and pulse output of any duty cycle.

The timers can operate at speeds up to one-quarter the CPU-clock (2Mhz for an 8Mhz CPU clock, 1.5Mhz for a 6Mhz CPU clock). Timer 0 and 1 input/output are connected to external pins, while timer 2 is not connected to any external pin. Timer 2 is useful for real-time coding and time delay application. In addition timer 2 can be used as prescaler to the other two, or as a DMA request source (disabled and enabled via the control word of the DMA channel).

Via the Mode Control register it is possible to program the operation or to check the current programmed status of the timers. Short description is given in figure 17.

In connection with the ETC, the timers are used as indicated below and in figure 18:

- Timer 0 V.24/V.28 Receive/Transmit clock DTE source. Useful for test purpose or if DTE must supply transmit/ receive clock.

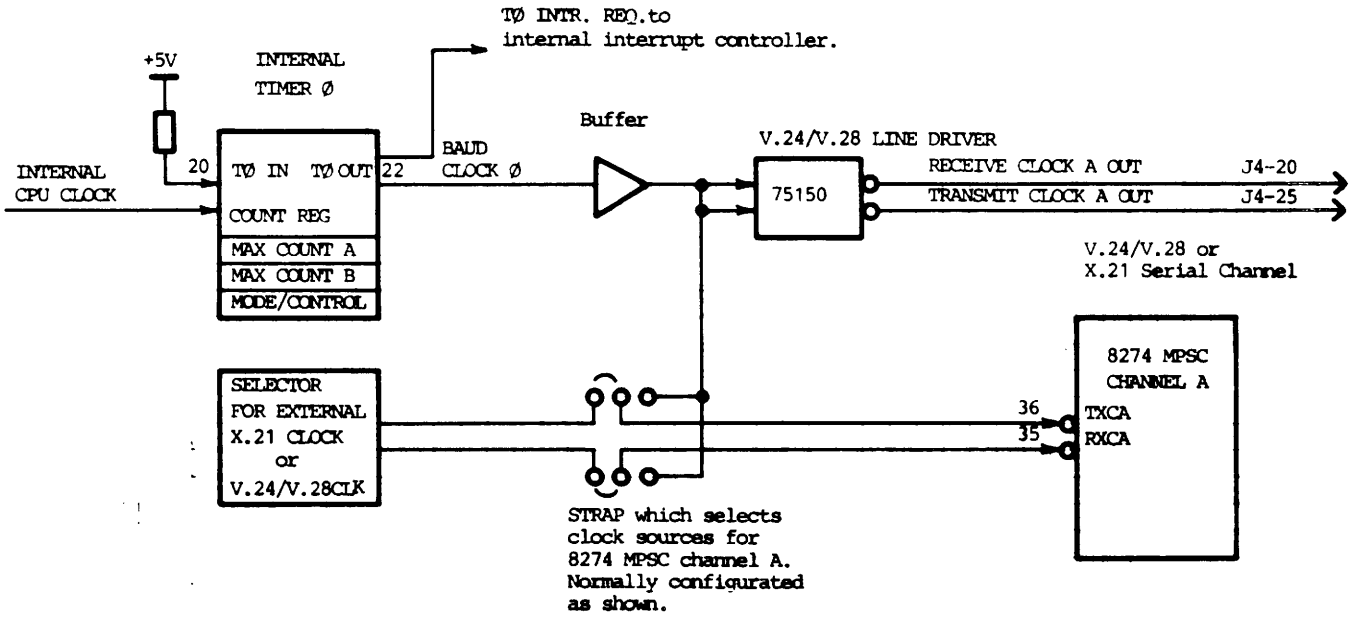
- Timer 1 Baud rate clock for console serial channel.

- Timer 2 Real-time coding. Delay applications.

*ALT (1)	0 Max Count Reg. A always used. 1 Alternate between Max Count A/B.
CONT (0)	0 Halt on max. count (A = max or A and B = max). 1 Run continously
*EXT (2)	0 Use internal CPU clock, use external input pin for control (function of external pin controlled by RTG bit). 1 Use external clocking.
*P (3)	0 Count one-fourth of CPU clock. 1 Use timer 2 as prescaler.
*RGT (4)	Only active if EXT = 0. 0 Level of external input pin gates internal count clock on and off. 1 External input pin detects low-to-high transitions, which starts timer.
EN (15)	0 Timer is inhibited from counting. External input pin transitions ignored. 1 Enable counts subject to external pin constraints in internal clock mode. (EXT = 0, RGT valid).
INH (14)	0 EN bit unaffected by write to Mode/Control. 1 EN bit is updated during write to Mode/Control Word.
INT (13)	0 Disable timer interrupt. 1 Enable timer interrupts on max. count.
MC (5)	0 Max count not reached. 1 Max Count reached, programmers intervention required to clear MC.
*RIU (12)	0 Max Count reg. A currently in use. 1 Max Count reg. B currently in use.

(x) x = Bit number in Mode/Control Word
* = These bits are hardwired to 0 in TIMER 2.

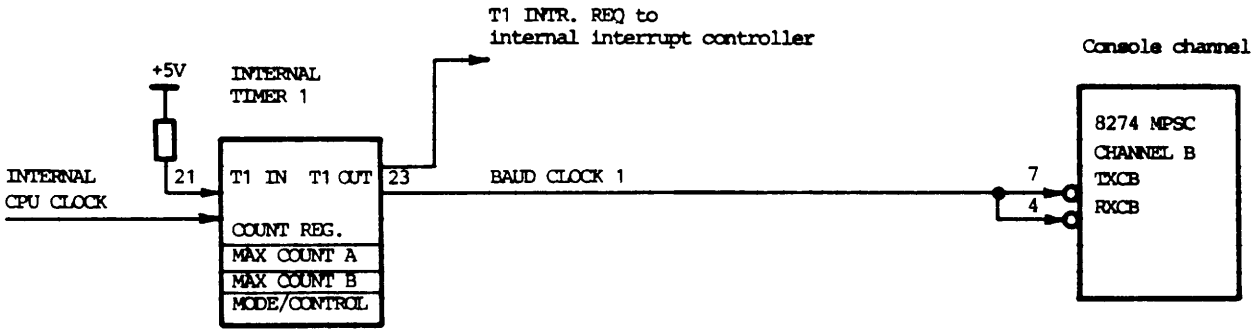
Fig. 17. Mode/Control Word of Internal Timers.



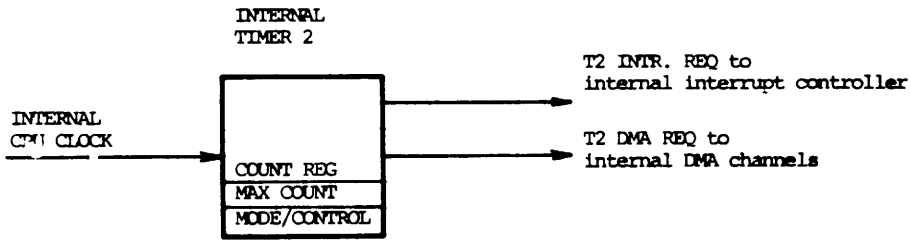
Initialize TIMER Ø to

- Max Count A= Max Count B= one half of Baud Rate period
  eks baud rate 300 baud, 6 Mhz CPU clock Max Count A/B = 2500_{10}
  2500 x 2 x 0,67µs = 3.333 ms = 300 baud

- Mode/Control Word = C003h
  Enable Count, Alternate between Max count A and B, Run continousty.



Initialize Timer 1 as described for TIMER Ø.



Use Timer 2 for real-time coding and delay application.

ETC601/611 Figure 18 Timer System in the ETC

A14734

3.2.7 Multiplexed Bus Arbitration

The Intel 80186 processing unit of the ETC shares its local bus with a co-processor the Intel 82586 Local Communications Controller. An exchange mechanism is provided through a HOLD REQUEST/HOLD ACKNOWLEDGE system. The 82586 generates the HOLD request when it needs the multiplexed bus, and the 80186 issues HLDA when the bus can be used by the 82586.

A HOLD request is the highest-priority activity the 80186 may receive, higher than instruction fetching or internal DMA cycles.

3.3 Intel 82586 Local Communications Controller

The Intel 82586 LCC is in the ETC used as an Ethernet, Cheapernet and RC Micronet controller. The 82586 LCC is an intelligent LCC, which relieves the 80186 microprocessor of many of the tasks accociated with Local Area Networks. It performs framing, link management, data modulation and also supports a network management interface.

The 82586 LCC and the 80186 CPU communicate through a shared memory space. There is no I/O port access to the 82586 LCC. The only direct control lines between the 80186 CPU and the 82586 LCC are the LAN INTERRUPT to the CPU and the CHANNEL ATTENTION (CA) to the LCC.

The LCC and the CPU connects to the same local bus - the multiplexed bus. An exchange mechanism is provided through a HOLD REQUEST/HOLD ACKNOWLEDGE system. The LCC uses two internal 16-byte FIFO's to buffer data to and from the multiplexed bus. Therefore, once a HOLD REQUEST is granted (by HOLD ack) the LCC is able to transfer multiple bytes of data with each HOLD request. Figure 19 is a blockdiagram of the Local Area Net system.

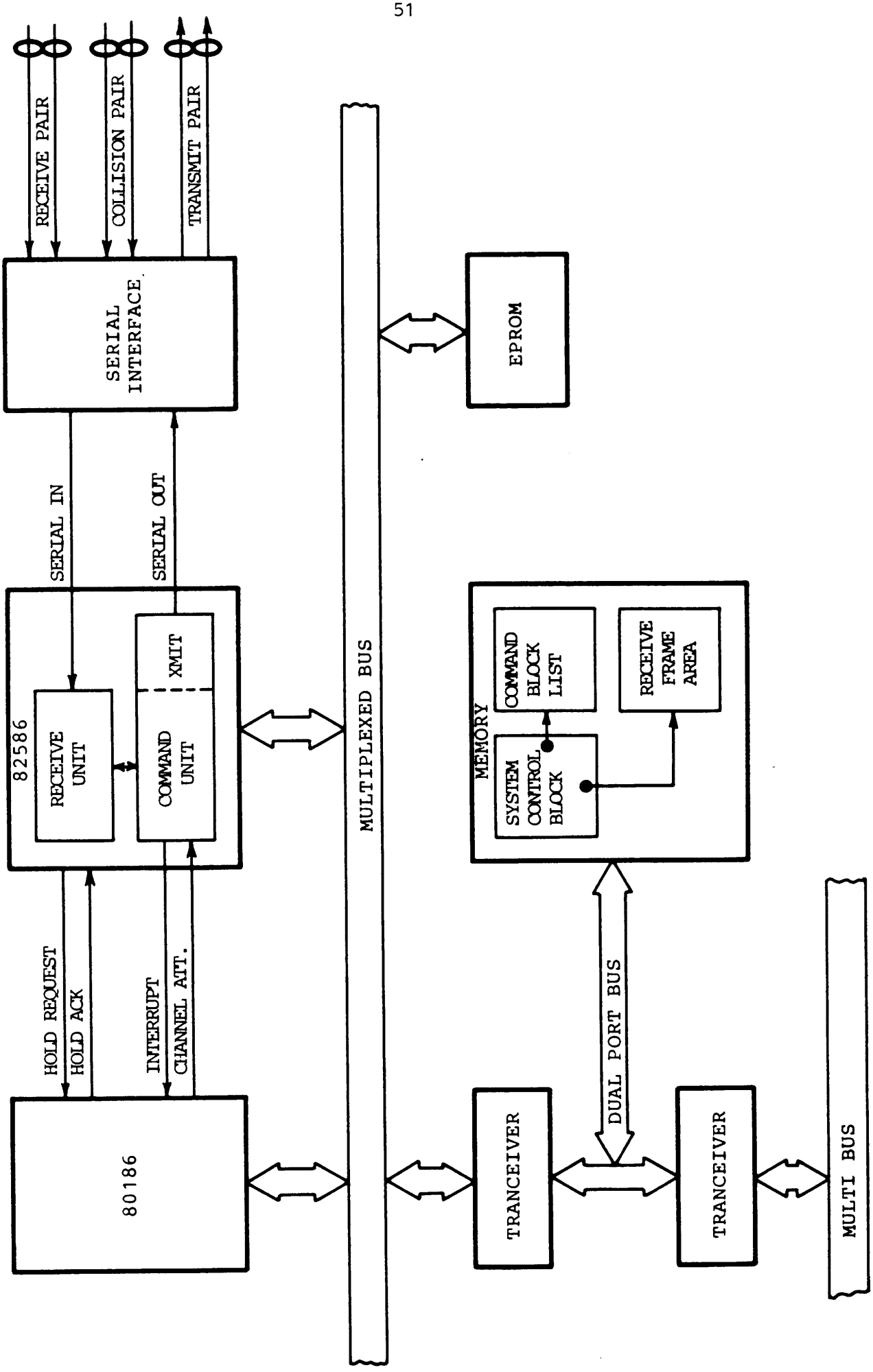


Figure 19 ETC LAN SYSTEM.

3.3.1 82586 Memory Structures

There are five memory structures used by the 80186 CPU and the 82586 LCC (figure 20):

- The System Configuration Pointer (SCP)
- The Intermediate System Control Pointer (ISCP)
- The System Control Block (SCB)
- The Command Block List (CBL)
- The Receive Frame Area (RFA)

The CPU sets up these structures in the shared memory.

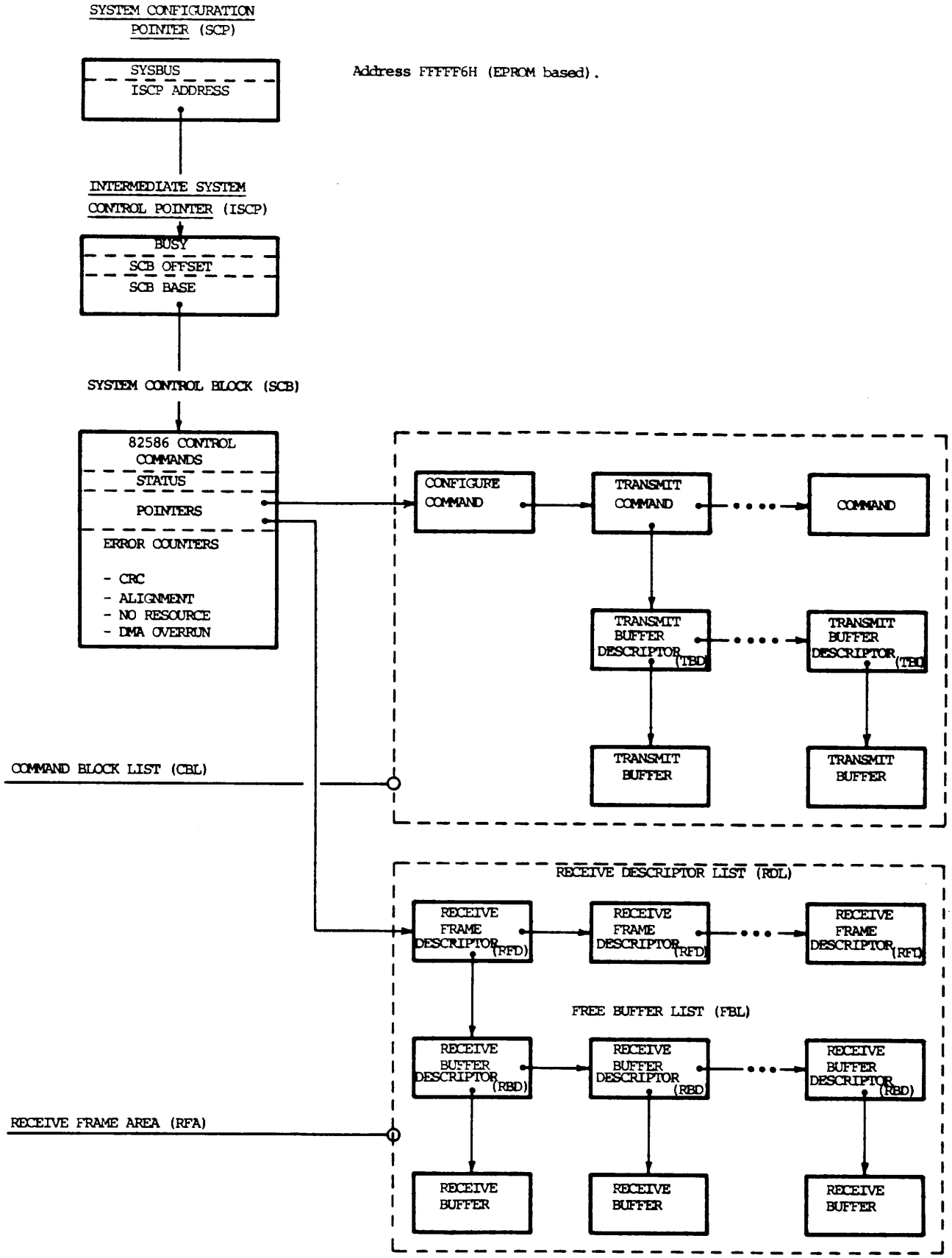
The SCP is located in EPROM and begins at location FFFFF6H . SCP specifies the width of the multiplexed bus and the address of the ISCP.

The ISCP is located in DRAM, and specifies the address of the SCB, besides this address, the ISCP contains a BUSY flag indicating that 82586 LCC is being initialized.

The SCB contains control commands, status registers, pointers to CBL and RFA, and error counters for CRC, Alignment, DMA Overrun and No Resource errors. By means of the SCB the 82586 LCC is able to report status and error counts to the 80186 CPU, execute programs contained in the Command Block List and store incoming frames in the Receive Frame Area.

The CBL is a list of Commands to be executed by the 82586. The commands contained in the CBL are called "Action Commands". The generalized form of a Command Block contains command status, command code link field, parameter field. By means of the link field commands can be chained to form the CBL. The parameter field contains parameters for the command or results from the command.

The RFA consists of a Receive Descriptor List (RDL) and a list of free buffers called the Free Buffer List (FBL). The 82586 stores destination address, source address, type field and status of each frame received in the individual Receive Frame Descriptors (RFD) of the RDL. The data portion of the frame is stored in the first free data buffer on the FBL, which is pointed to by the current RFD.



ETC601/611

Figure 20 82586 LCC MEMORY STRUCTURES

A14735

3.3.2 82586 Memory Addressing

The 82586 LCC can access memory by 24-bit addresses. There are two types of 24-bit address:

- Real addresses (Physical addresses must be even)
- Segmented addresses (must be even)

The real address is a single 24-bit entity, used primarily to address transmit or data buffers. The real address is equal to start address of the memory area that contains the buffer.

The segmented address uses a 24-bit base, and a 16-bit offset. A physical segmented address is generated by adding base and offset. The segmented address form is used for all Command Blocks, Buffer Descriptors, Frame Descriptors and System Control Blocks.

A 24-bit physical address allows for 16-Mbyte physical address space, however, the entire address space is not utilized in connection with the ETC. The space used can be partitioned into:

- ON-BOARD EPROM SPACE
- ON-BOARD DRAM SPACE
- OFF-BOARD MULITBUS WINDOW

The 82586 LCC uses address bit 14H = "1" to access EPROM. EPROM start address values as seen from the 82586 LCC must be as listed in figure 21. Top address of EPROM is always FFFFFFH.

Caution: The 82586 LCC addresses from FF0000H-FFFFFFH are the only 82586 addresses greater than one megabyte which are allowed in connection with the ETC. Failure to observe this when programming may cause start of unintentional RAM cycle or multibus access requests.

EPROM START ADDR. HEX VALUE	EPROM BLOCK SIZE IN K-BYTES	EPROM TYPES	WAIT STATES
FFC000	16	2764	0
FF8000	32	27128	0
FF0000	64	27256	0

Fig. 21. EPROM Start Address for 82586 LCC

Maximum ON-BOARD DRAM space as seen from the 82586 LCC is 1-Mbyte. Note that the 82586 LCC is able to access the entire DRAM space, while the 80186 CPU cannot access the amount of DRAM, which is defined by the Upper memory Chip Select.

Wait states when accessing RAM = 1

The 82586 is also allowed to access off board memory resources via the multibus interface.

The number of wait states inserted when accessing the Multibus is depending on the accessed memory and the time required to gain access to the multibus. The multibus is requested and surrendered via an INTEL 8289 arbiter.

Note that 82586 LCC is not able to generate LOCK signal to 8289 arbiter or multibus. It is emphasized that the 82586 LCC cannot be controlled by a multibus master, since the interrupt and channel attention signals are routed to the on-board 80186 CPU. However, the memory structures used by the 80186 CPU and the 82586 to pass control, status and data may reside in off-board memory, since the 82586 can prevent the 80186 CPU from gaining access to the Multibus via the HOLD request/HOLD acknowledg mechanism, while the 80186 CPU may lock the multibus memory via the LOCK function (A HOLD request is not acknowledged during a locked transfer). The 82586 may not be able to transmit/receive at full speed when using external memory. Note that the system configuration Pointer, which is EPROM based, must reside in local EPROM.

3.3.3 Channel Attention/Interrupt Handshake Mechanism

As mentioned the 80186 CPU and the 82586 LCC communicates via shared memory and the CHANNEL ATTENTION/INTERRUPT handshake mechanism.

Channel Attention signal to the 82586 LCC is generated using an I/O Write or I/O Read command to any of the following I/O addresses:

0300H - 037FH

The 82586 LCC may interrupt the 80186 CPU via an onboard 8259A Programmable Interrupt Controller. This interrupt, which is called LAN INTERRUPT, passes a strap field thus making interrupt sources and priority levels user selectable and configurable. Refer to figure 16 and section 3.6.

After reset of the 82586 LCC the LAN INT. pin is inactive and the 82586 LCC waits for CHANNEL ATTENTION (CA). The 80186 CPU may now start the initialization procedure, by setting up the SCP (EPROM based), ISCP and the SCB structures, set BUSY flag in ISCP to 01H and issue a CA signal to the 82586 LCC. Upon this CA the 82586 LCC reads the SCP at location FFFFF6 (figure 20). The SYSBUS byte of SCP is fetched in byte mode. SYSBUS byte determines the width of the multiplexed data bus (16-bits, SYSBUS = 00H). Once bus width is determined, all further memory transfers are word transfers. After SCP access, the 82586 fetches the ISCP, saves the SCB base and offset address and clears BUSY flag in the ISCP. It also clears the command word in SCB, sets interrupt event status in SCB and interrupts the 80186 CPU (LAN INT. active), hereafter the initialization sequence is terminated and the 82586 waits for CA.

The purpose of the initialization sequence is to bring the 82586 LCC into a well defined idle state and to locate the SCB.

After initialization, the 80186 CPU must establish the structures Command Block list for the Control Unit (CU) and Receive Frame Area for the Receive Unit (RU). It then writes the "Control Commands" for the CU and RU (typically starting). The 82586 LCC is started using the Channel Attention signal. The CU executes "Action Commands" from the command Block List and may be set to interrupt the 80186 CPU upon

completion of the commands of the list.

The RU of the 82586 handles all activities related to frame reception and interrupts the 80186 when a frame has been received. Before the 82586 issues interrupts it sets interrupt event status in the SCB. The 80186 acknowledges interrupts by writing acknowledge bits into the SCB and then commands the 82586 to examine the SCB via the Channel Attention signal.

3.3.4 82586 Reset

3.3.4

The 82586 may be reset in any of three ways:

- Via the Multibus INIT signal
- Via a Multibus Memory Write Command
- Via an I/O Write Command from the 80186 CPU.

The Multibus INIT signal resets the entire ETC to a known state, the signal is generated upon power-on. A Multibus Memory Write Command to a specific ETC DRAM address does also reset the entire ETC. The reset address is:

RESET ADDRESS = XY0400H

As seen from the Multibus the X ciffer selects a 1-Mbyte segment out of the total multibus address space (16-Mbyte), while the Y ciffer (which must be even - 128K boundaries) selects a start address within the 1-Mbyte segment.

An I/O Write Command from 80186 to a specific I/O address does also reset the 82586. The reset address is:

82586 RESET ADDRESS = 0184H

Note that in order to obtain a sufficient reset pulse width it is necessary to change the Peripheral Address Chip Select register to 003BH (3 wait states inserted) before the 82586 reset command is issued.

Note the 82586 uses 10 system clocks to execute any reset. This time is automatically generated in case of reset via Multibus INIT or Multibus Memory Write Command. However, in case of reset via 82586 reset address the 80186 must wait at least 10 system clocks

before issuing Channel Attention to trigger the initialization procedure.

Caution:

The software reset operation via reset bit in SCB, as explained in ref. (2), is recommended not to be used, due to a 82586 malfunction.

3.3.5 82586 Serial Interface

An 82501 ESI (Ethernet Serial Interface) or a MSI 601 (Micronet Serial Interface) can be connected to the serial interface of the 82586 LCC. The 82501 ESI or the MSI601 provides the programmer with an interface towards the Ethernet/Cheapernet or the RC micronet. The 82501 ESI/MSI601 are controlable only via the 82568 LCC with the exception of the LOOPBACK signal (see section 3.8.3). Conserning MSI601 consult ref. (8).

3.4 Memory Addressing

3.4.1 Multibus-Master Accessing Dual-Port RAM

ETC board provides you with the ability to relocate the On-Board Dual-Port memory to any 1 Mbyte segment (out of 16) in the Multibus address space. This is done by means of strap 22.

The 1 megabyte segment selected by strap 22 may be subdivided using the start/size value strap 4. The 1 megabyte segment is considered as consisting of eight 128Kbyte segments and the start value strap (3-bits) selects one of these segments as a start segment while the size value strap (3-bits) selects from 1 to 8 segments. The amount of on-board RAM available to the multibus-master can be expressed as:

RAM size = 128 * (size value + 1) kbytes

It is emphasized that following expression must be fullfilled when adjusting the start/size strap:

(size value + start value) $\leq$ 7

If the expression is not fullfilled it is not possible to read/write in ETC RAM from multibus.

Independent of the start segment selected this segment will always be located in the first 128 Kbyte of on-board memory.

For a Multibus-master executing write access to ETC dual-port RAM there are two important addresses:

ETC RESET ADDRESS = XY0400hex
ETC INTERRUPT ADDRESS = XY0402hex

Accessing these location causes either the ETC to be reset (same function as Multibus INIT signal) or the on-board 80186 CPU to be interrupted.

When the ETC is slave it locks its dual-port memory to the multibus when it is addressed and the multibus LOCK/ signal is active (low).

A mapping example is shown in figure 25. From left to right this example shows that the 1 megabyte segment selected by strap 22 starts with address A00000hex and ends with address AFFFFFhex. Start value in the selected 1 megabyte segment is 2 which corresponds to starting in address A40000hex. Size value is 1 which corresponds to 256 kbytes available to multibus master, and the last address becomes A7FFFFhex. Finally the RAM space is mapped into the on-board RAM space from address 00000hex to address 3FFFFhex.

3.4.2 On Board CPU´s Accessing EPROM

3.4.2

The 80186 CPU as well as the 82586 LCC may access EPROM memory. Two 28-pins EPROM sockets are available for EPROM memory. Figure 22 and 23 shows address space for the possible types of EPROM when accessed by the 80186 CPU (figure 22) or the 82586 LCC (figure 23).

EPROM TYPE	EPROM MEMORY SIZE	EPROM SPACE
2764	16Kbytes	FC000-FFFFF
27128	32Kbytes	F8000-FFFFF
27256	64Kbytes	F0000-FFFFF

Fig. 22. 80186 CPU Accessing EPROM

EPROM TYPE	EPROM MEMORY SIZE	EPROM SPACE
2764	16Kbytes	FFCOOO-FFFFFF
27128	32Kbytes	FF8000-FFFFFF
27256	64Kbytes	FF0000-FFFFFF

Fig. 23. 82586 LCC Accessing EPROM

It is emphasized that the 82586 addresses listed in figure 23 above are the only 82586 addresses greater than one megabyte which are allowed in connection with the ETC. Failure to observe this when programming may cause start of unintentional RAM cycles or multibus access requests.

The multibus master cannot access on-board EPROM. However, it is possible for the multibus master to access dual-port ram simultaneously with on board CPU´s accessing EPROM memory.

The 80186 CPU uses the Upper Memory Chip Select line (UMCS) as chip select for EPROM area and the upper memory chip select register must be programmed to accomplish this (refer to section 3.2.2.).

The 82586 LCC uses its address bit 14H as a condition for EPROM chip select.

Write access to EPROM locations does not hang up the CPU´s neither do write/read access to EPROM locations which does not exist. However, reading a non-existing EPROM location will result in erroneous data returned to the CPU´s.

It is recommended that an address in the EPROM holds information on the actual EPROM size.

When replacing 2764/27128 EPROM´s with 27256 EPROM´s it is necessary to install one strap (strap S1). From factory 27128 EPROM´s are used.

3.4.3 On Board CPU´s accessing RAM

The ETC may be equipped with either 64Kx1 memory chips or 256Kx1 memory chips which corresponds to 128Kbytes or 512Kbytes of RAM memory. The RAM memory is expandable using RAM expansion modules. (ref. 9).

ETC601	128 kbytes
ETC601 + MEX601 expansion	256 kbytes
ETC611	512 Kbytes
ETC611 + MEX611 expansion	1Mbytes

Note that only the listed combinations are allowed. The amount of RAM memory installed may be read via 8255 PPI port A (refer to section 3.8.1). Read or write access to non-existing RAM locations does not hang-up the CPU´s. One wait state is always inserted when accessing RAM. However read access to RAM locations which does not exist will result in erroneous data returned to the CPU´s.

The 80186 CPU (incl. its integrated DMA channels) and the 82586 LCC may access RAM. Arbitration is accomplished via the HOLD/HOLD ACK request/acknowledge mechanism.

Note that the 82586 LCC and a multibusmaster (strap dependent) is able to access the entire 1M-byte RAM space while the 80186 CPU cannot access the amount of RAM space shaded by the EPROM space i.e. the 80186 will always address EPROM when the upper memory chip select line is active even if maximum RAM memory is installed.

The 80186 LOCK/ signal (active low) is generated by the LOCK prefic instruction and allows the 80186 CPU to execute read-modify-write RAM cycles without the interference of the multibus-master between the read and the write.

The 82586 LCC has no LOCK signal thus the multibus master may gain access to on board RAM between 82586 LCC RAM cycles.

3.4.4 Multibus Access from On Board CPU´s

The 80186 CPU and the 82586 LCC is allowed to access off board memory via the multibus interface.

The Multibus is requested and surrendered via an INTEL 8289 bus arbiter. It is made possible to configurate the Multibus arbitration scheme by means of straps S2 and S17. Refer to GENERAL INFORMATION section 2.3.1. If the 80186 is multibus master it may generate a multibus LOCK/ signal (active low) if a locked bus transfer is required. The Multibus BUSY signal assures mutual exclusion on the Multibus (LOCK signal is also routed to the 8289 arbiter), while the LOCK/ signal allows mutual exclusion to be extended off the bus.

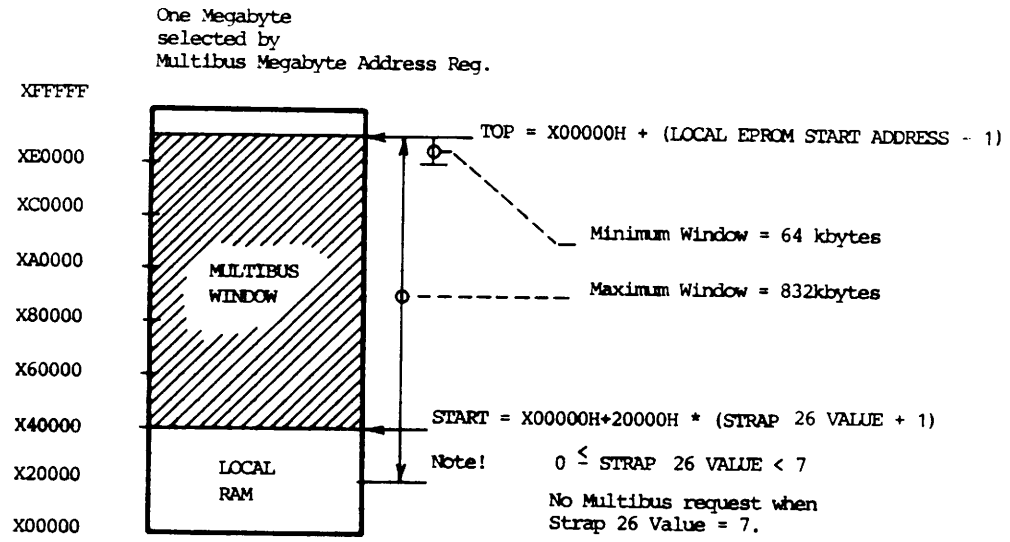
The 82586 LCC has no LOCK signal, and when the 82586 is multibus master it is therefore possible for other masters to gain access to the Multibus between 82586 multibus cycles.

Provisions have been made to configurate the relationship between on-board RAM and off-board RAM. RAM addresses not used on-board are used to address a Multibus window. This multibus window can be relocated to 1 of 16 megabytes of Multibus address space by means of the Multibus Mega-byte Address Register which allow a 4-bit select address to be send along with any 20-bit Multibus address. Refer to section 3.10.3.

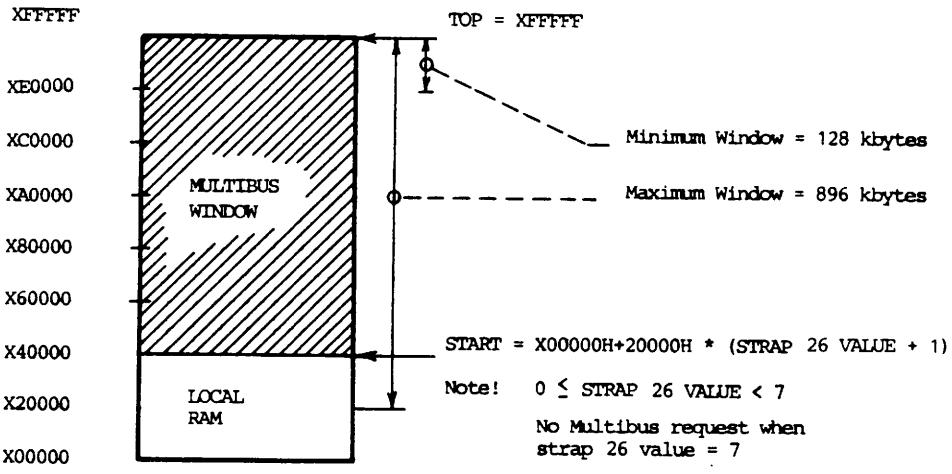
Within the selected megabyte the top address of the Multibus window is determined by the Upper Memory Chip Select register (local EPROM start address - 1) when the 80186 CPU is master, while top address is FFFFFH when the 82586 LCC is master. The Multibus window start address is made variable on 128 Kbytes boundaries by means of strap 26 (3-bits). Refer to GENERAL INFORMATION section 2.3.1. and figure 24.

Accessing a non-existing multibus resource does not hang up the on-board CPU´s due to a hardware timeout circuit. The 80186 CPU is not interrupted due to this

80186 CPU is MASTER, and Multibus Megabyte Address Register = X



82586 CPU is MASTER, and Multibus Megabyte Address Register = X



timeout.

Figure 25 shows an example of Multibus Window mapping. The window is mapped to the 1 megabyte multibus space from D00000 to DFFFFF. Start address within this space is D80000 (strap 26 value = 3).

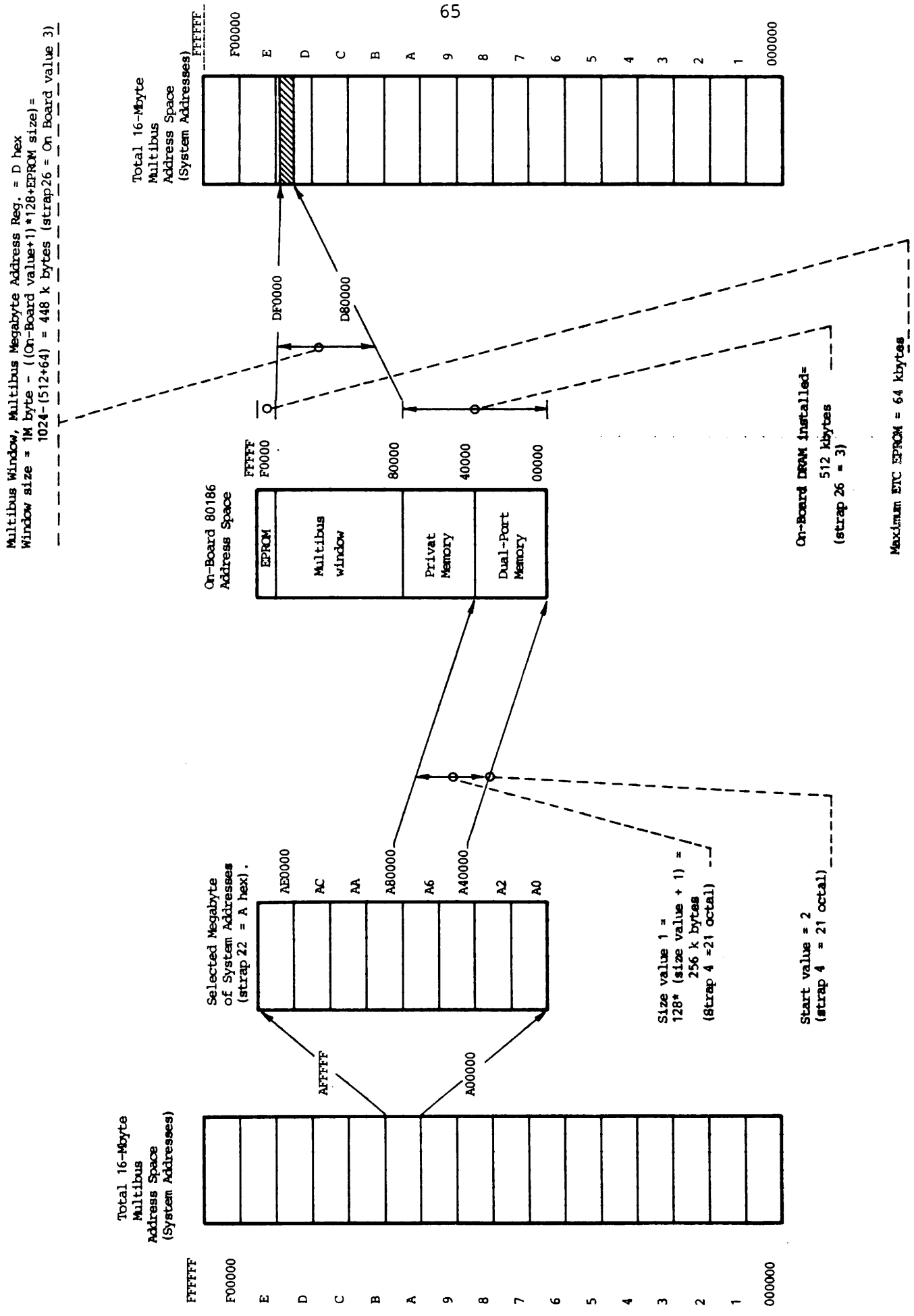


Figure 25 Multibus to Dual-Port mapping and Multibus Window mapping

3.5 On Board Input/Output

The ON-BOARD peripheral devices are located within the I/O address space of the 80186 CPU from address 0000h through 03FFH (refer to figure 13). I/O address decoders operates on 16-bits, and all divices must therefore be addressed using DX register. I/O addresses are assigned according to figure 26. It is emphasized that each of the Peripheral Chips Select lines are active for 128 addresses and that not all of the least significant bits are used in the decoders. Therefore it is possible to activate the devices using other addresses than indicated in figure 26, however, this is not recommended.

DEVICE	HEX ADDRESS	PCS INTERVAL HEX	ADDRESS BITS DECODED IN PCS INTERVAL 6 5 4 3 2 1 0	REQUIRED WAIT STATES	FUNCTION
8259A Interrupt Controller	0000	PCS 0 0000 to 007F	X X X X X 0 0	1	Write: ICW1, OCW2, OCW3 Read : Status and POLL
	0002		X X X X X 1 0	1	Write: ICW2, ICW3, ICW4, OCW1 (mask) Read : OCW1 (mask)
8274 Multi-Protocol Serial Controller	0080	PCS 1 0080 to 00FF	X X X X 0 0 0	1	Write: Channel A Data Read : Channel A Data
	0084		X X X X 1 0 0	1	Write: Channel A Command/Param. Read : Channel A status
	0082		X X X X 0 1 0	1	Write: Channel B Data Read : Channel B Data
	0086		X X X X 1 1 0	1	Write: Channel B Command/Param. Read : Channel B status
8255A Programmable Peripheral Controller	0100	PCS 2 0100 to 017F	X X X X 0 0 0	1	Read : Port A, strap 23 value and size of dual port ram.
	0102		X X X X 0 1 0	1	Read : Port B, iSBX options-Modem Stat. and X.21 Select.
	0104		X X X X 1 0 0	1	Write: Port C, Output to iSBX-DMA control 82501 Loop-Back-Indicators.
	0106		X X X X 1 1 0	1	Write: Control Register
Flag Byte Interrupt	0180	PCS 3 0180 to 01FF	0 X X X 0 0 0	1	Write: Flag Byte Interrupt Clear
	0182		0 X X X 0 1 0	1	Write: Flag Byte Interrupt Set
82586 LCC	0184		0 X X X 1 0 0	3	Write: 82586 LCC Reset Address
Multibus Mega-Byte Addr.Reg.	0186		0 X X X 1 1 0	1	Write: Load Multipus Megabyte Addr. Reg. (Data Bits 3:0)
Interrupts to Multibus and Reset of P. Error FF	01C0		1 X X X X 0 0	1	Write: Set Multibus Interrupts Data Bits 1:0 selects 1 of 4 interrupts.
	01C2		1 X X X X 1 0	1	Write: Clear P.Error FF if Data Bits 1:0=0,0 or clear 1 of 3 interrupts to Multibus if Data Bits 1:0=0,1-1,0 or 1,1.
Ethernet Address Prom.	Even addresses 0180 to 019E	PCS 3 0180 to 01FF	X X A A A A X	1	Read: Read up to 16 nipples from the Ethernet Address Prom. Data is transferred on Data lines 3:0 A=Address bits to Prom.
Multimodule Chip Select (iSBX)	0200 through 027F	PCS4 0200 to 027F	X S S M M M S M=MA2 : MA0 to Multimodule S= Strap-able Bits. See Section 3.9	0 or defined by Multi-Module Board	Write/Read: Generate MCS0 and/or MCS1. Via user installed jumpers MCS0/MCS1 may be configured for either 8- or 16 bits multimodule boards. As schipped from factory the configuration is: 0210 to 021F= Generate MCS 0 0220 to 022F= Generate MCS 1
Multimodule DMA Acknowledge (ISBX)	0280 through 02FF	PCS5 0280 to 02FF	X X X M M M X M=MA2: MA0 to ISBX device.	0 or defined by Multi-Module Board	Write: Generate MDACK to ISBX Read : Generate MDACK to ISBX Refer to section 3.5.5
82586 LCC Channel Attention	0300	PCS6 0300 to 037F	XX X X X X X	0	Write: 82586 Channel Attention Read : 82586 Channel Attention

X = don't care bits = not decoded by the ETC

ETC601/611 Figure 26 ETC I/O Address Assignments

A14737

3.6 8259A Programmable Interrupt Controller (PIC) 3.6

The ETC interrupt system is shown in figure 16 of section 3.2.5. Every interrupt source to the 8259A Programmable Interrupt Controller (PIC) passes a strap field thus making interrupt sources and priority levels user selectable and configurable. From factory the interrupt straps are set as shown in figure 16. The interrupt sources are described below.

3.6.1 Interrupt Sources 3.6.1

- Interrupt request lines from the iSBX Multimodule (2 lines).
- Interrupt request from the 82586 Local Communications Controller. Refer to (2) and section 3.3.
- Parity Error in the DRAM has been detected. Note that it is neccessary to reset the parity Error flip-flop during the interrupt routine.

  Parity Error reset address: 01C2H I/O Data Bits 1:0 = 0,0

- Flag Byte interrupt from Multibus. Generated upon write access to multiport RAM location:

  Interrupt Address: XY0402H.

As seen from the Multibus, the X ciffer selects a 1-Mbyte segment out of the total 16-Mbyte Multibus address space, while the Y ciffer, which must be even (128 k boundaries) selects a start address within the 1-Mbyte segment. Note that it is necessary to reset the Flag Byte interrupt flip-flop during the interrupt routine.

Flag Byte reset address : 0180H.

- Interrupt requests from Multibus (8 lines).

3.6.2 Initialization Control Words

The 8259A PIC must be initialized with a sequence of three Initialization Command Words ICW1, ICW2 and ICW4.

ICW1: Address 0000H.

7	6	5	4	3	2	1	0
X	X	X	1	0	X	1	1

X = don't care

B (0) = ICW4 needed
B (1) = Single mode
B (3) = Edge triggered (or level triggered B(3)=1)
B (4) = Initialization Sequence

ICW2: Address 0002H.

7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	L2	L1	L0

T(7-3) are the five most significant bits of the interrupt vector, which are user programmable.

L(2-0) are the three least significant bits of the interrupt vector, which are automatically supplied by the 8259A PIC according to the interrupt level.

ICW4: Address 0002H

7	6	5	4	3	2	1	0
0	0	0	0	0	X	EOI	1

x = don't care

B(0) = 8086/8088 Mode

B(1) EOI = 0, Normal End of Interrupt Mode
EOI = 1, Automatic EOI Mode.
B(3) = Non Buffered Mode
B(4) = Not Special Fully Nested Mode.
B(7-5) must be all zeroes.

3.6.3 Operation Control Words

After initialization, the 8259A PIC operates in fully nested mode. IR 0 is assigned priority 0 (highest), and IR 7 priority 7 (lowest). The chip is ready to accept interrupt. However, during the operation, the Operation Command Words can command the 8259A PIC to operate in various modes.

OCW1: Address 0002H.

7	6	5	4	3	2	1	0
M7	M6	M5	M4	M3	M2	M1	M0

Write commands to OCW1 address sets/clears the mask bits. Read commands reads the mask. M(0) = 1 indicates that IR0 is masked, M(1) = 1 indicates that IR1 is masked and so on.

OCW2: Address 0000H

7	6	5	4	3	2	1	0
R	SL	EOI	0	0	L2	L1	L0

OCW2 control the rotate and end of interrupt modes.

R1,SL,EOI	FUNCTION
001	Non-Specific EOI Command
011	Specific EOI Command
101	Rotate on non-specific EOI command
100	Rotate in automatic EOI mode (set)
000	Rotate in automatic EOI mode (clear)
111	Rotate on specific EOI command
110	Set priority command
010	No operation

L(2-0) These bits determine the level to be acted upon when SL=1 (active).

OCW 3: Address 0000H

7	6	5	4	3	2	1	0
0	ESMM	SMM	0	1	P	RR	RIS

ESMM,SMM	FUNCTION
00	No action
01	No action
10	Revert to normal mask mode
11	Enter special maske mode

POLL	FUNCTION
0	No Poll Command
1	Poll Command. Accept next read command to address 0000H as an interrupt acknowledge. Data on bus is:

7	6	5	4	3	2	1	0
I	X	X	X	X	W2	W1	W0

I = 1 if there is an interrupt

W(2-0) = Binary of highest priority level requesting interrupt

RR,RIS	FUNCTION
00	No action
01	No action
10	Read interrupt register (IRR) on next read command to address 0000H
11	Read in service register (ISR) on next read command to address 0000H

3.7 8274 Multi-Protocol-Serial-Controller (MPSC) 3.7

The seriel channels of the ETC is controlled by the INTEL 8274 MPSC. Channel A of the 8274 is used for the X.21 or the V.24/V.28 synchronous serial interface (3) and channel B for the V.24/V.28 asynchronous console interface.

The system interface to the 80186 CPU consists of 8 ports or buffers, the addresses of which are as shown in figure 26. Data buffers of the 8274 are addressed by address bit 2="0", and command ports are addressed by address bit 2="1".

3.7.1 8274 MPSC Command/Parameter and Status Registers 3.7.1

Command, parameter, and status information is held in 21 registers within the 8274 MPSC. There are 8 write registers for each channel (WR0-WR7), 2 read registers (RR0A,RR1A) for channel A and 3 read registers (RR0B-RR2B) for channel B. The registers are accessed via the command ports. An internal pointer register selects which of the registers will be written or read when the command port of an 8274 MPSC channel is accessed. After reset, the first byte written to a command port will be loaded into WR0. The three least significant bits of WR0 are loaded into the pointer, and the next read or write operation to the command port accesses the read or write register selected by the pointer. The pointer is reset after the read or write operation is completed.

A survey of COMMAND/PARAMETER registers are shown in figure 27 and 28 for the X.21 - V.24/V.28 synchronous channel A and the V.24/V.28 asynchronous channel B. It is assumed that channel A shall operate in HDLC mode.

Read Registers RR0 and RR1 exists in both channels and holds status information. Refer to (1) and figure 31. RR2 B contains the modified interrupt vector for the highest interrupt pending.

Initialization Sequence The initialization routine must issue a CHANNEL RESET command at the beginning. WR4 should be defined before other registers. At the end of init. sequence RESET EXT./STATUS INTERRUPT and ERROR RESET commands must be issued to clear interrupts, which may have been caused by power-up.

3.7.2 Channel A Data Transfer Mode 3.7.2

The X.21 and the V.24/V.28 synchronous interfaces are designed to utilize the DMA transfer mode of the 8274 MPSC channel A(WR2 D1, D0=0,1), however, the channel may be interrupt driven as well (WR2 D1, D0=0,0). The receive DMA request of channel A RXDRQA is connected to 80186 CPU DMA request input 1 (DRQ1). The DRQ0 input of the 80186 CPU is shared between channel A transmit DMA request TXDRQA and the DMA request from the iSBX interface (XDRQ). A select signal, which originates from the 8255 PPI port C bit 2, assigns DRQ0 to either channel A transmitter or iSBX interface (Port C bit 2=1 selects TXDRQA as DRQ 0). Refer to (3) for detailed description of the 8274 MPSC operation in interrupt driven/dma mode.

3.7.3 Channel A Interrupt Mode 3.7.3

Interrupt pair INT1/INTA1/ of the 80186 CPU is dedicated the 8274 MPSC. Refer to section 3.2.5. The interrupt Code of the 8264 MPSC must be set to 8086/88 Vector Mode (WR2A D5, D4, D3 = 1,1,0), and the status Affects Vector bit must be active (WR1B D2=1), which results in the interrupt structure indicated in figure 30.

Interrupts are serviced by their respective interrupt routines, which are pointed out by means of the variable vector. The routines must also read the status register (RR0 or RR1) to determine the interrupt source in details, and issue Reset commands to reset the status latches. After servicing the interrupt, two EOI commands must be issued, at first EOI to 8274 MPSC (WR0A command 7) and then EOI to 80186 Internal Interrupt Controller (Internal Control Block offset 22H). Channel A interrupt sources are listed in figure 31.

3.7.4 X.21 Interface of Channel A 3.7.4

The X.21/ SELECT signal being active (low) indicates that a X.21 cable is connected to channel A and selects the X.21 serial interface of channel A. The state of the X.21/ SELECT signal may be sensed via the 8255 PPI port B bit 7 (refer to section 3.8.2).

3.7.4.1 X.21 Phases

The X.21 operation can be described in four phases. The DCE provides bit clocking to channel A during all phases.

- Quiecent Phase is the nonactive phase during which the DCE and channel A indicate ready and not ready status. Channel A must indicate status using the Transmit (T) and Control (C) lines. The C line is controlled by the Data Terminal Ready signal (DTRA) of 8274 MPSC channel A. Steady state binary condition on T (0 or 1) must be signalled using the Request to send signal (RTSA) of 8274 MPSC channel A. The T line is logically the "and " of TXDA, RTSA. TXDA is transmitter serial output of 8274 MPSC channel A.

- Call Establishment Phase. In this phase a circuit-switched connection between remote DTE and channel A is established by way of T and R circuits using characters of International Alphabet number 5 (odd parity). SYN characters are used for synchronization between channel A and DCE.

- Data transfer Phase is indicated by a unique state of the X.21 interface control signals (Control and indication must both be on). A full duplex transmission pathe exists between channel A and remote DTE. The RTSA signal must be true in the data phase to allow TDXA to control the T line.

- Clearing Phase is the phase during which the circuit-switched connection is released, either by channel A or DCE clear request. After clearing channel A must return to a quiescent state. DCE clear indication is detected by hardware outside the 8274 MPSC, and causes generation of an External/status interrupt via the Carrier Detect input signal (CDA) of channel A.

3.7.4.2 X.21 Interchange Circuits

The physical elements of the X.21 serial interface complies with the CCITT recommendation X.21 (4) with the exception that the byte timing signal (B) is not used.

The interchange circuits of X.21 is connected to the 8274 MPSC channel A as described below.

- T (Transmit)
  This line is controlled by the transmitter serial output (TXDA) and the Request To Send signal. T line is logical the "and" of TXDA, RTSA. When RTS of WR5 is "1" and TXDA is "1", the T line will be "1" (mark). After power-on, reset from multibus or channel reset command TXDA will be "1" and RTSA "0". TX Enable of WR5 being "0" does also force TXDA to mark state, however, the marking state is not entered until after an eventual character or flag has been sent.

- C (Control)
  This line is controlled by the Data Terminal Ready signal (DTRA). When DTR of WR5 is "1", the C signal will be on. After power on, reset from multibus or channel reset command, the DTRA signal will be "0", which places channel A in the uncontrolled not ready state (T=0, C=OFF). The C signal is synchronized with signal element timing (S signal).

- R (Receive)
  This line controls the receiver serial input (RXDA) of the 8274 MPSC. Via the 8255 PPI port B bit 4 it is made possible to sense the state of R when channel A is in X.21 interface mode. Bit 4 of port B will be "1" if R is "1" (refer to section 3.8).

- I (Indication)
  This line controls the Clear To Send input (CTSA) of channel A. Any transition on the I line will generate an External/Status interrupt (if enabled - WR1, D0=1). A read of RR0, D5 immediately following a Reset External/Status interrupt command reflects the current state of I ("1" if I is ON).

- S (Signal element timing)
  This line controls the transmit/receive clock inputs of channel A (TXCA/RXCA).

- R=0 and I=OFF (DCE clearing state)
  The Carrier Detect (CDA) input of channel A is used to detect the DCE clearing state, which is a steady state condition that persists for at least 16 contigous bit intervals but not less than 10 mS. Whenever clearing is detected as valid an External/Status interrupt is generated, and this interrupt is also generated when the DCE leaves clearing state. A read of RR0, D3 immediately following a Reset External/Status interrupt command reflects the current clearing state (RR0, D3=0 if DCE clearing and RR0, D3=1 if DCE is not clearing).
  Figure 29 indicates by ✱ the times at which interrupt is generted.

3.7.5 V.24/V.28 Interface of Channel A

The X.21/ SELECT signal being off (high) indicates that a V.24/V.28 cable is connected to 8274 MPSC channel A, and selects the V.24/V.28 interface circuits. The state of the X.21/ SELECT signal may be sensed via the 8255 PPI port B bit 7 (refer to section 3.8).

3.7.5.1 V.24/V.28 Interchange Circuits

The definition of these interface circits complies with the CCITT recommendation V.24 (5), and the electrical characteristic complies with V.28 (5).

Following signals are included:

Received Data	104
Transmitted Data	103
Receiver Signal Element Timing (DCE)	115
Transmitter Signal Element Timing (DCE)	114
Request to Send	105
Data Terminal Ready	108/2
Ready for Sending (clear to send)	106
Data Set Ready	107
Data Carrier Detect	109
Calling Indicator	125
Receiver Signal Element Timing (DTE)	128
Transmitter Signal Element Timing (DTE)	113
Common Return	102

The interchange circuits are connected to 8274 MPSC channel A as described below.

- Received Data A.
  Controls the receiver serial input (RXDA)

- Transmitted Data A.
  Controlled by transmitter serial output (TXDA)

- Receive Clock A in/Transmit Clock A in. These lines provides the transmission timing signals for the channel and is connected to inputs RXCA/TXCA respectively. It is made possible for the V.24/V.28 interface to supply signal element timing to the DCE (DTE source). In this case the RXCA/TXCA is controlled by an ON BOARD TXCA clock, which is generated using 80186 internal timer 0 (refer to section 3.2.6 and figure 18). The ON BOARD TXCA clock does also drive the V.28 drivers for Receive Clock A out/Transmit Clock A out.

- Request To Send A
  Controlled by Request to Send output (RTSA).

- Data Terminal Ready A
  Controlled by Data Terminal Ready output (DTRA)

- Clear To Send A and Carrier Detect A.
  These lines are connected to the CTSA and CDA inputs. Any transitions on these lines will generate External/Status interrupts (if enabled - WR1, D0= 1). A read of RR0, D5 (CTSA) or D3 (CD) immediately following a Reset External/Status

interrupt command reflects the current state of the signal (RR0, D5 = "1" if Clear To Send is on and RRO, D3 = "1" if Date Carrier Detect is on).

- Data Set Ready A and Calling Indicator A.
  The State of these signals may be sensed via the 8255 PPI port B bit 4 and 3 respectively. Port B bit 4 will be "0" if Data Set Ready is on, and bit 3 will be "0" if Calling Indicator is on (calling signal received). Refer to section 3.8.2.

- Receive Clock A out/Transmit Clock A out.
  See description of Receive clock A in and Transmit Clock A in above.

Refer to figure 30 and 31 for interrupt structure and interrupt sources.

3.7.6 V.24/V.28 Interface of Channel B

3.7.6

The 8274 MPSC Channel B is utilized for a V.24/V.28 asynchronous console interface. The definition of the interface circuits complies with the CCITT recommendation V.24 (5), and the electical characteristics complies with V.28 (5).

Following signals are included:

Received Data	104
Transmitted Data	103
Request To Send	105
Data Terminal Ready	108/2
Ready For Sending (Clear To Send)	106
Data Set Ready	107
Data Carrier Detect	109
Calling Indicator	125
Common Return	102

The interchange circuits are connected to 8274 MPSC channel B as described below

- Received Data B.
  Controls the receiver serial input (RXDB)

- Transmitted Data B.
  Controlled by transmitter serial output (TXDB)

- Request To Send B.
  Controlled by Request to Send output (RTSB). WR2A D7 must be "0" = channel B pin 10 programmed as request to send.

- Data terminal Ready B.
  Controlled by Data Terminal Ready output (DTRB)

- Clear To Send B and Carrier Detect B.
  Connected to CTSB and CDB inputs. Any transitions on these lines will generate External/status interrupts (if enabled WR1 D0 ="1"). A read of RR0, D5 (CTSB) or D3 (CD) immediately following a Reset External/Status interrupt command reflects current state of the signals (RR0, D5 = "1" if Clear To Send is on and RR0, D3 = "1" if Carrier Detect is on).

- Data Set Ready B and Calling Indicator B.
  The state of these signals may be sensed via the 8255 PPI port B bit 6 and 5 respectively. Port B bit 6 will be "0" if Data Set Ready is on, and bit 5 will be "0" if Calling Indicator is on (calling signal received). Refer to Section 3.8.2.

Refer to figure 30 for interrupt structure and figure 31 for interrupt sources.

HDLC SYNCHRONOUS MODE

BIT / REG	D7	D6	D5	D4	D3	D2	D1	D0
WR 0	00 NUL 01 RES. RX CRC CHECK 10 RES. TX CRC GEN 11 RES. TX UNDERRUN		000 NUL 001 SEND ABORT 010 RES EXT./STATUS INTR 011 CHANNEL RESET 100 EN INTR. ON NEXT RX CHAR 101 RES. TX INTR/DMA PENDING 110 ERROR RESET 111 EOI - SEE NOTE ⚠1			REGISTER POINTER		
WR 1	0 DIS. WAIT	0 MUST BE ZERO	0 NOT USED	0 0 1 RX INTR ON FIRS CHAR OR SPEC. CONDITION		SEE NOTE ⚠2	TX INTR./ DMA EN.	EXT. INTR ENABLE
WR 2A	0 PIN 10=RTSB	0 MUST BE ZERO	1 VECTORED INTERRUPT	1 0 8086/8088 MODE		PRIORITY	0 A DMA ,	1 B INTR
WR 2B	V7	V6	V5 INTERRUPT VECTOR	V4	V3 * = VARIABLE VECTOR	V2*	V1*	V0*
WR 3	00 RX 5 B/CHAR 01 RX 7 B/CHAR 10 RX 6 B/CHAR 11 RX 8 B/CHAR		AUTO ENABLES	ENTER HUNT MODE	RX CRC ENABLE	ADDRESS SEARCH MODE	0 MUST BE ZERO IN HDLC	RX ENABLE
WR 4	0 1 X 1 CLOCK		1 HDLC MODE	0	0 ENABLE SYNC MODES	0	0 ODD PARITY	0 DIS. PARITY
WR 5	DTR	00 TX 5 B/CHAR 01 TX 7 B/CHAR 10 TX 6 B/CHAR 11 TX 8 B/CHAR	0 NO BREAK	TX ENABLE	0 SEL. HDLC CRC POLY- NOMIUM.	RTS	TX CRC ENABLE	
WR 6	ADDRESS BYTE							
WR 7	0 1 1 1 FLAG CHARACTER					1	1	0

BISYNC MODE (X.21 CALL ESTABLISHMENT PHASE)

BIT / REG	D7	D6	D5	D4	D3	D2	D1	D0
WR 0	SAME AS WR 0 ABOVE							
WR 1	0 DIS. WAIT	0 MUST BE ZERO	0 NOT USED	RX INTERRUPTS 00 DISABLE 01 FIRST CHAR OR SPEC. 10 ALL CHAR OR SPEC. 11 ALL CHAR OR SPEC.		SEE NOTE ⚠2	TX INTR./ DMA EN.	EXT. INTR ENABLE
WR 2A	0 PIN 10=RTSB	0 MUST BE ZERO	1 VECT. INTR.	1 0 8086/8088 MODE		PRIORITY	00 BOTH INTR. MODE 01 A DMA, B INTR	
WR 2B	SAME AS WR 2B ABOVE							
WR 3	0 1 RX 7B/CHAR		AUTO ENABLES	ENTER HUNT MODE	0 DIS. RX CRC	0 NO ADDRESS	SYNC. CHAR. LOAD INHIBIT	RX ENABLE
WR 4	0 0 X1 CLOCK		0 16 BITS SYNC	1	0 ENABLE SYNC MODES	0	0 ODD PARITY	1 EN. PARITY
WR 5	DTR	0 1 TX 7B/CHAR		SEND BREAK	TX ENABLE	0 NO CRC	RTS	0 NO CRC
WR 6	0 0 1 0 SYNC CHARACTER				1	1	0	0
WR 7	0 0 1 0 SYNC CHARACTER				1	1	0	0

Note 1: EOI can only be issued through channel A.
Note 2: Variable Vector=1 can only be set in WR1 B, which sets both channels to supply variable vector. Must be 0 in WR 1A.

Figure 27 COMMAND/PARAMETER REG. SURVEY
X.21-V.24/V.28 CHANNEL A

ASYNCHRONOUS MODE

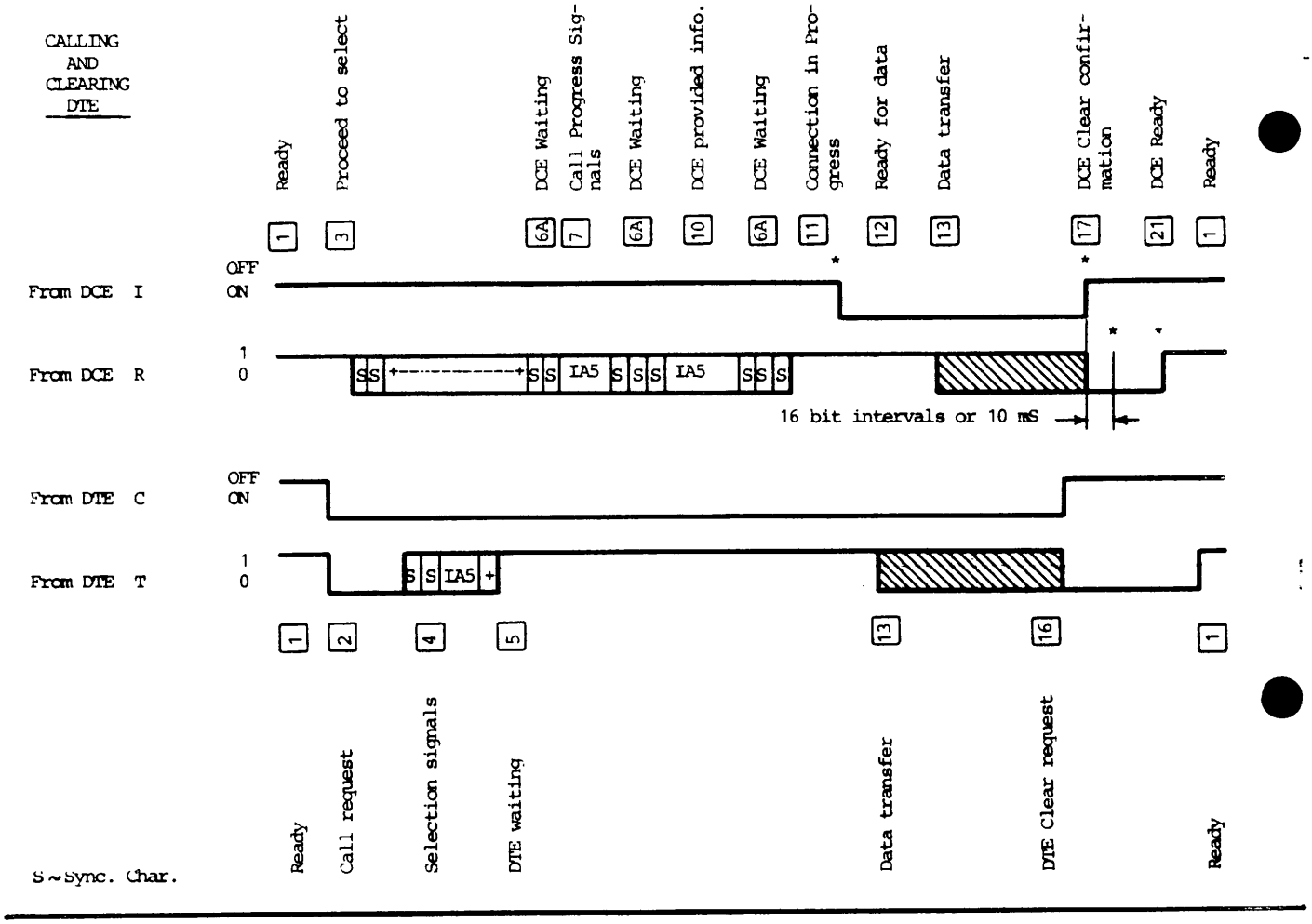
BIT / REG	D7	D6	D5	D4	D3	D2	D1	D0
WR 0	00 NUL 01 RES. RX CRC CHECK 10 RES. TX CRC GEN 11 RES TX UNDERRUN		000 NUL 001 SEND ABORT (HDLC ONLY) 010 RES. EXT./STATUS INTR. 011 CHANNEL RESET 100 EN. INTR. ON NEXT CHAR. 101 RES. TX INTR./DMA PENDING 110 ERROR RESET 111 EOI (1)			REGISTER POINTER		
WR 1	0 DIS. WAIT	0 MUST BE ZERO	0 NOT USED	RX INTERRUPTS 00 DISABLE 01 FIRST CHAR. OR SPEC. 10 ALL CHARS. OR SPEC. 11 ALL CHARS. OR SPEC.		1 Variable VEC-tor. (2)	TX INTR./ DMA EN.	EXT. INTR. ENABLE
WR2A	0 PIN10=RTSB	0 MUST BE ZERO	1 VECTORED INTERRUPT	1	0 8085/8088 MODE	PRIORITY	00 BOTH INTERRUPT MODE 01 A DMA, B INTR.	
WR2B	V7	V6	V5	V4	V3	V2*	V1*	V0*
	INTERRUPT VECTOR				* = VARIABLE VECTOR BITS			
WR3	00 RX 5 B/ CHAR. 01 RX 7 B/ CHAR. 10 RX 6 B/ CHAR. 11 RX 8 B/ CHAR.		AUTO ENABLES	0 NO HUNT MODE	0 NO CRC	0 NO ADDRESS	0 NO SYNC LOAD	RX ENABLE
WR4	00 x 1 CLOCK 01 x 16 CLOCK 10 x 32 CLOCK 11 x 64 CLOCK		0 NO SYNC CHARACTER	0	00 EN.SYNC. MODES 01 1 STOP BIT 10 1.5 STOP BITS 11 2 STOP BITS		EVEN/ODD PARITY	PARITY ENABLE
WR5	DTR	00 TX 5 B / CHAR. 01 TX 7 B / CHAR. 10 TX 6 B / CHAR. 11 TX 8 B / CHAR.	SEND BREAK	TX ENABLE	0 NO CRC	RTS	0 NO CRC	
WR 6 WR 7	NOT USED IN ASYNC. MODE							

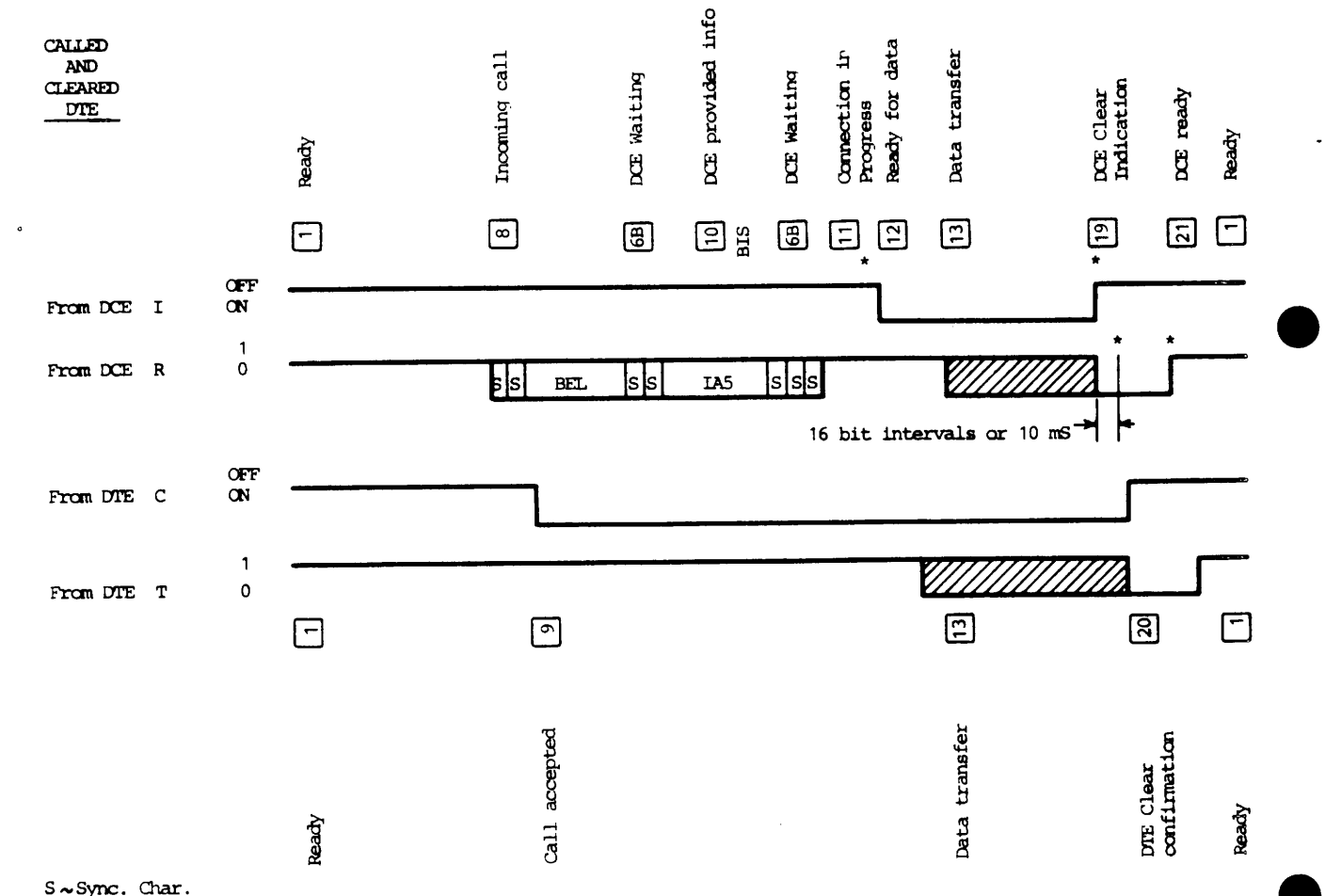
Note 1: EOI can only be issued through WR 0 A.

Note 2: Variable Vector = 1 can only be set in WR 1B, which sets both channels to supply variable vector. Must be 0 in WR 1A.

ETC601/611 . Figure 28 COMMAND/PARAMER REGISTER SURVEY
ASYNCHRONOUS V.24/V.28 CHANNEL B

A14739

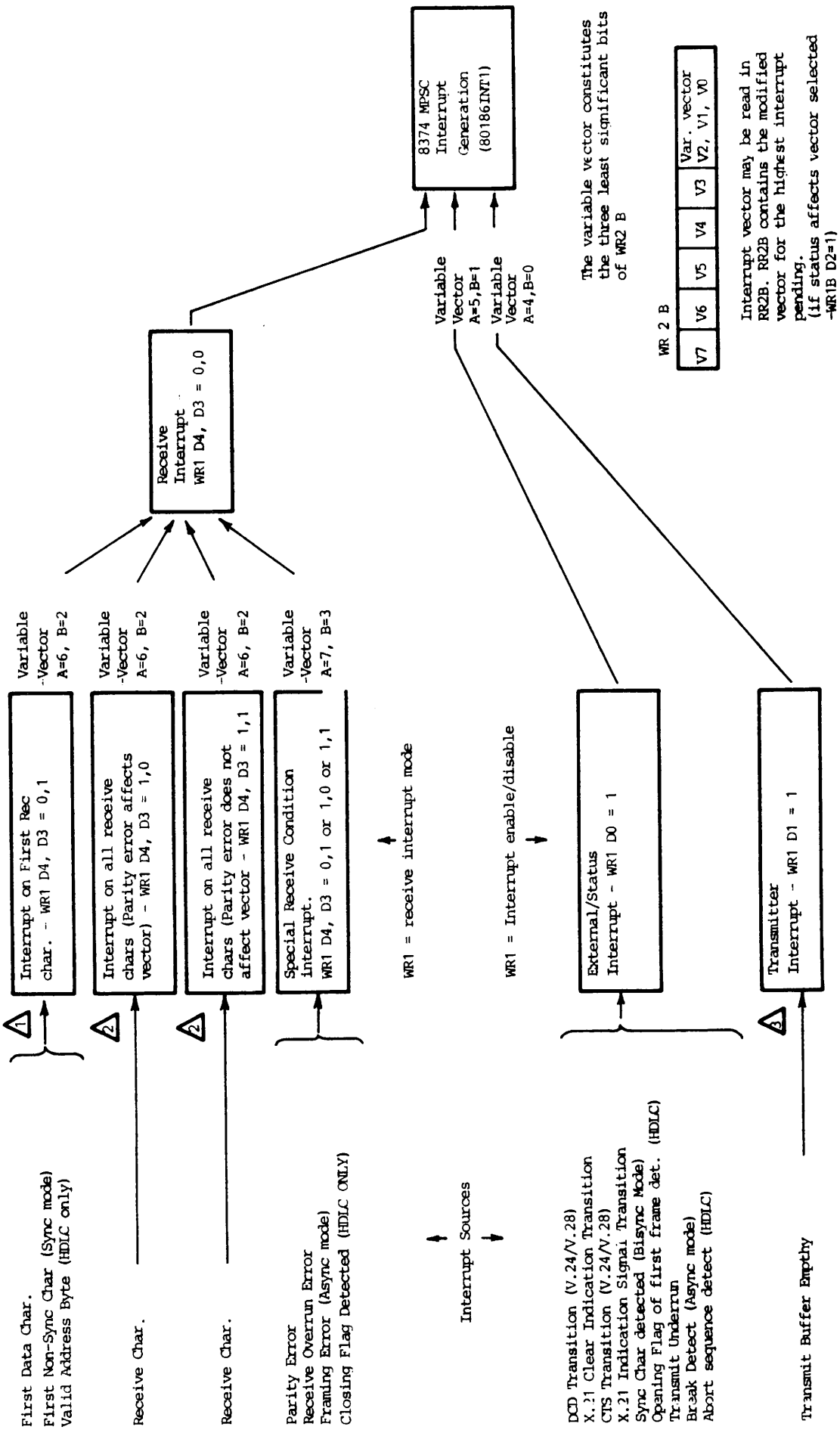




ETC601/611

A14740

Figure 29 Example of sequence of events Successfull call and clear for circuit-switched service.



Note 1: This mode must be used when channel A is operated in DMA mode
Interrupts as well as RXDRQ A is generated.

Note 2: These interrupts becomes RXDRQ A when channel A is operated in DMA mode

Note 3: These interrupts becomes TXDRQA when channel A is operated in DMA mode

Figure 30 8274 MPSC Interrupt Structure

Interrupt Source	Read Reg. Status bit Set condition	Read Reg. Status bit reset condition	Comments
First Data Char. First Non-Sync Char (Sync Mode) Valid Address Byte (HDLC only)	RR0 D0 Rec. Char available	Rec. Fifo empthy when char. is read	WR 0 command 4 reactivates interrupt on first char. next message.
Parity Error detected	RR 1 D4 latched when error occur	Error Reset Command	
Receive Overrun Err.	RR 1 D4 latched when error occur	Error Reset Command	Rec. Fifo overloaded last Last Char. overwritten
Framing Error (Async Mode)	RR 1 D6-updated on next received char.	Error Reset Command	
CRC Error (HDLC) NB! No Interrupt	RR 1 D6 This bit is set until a correct match is obtained.	Error Reset Command or correct CRC match	CPU must read the CRC bytes before checking for valid CRC result.
Closing Flag Det (End of Frame-HDLC ONLY).	RR 1 D7	Error Reset Command or reception of first char. of next frame	
DCD Transition (V.24/V.28) X.21 Clear Indication Transition	RR 0 D3 latched when DCD or Clear Indication signal changes.	Reset Ext./status interrupt command followed by read of RR0 reflects current state. D3 = "0" if Clear Ind. (X.21) D3 = "1" if DCD on. (V.24/28)	Interrupt is generated when the signal changes. Must be reset by issuing Reset Ext/Status intr. com.
CTS Transition (V.24/V.28) X.21 Indication Transition	RR 0 D5 latched when CTS or Indication changes.	Same as DCD transition except D5="1" if Indication on (X.21) D5= 1 if CTS on (V.24/V.28)	Same as DCD transition
Sync. Char. det. (Bisync mode)	RR 0 D4 Set to 1 when Enter Hunt mode bit is set-WR3 D4. Change from 0→1 causes interrupt.	reset when char synchronization is established. Change from 1→0 causes interrupt.	CPU sets Enter Hunt mode bit when EOM is detected or if synchronization is lost. Interrupt must always be reset issuing, Reset Ext/Status interrupt command.
Opening Flag of first frame det. (HDLC)	RR 0 D4 Set to 1 when Enter Hunt mode bit is set-WR3 D4 or when rec. is disabled. Change from 0→1 causes interrupt.	reset when opening flag of first frame is det. Change from 1→0 causes interrupt	Once this bit is reset it need not be set again by writing Enter Hunt mode bit. Interrupt must always be reset issuing Reset Ext/Status interrupt command.
Transmitter Underrun detected	RR 0 D6 Set following internal or external reset or when underrun occurs, which causes interrupt.	The only command, which can reset is Reset Transmit Underrun/EOM latch command- WR 0 D6,D7 = 1,1	Interrupt must always be reset issuing Reset Ext/Status intr. command
Break detected (Async mode) Abort detected (HDLC)	RR 0 D7 Set upon det. of Break or Abort and termition of Break/Abort, which causes interrupts.	reset by Reset Ext/Status interrupt command	Interrupt must always be reset issuing Reset Ext/Status interrupt command.
Transmit Buffer empthy	RR 0 D2 Transmit buffer empthy except when CRC chars are being sent	reset when transmit buffer is loaded	Set after MPSC reset.

ETC601/611

Figure 31 8274 MPSC Interrupt Sources and Status Bits in Read Registers (RR0,RR1)

A14742

3.8 8255A Programmable Peripheral Interface (PPI) 3.8

The 8255A contains three 8-bit ports (PA, PB and PC), which can be programmed to be input or output ports. In connection with the ETC the PA/PB ports must be configured as input ports and PC port as output. After reset signal, all ports are in input mode and Control Register cleared. The operating mode of the ports is defined by loading the Control Register with a control byte

Control Register: Address 0106H

7	6	5	4	3	2	1	0
1	0	0	1	0	0	1	0

Control Register can only be written.

3.8.1 Port A 3.8.1

Port A is an input port used to read the state of eight straps. The eight straps and the corresponding port A bits are defined as described below.

A PA bit is 0 when the corresponding strap bit jumper post are shortened (jumper installed).

Port A: Address 0100H

7	6	5	4	3	2	1	0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

PA7-
PA5: The amount of on board ram available to the multibus master may be read via these bits. PA7 is MSB and PA5 is LSB. This ram space is referred to as dual port memory, and is physically located from address 00000H and on. The size value which is strapable (3 bits) defines the size in number of 128kbytes segments.
size = 128* (size value + 1) kbytes

It is emphasized that following expression must be fullfilled when adjusting the size and start address straps (strap 4).

size value + start value $\leq$ 7

If this is not the case it is not possible to read/write in ETC dram from multibus.

PA4: 80186 CPU type
PA4 = 0 6 Mhz
PA4 = 1 8 Mhz

PA3: Select continous chip select test
PA3 = 0 normal
PA3 = 1 continous chip select

PA2: Master select
PA2 = 0 ETC is master
PA2 = 1 ETC is slave

PA1, PA0 DRAM memory size

PA1	PA0	
0	0	128 kbytes
0	1	256 kbytes
1	0	512 kbytes
1	1	1 Mbytes

3.8.2 Port B

Port B is an input used to read status for iSBX multimodule board, X.21-V.24/V.28 syncronous serial device and V.24/V.28 asynchronous serial device.

Port B: Address 0102H

7	6	5	4	3	2	1	0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

PB7: X.21/ SELECT. If this signal is active (low) a X.21 cable is connected to JACK 4 for X.21-V.24/V.28 serial interface. If the signal is high either no cable or a V.24/V.28 cable is connected (PB7 logical 1).

PB6: DSRB/. Data Set Ready B for asynchronous serial device connected to the 8274 MPSC channel B via JACK 3. PB6 is logical 0 if Data Set Ready is on.

PB5: CIB/. Calling Indicator for asynchronous serial device connected to 8274 MPSC channel B via JACK 3. PB5 is logical 0 if Calling Indicator is on (calling signal received).

PB4: DSRA/. Data Set Ready or Received Data. With V.24/V.28 cable connected to Jack 4, PB 4 reflects the state of the Data Set Ready signal for the V.24/ V.28 device (logical 0 if on). With a X.21 cable connected, PB4 reflects the state of the X.21 signal R (logical 0 if receive data is zero).

PB3: CIA/. Calling Indicator for synchronous serial device connected to 8274 MPSC channel A via JACK 4. PB 3 is logical 0 if Calling Indicator is on.

PB2-PB1: XOPT0 and XOPT1. Optional input lines from multimodules connected to the iSBX interface JACK 1.

PB0: XPST/. iSBX multimodule board present. PB0 = logical 0 when board is present.

3.8.3 Port C

3.8.3

Port C is an output port used to generate optional signals to the iSBX multimodule board, control the assignment of 80186 DMA channel 0, control the loop back function for ethernet/micronet serial interfaces and to control four indicators. The outputs can be controlled in two different ways:

Port C byte load: Address 0104H

7	6	5	4	3	2	1	0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Port C bit set/reset: Address 0106H

7	6	5	4	3	2	1	0	
0	x	x	x	B2	B1	B0	S	X= don't care

B(2-0) is a binary number, which addresses PC7 through PC0. B2 is MSB and BO is LSB.

S = 0: Reset addressed bit.
S = 1: Set addressed bit.

PC7-
PC4: LED 3 to LED 0. Outputs used to control four light emitting diodes. A PC7 - PC4 bit = 1 turns the corresponding LED ON.

PC3: LPBK/. This signal controls the loop back mode of the micronet/ethernet serial interfaces. When PC3 is 0 the LPBK/ signal is active (LOW), and the transmitted data output (TXDE) of the 82586 LCC is routed through the internal circuits of the micronet/ethernet serial interfaces and back to the received data input (RXDE) of the 82586 LCC without driving the tranceiver cable.

PC2: XDMA/. This signal controls the assignment of the 80186 DMA channel 0. If PC2 is 0 the XDMA/ signal is active (low), and the channel is assigned to the iSBX interface. If PC2 is 1 the XDMA/ signal is inactive (high), and the channel is assigned to the 8274 MPSC channel A transmitter.

PC1-
PC0: XOUTP 1 and XOUTP0. Optional outputs lines to multimodule board connected to the iSBX interface JACK 1.

3.9 iSBX Interface

One connector is available on the ETC which supports the iSBX system bus. This connector supports single transfers as well as DMA transfers via 80186 DMA channel 0. However, the DMA channel is shared with the 8274 MPSC channel A transmitter. The assignment of DMA channel 0 is under software control via the 8255 PPI port C bit 2. Refer to section 3.8.3. Although the iSBX bus on the ETC is intended for floppy disc support the presence of this bus allows many different functions to be added to the ETC. ref. (6).

As indicated on figure 26 the iSBX connector is provided with two Multimodule Chip select lines (MCS1/MCS0). The MCS lines can be controlled by either Address bits 5,4 or Address bit 0, Latched Byte High Enable (LBHE/). The configuration is selectable via straps S12, S10. See figure 32 below.

A DMA acknowledge signal is also provided for the iSBX connector by the way of Peripheral Chip Select line 5 (PCS5/).

Two interrupt requests from multimodule (XINT0, XINT1) may be connected to the 8259 PIC via straps. Refer to section 3.6.1 and figure 16.

PCS 4 active and Address bits 5,4 used

```
        1 2 3
S12     o o o   MCS0 strap
S10     o o o   MCS1 strap
```

X = not decoded by ETC

M = Multimodule Adr. bits MA2:MA0 to ISBX device.

PCS 4 Interval	ADDRESS BITS 6 5 4 3 2 1 0	FUNCTION
0200H to 027FH	X 0 0 M M M X	MCS0, MCS1 for 16-bits transfers (16 Bits boards).
	X 0 1 M M M X	MCS0 for byte/word transfers (8/16 Bits boards).
	X 1 0 M M M X	MCS1 for byte/word transfers (8/16 Bits boards).
	X 1 1 M M M X	No Function

PCS4 active and Address bit 0, $\overline{7}$LBHE used

```
        1 2 3
S12     o o o   MCS0 strap
S10     o o o   MCS1 strap
```

PCS4 Interval	ADDRESS BITS 6 5 4 3 2 1 0	$\overline{7}$LBHE	FUNCTION
0200H to 027FH	X X X M M M 0	0	MCS0, MCS1 for 16-bits transfers (16 Bits boards).
	X X X M M M 0	1	MCS0 for low byte transfers (8/16 Bits boards).
	X X X M M M 1	0	MCS1 for high byte transfers (16 Bits boards).
	X X X M M M 1	1	No Function

Figure 32 Multimodule Chip Select.

3.10 Special I/O devices 3.10

Peripheral Chip Select lines 3 and 6 are used to address special I/O functions such as

- Flag Byte Interrupt set/clear
- Channel Attention to 82586 LCC
- Reset of 82586 LCC
- Read of the contents of the Ethernet Address Prom
- Set/Clear Multibus interrupts
- Load of Multibus Mega-byte Address Register
- Reset of Parity Error Flip-Flop

3.10.1 Flag Byte Interrupt 3.10.1

The Flag Interrupt signal is an interrupt request from the multibus master to the ETC. If the multibus master writes into ETC multiport ram location

Interrupt Address XY0402H

the 80186 CPU is interrupted via the 8259 PIC. Refer to section 3.6 and figure 16. The interrupt request is latched in a R/S Flip-Flop which must be reset to reactivate the interrupt. This is done by an I/O write operation to

Flag Byte reset address : 0180H

For dianostic purpose it is made possible also to set the interrupt FF using an I/O write operation to

Flag Byte set address: 0182H

3.10.2 82586 LCC Channel Att. address, Reset address 3.10.2

and Ethernet address Prom

An I/O write or read operation to addresses

82586 CA Addresses: 0300 to 037F

generates Channel Attention signal to the 82586 local communications controller. Refer to section 3.3.3.

An I/O write operation to address

82586 Reset Address: 0184H

immediately terminates all 82586 LCC activity. Refer to section 3.3.4.

I/O read operations to

Ethernet Address Prom addresses:
0180 to 019E (even addresses)

transfers 16 nipples (16x4 bits) to the 80186 CPU. The transfer takes place via I/O Data lines 3:0. The contents of the Ethernet Address Prom should be transferred to the Command Block list for the 82586 LCC to be used in an ACTION command. The address will then be used by the 82586 LCC for recognition of destination address and insertion of source address. Every ETC has its own unique Ethernet Address Prom. Refer also to (2).

3.10.3 Multibus Mega-Byte Address Register

The ETC contains a programmable Multibus Mega-byte Address Register for sending a 4-bit select address along with any 20-bit Multibus Address. This register allows access to one of 16 megabytes of Multibus address space. The register is loaded with the contents of I/O data lines 3:0 (bit 3 corresponds to multibus address bit 17H) during an I/O write command to I/O address

Load Multibus Mega-byte Address Reg.
Address: 0186H

The register is reset to zero (select of Multibus Address space segment 0) upon Power-on, Multibus INIT signal or Multibus-master memory write command to ETC reset address

Reset Address XY0400H

As seen from the multibus-master the X ciffer selects one of 16 megabytes of Multibus address space, while the Y ciffer (which must be even - 128 K boundaries) selects a start address within a one megabyte segment.

3.10.4 Multibus Interr. and Reset of Parity Error FF

The 80186 CPU has the possibility of generating up to four Multibus interrupt requests named MBINTOUT 0 to 3. Any of the MBINTOUT requests drives an open collector gate the output of which can be strapped to any of the multibus interrupt lines INT/ 0-7. Refer to section 3.2.5 figure 16.

MBINTOUT 0 is an unlatched output i.e. the Multibus interrupt strapped to this output becomes a pulse. MBINTOUT 1:3 are latched outputs i.e. these interrupt requests must be reset by the Multibus master via a Multibus I/O write command. The master must address the latch to reset using Multibus data lines 1:0 and a Multibus address. The upper 8 bits and the lower 4 bits (bits 17H to 10H and bits 3 to 0) of this Multibus interrupt reset address are "don't cares". The remaining Multibus address bits F to 4 are compared with the state of a 12 bits strap field.

The 80186 CPU must address the MBINTOUT interrupt request to set using I/O data lines 1:0 and an I/O write command to i/O address

Set Multibus Interrupt request out
Address: 1COH

For dianostic purposes it is also made possible for the 80186 CPU to reset the MBINTOUT 1:3 latches using I/O data lines 1:0 and and I/O write command to the I/O address

Reset Multibus Interrupt request out
Address: 1C2H

Figure 33 shows set/reset conditions for the MBINTOUT requests.

MBINTOUT requests and Parity Error FF are all reset upon Power-on, Multibus INIT signal or Multibus-master memory write command to ETC reset address.

Note that Parity Error FF is reset via a 80186 I/O write command to address 1C2H whenever I/O data bits 1:0 = zero.

BUS Master I/O Write to Multibus Address X X $S_1S_2S_3$ X HEX X are "don't care hex ciffers. S_1 , S_2 and S_3 are compared with an on board 12-bits strap field (strap 14 and 13)	
DATA BYTE WRITTEN (HEX notation Y ciffer don't care)	FUNCTION
Y0, Y4, Y8, YC	No Function
Y1, Y5, Y9, YD	Reset MBINTOUT 1 request
Y2, Y6, YA, YE	Reset MBINTOUT 2 request
Y3, Y7, YB, YF	Reset MBINTOUT 3 request

80186 CPU I/O Write to I/O Address 1C0 HEX	
DATA BYTE WRITTEN (HEX notation Y ciffer don't care)	FUNCTION
Y0, Y4, Y8, YC	Generate MBINTOUT 0 request (pulse)
Y1, Y5, Y9, YD	Set MBINTOUT 1 request
Y2, Y6, YA, YE	Set MBINTOUT 2 request
Y3, Y7, YB, YF	Set MBINTOUT 3 request

80186 CPU I/O Write to I/O Address 1C2 HEX	
DATA BYTE WRITTEN (HEX notation Y ciffer don't care)	FUNCTION
Y0, Y4, Y8, YC	Reset PARITY ERROR FF.
Y1, Y5, Y9, YD	Reset MBINTOUT 1 request
Y2, Y6, YA, YE	Reset MBINTOUT 2 request
Y3, Y7, YB, YF	Reset MBINTOUT 3 request

Figure 33 Multibus interrupt requests out set/reset.

4. TECHNICAL DESCRIPTION 4.

4.1 Introduction 4.1

This chapter constitutes the technical description of the ETC board. The intention with section 4.2 is to give the reader an overview of the ETC structure. Detailled description may be found in section 4.3 - Logic diagrams with signal description together with section 4.4 - PAL/PROM description and section 4.5 - Timing diagrams.

A description of the LSI components used is not given in this chapter. It is recommended that the reader, who wants a complete understanding of the ETC, consults the relevant data sheets (see appendix A references).

4.2 Short Description 4.2

4.2.1 Address Bus 4.2.1

Fig. 34 shows address bus structure.

The shared Multiplexed Address Bus is 20-bits wide. Bus arbitraiton is resolved by the HOLD/HOLD ACK signal pair. The 80186 CPU grants the bus to the 82586 LCC by issuing HOLD ACK as a response to bus request (HOLD) from the 82586. The address on the Multiplexed Address Bus is latched by the PUADR latches. PUADR is routed to the I/O devices, the On/off board address decoding, the buffer for the On board dual port Address Bus and the EPROM´s.

I/O devices are controlled only by the 80186 CPU utilizing the peripheral chip select lines and the PUADR. I/O address space not utilized on board can address off board I/O devices via Multibus.

The EPROM, On board DRAM and Off board RAM resources can be accessed either by the 80186 CPU or by the 82586 LCC. The 80186 CPU addresses EPROM utilizing the upper memory select line and PUADR F-1. The 82586 addresses EPROM utilizing its address bit 14H and

PUADR F-1. The dual-port DRAM is addressed via the on-board dual port Address Bus. The buffer between PUADR and the On-board dual port Address BUS makes it possible to access EPROM and On board I/O simultaneously with and eventual Multibusmaster accessing the dual port DRAM. The memory address space not utilized on board can address off board RAM resources via the Multibus. A 4-bit Multibus Mega-byte Address Register allow a 4-bit select address to be send along with any 20-bit Multibus address thus a 16 megabyte memory space can be accessed.

A Multibus master can address on board dual port DRAM via the Multibus and the On-board dual port Address Bus. Arbitration logic assigns DPA Bus to either the Multibus master or the 80186/82586.

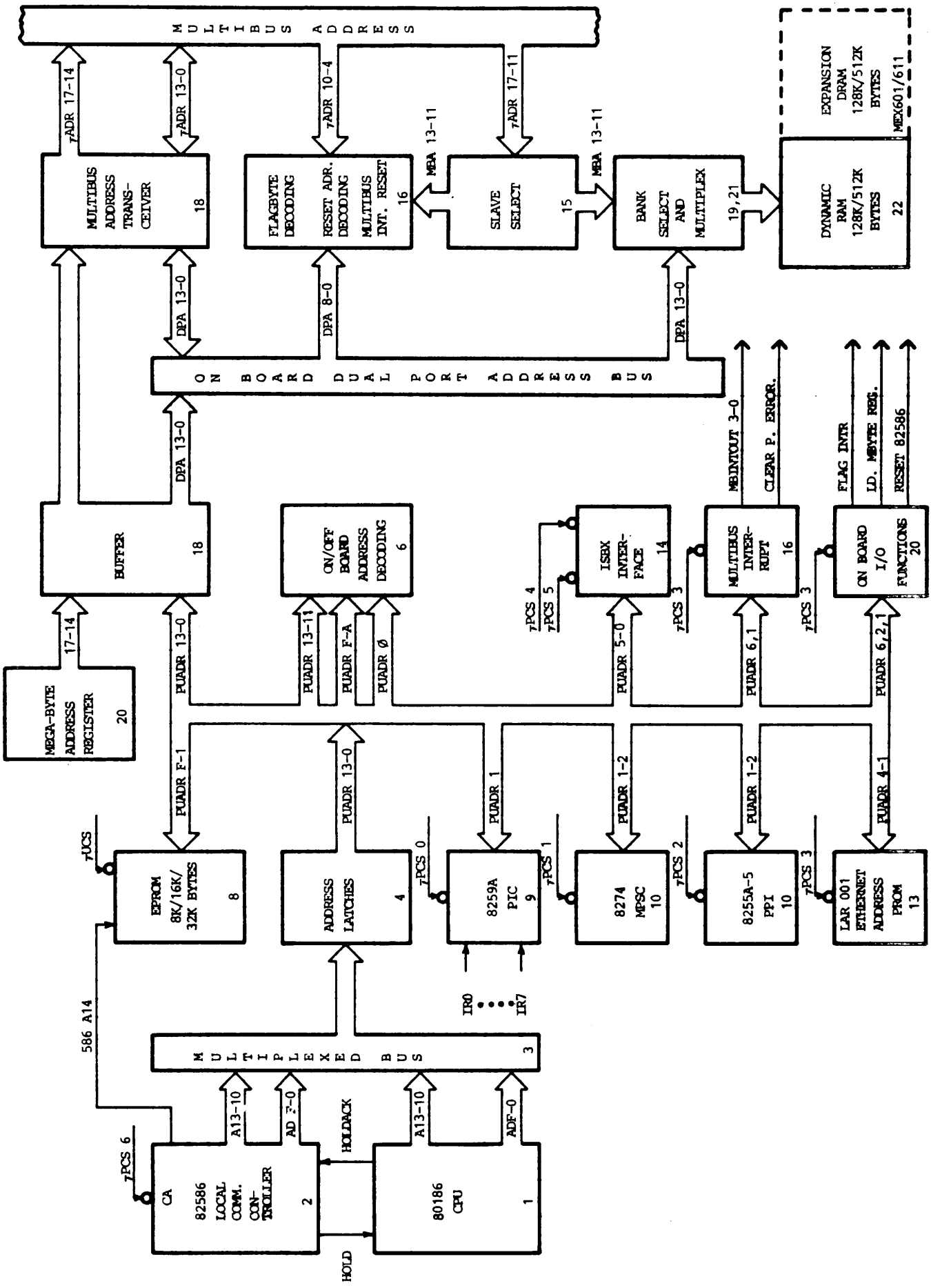
4.2.2 Data Bus

4.2.2

Fig. 35 shows the data bus structure.

Three 16-bits data busses are used on the ETC board: The Multiplexed Data Bus, the On board I/O Data Bus and the On board dual-port Data Bus.

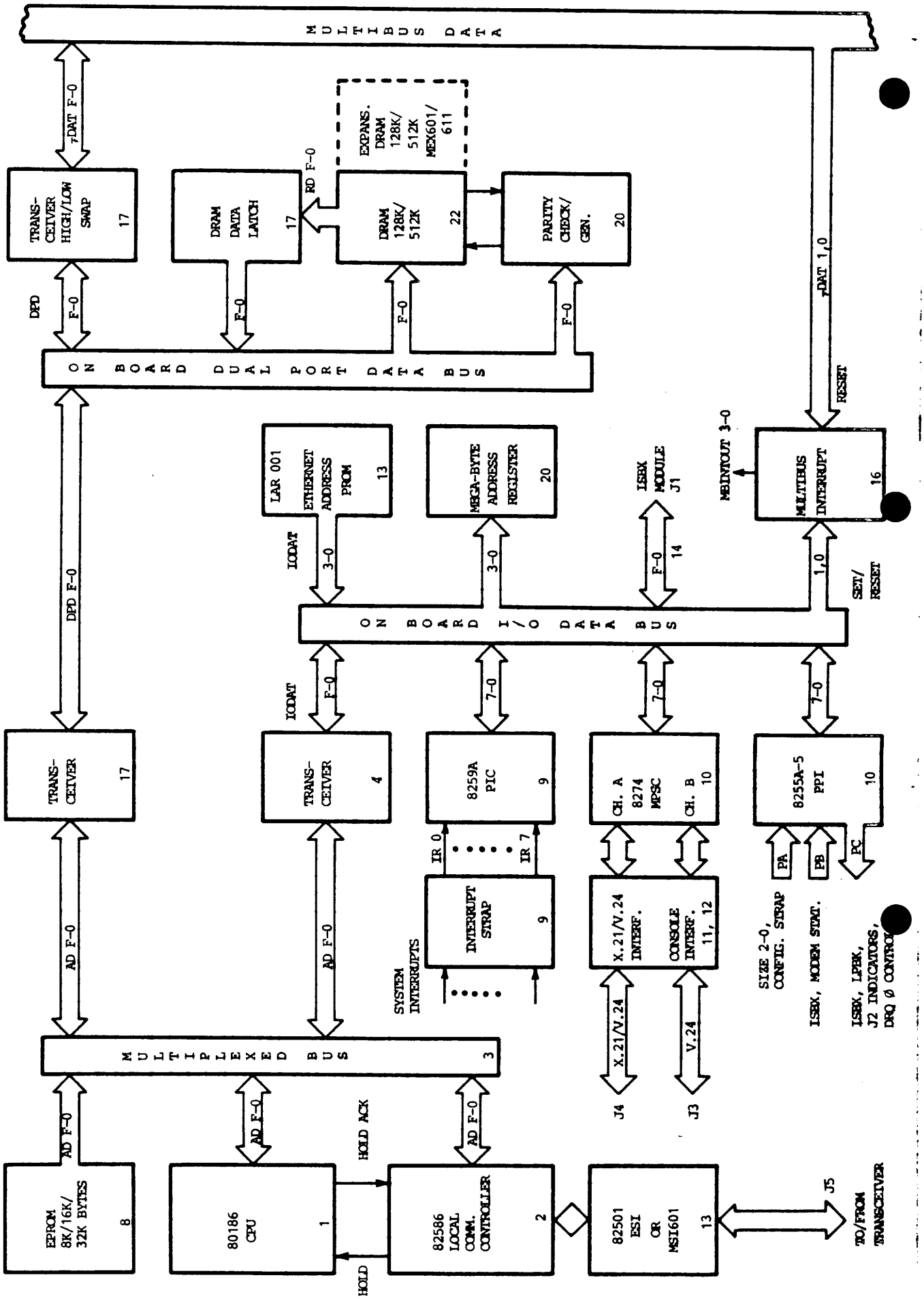
Multiplexed bus arbitration is resolved via the HOLD/HOLD ACK signal pair. The on board I/O devices can be accessed by the 80186 CPU only, while dual port DRAM can be accessed by either the 80186 CPU, the 82586 LCC or an eventual Multibus master. Communication between 80186 and 82586 on task level is accomplished by a shared dual port DRAM mailbox and a 82586/80186 channel attention/interrupt handshake mechanism.



ETC601/611

ADDRESS BUS BLOCK DIAGRAM
Figure 34

A14744



ETC601/611

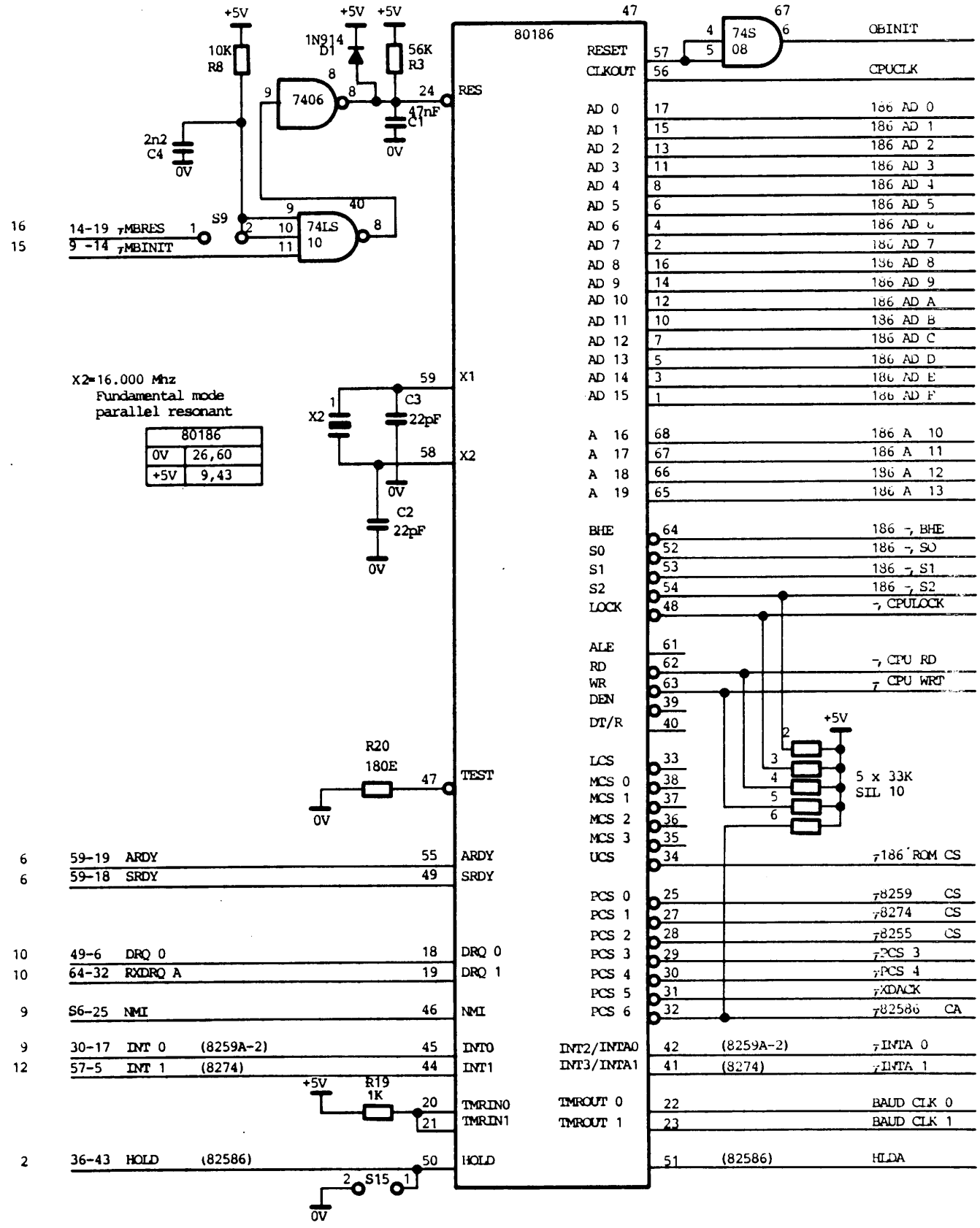
DATABUS BLOCK DIAGRAM

Figure 35

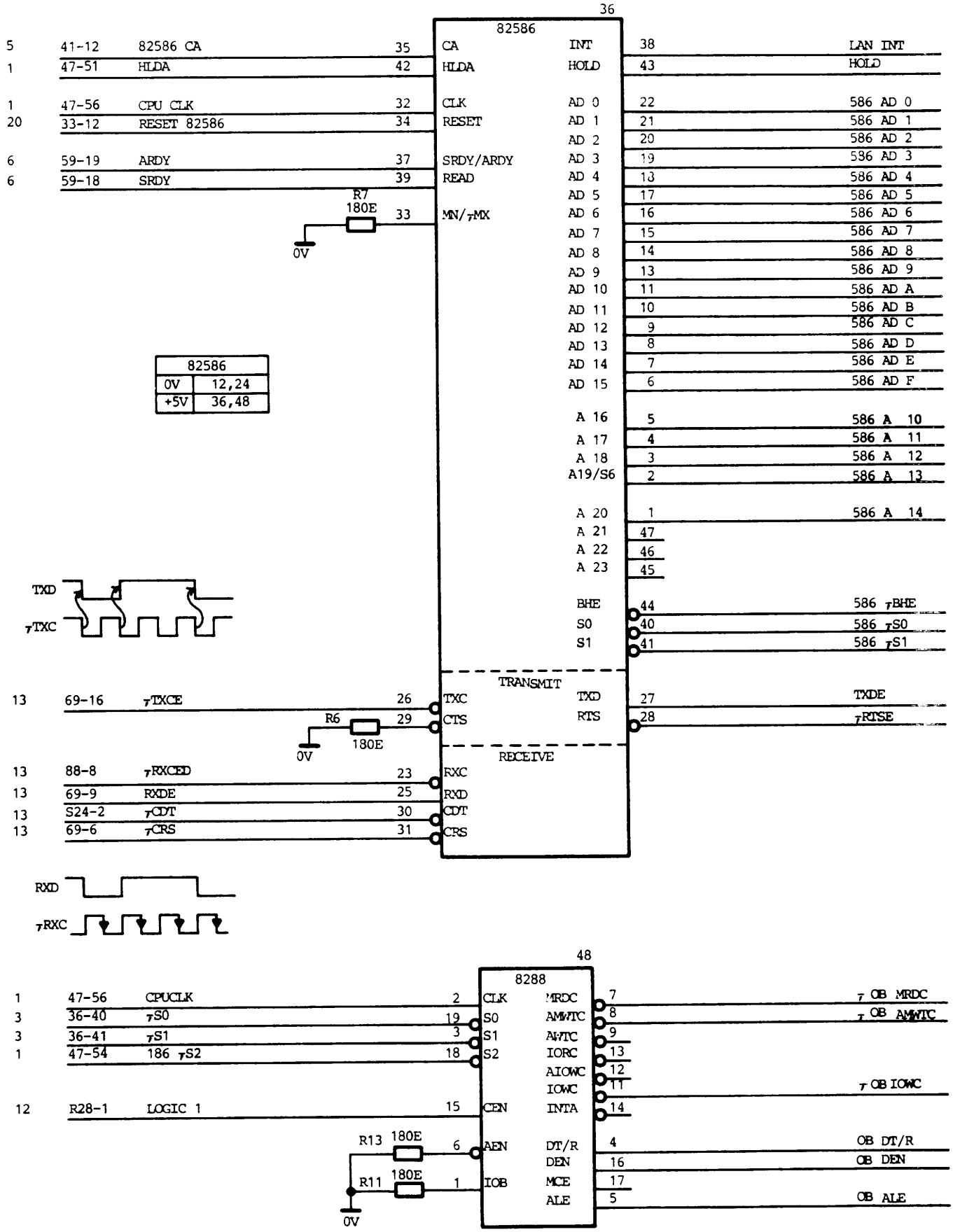
A14745

4.3 Logic Diagrams with Signal Descriptions 4.3

SIGNAL	DESTINATION	DESCRIPTION
OBINIT	P5,P10,P14	On Board Initialize. OBINIT is an active high signal, which resets the ETC to a well known state. The signal is synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the ₇RES signal.
CPUCLK	P2,P5	CPU clock provides the ETC with a 50% duty cycle waveform, the frequency of which is half of the crystal frequency.
186 ADØ - 186 ADF	P3	80186 Address/Data BUS (Ø-F) constitute the time multiplexed memory or I/O address and data bus. The bus is active high.
186 A1Ø - 186 A13	P3	80186 Address BUS (1Ø-13) reflect the four most significant address bits during T1. The bus is active high.
186 ₇BHE	P3	80186 BUS High Enable signal.
186 ₇S0, 186 ₇S1 186 ₇S2	P3 P2,P4,P5	80186 bus cycle status signals.
₇CPULOCK	P5,P15,P19	₇CPULOCK signal is active low during locked transfer to onboard or off-board memory. The signal indicates, that other multibus masters are not to gain control over the system bus.
₇CPU RD	P9,P10 P13,P14	80186 Read Data strobe indicates that 80186 is performing a memory or I/O read cycle.
₇CPU WRT	P9,P10,P14, P20	80186 Write Data strobe indicates that 80186 is performing a memory or I/O write cycle.
₇186 ROM CS	P8	80186 EPROM Chip Select. The signal is active low when a memory reference is made to the defined upper portion of memory (1K - 256K). The address range activating the Chip Selec signal is software programmable.
₇8259 CS	P9	Chip Select signal to 8259 Programmable Interrupt Controller. The ₇PCS signals (Peripheral Chip Select signals of the 80186 are active low when a reference is made to the defined peripheral area (64 Kbyte I/O space). The address ranges activating the ₇PCS signals are software programmable and so are the number of wait states inserted.
₇8274 CS	P10	Chip Select to 8274 Multi-Protocol Serial Controller. Refer also to ₇8259 CS description on this page.
₇8255 CS	P10	Chip Select to 8255 Programmabel Peripheral Controller. Refer also to ₇8259 CS description on this page.
₇PCS 3	P13,P16,P20	Chip Select to various I/O functions: - Flag byte interrupt set/clear. - Reset of 82586 Local Com. Controller. - Load of Multibus Megabyte Addr. Reg. - Set of Multibus Interrupts - Clear of Parity Error FF. - Read of Ethernet Address. Refer also to ₇8259 CS description on this page.
₇PCS 4	P14	Peripheral Chip select signal used by the ISBX interface. Refer also to the ₇8259 CS description this page.
₇XDAC	P14	DMA acknowledge signal to ISBX interface. Refer also to ₇8259 CS description this page.
₇82586 CA	P5	Via the inverter on page 5 this signal becomes the Channel Attention signal to the 82586 Local Com. Controller. Refer also to ₇8259 CS description on this page.
₇INTA Ø	P9	Interrupt Acknowledge signal to the 8259 interrupt controller.
₇INTA 1	P10	Interrupt Acknowledge signal to the 8274 Multi-Protocol-Serial Controller.
BAUD CLK Ø	P12	Output from 80186 internal timer Ø. Used as test baud clock for 8274 MPSC channel A.
BAUD CLK 1	P10	Output from 80186 internal timer 1. Used as baud clock for 8274 MPSC channel B (console interface).
HLDA	P2,P8	Hold Acknowledge is issued as a response to a HOLD request. HLDA indicates that 80186 has released the multiplexed bus and the control lines. The 82586 Local Communications Controller may now take control over the multiplexed bus.


80186
RESET
CLKOUT
AD 0
AD 1
AD 2
AD 3
AD 4
AD 5
AD 6
AD 7
AD 8
AD 9
AD 10
AD 11
AD 12
AD 13
AD 14
AD 15
A 16
A 17
A 18
A 19
BHE
S0
S1
S2
LOCK
ALE
RD
WR
DEN
DT/R
LCS
MCS 0
MCS 1
MCS 2
MCS 3
UCS
PCS 0
PCS 1
PCS 2
PCS 3
PCS 4
PCS 5
PCS 6
RES
X1
X2
TEST
ARDY
SRDY
DRQ 0
DRQ 1
NMI
INT0
INT1
TMRIN0
TMRIN1
HOLD
INT2/INTA0
INT3/INTA1
TMROUT 0
TMROUT 1
+5V
10K
R8
1N914
D1
56K
R3
7406
47nF
C1
2n2
C4
0V
74LS
10
S9
14-19 ₇MBRES
9 -14 ₇MBINIT
X2=16.000 Mhz
Fundamental mode
parallel resonant
80186
0V 26,60
+5V 9,43
C3
22pF
C2
22pF
R20
180E
R19
1K
S15
74S
08
OBINIT
CPUCLK
186 AD 0
186 AD 1
186 AD 2
186 AD 3
186 AD 4
186 AD 5
186 AD 6
186 AD 7
186 AD 8
186 AD 9
186 AD A
186 AD B
186 AD C
186 AD D
186 AD E
186 AD F
186 A 10
186 A 11
186 A 12
186 A 13
186 ¬ BHE
186 ¬ S0
186 ¬ S1
186 ¬ S2
¬ CPULOCK
¬ CPU RD
₇ CPU WRT
5 x 33K
SIL 10
₇186 ROM CS
₇8259 CS
₇8274 CS
₇8255 CS
₇PCS 3
₇PCS 4
₇XDACK
₇82586 CA
(8259A-2)
(8274)
BAUD CLK 0
BAUD CLK 1
(82586)
HLDA
59-19 ARDY
59-18 SRDY
49-6 DRQ 0
64-32 RXDRQ A
S6-25 NMI
30-17 INT 0 (8259A-2)
57-5 INT 1 (8274)
36-43 HOLD (82586)

SIGNAL	DESTINATION	DESCRIPTION
LAN INT	P 9	Active high interrupt request signal from the 82586 LCC.
HOLD	P 1	HOLD is an active high signal used by the 82586 LCC to request control over the multiplexed bus.
586 AD0 - 586 ADF	P 3	82586 Address/Data BUS (0-F) constitute the time multiplexed memory address and data bus.
586 A10 - 586 A13	P 3	82586 Address BUS (10-13) constitute 4 out of 8 most significant address bits for memory operation.
586 A14	P 8	82586 Address BUS 14 is used by the 82586 LCC to address EPROM. When 586 A14 and HLDA are both high a Chip Select signal to EPROM is generated. 82586 Address BUS (15-17) are not used.
586 $\overline{\text{BHE}}$	P 3	82586 Bus High Enable signal.
586 $\overline{\text{S0}}$, $\overline{\text{S1}}$	P 3	82586 bus cycle status signals.
TXDE	P 13	82586 transmitted data output signal. The signal will be high when the 82586 LCC is not transmitting.
$\overline{\text{RTSE}}$	P 13	82586 request to send signal when low notifies the 82501 ESI (Ethernet Serial Interface) or the MSI (Micronet Serial Interface) when the 82586 LCC has data to transmit. The 8288 bus controller on this page constitute the bus controller for the on Board bus. The 80186, 82586 bus cycle status signals S0, S1 are wired together, driving the 8288 bus controller. The S2 input is driven only from the 80186, since 82586 LCC accesses memory only (No I/O).
$\overline{\text{OB MRD C}}$	P 6, P 8, P 19	On board memory read command. This command line instructs on board RAM/EPROM memory to drive data onto the on board dual ported RAM data bus (RAM access) or the multiplexed bus (EPROM access).
$\overline{\text{OB AMWTC}}$	P 6, P 19	On board advanced memory write command. This command line instructs the on board RAM to record the data present on the on board dual ported RAM data bus.
$\overline{\text{OB IOWC}}$	P 16	On board I/O write command. This command line is used only to set the multibus interrupt out signal addressed by I/O Data lines 0-1 or to generate the $\overline{\text{clear}}$ Parity Error signal.
OB DT/R	P 4, P 17	On board data transmit/receive. This signal establishes the direction of data flow through the data transceivers for the on board I/O data bus and the on board dual port data bus.
OBDEN	P 5, P 7	On board data enable. This signal serves to enable data transceivers onto the on board I/O data bus or the on board dual port data bus.
OB ALE	P 4, P 5	On board address latch enable. This signal serves to strobe an address from the 80186 CPU or the 82586 LCC into the address latches.

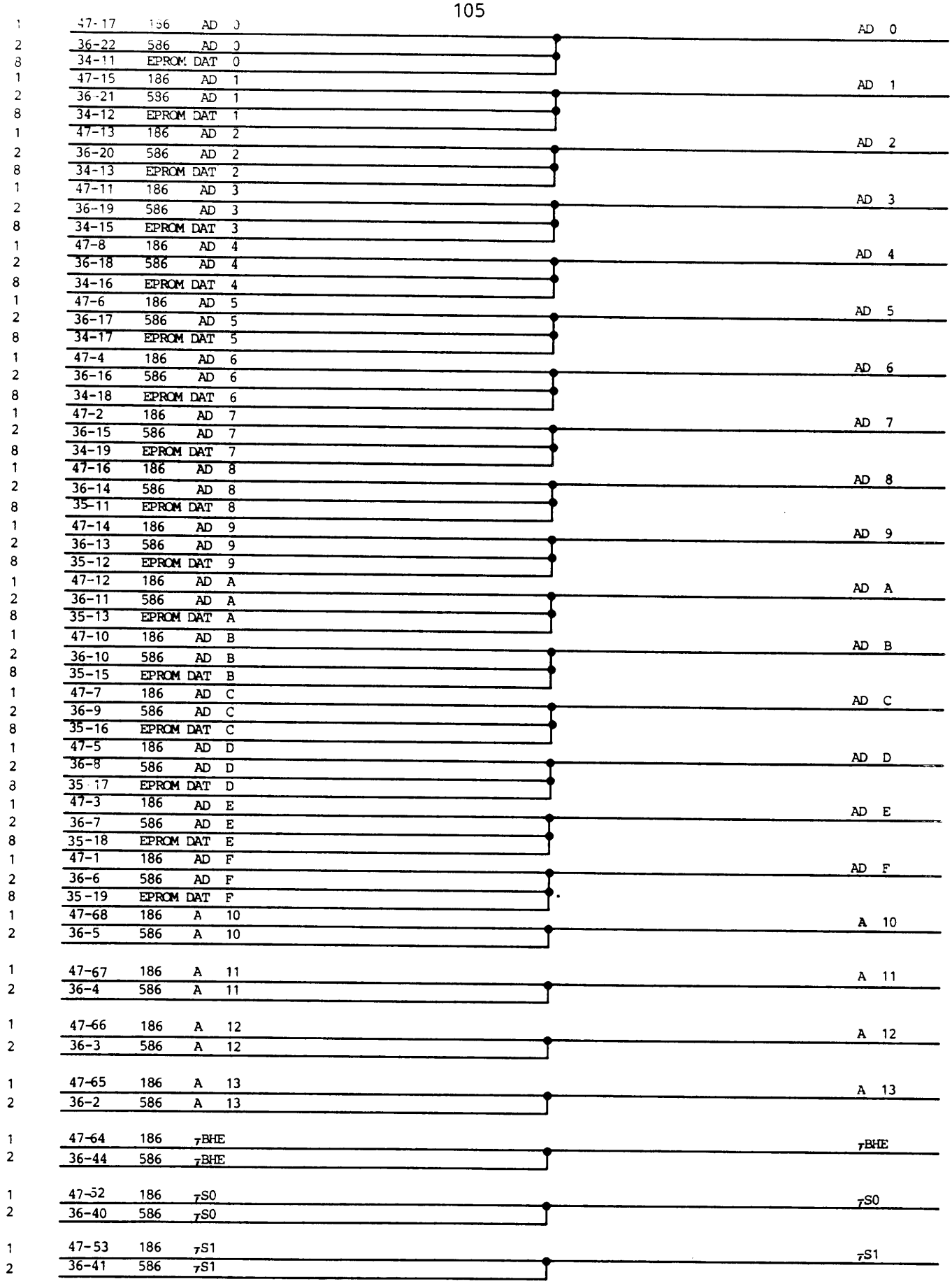

36
82586
5 41-12 82586 CA 35 CA INT 38 LAN INT
1 47-51 HLDA 42 HLDA HOLD 43 HOLD
1 47-56 CPU CLK 32 CLK AD 0 22 586 AD 0
20 33-12 RESET 82586 34 RESET AD 1 21 586 AD 1
AD 2 20 586 AD 2
6 59-19 ARDY 37 SRDY/ARDY AD 3 19 586 AD 3
6 59-18 SRDY 39 READ AD 4 18 586 AD 4
AD 5 17 586 AD 5
R7 180E
0V 33 MN/ MX AD 6 16 586 AD 6
AD 7 15 586 AD 7
AD 8 14 586 AD 8
AD 9 13 586 AD 9
AD 10 11 586 AD A
AD 11 10 586 AD B
AD 12 9 586 AD C
AD 13 8 586 AD D
AD 14 7 586 AD E
AD 15 6 586 AD F
82586
0V 12,24
+5V 36,48
A 16 5 586 A 10
A 17 4 586 A 11
A 18 3 586 A 12
A19/S6 2 586 A 13
A 20 1 586 A 14
A 21 47
A 22 46
A 23 45
TXD
TXC
BHE 44 586 BHE
S0 40 586 S0
S1 41 586 S1
TRANSMIT
13 69-16 TXCE 26 TXC TXD 27 TXDE
R6 180E
0V 29 CTS RTS 28 RTSE
RECEIVE
13 88-8 RXCED 23 RXC
13 69-9 RXDE 25 RXD
13 S24-2 CDT 30 CDT
13 69-6 CRS 31 CRS
RXD
RXC
48
8288
1 47-56 CPUCLK 2 CLK MRDC 7 OB MRDC
3 36-40 S0 19 S0 AMWTC 8 OB AMWTC
3 36-41 S1 3 S1 AWTC 9
1 47-54 186 S2 18 S2 IORC 13
AIOWC 12
IOWC 11 OB IOWC
12 R28-1 LOGIC 1 15 CEN INTA 14
R13 180E 6 AEN DT/R 4 OB DT/R
DEN 16 OB DEN
R11 180E 1 IOB MCE 17
ALE 5 OB ALE
0V

SIGNAL	DESTINATION	DESCRIPTION
AD0 - ADF A10 - A13 $\overline{7}$BHE	P4, P17 P4 P4	This diagram shows the multiplexed bus, which is made by wiring together address/data busses of the 80186 CPU and the 82586 LCC. Note that data lines from EPROM is connected directly to the multiplexed bus, while data from/to on board I/O data bus or on board dual port data bus flows through transceivers. Bus arbitration is resolved by the HOLD and HOLD acknowledge signals. The 80186 CPU releases the multiplexed bus to the 82586 by issuing HOLD acknowledge signal as a response to bus request from the 82586 (HOLD).
$\overline{7}$ S0, $\overline{7}$ S1	P2,P4,P5	
$\overline{7}$ BHE	P4	Byte high enable signal, which is made by wiring together the 80186 $\overline{7}$ BHE and the 82586 $\overline{7}$ BHE signals.
$\overline{7}$ S0, $\overline{7}$ S1	P2,P4,P5	Bus cycle status signals, which are made by wiring together the 80186 $\overline{7}$S0, $\overline{7}$ S1 and the 82586 $\overline{7}$ S0, $\overline{7}$ S1 status signals.

Designed by

Drawn by

Dwg. Office Check


1 47-17 186 AD 0
2 36-22 586 AD 0
8 34-11 EPROM DAT 0
AD 0
1 47-15 186 AD 1
2 36-21 586 AD 1
8 34-12 EPROM DAT 1
AD 1
1 47-13 186 AD 2
2 36-20 586 AD 2
8 34-13 EPROM DAT 2
AD 2
1 47-11 186 AD 3
2 36-19 586 AD 3
8 34-15 EPROM DAT 3
AD 3
1 47-8 186 AD 4
2 36-18 586 AD 4
8 34-16 EPROM DAT 4
AD 4
1 47-6 186 AD 5
2 36-17 586 AD 5
8 34-17 EPROM DAT 5
AD 5
1 47-4 186 AD 6
2 36-16 586 AD 6
8 34-18 EPROM DAT 6
AD 6
1 47-2 186 AD 7
2 36-15 586 AD 7
8 34-19 EPROM DAT 7
AD 7
1 47-16 186 AD 8
2 36-14 586 AD 8
8 35-11 EPROM DAT 8
AD 8
1 47-14 186 AD 9
2 36-13 586 AD 9
8 35-12 EPROM DAT 9
AD 9
1 47-12 186 AD A
2 36-11 586 AD A
8 35-13 EPROM DAT A
AD A
1 47-10 186 AD B
2 36-10 586 AD B
8 35-15 EPROM DAT B
AD B
1 47-7 186 AD C
2 36-9 586 AD C
8 35-16 EPROM DAT C
AD C
1 47-5 186 AD D
2 36-8 586 AD D
8 35-17 EPROM DAT D
AD D
1 47-3 186 AD E
2 36-7 586 AD E
8 35-18 EPROM DAT E
AD E
1 47-1 186 AD F
2 36-6 586 AD F
8 35-19 EPROM DAT F
AD F
1 47-68 186 A 10
2 36-5 586 A 10
A 10
1 47-67 186 A 11
2 36-4 586 A 11
A 11
1 47-66 186 A 12
2 36-3 586 A 12
A 12
1 47-65 186 A 13
2 36-2 586 A 13
A 13
1 47-64 186 ~BHE
2 36-44 586 ~BHE
~BHE
1 47-52 186 ~S0
2 36-40 586 ~S0
~S0
1 47-53 186 ~S1
2 36-41 586 ~S1
~S1

SIGNAL	DESTINATION	DESCRIPTION
PUADR 0	P6,P14,P18	The address latches makes the addresses from the 80186 or the 82586 available during the entire bus cycle. Latching occur on the falling edge of the OB ALE signal, which is generated during T1 when the multiplexed bus contains the address.
PUADR 1	P8,P9,P10 P13,P14, P16,P18 P20 *	
PUADR 2	P8,P10,P13 P18,P20	
PUADR 3,4	P8,P13,P14 P18	
PUADR 5	P8,P14,P18	
PUADR 6	P8,P16,P18 P20	
PUADR 7 - PUADR 9	P8,P18	
PUADR A - PUADR F	P6,P8,P18	
PUADR 10	P18	
PUADR 11 - PUADR 13	P6, P18	
$\overline{7}$ LBHE	P6,P14,P19	Latched byte high enable signal.
$\overline{7}$ LS0 - $\overline{7}$ LS2	P6	Latched $\overline{7}$ S0, $\overline{7}$ S1 and $\overline{7}$ S2 status.
IODAT 0,1	P9,P10,P13 P14,P16,P20	I/O data 0 - I/O data F constitute the on board I/O data bus.
IODAT 2,3	P9,P10,P13 P14,P20	
IODAT 4 - IODAT 7	P9,P10,P14	
IODAT 8 - IODAT F	P14	

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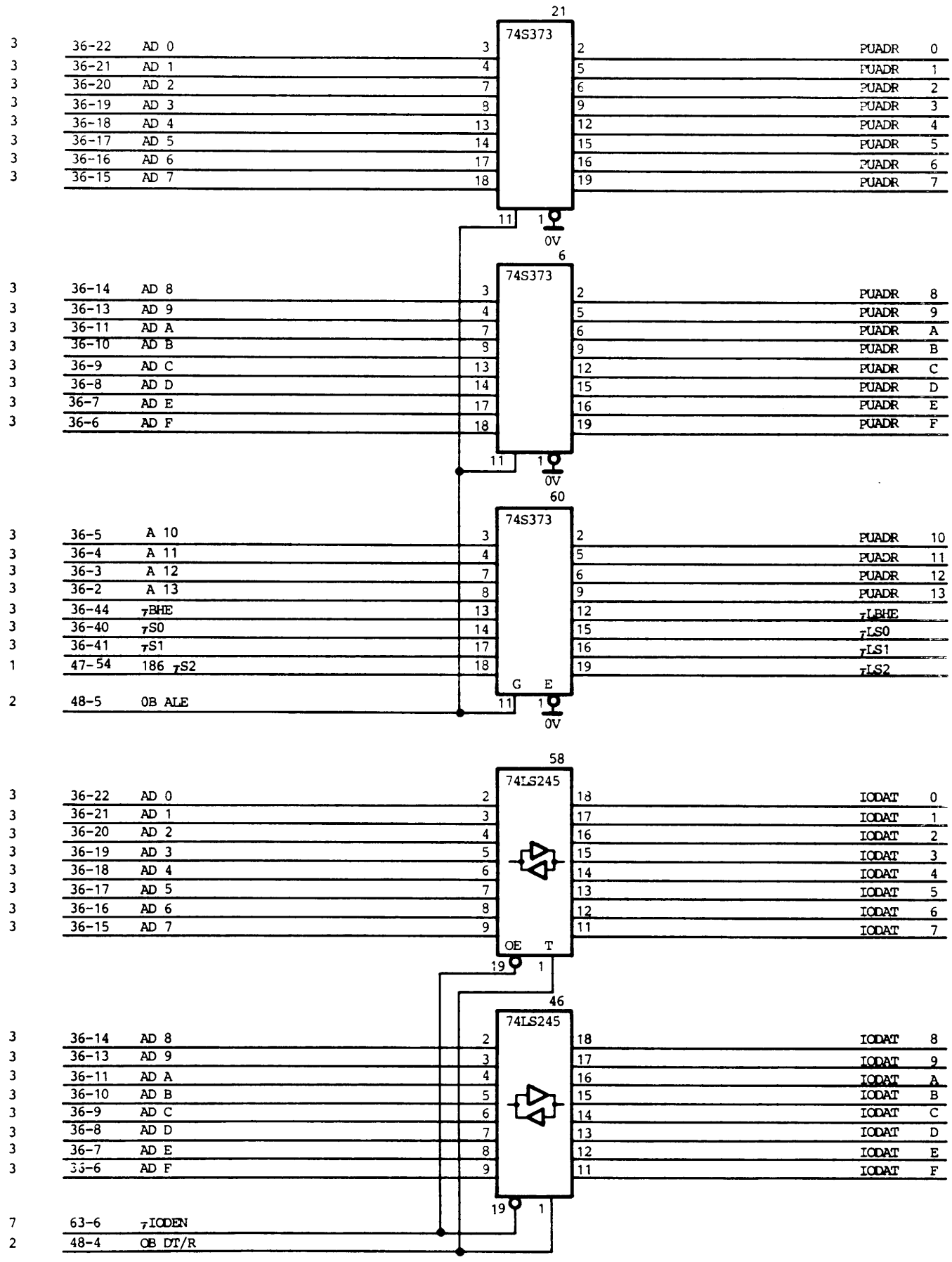
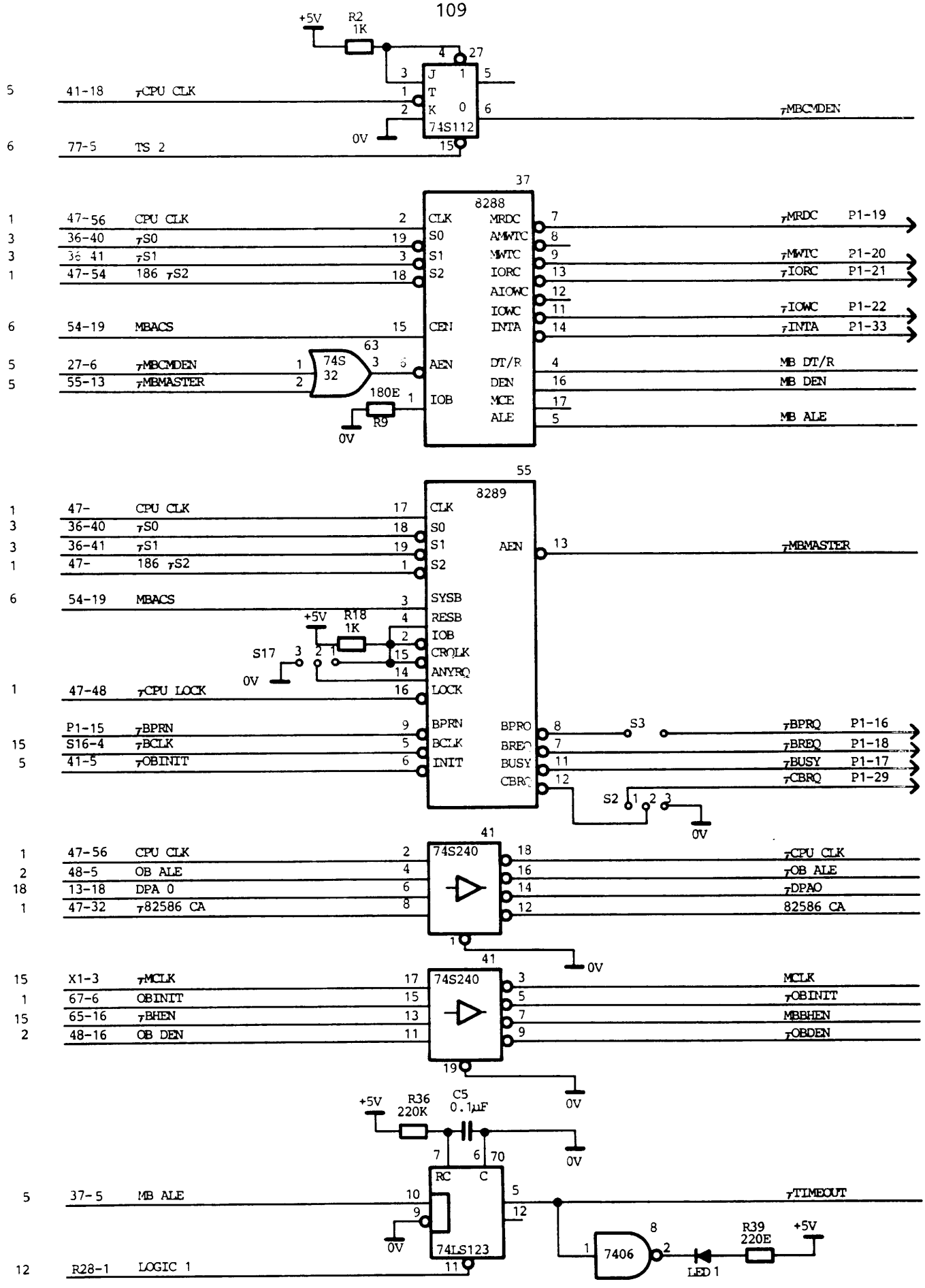
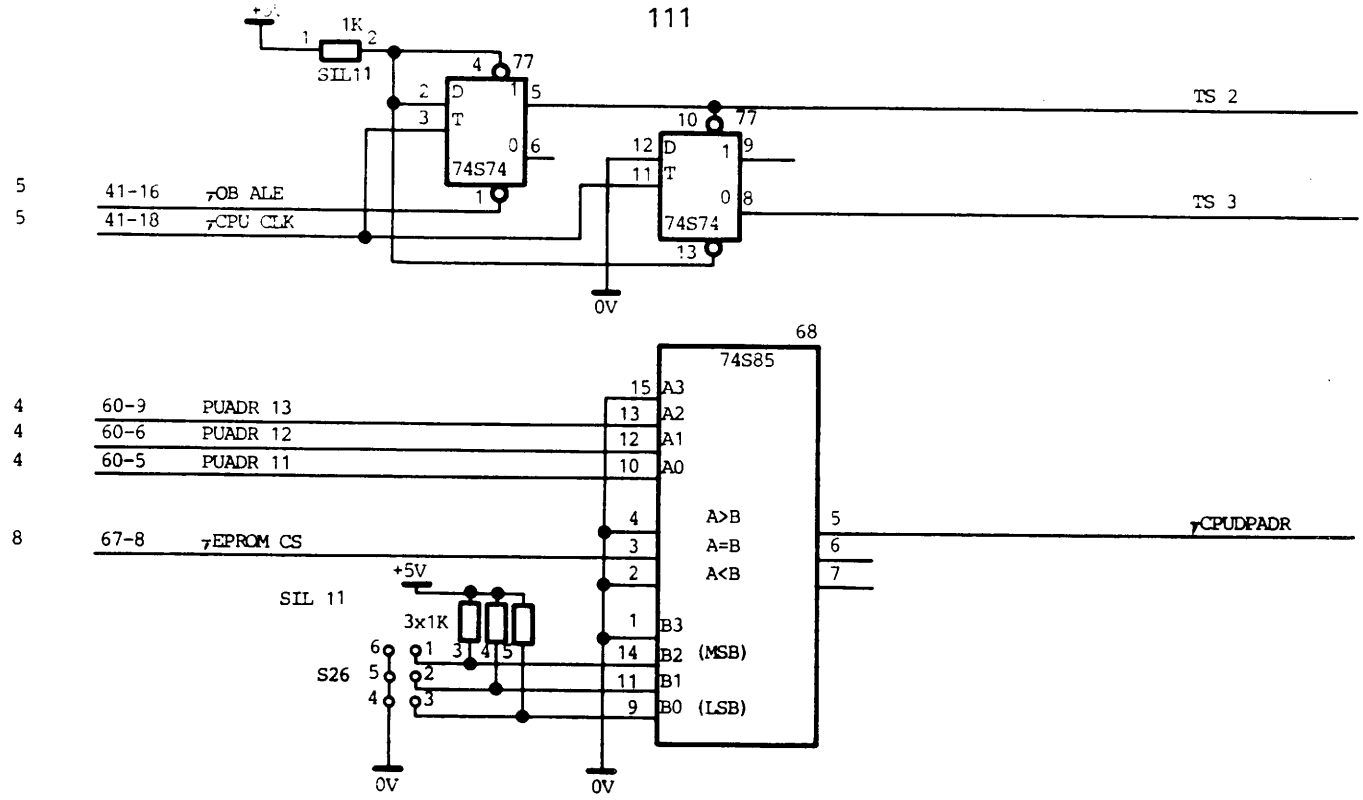
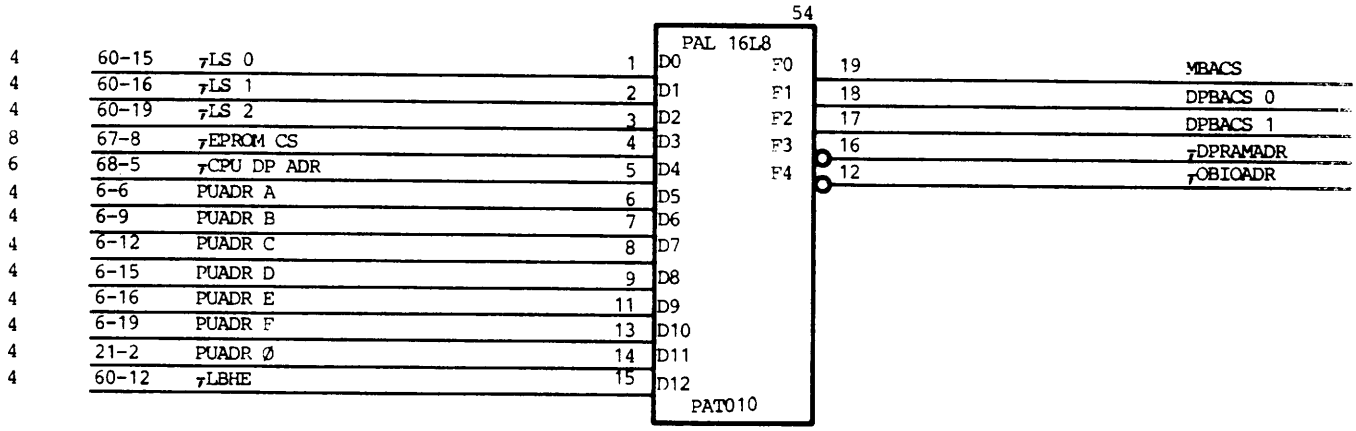

21
74S373
3 36-22 AD 0 3
3 36-21 AD 1 4
3 36-20 AD 2 7
3 36-19 AD 3 8
3 36-18 AD 4 13
3 36-17 AD 5 14
3 36-16 AD 6 17
3 36-15 AD 7 18
2 PUADR 0
5 PUADR 1
6 PUADR 2
9 PUADR 3
12 PUADR 4
15 PUADR 5
16 PUADR 6
19 PUADR 7
11 1
0V
6
74S373
3 36-14 AD 8 3
3 36-13 AD 9 4
3 36-11 AD A 7
3 36-10 AD B 8
3 36-9 AD C 13
3 36-8 AD D 14
3 36-7 AD E 17
3 36-6 AD F 18
2 PUADR 8
5 PUADR 9
6 PUADR A
9 PUADR B
12 PUADR C
15 PUADR D
16 PUADR E
19 PUADR F
11 1
0V
60
74S373
3 36-5 A 10 3
3 36-4 A 11 4
3 36-3 A 12 7
3 36-2 A 13 8
3 36-44 ₇BHE 13
3 36-40 ₇S0 14
3 36-41 ₇S1 17
1 47-54 186 ₇S2 18
2 48-5 0B ALE
G E
11 1
0V
2 PUADR 10
5 PUADR 11
6 PUADR 12
9 PUADR 13
12 ₇LBHE
15 ₇LS0
16 ₇LS1
19 ₇LS2
58
74LS245
3 36-22 AD 0 2
3 36-21 AD 1 3
3 36-20 AD 2 4
3 36-19 AD 3 5
3 36-18 AD 4 6
3 36-17 AD 5 7
3 36-16 AD 6 8
3 36-15 AD 7 9
OE T
19 1
18 IODAT 0
17 IODAT 1
16 IODAT 2
15 IODAT 3
14 IODAT 4
13 IODAT 5
12 IODAT 6
11 IODAT 7
46
74LS245
3 36-14 AD 8 2
3 36-13 AD 9 3
3 36-11 AD A 4
3 36-10 AD B 5
3 36-9 AD C 6
3 36-8 AD D 7
3 36-7 AD E 8
3 36-6 AD F 9
7 63-6 ₇IODEN
2 48-4 0B DT/R
19 1
18 IODAT 8
17 IODAT 9
16 IODAT A
15 IODAT B
14 IODAT C
13 IODAT D
12 IODAT E
11 IODAT F

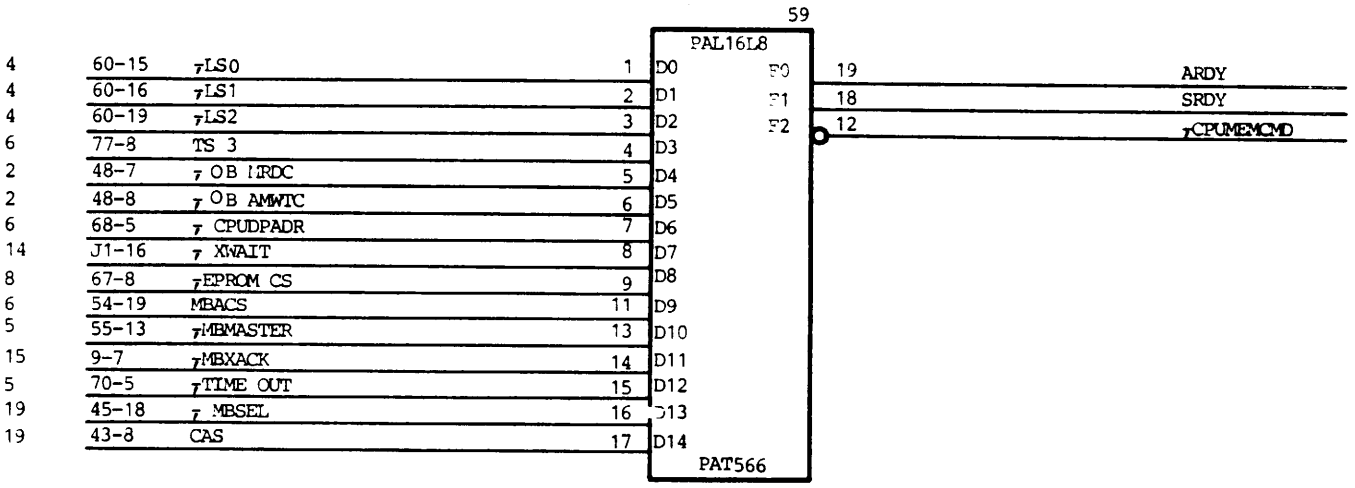
SIGNAL	DESTINATION	DESCRIPTION
		The 8288 bus controller on this page constitute the bus controller for the Multibus. The 80186, 82586 bus cycle status signals are wired together driving the 8288 bus controller. The 8288 is only enabled when the multibus is requested (MBACS active high and ₇AEN input active low)
₇MBCMDEN	P5	Multibus command enable. This signal ensures that command outputs of the 8288 are correctly enabled when the 8289 arbiter is strapped to retain control of the multibus until another bus master pulls ₇CBREQ low. The signal is inactive from leading edge of OB ALE and until the midle of T2.
₇MRDC	Plug 1-19	Memory read command to Multibus.
₇MWTC	Plug 1-20	Memory Write command to Multibus.
₇IORC	Plug 1-21	I/O read command to Multibus.
₇IOWC	Plug 1-22	I/O write command to Multibus.
₇INTA	Plug 1-33	Interrupt acknowledge to Multibus. This signal is used only with multibus devices which supports bus vectored interrupts. ETC does not support bus vectored multibus interrupts neither as master nor as slave.
MB DT/R	P7	Multibus data transmit/receive. Via gates on diagram page 7 this signal establishes the direction of data flow through the data tranceivers for the Multibus, when ETC is master.
MB DEN	P7	Multibus data enable. This signal serves via gates on diagram page 7 to enable Multibus data transceivers, when ETC is master.
MB ALE	P5	Multibus address load enable. This signal, which is generated in any 80186, 82586 bus cycle, is only used to re-trigger the time-out delay.
₇MBMASTER	P5,P6,P7,P15	Multibus master signal, which is active low when the ETC is master on the multibus.
₇BPRO	Plug 1-16	BUS priority out signal used with serial (daisy chain) bus priority resolution schemes. ₇BPRO is passed to the ₇BPRN input of the master with the next lower bus priority.
₇BREQ	Plug 1-18	BUS request is used with parallel priority resolution scheme to request the Multibus.
₇BUSY	Plug 1-17	BUS busy is activated when the ETC is multibus master, which prevent other masters from gaining control of the bus. This line is also an input line driven by other bus masters when they acquire the bus.
₇CBRQ	Plug 1-29	Common bus request is used to allow a bus master to retain control of the multibus without contending for it each processor cycle, as long as no other master is requesting control of the bus. A bus master requesting control of the multibus but not currently controlling it, activates ₇CBRQ (low), and since ₇CBRQ is also an input line this causes the controlling bus master to relinquish control of the bus.
₇CPU CLK	P5,P6,P19	Inverted CPU clock signal.
₇OB ALE	P6	Inverted On Board address load enable aignal used to reset TS2, TS3 timing flip flops.
₇DPA Ø	P7	Inverted dual port address bit 0.
82586 CA	P2	Channel attention to 82586. The 80186 generates the 82586 channel attention signal to initiate execution by the 82586 of memory resident command blocks.
MCLK	P14, P15	10 Mhz clock signal to ISBX multimodule board.
₇OBINIT	P5, P10, P12 P13, P16, P20	Inverted On Board initialize signal. Refer to description on page 1.
MBBHEN	P7, P19	Multibus Byte High Enable signal used to select the upper byte (bits 8-F) of a 16 bit word.
₇OBDEN	P7, P8	Inverted On Board data enable signal. The signal serves to enable I/O data bus transceivers. EPROM data is also enabled onto the multiplexed bus using this signal.
₇TIMEOUT	P6	The Time Out MMV is retriggered in every 80186, 82586 bus cycle, which keeps the ₇TIME OUT signal inactive and the RUN indicator turned on. The ₇TIME OUT signal causes generation of a ready signal to one of the processors if a multibus cycle acknowledge signal is not generated as a response to a multibus request. Time out period is app.10 mS.


+5V
R2
1K
74S112
0V
41-18 ₇CPU CLK
77-5 TS 2
₇MBCMDEN
8288
CLK
S0
S1
S2
CEN
AEN
IOB
MRDC
AMWTC
MWTC
IORC
AIOWC
IOWC
INTA
DT/R
DEN
MCE
ALE
47-56 CPU CLK
36-40 ₇S0
36-41 ₇S1
47-54 186 ₇S2
54-19 MBACS
27-6 ₇MBCMDEN
55-13 ₇MBMASTER
74S 32
180E
R9
₇MRDC P1-19
₇MWTC P1-20
₇IORC P1-21
₇IOWC P1-22
₇INTA P1-33
MB DT/R
MB DEN
MB ALE
8289
47- CPU CLK
36-40 ₇S0
36-41 ₇S1
47- 186 ₇S2
54-19 MBACS
47-48 ₇CPU LOCK
P1-15 ₇BPRN
S16-4 ₇BCLK
41-5 ₇OBINIT
SYSB
RESB
IOB
CRQLK
ANYRQ
LOCK
BPRN
BCLK
INIT
AEN
BPRO
BREQ
BUSY
CBRQ
R18
1K
S17
S2
S3
₇MBMASTER
₇BPRQ P1-16
₇BREQ P1-18
₇BUSY P1-17
₇CBRQ P1-29
74S240
47-56 CPU CLK
48-5 OB ALE
13-18 DPA 0
47-32 ₇82586 CA
₇CPU CLK
₇OB ALE
₇DPA0
82586 CA
X1-3 ₇MCLK
67-6 OBINIT
65-16 ₇BHEN
48-16 OB DEN
MCLK
₇OBINIT
MBBHEN
₇OBDEN
R36
220K
C5
0.1µF
RC
C
74LS123
37-5 MB ALE
R28-1 LOGIC 1
₇TIMEOUT
7406
R39
220E
LED 1

SIGNAL	DESTINATION	DESCRIPTION
TS 2 TS 3	P5 P6	TS2,3 are timing flip flops. They are cleared at the beginning of T1 in a bus cycle. TS 2 is set at the beginning of T2 and TS3 at the beginning of T3.TS2 is used to generate the ₇ MBCMDEN signal (refer to description on page 5). TS3 is used in the ready logic.
₇ CPUDPADR	P6, P19	CPU dual port address. ₇ CPUDPADR is active low during access to on board RAM memory.
MBACS	P5, P6	Multibus access. MBACS is active high during access of the Multibus. The signal serves to request multibus access via the 8289 arbiter, to enable the 8288 Multibus controller and to control the ready signal during multibus access.
DBACS 0,1	P7	On Board dual port bus access. The signals control enabling of the on board dual port data bus transceivers.
₇ DPRAMADR	P19	Dual port RAM address. This signal serves to enable write pulses to RAM and to enable RAM data onto the on Board dual port data bus during 80186 or 82586 access of on board RAM.
₇ OBIOADR	P7	On Board I/O address. This signal is active low during 80186 access to on board I/O devices. The signal controls enabling of the I/O data bus transceivers. The Ready and Memory Command decoding PAL on this page generates the ready signals to the 80186 CPU and the 82586 LCC. The asynchronous ready signal is generated during access of the Multibus and the iSBX multimodule. The synchronous ready signal is generated during 80186 INTA cycles and access of on board RAM. ARDY or SRDY must be active high to terminate a bus cycle. ARDY and SRDY are both high during access of EPROM which causes no waite state generation. The 80186 has an internal ready generator, which operates in parallel with the external ready generator. The internal ready generator inserts wait state during 80186 access to on board I/O devices.
ARDY	P1, P2	Asynchronous ready.
SRDY	P1, P2	Synchronous ready.
₇ CPUMEMCMD	P19	CPU memory command. This signal is active low during 80186 or 82586 memory read/write commands. The signal serves to enable the Dual-Port DRAM controller PAL during 80186, 82586 RAM access.


+5V
1K
SIL11
74S74
TS 2
TS 3
5 41-16 7OB ALE
5 41-18 7CPU CLK
0V
68
74S85
4 60-9 PUADR 13
4 60-6 PUADR 12
4 60-5 PUADR 11
8 67-8 7EPROM CS
A>B
A=B
A<B
5
6
7
7CPUDPADR
SIL 11
3x1K
S26
B3
B2 (MSB)
B1
B0 (LSB)
0V
0V


54
PAL 16L8
4 60-15 7LS 0
4 60-16 7LS 1
4 60-19 7LS 2
8 67-8 7EPROM CS
6 68-5 7CPU DP ADR
4 6-6 PUADR A
4 6-9 PUADR B
4 6-12 PUADR C
4 6-15 PUADR D
4 6-16 PUADR E
4 6-19 PUADR F
4 21-2 PUADR Ø
4 60-12 7LBHE
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12
F0 F1 F2 F3 F4
19 18 17 16 12
MBACS
DPBACS 0
DPBACS 1
7DPRAMADR
7OBIOADR
PAT010


59
PAL16L8
4 60-15 7LS0
4 60-16 7LS1
4 60-19 7LS2
6 77-8 TS 3
2 48-7 7 OB MRDC
2 48-8 7 OB AMWTC
6 68-5 7 CPUDPADR
14 J1-16 7 XWAIT
8 67-8 7EPROM CS
6 54-19 MBACS
5 55-13 7MBMASTER
15 9-7 7MBXACK
5 70-5 7TIME OUT
19 45-18 7 MBSEL
19 43-8 CAS
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14
F0 F1 F2
19 18 12
ARDY
SRDY
7CPUMEMCMD
PAT566

SIGNAL	DESTINATION	DESCRIPTION
$\overline{7}$ IODEN	P4	I/O data enable. This signal when low enables I/O data bus transceivers.
$\overline{7}$ DPDEN 0,1	P17	Dual port data enable. These signals when low enable the On Board dual port bus transceivers.
$\overline{7}$ MBLBEN	P17	Multibus low byte enable. This signal serves to enable Multibus low byte (0-7) data transceiver.
$\overline{7}$ MBSWAP	P17	Multibus swap byte enable. This signal serves to enable the Multibus swap byte transceiver.
$\overline{7}$ MBHBEN	P17	Multibus high byte enable. This signal serves to enable the Multibus high byte (8-F) data transceiver.
$\overline{7}$ MBADREN	P18	Multibus address enable. This signal serves to enable the Multibus address transceivers.
MBDTRM	P17	Multibus data transmit/receive. This signal establishes the direction of data flow through the Multibus data transceivers.
MBSEL	P7,P18, P21	Multibus Select. This signal is generated when the ETC dual port RAM is accessed via the Multibus (ETC is slave).

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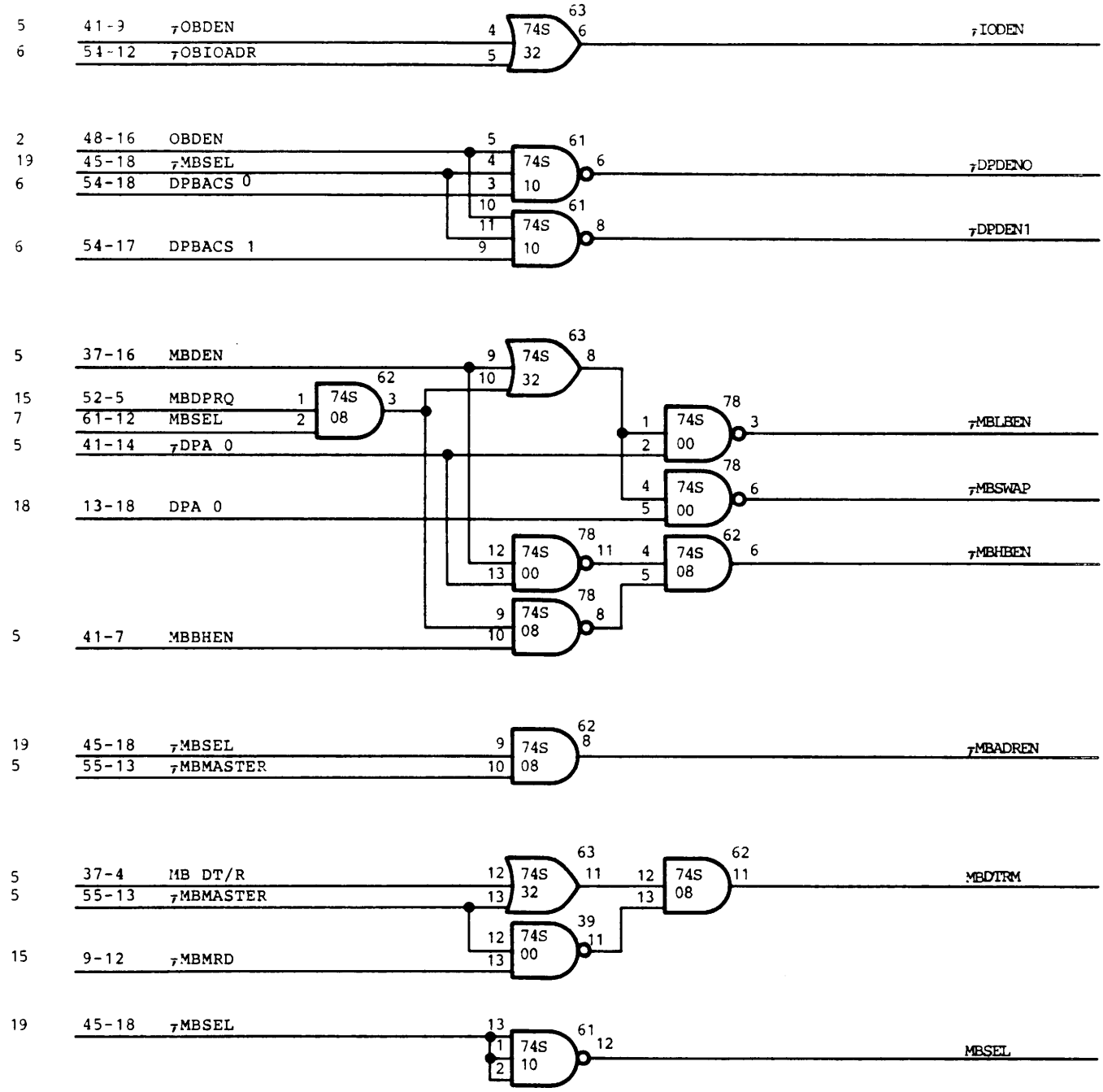
Unit		
ETC601/611	BUS TRANSCEIVER	PAGE 7
Dwg. No.	and	
A26358	DRIVER CONTROL SIGNALS	


5 41-3 ~OBDEN
6 54-12 ~OBIOADR
63 74S 32
~IODEN
2 48-16 OBDEN
19 45-18 ~MBSEL
6 54-18 DPBACS 0
6 54-17 DPBACS 1
61 74S 10
~DPDEN0
~DPDEN1
5 37-16 MBDEN
15 52-5 MBDPRQ
7 61-12 MBSEL
5 41-14 ~DPA 0
18 13-18 DPA 0
5 41-7 MBBHEN
62 74S 08
78 74S 00
~MBLBEN
~MBSWAP
~MBHBEN
19 45-18 ~MBSEL
5 55-13 ~MBMASTER
~MBADREN
5 37-4 MB DT/R
5 55-13 ~MBMASTER
15 9-12 ~MBMRD
39 74S 00
MBDTRM
19 45-18 ~MBSEL
MBSEL

SIGNAL	DESTINATION	DESCRIPTION
EPROM DAT 0- EPROM DAT F	P3	EPROM data is gated onto the multiplexed bus during 80186 CPU or 82586 read access of EPROM.
$\overline{7}$ EPROM CS	P6	EPROM Chip Select signal.

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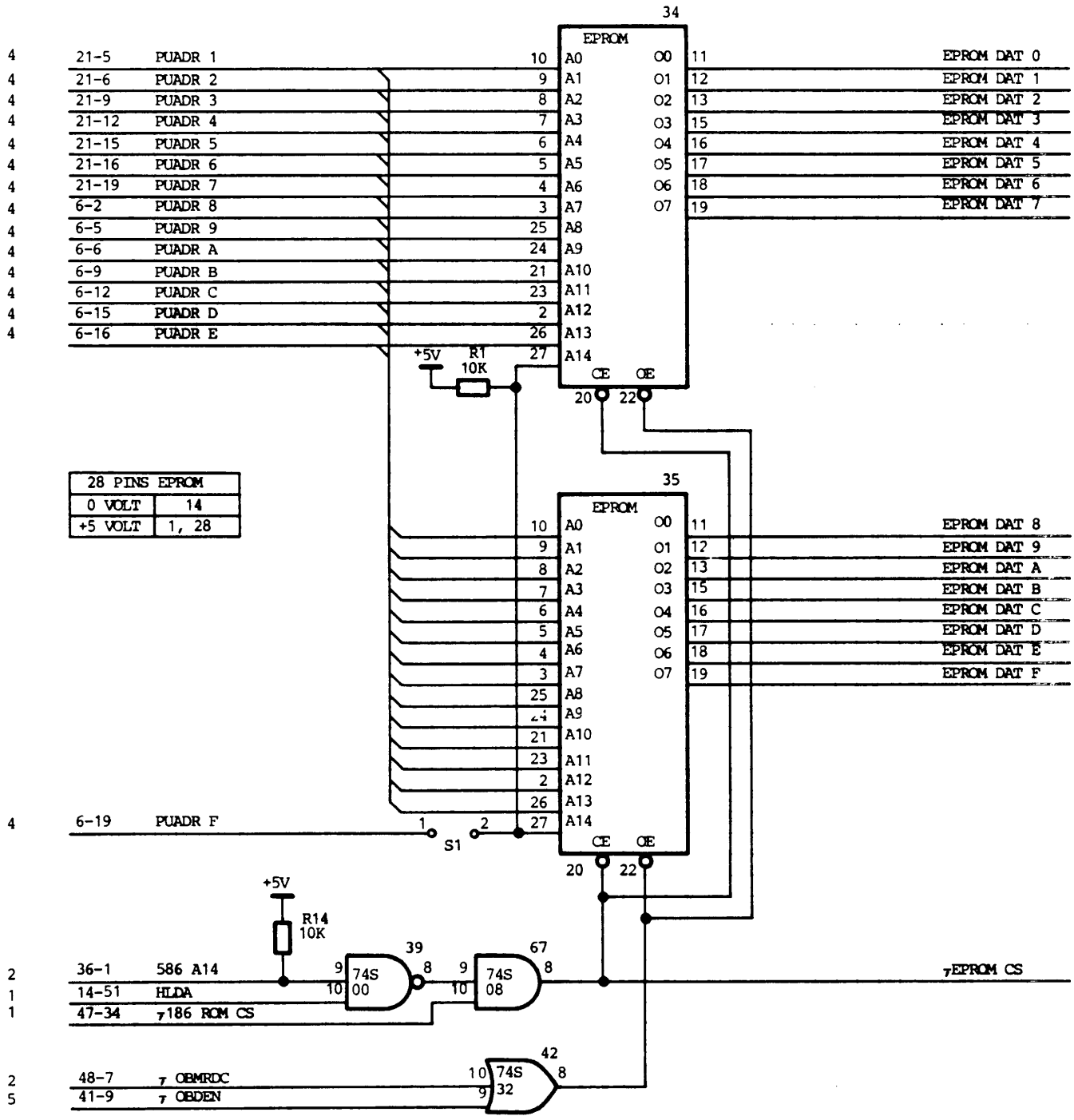
34
EPROM
4 21-5 PUADR 1
4 21-6 PUADR 2
4 21-9 PUADR 3
4 21-12 PUADR 4
4 21-15 PUADR 5
4 21-16 PUADR 6
4 21-19 PUADR 7
4 6-2 PUADR 8
4 6-5 PUADR 9
4 6-6 PUADR A
4 6-9 PUADR B
4 6-12 PUADR C
4 6-15 PUADR D
4 6-16 PUADR E
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
O0 O1 O2 O3 O4 O5 O6 O7
CE OE
EPROM DAT 0
EPROM DAT 1
EPROM DAT 2
EPROM DAT 3
EPROM DAT 4
EPROM DAT 5
EPROM DAT 6
EPROM DAT 7
+5V R1 10K
28 PINS EPROM
0 VOLT 14
+5 VOLT 1, 28
35
EPROM
EPROM DAT 8
EPROM DAT 9
EPROM DAT A
EPROM DAT B
EPROM DAT C
EPROM DAT D
EPROM DAT E
EPROM DAT F
4 6-19 PUADR F
S1
+5V R14 10K
2 36-1 586 A14
1 14-51 HLDA
1 47-34 7186 ROM CS
39 74S 00
67 74S 08
7EPROM CS
2 48-7 7 OBMRDC
5 41-9 7 OBDEN
42 74S 32

SIGNAL	DESTINATION	DESCRIPTION
		This diagram shows the 8259A Programmable Interrupt Controller. Every interrupt to the PIC passes a strap field making interrupt sources and priority levels user selectable and configureable. This diagram also contains buffers for reception and generation of Multibus interrupts.
INT 0	P1	This signal becomes active high whenever a valid interrupt request is asserted (IR0-IR7). The signal serves to interrupt the 80186 CPU via its interrupt input 0 line.
MBINT 0 - MBINT 7	P9	Multibus interrupt 0-7.
NMI	P1	Non Maskable Interrupt to the 80186 CPU.
IR0 - IR7	P 9	Interrupt request 0-7 to the 8259 PIC.

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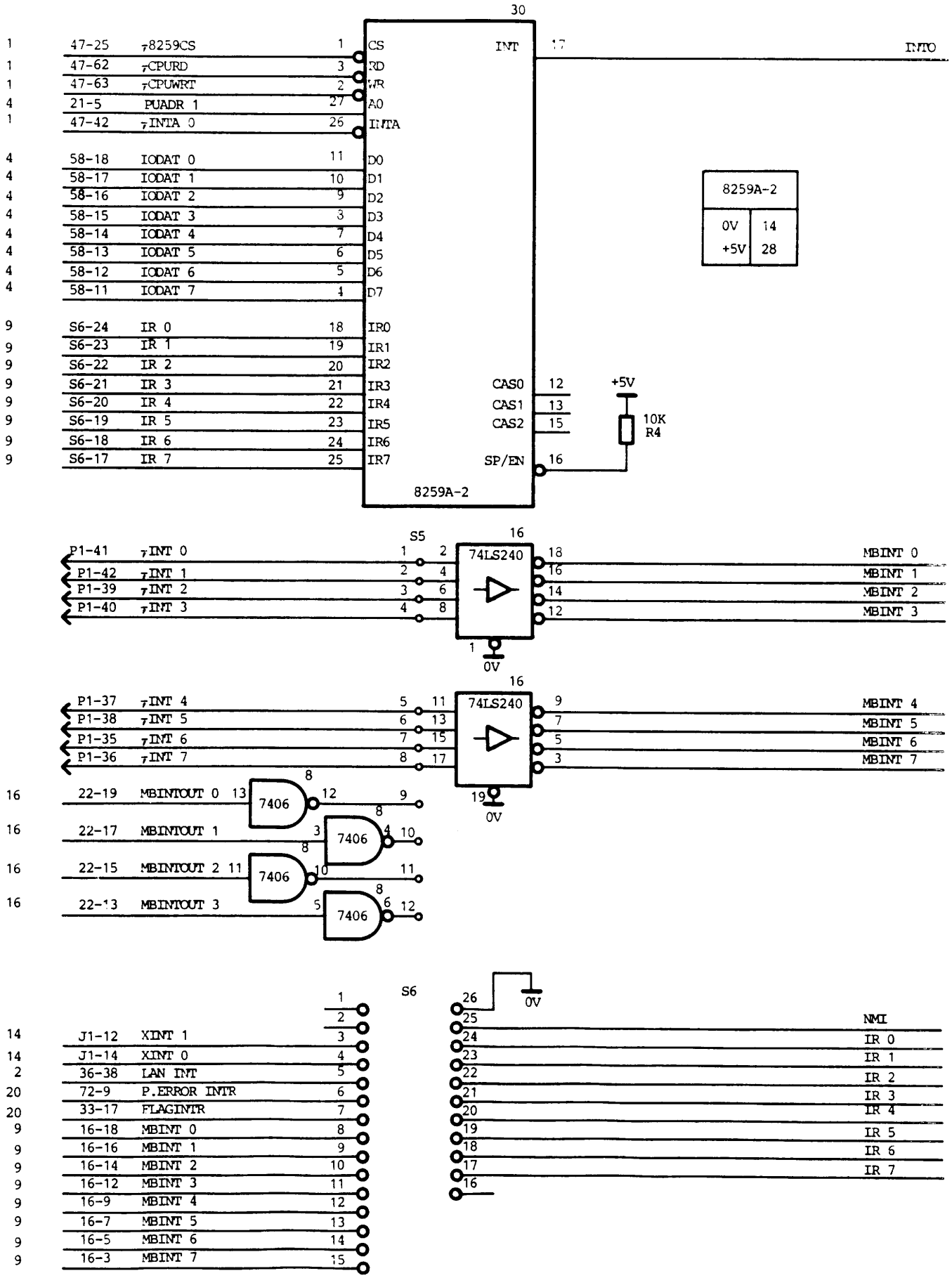
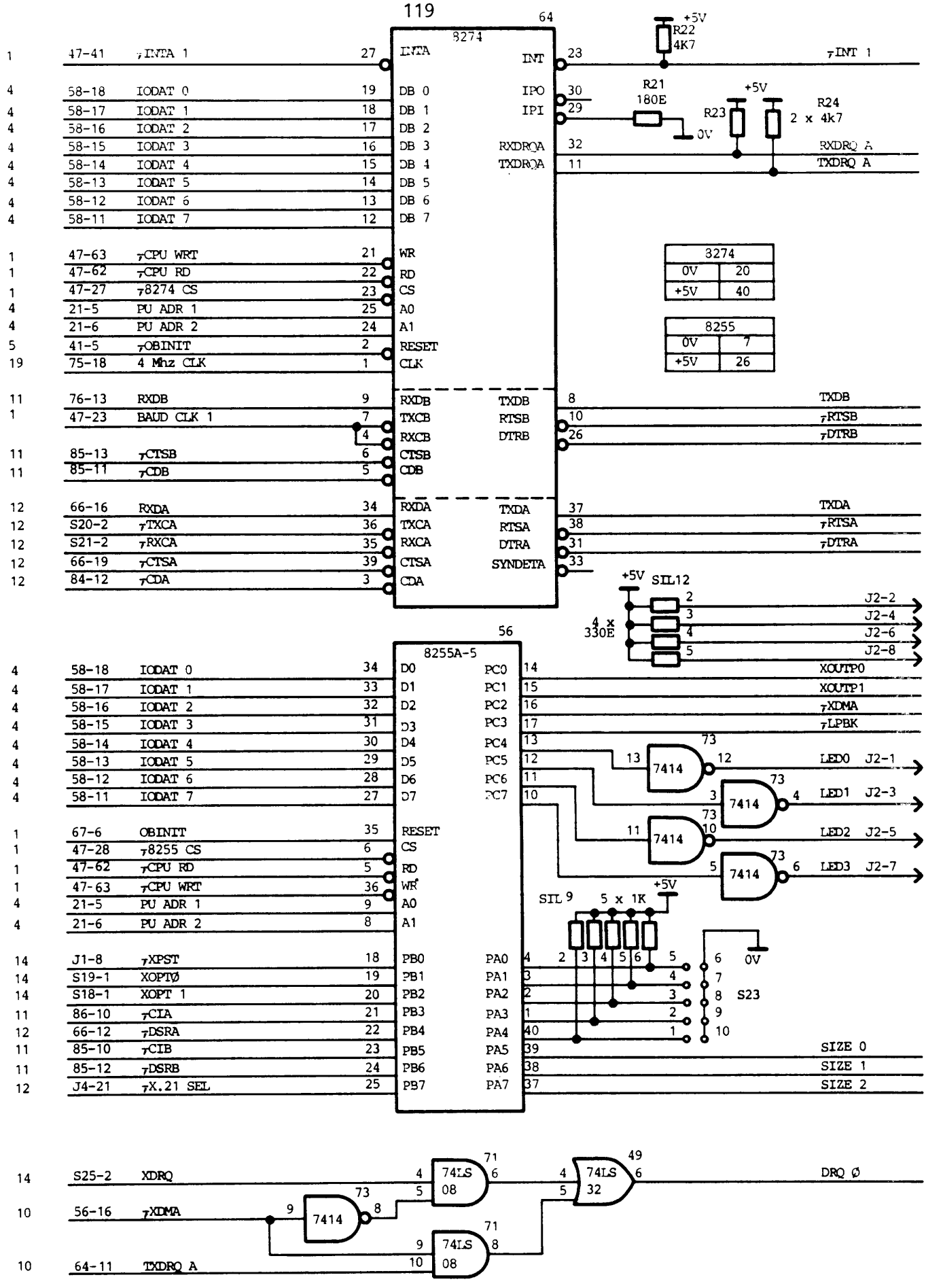
Unit		
EIC601/611	ON BOARD INTERRUPT CONTROLLER	PAGE 9
Dwg. No. A26360		

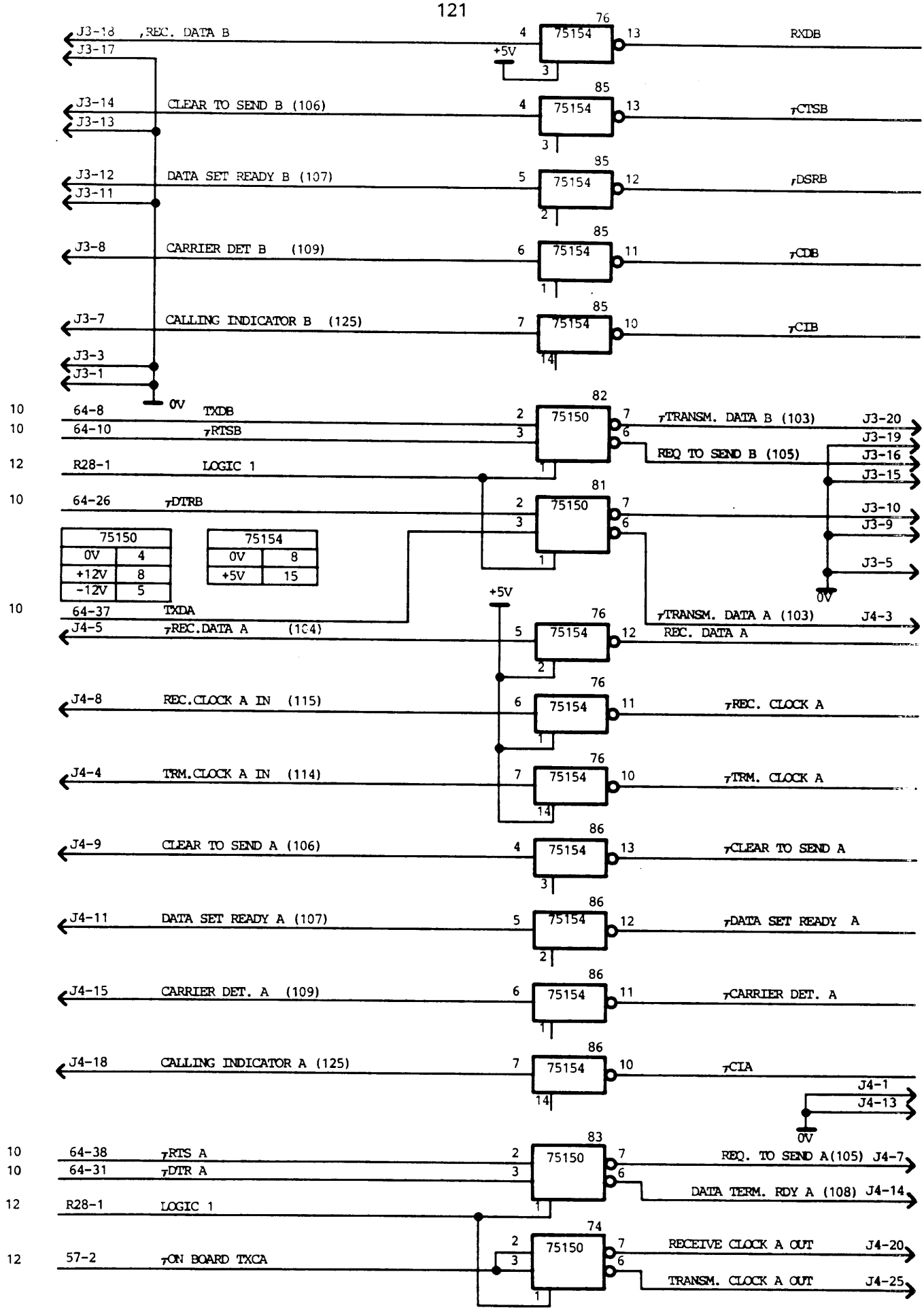

30
1 47-25 ₇8259CS 1 CS
1 47-62 ₇CPURD 3 RD
1 47-63 ₇CPUWRT 2 WR
4 21-5 PUADR 1 27 A0
1 47-42 ₇INTA 0 26 INTA
INT 17 INTO
4 58-18 IODAT 0 11 D0
4 58-17 IODAT 1 10 D1
4 58-16 IODAT 2 9 D2
4 58-15 IODAT 3 3 D3
4 58-14 IODAT 4 7 D4
4 58-13 IODAT 5 6 D5
4 58-12 IODAT 6 5 D6
4 58-11 IODAT 7 4 D7
8259A-2
0V 14
+5V 28
9 S6-24 IR 0 18 IR0
9 S6-23 IR 1 19 IR1
9 S6-22 IR 2 20 IR2
9 S6-21 IR 3 21 IR3
9 S6-20 IR 4 22 IR4
9 S6-19 IR 5 23 IR5
9 S6-18 IR 6 24 IR6
9 S6-17 IR 7 25 IR7
CAS0 12
CAS1 13
CAS2 15
SP/EN 16
+5V
10K
R4
8259A-2
S5
16
P1-41 ₇INT 0 1 2
P1-42 ₇INT 1 2 4
P1-39 ₇INT 2 3 6
P1-40 ₇INT 3 4 8
74LS240
18 MBINT 0
16 MBINT 1
14 MBINT 2
12 MBINT 3
1 0V
16
P1-37 ₇INT 4 5 11
P1-38 ₇INT 5 6 13
P1-35 ₇INT 6 7 15
P1-36 ₇INT 7 8 17
74LS240
9 MBINT 4
7 MBINT 5
5 MBINT 6
3 MBINT 7
19 0V
8
16 22-19 MBINTOUT 0 13 7406 12 9
8
16 22-17 MBINTOUT 1 3 7406 4 10
8
16 22-15 MBINTOUT 2 11 7406 10 11
8
16 22-13 MBINTOUT 3 5 7406 6 12
1
2
14 J1-12 XINT 1 3
14 J1-14 XINT 0 4
2 36-38 LAN INT 5
20 72-9 P.ERROR INTR 6
20 33-17 FLAGINTR 7
9 16-18 MBINT 0 8
9 16-16 MBINT 1 9
9 16-14 MBINT 2 10
9 16-12 MBINT 3 11
9 16-9 MBINT 4 12
9 16-7 MBINT 5 13
9 16-5 MBINT 6 14
9 16-3 MBINT 7 15
S6
26 0V
25 NMI
24 IR 0
23 IR 1
22 IR 2
21 IR 3
20 IR 4
19 IR 5
18 IR 6
17 IR 7
16

SIGNAL	DESTINATION	DESCRIPTION
₇ INT 1	P12	This signal becomes active low when the highest priority internal interrupt of the 8274 MPSC requires service. The signal serves to interrupt the 80186 CPU via its interrupt input 1 line.
RXDRQ A	P1	Receiver channel A DMA request. This signal requests a DMA transfer of data for a receive operation for channel A.
TXDRQ A	P 10	Transmit channel A DMA request. This signal requests a DMA transfer of data for transmit operation for channel A.
TXDB	P11	Transmit data channel B. This line transmits the serial data from communications channel B. (The console channel)
₇ RTSB	P11	Request to send channel B signals ready to send data.
₇ DTRB	P11	Data terminal ready channel B.
TXDA	P11,P12	Transmit data channel A. This line transmits the serial data from communications channel A. (the synchronous X.21/V.24 channel). The negative going edge of TXCA (transmit clock) shifts data out of the 8274 MPSC shift register to TXDA.
₇ RTSA	P11,P12	Request to send channel A signals ready to send data.
₇ DTRA	P11,P12	Data terminal ready channel A. If the 8274 MPSC channel A operates in V.24/V.28 mode this signal controls the V.24 circuit data terminal ready. In X.21 mode the signal controls the X.21 circuit C (Control) via the synchronization FF on diagram 12.
XOUTP0, XOUTP1	P14	Optional output lines to the iSBX Multimodule board.
₇ XDMA	P10	This signal when low assigns 80186 CPU DMA channel 0 to the iSBX Multimodule. When the signal is high the DMA channel is assigned to the 8274 MPSC transmit channel A.
₇LPBK	P13	Loop back. This signal when active low enables the loop back mode of the ESI (Ethernet Sereial Interface) or the MSI (Micronet Serial interface).
LED 0 LED 1 LED 2 LED 3	Jack 2-1 Jack 2-3 Jack 2-5 Jack 2-7	Drivers for four light emitting diodes not located on the ETC PCB.
Size 0 - Size 2	P15	These lines are inputs to the 8255 PPI. The lines originate from a strap on diagram 15. This strap determines the amount of ETC on board RAM, which is available to the multibus master.
DRQ 0	P1	DMA request 0 to 80186 CPU. Refer to the description of ₇ XDMA this page.

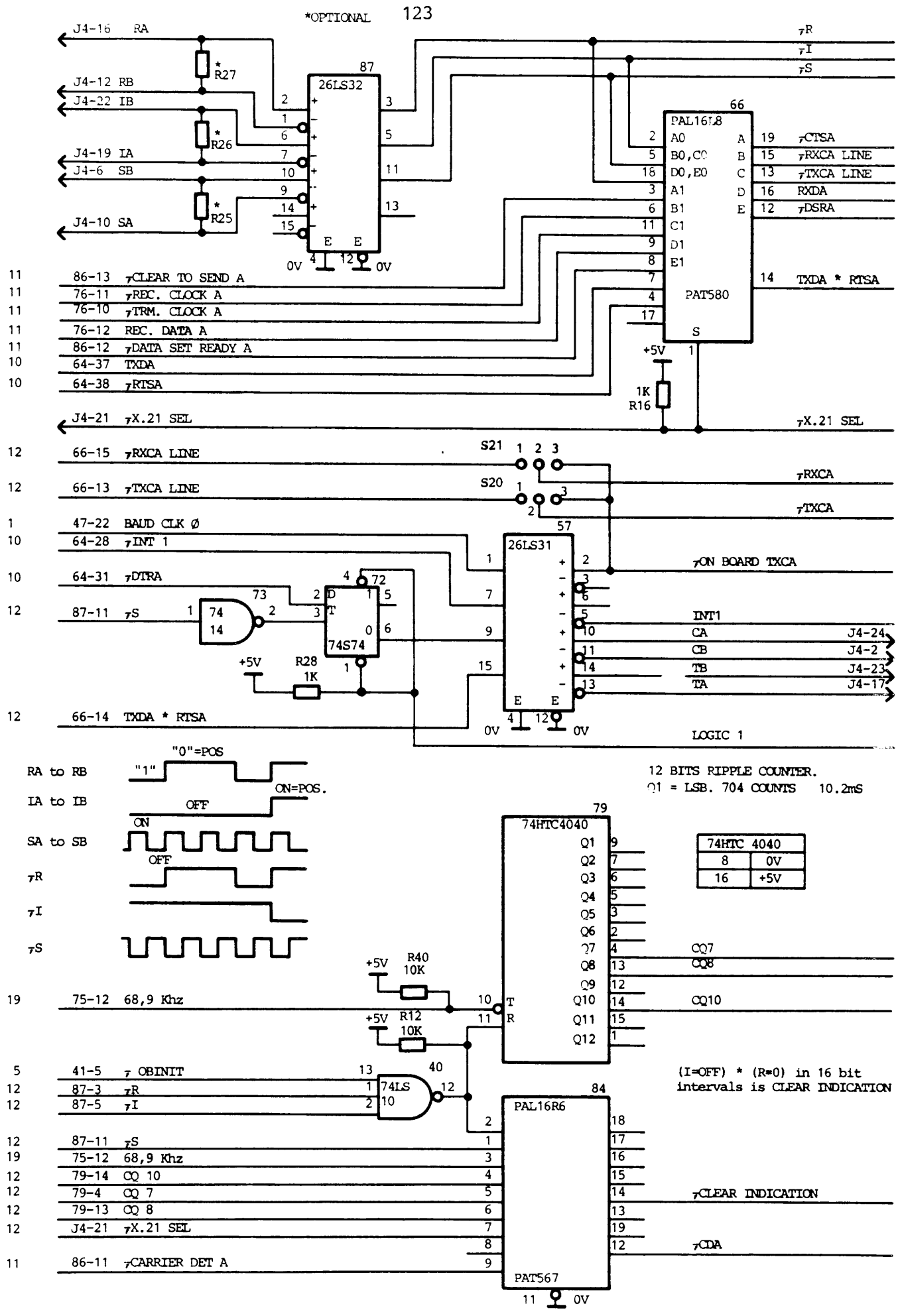


1	47-41	₇INTA 1	27	INTA	INT	23	₇INT 1
4	58-18	IODAT 0	19	DB 0	IPO	30	
4	58-17	IODAT 1	18	DB 1	IPI	29	
4	58-16	IODAT 2	17	DB 2			
4	58-15	IODAT 3	16	DB 3	RXDRQA	32	RXDRQ A
4	58-14	IODAT 4	15	DB 4	TXDRQA	11	TXDRQ A
4	58-13	IODAT 5	14	DB 5			
4	58-12	IODAT 6	13	DB 6			
4	58-11	IODAT 7	12	DB 7			
1	47-63	₇CPU WRT	21	WR			
1	47-62	₇CPU RD	22	RD			
1	47-27	₇8274 CS	23	CS			
4	21-5	PU ADR 1	25	A0			
4	21-6	PU ADR 2	24	A1			
5	41-5	₇OBINIT	2	RESET			
19	75-18	4 Mhz CLK	1	CLK			
11	76-13	RXDB	9	RXDB	TXDB	8	TXDB
1	47-23	BAUD CLK 1	7	TXCB	RTSB	10	₇RTSB
			4	RXCB	DTRB	26	₇DTRB
11	85-13	₇CTSB	6	CTSB			
11	85-11	₇CDB	5	CDB			
12	66-16	RXDA	34	RXDA	TXDA	37	TXDA
12	S20-2	₇TXCA	36	TXCA	RTSA	38	₇RTSA
12	S21-2	₇RXCA	35	RXCA	DTRA	31	₇DTRA
12	66-19	₇CTSA	39	CTSA	SYNDETA	33	
12	84-12	₇CDA	3	CDA			
4	58-18	IODAT 0	34	D0	PC0	14	XOUTP0
4	58-17	IODAT 1	33	D1	PC1	15	XOUTP1
4	58-16	IODAT 2	32	D2	PC2	16	₇XDMA
4	58-15	IODAT 3	31	D3	PC3	17	₇LPBK
4	58-14	IODAT 4	30	D4	PC4	13	
4	58-13	IODAT 5	29	D5	PC5	12	LED0 J2-1
4	58-12	IODAT 6	28	D6	PC6	11	LED1 J2-3
4	58-11	IODAT 7	27	D7	PC7	10	LED2 J2-5
1	67-6	OBINIT	35	RESET			LED3 J2-7
1	47-28	₇8255 CS	6	CS			
1	47-62	₇CPU RD	5	RD			
1	47-63	₇CPU WRT	36	WR			
4	21-5	PU ADR 1	9	A0			
4	21-6	PU ADR 2	8	A1			
14	J1-8	₇XPST	18	PB0	PA0	4	
14	S19-1	XOPTØ	19	PB1	PA1	3	
14	S18-1	XOPT 1	20	PB2	PA2	2	
11	86-10	₇CIA	21	PB3	PA3	1	
12	66-12	₇DSRA	22	PB4	PA4	40	
11	85-10	₇CIB	23	PB5	PA5	39	SIZE 0
11	85-12	₇DSRB	24	PB6	PA6	38	SIZE 1
12	J4-21	₇X.21 SEL	25	PB7	PA7	37	SIZE 2
14	S25-2	XDRQ					DRQ Ø
10	56-16	₇XDMA					
10	64-11	TXDRQ A					

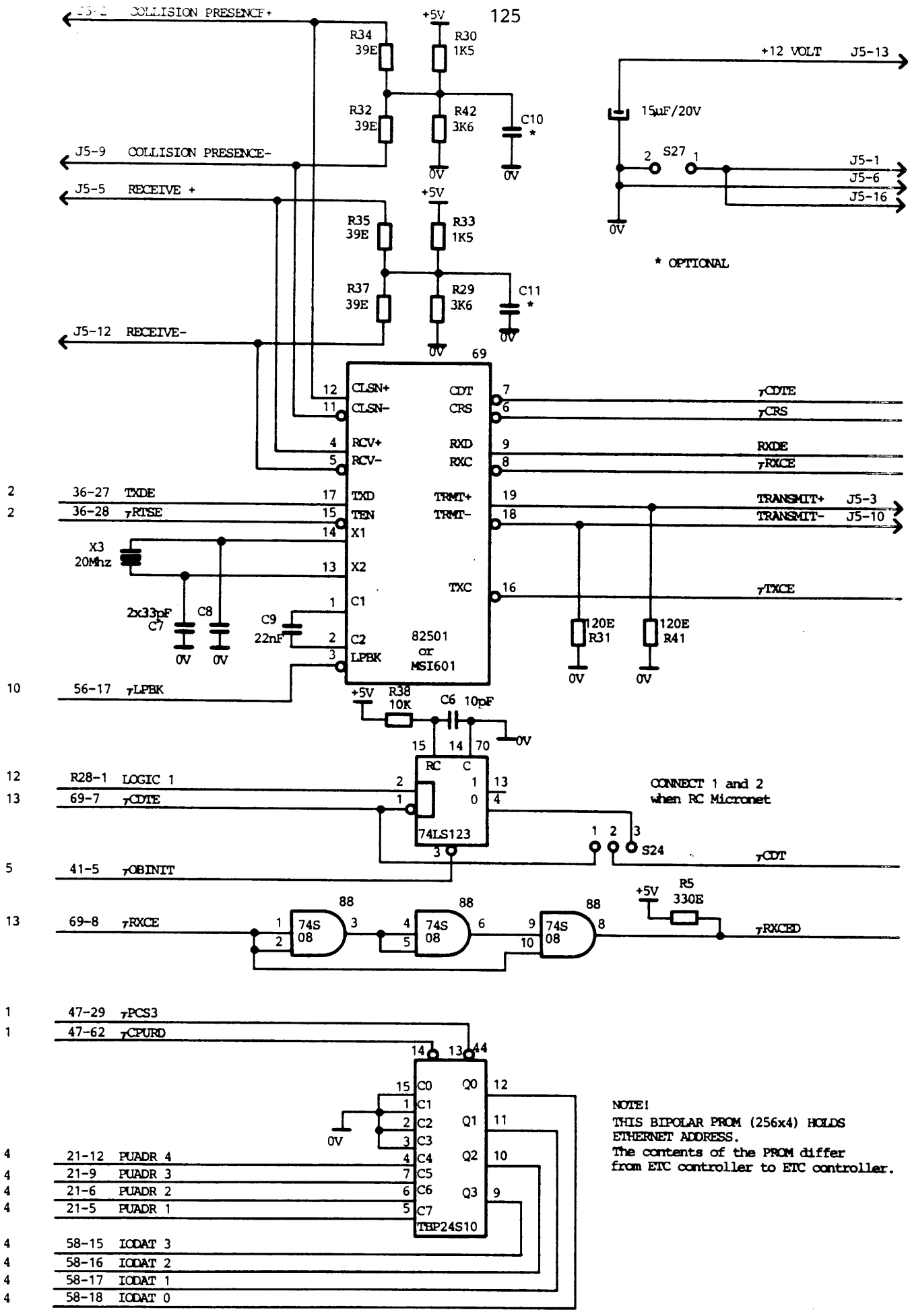
SIGNAL	DESTINATION	DESCRIPTION
RXDB	P10	Receive serial data channel B.
7 CTSB	P10	Clear to send channel B.
7 DSRB	P10	Data set ready channel B.
7 CDB	P10	Carrier detect channel B.
7 CIB	P10	Calling indicator channel B.
7 TRANSM. DATA B	Jack 3-20	Transmitted serial data channel B. This line is app. -10 Volt when a "1" is transmitted, and +10 Volt when a "0" is transmitted.
REQ TO SEND B	Jack 3-16	Request to send channel B. This line is app. + 10Volt if the 8274 MPSC signals request to send else app. -10 Volt.
DATA TERM. RDY. B	JACK 3-10	Data terminal ready channel B. This line is app. +10 Volt if the 8274 MPSC signals data terminal ready else app. -10 Volt.
7 TRANSM. DATA A	Jack 4-3	Transmitted serial data channel B. This line is app. -10 Volt when a "1" is transmitted, and app. +10 Volt when a "0" is transmitted.
7 Rec. DATA A	P12	Receive serial data from the V.24/V.28 interface to 8274 channel A.
7 REC. CLOCK A	P12	Receiver clock from the V.24/V.28 interface to 8274 channel A.
7 TRM. CLOCK A	P12	Transmit clock from the V.24/V.28 interface to 8274 channel A.
7 CLEAR TO SEND A	P12	Clear to send from the V.24/V.28 interface to 8274 channel A.
7 DATA SET READY A	P12	Data set ready from the V.24/V.28 interface to 8274 channel A.
7 CARRIER DET. A	P12	Carrier detect from the V.24/V.28 interface to 8274 channel A.
7 CIA	P10	Calling indicator from the V.24/V.28 interface to 8274 channel A.
REQ. TO SEND A	Jack 4-7	Request to send channel A. This line is app. +10Volt if the 8274 signals request to send else app. -10 Volt.
DATA TERM. RDY A	Jack 4-14	Data terminal ready channel A. This line is app. +10 Volt if the 8274 MPSC signals data terminal ready else -10 Volt.
RECEIVE CLOCK A OUT	Jack 4-20	Receive clock channel A EIC source. The data communication equipment (DCE) shall present receive data A (Jack 4-5) in which transitions between signal elements nominel occur at the rising edge of this clock.
TRANSMIT. CLOCK A OUT	Jack 4-25	Transmit clock channel A EIC source. The falling edge of this clock indicates the centre of each signal element transmitted on data A (Jack 4-3).


J3-18 ,REC. DATA B
J3-17
J3-14 CLEAR TO SEND B (106)
J3-13
J3-12 DATA SET READY B (107)
J3-11
J3-8 CARRIER DET B (109)
J3-7 CALLING INDICATOR B (125)
J3-3
J3-1
0V
10 64-8 TXDB
10 64-10 ŗRTSB
12 R28-1 LOGIC 1
10 64-26 ŗDTRB
10 64-37 TXDA
J4-5 ŗREC.DATA A (104)
J4-8 REC.CLOCK A IN (115)
J4-4 TRM.CLOCK A IN (114)
J4-9 CLEAR TO SEND A (106)
J4-11 DATA SET READY A (107)
J4-15 CARRIER DET. A (109)
J4-18 CALLING INDICATOR A (125)
10 64-38 ŗRTS A
10 64-31 ŗDTR A
12 R28-1 LOGIC 1
12 57-2 ŗON BOARD TXCA
75150
0V 4
+12V 8
-12V 5
75154
0V 8
+5V 15
75154
75150
+5V
RXDB
ŗCTSB
ŗDSRB
ŗCDB
ŗCIB
ŗTRANSM. DATA B (103)
REQ TO SEND B (105)
J3-20
J3-19
J3-16
J3-15
J3-10
J3-9
J3-5
ŗTRANSM. DATA A (103)
REC. DATA A
J4-3
ŗREC. CLOCK A
ŗTRM. CLOCK A
ŗCLEAR TO SEND A
ŗDATA SET READY A
ŗCARRIER DET. A
ŗCIA
J4-1
J4-13
REQ. TO SEND A(105) J4-7
DATA TERM. RDY A (108) J4-14
RECEIVE CLOCK A OUT J4-20
TRANSM. CLOCK A OUT J4-25

SIGNAL	DESTINATION	DESCRIPTION
		The V.24/X.21 selector PAL on this page is controlled by the ₇X.21 SEL. signal. If ₇X.21 SEL. is low signals from the X.21 interface is gated to the 8274 MPSC channel A. If ₇X.21 SEL. is high signals from the V.24/V.28 interface is gated to the 8274 MPSC channel A.
₇R	P12	X.21 Circuit R-Receive.
₇I	P12	X.21 Circuit I- Indication.
₇S	P12	X.21 Circuit S-Signal element timing.
₇CTS A	P10	Clear to Send to 8274 channel A.
₇RXCA LINE	P12	Receive clock A from X.21 or V.24/V.28 interface.
₇TXCA LINE	P12	Transmit clock A from X.21 or V.24/V.28 interface.
RXDA	P10	Received Serial data to 8274 channel A. The positive going edge of ₇RXCA (Receive clock) shifts data from RXDA into the 8274 MPSC channel A.
₇DSR A	P10	Data Set ready channel A to 8255 PPI.
TXDA * RTS A	P12	Transmitted data from the 8274 to the X.21 transmit data driver.
₇X.21 SEL.	P10, P12	X.21 Select signal. This signal originates in the Cable connected to Jack 4. If this cable is a X.21 interface cable this signal will be low. If the cable is a V.24/V.28 cable the signal is high.
₇RXCA	P10	Receive clock to 8274 channel A. Note that this clock originates in a strap which makes it possible to select the receive clock source from either the X.21/V.24 interface or from an on board clock (BAUD CLK Ø).
₇TXCA	P10	Transmit clock to 8274 channel A. Note that this clock originates in a strap which makes it possible to select the transmit clock source from either the X.21/V.24 interface or from an on board clock (BAUD CLK Ø).
₇ON BOARD TXCA	P11	On board clock which can be used as clock source for the 8274 MPSC channel A. This clock is also wired to V.24/V.28 drivers on diagram 11 to be used as transmitter/receiver signal element timing DTE source.
INT 1	P1	8274 MPSC interrupt to 80186 CPU.
CA CB	Jack 4-24 Jack 4-2	X.21 circuit C- control. CA is positive relative to CB when control is on (DTR SYN. A signal logical 1).
TB TA	Jack 4-23 Jack 4-17	X.21 Circuit T-Transmit. TA is negative relative to TB when a logical 1 is transmitted.
CQ7,CQ8,CQ10	P12	Outputs from a 12 bits CMOS ripple counter used to detect the X.21 Clear indication state.
DTR SYN A	P12	Data terminal ready from 8274 channel A synchronized with X.21 interface circuit S. DTR SYN A serves to drive the X.21 circuit C. The X21 counter PAL contains a counter the purpose of which is to detect the X.21 clear indication state. The ₇CLEAR INDICATION signal becomes low after sixteen periods of the S clock supposing that I (Indication) has been off and R (Receive) has been logical "O" in sixteen bit intervals. When the transmission rate becomes lower than 1600 bps (16 bit invervals > 10 mS) the 12 bits CMOS counter takes over the detection of the clear indication state, and the ₇CLEAR INDICATION signal now becomes low whenever I (Indication) has been off and R (Receive) has been logical 0 in 10 mS. The ₇CLEAR INDICATION signal is gated to the ₇CDA output when the X.21 mode of operation is selected (X.21 SEL. = LOW). ₇CDA reflects the state of the V.24/V.28 carrier detect A signal when the V.24/V.28 mode of operation is selected.
₇CDA	P10	Carrier detect A to 8274 channel A. Refer to the description above.

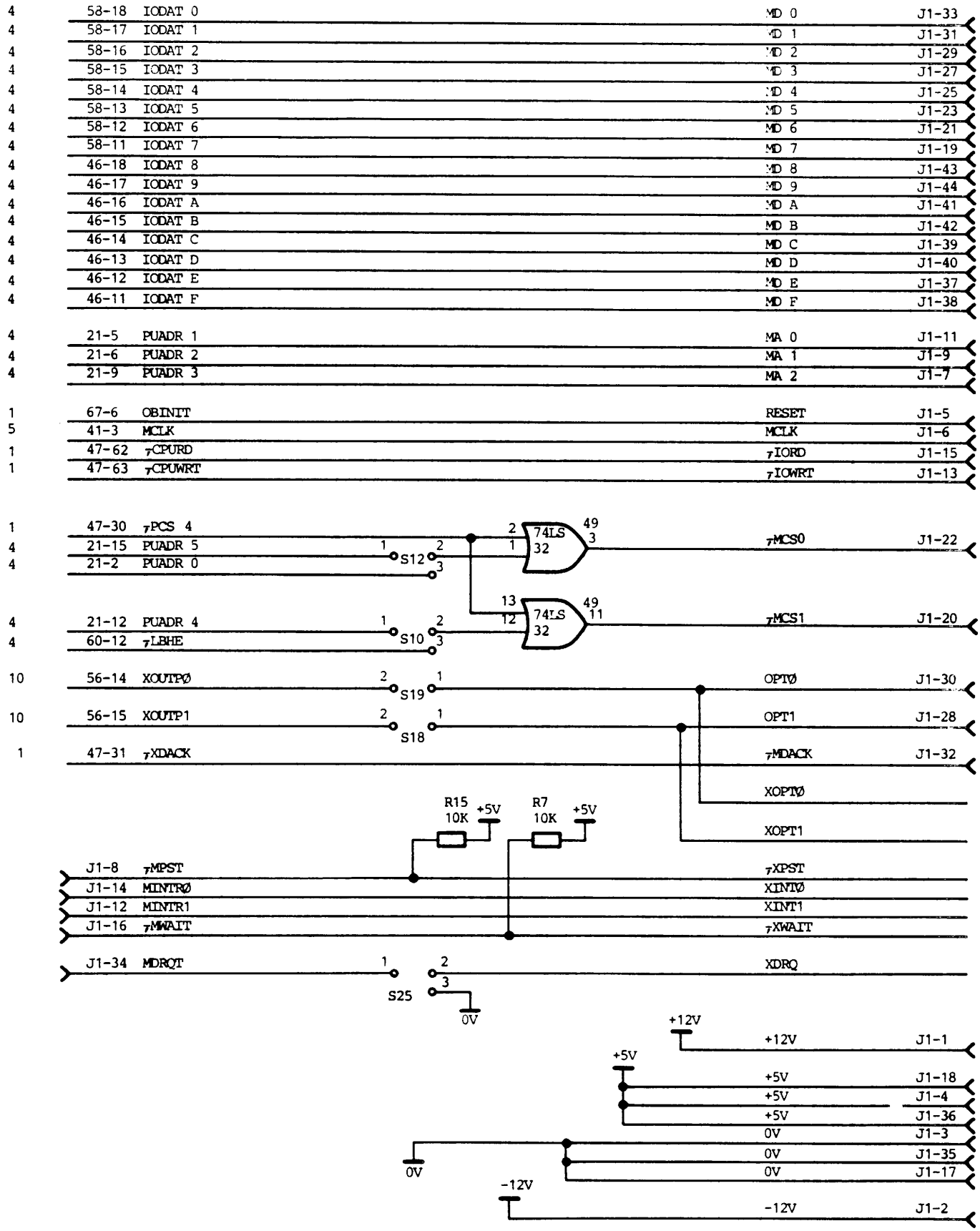

*OPTIONAL
J4-16 RA
J4-12 RB
J4-22 IB
J4-19 IA
J4-6 SB
J4-10 SA
R27
R26
R25
26LS32
87
PAL16L8
66
PAT580
7R
7I
7S
7CTSA
7RXCA LINE
7TXCA LINE
RXDA
7DSRA
TXDA * RTSA
86-13 7CLEAR TO SEND A
76-11 7REC. CLOCK A
76-10 7TRM. CLOCK A
76-12 REC. DATA A
86-12 7DATA SET READY A
64-37 TXDA
64-38 7RTSA
J4-21 7X.21 SEL
1K R16
66-15 7RXCA LINE
66-13 7TXCA LINE
47-22 BAUD CLK Ø
64-28 7INT 1
64-31 7DTRA
87-11 7S
S21
S20
7RXCA
7TXCA
26LS31
57
7ON BOARD TXCA
INT1
CA J4-24
CB J4-2
TB J4-23
TA J4-17
74S74
72
73
74
14
R28 1K
66-14 TXDA * RTSA
LOGIC 1
RA to RB
IA to IB
SA to SB
7R
7I
7S
"0"=POS
"1"
ON=POS.
OFF
ON
OFF
12 BITS RIPPLE COUNTER.
Q1 = LSB. 704 COUNTS 10.2mS
74HTC4040
79
Q1 9
Q2 7
Q3 6
Q4 5
Q5 3
Q6 2
Q7 4
Q8 13
Q9 12
Q10 14
Q11 15
Q12 1
CQ7
CQ8
CQ10
74HTC 4040
8 0V
16 +5V
R40 10K
R12 10K
75-12 68,9 Khz
41-5 7 OBINIT
87-3 7R
87-5 7I
74LS
40
84
PAL16R6
PAT567
(I=OFF) * (R=0) in 16 bit intervals is CLEAR INDICATION
87-11 7S
75-12 68,9 Khz
79-14 CQ 10
79-4 CQ 7
79-13 CQ 8
J4-21 7X.21 SEL
86-11 7CARRIER DET A
7CLEAR INDICATION
7CDA
0V
+5V

SIGNAL	DESTINATION	DESCRIPTION
		The 82501 ESI on this page constitutes the Ethernet Serial Interface. The 82501 ESI integrated circuit is mounted in a 20-pin socket. When the ETC is to be used in connection with the RC micronet, the 82501 must be replaced by the MSI 601 (Micronet Serial Interface) which fits directly into the 20-pin socket.
+12 Volt	Jack -13	+12 Volt to Ethernet or Micronet transceiver.
Ø Volt	Jack -6	+12 Volt return from Ethernet or Micronet transceiver.
Ø Volt	Jack -1,16	Shield for Ethernet or Micronet transceiver cable. The strap makes it possible only to connect the shield in the transceiver end of the cable.
$_7$ CDTE	P13	Collision Detect drives the $_7$CDT input of the 82586 LCC. $_7$CDTE is active low as long as there is activity on the Collision-presence pair. The collision detect output of the 82501 (A-1) versions is a 10 Mhz signal instead of a DC level, which makes it necessary to convert the signal to a DC level using a MMV. Connect strap pin 2 3 for 82501 (A-1) step and connect strap pin 1 2 for Micronet interface and next stepping of the 82501.
$_7$CRS	P2	Carrier Sense output when active low notifies the 82586 that there is activity on the coaxial cable.
RXDE	P2	Receive Data is tied directly to the RXD input of the 82586 controller and sampled by the 82586 at the negative going edge of $_7$RXCE (Receive clock).
$_7$RXCE	P13	Receive Clock output is via buffers connected to the 82586 receive clock input ($_7$RXC).
TRANSMIT + TRANSMIT -	Jack -3 Jack -10	Transmit Pair generates the differential signal for the transmit pair of Ethernet or Micronet transceiver cable.
$_7$TXCE	P2	Transmit Clock. This clock is provided for the 82586 serial transmission. The frequency is 10 Mhz in connection with the Ethernet and 1 Mhz in connection with RC Micronet.
$_7$CDT	P2	Collision Detect. Refer to the description of $_7$CDTE this page.
$_7$RXCED	P2	Buffered Receive Clock.

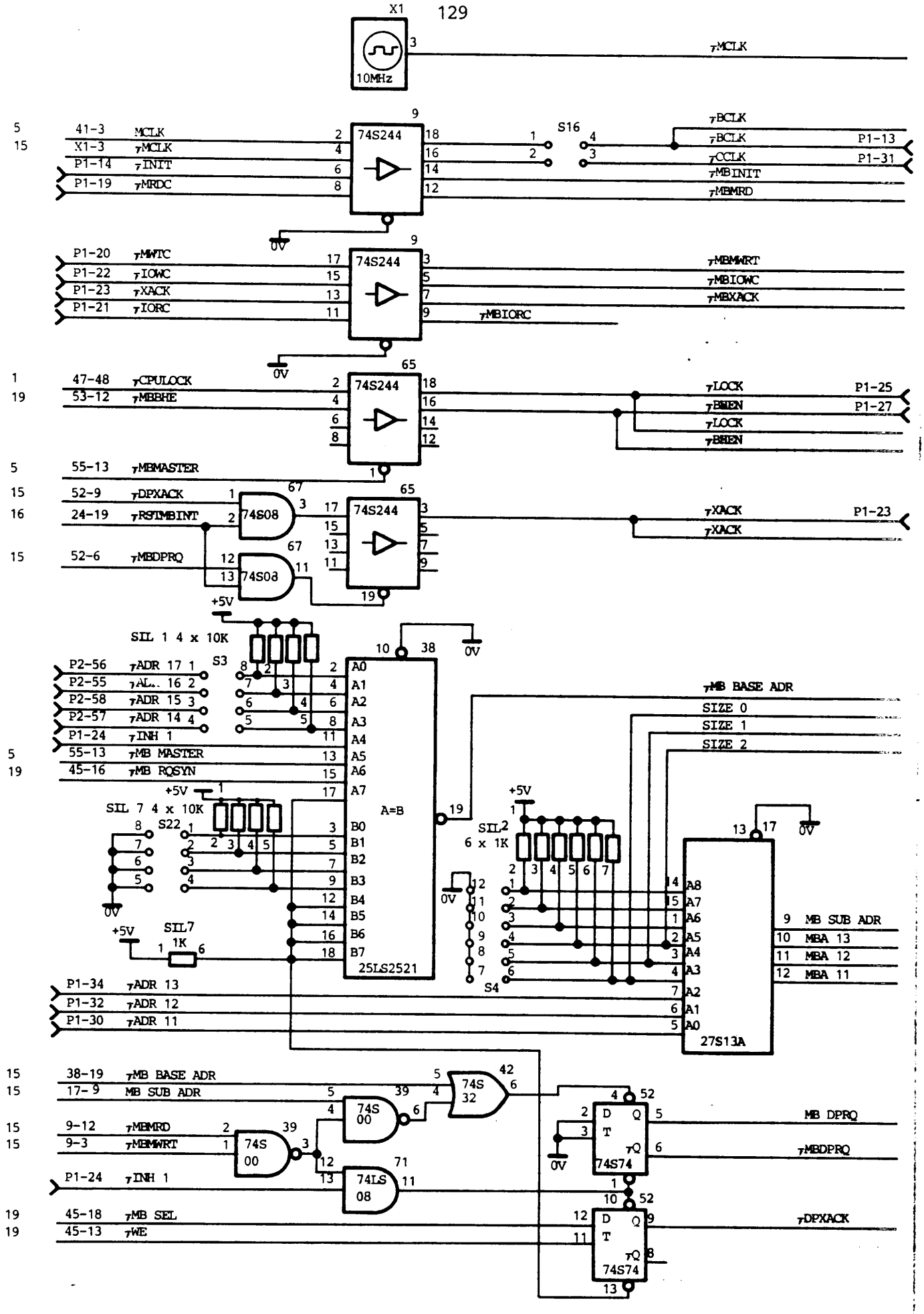


NOTE!
THIS BIPOLAR PROM (256x4) HOLDS ETHERNET ADDRESS.
The contents of the PROM differ from ETC controller to ETC controller.

SIGNAL	DESTINATION	DESCRIPTION
MDØ - MDF	Jack 1	Sixteen bidirectional data lines (active high) to the ISBX Multimodule board. The data lines connect directly to the ETC I/O data bus. MDØ is least significant bit.
MAØ - MA2	Jack 1	Three address lines to the ISBX Multimodule board. The address lines are connected directly to the ETC PUADR 1-3. MAØ is least significant bit.
RESET	Jack 1-5	This line reflects the state of the OBINIT signal. Refer to the description of the OBINIT signal page 1. Reset signal puts the ISBX Multimodule board into a known internal state.
MCLK	Jack 1-6	10 Mhz clock to ISBX Multimodule board.
₇IORD ₇IOWRT	Jack 1-15 Jack 1-13	Read and Write command lines to ISBX Multimodule board. An active low command line conditioned by chip select, indicates to ISBX board that address are valid and the ISBX board should perform the specified operation.
MCSØ MCS 1	Jack 1-22 Jack 1-20	Chip Select lines to ISBX Multimodule board. ₇MCSØ-1 are active low signals which condition the I/O command signals.
OPTØ OPT1 XOPTØ XOPT1	Jack 1-30 Jack 1-28 P10 P10	Option lines to/from the ISBX Multimodule. If the lines are used as input to the ETC, the straps should not be installed.
₇MDACK	Jack 1-32	₇MDACK is an active low input signal to the ISBX Multimodule board from the ETC acknowledging that the requested DMA cycle has been granted.
₇XPST	P10	This signal when active low informs the ETC that an ISBX Multimodule board has been installed.
XINTØ, XINT 1	P9	These active high interrupt lines from the ISBX Multimodule board are used to make interrupt requests to the 80186 CPU on the ETC board. Note that the interrupt lines passes the interrupt strap field on diagram 9.
₇XWAIT	P6	This signal when active low will put the 80186 CPU into a wait state providing additional time for the ISBX Multimodule board to perform the requested operation. Note that some Multimodules does not generate the ₇XWAIT signal. In these cases the 80186 CPU makes use of its internal programmable wait state generator.
XDRQ	P10	XDRQ is an active high output signal from the ISBX Multimodule board to the ETC. The signal is used to request a DMA cycle. Note that the Multimodule board shares 80186 CPU DMA channel Ø with the 8274 MPSC. Refer to the description of the ₇XDMA signal on page 10.
+12 Volt -12 Volt	Jack 1-1 Jack 1-2	±12 Volt to ISBX Multimodule board, The maximum current must not exceed 1 Amps.
+5Volt	Jack 1-18 Jack 1-4 Jack 1-36	+5 Volt to ISBX Multimodule board. The maximum current must not exceed 3 Amps.
Ø Volt	Jack 1-3 Jack 1-17 Jack 1-35	Ø Volt to ISBX Multimodule board. Maximum current is 6 Amps.


4 58-18 IODAT 0
4 58-17 IODAT 1
4 58-16 IODAT 2
4 58-15 IODAT 3
4 58-14 IODAT 4
4 58-13 IODAT 5
4 58-12 IODAT 6
4 58-11 IODAT 7
4 46-18 IODAT 8
4 46-17 IODAT 9
4 46-16 IODAT A
4 46-15 IODAT B
4 46-14 IODAT C
4 46-13 IODAT D
4 46-12 IODAT E
4 46-11 IODAT F
MD 0 J1-33
MD 1 J1-31
MD 2 J1-29
MD 3 J1-27
MD 4 J1-25
MD 5 J1-23
MD 6 J1-21
MD 7 J1-19
MD 8 J1-43
MD 9 J1-44
MD A J1-41
MD B J1-42
MD C J1-39
MD D J1-40
MD E J1-37
MD F J1-38
4 21-5 PUADR 1
4 21-6 PUADR 2
4 21-9 PUADR 3
MA 0 J1-11
MA 1 J1-9
MA 2 J1-7
1 67-6 OBINIT
5 41-3 MCLK
1 47-62 ₇CPURD
1 47-63 ₇CPUWRT
RESET J1-5
MCLK J1-6
₇IORD J1-15
₇IOWRT J1-13
1 47-30 ₇PCS 4
4 21-15 PUADR 5
4 21-2 PUADR 0
S12
74LS 32
₇MCS0 J1-22
4 21-12 PUADR 4
4 60-12 ₇LBHE
S10
74LS 32
₇MCS1 J1-20
10 56-14 XOUTPØ
S19
OPTØ J1-30
10 56-15 XOUTP1
S18
OPT1 J1-28
1 47-31 ₇XDACK
₇MDACK J1-32
XOPTØ
XOPT1
R15 10K +5V
R7 10K +5V
J1-8 ₇MPST
J1-14 MINTRØ
J1-12 MINTR1
J1-16 ₇MWAIT
₇XPST
XINTØ
XINT1
₇XWAIT
J1-34 MDRQT
S25
0V
XDRQ
+12V
+12V J1-1
+5V
+5V J1-18
+5V J1-4
+5V J1-36
0V J1-3
0V J1-35
0V J1-17
0V
-12V
-12V J1-2

SIGNAL	DESTINATION	DESCRIPTION
₇MCLK	P5,P15	10 Mhz clock used to generate ₇BCLK, ₇CCLK to Multibus and MCLK to ISBX Multimodule.
₇BCLK	Plug 1-13, P5	BUS Clock. This clock signal is used to synchronize the Multibus contention logic (8289 arbiter). If there is more than one master on the system, one and only one should be used to generate a master clock. This is made possible by means of a strap.
₇CCLK	Plug 1-31	Constant Clock may be used by bus masters or slaves as a master clock. If there is more than one master on the system, one and only one should be used to generate a master clock. This is made possible by means of a strap.
₇MBINIT	P1, P19	The Multibus initialize signal is generated to reset the entire system to a known internal state.
₇MBMRD ₇MBMWRT ₇MBIOWC	P7,P15,P19 P15,P16,P19 P16	Buffered command lines from the Multibus to the ETC. There are four command lines for memory and I/O reads and writes, however, ₇MBIORC is not used in the ETC.
₇MBXACK	P6	Buffered Transfer acknowledge line from the Multibus to the ETC. This line is the slave's acknowledgment of Master's command.
₇LOCK	Plug 1-25, P19	₇LOCK signal to Multibus allows mutual exclusion to be extended off the bus when ETC is master. Note that the 82586 LCC is unable to generate ₇LOCK signal. If ETC is slave it locks its on board dual port memory to the Multibus when ₇LOCK is active low and ETC is adressed.
₇BHEN	Plug 1-27, P5.	Byte Control line is used to select the upper byte of a 16 bit word.
₇XACK	Plug 1-23	Transfer acknowledge line from ETC to the Multibus.
₇MB BASE ADR	P15	Active low when the ETC dual port memory is accessed from another bus master (ETC is slave). Strap S22 value must be equal to Multibus address lines ADR14-ADR17 value in order to select the ETC.
SIZE 0 -SIZE 2	P10	Strap S4 size value determines the amount of ETC dual port RAM available to the multibus master.
MB SUB ADR	P15	Active high when the ETC dual port memory is accessed from another bus master. Strap S4 selects from 1-8 128K byte segments out of the one megabyte system memory selected by strap S22.
MBA 11 MBA 12 MBA 13	P16, P19, P21 P16, P21 P16, P19	The ROA917 converts Multibus address lines ADR 11-13 into MBA 11-13 in order to place the Multibus accessable portion of ETC dual port RAM from address Ø and on.
MBDPRQ ₇MBDPRQ	P7 P15, P19	These signals becomes active when the ETC dual port memory is accessed by another bus master.
₇DPXACK	P15	Cycle acknowledge signal from ETC dual port RAM when accessed by another bus master.


X1
10MHz
~MCLK
74S244
74S08
74LS 08
74S 00
74S 32
74S74
25LS2521
27S13A
S16
S3
S4
S22
SIL 1 4 x 10K
SIL 7 4 x 10K
SIL7 1K
SIL2 6 x 1K
A=B
~MB BASE ADR
SIZE 0
SIZE 1
SIZE 2
MB SUB ADR
MB DPRQ
~MBDPRQ
~DPXACK
~MCLK
~BCLK
~CCLK
~MBINIT
~MBMRD
~MBMWRT
~MBIOWC
~MBXACK
~MBIORC
~LOCK
~BHEN
~XACK
P1-13
P1-31
P1-25
P1-27
P1-23
P1-34 ~ADR 13
P1-32 ~ADR 12
P1-30 ~ADR 11
P2-56 ~ADR 17 1
P2-55 ~AL.. 16 2
P2-58 ~ADR 15 3
P2-57 ~ADR 14 4
P1-24 ~INH 1
55-13 ~MB MASTER
45-16 ~MB RQSYN
38-19 ~MB BASE ADR
17- 9 MB SUB ADR
9-12 ~MBMRD
9-3 ~MBMWRT
45-18 ~MB SEL
45-13 ~WE
41-3 MCLK
X1-3 ~MCLK
P1-14 ~INIT
P1-19 ~MRDC
P1-20 ~MWTC
P1-22 ~IOWC
P1-23 ~XACK
P1-21 ~IORC
47-48 ~CPULOCK
53-12 ~MBBHE
55-13 ~MBMASTER
52-9 ~DPXACK
24-19 ~RSTMBINT
52-6 ~MBDPRQ

SIGNAL	DESTINATION	DESCRIPTION
₇(ADR F:9 = 2 * WE)	P16	This signal is used to generate the ETC Reset Address and the ETC Interrupt Address. The signal is active low during Multibus write access to dual port RAM if Multibus address lines ADR 9 - ADRF = 2.
A,B < > 1,0 A,B < > 0,1	P16 P16	These signals are used to generate the Reset Multibus interrupt signal. When both of the signals are true it indicates that strap S14 value is equal to Multibus address lines ₇ADR 9 - ₇ADR F.
₇RSTMBINT	P15, P16	Reset Multibus Interrupt. Generated by a multibus master during an I/O write operation to reset the ETC Multibus Interrupt out latch adressed by Multibus data lines Ø,1.
MBINTOUT Ø - MBINTOUT 3	P9	Multibus Interrupt Request lines serves to interrupt the multibus master when ETC is slave.
₇CLEAR P. ERROR	P20	This signal serves to clear the parity error flip-flop after a parity error has been detected in ETC dual port RAM.
₇FLAGBYTE	P20	Active low during a Multibus memory write operation if the Multibus master accesses the ETC flagbyte interrupt address.
₇MBRES	P1	Active low during a Multibus memory write operation if the Multibus master accesses the ETC reset address. If strap S9 on diagram 1 is installed the function of the ₇MBRES signal is equivalent to the function of ₇MBINIT i.e. the ETC is reset to a known internal state.

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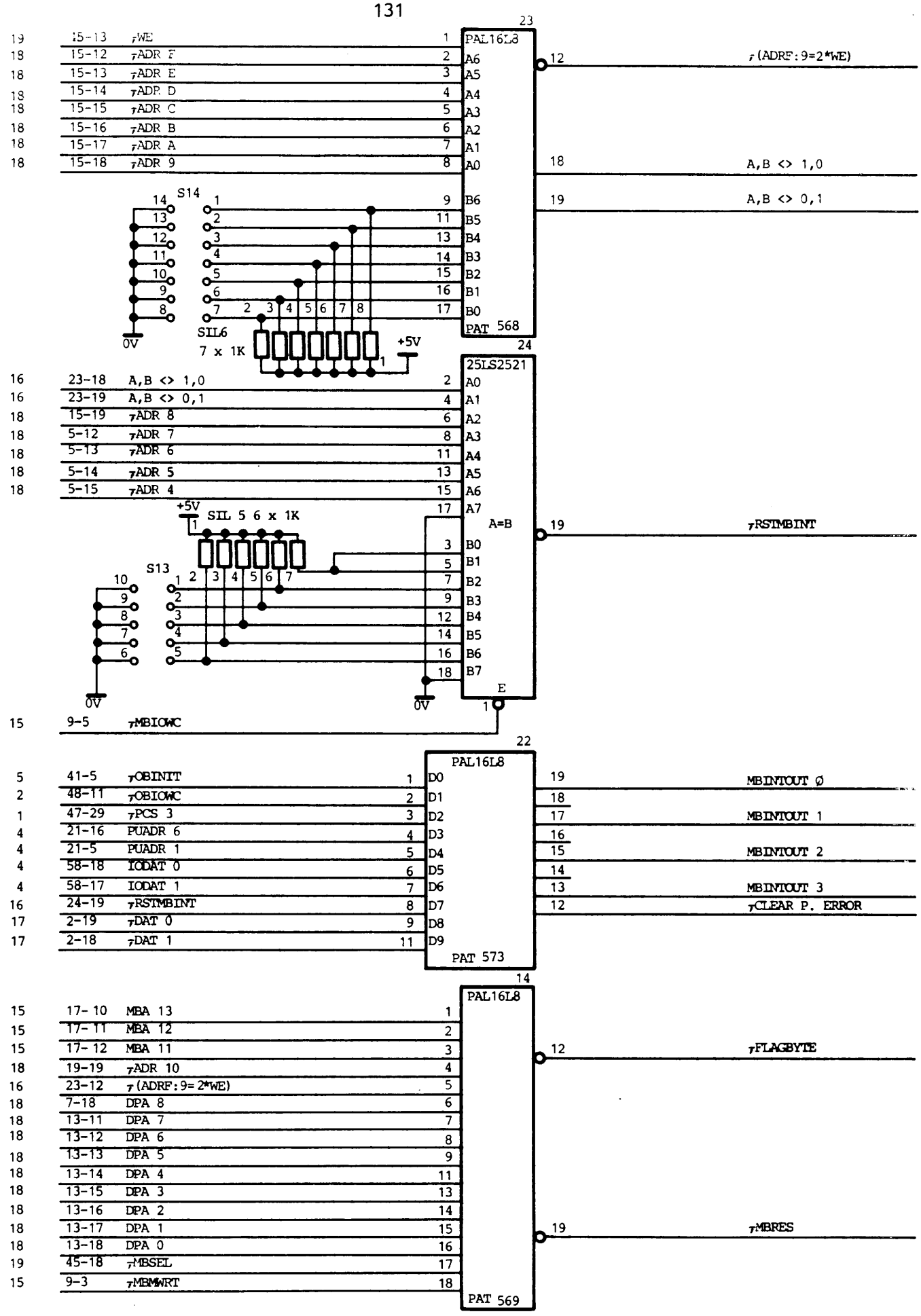
Unit		
ETC601/611	CPU TO MULTIBUS INTERRUPT CONTROL LOGIC	PAGE 16
Dwg. No.	AND	
A26361	MULTIBUS TO CPU MEM WRITE INTERRUPT	


23
PAL16L8
19 15-13 ₇WE 1
18 15-12 ₇ADR F 2
18 15-13 ₇ADR E 3
18 15-14 ₇ADR D 4
18 15-15 ₇ADR C 5
18 15-16 ₇ADR B 6
18 15-17 ₇ADR A 7
18 15-18 ₇ADR 9 8
A6
A5
A4
A3
A2
A1
A0
12 ₇(ADRF:9=2*WE)
18 A,B <> 1,0
19 A,B <> 0,1
S14
14 13 12 11 10 9 8
1 2 3 4 5 6 7 8
9 B6
11 B5
13 B4
14 B3
15 B2
16 B1
17 B0
PAT 568
0V
SIL6
7 x 1K
+5V
24
25LS2521
16 23-18 A,B <> 1,0 2 A0
16 23-19 A,B <> 0,1 4 A1
18 15-19 ₇ADR 8 6 A2
18 5-12 ₇ADR 7 8 A3
18 5-13 ₇ADR 6 11 A4
18 5-14 ₇ADR 5 13 A5
18 5-15 ₇ADR 4 15 A6
17 A7
+5V
SIL 5 6 x 1K
A=B
19 ₇RSTMBINT
S13
10 9 8 7 7 6
1 2 3 4 5 6 7
3 B0
5 B1
7 B2
9 B3
12 B4
14 B5
16 B6
18 B7
0V
0V
E
15 9-5 ₇MBIOWC
22
PAL16L8
5 41-5 ₇OBINIT 1 D0
2 48-11 ₇OBIOWC 2 D1
1 47-29 ₇PCS 3 3 D2
4 21-16 PUADR 6 4 D3
4 21-5 PUADR 1 5 D4
4 58-18 IODAT 0 6 D5
4 58-17 IODAT 1 7 D6
16 24-19 ₇RSTMBINT 8 D7
17 2-19 ₇DAT 0 9 D8
17 2-18 ₇DAT 1 11 D9
PAT 573
19 MBINTOUT Ø
18
17 MBINTOUT 1
16
15 MBINTOUT 2
14
13 MBINTOUT 3
12 ₇CLEAR P. ERROR
14
PAL16L8
15 17-10 MBA 13 1
15 17-11 MBA 12 2
15 17-12 MBA 11 3
18 19-19 ₇ADR 10 4
16 23-12 ₇(ADRF:9=2*WE) 5
18 7-18 DPA 8 6
18 13-11 DPA 7 7
18 13-12 DPA 6 8
18 13-13 DPA 5 9
18 13-14 DPA 4 11
18 13-15 DPA 3 13
18 13-16 DPA 2 14
18 13-17 DPA 1 15
18 13-18 DPA 0 16
19 45-18 ₇MBSEL 17
15 9-3 ₇MBMWRT 18
PAT 569
12 ₇FLAGBYTE
19 ₇MBRES

SIGNAL	DESTINATION	DESCRIPTION
DPD Ø - DPD F	P20,P22	On Board dual port RAM data bus.
$\overline{7}$DAT Ø, $\overline{7}$DAT 1	Plug1-73,74 P16.	Sixteen bidirectional lines are used to transfer information between ETC dual port RAM and the Multibus master. $\overline{7}$DAT Ø is least significant bit.
$\overline{7}$DAT 2 - $\overline{7}$DAT F	Plug 1	

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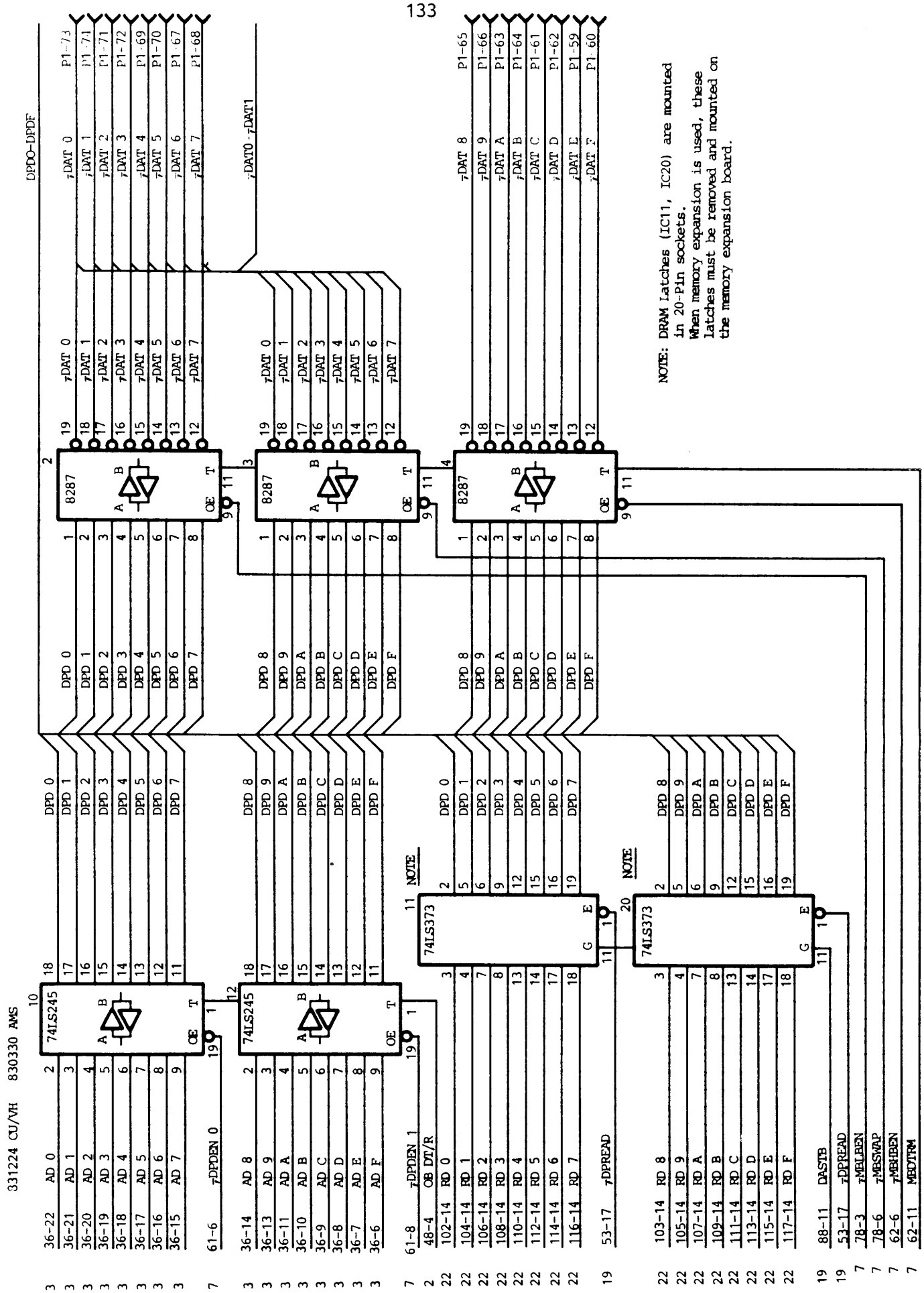
Unit		
ETC601/611	DUAL PORT RAM DATA BUS (ON BOARD DATA BUS),	PAGE 17
Dwg. No. A26362	MULTIBUS DATA TRANSCEIVERS	


NOTE: DRAM Latches (IC11, IC20) are mounted in 20-Pin sockets. When memory expansion is used, these latches must be removed and mounted on the memory expansion board.
NOTE
NOTE
74LS245
74LS373
8287
DPD0-DPDF
7DAT0-7DAT1
331224 CU/VH 830330 AMS

SIGNAL	DESTINATION	DESCRIPTION
DPA Ø	P5,P7,P16, P19	On Board dual port RAM address bus.
DPA 1 - DPA 8	P16,P21	
DPA 9 - DPA 1Ø	P21	
DPA 11	P19,P21	
DPA 12	P21	
DPA 13	P19	
$\overline{7}$ADR 0-3	Plug 1	Multibus Address lines. $\overline{7}$ADR Ø - $\overline{7}$ADR F, $\overline{7}$ADR 10 - $\overline{7}$ADR 13 and $\overline{7}$ADR 14 - $\overline{7}$ADR 17 are 24 address lines that carry the address of the memory or I/O device that is being referenced. Twenty four address lines allow a maximum of sixteen mega bytes of memory to be accessed.
$\overline{7}$ADR 4-10	Plug 1, P16	
$\overline{7}$ADR 11-13	Plug 1, P15	
$\overline{7}$ADR 14-17	Plug 2, P15	

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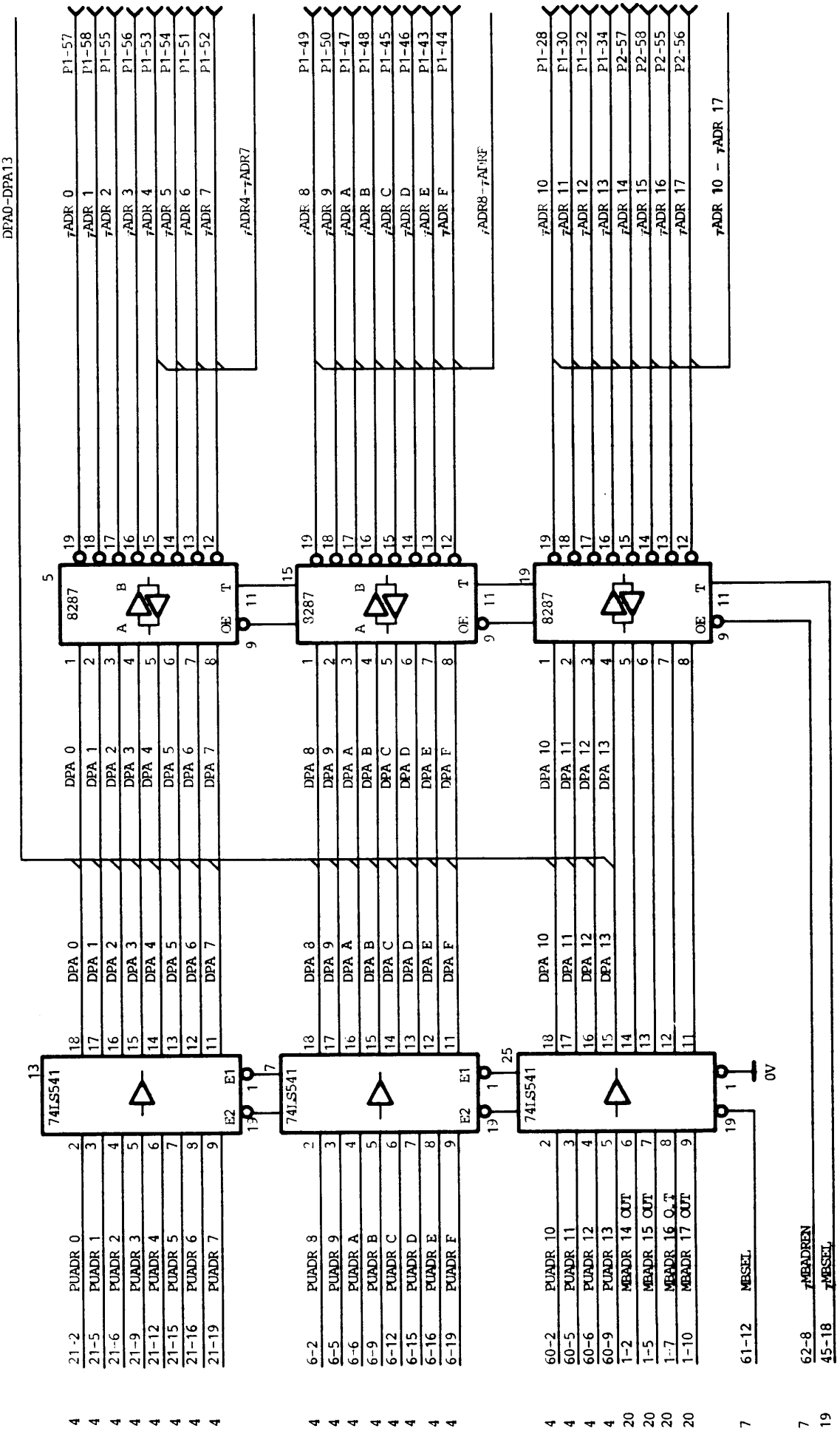
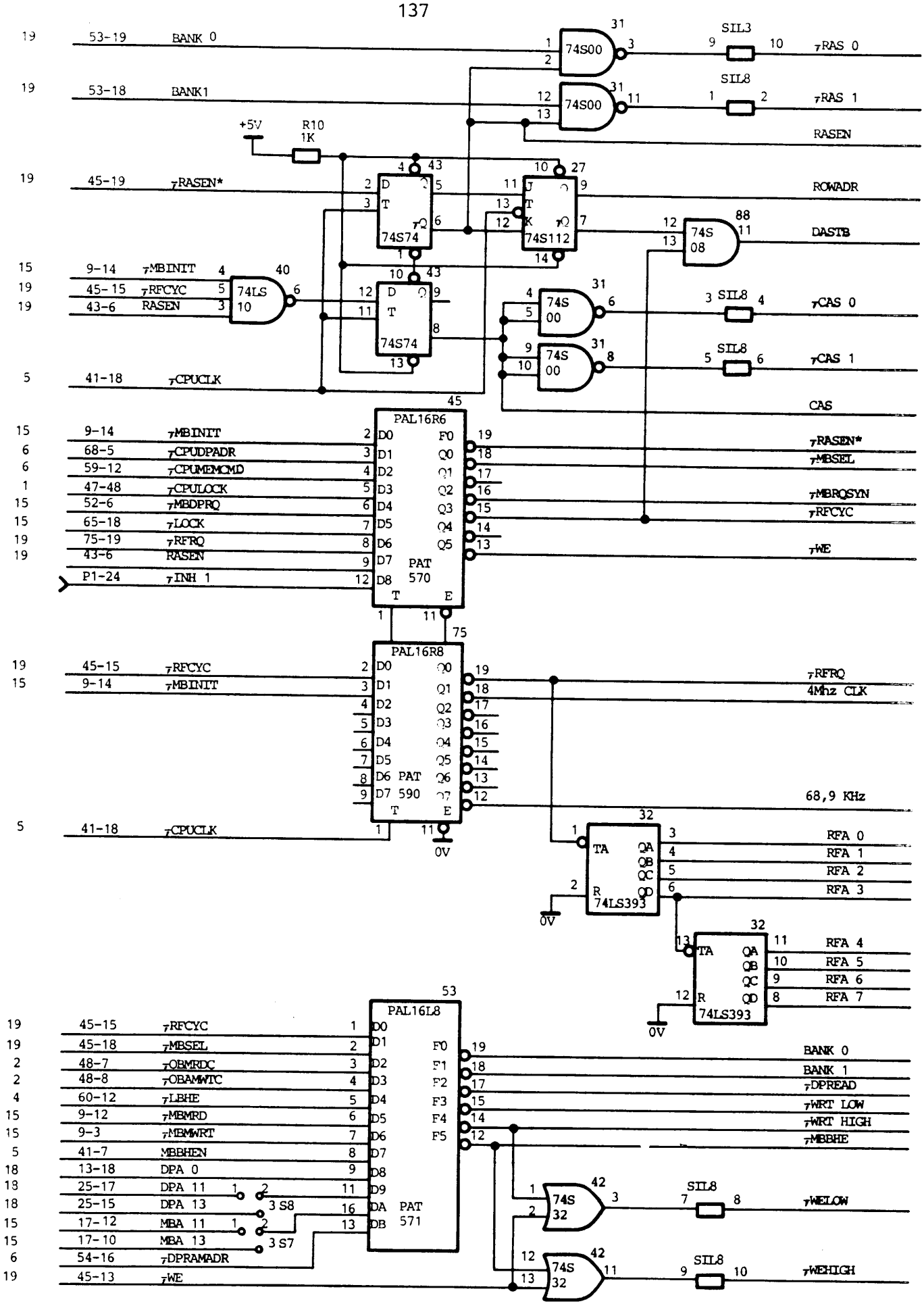
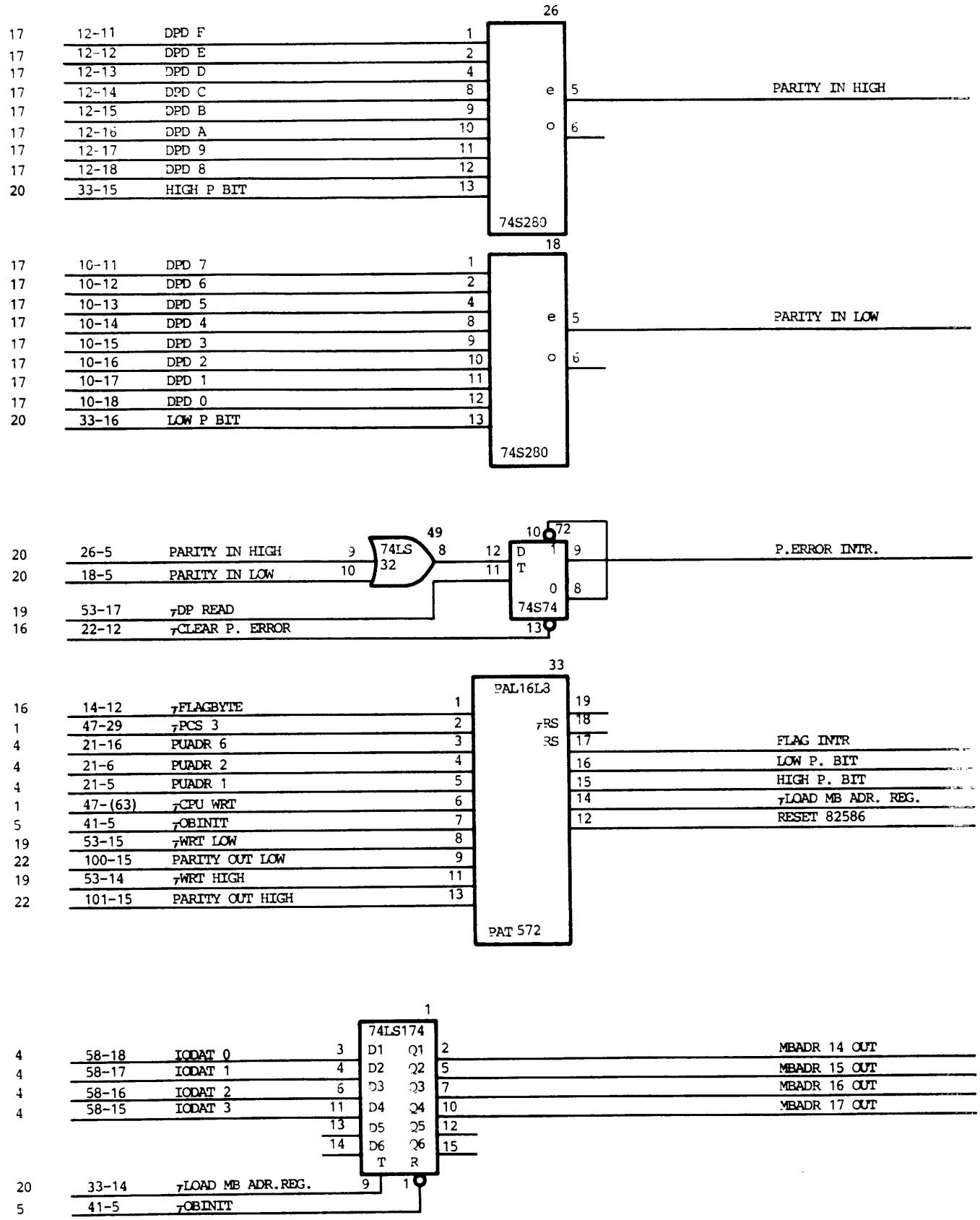
Unit		
ETC601/611	DUAL PORT RAM ADDRESS BUS (ON BOARD ADDRESS BUS), MULTIBUS ADDRESS TRANSCEIVERS.	PAGE 18
Dwg. No. A26363		


DPA0-DPA13
8287
3287
74LS541
DPA 0
DPA 1
DPA 2
DPA 3
DPA 4
DPA 5
DPA 6
DPA 7
DPA 8
DPA 9
DPA A
DPA B
DPA C
DPA D
DPA E
DPA F
DPA 10
DPA 11
DPA 12
DPA 13
PUADR 0
PUADR 1
PUADR 2
PUADR 3
PUADR 4
PUADR 5
PUADR 6
PUADR 7
PUADR 8
PUADR 9
PUADR A
PUADR B
PUADR C
PUADR D
PUADR E
PUADR F
PUADR 10
PUADR 11
PUADR 12
PUADR 13
MBADR 14 OUT
MBADR 15 OUT
MBADR 16 OUT
MBADR 17 OUT
MBSEL
MBADREN
0V
P1-57
P1-58
P1-55
P1-56
P1-53
P1-54
P1-51
P1-52
P1-49
P1-50
P1-47
P1-48
P1-45
P1-46
P1-43
P1-44
P1-28
P1-30
P1-32
P1-34
P2-57
P2-58
P2-55
P2-56
ADR 0
ADR 1
ADR 2
ADR 3
ADR 4
ADR 5
ADR 6
ADR 7
ADR 8
ADR 9
ADR A
ADR B
ADR C
ADR D
ADR E
ADR F
ADR 10
ADR 11
ADR 12
ADR 13
ADR 14
ADR 15
ADR 16
ADR 17
ADR4-ADR7
ADR8-ADRF
ADR 10 - ADR 17

SIGNAL	DESTINATION	DESCRIPTION
		This diagram shows control logic for the dual ported dynamic RAM. PAT570 controls access to the DRAM from two request sources CPUDPADR * CPUMEMCMD (80186/82586 request) and MBDPRQ (Multibus request). ₇MBSEL active low indicates that a Multibus request is being serviced. ₇MSEL cannot be generated when ₇INH is active low. A refresh cycle is generated when ₇RFRQ is active low. PAT570 does also control the timing of RAS, CAS,WE and the address multiplexing. PAT007/590 are refresh timing generators for 6/8 Mhz CPU's. A refresh request (₇RFRQ active low) is generated every 14.5 microsec. PAT571 generates BANKØ and BANK1 select signals for the two DRAM banks. ₇DPREAD is output enable signal for the DRAM latches. ₇WRT LOW and ₇WRT HIGH are byte write control signals for the DRAM. MBBHE is a byte control signal for the Multibus.
₇RAS Ø, ₇RAS.1	P22	Row Address Strobe Ø and 1.
RASEN	P19	Row Address Strobe Enable FF.
ROWADR	P21	Row Address. This signal when active high serves to gate row address bits to DRAM.
DASTB	P17	Data strobe serves to load read data from DRAM into DRAM latches.
₇CASØ, ₇CAS1	P22	Column Address Strobe Ø and 1.
CAS	P6	Column Address Strobe to ready circuits.
₇RASEN*	P19	This signal serves to enable the Row Address Strobe Enable FF.
₇MBSEL	P6, P7, P15, P16, P18, P19	This signal when active low indicates that a multibus request is being serviced.
₇MBRQSYN	P15	Synchronized Multibus request. ₇MBRQSYN is active low when another multibus master requests access to the dual-port DRAM via the Multibus.
₇RFCYC	P19, P21	Refresh Cycle. ₇RFCYC indicates that a refresh cycle is being serviced.
₇WE	P15,P16,P19	Write Enable DRAM timing.
₇RFRQ	P19	Refresh Request. ₇RFRQ is active low when a refresh cycle is needed.
4 Mhz	P10	4 Mhz clock to the 8274 MPSC.
68.9 Khz	P12	68.9 Khz clock to X.21 interface.
RFA Ø - RFA 7	P21	Refresh Address bits Ø-7.
BANK 0 - BANK 1	P19	Bank select signals to memory banks. Bank Ø is located on the ETC printed circuit board, while MEX (Memory expansion) printed circuit board constitutes Bank 1. The straps shown controls the size of the banks. When strap pin 1 is connected to 2 the banks are 128 Kbyte each (64K x 1 chips). When strap pin 3 is connected to 2 the banks are 512 kbyte each (256K x 1 cpips).
₇DPREAD	P17, P20	Dual-port read. ₇DPREAD enables the contents of DRAM latches onto the on board dual port data bus, and triggers the Parity Error FF if a parity error is detected.
₇WRT LOW - ₇WRT HIGH	P20	Byte Write control signals for DRAM. ₇WRT LOW Serves to enable write pulse to DRAM bits 0-7. ₇WRT HIGH serves to enable write pulse to DRAM bits 8-15.
₇MBBHE	P15	Multibus Byte High Enable.
₇WELOW, ₇WEHIGH	P22	Write Enable signals to DRAM chips.


19 53-19 BANK 0
19 53-18 BANK1
+5V R10 1K
19 45-19 ₇RASEN*
15 9-14 ₇MBINIT
19 45-15 ₇RFCYC
19 43-6 RASEN
5 41-18 ₇CPUCLK
74S00
74S74
74S112
74LS 10
74S 08
74S 00
SIL3
SIL8
₇RAS 0
₇RAS 1
RASEN
ROWADR
DASTB
₇CAS 0
₇CAS 1
CAS
PAL16R6
15 9-14 ₇MBINIT
6 68-5 ₇CPUDPADR
6 59-12 ₇CPUMEMCMD
1 47-48 ₇CPULOCK
15 52-6 ₇MBDPRQ
15 65-18 ₇LOCK
19 75-19 ₇RFRQ
19 43-6 RASEN
P1-24 ₇INH 1
₇RASEN*
₇MBSEL
₇MBRQSYN
₇RFCYC
₇WE
PAL16R8
19 45-15 ₇RFCYC
15 9-14 ₇MBINIT
5 41-18 ₇CPUCLK
0V
₇RFRQ
4Mhz CLK
68,9 KHz
74LS393
RFA 0
RFA 1
RFA 2
RFA 3
RFA 4
RFA 5
RFA 6
RFA 7
PAL16L8
19 45-15 ₇RFCYC
19 45-18 ₇MBSEL
2 48-7 ₇OBMRDC
2 48-8 ₇OBAMWTC
4 60-12 ₇LBHE
15 9-12 ₇MBMRD
15 9-3 ₇MBMWRT
5 41-7 MBBHEN
18 13-18 DPA 0
18 25-17 DPA 11
18 25-15 DPA 13
15 17-12 MBA 11
15 17-10 MBA 13
6 54-16 ₇DPRAMADR
19 45-13 ₇WE
3 S8
3 S7
BANK 0
BANK 1
₇DPREAD
₇WRT LOW
₇WRT HIGH
₇MBBHE
₇WELOW
₇WEHIGH

SIGNAL	DESTINATION	DESCRIPTION
PARITY IN HIGH	P20,P22	High byte parity bit to DRAM. The high byte parity bit makes the parity of high byte (bits 8-15 and P bit) odd during dual-port memory write operations. During dual-port memory read operation this signal becomes logical 1 when a parity error is detected in high byte.
PARITY IN LOW	P20, P22	Low byte parity bit to DRAM. The low byte parity bit makes the parity of low byte (bits 0-7 and P bit) odd during dual-port memory write operations. During dual-port memory read operations this signal becomes logical 1 when a parity error is detected in low byte.
P.ERROR INTR.	P9	The parity error FF is set to logical one on the rising edge of the ₇DPREAD signal whenever a parity error in high or low byte is detected. The P.ERROR INTR signal can be strapped to any interrupt input of the 8259 PIC.
FLAG INTR	P9	FLAG INTERRUPT is an output from a R/S FF, which is set to logical 1 when a Multibus Master writes into the interrupt address of the ETC dual-port DRAM. FLAG INTR. signal can be strapped to any interrupt input of the 8259 PIC.
LOW P. BIT	P20	LOW P.BIT is logical 0 (low) during dual-port memory write operations. During dual-port memory read operations this bit is equal to the low byte parity bit from the DRAM (PARITY OUT LOW).
HIGH P. BIT	P20	HIGH P. BIT is logical 0 (low) during dual-port memory write operations. During dual-port memory read operations this bit is equal to the high byte parity bit from DRAM (PARITY OUT HIGH).
₇LOAD MB ADR. REG	P20	This signal serves to load the Multibus Mega-byte Address Register.
RESET 82586	P2	Active high reset pulse to the 82586 LCC.
MBADR 14 OUT MBADR 15 OUT MBADR 16 OUT MBADR 17 OUT	P18 P18 P18 P18	The multibus mega byte address register allows access to 16 megabytes of multibus address space. The register can be loaded with the contents of the I/O data bus lines 3:0 during an I/O write command. The register is reset to zero upon power-on.


26
17 12-11 DPD F 1
17 12-12 DPD E 2
17 12-13 DPD D 4
17 12-14 DPD C 8
17 12-15 DPD B 9
17 12-16 DPD A 10
17 12-17 DPD 9 11
17 12-18 DPD 8 12
20 33-15 HIGH P BIT 13
e 5 PARITY IN HIGH
o 6
74S280
18
17 10-11 DPD 7 1
17 10-12 DPD 6 2
17 10-13 DPD 5 4
17 10-14 DPD 4 8
17 10-15 DPD 3 9
17 10-16 DPD 2 10
17 10-17 DPD 1 11
17 10-18 DPD 0 12
20 33-16 LOW P BIT 13
e 5 PARITY IN LOW
o 6
74S280
49
20 26-5 PARITY IN HIGH 9
20 18-5 PARITY IN LOW 10
74LS 32
8 12
10 72
D 1 9
T
0 8
74S74
11 13
19 53-17 ₇DP READ
16 22-12 ₇CLEAR P. ERROR
P.ERROR INTR.
33
PAL16L8
16 14-12 ₇FLAGBYTE 1
1 47-29 ₇PCS 3 2
4 21-16 PUADR 6 3
4 21-6 PUADR 2 4
4 21-5 PUADR 1 5
1 47-(63) ₇CPU WRT 6
5 41-5 ₇OBINIT 7
19 53-15 ₇WRT LOW 8
22 100-15 PARITY OUT LOW 9
19 53-14 ₇WRT HIGH 11
22 101-15 PARITY OUT HIGH 13
₇RS 19
RS 18
17 FLAG INTR
16 LOW P. BIT
15 HIGH P. BIT
14 ₇LOAD MB ADR. REG.
12 RESET 82586
PAT 572
1
74LS174
4 58-18 IODAT 0 3
4 58-17 IODAT 1 4
4 58-16 IODAT 2 6
4 58-15 IODAT 3 11
13
14
D1 Q1 2
D2 Q2 5
D3 Q3 7
D4 Q4 10
D5 Q5 12
D6 Q6 15
T R
MBADR 14 OUT
MBADR 15 OUT
MBADR 16 OUT
MBADR 17 OUT
20 33-14 ₇LOAD MB ADR.REG. 9
5 41-5 ₇OBINIT 1

SIGNAL	DESTINATION	DESCRIPTION
R/C Ø - R/C 8	P22	ROW/ Column address to dynamic ram.

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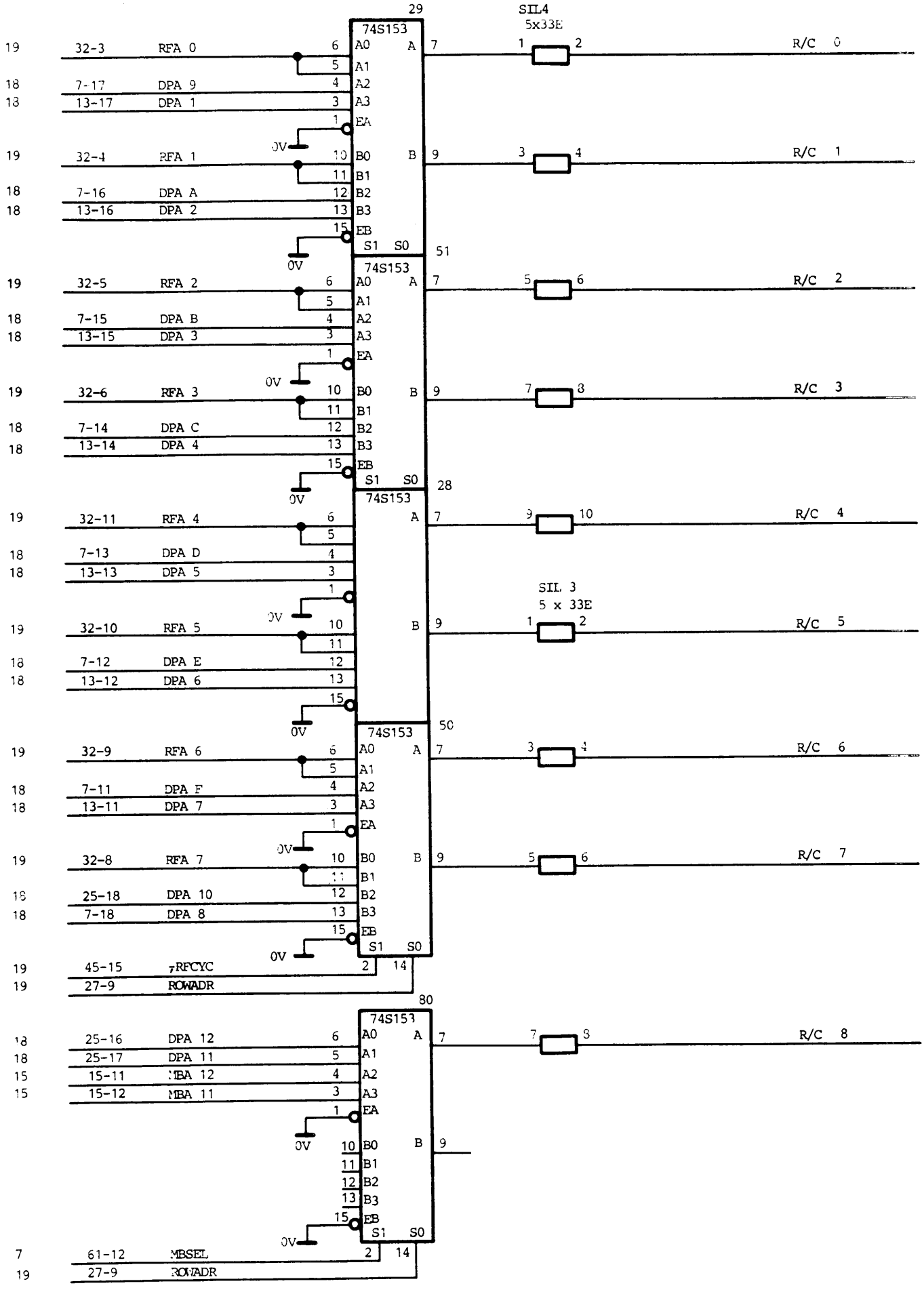
29
74S153
SIL4
5x33E
19 32-3 RFA 0
18 7-17 DPA 9
18 13-17 DPA 1
19 32-4 RFA 1
18 7-16 DPA A
18 13-16 DPA 2
0V
A0
A1
A2
A3
EA
B0
B1
B2
B3
EB
S1 S0
A
B
R/C 0
R/C 1
51
74S153
19 32-5 RFA 2
18 7-15 DPA B
18 13-15 DPA 3
19 32-6 RFA 3
18 7-14 DPA C
18 13-14 DPA 4
R/C 2
R/C 3
28
74S153
19 32-11 RFA 4
18 7-13 DPA D
18 13-13 DPA 5
19 32-10 RFA 5
18 7-12 DPA E
18 13-12 DPA 6
SIL 3
5 x 33E
R/C 4
R/C 5
50
74S153
19 32-9 RFA 6
18 7-11 DPA F
18 13-11 DPA 7
19 32-8 RFA 7
18 25-18 DPA 10
18 7-18 DPA 8
19 45-15 RFCYC
19 27-9 ROWADR
R/C 6
R/C 7
80
74S153
18 25-16 DPA 12
18 25-17 DPA 11
15 15-11 MBA 12
15 15-12 MBA 11
7 61-12 MBSEL
19 27-9 ROWADR
R/C 8

SIGNAL	DESTINATION	DESCRIPTION
PARITY OUT HIGH	P20	High byte parity bit.
RDF - RD 8	P17	Read Data F-8 from DRAM.
PARITY OUT LOW	P20	LOW byte parity bit.
RD 7 - RD 0	P17	Read Data 7-0 from DRAM.

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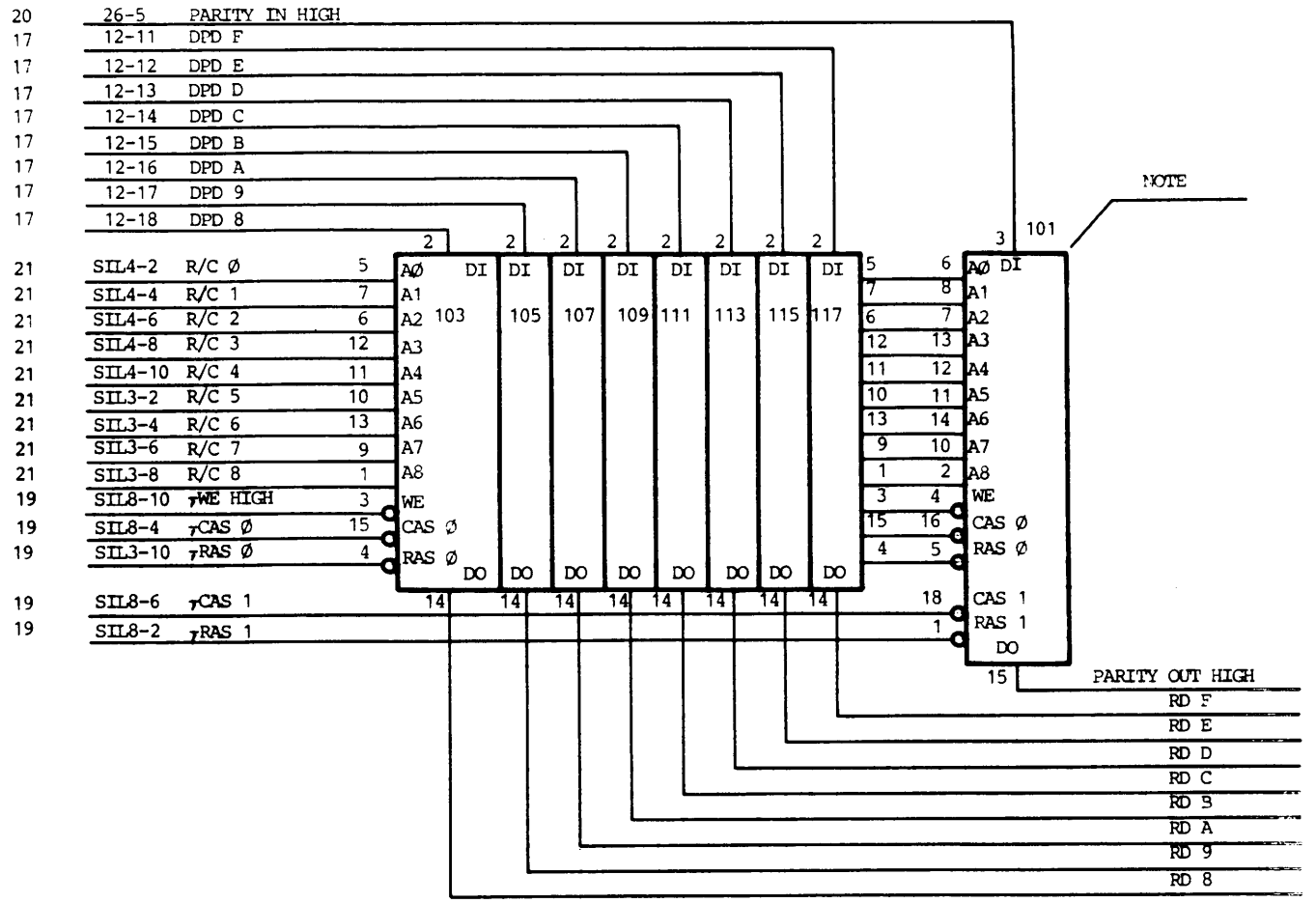
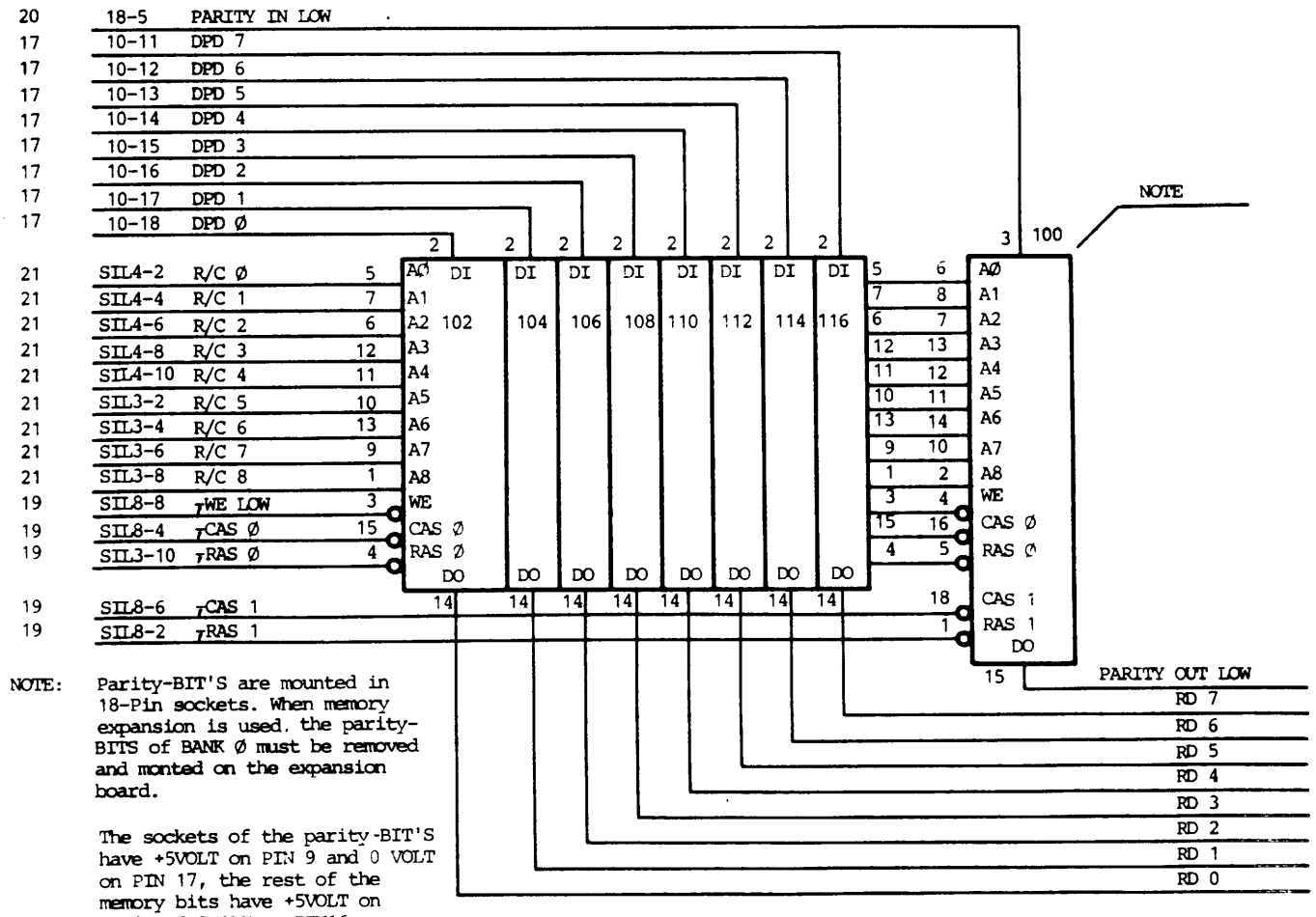
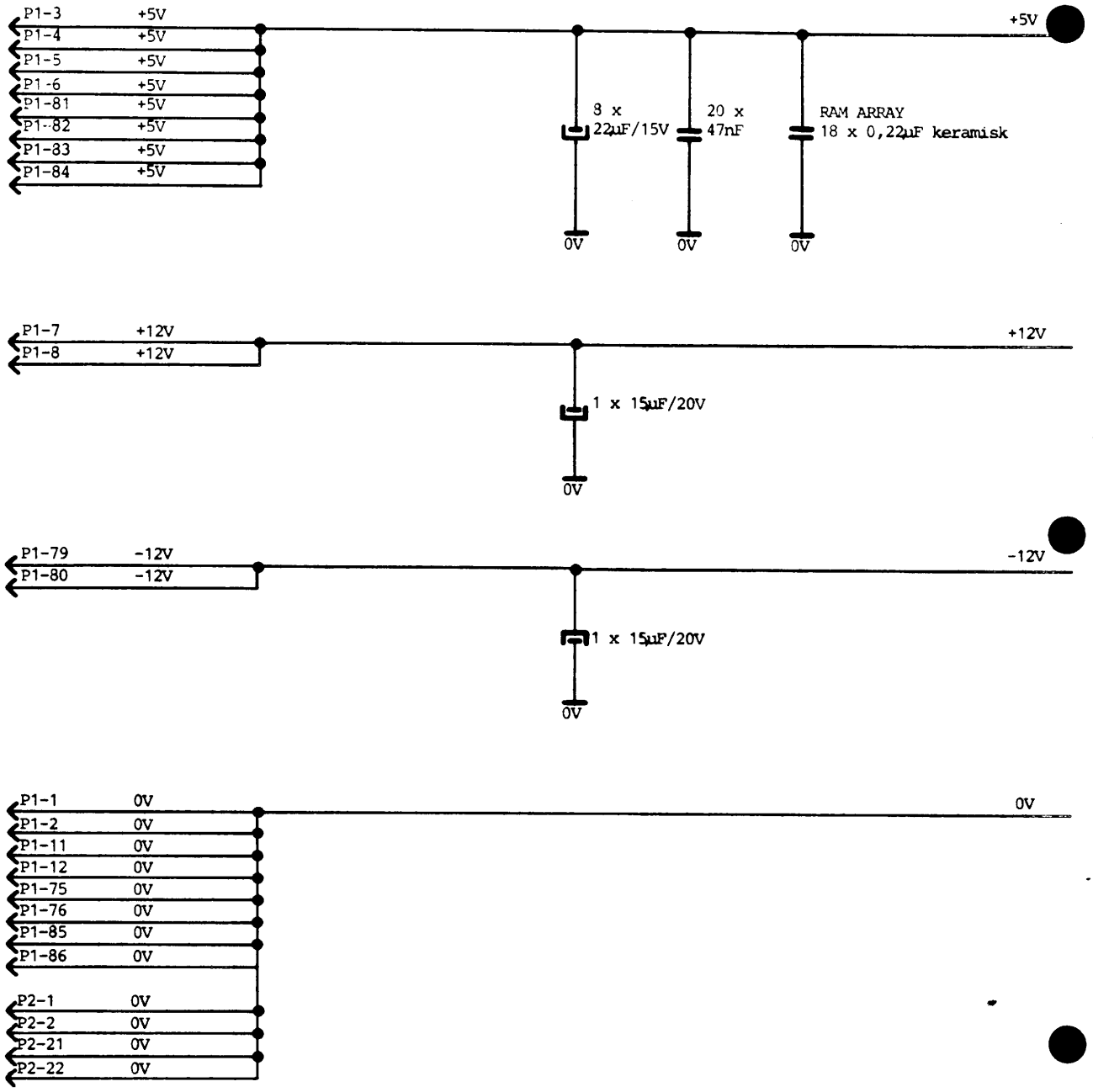
Dwg. Office Check



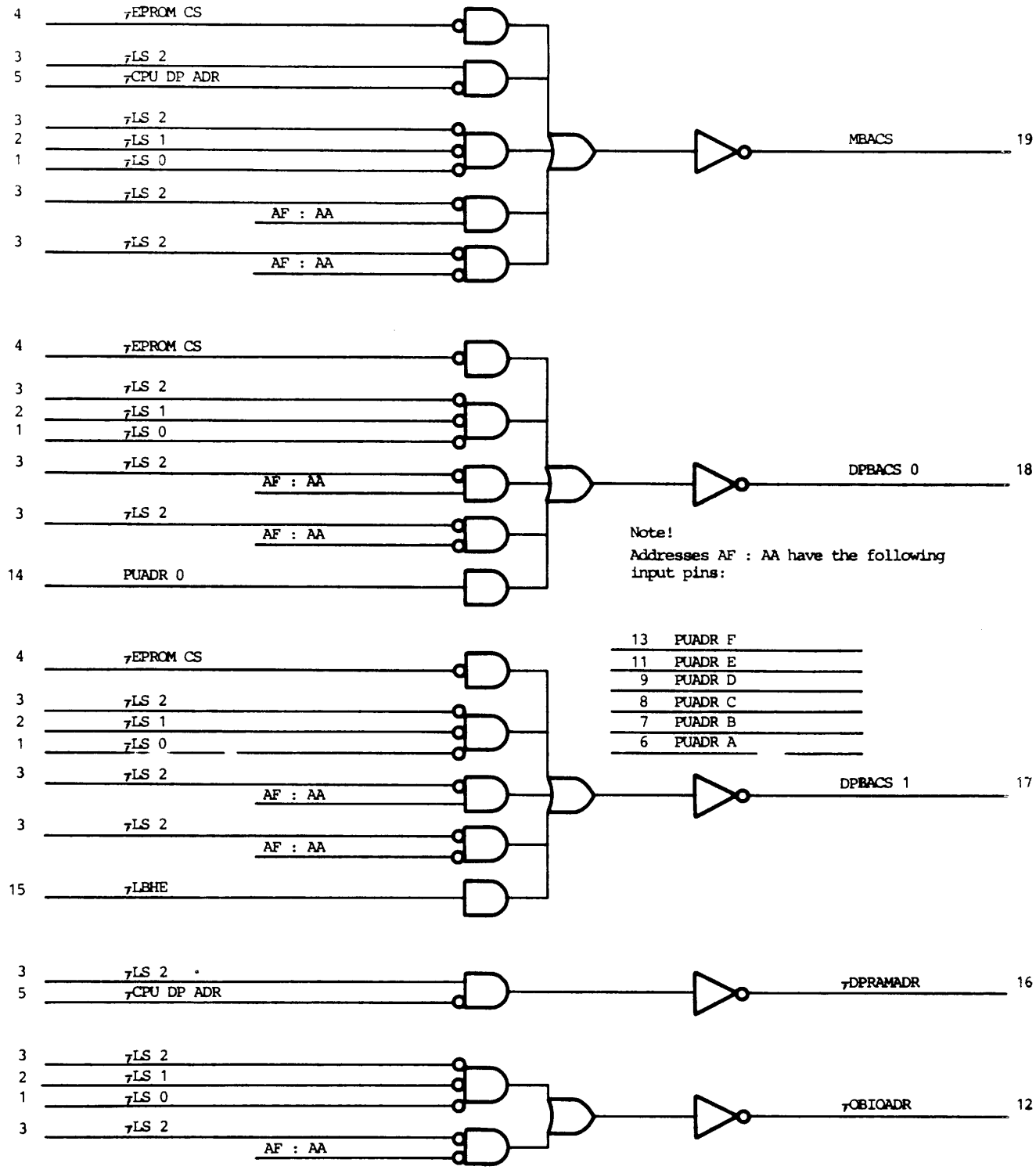


NOTE: Parity-BIT'S are mounted in 18-Pin sockets. When memory expansion is used, the parity-BITS of BANK Ø must be removed and monted on the expansion board.

The sockets of the parity-BIT'S have +5VOLT on PIN 9 and 0 VOLT on PIN 17, the rest of the memory bits have +5VOLT on PIN8 and 0VOLT on PIN16.


P1-3 +5V
P1-4 +5V
P1-5 +5V
P1-6 +5V
P1-81 +5V
P1-82 +5V
P1-83 +5V
P1-84 +5V
+5V
8 x 22µF/15V
20 x 47nF
RAM ARRAY 18 x 0,22µF keramisk
0V
0V
0V
P1-7 +12V
P1-8 +12V
+12V
1 x 15µF/20V
0V
P1-79 -12V
P1-80 -12V
-12V
1 x 15µF/20V
0V
P1-1 0V
P1-2 0V
P1-11 0V
P1-12 0V
P1-75 0V
P1-76 0V
P1-85 0V
P1-86 0V
P2-1 0V
P2-2 0V
P2-21 0V
P2-22 0V
0V

4.4 PAL and PROM Description 4.4

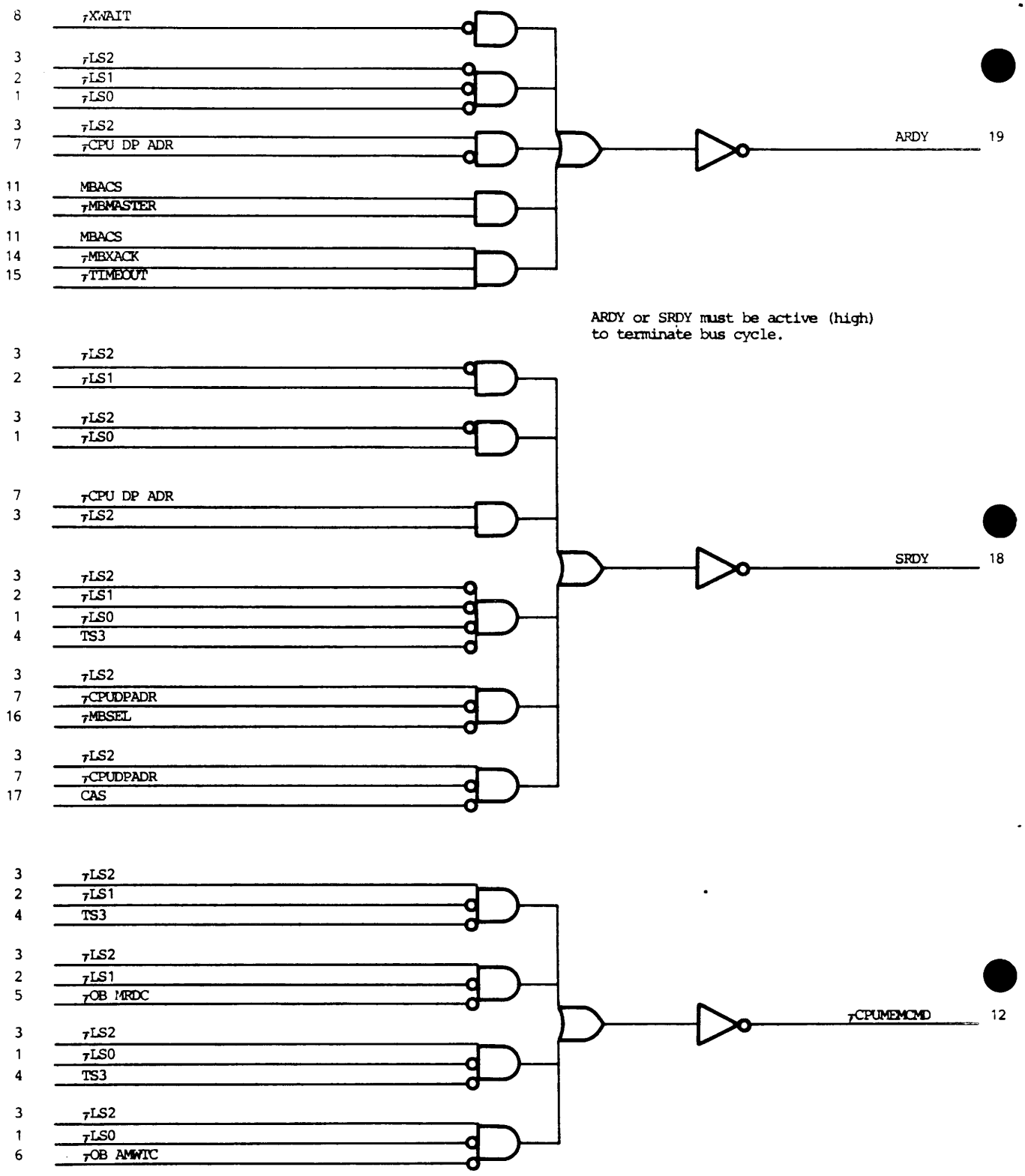


Description:

The address decoder generates control signals for multibus access (MBACS), dual-port bus buffer (DBACS 0, DBACS 1), on-board ram access (₇DPRAMADR) and on-board I/O access (₇OBIOADR).

₇LS2	₇LS1	₇LS0	FUNCTION
L	L	L	INTA
L	L	H	READ I/O
L	H	L	WRITE I/O
L	H	H	HALT
H	L	L	FETCH
H	L	H	READ MEM
H	H	L	WRITE MEM
H	H	H	PASSIVE

840111 VH/CU 841019 AMS

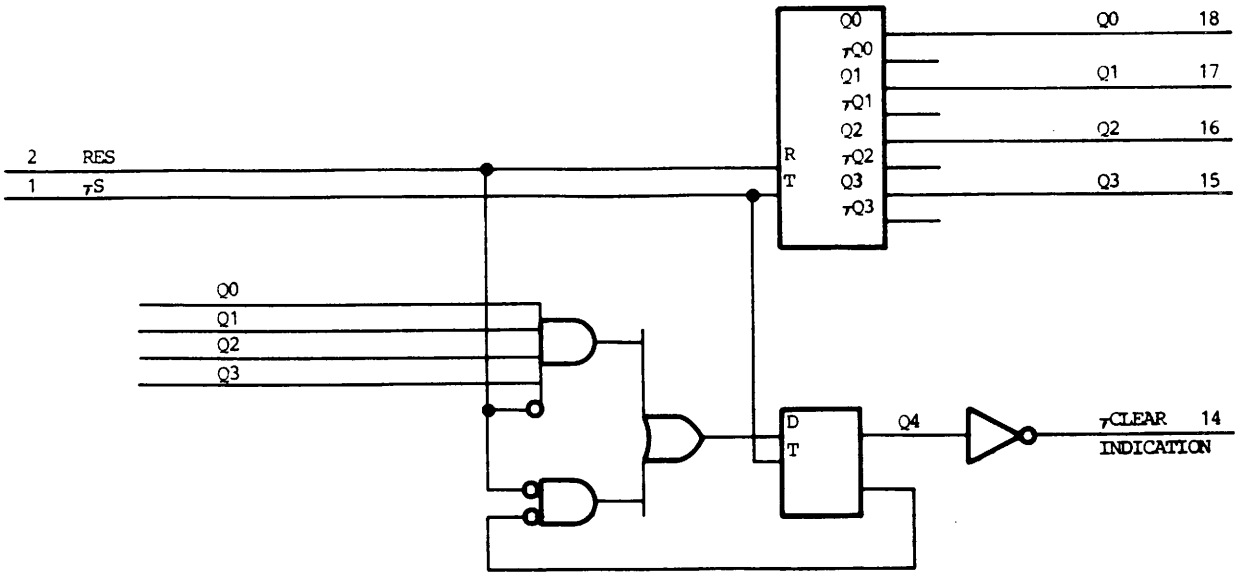


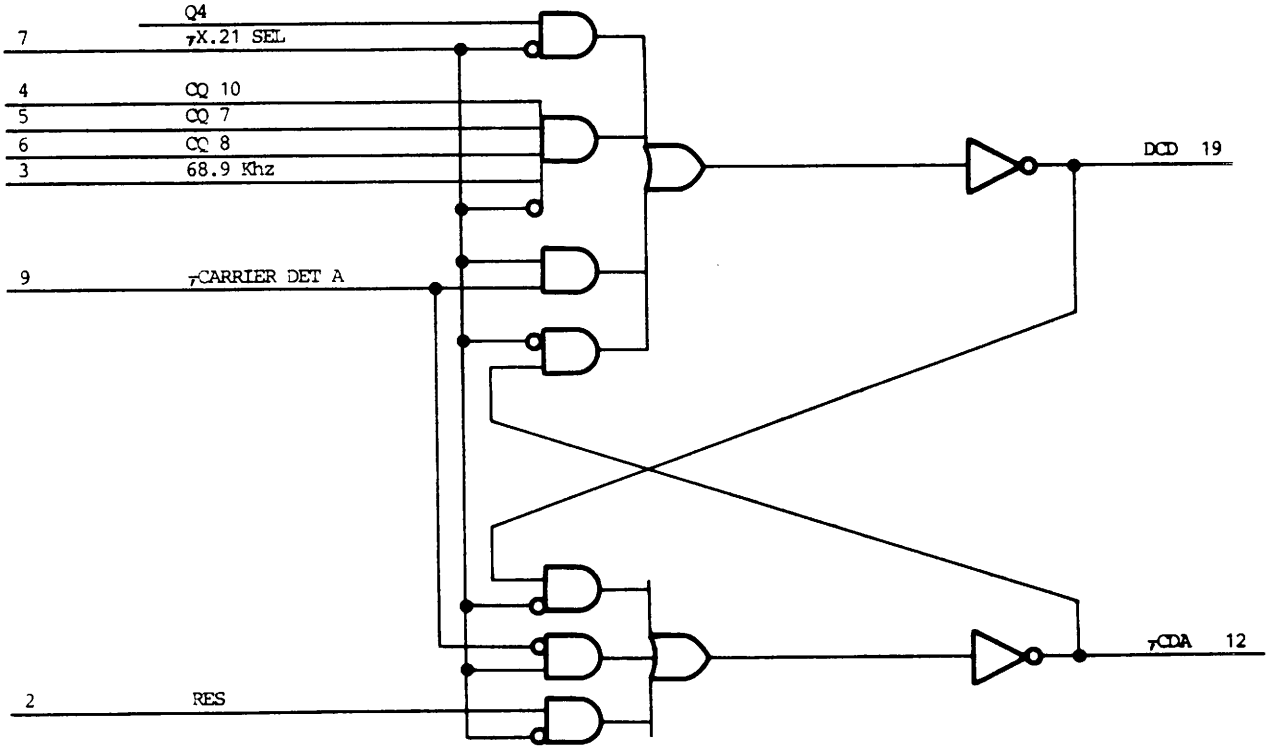
840111 VH/CU 841019 AMS

Description:

The circuit generates the ready signals ARDY and SRDY for the 80186 processor/82586 co-processor. The memory command signal (7CPUMEMCMD) is decoded from the latched status signals 7LS2, 7LS1 and 7LS0.

SYNCHRONOUS 4-BITS COUNTER
SYNCHRONOUS RESET

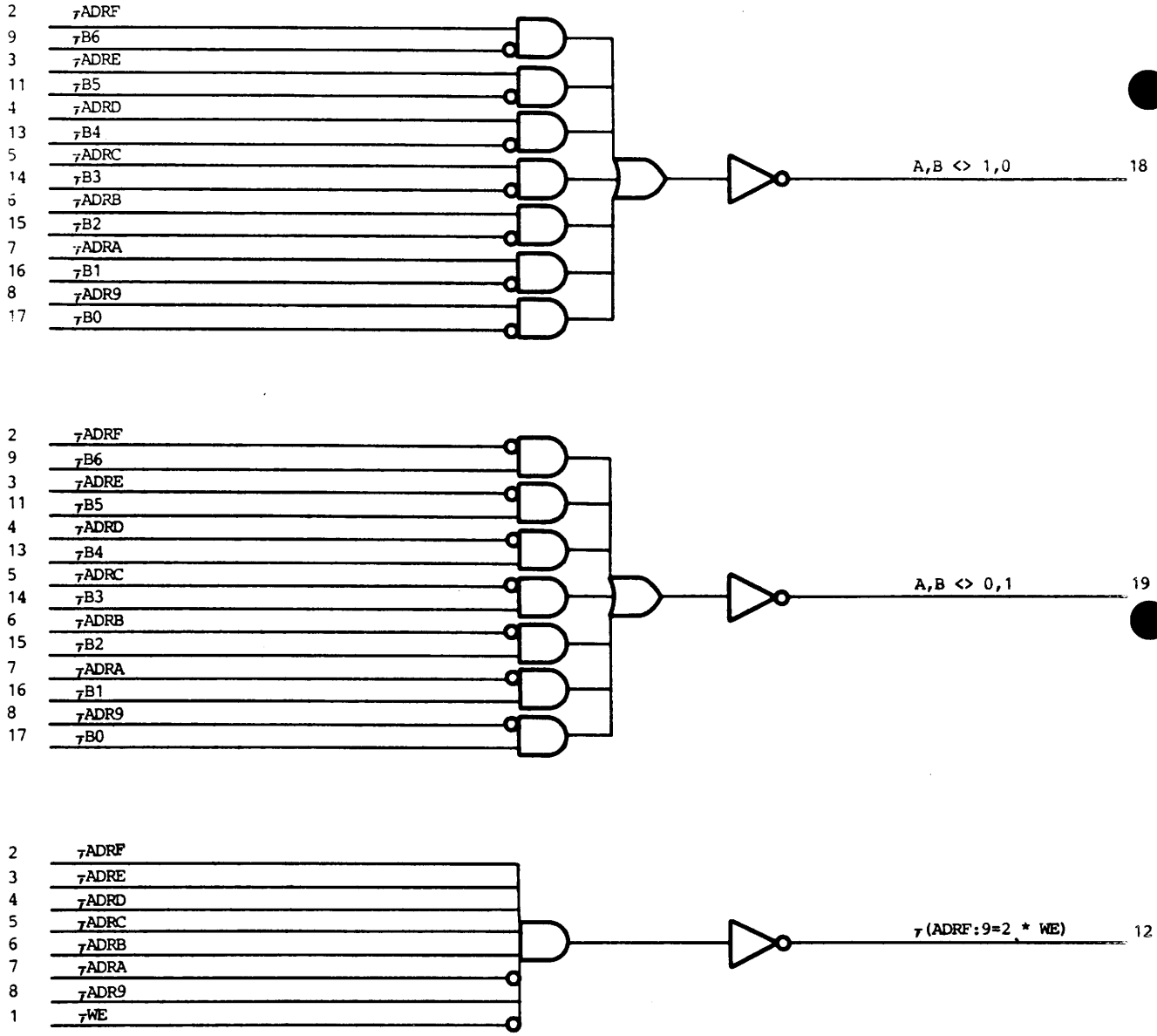




Description:

₇CLEAR INDICATION is an output, which becomes low after sixteen periods of ₇S supposing RES input has not been active during sixteen ₇S periods.
₇CDA is an output of a RS flip-flop, which is set by Q4 or CQ10, CQ8, CQ7,68,9 Khz true supposing ₇ X.21 input is low. The RES input resets the RS flip-flop (₇CDA = LOW and DCD high).
If the ₇X.21 input is high, the DCD output becomes the inverse of the ₇CARRIER DET A input.

840111 VH/CU 841019 AMS

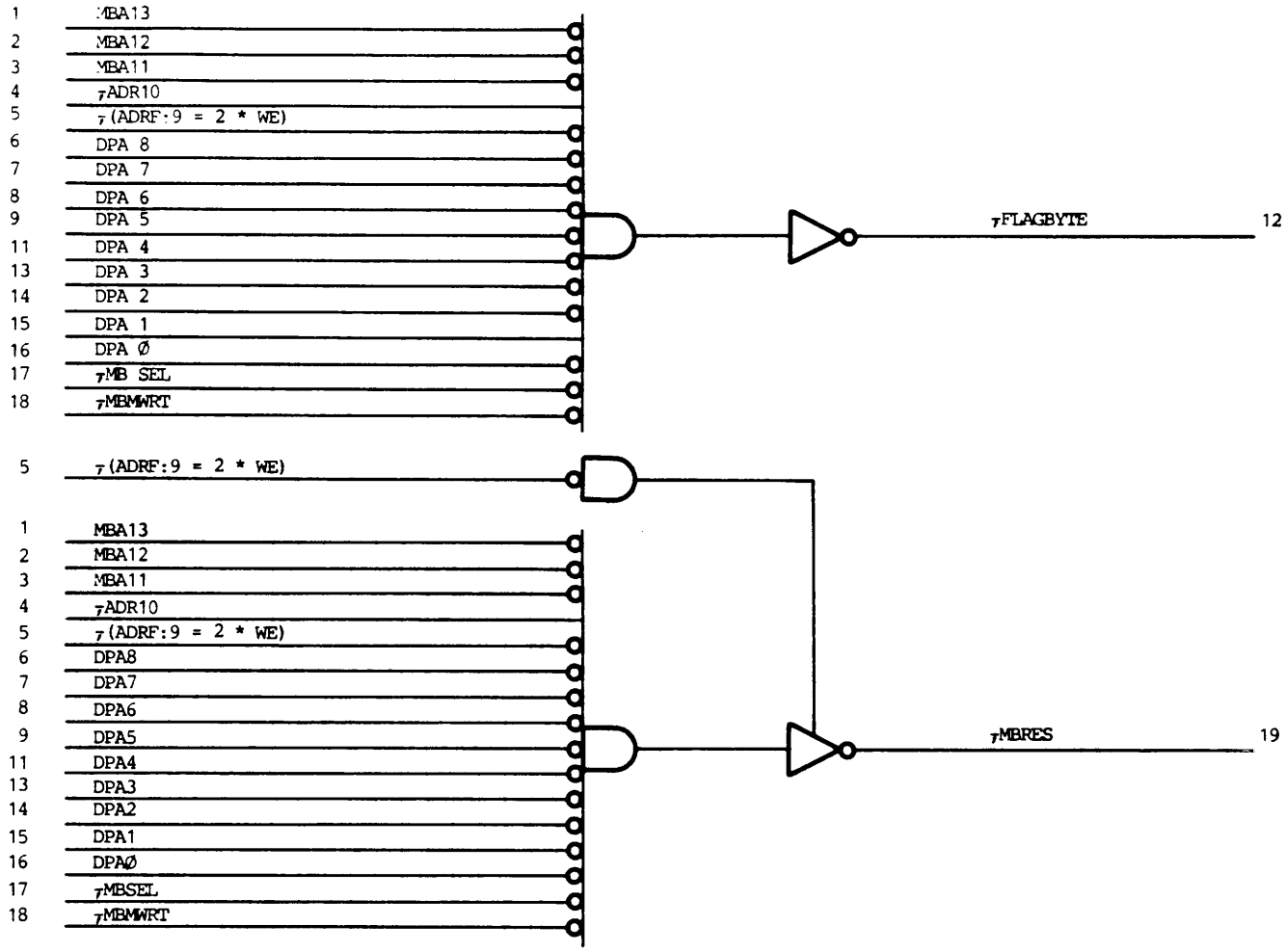


Description:

A,B <> 0,1 AND A,B <> 1,0 ARE OUTPUTS, WHICH WHEN BOTH HIGH INDICATES THAT PATTERN ADR IS EQUAL TO PATTERN B.

₇(ADRF:9 = 2 *WE) IS AN OUTPUT WHICH IS LOW WHEN ₇ADRF, ₇ADRE, ₇ADRD, ₇ADRC, ₇ADRB, ADRA, ₇ADR9 ARE ALL HIGH AND ₇WE IS LOW.

840111 VH/CU 841019 AMS

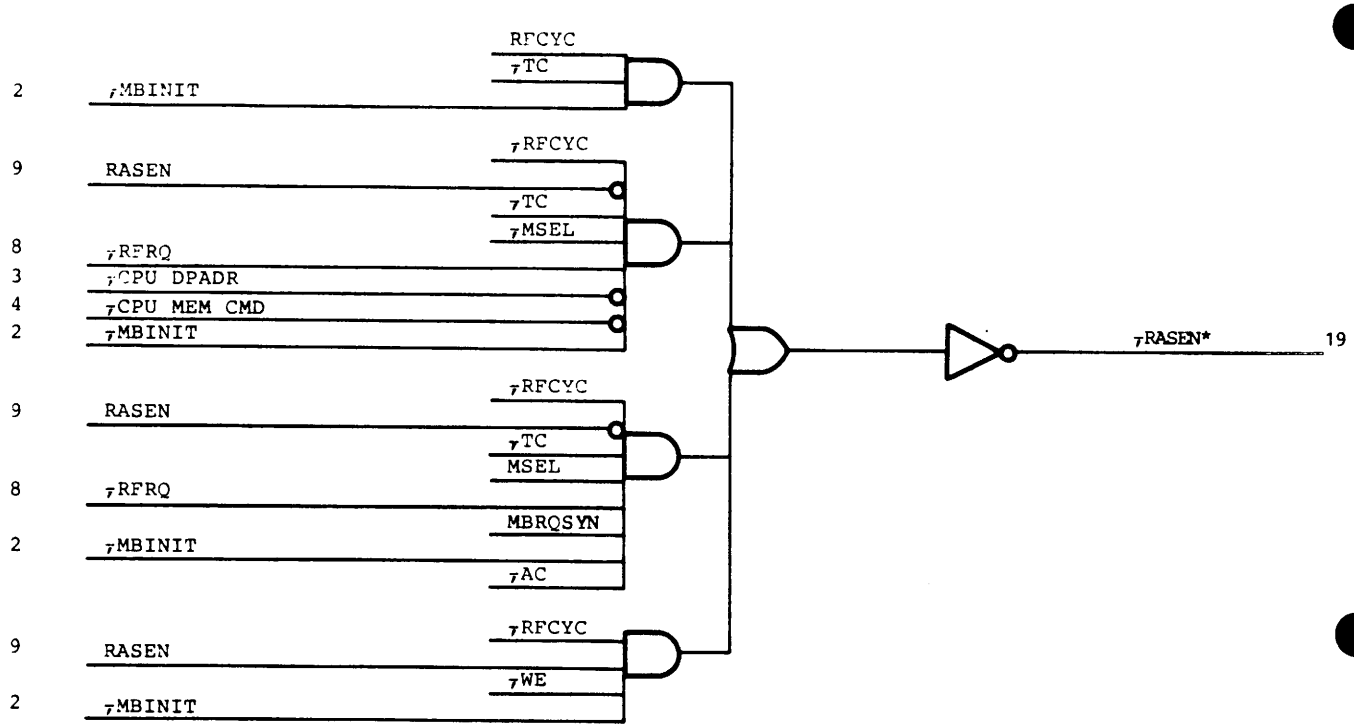


ADDRESS BITS	17 16 15 14 13 12 11 10	F E D C	B A 9 8	7 6 5 4	3 2 1 0	
FLAG BYTE	←MODULE SEL→		1		1	= 402H
RESET BYTE	←MODULE SEL→		1			= 400H

Description:

₇FLAGBYTE and ₇MBRES are outputs which becomes low when a multibus master writes into the FLAGBYTE respective the RESET BYTE.

840111 VH/CU 841019 AMS

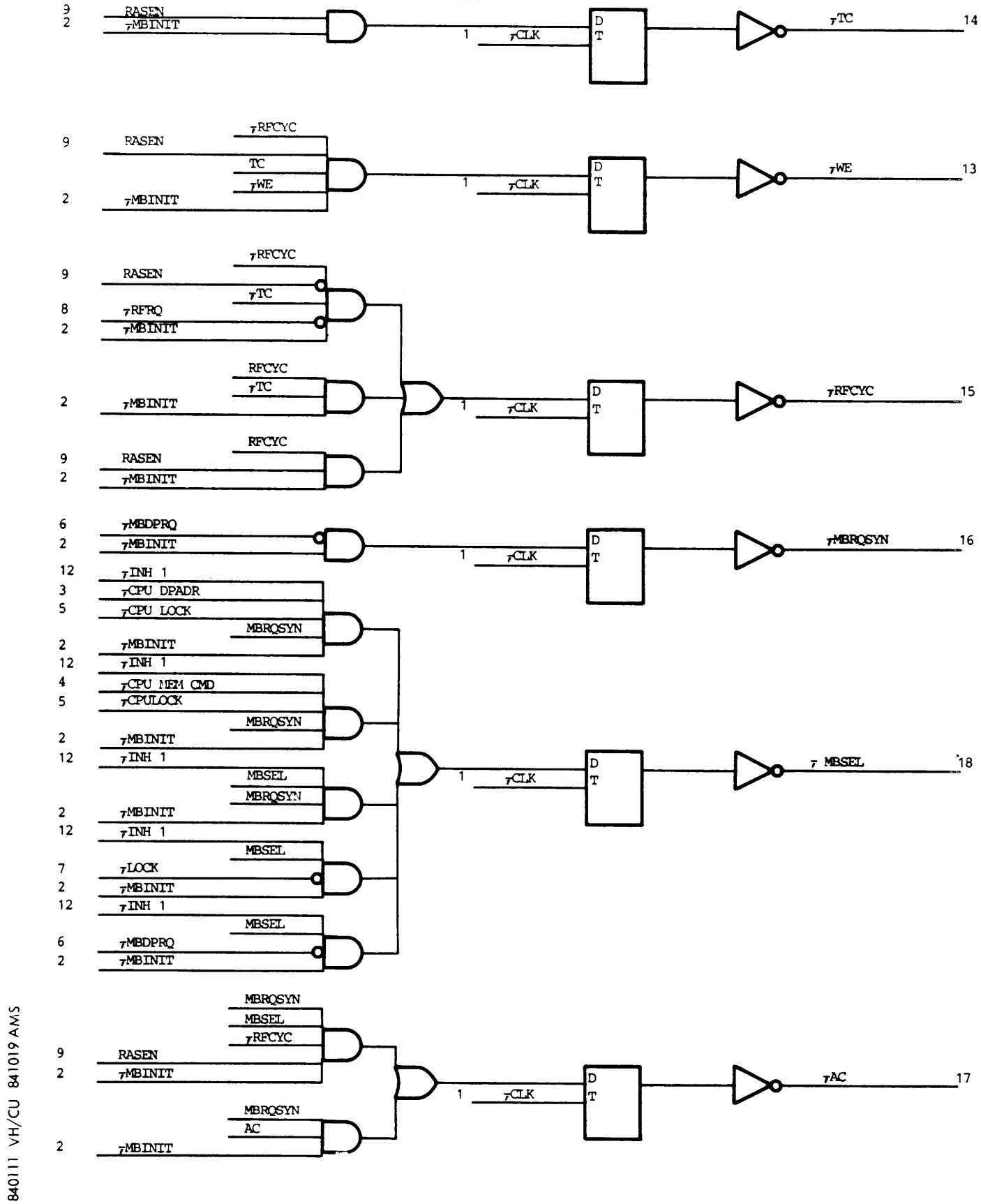


840111 VH/CU 841019 AMS

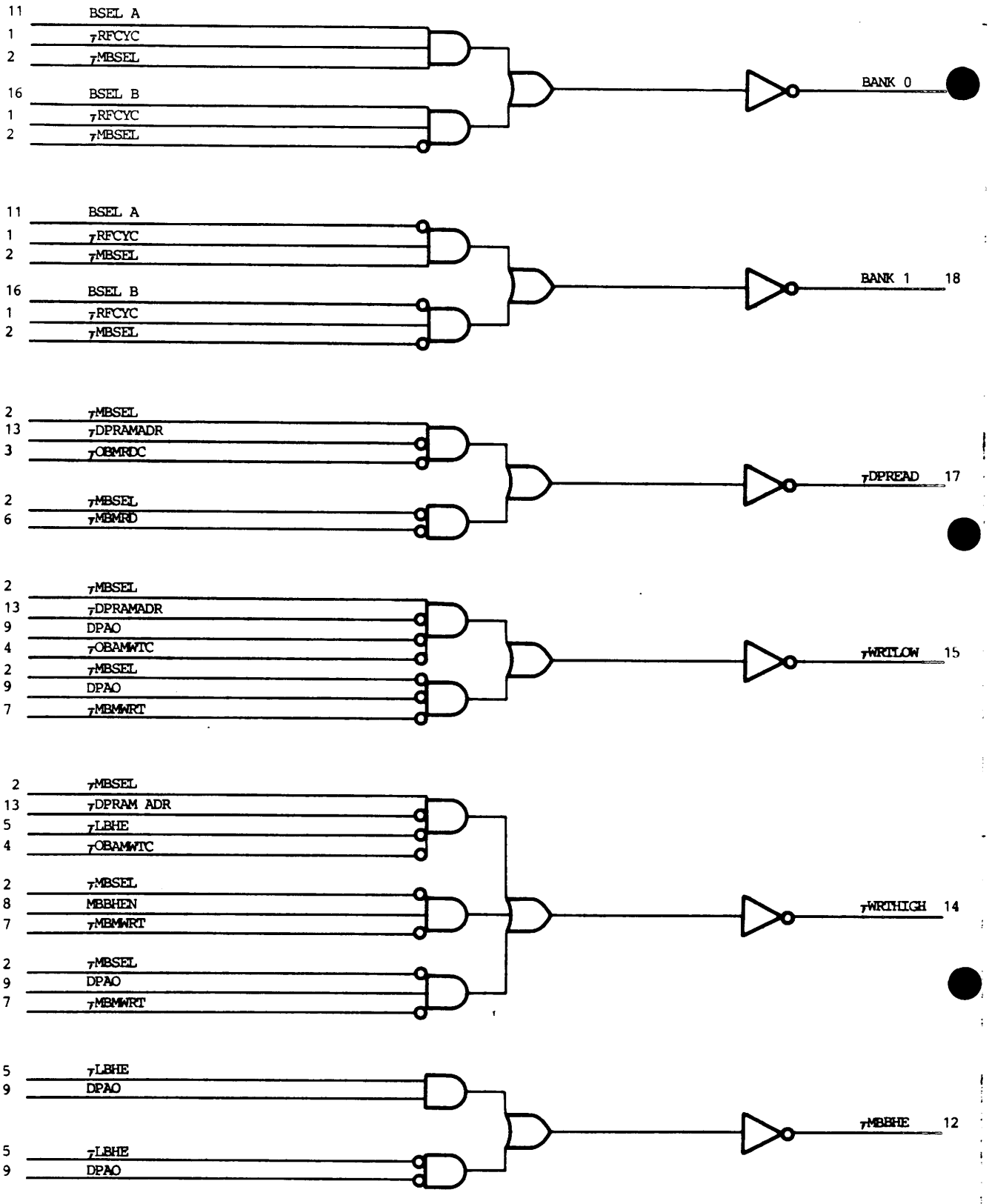
Description:

This circuit controls access to the dynamic RAM from 2 sources-CPUDPADR * CPUMEMCMD and MBDPRQ. 7MSEL = low indicates that MBDPRQ is being serviced.

A refresh cycle is generated when 7RFRQ = low. The circuit also controls the timing of RAS, CAS and the address multiplexing. The MSEL signal cannot be generated when 7INH 1 = low.



840111 VH/CU 841019 AMS

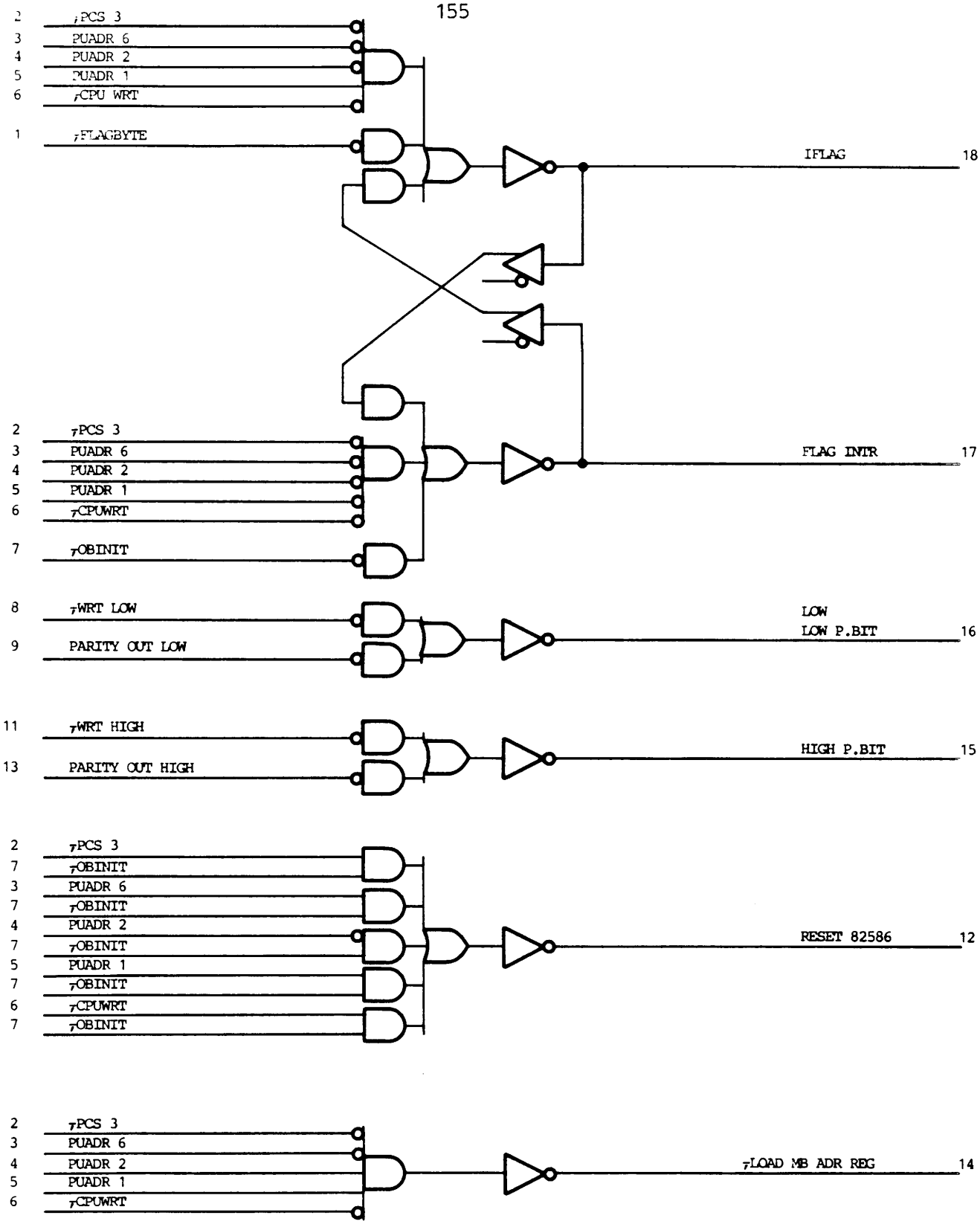


840111 VH/CU 841019 AMS

Description:

BANK 0 and BANK 1 are bank select signals for the two DRAM banks (one bank on the ETC printed circuit itself and one bank on the memory expansion board).

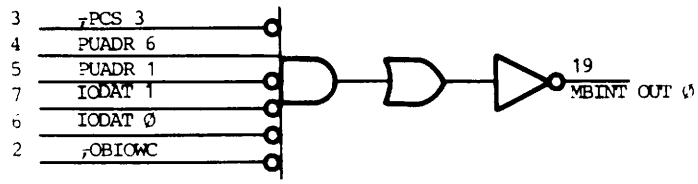
₇DPREAD is output enable signal for the DRAM read data latches.
₇WRTLOW, ₇WRTHIGH are byte write control signals for the DRAM.
₇MBBHE is a byte control signal for the multibus.

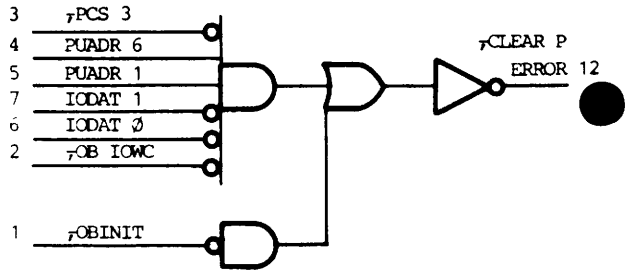


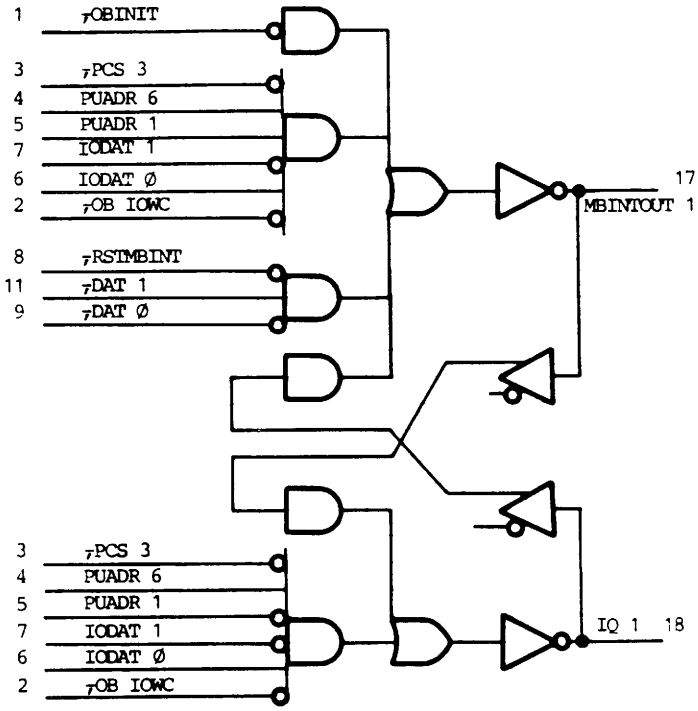
Description:

FLAG INTR is a RS flip-flop, which is set by an 80186 CPU I/O write command or the ₇FLAGBYTE signal active (low). The RS flip-flop is reset by an 80186 CPU I/O write command or ₇OBINIT active (low).
LOW P.BIT/HIGH P.BIT outputs are low/high parity bits used as inputs to the parity generator/checker.

RESET 82586 is an output which resets the 82586 LCC during an 80186 CPU I/O write command.
₇LOAD MB ADR REG loads the megabyte select register during an 80186CPU I/O write cmd.







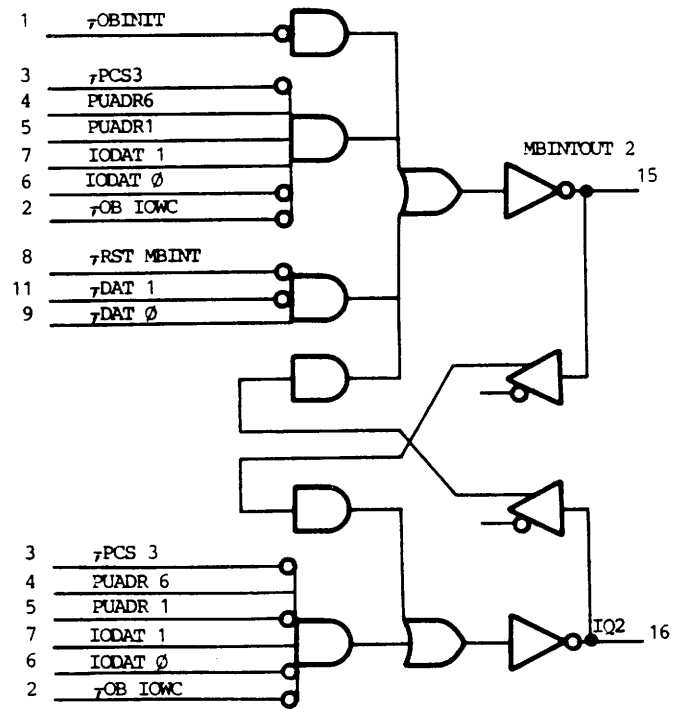
Description:

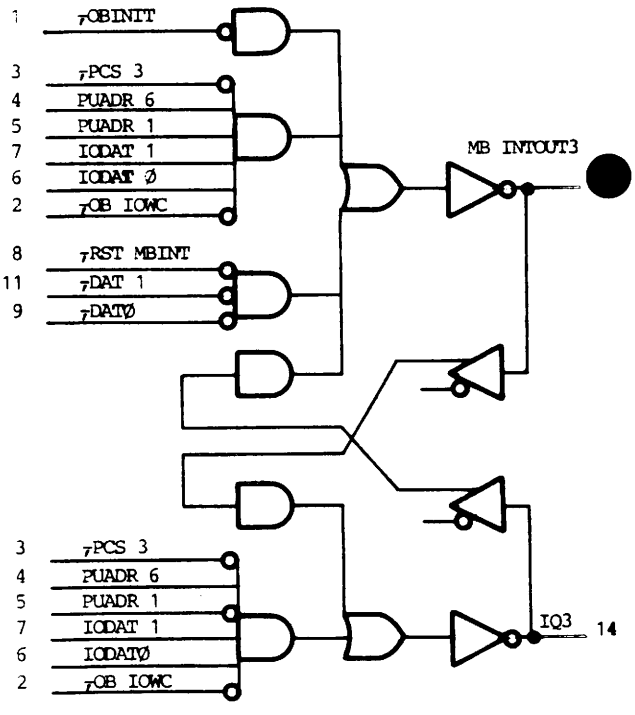
The circuit contains 3 set-reset latches (MBINTOUT1 -MBINTOUT 3) and 2 nonlatched outputs (MBINTOUTØ and ₇CLEAR P. ERROR).

PCS3 * OBIOWC * PUADR 6 * ₇PUADR 1 sets the latc (MBINTOUT = 1) selected by IODATØ, IODAT 1 or pul ses MBINTOUTØ if IODATØ = IODAT1 = low.

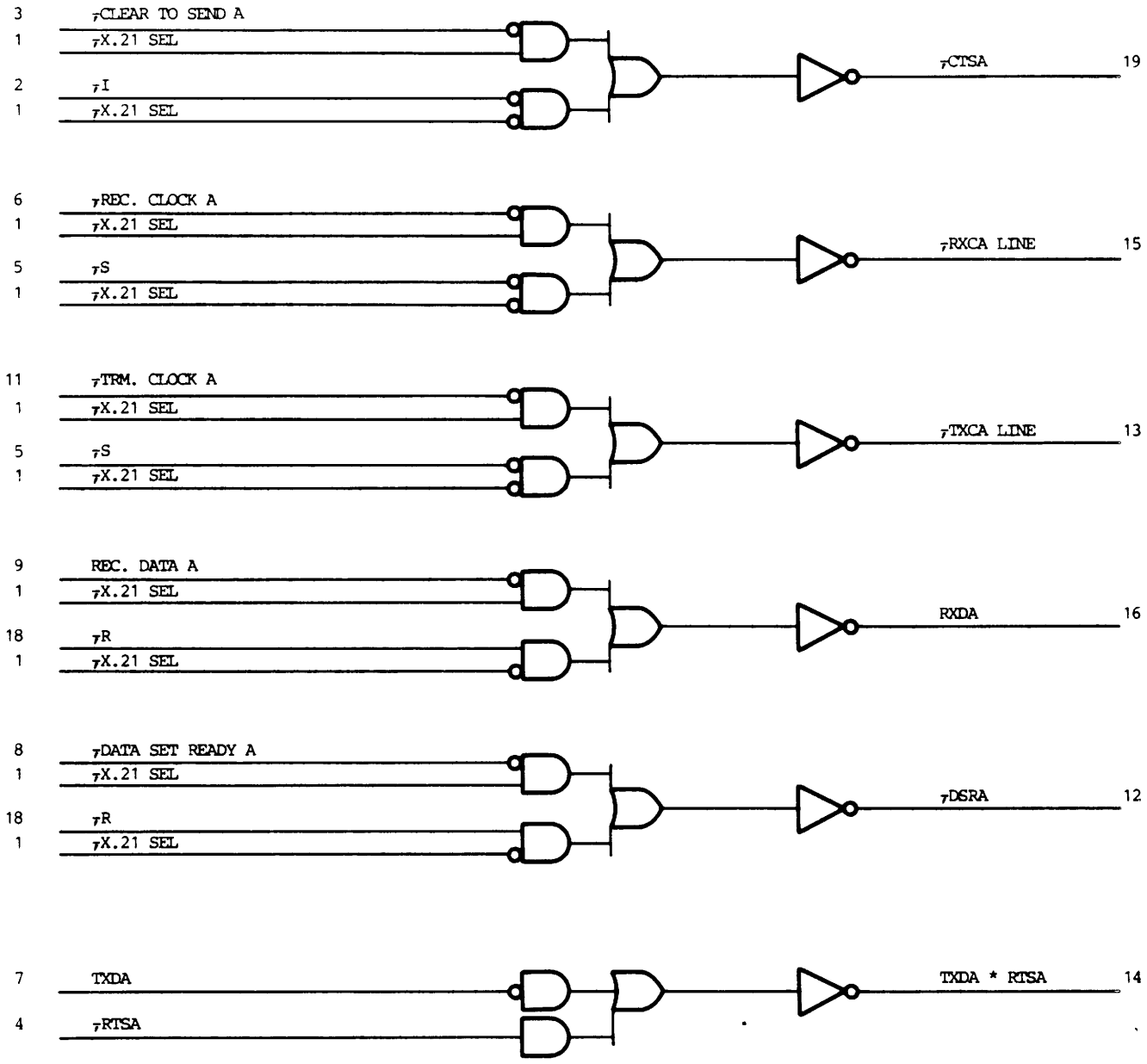
PCS 3 * OBIOWC * PUADR 6 * PUADR 1 resets the latch (MBINTOUT = 0) selected by IODATØ, IODAT1 or pulses ₇CLEAR P.ERROR (active low) if IODATØ = IODAT1 = low.

₇RSTMBINT clears the latch selected by ₇DAT1, ₇DATØ. OBINIT clears all latches and pulses ₇CLEAR P.ERROR.





840111 VH/CU 841019 AMS



PIN 17 NOT USED

840111 VH/CU 841019 AMS

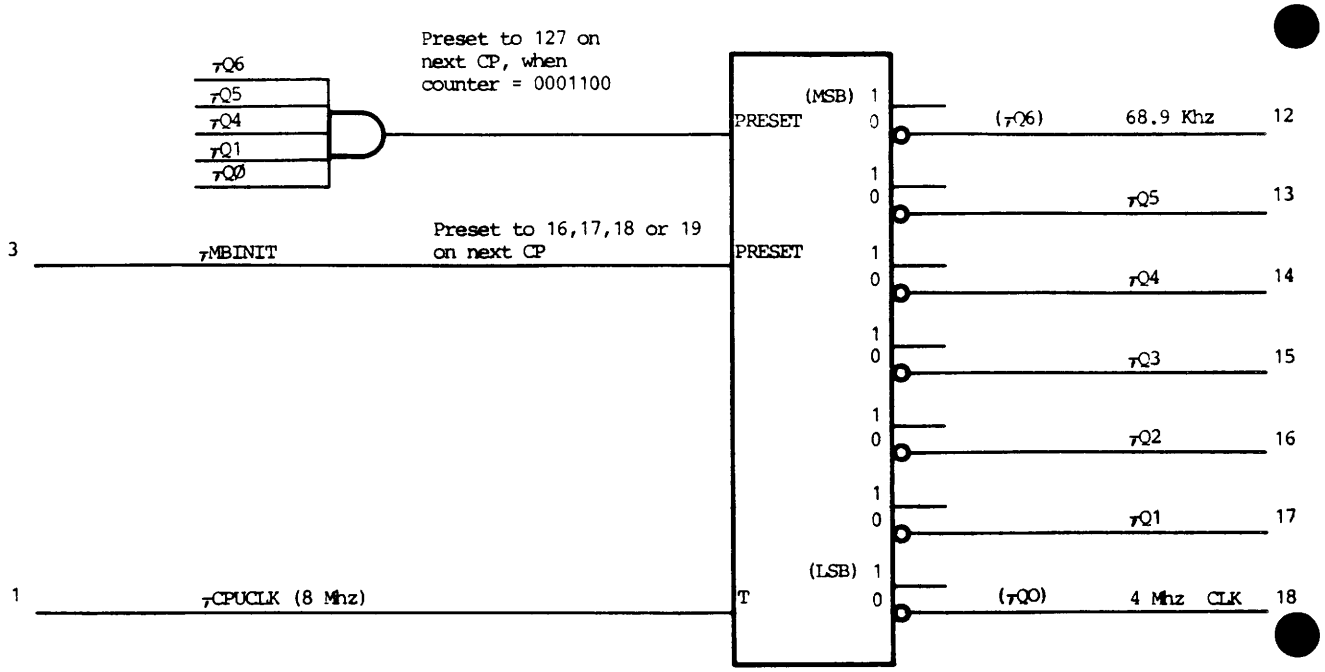
Description:

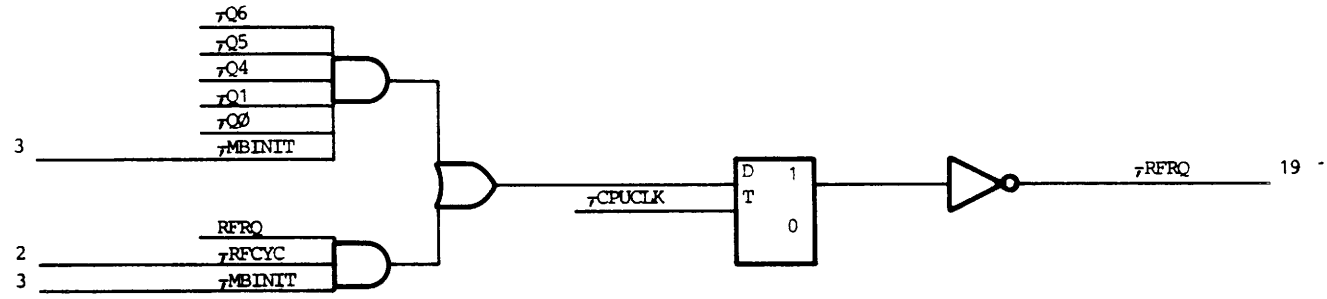
This selector selects between five V.24 and three X.21 signals as indicated below:

OUTPUT PIN	19	15	13	16	12
X.21 (7X.21=low) V.24 (7X.21=high)	7I 7CLEAR TO SEND A	7S 7REC. CLOCK A	7S 7TRM. CLOCK A	R REC. DATA A	R 7DATA SET RDY. A

Output PIN 14 is transmitter serial output "anded" with request to send.

7-BITS SYNCRON COUNT-DOWN COUNTER WITH
SYNCRON PRESET TO 127 or
SYNCRON PRESET TO 16,17,18 or 19





Description:

With a clock frequency of 8 Mhz the refresh timer generates a refresh request (7RFRQ = low) every 14.5 micto sec. RFRQ is cleared when the refresh request is accepted (7RFCYC = low).

The 7-bits counter counts from all ones down wards to 12 decimal, this is 116 counts (128-12)~ 116*125 nS = 14.5 µS.

116 is divideable by 2 and 4, which gives symmetric outputs on Q0 (4 Mhz) and Q1 (2 Mhz).

840111 VH/CU 841019 AMS

OCTAL ADDR	HEX DATA	OCTAL ADDR	HEX DATA	OCTAL ADDR	HEX DATA	OCTAL ADDR	HEX DATA	OCTAL ADDR	HEX DATA	OCTAL ADDR	HEX DATA	OCTAL ADDR	HEX DATA	OCTAL ADDR	HEX DATA
000	0	100	0	200	0	300	0	400	0	500	0	600	0	700	8
												601	8		
										502	8				
								403	8						
						304	3								
				205	8										
		106	3												
007	8														
													610	9	
										511	9	611	8		
								412	9	512	8				
						313	9	413	8						
				214	9	314	8								
		115	9	215	8										
016	9	116	8												
017	8														
										520	A				
								421	A	521	9				
						322	A	422	9	522	8				
				223	A	323	9	423	8						
		124	A	224	9	324	8								
025	A	125	9	225	8										
026	9	126	8												
027	8														
								430	B						
						331	B	431	A						
				232	B	332	A	432	9						
		133	B	233	A	333	9	433	8						
034	B	134	A	234	9	334	8								
035	A	135	9	235	8										
036	9	136	8												
037	8														
						340	C								
				241	C	341	B								
		142	C	242	B	342	A								
043	C	143	B	243	A	343	9								
044	B	144	A	244	9	344	8								
045	A	145	9	245	8										
046	9	146	8												
047	8														
				250	D										
		151	D	251	C										
052	D	152	C	252	B										
053	C	153	B	253	A										
054	B	154	A	254	9										
055	A	155	9	255	8										
056	9	156	8												
057	8														
		160	E												
061	E	161	D												
062	D	162	C												
063	C	163	B												
064	B	164	A												
065	A	165	9												
066	9	166	8												
067	8														
070	F														
071	E														
072	D														
073	C														
074	B														
075	A														
076	9														
077	8	177	0	277	0	377	0	477	0	577	0	677	0	777	0

Addresses not shown or data = 0_H are unprogrammed cells (All data bits = "0").

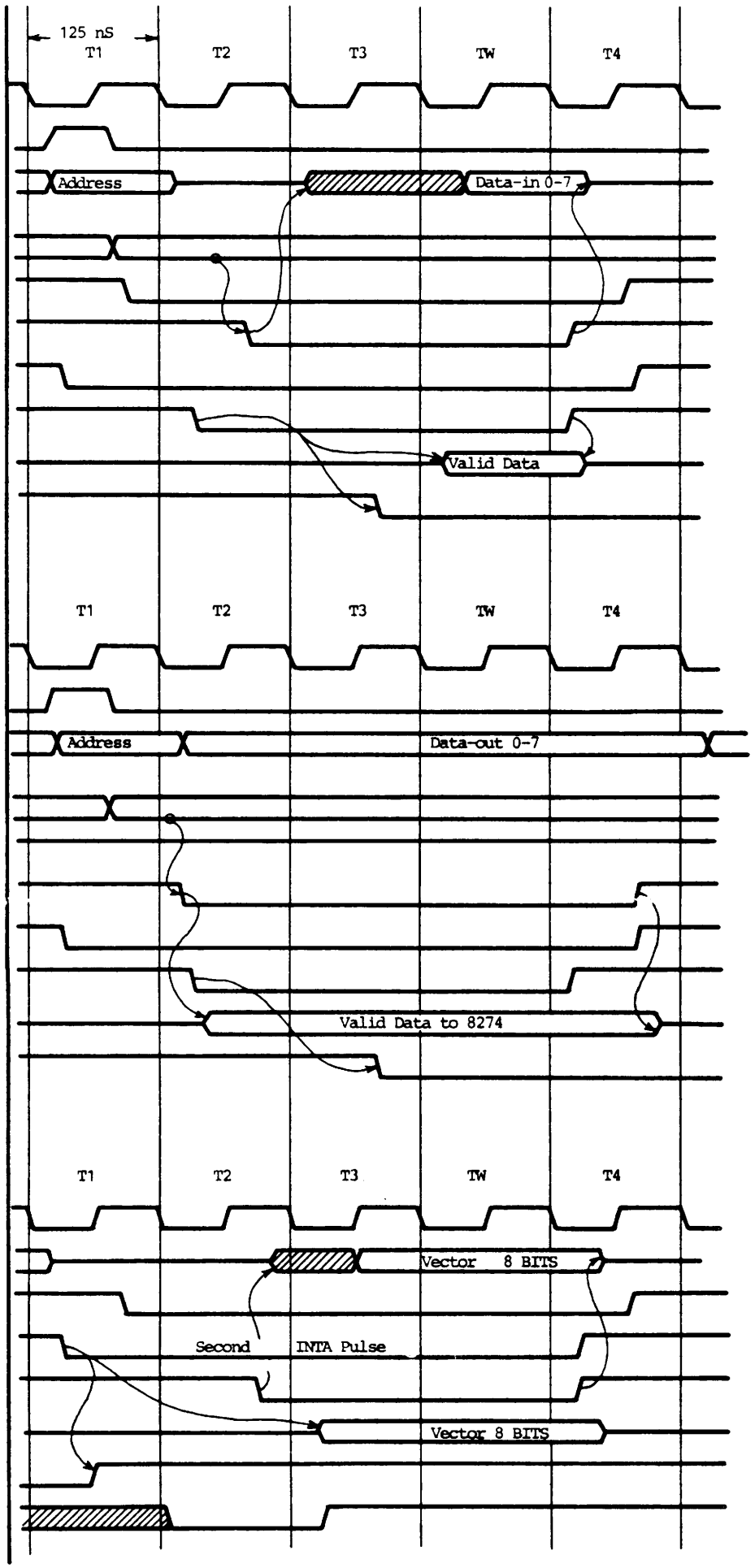
Address pins are : 14,15,1 (START STRAP) 2,3,4 (SIZE STRAP) 7,6,5 ($_7$ADR 13_H - $_7$ADR 10_H)

Data pins are 9 (MB SUB ADR) 10,11,12 (MBA 13_H - MBA 10_H).

ETC601/611 ROA 917 (512 x 4 Bipolar PROM)

A14721

4.5 Timing Diagrams



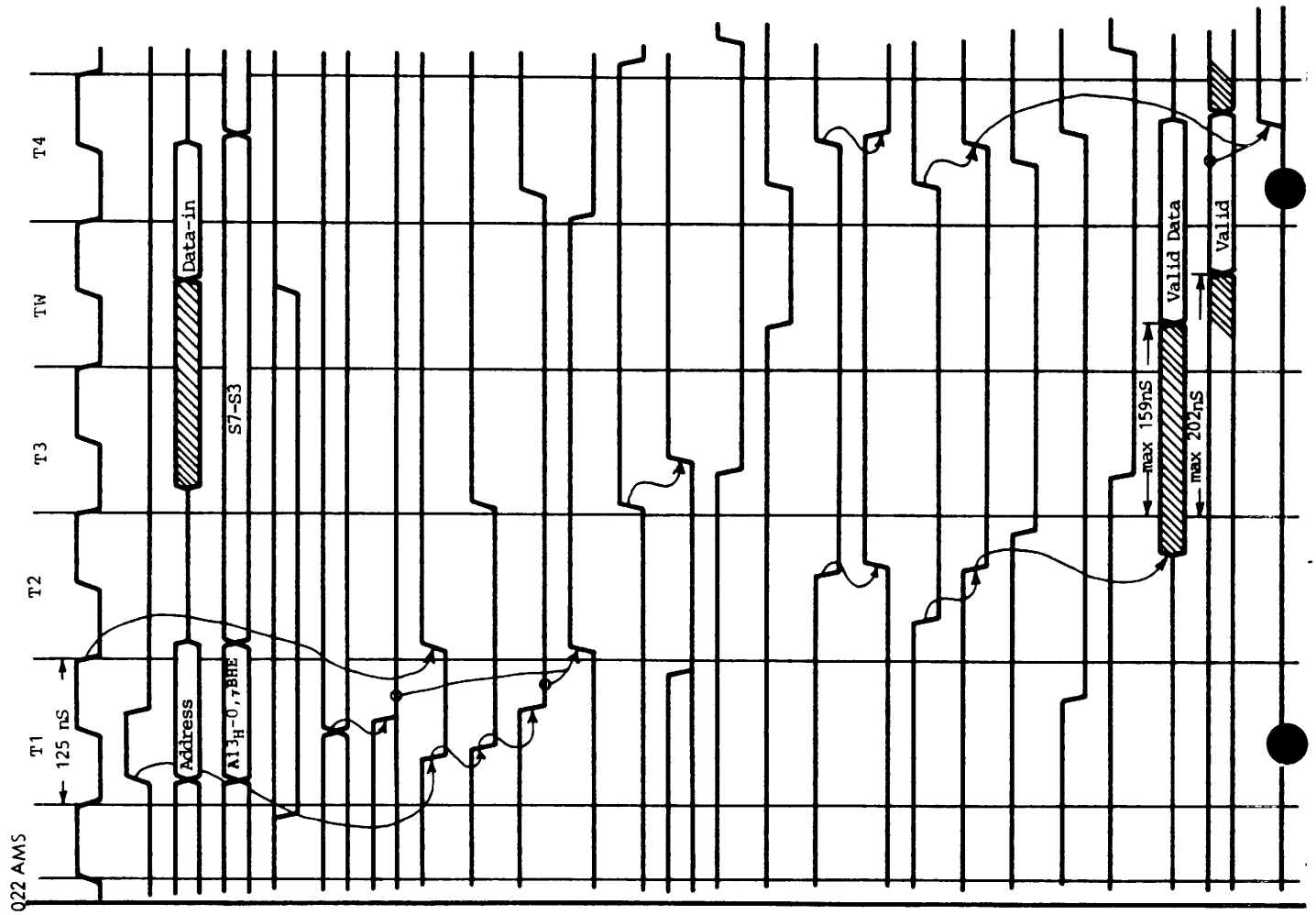
840822 VH/CU 841023 AM S

ETC601/611

8274 MPSC I/O READ, I/O WRITE and INTERRUPT ACKNOWLEDGE
(I/O Read, I/O Write Wait States are programmed to 1)

TC 1

A14722

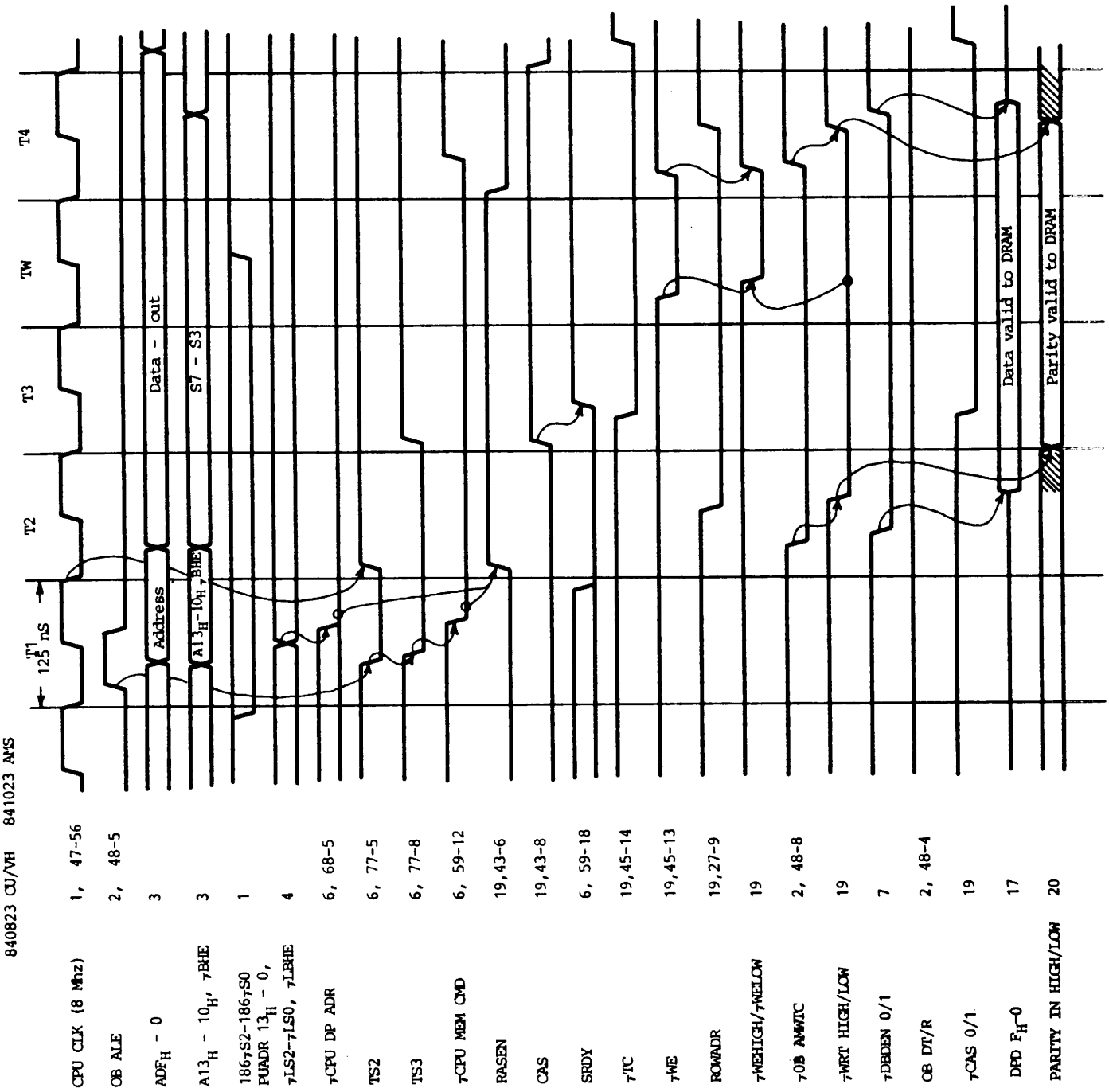


ETC601/611

80186 ACCESS TO DUAL PORT DRAM (Read Cycle).

TC 2

A14723

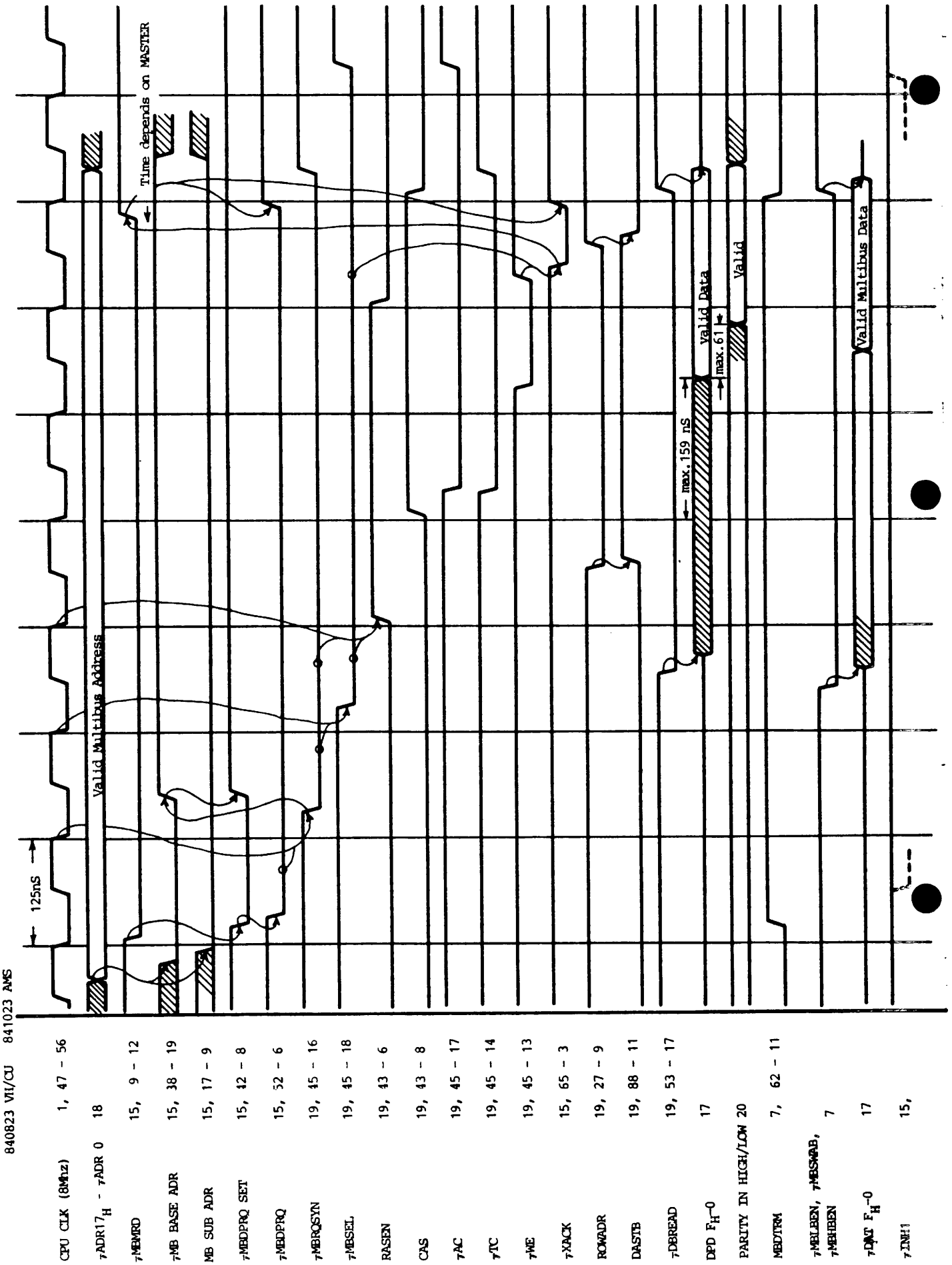


ETC601/611

80186 ACCESS TO DUAL-PORT DRAM (Write Cycle).

TC 3

A14724

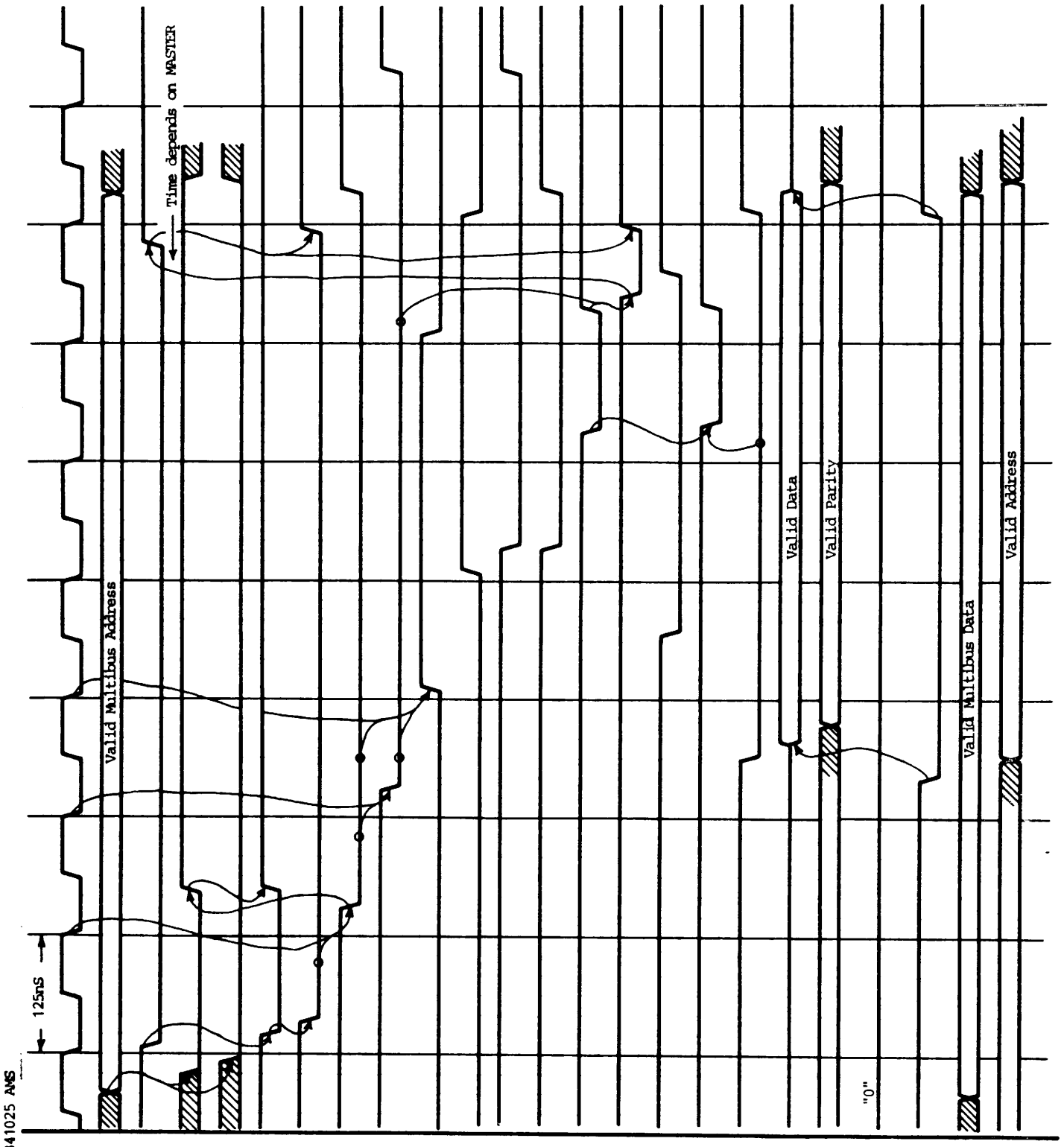


ETC601/611

MULTIBUS MASTER ACCESS TO DUAL-PORT DRAM (Read Cycle)

TC 4

A14725

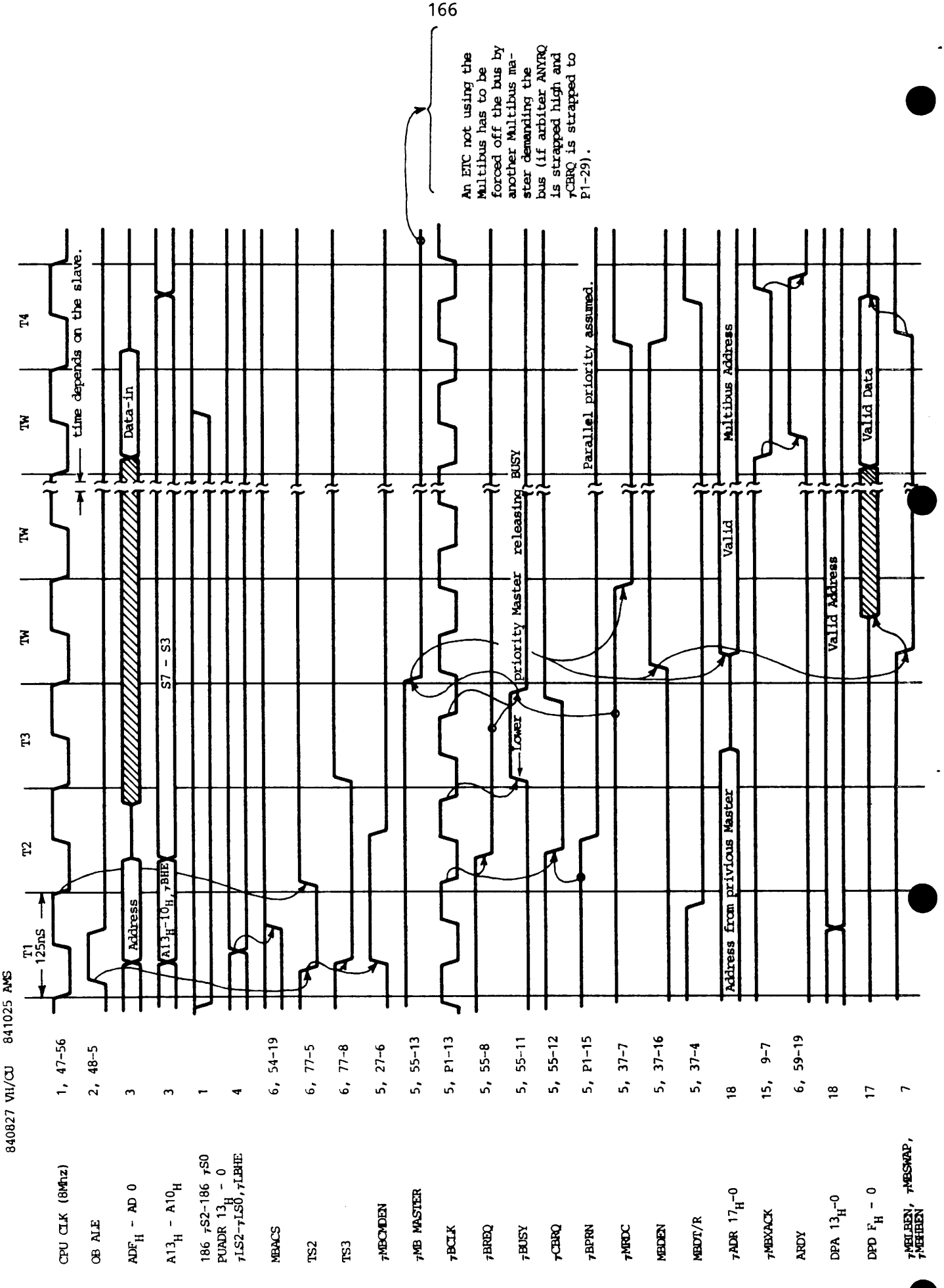


ETC601/611

MULTIBUS MASTER ACCESS TO DUAL-PORT DRAM (Write Cycle)

TC 5

A14726

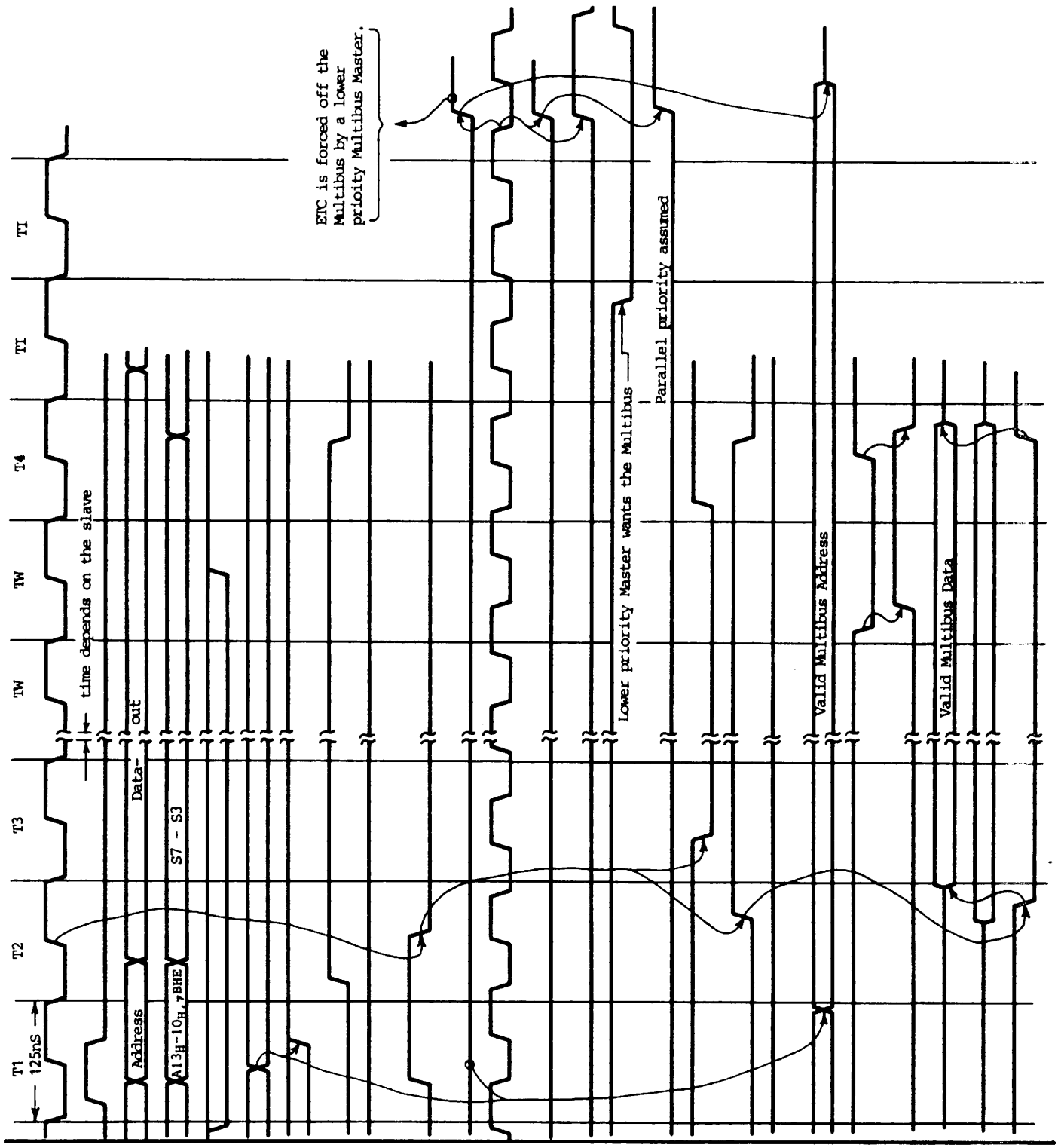


ETC601/611

80186 ACCESS OF MULTIBUS (memory Read Cycle).

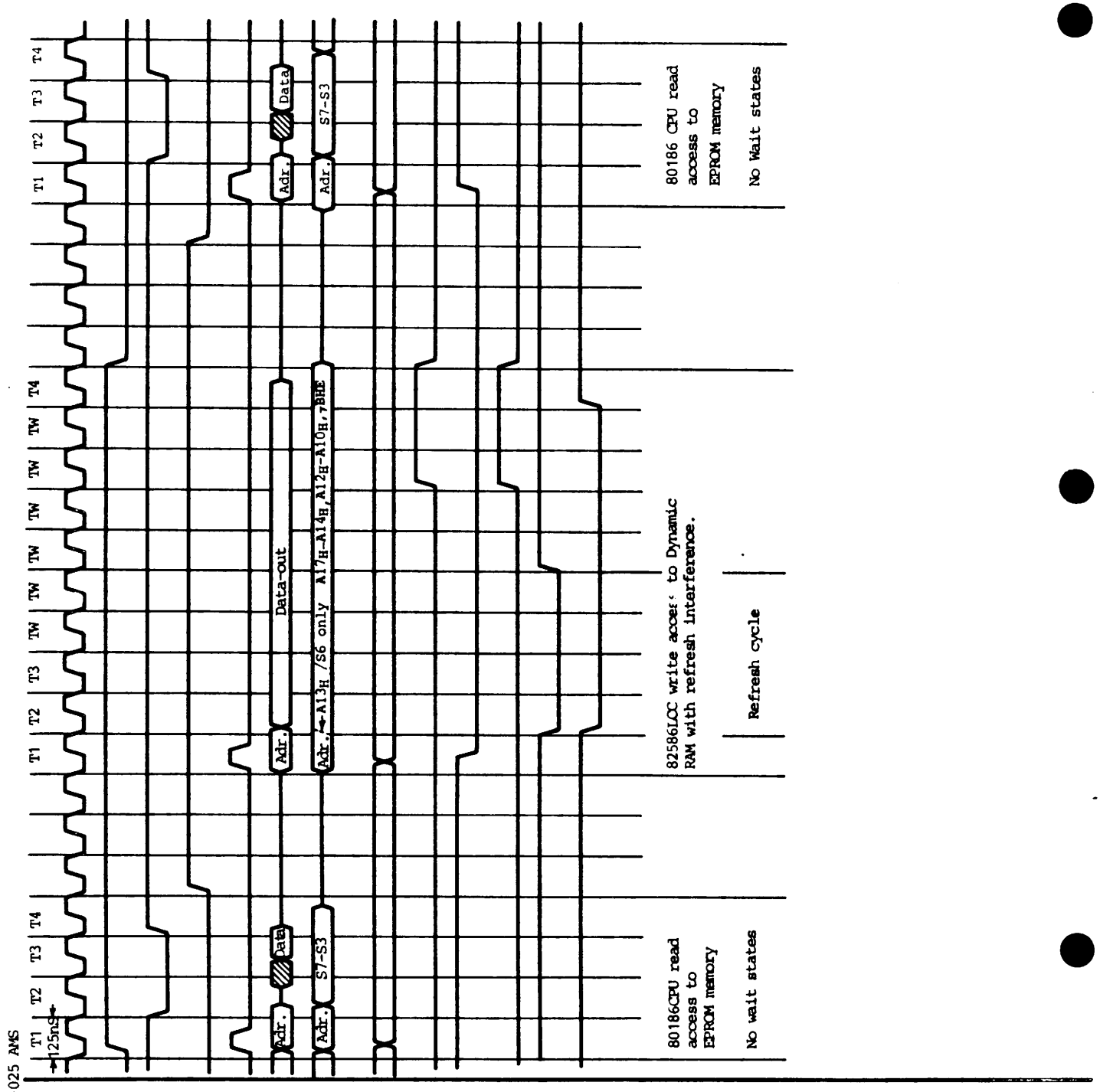
TC 6

A14727



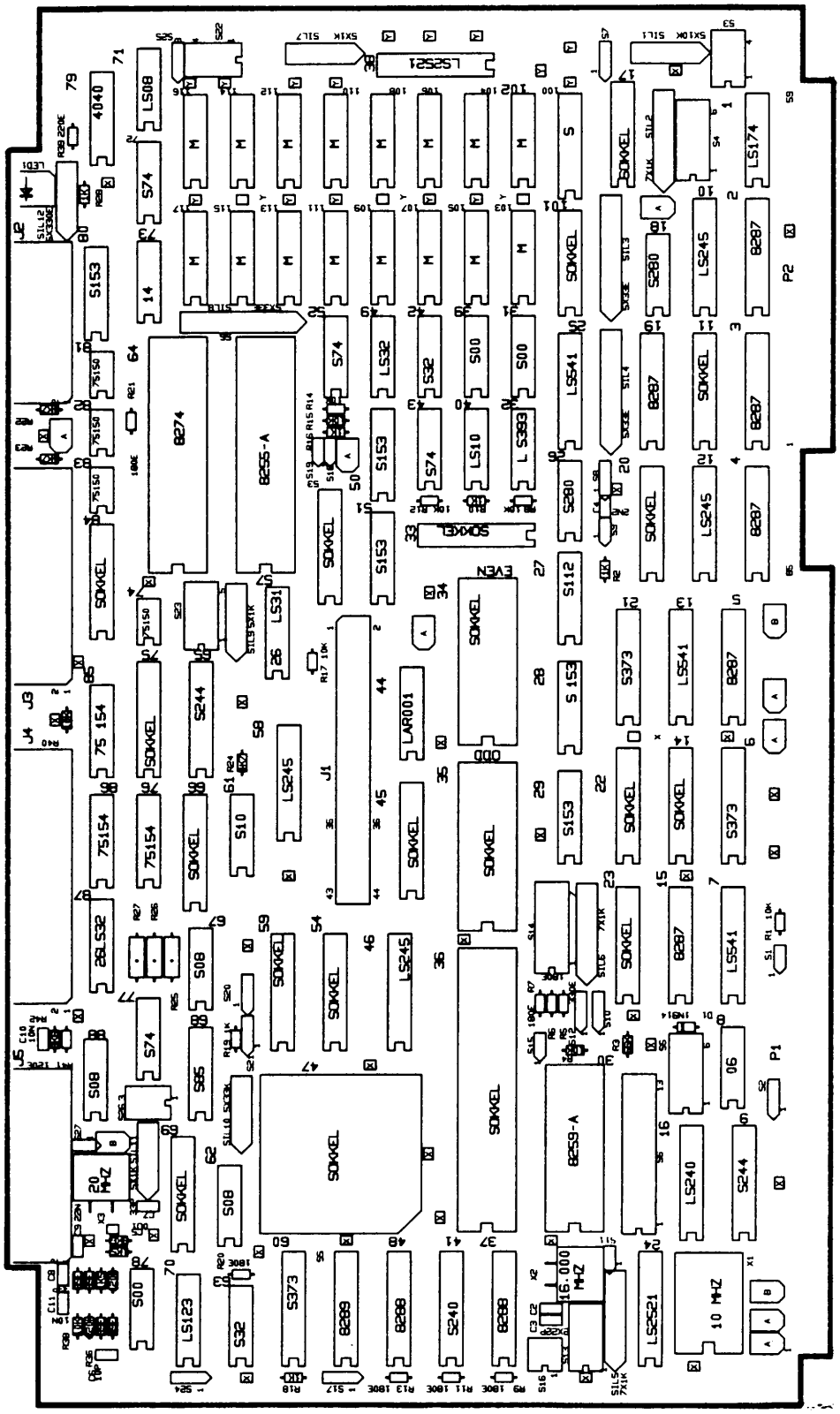
ETC601/611 80186 ACCESS OF MULTIBUS (Memory Write Cycle). TC 7

A14728



HOLD/HOLD ACKNOWLEDGE TIMING
EPROM ACCESS TIMING AND
REFRESH INTERFERENCE

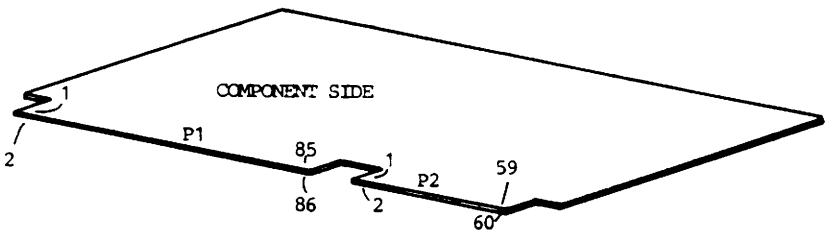
4.6 Assembly Drawing



PCB156 COMPONENT NOTATION

4.7 Plugs/Jacks

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	0 VOLT	2	0 VOLT
3	+ 5 VOLT	4	+ 5 VOLT
5	+ 5 VOLT	6	+ 5 VOLT
7	+ 12 VOLT	8	+ 12 VOLT
9	N. C	10	N. C
11	0 VOLT	12	0 VOLT
13	₇BCLK	14	₇INIT
15	₇BPRN	16	₇BPRQ
17	₇BUSY	18	₇BREQ
19	₇MRDC	20	₇MWTC
21	₇IORC	22	₇IOWC
23	₇XACK	24	₇INH 1
25	₇LOCK	26	N. C
27	₇BHEN	28	₇ADR 10
29	₇CBRQ	30	₇ADR 11
31	₇CCLK	32	₇ADR 12
33	₇INTA	34	₇ADR 13
35	₇INT 6	36	₇INT 7
37	₇INT 4	38	₇INT 5
39	₇INT 2	40	₇INT 3
41	₇INT 0	42	₇INT 1
43	₇ADR E	44	₇ADR F
45	₇ADR C	46	₇ADR D
47	₇ADR A	48	₇ADR B
49	₇ADR 8	50	₇ADR 9
51	₇ADR 6	52	₇ADR 7
53	₇ADR 4	54	₇ADR 5
55	₇ADR 2	56	₇ADR 3
57	₇ADR 0	58	₇ADR 1
59	₇DAT E	60	₇DAT F
61	₇DAT C	62	₇DAT D
63	₇DAT A	64	₇DAT B
65	₇DAT 8	66	₇DAT 9
67	₇DAT 6	68	₇DAT 7
69	₇DAT 4	70	₇DAT 5
71	₇DAT 2	72	₇DAT 3
73	₇DAT 0	74	₇DAT 1
75	0 VOLT	76	0 VOLT
77	N. C	78	N. C
79	- 12 VOLT	80	- 12 VOLT
81	+ 5 VOLT	82	+ 5 VOLT
83	+ 5 VOLT	84	+ 5 VOLT
85	0 VOLT	86	0 VOLT



PIN ASSIGNMENT FOR P1 AND P2

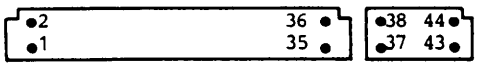
840827 VH/CU 841030 AMS

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	0 VOLT	2	0 VOLT
3		4	
5		6	
7		8	
9		10	
11		12	
13		14	
15		16	
17		18	
19		20	
21	0 VOLT	22	0 VOLT
23		24	
25		26	
27		28	
29		30	
31		32	
33		34	
35		36	
37		38	
39		40	
41		42	
43		44	
45		46	
47		48	
49		50	
51		52	
53		54	
55	₇ADR 16	56	₇ADR 17
57	₇ADR 14	58	₇ADR 15
59		60	

840827 VH/CU 841030 AMS

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	+ 12 VOLT	2	- 12 VOLT
3	0 VOLT	4	+ 5 VOLT
5	RESET	6	MCLK
7	MA 2	8	₇MPST
9	MA 1	10	N. C
11	MA 0	12	MINTR 1
13	₇IOWRT	14	MINTR Ø
15	₇IORD	16	₇MWAIT
17	0 VOLT	18	+ 5 VOLT
19	MD 7	20	₇MCS 1
21	MD 6	22	₇MCS Ø
23	MD 5	24	N. C
25	MD 4	26	N. C
27	MD 3	28	OPT 1
29	MD 2	30	OPT Ø
31	MD 1	32	₇MDACK
33	MD 0	34	MDRQT
35	0 VOLT	36	+ 5 VOLT
37	MD E	38	MD F
39	MD C	40	MD D
41	MD A	42	MD B
43	MD 8	44	MD 9

N.C = NO CONNECTION

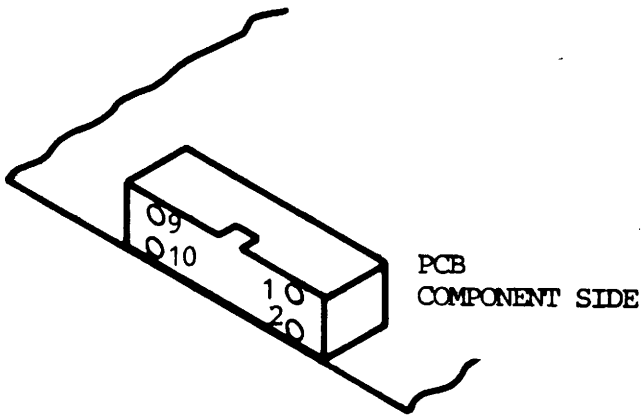


J1 PIN ASSIGNMENT TOP VIEW (SEEN FROM COMPONENT SIDE)

840827 VH/CU 841030 AMS

PIN NUMMER	SIGNAL NAME
1	LED 0 CATHODE
2	LED 0 ANODE
3	LED 1 CATHODE
4	LED 1 ANODE
5	LED 2 CATHODE
6	LED 2 ANODE
7	LED 3 CATHODE
8	LED 3 ANODE
9	N. C
10	N. C

N. C = NO CONNECTION

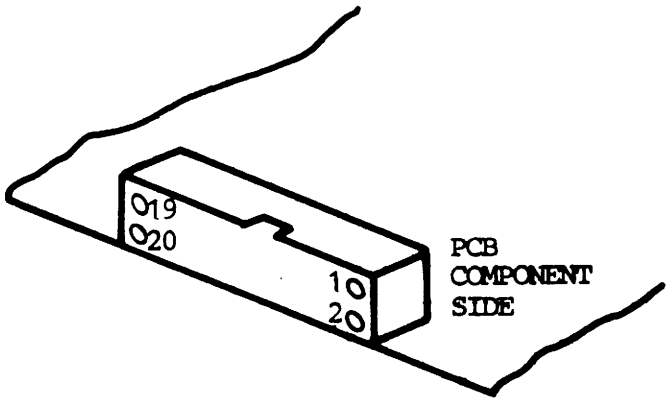


J2 PIN ASSIGNMENT

840827 VH/CU 841030 AMS

PIN NUMBER	SIGNAL NAME
1	0 VOLT
2	N.C
3	N.C
4	N.C
5	0 VOLT
6	N.C
7	CALLING INDICATOR B (125)
8	CARRIER DET B (109)
9	0 VOLT
10	DATA TERM. RDY B (108)
11	0 VOLT
12	DATA SET READY B (107)
13	0 VOLT
14	CLEAR TO SEND B (106)
15	0 VOLT
16	REQ. TO SEND B (105)
17	0 VOLT
18	₇REC. DATA B (104)
19	0 VOLT
20	₇TRANSM. DATA B (103)

N.C = NO CONNECTION



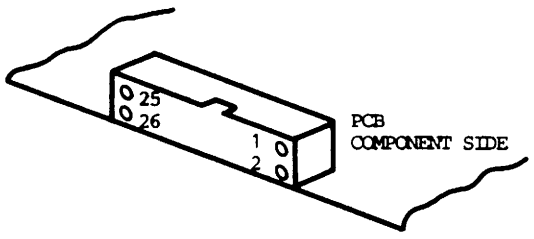
J3 PIN ASSIGNMENT

840827 VH/CU 841029 AMS

*: X.21 SIGNALS

**: WHEN TIED TO 0 VOLT THE X.21 INTERFACE CIRCUITS ARE SELECTED.

PIN NUMBER	SIGNAL NAME	
1	0 VOLT	
2	CB	*
3	₇TRANSM. DATA A (103)	
4	TRM. CLOCK A IN (114)	
5	₇REC. DATA A (104)	
6	SB	*
7	REQ. TO SEND A (105)	
8	REC. CLOCK A IN (115)	
9	CLEAR TO SEND A (106)	
10	SA	*
11	DATA SET READY A (107)	
12	RB	*
13	0 VOLT	
14	DATA TERM. RDY A (108)	
15	CARRIER DET. A (109)	
16	RA	*
17	TA	*
18	CALLING INDICATOR A (125)	
19	IA	*
20	RECEIVE CLOCK A OUT	
21	₇X.21 SEL	**
22	IB	*
23	TB	*
24	CA	*
25	TRANSM. CLOCK A OUT	
26	NO CONNECTION	

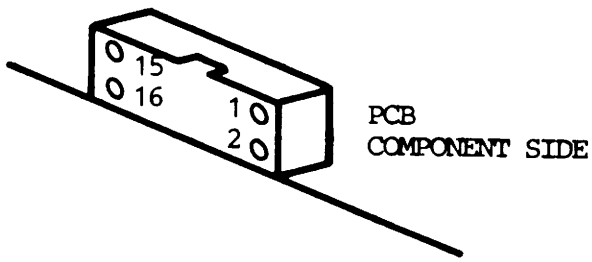


J4 PIN ASSIGNMENT

PIN NUMBER	SIGNAL NAME
1	SHIELD*
2	COLLISION PRESENCE (+)
3	TRANSMIT(+)
4	N. C
5	RECEIVE(+)
6	0 VOLT
7	N. C
8	N. C
9	COLLISION PRESENCE (-)
10	TRANSMIT(-)
11	N. C
12	RECEIVE (-)
13	+ 12 VOLT
14	N. C
15	N. C
16	SHIELD*

N. C. = NO CONNECTION
* CAN BE TIED TO 0 VOLT BY USE OF ONBOARD JUMPER S27

840827 VH/CU 841030 AMS



J5 PIN ASSIGNMENT

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(5) CCITT YELLOW BOOK, VOL. VIII-Fascicle VIII.1.

(6) Intel Systems Data Catalog 1982.

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(8) MSI601 Hardware Reference Manual
RCSL No. 99 0 00774.

(9) MEX601/611 Hardware Reference Manual
RCSL No. 99 0 00773.

B. INDICES B.

B.1 Survey of Figures B.1

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